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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Intel Corporation
Petitioner

v.

VLSI Technology, LLC
Patent Owner

Case IPR2019-01194

PETITIONER'S NOTICE OF APPEAL

U.S. PATENT NO. 8,081,026
CHALLENGING CLAIMS 1, 2, 4, 5, and 7

Pursuant to 35 U.S.C. §§ 141-144 and 319, 5 U.S.C. §§ 701-706, 28 U.S.C. § 1295(a)(4)(A), and 28 U.S.C. § 1651, and 37 C.F.R. § 90.2-90.3, notice is hereby given that Petitioner Intel Corporation appeals to the U.S. Court of Appeals for the Federal Circuit from the Final Written Decision entered January 12, 2021 (Paper 29) in IPR2019-01194, attached as Exhibit A, and all prior and interlocutory rulings related thereto or subsumed therein.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Petitioner indicates that the issues for appeal include the holding that claims 4, 5, and 7 of the '026 patent are not unpatentable, as well as all other issues decided adversely to Petitioner in any orders, decisions, rulings, and opinions.

This Notice of Appeal is timely, having been duly filed within 63 days after the date of the Final Written Decision.

A copy of this Notice of Appeal is being filed simultaneously with the Patent Trial and Appeal Board, the Clerk's Office for the United States Court of Appeals for the Federal Circuit, and the Director of the U.S. Patent and Trademark Office.

Dated: March 15, 2021

Respectfully Submitted,

/Dominic Massa/
Dominic Massa, Reg. No. 44,905

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 90.2(a)(1) and 104.2(a), I hereby certify that, in addition to being filed electronically through the Patent Trial and Appeal Board's End to End (PTAB E2E), a true and correct original version of the foregoing PETITIONER'S NOTICE OF APPEAL is being filed by Express Mail on this 15th day of March, 2021, with the Director of the United States Patent and Trademark Office, at the following address:

Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to 37 C.F.R. § 90.2(a)(2) and Federal Circuit Rule 15(a)(1), and Rule 52(a),(e), I hereby certify that a true and correct copy of the foregoing PETITIONER'S NOTICE OF APPEAL is being filed in the United States Court of Appeals for the Federal Circuit using the Court's CM/ECF filing system on this 15th day of March, 2021, and the filing fee is being paid electronically using pay.gov.

I hereby certify that on March 15, 2021, I caused a true and correct copy of the following materials:

- PETITIONER'S NOTICE OF APPEAL

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Exhibit A

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Paper 29
Date: January 12, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2019-01194
Patent 8,081,026 B1

Before BART A. GERSTENBLITH, MINN CHUNG, and KIMBERLY McGRAW, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Intel Corporation ("Petitioner") challenges the patentability of claims 1, 2, 4, 5, and 7 (the "challenged claims") of U.S. Patent No. 8,081,026 B1 (Ex. 1001, "the '026 patent"), owned by VLSI Technology LLC ("Patent Owner"). This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1 and 2 of the '026 patent are unpatentable, but has not proven by a preponderance of the evidence that claims 4, 5, and 7 of the '026 patent are unpatentable.

II. BACKGROUND

A. Procedural History

On June 28, 2019, Petitioner filed a Petition (Paper 3, "Pet.") requesting *inter partes* review of the challenged claims of the '026 patent. Patent Owner filed a Preliminary Response (Paper 7, "Prelim. Resp."). Petitioner then filed an authorized reply to address Patent Owner's arguments in the Preliminary Response regarding discretion under 35 U.S.C. § 314(a) (Paper 9), to which Patent Owner filed an authorized sur-reply (Paper 10).

On January 13, 2020, applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we instituted an *inter partes* review of all challenged claims of the '026 patent based on the ground presented in the Petition. Paper 11 ("Inst. Dec."), 66.

After institution, Patent Owner filed a Patent Owner Response (Paper 15, "PO Resp."), Petitioner filed a Reply to Patent Owner Response (Paper 17, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 24, "PO Sur-reply"). An oral hearing was held on October 6, 2020, and a copy of the hearing transcript has been entered into the record. Paper 28 ("Tr.").

B. Related Matters

According to the parties, the '026 patent is the subject of the following district court litigation: *VLSI Technology LLC v. Intel Corp.*, No. 18-966-CFC (D. Del.). Pet. 2; Paper 6, 2. Petitioner also filed a petition for *inter partes* review in IPR2019-01195, challenging claims 13, 14, 17, 18, and 20 of the '026 patent. Pet. 2; Paper 6, 2. We instituted trial in IPR2019-01195 on January 13, 2020. IPR2019-01195, Paper 11.

C. The '026 Patent

The '026 patent describes supplying an output supply voltage to a power gated circuit included in an integrated circuit. Ex. 1001, 1:7–9. As background, the '026 patent describes that seemingly identical integrated circuits fabricated using the same design may actually differ from each other due to variations in the semiconductor manufacturing process. *Id.* at 1:13–22. For example, ideally identical integrated circuits may differ in their operating speed, some being faster than others. *Id.* at 1:20–22. In view of the variations in the manufacturing process, the fastest circuits are considered "best process case" integrated circuits, whereas the slowest circuits are deemed "worst process case" integrated circuits. *Id.* at 1:23–30. According to the '026 patent, faster circuits generally have higher leakage current (*id.* at 1:20–23), which means that the fastest integrated circuits have

the highest leakage current and the slowest integrated circuits have the lowest leakage current (*id.* at 1:27–30). The '026 patent describes that, as a result of this direct correspondence between the speed of the circuits and the amount of leakage current, the competing or conflicting requirements of high speed and low current consumption for integrated circuits can reduce the yield of the manufacturing process because some circuits may satisfy the speed requirements but have too high current consumption, whereas other circuits may comply with the current consumption requirements but are too slow to meet the speed requirements. *Id.* at 1:34–40.

According to the '026 patent, applying a lower supply voltage to an integrated circuit reduces both the speed and the current leakage of the circuit, which may allow a very fast integrated circuit that was rejected for being too leaky to have acceptable performance ranges for both speed and current consumption, thereby increasing the yield of the semiconductor manufacturing process. *Id.* at 3:4–11.

Figure 1 of the '026 patent is reproduced below.

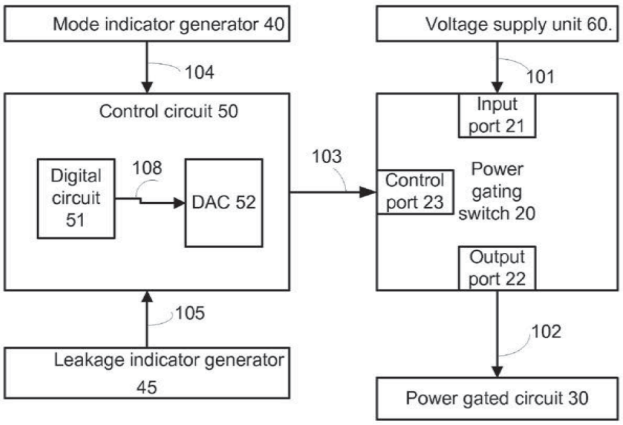


FIG. 1

Figure 1 schematically shows a block diagram of an exemplary integrated circuit. *Id.* at 1:62–63.

As shown in Figure 1, integrated circuit 10 includes power gated circuit 30, power gating switch 20, and control circuit 50 for controlling power gating switch 20 by selecting control signal 103 that determines the conductivity of the power gating switch. *Id.* at 2:40–44. According to the '026 patent, this conductivity determines the difference between input supply voltage 101 provided to power gating switch 20 and output supply voltage 102 that is provided to power gated circuit 30 from power gating switch 20. *Id.* at 2:44–54.

Integrated circuit 10 also includes mode indicator generator 40 and leakage indicator generator 45. *Id.* at 3:35–37. The '026 patent describes that mode indicator generator 40 generates mode indicator 104 that indicates a desired mode of power gated circuit 30 (*id.* at 3:39–41) and leakage indicator generator 45 generates leakage indicator 105 that indicates a leakage level of power gated circuit 30 (*id.* at 3:46–48). As depicted in Figure 1, control circuit 50 receives mode indicator 104 and leakage indicator 105. *Id.* at 4:4–7. According to the '026 patent, control circuit 50 can select the value of control signal 103 based on mode indicator 104 and on leakage indicator 105. *Id.* at 4:7–9.

The '026 patent describes that leakage indicator generator 45 can comprise a memory in which a leakage level value is stored during the manufacturing process of integrated circuit 10 or during a leakage test conducted after the production of integrated circuit 10. *Id.* at 3:48–52. According to the '026 patent, leakage indicator generator 45 can include "fuses, one time programmable element or other programmable elements that can be programmed to reflect the determined leakage." *Id.* at 3:61–64. The '026 patent describes that leakage indicator 105 can indicate whether

integrated circuit 10 has a leakage level that corresponds to a best process case, typical process case, or worst process case. *Id.* at 3:64–67.

As described in the ’026 patent, power gated circuit 30 can operate in at least the following modes: (i) a performance oriented mode (also referred to as high throughput mode or high performance mode), (ii) a retention mode, and (iii) a power gated mode. Ex. 1001, 2:57–60. The ’026 patent describes that, during the retention mode, power gated circuit 30 can store data in retention circuits and consume less power in comparison to the performance oriented mode, whereas, during the power gated mode, power gated circuit 30 is shut down and data is not retained. *Id.* at 2:63–67. The ’026 patent notes that additional modes can exist in which a different trade-off between speed and leakage can be provided. *Id.* at 2:60–62.

The ’026 patent describes that control circuit 50 can select a performance value for control signal 103 when (i) leakage indicator 105 indicates that a leakage of power gated circuit 30 is below a low leakage threshold and (ii) mode indicator 104 indicates that power gated circuit 30 is requested to operate at a performance oriented mode. *Id.* at 4:30–37. Control circuit 50 can also be arranged to select a leakage reduction value of control signal 103 suitable to reduce leakage while allowing power gated circuit 30 to operate in performance mode when (i) leakage indicator 105 indicates that the leakage of power gated circuit 30 is above the low leakage threshold and (ii) mode indicator 104 indicates that power gated circuit 30 is requested to operate at the performance oriented mode. *Id.* at 4:38–45. The performance value of the control signal causes a higher conductivity of power gating switch 20, with a smaller difference between the values of

input supply voltage 101 and output supply voltage 102 than the leakage reduction value of the control signal. *Id.* at 5:10–14.

According to the '026 patent, the low leakage threshold assists in differentiating between integrated circuits of different types in that faster integrated circuits will receive lower output supply voltage levels. *Id.* at 4:46–48. The value of the low leakage threshold can be based on a desired speed of the integrated circuit and on leakage limitations. *Id.* at 4:49–51.

The '026 patent describes that control circuit 50 can be arranged to select a retention value of the control signal 103 when mode indicator 104 indicates that power gated circuit 30 is requested to enter a retention mode and select a shut-down value of control signal 103 when mode indicator 104 indicates that power gated circuit 30 should be shut down. *Id.* at 5:3–9.

D. Illustrative Claims

Of the challenged claims, only claim 1 is independent. Claims 1 and 2 are illustrative of the challenged claims and are reproduced below.

1. An integrated circuit, comprising:

a power gating switch, the switch comprises:

an input port for receiving an input supply voltage;

an output port for providing an output supply voltage to a power gated circuit; and

a control port for receiving a control signal that determines a difference between the input supply voltage and the output supply voltage;

wherein the integrated circuit further comprising the power gated circuit, being gated relative to the input supply voltage by the switch, the power gated circuit being coupled to the output port of the switch for receiving the output supply voltage;

a mode indicator generator for generating a mode indicator that indicates a desired mode of the power gated circuit;

a leakage indicator generator for generating a leakage indicator that indicates a leakage level of the power gated circuit; and

a control circuit, connected to the mode indicator generator and the leakage indicator generator, for receiving the mode indicator and the leakage indicator, the control circuit being arranged to select the value of the control signal based on the mode indicator and on the leakage indicator.

Ex. 1001, 15:10–33.

2. The integrated circuit according to claim 1, wherein the control circuit is arranged to:

select a performance value of the control signal when (i) the leakage indicator indicates that a leakage of the power gated circuit is below a low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at a performance oriented mode;

select a leakage reduction value of the control signal when (i) the leakage indicator indicates that the leakage of the power gated circuit is above the low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at the performance oriented mode; and

select a shut down value of the control signal when the mode indicator indicates that the power gated circuit should be shut down.

Id. at 15:34–50.

E. Applied References and Asserted Ground of Unpatentability

Petitioner relies upon the following references in its challenge to patentability.

Reference and Date	Designation	Exhibit No.
U.S. Patent Application Publication No. 2008/0136507 A1 (published June 12, 2008)	Kim	1004
U.S. Patent Application Publication No. 2007/0147159 A1 (published June 28, 2007)	Lee	1005

Petitioner asserts the following ground of unpatentability.

Claims Challenged	35 U.S.C. §	References/Basis
1, 2, 4, 5, 7	103(a)[1]	Kim, Lee

Pet. 6.

F. Testimonial Evidence

Petitioner relies on two Declarations from David Harris, Ph.D. in support of its Petition and Reply. Ex. 1002 ("Harris Declaration"); Ex. 1030 ("Harris Reply Declaration"). Patent Owner cross-examined Dr. Harris via deposition. Ex. 2010 ("Harris Dep.").

In support of its Patent Owner Response, Patent Owner relies on the Declaration of Professor Murali Annavaram. Ex. 2009 ("Annavaram

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. § 103. Because the '026 patent has an effective filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

Declaration"). Petitioner cross-examined Dr. Annavaram by deposition. Ex. 1031 ("Annavaram Dep.").

III. ANALYSIS

A. Level of Ordinary Skill in the Art

We begin our analysis by addressing the level of ordinary skill in the art. Citing the testimony of its declarant, Dr. Harris, Petitioner asserts that a person of ordinary skill in the art at the time of the invention of the '026 patent would have had a Master's degree in Electrical Engineering or Computer Engineering, plus at least two years of experience in integrated circuit design, or alternatively a Bachelor's degree in one of those fields plus at least four years of experience in integrated circuit design. Pet. 16 (citing Ex. 1002 ¶ 49). In our Institution Decision, we found Petitioner's proposal consistent with the level of ordinary skill in the art reflected by the prior art of record, *see Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978), and, therefore, preliminarily adopted Petitioner's unopposed position as to the level of ordinary skill in the art. Inst. Dec. 15.

Neither Patent Owner, in its Response, nor Dr. Annavaram, in his declaration, proposes a level of ordinary skill in the art. Instead, Patent Owner states that "Patent Owner applies Petitioner's stated skill level for this response" (PO Resp. 25), and Dr. Annavaram similarly states that "[f]or the purpose of this declaration, I adopt Dr. Harris' definition of a [person of ordinary skill in the art]" (Ex. 2009 ¶ 24).

Nothing in the full record persuades us that our preliminary finding as to the level of ordinary skill in the art was incorrect. Based on the complete record, because our preliminary finding is consistent with the level of

ordinary skill in the art reflected by the prior art of record, we maintain and reaffirm that one of ordinary skill in the art at the time of the invention would have had a Master's degree in Electrical Engineering or Computer Engineering, plus at least two years of experience in integrated circuit design, or alternatively a Bachelor's degree in one of those fields plus at least four years of experience in integrated circuit design. Inst. Dec. 15; *see* Pet. 16 (citing Ex. 1002 ¶ 49).

B. Claim Construction

In an *inter partes* review, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), following the standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

In the Petition, Petitioner asserts that no express constructions are necessary in this proceeding. Pet. 15–16. Petitioner also notes that the parties in the related district court litigation did not propose constructions for any claim terms from the '026 patent. *Id.* at 16.

In our Decision on Institution, we rejected Patent Owner's argument that claim 2 requires the control circuit to "select *among*" "a performance value of the control signal," "a leakage reduction value of the control signal," and "a shut down value of the control signal." Dec. Inst. 60–62 (citing Prelim. Resp. 53; Ex. 2007, 1578). We noted that claim 2 does not recite selecting *among* the three recited values. *Id.* at 60. We were not persuaded by Patent Owner's citation to a general dictionary definition of "select" as to "*take a choice from among several*; pick out," citing to other general dictionary definitions that did not recite "*among*." *Id.* at 61 (citing Ex. 3002, 1; Ex. 3003, 1017).

In its Patent Owner Response, Patent Owner proposes a construction for only one term—"select"—recited in all challenged claims. PO Resp. 25–32. Citing dictionary definitions (Ex. 3002;[2] Ex. 2007), Patent Owner asserts that the term "select" should be construed to mean "[t]o choose or pick out in preference to another or others," which requires "a set of more than one item be available from which one or more items are chosen in preference to another or others." *Id.* at 25–27 (citing Ex. 3002; Ex. 2007; Ex. 2009 ¶ 67; Inst. Dec. 61). Patent Owner further contends that the term

[2] Oxford English Dictionary (Ex. 3002), available at https://www.oed.com/view/Entry/175028?isAdvanced=false&result=2&rskey=LW57Dp&.

"select" should be accorded the same meaning in each claim because "claim terms are normally used consistently throughout the patent." *Id.* at 27 (quoting *Phillips*, 415 F.3d at 1314). As a corollary, Patent Owner argues that an alternative dictionary definition (Ex. 3003)[3] discussed in the Institution Decision (Inst. Dec. 61), "[t]o identify, within a set of items, all items that meet a particular criterion," should be rejected because the definition is inconsistent with the language of claim 4, which requires "select[ing] the leakage reduction value *out of a group* of leakage reduction values." *Id.* at 26–27 (emphasis added) (citing Ex. 3003; Ex. 1001, 15:55–59).

Petitioner replies that no express construction is necessary and that the term "select" should be accorded its plain and ordinary meaning. Pet. Reply 3–4. Petitioner also argues that the definition of "select" provided by Exhibit 3003 should not be excluded from the scope of the claims. *Id.* at 4.

As an initial matter, we note that the definitions from the dictionaries discussed above indicate that "to select" or "selecting" something generally involves choosing or picking out something. *See* Ex. 2007, 1578 (defining "select" as "[t]o take as a *choice* from among several; *pick out*" (emphases added)); Ex. 3002, 1 (defining "select" as "[t]o *choose* or *pick out* in preference to another or others" (emphases added)); Ex. 3003, 1017 (defining "select" as "[t]o *identify*, within a set of items, all items that meet a particular criterion" (emphasis added)). As discussed below, "select," as recited in the challenged claims, also involves choosing or picking out something at a general level.

[3] IEEE 100 THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS (7th ed. 2000) (Ex. 3003).

But our analysis does not stop there because the challenged claims do not merely recite selecting something in general. Rather, the challenged claims recite more particularized selection clauses by setting forth specific limitations that modify the recitation of "select" each claim. For example, claim 1 recites that the control circuit is arranged to "select" the value of the control signal "based on" the mode indicator and on the leakage indicator. Ex. 1001, 15:30–33. Claim 2, on the other hand, recites that the control circuit is arranged to "select" a performance value, a leakage reduction value, and a shut down value "when" the conditions recited for one of the values are met. *Id.* at 15:34–33. Claim 4 recites that the control circuit is arranged to "select" the leakage reduction value "out of a group" of leakage reduction values. *Id.* at 15:55–57.

To the extent Patent Owner argues that these particularized selection clauses recited in different claims must have the same or similar meaning because they all use the word "select" (*see* PO Resp. 27), we disagree with Patent Owner. *See IGT v. Bally Gaming Int'l, Inc.*, 659 F.3d 1109, 1117 (Fed. Cir. 2011) ("We caution that claim language must be construed in the context of the claim in which it appears. *Extracting a single word from a claim divorced from the surrounding limitations can lead construction astray*. Claim language must be construed in the claim in which it appears." (emphasis added)). The selection clauses recited in these claims are plainly different on the face of the claims when considering the material differences in the claim language set forth above. According the same meaning to the limitations that recite "select . . . based on" indicators, "select . . . when" certain conditions are met, and "select . . . out of a group" of values would be improper because it would blur the material differences in the claim

language recited expressly in the claims. Instead, we interpret the selection clauses recited in the challenged claims "in the context of the particular claim in which the disputed term appears" and "in the context of the entire patent, including the specification." *Phillips*, 415 F.3d at 1313. In other words, we do not construe the single word "select" in isolation, but, rather, interpret the full selection clauses recited in the challenged claims in the context of the entire patent.

Claim 1 requires that the control circuit is arranged to "select the value of the control signal based on the mode indicator and on the leakage indicator." In our view, the plain meaning of this limitation is clear on the face of the claim—the value of the control signal is selected based on two indicators, the mode indicator and the leakage indicator.

The plain meaning of the term is supported by the Specification of the '026 patent, which states:

> The control circuit 50 is connected to the leakage indicator generator for receiving the mode indicator 104. The control circuit is further connected to the mode indicator generator 40, for receiving the leakage indicator 105. The control circuit 50 can *select the value of the control signal* 103 *based on the mode indicator 104 and on the leakage indicator 105*. The control circuit 50 can output a *control signal* 103 that has a *value* that is *determined* based on one or more indicators.

Ex. 1001, 4:4–11 (emphases added). Thus, at least in this example, the Specification indicates that "select[ing] the value of the control signal based on the mode indicator and on the leakage indicator" recited in claim 1 is synonymous to *determining* the value based on the recited indicators. Determining the value of the control signal based on the mode indicator and on the leakage indicator, as described in the Specification, is consistent with

the plain meaning of the claim language—i.e., the value of the control signal is selected based on the mode indicator and on the leakage indicator.

Although Patent Owner proposes to construe "select" as "[t]o choose or pick out in preference to another or others" (PO Resp. 25–26), Patent Owner also asserts that "select[ing] the value of the control signal based on the mode indicator and on the leakage indicator" recited in claim 1 requires the indicators to "play a role in deciding *which of the multiple values* will be chosen or picked" (*id.* at 31 (emphasis added)). To the extent Patent Owner argues claim 1's selecting a value "based on the mode indicator and on the leakage indicator" requires selecting a value from or among a group of multiple values, we disagree with Patent Owner's argument.[4] As noted above, claim 4 recites that the control circuit is arranged to select a value "out of a group of" values. This shows that the patentee knew how to use the words selecting out of a group of values to describe the selection recited in claim 4. If the patentee had intended to similarly describe the selection recited in claim 1, it could have done so using the language of claim 4, but did not. *See Intellectual Ventures I LLC v. T-Mobile USA, Inc.*, 902 F.3d 1372, 1379 (Fed. Cir. 2018) (citing *Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1359 (Fed. Cir. 2016)). We disagree with the "[selecting from among] multiple values" aspect of Patent Owner's construction because it would blur the material differences in the claim language of claim 1 and claim 4 discussed above.

[4] As discussed above, Patent Owner notes that the dictionary definition it proposed in the Preliminary Response for "select" was "to take as a choice from *among several*." PO Resp. 25–26 (emphasis added) (citing Ex. 2007).

In support of its argument, Patent Owner cites Figures 3 and 4 of the '026 patent, which, according to Patent Owner, describe "different curves correlating the level of control signals and the supply voltage as a function of the process conditions (which indirectly indicates a leakage level and is therefore a leakage indicator), the mode of operation (retention mode versus *performance-oriented mode*) and temperature." PO Resp. 31 (emphasis added) (citing Ex. 1001, 5:55–9:37, Figs. 3, 4). Patent Owner further asserts that "when a mode indicator indicates a *performance oriented mode*, curves in Figure 3 will be referenced" and that "[t]he appropriate value or level of the control signal will then be read from the chosen curves and be selected accordingly." *Id.* (emphasis added) (citing Ex. 2009 ¶ 81). Patent Owner argues "[i]n this selection process, both the mode indicator and the leakage indicator *affect* which curve(s) will be selected and which associated value of the control signal will be picked in the end." *Id.* (emphasis added) (citing Ex. 2009 ¶ 81; Ex. 1001, 5:48–51).

The term "performance oriented mode," however, is recited in claim 2, not in claim 1. As discussed above, claim 2 depends from claim 1 and recites additional selections the control circuit is arranged to make, including selecting "a performance value of the control signal when (i) the leakage indicator indicates that a leakage of the power gated circuit is below a low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at a *performance oriented mode*." Ex. 1001, 15:36–41 (emphasis added). Again, Patent Owner does not explain adequately why the subject matter of the selection recited in claim 2 is the same as or is included in the subject matter of the selection recited in claim 1, despite the material differences in the claim language on the face of

the claims discussed above. Accordingly, we disagree with Patent Owner's argument that claim 1 *requires* the mode indicator and the leakage indicator to "play a role in deciding which of the multiple values will be chosen or picked" *in the manner recited in claim 2 or described in the embodiment of Figure 3* of the '026 patent. *See* PO Resp. 31.

Nonetheless, to the extent Patent Owner's proposed definition indicates that selecting a value "based on" indicators involves "deciding" a value to choose or pick based on indicators, we agree with Patent Owner because this aspect of Patent Owner's proposed construction is consistent with the Specification's description of "select[ing] the value of the control signal based on the mode indicator and on the leakage indicator" as *determining* the value based on the recited indicators.

Other than finding that the selection clause recited in claim 1 encompasses determining the value of the control signal based on the mode indicator and on the leakage indicator, for purposes of this Final Written Decision, we need not provide an express construction for other terms within claim 1's selection clause—"select the value of the control signal based on the mode indicator and on the leakage indicator." *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that only terms that are in controversy need to be construed, and "only to the extent necessary to resolve the controversy"); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

Turning next to claim 2, the claim recites:

> 2. The integrated circuit according to claim 1, wherein the control circuit is arranged to:
>
> select a performance value of the control signal when (i) the

> leakage indicator indicates that a leakage of the power gated circuit is below a low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at a performance oriented mode;
>
> select a leakage reduction value of the control signal when (i) the leakage indicator indicates that the leakage of the power gated circuit is above the low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at the performance oriented mode; and
>
> select a shut down value of the control signal when the mode indicator indicates that the power gated circuit should be shut down.

Ex. 1001, 15:34–50.

In the Institution Decision, although we determined that we need not expressly construe any claim term for purposes of deciding whether to institute a review (Inst. Dec. 17), we addressed Patent Owner's apparent or implicit claim construction argument that claim 2 requires the control circuit to "select *among*" or "select *between*" "a performance value of the control signal," "a leakage reduction value of the control signal," and "a shut down value of the control signal." *Id.* at 60–62 (emphases added) (citing Prelim. Resp. 53). Considering the claim language, we noted that claim 2 does *not* recite selecting "among" a performance value, a leakage reduction value, and a shut down value. *Id.* at 60. Rather, the claim merely recites the control circuit is arranged to "select a performance value of the control signal," "select a leakage reduction value of the control signal," and "select a shut down value of the control signal." *Id.* (citing Ex. 1001, 15:34–50). We also found that the plain meaning of the claim language, "selecting" a value "when" the recited conditions are met, is consistent with the written description in the Specification. *Id.* at 61–62 (citing Ex. 1001, 4:30–45, 5:3–

9). In addition, we noted that the plain language of the claim appears to be consistent with the definition from an IEEE dictionary that defines "select" as "[t]o identify, within a set of items, all items that meet a particular criterion." *Id.* at 61 (citing Ex. 3003, 1017).

At trial, Patent Owner does not argue claim 2 requires "selecting among" the three types of control signal values recited in claim 2. *See generally* PO Resp. Thus, nothing in the full record persuades us that our preliminary construction of claim 2 was incorrect. Based on the complete record, we determine that claim 2 does *not* require the control circuit to "select *among*" "a performance value of the control signal," "a leakage reduction value of the control signal," and "a shut down value of the control signal."

In the Patent Owner Response, Patent Owner asserts that the IEEE dictionary definition conflicts with the language of claim 4, which depends from claim 2 and additionally recites "wherein the control circuit is arranged to *select* the leakage reduction value *out of a group* of leakage reduction values . . . ." PO Resp. 26–27 (emphasis added) (citing Ex. 1001, 15:55–59). In the Institution Decision, we considered the IEEE definition to interpret the selection clause recited in claim 2, not claim 4. *See* Inst. Dec. 53–65. As discussed above, we disagree with Patent Owner that selection clauses recited in different challenged claims must have the same or similar meaning. Claim 2 recites that the control circuit is arranged to "select" a performance value, a leakage reduction value, and a shut down value "when" the conditions recited for each value are met. Ex. 1001, 15:34–33. Claim 4, on the other hand, additionally requires that the control circuit is arranged to "select" the leakage reduction value "out of a group" of leakage

reduction values. *Id.* at 15:55–57. The selection clauses recited in these claims are plainly different on the face of the claims when considering the material differences in the claim language set forth above. Patent Owner does not explain adequately why the selection clauses recited in claim 2 must have the same meaning as the selection clause recited in claim 4 despite the material differences in the language of the claims.

To the extent Patent Owner implicitly argues that the selection clause recited in claim 2 must encompass the selection clause recited in claim 4, which depends from claim 2, we disagree with Patent Owner's argument. *See* PO Resp. 26–27. As noted above, claim 4 recites an *additional*, different selection clause than the selection clause recited claim 2. As such, claim 4 does not recite a restricted version of either claim 1's or claim 2's selection clause but, instead, recites an additional selection the control circuit is arranged to make.

Although claim 1 is presumed to be broader than its dependent claims 2 and 4, *see Trustees of Columbia Univ. v. Symantec Corp.*, 811 F.3d 1359, 1370 (Fed. Cir. 2016), *but cf. ERBE Elektromedizin GmbH v. Canady Tech. LLC*, 629 F.3d 1278, 1286 (Fed. Cir. 2010) ("no canon of [claim] construction is absolute in its application") (citation omitted), that does not necessary mean that a particular limitation recited in claim 1 encompasses the additional limitation recited in dependent claims 2 or 4. As discussed below in Section III.C.5, we interpret the phrase "the control circuit [is] arranged to select" a value recited in the challenged claims to mean that the recited control circuit is capable of making the recited selection. Thus, the dependent challenged claims recite additional selections the control circuit is capable of making in addition to the selections recited in the base claims

from which they depend. That is, the dependent claims recite *additional* requirements of the recited control circuit, not necessarily a restricted version of the selection methods recited in the base claims from which they depend. Thus, the selection clause recited in claim 1 need not encompass the selection clauses recited in the dependent claims that depend from claim 1 (and the selection clauses recited in claim 2 need not encompass the selection clause recited in claim 4, which depends from claim 2) unless the claim language and the Specification indicate such relationship.

Because the selection clauses recited in these claims are plainly different on the face of the claims, there is nothing in the claim language that indicates that the recited selection clauses must be the same or that the selection clause recited in dependent claim 4 is encompassed in the selection clause recited in claim 4's base claim 2. Patent Owner does not explain adequately why the selection clauses recited in these claims should be considered to be the same or similar despite the material differences in the claim language on the face of the claims. The alleged "conflict" argued by Patent Owner simply reflects the patentee's choice to recite a different selection the control circuit is capable of making in claim 4 from the recited selection the control circuit is capable of making in claim 2.

In our view, the plain meaning of the additionally recited limitations of claim 2 is clear on the face of the claim—the control circuit is arranged such that a performance value, a leakage reduction value, and a shut down value of the control signal are selected "when" the conditions recited in the

limitations are met.[5] Similar to our analysis of claim 1, we perceive no ambiguities in the claim language that require an express construction of the limitations recited in claim 2.

Petitioner asserts that the definition of "select" from an IEEE dictionary discussed in the Institution Decision—"[t]o identify, within a set of items, all items that meet a particular criterion"—is consistent with the plain meaning of claim 2. Pet. Reply 3–5 (citing Ex. 3003; Inst. Dec. 61). We agree with Petitioner. Considering the language of claim 2 that recites "select[ing]" a performance value, a leakage reduction value, and a shut down value "when" the conditions recited in the limitations are met, we find that the plain language of the claim 2's selection clause is consistent with the IEEE dictionary definition of "select" as "[t]o identify, within a set of items, all items that meet a particular criterion." *See* Ex. 3003, 1017.

Patent Owner also asserts that the aspect of the IEEE dictionary definition that states "select" means identifying "all items" that meet a particular criterion conflicts with the language of claim 4 because claim 4 recites selecting a value "out of a group" of values, not *all* values that meet a condition. PO Resp. 26–27. We, however, do *not* interpret claim 2 as selecting "all items" that meet the recited conditions. As discussed above, the plain meaning of claim 2's selection clauses is "selecting" ***a*** *value*—i.e., "a performance value," "a leakage reduction value," and "a shut down value"—of the control signal "when" the recited conditions are met. Thus, the plain language of claim 2 is consistent with the aspect of the IEEE

[5] The parties do not argue the terms "performance value," "leakage reduction value," or "shut down value" are ambiguous, nor do the parties propose constructions for these terms.

dictionary definition to the extent the dictionary defines "select" as "identify[ing]" or picking "an item" that "meets a particular criterion." We did not suggest adopting in our Institution Decision, nor do we adopt for this Final Written Decision the choosing "all items" aspect of the IEEE dictionary.

Turning to the Specification, the '026 patent describes as follows:

> [T]he control circuit 50 may *select the performance value* of the control signal 103 *when* the leakage indicator 105 indicates that the integrated circuit 10 is slow (and hence exhibit less leakage) in comparison to most integrated circuits of a batch of integrated circuits that includes the integrated circuit 10. Similarly, the control circuit 50 may *select the leakage reduction value* of the control signal 103 *when* the leakage indicator 105 indicates that the integrated circuit 10 is fast (and hence has high leakage) in comparison to most integrated circuits of a batch of integrated circuits that includes the integrated circuit 10.

Ex. 1001, 4:59–5:2 (emphases added). These disclosures in the Specification are consistent with the plain meaning and the modified IEEE dictionary definition discussed above. They are also consistent with the alternative dictionary definition discussed in the Institution Decision—"[t]o choose or pick out in preference to another or others." *See* Ex. 3002, 1; Inst. Dec. 61.

As discussed above, Patent Owner cites Figures 3 and 4 of the '026 patent to argue the selection recited in the challenged claims requires the indicators to "play a role in deciding which of the multiple values will be chosen or picked." PO Resp. 31. To the extent Patent Owner argues selecting "performance value," "leakage reduction value," and "retention value" recited in claims 2, 4, 5, or 7 requires using functional relationships depicted in the curves shown on Figures 3 and 4, we disagree with Patent

Owner's argument. We depart from the plain and ordinary meaning in only two instances: (1) when a patentee acts as his own lexicographer and (2) when the patentee disavows the full scope of the claim term in the specification or during prosecution. *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016) (citing *Hill–Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014)). Here, Patent Owner argues neither lexicography nor disavowal, and the words "play a role" do not appear in any of the challenged claims.

In addition, for reasons similar to those discussed above with respect to claim 1, to the extent Patent Owner argues the selection clause recited in claim 2 requires selecting a value from or among a group of multiple values, we disagree with Patent Owner's argument. As discussed above, the patentee knew how to describe the concept of selecting a value out of a group of values for claim 4. If the patentee had intended to similarly describe the method of selection recited in claim 2, it could have done so using the language of claim 4, but did not. We disagree with the "[selecting from among] multiple values" aspect of Patent Owner's construction because it would blur the material differences in the language of claim 2 and claim 4 discussed above.

Based on the complete record, we determine that the selection clauses recited in the claim 2 are not limited as Patent Owner argues.

We need not construe any other claim terms for purposes of this Final Written Decision. *See Vivid Techs.*, 200 F.3d at 803.

C. Obviousness over Kim and Lee

In this asserted ground of obviousness, Petitioner contends that claims 1, 2, 4, 5, and 7 are unpatentable under 35 U.S.C. § 103(a) over the combination of Kim and Lee. Pet. 26–83.

1. Relevant Principles of Law

To prevail in challenging Patent Owner's claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). Apart from limited circumstances not presented here, this burden does not shift to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

of skill in the art; and (4) where in evidence, so-called secondary considerations.[6] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

An invention "composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418 (for an obviousness analysis, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does"). Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); *accord In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (stating that "conclusory statements" amount to an "insufficient articulation[] of motivation to combine"; "instead, the finding must be supported by a 'reasoned explanation'"); *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) ("To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The

[6] The parties do not address secondary considerations, which therefore do not constitute part of our analysis.

petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.").

We analyze the asserted ground based on obviousness with the principles identified above in mind.

2. Overview of Kim (Ex. 1004)

Kim relates generally to die-to-die process variation compensation for digital circuits. Ex. 1004 ¶ 7. In particular, Kim describes an array of sleep transistors that can be used to reduce leakage of a circuit by enabling a combination of sleep transistors. *Id.* at code (57). As background, Kim describes that "as transistor sizes have become ever smaller, the leakage power consumption during active modes has become a serious problem thereby resulting in some fast dies that are excessively leaky to . . . be discarded." *Id.* ¶ 8. According to Kim, therefore, "it would be desirable to find a way to retain and use these 'leaky' dies." *Id.* Kim purports to provide this desired solution.

> As presented in some embodiments disclosed herein, it has been discovered that for fast but leaky dies, *desired performance and leakage reduction can be attained* at the same time by, if necessary, *turning on a sub-combination of the sleep transistors* during active modes, depending on the leakage characteristics of a particular chip or group of associated chips.

Id. ¶ 10 (emphases added).

Figure 1 of Kim is reproduced below.

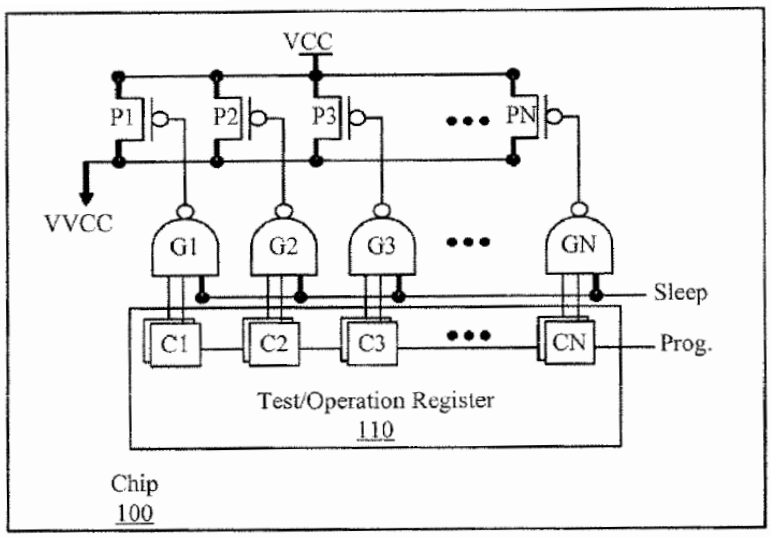


FIGURE 1

Figure 1 is a schematic diagram of an exemplary processor chip with a programmable sleep transistor array and a virtual supply. *See* Ex. 1004 ¶¶ 2, 11. As shown in Figure 1, chip 100 comprises an array of sleep transistors P1 to PN, NAND gates G1 to GN, and test/operation register 110 comprising memory cells C1 to CN. *Id.* ¶ 11.

Kim describes that sleep transistors P1 to PN are PMOS transistors that are coupled to a high supply voltage reference (VCC) and NAND gates G1 to GN. *See id.* Each of NAND gates G1 to GN is coupled to a memory cell (one of memory cells C1 to CN) associated with the particular NAND gate and sleep transistor combination. *Id.* As depicted in Figure 1, sleep transistors P1 to PN are used to provide a virtual high supply voltage (VVCC) from a high supply reference voltage (VCC). *See id.* ¶¶ 11, 21, 23; Fig. 1.

Figure 5 of Kim is reproduced below.

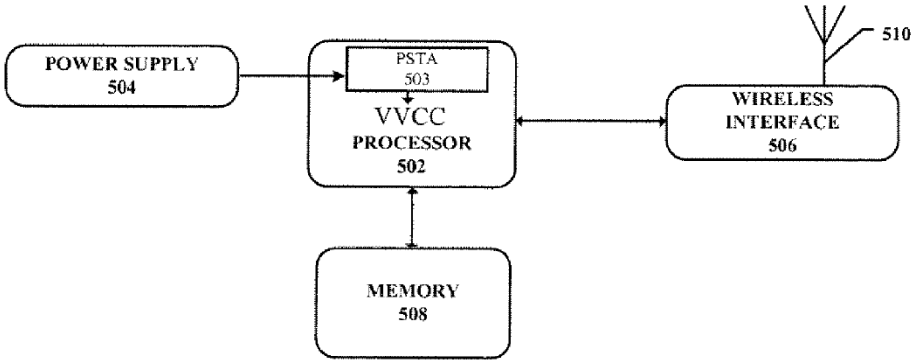


FIGURE 5

Figure 5 is a block diagram of a computer system having a microprocessor with at least one programmable sleep transistor array in an exemplary embodiment. Ex. 1004 ¶ 6. As depicted in Figure 5, microprocessor 502 includes programmable sleep transistor array (PTSA) 503. *Id.* ¶ 23. Also, microprocessor 502 is coupled to power supply 504 to receive power for operation. *Id.* Kim describes that PTSA 503 receives power from power supply 504 and provides a virtual high supply voltage (VVCC) to one or more functional blocks within microprocessor 502 to reduce leakage during an active mode. *Id.*

Kim provides disclosures on programming a programmable sleep transistor array to obtain suitable sleep transistor array combinations to supply a virtual supply voltage that reduces leakage in a processor or chip. Ex. 1004 ¶¶ 10–23. As depicted in Figure 1, test/operation register 110 has a signal (labeled Prog.) to program the memory cells. *Id.* ¶ 14. Figure 1 also shows a sleep mode signal (labeled Sleep) coupled to each of the NAND gates. *Id.* ¶ 11. Kim describes that the Sleep signal controls the sleep transistors that have been designated for active use once the cells are

programmed for normal operation (e.g., burned at the factory or loaded at start-up). *Id.* ¶ 16. Referencing Figure 1, Kim describes that, in the depicted embodiment, when the Sleep signal is asserted (Low), NAND gates G1 to GN all output a High, which turns off the sleep transistors. *Id.* On the other hand, when the Sleep signal is de-asserted (High) during an active mode, the NAND gates are controlled by the cells, C1 to CN, that are used for normal operation. *Id.* Kim describes that when a cell outputs a High signal to its NAND gate, the sleep transistor coupled to the gate is turned on, whereas a cell output of a Low causes the sleep transistor to be turned off. *Id.*

Figure 2 of Kim is reproduced below.

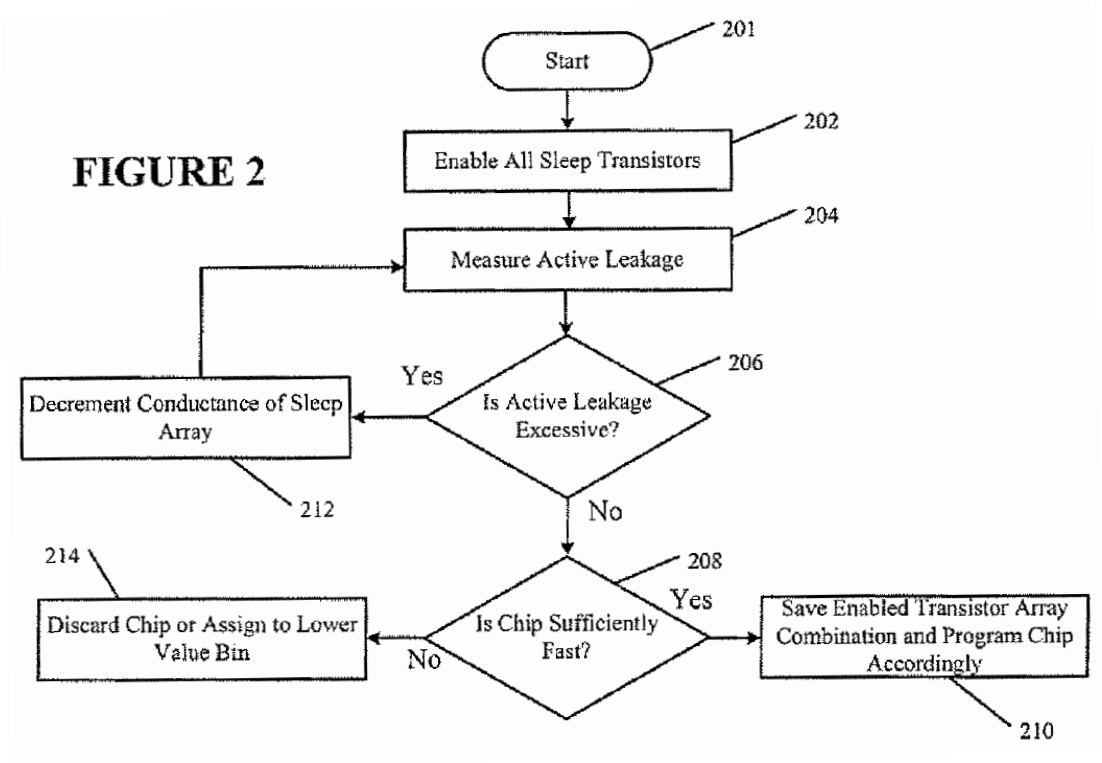


Figure 2 shows an exemplary routine for identifying a suitable combination of enabled sleep transistors in a programmable sleep transistor array. Ex. 1004 ¶ 3.

Kim describes that routine 201, shown in Figure 2, is used for testing a chip to determine sleep transistor combinations to be turned on during an active mode in order to provide a virtual supply voltage (VVCC) to the chip or a functional block of the chip. Ex. 1004 ¶¶ 17, 18. According to Kim, routine 201 may be performed during the manufacturing process to test chips and determine the amount of leakage in a chip during an active mode. *Id.* ¶ 17. Kim describes that routine 201 may also be used to program the memory cells in the test/operation register at the start-up of an operation in order to determine a suitable array of enabled sleep transistors during normal operation. *Id.* ¶¶ 20, 22. Referencing Figure 1, Kim also describes that test/operation register 110 (i.e., memory cells C1 to CN) should be programmable during a test phase (e.g., during the manufacturing process) and should also be programmable for normal operation. *Id.* ¶ 14. According to Kim, both types of programming may be achieved using the same structure. *Id.*

Regarding the steps performed by routine 201, Kim describes that initially at step 202, each sleep transistor in an array is enabled, e.g., by programming each memory cell with a value of 1. Ex. 1004 ¶ 18. Next, at step 204, with the sleep transistor array providing a virtual supply voltage to the chip or a functional block of the chip, the active leakage in the chip is measured. *Id.* Then at step 206, a determination is made whether the active leakage is excessive. *Id.* ¶ 19. If the answer is Yes (i.e., the leakage is excessive), then the conductance of the sleep transistor array is decremented, e.g., by turning off one or more sleep transistors in the array. *Id.* Then, the routine loops back to step 204 to measure the leakage with the modified sleep transistor array combination (having a decreased conductance), and

then proceeds again to step 206 to check if the newly measured leakage is excessive. *Id.* This process continues until the measured active leakage is not excessive, at which time the routine proceeds to step 208 to determine whether the chip is sufficiently fast. *Id.* ¶¶ 19, 20. If the chip is fast enough (with the reduced virtual supply voltage provided to the chip by the sleep transistor array combination determined in steps 204 and 206 that results in non-excessive leakage), then at step 210 the determined enabled transistor array combination is stored or programmed into register 110. *Id.* ¶ 20. For example, the combination may be burned into the register if it is one time-programmable memory, or it may be stored to be part of a start-up routine to be programmed into the register when the chip starts up. *Id.* If, on the other hand, the chip is determined to be not sufficiently fast, then at step 214 the chip may be discarded or otherwise devalued. *Id.*

Once determined, an enabled transistor combination may be saved to be programmed at startup of an operation or during the manufacturing process. *Id.* ¶ 22.

3. Overview of Lee (Ex. 1005)

Lee describes a standby leakage current reduction circuit and a semiconductor memory device comprising the standby leakage current reduction circuit. Ex. 1005, code (57).

Figure 4 of Lee is reproduced below.

FIG. 4

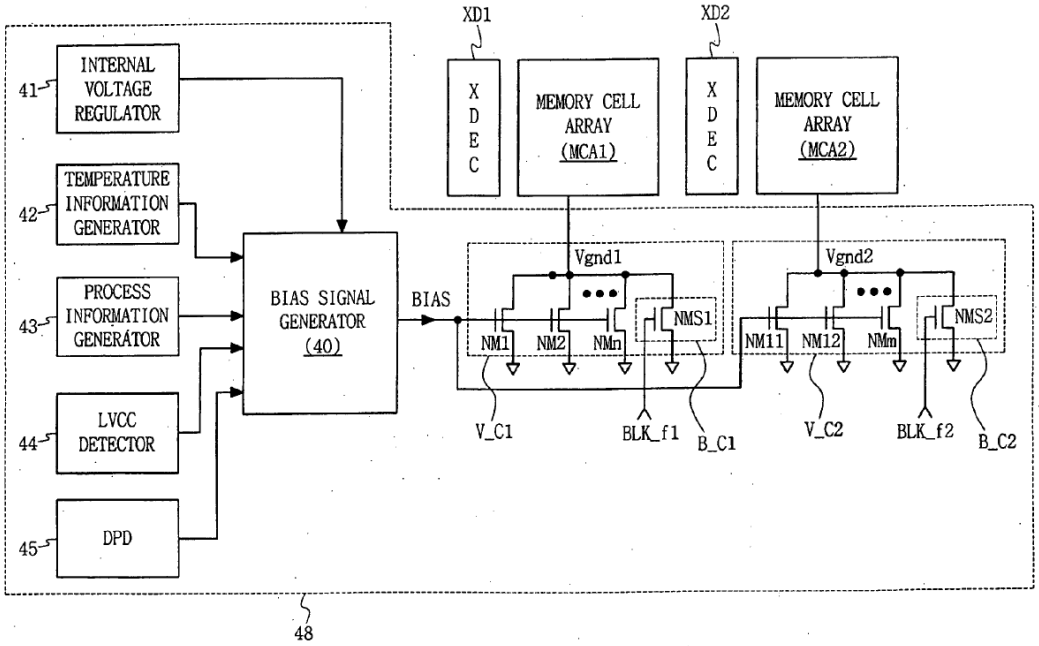


Figure 4 schematically illustrates an exemplary semiconductor memory device that comprises an exemplary standby leakage current reduction circuit. Ex. 1005 ¶ 50.

As shown in Figure 4, standby leakage current reduction circuit 48 includes deep power down setting unit 45, temperature information generator 42, bias signal generator 40, and internal voltage regulator 41. *Id.* ¶ 51. As illustrated in Figure 4, Lee's Bias signal generator 40 controls the output supply voltage provided by virtual ground controller VC_1 based on several inputs, such as input from temperature sensor 42, process information generator 43, and deep power down (DPD) indicator 45 (blue), which provides an input that indicates whether the memory cells are in a deep power down mode. *Id.* ¶¶ 57, 71, 81, 86, 133, 152.

Lee describes that the bias signal is an analog signal applied to the NMOS sleep transistors (e.g., NM1 to NMn) that modifies the virtual ground for the NMOS transistors, which changes the conductivity (or the operational resistance) of the sleep transistors. *See id.* ¶¶ 22, 52, 61.

Lee describes that deep power down setting unit 45 may set a deep power down mode of the semiconductor memory device. *Id.* ¶ 57. Lee further describes that when the semiconductor memory device is in an active mode or a standby mode, deep power down signal DPD has a logic low level and that when the semiconductor memory device is in the deep power down mode, deep power down signal DPD has a logic high level. *Id.* ¶ 71.

4. Discussion of Independent Claim 1 — Differences Between the Claimed Subject Matter and the Prior Art

Petitioner relies on Kim to teach or render obvious nearly all limitations recited in claim 1 with one exception, "a mode indicator generator" included in the recited "integrated circuit," for which Petitioner relies on the combination of Kim and Lee. Pet. 26–59. Patent Owner does not dispute Petitioner's contentions on most of the limitations of claim 1. For example, Patent Owner does not dispute Kim teaches or renders obvious the following recitations of claim 1.

> An integrated circuit, comprising:
>
> a power gating switch, the switch comprises:
>
> an input port for receiving an input supply voltage;
>
> an output port for providing an output supply voltage to a power gated circuit; and
>
> a control port for receiving a control signal that determines a difference between the input supply voltage and the output supply voltage;

> wherein the integrated circuit further comprising the power gated circuit, being gated relative to the input supply voltage by the switch, the power gated circuit being coupled to the output port of the switch for receiving the output supply voltage;

See PO Resp. 32–65. Patent Owner also does not dispute Kim teaches "a leakage indicator generator for generating a leakage indicator that indicates a leakage level of the power gated circuit," as recited in claim 1. *See id.* Patent Owner, however, disputes Kim teaches "a control circuit . . . arranged to select the value of the control signal based on the mode indicator and on the leakage indicator." *Id.* at 32–33. Patent Owner also argues that the combination of Kim and Lee does not teach "a mode indicator generator for generating a mode" recited in claim 1. *Id.* at 51–54. In addition, Patent Owner asserts that a person of ordinary skill in the art would not have been motivated to combine Kim and Lee as proposed by Petitioner. *Id.* at 55. In what follows, we first discuss Petitioner's contentions on the undisputed recitations of claim 1 and then discuss the parties' arguments and evidence on the disputed limitations of claim 1.

a. Undisputed Recitations of Claim 1

(i) "An integrated circuit, comprising a power gating switch"

Petitioner contends that the embodiments depicted in Figures 1, 2, 4, and 5 of Kim teach an "integrated circuit" comprising "a power gating switch," where the switch comprises "an input port for receiving an input supply voltage," "an output port for providing an output supply voltage to a power gated circuit," and "a control port for receiving a control signal that determines a difference between the

input supply voltage and the output supply voltage," as recited in claim 1. Pet. 26–38.

Figures 4 and 5 of Kim, as annotated by Petitioner in different colors, are reproduced below.

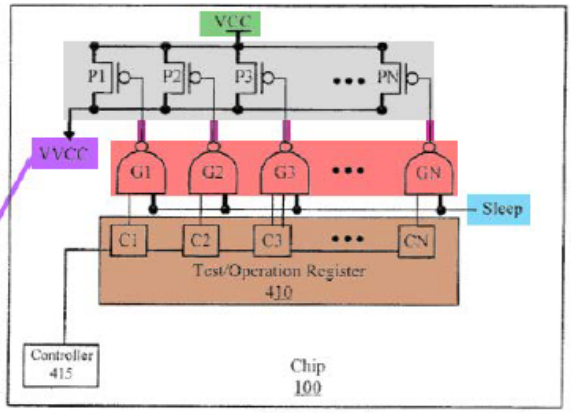


FIGURE 4

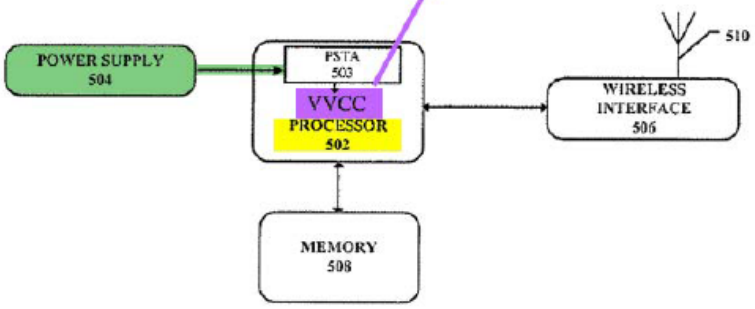


FIGURE 5

Id. at 27. Annotated Figures 4 and 5 reproduced above show Petitioner's identification of many of claim 1's recited circuits or circuit components allegedly present in Kim, including an "integrated circuit," "a power gating switch," "an input port," "an output port," and "a control port." *See id.* at 26–35.

Petitioner asserts that chip 100, depicted in Annotated Figure 4 (uncolored), teaches the "integrated circuit" recited in the preamble of

claim 1.[7] *Id.* at 26 (citing Ex. 1004 ¶ 24; Figs. 1, 3, 4). Petitioner also asserts that sleep transistor array P1–PN, shown in Annotated Figures 4 and 5 (annotated in grey), teaches the "power gating switch" recited in claim 1. *Id.* at 27. Referencing Annotated Figures 4 and 5, Petitioner argues that, as shown in the figures, Kim's sleep transistor array P1–PN in chip 100 receives input voltage VCC (annotated in green) (the recited "input supply voltage") and provides virtual supply voltage VVCC (annotated in purple) (the recited "output supply voltage") to "one or more functional blocks within the processor 502" (annotated in yellow) (the recited "power gated circuit"). *Id.* at 26–27 (citing Ex. 1004 ¶ 23; Figs. 4, 5). Petitioner further contends that Kim's sleep transistor array P1–PN

> (1) . . . switches ON virtual supply voltage VVCC to processor 502 when the received Sleep signal (blue) is high (indicating an active mode), and (2) switches OFF virtual supply voltage VVCC to processor 502 when the received Sleep signal (blue) is low (indicating a sleep mode) by providing a high resistance path between the input supply voltage VCC and output virtual supply voltage VVCC.

Id. at 27–28 (citing Ex. 1004 ¶ 16). Petitioner argues that Kim's sleep transistor array P1–PN teaches the "power gating switch" recited in claim 1 because the array "gates" virtual supply voltage VVCC by turning output supply voltage VVCC ON and OFF. *Id.* at 28. Petitioner further asserts that Kim's sleep transistor array P1–PN provides its gating function by changing its conductivity or conductance, similar to the way the power gating switch of the '026 patent functions as described in the Specification. *Id.*

[7] Because Petitioner has shown that the "integrated circuit" recited in the preamble is satisfied by Kim, we need not determine whether the preamble is limiting. *See Vivid Techs.*, 200 F.3d at 803.

(comparing Ex. 1001, 2:40–44 ("selecting a control signal that determines *the conductivity* of the power gating switch" (emphasis added)), with Ex. 1004 ¶ 19 (describing how "the sleep transistor array *conductance* is decremented" by changing a control signal) (emphasis added)).

Petitioner presents an annotated version of Figure 4 of Kim (not reproduced herein) and identifies the connection between input supply voltage VCC (the claimed "input supply voltage") and the sources of sleep transistors P1–PN as the recited "input port for receiving an input supply voltage" (Pet. 29 (citing Ex. 1004 ¶ 11 (explaining the sleep transistors "are coupled [to] a high supply reference (VCC)"), Fig. 4)). Petitioner also maps the recited "output port for providing an output supply voltage to a power gated circuit" to the drains of sleep transistor array P1–PN (the recited "output port") providing output virtual supply voltage VVCC (the recited "output supply voltage") to "one or more functional blocks" within processor 502 (annotated in yellow in Annotated Figures 4 and 5 reproduced above) (the recited "power gated circuit"). *Id.* at 30–33 (citing Ex. 1004 ¶ 23, Figs. 4, 5), 42–43 (citing Ex. 1004 ¶ 16, 23).

Next, Petitioner provides an annotated version of Kim's Figure 4, which we refer to as Second Annotated Version of Figure 4, and asserts that Kim teaches "a control port for receiving a control signal," as recited in claim 1. Pet. 33–35.

Second Annotated Version of Kim's Figure 4 provided in the Petition is reproduced below.

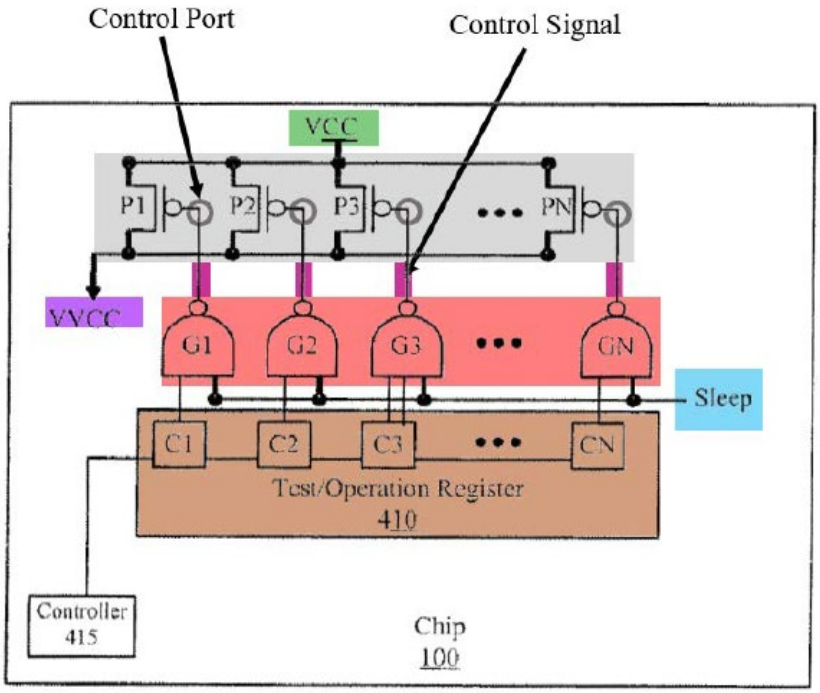


FIGURE 4

Id. at 34. Second Annotated Version of Kim's Figure 4 reproduced above shows Petitioner's identification of "a control port for receiving a control signal" allegedly present in Kim. *Id.*

Referencing Second Annotated Version of Figure 4 Petitioner contends that the port (annotated in dark grey circles) driving the gates of the sleep transistors in the array is the "control port" recited in claim 1. Pet. 34, 37. Petitioner also identifies the output (annotated in magenta) of NAND gates G1–GN (annotated in red) as the recited "control signal" received by the "control port." *Id.* at 34–35 (citing Ex. 1004, Fig. 4, ¶ 16 (explaining how NAND gates G1–GN control sleep transistor array P1–PN in a sleep mode by turning all sleep transistors OFF and in an active mode by selectively turning individual sleep transistors ON or OFF)).

Petitioner further asserts that Kim teaches the "control signal . . . determines a difference between the input supply voltage and the output supply voltage," as recited in claim 1. *Id.* at 35–37. In support of its contention, Petitioner cites routine 201, depicted in Figure 2 of Kim, and the description of routine 201, provided in the related text of Kim, as teaching reducing or decrementing the conductance of the sleep transistor array by turning OFF one or more sleep transistors in a loop to find a combination of enabled sleep transistors resulting in satisfactory leakage in a functional block of Kim's processor. *Id.* at 35–36 (citing Ex. 1004, Fig. 2, claim 8, ¶¶ 10, 16, 18, 19). According to Petitioner, Kim further teaches that the output of NAND gates G1–GN (the claimed "control signal") determines multiple voltage differences between VCC (the claimed "input supply voltage") and VVCC (the claimed "output supply voltage") because Kim discloses, for example,

> (1) when the Sleep signal is low, the outputs of the NAND gates turn OFF every transistor P1-PN, such that VVCC will be lower than VCC); (2) when the Sleep signal changes from low to high, the NAND gate outputs (in step 202) turn ON every transistor P1-PN, such that VCC and VVCC will be as close as possible; and (3) when there is excessive leakage, the NAND gates turn ON some sleep transistors and turn others OFF, which will increase the difference between VCC and VVCC.

Id. at 36–37 (citing Ex. 1004 ¶¶ 16, 18–20; Ex. 1002 ¶ 77). Petitioner presents a comparison of color-annotated Figure 1 of the '026 patent and color-annotated Figure 4 of Kim and asserts that

> both figures depict a "power gating switch" (grey) with a "control port" (grey circles) that receives a "control signal" (vertical magenta rectangles) used to determine a difference between the input supply voltage (green) and the output supply voltage (purple).

Id. at 37–38 (comparing Ex. 1001, Fig. 1, with Ex. 1004, Fig. 4).

As discussed above, Patent Owner does not dispute Kim teaches the recitations of claim 1 discussed in this subsection. *See* PO Resp. 32–65.

We agree with Petitioner's analysis and find, based on the complete record and for the reasons explained by Petitioner, that Petitioner has demonstrated sufficiently Kim teaches an "integrated circuit" comprising "a power gating switch," where the switch comprises "an input port for receiving an input supply voltage," "an output port for providing an output supply voltage to a power gated circuit," and "a control port for receiving a control signal that determines a difference between the input supply voltage and the output supply voltage," as recited in claim 1.[8]

(ii) "the integrated circuit further comprising the power gated circuit"

Next, Petitioner contends that Kim teaches or renders obvious "the integrated circuit further comprising the power gated circuit, being gated relative to the input supply voltage by the switch, the power gated circuit being coupled to the output port of the switch for receiving the output supply voltage," as recited by claim 1. Pet. 38–41.

Citing the testimony of Dr. Harris, Petitioner asserts that a person of ordinary skill in the art would have understood Kim to teach placing the recited "power gating switch" and "power gated circuit" on the same integrated circuit because Kim describes that sleep transistor array P1–PN

[8] We also find that Patent Owner has waived any argument directed to these recitations of claim 1. *See* Paper 12 (Scheduling Order), 7 ("Patent Owner is cautioned that any arguments for patentability not raised in the response may be deemed waived.").

(the claimed "power gating switch") is included in a microprocessor with one or more functional blocks (the claimed "power gated circuit"), and Figure 5 shows the sleep transistor array (PSTA 503) as part of the same integrated circuit as processor 502. *Id.* at 39–40 (citing Ex. 1004, Fig. 5, ¶¶ 23 ("Microprocessor 502 comprises a programmable sleep transistor array (PSTA) 503."), 24 ("[T]he present invention is applicable for use with all types of semiconductor integrated circuit ('IC') chips . . . *IC chips include . . . processors* . . . and the like." (emphases by Petitioner)); Ex. 1002 ¶ 82).

In addition, Petitioner contends that placing the "power gating switch" and the "power gated circuit" on the same integrated circuit would have been obvious to a person of ordinary skill in the art in view of Kim because doing so would have been one of a finite number of options—namely, placing the power gating switch and the power gated circuit either on the same chip or on separate chips. *Id.* at 40. Citing the testimony of Dr. Harris and an article in the April 19, 1965, issue of the Electronics magazine, Petitioner argues that a person of ordinary skill in the art would have been motivated to place the switch and the circuit on the same chip due to the well-known trend of placing increasing amounts of functionality on a chip and the benefits of increased speed, reduced size, reduced cost, reduced number of pins, and improved power supply integrity, as compared to placing the switch and circuit on separate chips. *Id.* at 40–41 (citing Ex. 1013, 115; Ex. 1002 ¶ 82).

Petitioner also argues that, for the reasons discussed in the immediately preceding subsection with respect to the recitations "power gating switch" and "determin[ing] a difference between the input supply

voltage and the output supply voltage," Kim teaches "the power gated circuit, being gated relative to the input supply voltage by the switch, the power gated circuit being coupled to the output port of the switch for receiving the output supply voltage," as recited in claim 1. *Id.* at 38–39 (citing Pet. §§ X.A.1.b., X.A.1.e.; Ex. 1004, Figs. 4, 5, ¶ 23).

As discussed above, Patent Owner does not dispute Kim teaches the limitation of claim 1 discussed in this subsection. *See* PO Resp. 32–65.

We agree with Petitioner's analysis and find, based on the complete record and for the reasons explained by Petitioner, that Petitioner has demonstrated sufficiently Kim teaches or renders obvious "the integrated circuit further comprising the power gated circuit, being gated relative to the input supply voltage by the switch, the power gated circuit being coupled to the output port of the switch for receiving the output supply voltage," as recited in claim 1.[9]

(iii) "a leakage indicator generator for generating a leakage indicator that indicates a leakage level of the power gated circuit"

Claim 1 recites "a leakage indicator generator for generating a leakage indicator that indicates a leakage level of the power gated circuit." Referencing Annotated Figure 4 of Kim reproduced above, Petitioner asserts that memory cells C1–CN of register 410 (annotated in brown) teach the recited "leakage indicator generator" and the output of memory cells C1–CN teaches the recited "leakage indicator that indicates a leakage level of the power gated circuit." Pet. 50, 53 (citing Ex. 1004, Fig. 4, ¶¶ 14–20).

[9] We also find that Patent Owner has waived any argument directed to this claim limitation. *See* Paper 12, 7.

Turning first to Petitioner's contention that the output of Kim's memory cells C1–CN teaches the "leakage indicator that indicates a leakage level of the power gated circuit" recited in claim 1, Petitioner cites routine 201 depicted in Figure 2 of Kim (reproduced in Section III.C.2. above) and asserts that "Kim details how memory cells C1-CN are used in 'routine 201 for testing a chip . . . to determine the amount of leakage in a chip' and 'sleep transistor combinations to be turned on . . . during an active mode.'" *Id.* at 51 (citing Ex. 1004, Fig. 2, ¶¶ 17–20). Petitioner asserts that Kim teaches

> (1) turning ON all sleep transistors P1-PN (step 202), which maximizes the output level for virtual supply voltage VVCC, Ex. 1004, [0018];
>
> (2) measuring "the active leakage in the chip (or functional block supplied by [VVCC])" (step 204), *id.*, [0018], [0023] (explaining that "functional blocks" can be "functional blocks within the processor 502");
>
> (3) determining "if the active leakage is excessive" (step 206), *id.*, [0019];
>
> (4) if leakage is excessive, turning OFF at least one sleep transistor to decrease the output level for virtual supply voltage VVCC (step 212), *id.*, [0019]; *see also id.*, [0016] ("[D]uring an active mode, the NAND gates in effect are then controlled by the cells, C1 to CN ….. If a sleep transistor was designated to be on during an active mode, then its cell outputs a High to its NAND gate, causing the transistor to be turned on. Alternatively, if a sleep transistor was designated to be off, then its cell outputs a Low, causing the transistor to be turned off during the active mode.")
>
> (5) repeating steps 204 (measure leakage), 206 (determining if the measured leakage is excessive), and 212 (decreasing VVCC) until the measured leakage is not excessive, *id.*; and
>
> (6) "stor[ing] the enabled transistor array combination … so that it will be programmed into the register 110 [410]," and

> using those stored values to determine the level of VVCC during active mode, *id.*, [0016], [0020], [0022]; Ex. 1002, ¶ 95.

Pet. 51–53 (citing Ex. 1004 ¶¶ 16, 18, 19, 20, 22, 23; Ex. 1002 ¶ 95). According to Petitioner, the cited disclosure of Kim teaches that the output of memory cells C1–CN reflects the amount of measured leakage in processor 502, and is used to determine which sleep transistors P1–PN will be ON and OFF when the processor is in the active mode.

Citing the testimony of Dr. Harris, Petitioner provides examples of the amount of measured leakage in processor 502 indicated by the output of memory cells C1–CN. *Id.* at 53 (citing Ex. 1004 ¶¶ 14–20; Ex. 1002 ¶ 96). Petitioner argues that because Kim's routine 201 starts with turning ON all sleep transistors P1–PN, if processor 502 is found to not have excessive leakage at the very first execution of Kim's step 206, the output from cells C1–CN would have the value of all ones (1s) after completion of routine 201, indicating that processor 502, as found, has low leakage. *Id.* Petitioner contends that, if, on the other hand, processor 502 is found to have higher leakage, routine 201 would execute step 206 more than once, turning OFF some transistors in the sleep transistor array, and the output from Kim's cells C1–CN would include some zeroes (0s) upon completion of routine 201. *Id.* In other words, the output from Kim's memory cells C1–CN, as determined by the value stored in the cells at the end of executing routine 201, would indicate the leakage level of processor 502 as found, before applying Kim's leakage reduction method—that is, a leakage level lower than the excessive level threshold (when the output of the memory cells is all ones (1s)) or a leakage level at or higher than the excessive level threshold (when the output of the memory cells includes some zeroes (0s)).

See id. Petitioner argues, therefore, the output of Kim's memory cells C1–CN is the claimed "leakage indicator that indicates a leakage level of the power gated circuit." *Id.*

Petitioner asserts that Kim measures leakage during manufacturing and then stores in memory cells C1–CN the results of the leakage measurement, which determines during operation which sleep transistors will be ON and OFF in an active mode. Pet. 54 (citing Ex. 1004 ¶ 20). According to Petitioner, this is similar to the disclosure in the '026 patent, which describes that "leakage indicator" can be used "during the manufacturing process of the integrated circuit 10 or based on a leakage test conducted after the production of the integrated circuit 10 . . ., [and] can include measuring the actual leakage of the integrated circuit 10, or determining indirectly the leakage." *Id.* (quoting Ex. 1001, 3:46–54).

Turning next to Petitioner's arguments and evidence on the recited "leakage indicator generator," Petitioner asserts that Kim's memory cells C1–CN collectively are the recited "leakage indicator generator" because the cells generate the output signal (the recited "leakage indicator"). Pet. 53 (citing Ex. 1004 ¶¶ 14–20; Ex. 1002 ¶ 96). As discussed above in Section III.C.4.a(ii), Petitioner asserts, citing the testimony of Dr. Harris, that a person of ordinary skill in the art would have understood Kim to teach placing the recited "power gating switch" and "power gated circuit" on the same integrated circuit because Kim describes that sleep transistor array P1–PN (the recited "power gating switch") is included in a microprocessor with one or more functional blocks (the recited "power gated circuit") and also because Figure 5 shows the sleep transistor array (PSTA 503) as part of the same integrated circuit as processor 502. *Id.* at 39–40 (citing Ex. 1004,

Fig. 5, ¶¶ 23, 24; Ex. 1002 ¶ 82). As discussed below in Section III.C.4.b(i), Petitioner argues that Kim teaches or suggests "a control circuit" included in the "integrated circuit" recited in claim 1 because Figures 1 and 4 of Kim show that NAND gates G1–GN (the recited "control circuit") are located on chip 100 (the recited "integrated circuit"), and Kim's Figure 5 shows that PTSA 503 can be on-chip with processor 502. Pet. 57 (citing Ex. 1004, Figs. 1, 4, 5, ¶ 24). Because Figure 4 of Kim shows that memory cells C1–CN, NAND gates G1–GN, and sleep transistor array P1–PN are all located on the same chip 100 (the recited "integrated circuit"), Petitioner has provided evidence to show "a leakage indicator generator" is included in the "integrated circuit" recited in claim 1.

Patent Owner does not dispute Kim teaches "a leakage indicator generator for generating a leakage indicator that indicates a leakage level of the power gated circuit," as recited in claim 1. *See* PO Resp. 32–65.

We agree with Petitioner's analysis and find, based on the complete record and for the reasons explained by Petitioner, that Petitioner has demonstrated sufficiently Kim teaches "a leakage indicator generator for generating a leakage indicator that indicates a leakage level of the power gated circuit," as recited in claim 1.[10]

b. Disputed Limitations

As discussed above, Patent Owner disputes Kim teaches "a control circuit . . . arranged to select the value of the control signal based on the mode indicator and on the leakage indicator." PO Resp. 32–33. Patent

[10] We also find that Patent Owner has waived any argument directed to this claim limitation. *See* Paper 12, 7.

Owner also argues that the combination of Kim and Lee does not teach "a mode indicator generator for generating a mode" recited in claim 1. *Id.* at 51–54. In addition, Patent Owner asserts that a person of ordinary skill in the art would not have been motivated to combine Kim and Lee as proposed by Petitioner. *Id.* at 55. We discuss the parties' arguments and evidence on each of these issues below.

(i) "a control circuit, connected to the mode indicator generator and the leakage indicator generator, for receiving the mode indicator and the leakage indicator, the control circuit being arranged to select the value of the control signal based on the mode indicator and on the leakage indicator"

Turning first to Petitioner's contentions on "a control circuit, connected to the mode indicator generator and the leakage indicator generator, for receiving the mode indicator and the leakage indicator," as recited in claim 1, Petitioner asserts that Kim alone or in combination with Lee teaches this limitation. Pet. 54–57. As discussed above, Petitioner identifies the output of NAND gates G1–GN as the "control signal" recited in claim 1. *Id.* at 34–35 (citing Ex. 1004, Fig. 4, ¶ 16). Referencing a color-annotated version of Kim's Figure 4 similar to Second Annotated Version of Figure 4 reproduced above in Section III.C.4.a(i), Petitioner asserts that NAND gates G1–GN (annotated in red) depicted in the figure are the recited "control circuit." *Id.* at 55 (citing Ex. 1004, Fig. 4). Referencing the same color-annotated Figure 4, Petitioner argues that NAND gates G1–GN are connected to both memory cells C1–CN (the recited "leakage indicator generator") and the source of the Sleep signal (the recited "mode indicator generator"). *Id.* at 55–56 (citing Ex. 1004, Fig. 4). Petitioner also asserts that Kim teaches that NAND gates G1–GN receive the

Sleep signal (the recited "mode indicator") and the output of memory cells C1–CN (the recited "leakage indicator"). *Id.* at 56 (citing Ex. 1004 ¶ 11; Ex. 1002 ¶ 99).

Petitioner further asserts that Kim teaches or suggests "a control circuit" included in the recited "integrated circuit" because Figures 1 and 4 of Kim show that NAND gates G1–GN (the recited "control circuit") are located on chip 100 (the recited "integrated circuit"), and Kim's Figure 5 shows that programmable sleep transistor array 503 can be on-chip with processor 502. Pet. 57 (citing Ex. 1004 ¶ 24, Figs. 1, 4, 5). Petitioner also argues that it would have been obvious to have Kim's NAND gates on the same integrated circuit as Kim's processor for the same reasons discussed above with respect to the recitation "the integrated circuit further comprising the power gated circuit" in Section III.C.4.a(ii).

In the alternative, Petitioner asserts that the combination of Kim and Lee teaches "a control circuit, connected to the mode indicator generator and the leakage indicator generator, for receiving the mode indicator and the leakage indicator," as recited in claim 1. Pet. 56. In this alternative, Petitioner argues that, to the extent this limitation is interpreted to require the recited "control circuit" to be connected to the recited "mode indicator generator" included in the recited "integrated circuit," the combination of Kim and Lee teaches such a "control circuit" for the reasons discussed above with respect to the "mode indicator generator" limitation. *Id.* at 56–57 (citing Pet. § X.A.1.g.).

Turning next to Petitioner's contentions on the recitation "the control circuit being arranged to select the value of the control signal based on the mode indicator and on the leakage indicator," Petitioner asserts that the

operation of Kim's NAND gates G1–GN (the recited "control circuit") teaches this limitation. Pet. 57–59. As discussed above, Petitioner maps the output of NAND gates G1–GN to the "control signal" recited in claim 1. *Id.* at 34–35 (citing Ex. 1004, Fig. 4, ¶ 16). Petitioner asserts that Kim also teaches that the value[11] of the collective output of NAND gates G1–GN (the recited "control signal") is selected based on the Sleep signal (the recited "mode indicator") and the output of memory cells C1–CN (the recited "leakage indicator"). *Id.* at 57 (citing Ex. 1002 ¶ 103).

Addressing the recitation that the control circuit selects the value of the control signal "based on the mode indicator," Petitioner contends that during a sleep mode, the Sleep signal is asserted low, which in turn causes NAND gates G1–GN to all output a high signal that turns off all their respective sleep transistors P1–PN. Pet. 58 (citing Ex. 1004 ¶ 16 ("[W]hen the Sleep signal is asserted (Low), then the NAND gates G1 to GN all output a High, which turn off the sleep transistors."); Ex. 1002 ¶ 104). Petitioner argues, therefore, the output (the recited "control signal") from NAND gates G1–GN (the recited "control circuit") is based on the Sleep signal (the recited "mode indicator"). *Id.* (citing Ex. 1002 ¶ 104).

Next, regarding the recitation that the control circuit selects the value of the control signal "based on the leakage indicator," Petitioner cites Kim's disclosure that

[11] As discussed below in the section on claim 2, Petitioner's declarant, Dr. Harris, illustrates various values of the collective output of NAND gates G1–GN in the context of his testimony on claim 2. *See* Ex. 1002 ¶ 108 (providing a table of various values of the collective output of NAND gates G1–GN for an example case of 5 NAND gates).

> when the Sleep signal is de-asserted (High) during an active mode, *the NAND gates in effect are then controlled by the cells, C1-CN*, that are used for normal operation. If a sleep transistor was designated to be on during an active mode, then its cell outputs a High to its NAND gate, causing the transistor to be turned on. Alternatively, if a sleep transistor was designated to be off, then its cell outputs a Low, causing the transistor to be turned off during the active mode

(Pet. 58 (emphasis added) (quoting Ex. 1004 ¶ 16)) and asserts that, during an active mode, the output of NAND gates G1–GN is based on both the Sleep signal (which is de-asserted high) and the outputs of memory cells C1–CN, which adjust the value of the output of the NAND gates G1–GN in accordance with the leakage measurements and adjustments made using the method of Figure 2. *Id.* (citing Ex. 1004 ¶ 16; Ex. 1002 ¶ 105). Petitioner argues that, because the value of the NAND gate output (the recited "control signal") depends on both the "Sleep signal" (the recited "mode indicator") and the output of memory cells C1–CN (the recited "leakage indicator"), Kim teaches "the control circuit being arranged to select the value of the control signal based on the mode indicator and on the leakage indicator," as recited in claim 1. *Id.* at 59.

Patent Owner makes two separate but related arguments against Petitioner's contentions—(1) the value of the NAND gate output (the recited "value of the control signal") does not depend on both the "Sleep signal" (the recited "mode indicator") and the output of memory cells C1–CN (the recited "leakage indicator") and (2) Kim's NAND gates do not "select" the value of the control signal, as recited in the claim. *See* PO Resp. 32–33. We address each of these arguments in turn.

First, Patent Owner asserts that Kim does not teach the claimed "control circuit arranged to select the value of the control signal" based on *both* "the mode indicator and on the leakage indicator," as recited in claim 1, because Kim's NAND gate "decides whether to pass through the bit pattern in the memory cells C1-CN, based solely on the value of the sleep signal." PO Resp. 33 (emphasis added). Citing the testimony of its declarant, Dr. Annavaram, Patent Owner contends that Kim's NAND gate operates such that "[i]f the sleep signal is 0, it does not pass through those bits and outputs all 1's instead; and if the sleep signal is low, it passes through the bit pattern with inversion." *Id.* (citing Ex. 2009 ¶ 84).

As discussed above in Section III.B (Claim Construction), Patent Owner argues that "select[ing] the value of the control signal based on the mode indicator and on the leakage indicator" recited in claim 1 requires the indicators to "play a role in deciding which of the multiple values will be chosen or picked." *Id.* at 31.[12] Patent Owner argues that the output of Kim's NAND gates (the claimed "control signal") is not "based on" the bit pattern in Kim's memory cells C1–CN (the claimed "leakage indicator") because "a bit pattern that is being passed through with inversion" does not "play a role" in selecting the value of the control signal. *Id.* at 31–32 (citing Ex. 2009 ¶ 82); *see also id.* at 33 (making the same argument, citing Ex. 2009 ¶¶ 80–82, 84, 85).

[12] As discussed in Section III.B, to the extent Patent Owner argues claim 1 requires selecting a value from or among a group of multiple values, we disagree with Patent Owner's argument. Claim 1 does not require selecting a value among several or multiple (i.e., more than two) values.

In reply, Petitioner asserts that Kim's sleep signal (the claimed "mode indicator") and the memory cell signal value (the claimed "leakage indicator") "play a role" in deciding what control signal value is chosen because when Kim's sleep signal indicates "an active mode," the outputs of Kim's NAND gates (the claimed "value of the control signal") are controlled by the values in cells C1–CN. Pet. Reply 11–12 (citing Pet. 57–59 (citing Ex. 1004 ¶ 16)).

We agree with Petitioner's argument and disagree with Patent Owner's argument. As Petitioner persuasively argues (Pet. Reply 11–12 (citing Pet. 57–59)), when the sleep signal is active (or 1), the output of Kim's NAND gates (the claimed "value of the control signal") would be different for different value of Kim's memory cells C1–CN (the claimed "leakage indicator") because, as Patent Owner concedes, the value of the output of Kim's NAND gates equals the value of Kim's memory cells C1–CN "with inversion" (*see* PO Resp. 33 (citing Ex. 2009 ¶ 84)).

During the oral hearing, Patent Owner acknowledged that, when the "bit pattern" of Kim's memory cells C1–CN is allowed to "pass through," the output of Kim's NAND gates will be different depending on the value of Kim's memory cells C1–CN.

> JUDGE CHUNG: If you have a different bit pattern, when the bit pattern is allowed to pass through, the different bit pattern [passed through] will affect the output, right?
>
> MS. ZHONG: With respect -- I'm sorry.
>
> JUDGE CHUNG: Go ahead.
>
> MS. ZHONG: Your Honor has the --

> JUDGE CHUNG: So my question is, isn't it the case the value of the bit pattern does have an effect on the output because depending on what the bit pattern is the output will be different?
> MS. ZHONG: Yes. So I think it comes back to what the claim language is. The claim language is a control circuit arranged to select a value. It's not a control circuit being arranged to produce or output a value. That's different. Select doesn't equal to produce or output.

Tr. 47:7–23. Because the output of Kim's NAND gates will be different depending on the value of Kim's memory cells C1–CN allowed to "pass through," we agree with Petitioner that the value of Kim's memory cells C1–CN (the claimed "leakage indicator") "plays a role" in deciding what the output of Kim's NAND gates (the claimed "value of the control signal") will be.

Moreover, Patent Owner acknowledged that the output of Kim's NAND gate is determined based on the inputs to the NAND gates (i.e., the sleep signal input and the memory cell signal input).

> JUDGE CHUNG: But, knowing a little bit about how a NAND gate works, isn't it the case that the input to the NAND gates, G1 through GN, with the input of the sleep signal and the C1 through CN signal, isn't it the case that input to the NAND gate determines what the output is?
> MS. ZHONG: Okay. So any logic gate, the output will depend on the input. That's for sure.

Tr. 44:18–25; *but see id.* at 45:3–10 (stating that even if the "output is in control of the input, . . . that does not mean the selection is based on that

input"). Thus, we find that Kim's NAND gate (the claimed "control circuit") operates to *determine* its output (the claimed "value of the control signal") based on its input of the sleep signal (the claimed "mode indicator") and the memory cell value input (the claimed "leakage indicator"). As discussed in Section III.B, the Specification indicates that "select[ing] the value of the control signal based on the mode indicator and on the leakage indicator" recited in claim 1 is synonymous to *determining* the value based on the recited indicators. *See* Ex. 1001, 4:4–11. Thus, the evidence of record shows that Kim teaches "the control circuit being arranged to select the value of the control signal based on the mode indicator and on the leakage indicator," as recited in claim 1.

As discussed above, Patent Owner asserts that the term "select" should be construed to mean "[t]o choose or pick out in preference to another or others." PO Resp. 25–27 (citing Ex. 3002). Patent Owner contend that Kim does not disclose the control circuit arranged to "select the value of the control signal based on the mode indicator and on the leakage indicator" under this construction. *See* PO Sur-reply 8–9.

We disagree with Patent Owner's argument. On the contrary, we find that Patent Owner's description of the operation of Kim's NAND gates—"[i]f the sleep signal is 0, it does not pass through those bits and outputs all 1's instead; and if the sleep signal is low, it passes through the bit pattern with inversion" (PO Resp. 33)—meets Patent Owner's proposed definition. That is, when the sleep signal (the claimed "mode indicator") is 0, the NAND gates choose the output to be a signal of all 1s (the claimed "value of the control signal") in preference to another value, e.g., the value determined by the output of the memory cells C1-CN. When, on the other hand, the

sleep signal is 1, the NAND gates choose the output to be a signal of the inverse (or complement) of the output of the memory cells C1-CN (the claimed "leakage indicator"), as opposed to another value, e.g., all 1s. Thus, Kim's NAND gates select the value of the control signal based on the mode indicator and on the leakage indicator even under Patent Owner's proposed construction of "select."

Petitioner argues that the '026 patent describes selecting the value of the control signal by a control circuit comprising "one or more logical gates," such as Kim's NAND gates. Pet. Reply 12–13 (citing Ex. 1001, 4:22–25; Ex. 1030 ¶¶ 21, 23–31, 34–36). In the cited portion of his Reply Declaration, Dr. Harris cites the following disclosures from the Specification

> In the shown example, the control circuit 50 includes a digital circuit 51 that is arranged to (i) *receive indicators (such as the mode indicator 104, the leakage indicator 105* and (ii) *send a digital control signal 108* to a digital to analog converter (DAC) 52. . . . The digital circuit 51 can include a storage element such as a register or multiple flip flops, can include one or more logical gates, can include a combination of a storage element and *one or more logical gates*, and the like.

Ex. 1030 ¶ 35 (emphases added) (citing Ex. 1001, 4:15–25). Dr. Harris testifies that "Kim's NAND gates exactly match the '026 patent's disclosed control circuit," producing the same output given the same inputs. *Id.* We are persuaded by Petitioner's argument and evidence that Kim's NAND gates are logical gates similar to the '026 patent's disclosed control circuit comprising one or more logical gates, producing the control signal output based on the inputs of the mode indicator and the leakage indicator.

For the foregoing reasons and based on the complete record, we determine that Petitioner has demonstrated sufficiently that Kim teaches "a

control circuit, connected to the mode indicator generator and the leakage indicator generator, for receiving the mode indicator and the leakage indicator, the control circuit being arranged to select the value of the control signal based on the mode indicator and on the leakage indicator," as recited in claim 1, notwithstanding the arguments from Patent Owner.

(ii) "a mode indicator generator for generating a mode indicator that indicates a desired mode of the power gated circuit"

Taking up next the recited "mode indicator" limitation, Petitioner asserts that Kim teaches "a mode indicator that indicates a desired mode of the power gated circuit," as recited in claim 1, because Kim describes a Sleep signal that indicates whether processor 502 will be in an active mode or a sleep mode. Pet. 41–42 (citing Ex. 1004 ¶ 16, Figs. 4, 5). Petitioner contends that setting Kim's Sleep signal to low (when processor 502 is in a sleep state) turns OFF all transistors in sleep transistor array P1–PN, whereas setting Kim's Sleep signal to high (when processor 502 is in an active state) turns ON at least some of Kim's sleep transistors P1–PN, and thereby provides the gated supply voltage VVCC to functional blocks within processor 502. *Id.* at 42–43 (citing Ex. 1004 ¶¶ 10, 16, 23). Petitioner argues that because Kim's Sleep signal indicates the desired mode (active or sleep) of functional blocks of processor 502 (the recited "power gated circuit"), that signal is "a mode indicator that indicates a desired mode of the power gated circuit." *Id.* at 43 (citing Ex. 1002 ¶ 85).

Turning next to the recited "mode indicator generator," although Petitioner argues that Kim teaches or suggests "a mode indicator," Petitioner appears to acknowledge that there is no express teaching in Kim of the "mode indicator generator" included in the recited "integrated circuit." *Id.* at

43–44. Petitioner asserts that a person of ordinary skill in the art would have understood that Kim includes a component that asserts and de-asserts (i.e., generates) the Sleep signal (the recited "mode indicator"), and that the allegedly included component is a "mode indicator generator." *Id.* (citing Ex. 1004, Fig. 4, ¶¶ 16, 25). Petitioner, however, does not contend that such a component is included in Kim's chip 100 or processor 502 (the recited "integrated circuit"). *Id.*

To remedy this deficiency, Petitioner relies on Lee. *Id.* at 45–50. Petitioner asserts that Lee teaches a deep power down unit 45 that generates a deep power down signal DPD that is either (1) de-asserted low, which indicates that a memory device is in an active/standby mode, or (2) asserted high, which indicates that the device is in a deep power down mode. *Id.* at 45 (citing Ex. 1005, claim 12, ¶¶ 57, 71). Petitioner provides a color-annotated version of Figure 4 of Lee (not reproduced herein) and, citing the testimony of Dr. Harris, asserts that a person of ordinary skill in the art would have understood that all components depicted in Figure 4, including deep down power unit 45 (annotated in blue in Petitioner's color-annotated version of Figure 4), are on the same integrated circuit. *Id.* at 46–47 (citing Ex. 1005, Fig. 4, ¶¶ 49, 50, 147–148, 155; Ex. 1002 ¶ 88).

Petitioner argues that it would have been obvious to a person of ordinary skill in the art to have Kim's system use an on-chip mode indicator generator, such as Lee's deep power down unit 45, to provide Kim's Sleep signal. Pet. 47. Petitioner asserts that Kim and Lee are in the same field, and both use similar approaches to produce a gated supply voltage by adjusting the resistance of a transistor array. *Id.* at 47–48 (citing Ex. 1004, Figs. 4, 5; Ex. 1005, Fig. 4). Petitioner further contends that Kim's Sleep

signal and Lee's deep power down signal do the same thing in that they both disconnect the output virtual supply from the input supply to power down the power gated circuit. *Id.* at 48 (citing Ex. 1004 ¶ 16; Ex. 1005 ¶ 101, claim 12; Ex. 1002 ¶ 89). Petitioner argues that a person of ordinary skill in the art, therefore, would have found it obvious to use Lee's teaching of on-chip deep power down unit 45 to provide Kim's Sleep signal because doing so would have involved nothing more than combining well-known elements (high and low control signals) to produce a predictable result (switching a circuit between modes). *Id.* at 49. Petitioner contends that Kim's circuit would have responded to Kim's Sleep signal in the same way regardless of whether the component providing the Sleep signal was on-chip or off-chip. *Id.*

Petitioner contends that a person of ordinary skill in the art would have been motivated by Kim's teaching to incorporate Lee's teaching of an on-chip mode indicator generator because, as recognized by Kim, the trend in chip manufacturing before the claimed invention was to develop technologies that would allow "devices of smaller size [to] be manufactured." Pet. 49 (citing Ex. 1004 ¶ 25). Petitioner further argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Kim and Lee to place the source of Kim's Sleep signal on chip 100, i.e., use an on-chip Sleep signal generator in Kim, based on "the long-standing understanding pervasive in the semiconductor industry that it is advantageous (to save space and cost) to add more functionality onto each chip." *Id.* (citing Ex. 1013, 115; Ex. 1002 ¶ 92).

Patent Owner contends that Lee's DPD signal generator unit 45 is not the claimed "mode indicator generator." PO Resp. 51–53; PO Sur-reply 11–

13. Patent Owner asserts that Lee uses two separate signals, BLK_f1 and DPD, to select between "Active," "Standby," and "Deep Power Down" modes. PO Resp. 52.

To illustrate its argument, Patent Owner reproduces a table from the Petition as follows.

BLK_f1	DPD	Mode
0	0	Standby
0	1	Deep Power Down
1	0	Active
1	1	Not Applicable

Id. (citing Pet. 75–76). The table above shows "how Lee selects [its] modes." Pet. 75–76; PO Resp. 52 (citing Pet. 75–76).

Patent Owner asserts that, as illustrated in the table above, in Lee "indicating a desired mode requires a combination of the DPD signal and the BLK_f1." PO Resp. 52–53. Patent Owner argues Lee's DPD unit 45 generates only a single bit DPD signal and therefore cannot generate Lee's mode indicator that requires two bits—the BLK_f1 bit and the DPD bit. PO Sur-reply 12.

Petitioner, however, does not rely on Lee's DPD unit 45 to teach "a mode indicator generator" recited in claim 1. Rather, as discussed above, Petitioner relies on Kim's Sleep signal to teach the claimed "mode indicator" and combines this teaching of Kim with Lee's teaching of on-chip DPD signal generator to place the source of Kim's Sleep signal on chip 100, i.e., to obtain an on-chip Sleep signal generator (the claimed "mode indicator

generator") in the proposed combination of Kim and Lee. Pet. 49; *see also* Pet. Reply 15 ("Lee's teaching of an on-chip deep power down unit generating a DPD signal would have motivated a [person of ordinary skill in the art] to modify Kim to incorporate an on-chip mode indicator generator." (citing Pet. 44–50)). Patent Owner's argument is inapposite because it does not address the combination proposed by Petitioner.

Although Patent Owner is correct that Lee uses both the DPD signal and the BLK_f1 signal to switch between Lee's "Active," "Standby," and "Deep Power Down" modes, the table reproduced above also shows that, when the BLK_f1 signal is set to 0, the DPD signal switches Lee's modes between the "Standby" and "Deep Power Down" modes. *See* Pet. 75–76; PO Resp. 52. Thus, we agree with Petitioner that Lee's DPD unit 45 teaches an on-chip signal source that generates signals indicating some of Lee's modes under certain circumstances (i.e., when BLK_f1 is set to 0). For the reasons explained by Petitioner, we agree with Petitioner that a person of ordinary skill in the art would have been motivated to combine this teaching of Lee with Kim's teaching of the Sleep signal (the claimed "mode indicator") to place the source of Kim's Sleep signal on Kim's chip 100, i.e., to obtain an on-chip Sleep signal generator (the claimed "mode indicator generator") in the proposed combination of Kim and Lee.

To the extent Patent Owner argues that Petitioner's proposed combination does not include Lee's exact teaching of using both the DPD signal and the BLK_f1 signal to provide a full range of Lee's mode switching, there is no requirement that a proposed combination include all (or a full range) of the teachings from a reference. Nor is it required that teachings from references must be combined without modification. *See*

ClassCo, Inc. v. Apple, Inc., 838 F.3d 1214, 1219 (Fed. Cir. 2016) ("*KSR* does not require that a combination only unite old elements without changing their respective functions."). Indeed, "[o]ur obviousness framework permits modifying one reference and combining it with a second reference." *Google LLC v. Ji-Soo Lee*, 759 F. App'x 992, 997 (Fed. Cir. 2019) (nonprecedential) (citing *Smith & Nephew, Inc. v. Rea*, 721 F.3d 1371, 1380–81 (Fed. Cir. 2013)). Thus, we discern nothing improper in Petitioner's proposed combination of Kim's teaching of the Sleep signal with Lee's teaching of on-chip DPD signal generator to obtain an on-chip Sleep signal generator.

Patent Owner further asserts that Petitioner's proposed combinations for claims 5 and 7 require a "mode indicator generator" that generates both the DPD signal and the BLK_f1 signal and, therefore, in order to prevail on claims 1, 5, and 7, Petitioner must rely on the same structure from Lee for all of the claims. *See* PO Resp. 53–54; PO Sur-reply 11–12. We need not address this issue here because we address any impact of this analysis on claims 5 and 7 in our discussion of those claims.

Finally, Patent Owner contends because the named inventors of Kim had above-average skill levels at the time of Kim's filing, any feature not described in Kim, such as an on-chip mode indicator, had a "sound reason" for the omission. PO Resp. 55 (citing Ex. 2009 ¶¶ 25–27). Petitioner responds that Kim's skill level is irrelevant to the patentability analysis relying on Kim. Petitioner argues that what is relevant is the skill level of a person of ordinary skill in the art reading Kim. We agree with Petitioner's argument. *See Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1374 (Fed. Cir. 2011) ("Whether prior art invalidates a patent claim as

obvious is determined from the perspective of one of ordinary skill in the art.").

For the foregoing reasons and based on the complete record, we determine that Petitioner has demonstrated sufficiently that the combination of Kim and Lee teaches "a mode indicator generator for generating a mode indicator that indicates a desired mode of the power gated circuit," as recited in claim 1, and has articulated sufficient reasoning with rational underpinning for combining Kim and Lee to arrive at the subject matter of this claim limitation.

c. Conclusion on Claim 1

In consideration of the foregoing and based on the complete record, we are persuaded by Petitioner's arguments and evidence, notwithstanding Patent Owner's arguments, addressed above. Having weighed each of the *Graham* factors, including the scope and content of the prior art, and the differences between the prior art and the challenged claim, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 1 is unpatentable under 35 U.S.C. § 103(a) over the combination of Kim and Lee.

5. Dependent Claim 2

Claim 2 depends from claim 1 and further recites

> wherein the control circuit is arranged to:
>
> select a performance value of the control signal when (i) the leakage indicator indicates that a leakage of the power gated circuit is below a low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at a performance oriented mode;
>
> select a leakage reduction value of the control signal when (i) the

> leakage indicator indicates that the leakage of the power gated circuit is above the low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at the performance oriented mode; and
>
> select a shut down value of the control signal when the mode indicator indicates that the power gated circuit should be shut down.

Ex. 1001, 15:34–50.

Petitioner contends that Kim teaches the additionally recited limitations of claim 2. Pet. 59–63. As discussed above in Section III.C.4.b(i), Petitioner asserts that Kim teaches that the value of the collective output of NAND gates G1–GN (the recited "control signal") is selected based on the Sleep signal (the recited "mode indicator") and the output of memory cells C1–CN (the recited "leakage indicator"). *Id.* at 57. Addressing the additionally recited limitations of claim 2, Petitioner contends that Kim also teaches selecting various values of the control signal as recited in claim 2, when the "leakage indicator" and the "mode indicator" indicate the recited conditions. *Id.* at 59–63.

As an initial matter, Dr. Harris illustrates exemplary values for the outputs of Kim's NAND gates G1–GN for the case of N=5, i.e., when there are 5 NAND gates in Kim's chip 100, by providing a table in his Declaration.

Table A provided by Dr. Harris in paragraph 108 of his Declaration is reproduced below.

	G1	G2	G3	G4	G5
Sleep Mode Shutdown Value	1	1	1	1	1
Retention Mode[6]: 1 transistor ON Retention Value 2	0	1	1	1	1
Retention Mode: 2 transistors ON Retention Value 1	0	0	1	1	1
Active Mode: 3 transistors ON Leakage Reduction Value 2	0	0	0	1	1
Active Mode: 4 transistors ON Leakage Reduction Value 1	0	0	0	0	1
Active Mode: 5 transistors ON Performance Value	0	0	0	0	0

Ex. 1002 ¶ 108 (Table A). Table A provided by Dr. Harris illustrates various values of the collective output of Kim's NAND gates G1–G5 during various modes of Kim's processor or chip. *Id.*; *see also* Pet. 59 (citing Ex. 1002 ¶¶ 107–111).

In his Declaration, Dr. Harris explains that

> As shown in Table A, during Kim's sleep mode, all of the NAND gates output a High, or digital "1" signal. . . . This turns OFF all of Kim's transistors P1-PN during sleep mode. Other values of Kim's NAND gates outputs, i.e., when at least one of the NAND gates outputs a Low, or digital "0" signal, correspond to Kim's active mode. . . . When at least one of the NAND gates outputs a Low, then at least one of the transistors P1-PN are ON, providing a conduction path between the input supply voltage VCC and the virtual supply voltage VVCC.

Ex. 1002 ¶ 109 (citing Ex. 1004 ¶ 16).

As discussed above in our overview of Kim (Section III.C.2) and also discussed in the Petition, Kim teaches determining suitable combinations of

transistors in the sleep transistor array by executing routine 201 during a test phase of manufacturing. *See* Ex. 1004 ¶¶ 20, 22; *see also* Pet. 21 (citing Ex. 1004 ¶¶ 14, 20, 22). Once determined, the combination may be saved in a register. Ex. 1004 ¶¶ 20, 22. Petitioner asserts that Kim uses the configuration information determined from the testing phase (stored in a register) during an active state of normal operation to "determine which of NAND gates G1-GN output low or high signals, which in turn determines which sleep transistors P1-PN are ON and OFF." Pet. 21–22 (citing Ex. 1004 ¶ 16; Ex. 1002 ¶ 54).

Addressing the recitation "the control circuit is arranged to: select a performance value of the control signal when (i) the leakage indicator indicates that a leakage of the power gated circuit is below a low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at a performance oriented mode," Petitioner asserts that Kim's testing operation when the chip under testing is found to not have excessive leakage prior to testing and subsequent normal operation during an active mode using such test results teach these limitations. Pet. 59–61. First, Petitioner argues that because Kim's routine 201 starts with turning ON all sleep transistors P1–PN, if a functional block of processor 502 (the claimed "power gated circuit") is found to not have excessive leakage at the very first execution of Kim's step 206, the output from cells C1–CN would have the value of all ones (1s) after completion of routine 201. *Id.* at 60 (citing Ex. 1004 ¶ 20; Ex. 1002 ¶ 112); *see also id.* at 53 (describing the same cell value determination). In other words, according to Petitioner and Dr. Harris, Kim discloses that if the leakage level of functional blocks of the chip (the recited "power gated circuit"), as found, is determined to be *not*

excessive (i.e., "below a low leakage threshold" as recited in the claim) during testing, Kim's memory cell value determined at the end of testing would be all ones (1s). *See id.* at 53, 60; Ex. 1002 ¶ 112.

Dr. Harris further explains that Kim describes that when this stored value is used to drive the output of memory cells C1–CN (the "leakage indicator" indicating "a leakage of the power gated circuit is below a low leakage threshold" as recited in the claim) during an active mode of normal operation, i.e., when the Sleep signal (the recited "mode indicator") is High during normal operation, the value of the output of NAND gates G1–GN would be all zeroes (0s) (i.e., selecting "a value of the control signal" of all 0s), causing all of the sleep array transistors to be turned ON. Ex. 1002 ¶ 113. This in turn would cause the sleep transistor array (the recited "power gating switch") to have maximum conductance and supply a highest output voltage (VCC or close to VCC) to "the chip []or functional block supplied by the sleep transistor's virtual supply[]," allowing the processor to have the highest speed. *See* Pet. 36 (citing Ex. 1004 ¶ 18); Ex. 1002 ¶¶ 76, 111. Thus, Petitioner argues Kim's all zeroes (0s) output of NAND gates G1–GN teaches "a performance value of the control signal" recited in claim 2. Pet. 60. Petitioner argues, therefore, Kim's normal operation using memory cells C1–CN having the value of all ones (1s) teaches "the control circuit is arranged to: select a performance value of the control signal when (i) the leakage indicator indicates that a leakage of the power gated circuit is below a low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at a performance oriented mode," as recited in claim 2. *Id.* at 60–61 (citing Ex. 1002 ¶¶ 113–114).

Petitioner presents similar arguments and evidence in its contention that Kim teaches "the control circuit is arranged to: . . . select a leakage reduction value of the control signal when (i) the leakage indicator indicates that the leakage of the power gated circuit is above the low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is requested to operate at the performance oriented mode," as recited in claim 2, except that Petitioner relies on Kim's testing that results in the output of memory cells C1–CN having some zeroes (0s) because the chip (or functional block of the chip) tested, as found, was determined to have a leakage level that is excessive, i.e., "above the low leakage threshold" as recited in claim 2. Pet. 61–62 (citing Ex. 1004 ¶¶ 16–20; Ex. 1002 ¶¶ 115–117). Similar to our discussion above, Petitioner asserts that when Kim's testing-determined memory cell value having some 0s is used to drive the NAND gates G1–GN during an active mode of normal operation (i.e., when the Sleep signal is High), the NAND gates turn some sleep transistors ON and turn others OFF, which will decrease the conductance of the sleep transistor array and increase the difference between VCC and VVCC. *Id.* at 37 (citing Ex. 1004 ¶¶ 16, 18–20; Ex. 1002 ¶ 77), 61–62 (citing Ex. 1004 ¶¶ 16–20; Ex. 1002 ¶¶ 115–117). Thus, Petitioner argues the value of the output of NAND gates G1–GN with some zeroes (0s) and some ones (1s) teaches "a leakage reduction value of the control signal" recited in claim 2. *Id.* at 61–62. Petitioner asserts, therefore, during normal operation using memory cells C1–CN having some zeroes (0s), Kim's NAND gates G1–GN "select a leakage reduction value of the control signal when (i) the leakage indicator indicates that the leakage of the power gated circuit is above the low leakage threshold and (ii) the mode indicator indicates that the power gated circuit is

requested to operate at the performance oriented mode," as recited in claim 2. *Id.*

Addressing the recitation "the control circuit is arranged to: . . . select a shut down value of the control signal when the mode indicator indicates that the power gated circuit should be shut down," Petitioner asserts that Kim teaches this limitation when Kim's Sleep signal is Low during the sleep mode of normal operation. Pet. 63 (citing Ex. 1004 ¶¶ 9, 16; Ex. 1002 ¶¶ 118–119). Petitioner contends Kim teaches that "when the Sleep signal is asserted (Low) . . ., the NAND gates G1 to GN all output a High" (*id.* (citing Ex. 1004 ¶ 16)) and "[t]hat value of the NAND gates turns OFF all of the PMOS transistors and shuts down the function blocks of processor 502" (*id.* (citing Ex. 1004 ¶¶ 9, 16)). Petitioner argues that an output of all ones from NAND gates G1–GN is therefore a "shut down value of the control signal," as recited in claim 2, because it turns OFF the array of sleep transistors and disconnects the processor (or the functional block of the processor) from the supply voltage VCC. *Id.* (citing Ex. 1002 ¶¶ 118–119).

Patent Owner makes several arguments disputing Petitioner's contentions. PO Resp. 33–51; PO Sur-reply 13–18.

First, Patent Owner asserts that claim 2 recites a control circuit that is arranged to select at least three different types of control signal values—"a performance value," "a leakage reduction value," and "a shutdown value." PO Resp. 33–34. Patent Owner contends that Kim's NAND gates G1–GN (the clamed "control circuit"), however, can output at most two values (the claimed "value of the control signal") during the entire product life of "each of Kim's processors" because Kim's NAND gates output either all 1s (when the Sleep signal is 0) or the bit pattern (or its complement) stored in Kim's

memory cell C1–C2, which has a fixed value determined during the testing phase. *Id.* at 35–36 (citing Ex. 1004 ¶¶ 16, 20, 22; Ex. 2009 ¶ 92).

Petitioner responds by citing the disclosures in the Specification of the '026 patent that describe the same or similar method of determining a fixed value of the leakage indicator during testing, which is thereafter used during the normal operation. Pet. Reply 16–17 (citing Pet. 54; Ex. 1001, 3:61–67). Petitioner reproduces the relevant passage as follows.

> The leakage indicator generator 45 can include, for example: ***fuses***, ***one time programmable element*** or other programmable elements that can be programmed ***to reflect the determined leakage***. The leakage indicator 105 can, for example, indicate whether ***the integrated circuit 10*** has a leakage level that ***corresponds to a best process case, typical process case or worst process case***."

Id. (quoting Ex. 1001, 3:61–67). Petitioner argues that in the '026 patent, just as in Kim,

> In any particular instance of such a device, that single fixed value of the leakage indicator will result in the control circuit selecting ***either*** the performance value of the control signal or the leakage reduction value of the control signal, ***but not both*** (the control circuit would also select the shut down value of the control signal when the mode indicator indicated a shut down mode).

Id. at 17–18 (citing Ex. 1030 ¶¶ 43–46). Petitioner argues, therefore, claim 2 does not require "a particular control circuit (e.g., a particular instance of a manufactured circuit) to select both a performance value of the control signal ***and*** a leakage reduction value." *Id.* at 16.

Patent Owner responds that, if the embodiment of the '026 patent cited by Petitioner describes "control circuits that are arranged to select only one of a performance value or a leakage reduction value during the entire

device life, then they would also fall outside the claim scope." PO Sur-reply 14–15 (citing *Intamin Ltd. v. Magnetar Techs., Corp.*, 483 F.3d 1328, 1336–37 (Fed. Cir. 2007)).

We disagree with Patent Owner that Kim's NAND gates must select all three recited control signal values in order to satisfy the limitations of claim 2.

Claim 2 does *not* recite that "the control circuit selects" "a performance value," "a leakage reduction value," and "a shut down value." Rather, claim 2 recites that "the control circuit is *arranged to*" select the recited values. Ex. 1001, 15:34–50 (emphasis added). Thus, the claim language indicates that claim 2 requires the recited "control circuit" be *capable of* selecting the recited values when the conditions recited in the claim are met. This interpretation of claim 2 is consistent with the Specification, which describes as follows:

> [T]he control circuit 50 ***may*** *select the performance value* of the control signal 103 *when* the leakage indicator 105 indicates that the integrated circuit 10 is slow (and hence exhibit less leakage) in comparison to most integrated circuits of a batch of integrated circuits that includes the integrated circuit 10. Similarly, the control circuit 50 ***may*** *select the leakage reduction value* of the control signal 103 *when* the leakage indicator 105 indicates that the integrated circuit 10 is fast (and hence has high leakage) in comparison to most integrated circuits of a batch of integrated circuits that includes the integrated circuit 10.

Ex. 1001, 4:59–5:2 (emphases added). The use of permissive word "may" in the Specification to describe selecting a performance value or a leakage reduction value depending on whether the gated integrated circuit is slow or fast in comparison to other integrated circuits in a batch of integrated circuits indicates that the '026 patent contemplates the control circuit be *capable of*

selecting a performance value or a leakage reduction value and does not necessarily require the control circuit select both the performance value and the leakage reduction value during the normal operation.

In view of the claim language and the Specification, we interpret claim 2 to require the recited "control circuit" only be *capable of* selecting the recited values when the conditions recited in the claim are met. This interpretation of claim 2 is consistent with the embodiment of the '026 patent cited by Petitioner, where the leakage level measured during testing or manufacturing is saved in fuses or "one time programmable element" to be used as a leakage indicator during the normal operation of the circuit. *See* Pet. Reply 16–17 (citing Pet. 54; Ex. 1001, 3:61–67). "A claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct." *Network-1 Techs., Inc. v. Hewlett-Packard Co.*, 981 F.3d 1015, 1024 (Fed. Cir. 2020) (quoting *MBO Labs., Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007)); *see also GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1311 (Fed. Cir. 2014) ("[W]here claims can reasonably [be] interpreted to include a specific embodiment, it is incorrect to construe the claims to exclude that embodiment, absent probative evidence on the contrary." (quoting *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1277 (Fed. Cir. 2008)). Here, Patent Owner does not point to any intrinsic evidence, such as express claim language, or statements made during prosecution or in the Specification that indicate the patentee's intent to exclude the disclosed embodiment from the scope of claim 2.

Petitioner asserts, and Patent Owner does not dispute, claim 2 does not require "a particular instance of a manufactured circuit" to select all

three recited values of the control signal. *See* Pet. Reply 16; PO Sur-reply 14 ("Petitioner mischaracterizes Patent Owner's argument as requiring 'a particular instance of a manufactured circuit' 'to select both a performance value of the control signal and a leakage reduction value.' . . . Not so. Patent Owner's argument is that Kim's NAND gates 'only output at most two values [during] [the device's] entire product life.'"). We determine that Kim teaches the recited limitations of claim 2 because Kim's NAND gates are *capable of* outputting three different values of the control signal that Petitioner alleges correspond to "a performance value," "a leakage reduction value," and "a shut down value" during the device's entire product life.

Thus, we find that Kim teaches a control circuit "arranged to" select "a performance value," "a leakage reduction value," and "a shut down value" when the conditions recited for each value are met.

Next, Patent Owner argues that the bit patterns stored in Kim's memory cells are merely passed through the NAND gates (PO Resp. 34, PO Sur-reply 16) and Kim therefore does not teach the selections recited in claim 2 because "such pass-through does not involve 'choos[ing] or pick[ing] out [a control signal value] in preference to another or others' by the control circuit based on the leakage indicator" (PO Sur-reply 16).

We disagree with Patent Owner's argument for the reasons discussed above in Section III.C.4.b(i). As discussed in the same section, when the sleep signal (the claimed "mode indicator") is 0, Kim's NAND gates choose the output to be a signal of all 1s (the claimed "value of the control signal") in preference to another value, e.g., the value determined by the output of the memory cells C1–CN. When, on the other hand, the sleep signal is 1, the NAND gates choose the output to be a signal of the complement of the

output of the memory cells C1–CN (the claimed "leakage indicator"), as opposed to another value, e.g., all 1s. Thus, Kim's NAND gates select the value of the control signal based on the mode indicator and on the leakage indicator even under Patent Owner's proposed construction of "select."

Kim also teaches the limitations of claim 2 under the modified IEEE dictionary definition discussed above—"identify[ing]" or picking "an item" that "meets a particular criterion." Based on the evidence presented by Petitioner, Kim's NAND gates are arranged to identify or pick (or determine) the output value of all 0s (the claimed "performance value of the control signal") when the following criteria or conditions are met: (i) Kim's memory cells C1–CN (the claimed "leakage indicator") have the value of all 1s, indicating the leakage of the functional blocks of processor 502 is below a leakage threshold (as determined at the end of testing and saved in the cells or register) and (ii) the Sleep signal (the claimed "mode indicator") is High, indicating the active mode (the claimed "performance oriented mode). *See* Pet. 59–61 (citing Ex. 1004 ¶¶ 16, 18, 20, Ex. 1002 ¶¶ 112–114). Kim's NAND gates are also arranged to identify or pick the output value of some 0s (the claimed "leakage reduction value of the control signal" when the following criteria or conditions are met: (i) Kim's memory cells C1–CN (the claimed "leakage indicator") have the value of some 0s and some 1s, indicating the leakage of the functional blocks of processor 502 is above a leakage threshold and (ii) the Sleep signal is High, indicating the active mode (the claimed "performance oriented mode). *See id.* at 61–62 (citing Ex. 1004 ¶¶ 16–20, Ex. 1002 ¶¶ 115–117). In addition, Kim's NAND gates are arranged to identify or pick the output value of all 1s (the claimed "shut down value of the control signal") when the following criterion or condition

is met: the Sleep signal (the claimed "mode indicator") is Low, indicating the function blocks of processor 502 is to be shut down. *See id.* at 63 (citing Ex. 1004 ¶¶ 9, 16; Ex. 1002 ¶¶ 118–119).

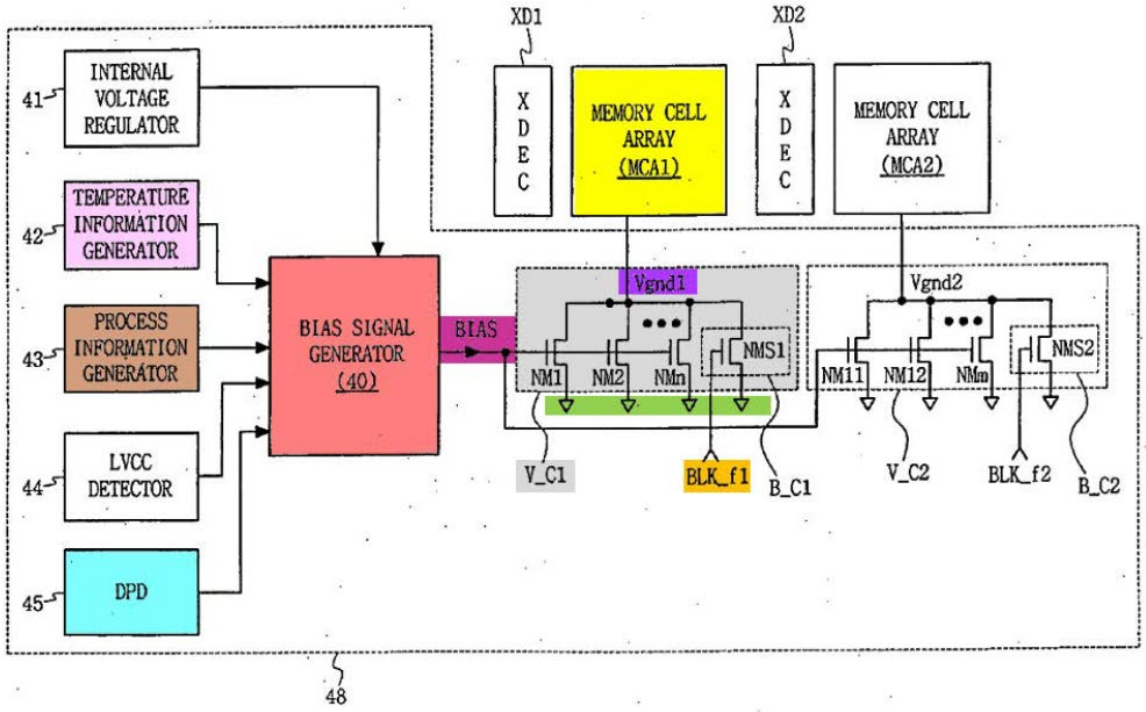
Based on the foregoing and considering the complete record, we find that Petitioner has demonstrated sufficiently Kim teaches the additionally recited limitations of claim 2. Accordingly, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 2 is unpatentable under 35 U.S.C. § 103(a) over the combination of Kim and Lee.

6. Dependent Claims 4 and 7

Claims 4 and 7 depend directly or indirectly from claim 2 and each further recites that the control circuit is arranged to select the leakage reduction value (claim 4) or the retention value (claim 7) "based on a temperature of the integrated circuit and on the leakage indicator." Ex. 1001, 15:55–59 (claim 4), 16:1–4 (claim 7). For both of these claims, Petitioner relies on Lee to teach using temperature as a stimulus for selecting the value of a control signal. Pet. 64–68 (claim 4), 79–83 (claim 7).

Figure 4 of Lee, as annotated by Petitioner in different colors, is reproduced below.

FIG. 4



Pet. 65. Annotated Figure 4 of Lee reproduced above shows Petitioner's identification of various circuits or circuit components of Lee's standby leakage current reduction circuit. *Id.* at 65 (citing Ex. 1005 ¶ 50, Fig. 4).

Petitioner asserts that Lee uses a virtual ground controller comprising NMOS transistors NM1 to NMn (annotated in grey) to control the level of a virtual ground Vgnd1 (annotated in purple) for memory cells (annotated in yellow). Pet. 66. According to Petitioner, Lee's bias signal generator (annotated in red) adjusts the signal BIAS (annotated in magenta) to determine the conductivity of NMOS transistors NM1–NMn, which in turn control the voltage apparent applied to the memory cells. *Id.* at 66–67 (citing Ex. 1005 ¶¶ 52, 54, 58, 61, 65; Ex. 1002 ¶ 123). Petitioner contends

that Lee's bias signal generator (red) sets the BIAS signal (and thereby determines the conductivity of the ground controller, i.e., the NMOS transistor array) based on multiple information sources including temperature information generator 42 (annotated in pink). *Id.* at 67–68 (citing Ex. 1005 ¶¶ 50–57, 81).

Petitioner asserts that it would have been obvious to a person of ordinary skill in the art to "use in Kim the technique of Lee of selecting the control signal based on temperature." Pet. 69 (citing Ex. 1004, Fig. 4; Ex. 1005, Fig. 4). According to Petitioner, "Lee . . . uses temperature as a stimulus to compensate for such temperature induced changes by adjusting its *control signal (BIAS)*." *Id.* (emphasis added) (citing Ex. 1005, Fig. 4, ¶ 54). Petitioner contends that it would have been obvious and beneficial to use temperature, as taught by Lee, as an additional stimulus in Kim "to determine a suitable array of enabled *sleep transistors*" to provide increased control of Kim's virtual supply voltage VVCC. *Id.* (emphasis added) (citing Ex. 1004 ¶ 22; Ex. 1005, Fig. 4, ¶ 54).

Patent Owner contends that, in order to show obviousness, "Petitioner must point to specific disclosures in prior art for material limitations to avoid hindsight bias and to ensure that obviousness analysis is specific to the claims at issue" and argues that Petitioner's reliance on a broad concept of "incorporat[ing] a temperature factor" from Lee is insufficient to demonstrate unpatentability of claim 4. *See* PO Resp. 56–57 (citing *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1365–66 (Fed. Cir. 2016) and characterizing *Arendi*'s finding as "while prior art supports the broader notion of searching for data in a database, [p]etitioner has failed to show why it would be *common sense* for the 'Add to address book' function to

operate by search for phone numbers as claimed" (emphasis added) (internal quotation marks omitted)). Patent Owner further asserts that "obviousness requires a showing of a specific reason to combine and *not what could be done generally* in the abstract." PO Sur-reply 21 (emphasis added) (citing *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012)). Based on the complete record, we understand Patent Owner to argue that relying on Lee as the source of what was well-known in the prior art—the general concept of using temperature to modify a control signal—is insufficient and that Petitioner instead must identify specific teachings of Lee it relies on in order to demonstrate obviousness based on Lee and Kim in this case.

We agree with Patent Owner that relying on Lee only for the generally well-known concept of using temperature is insufficient to demonstrate obviousness of claims 4 and 7 under the facts and circumstances of this case. *See Arendi*, 832 F.3d at 1363 ("In cases in which 'common sense' [or general knowledge in the art] is used to supply a *missing* limitation, *as distinct from a motivation to combine* . . . our search for a reasoned basis for resort to common sense must be searching." (emphases added)). In *Arendi*, the Federal Circuit found that common sense or general knowledge in the art may not provide a limitation missing from the prior art when the limitation at issue "plays a major role in the subject matter claimed," rather than, "the limitation in question [is] unusually simple and the technology particularly straightforward." *Id.* at 1362. In this case, we find that selecting the leakage reduction value or the retention value of the control signal "based on a temperature of the integrated circuit," as recited in claims 4 or 7, "plays a major role" in the subject matter of these claims. In addition, as

demonstrated below by Petitioner's proposed modifications to Kim to incorporate teachings of Lee, the technology at issue here is far from "straightforward"; rather, it is highly complex. Under the particular facts and circumstances of this case, we determine that relying on Lee only for the generally well-known concept of using temperature is insufficient to demonstrate obviousness of claims 4 and 7.

Petitioner asserts that it relies on "[i]ncorporating Lee's teaching of adjusting a power gate," i.e., Lee's teaching of adjusting its "control signal (BIAS)" (Pet. 70), to adjust the conductivity of Lee's sleep transistors NM1–NMn (*id.* at 69 (citing Ex. 1005, Fig. 4, ¶ 54)). Petitioner further contends that "the Petition provides examples of how a combined system of Lee and Kim would have been designed." Pet. Reply 26 (citing Pet. 63–73; Ex. 1002 ¶¶ 120–138). In the cited portion of the Petition, Petitioner relies on the testimony of Dr. Harris and explains how Petitioner proposes to combine specific teachings of Lee with Kim. *See* Pet. 71–72 (citing Ex. 1002 ¶¶ 130–135). Specifically, Petitioner contends that a person of ordinary skill in the art would have understood that

> to account for temperature in Kim's system, Kim would have been modified, for example, to: 1) store values in *registers C1 to CN* using Kim's Figure 2 method at various temperatures, and 2) select from the stored values based on the "stimulus" of a detected temperature during operation as taught by Lee.

Pet. 71–72 (emphasis added) (citing Ex. 1002 ¶¶ 130–135). In his Declaration, Dr. Harris illustrates an example of such modification of Kim using a modified Figure 4 of Kim, which he labels as Figure A. Ex. 1002 ¶ 130.

Figure A presented by Dr. Harris in his Declaration is reproduced below.

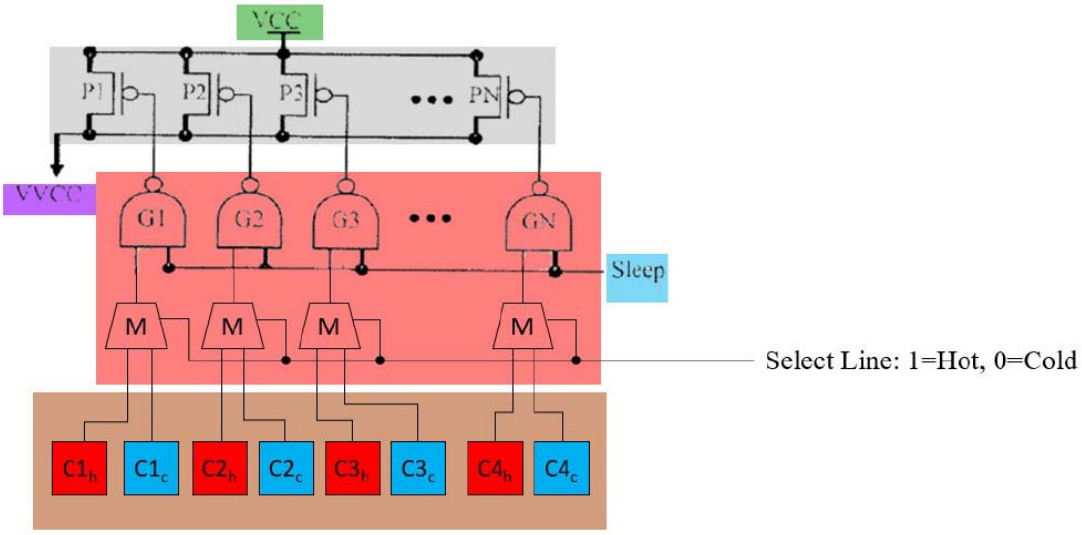


Figure A

Ex. 1002 ¶ 130. Figure A reproduced above shows Dr. Harris's proposed modification to Figure 4 of Kim to incorporate Lee's teaching of altering the control signal based on temperature. *Id.*

Referencing Figure A, Dr. Harris proposes modifying the circuit of Kim's Figure 4 (including an array of sleep transistors P1–PN, NAND gates G1–GN, and memory cells C1–CN) by replacing memory cells C1–CN with cells $C1_h$–$C4_h$ (red) and $C1_c$–$C4_c$ (blue), adding multiplexors M between the NAND gates G1–GN and the memory cells, and adding a temperature indicator line. Ex. 1002 ¶¶ 131–132. According to Dr. Harris, this modification would have allowed changing the output of the NAND gates G1–GN (i.e., the claimed "control signal"), turning different sleep transistors P1–PN on or off, based on the temperature indicator. *Id.* ¶ 131.

We are not persuaded by Petitioner's argument and evidence. First, although Petitioner proposes "[s]ubstituting Lee's inputs of leakage current and temperature for generating a power gate control signal" (i.e., Lee's

"control signal (BIAS)") for "Kim's inputs of leakage current and other 'stimuli' for generating a power gate control signal" (Pet. 70 (citing Ex. 1002 ¶ 129)), neither Petitioner nor Dr. Harris explains adequately how they are proposing to "substitute" Kim's control signal with Lee's "control signal (BIAS)."

For example, Figure A reproduced above does not show how Petitioner or Dr. Harris proposes to use Lee's "control signal (BIAS)" in the proposed combination. Petitioner asserts that "[a]lthough *Lee's control signal is analog and Kim's control signal is digital*, it was well known to apply teachings in an analog domain to a digital domain, and *conversions between analog and digital* domains were easy to implement." Pet. 72 (emphases added) (citing Ex. 1002 ¶ 136; Ex. 1015). Dr. Harris similarly states that

> Figures A and B show examples of obvious ways *to use in Kim's system Lee's teaching* of setting conductance of the array based on temperature. A POSA would have found both of these ways obvious. That Lee uses an analog control signal and Kim uses a digital control signal would have presented no obstacle to a POSA. . . . That is, *converting analog circuit elements and signals to digital was well known* long before the '026 patent.

Ex. 1002 ¶ 136 (emphases added) (citing (Ex. 1015) ("Analog-to-digital converters (ADC's) are ubiquitous, critical components of software radio and other signal processing systems.")). But Dr. Harris does not explain adequately how "to use in Kim's system" the digitized BIAS signal of Lee. *See id.* The only additional input signal shown in Figure A compared to Figure 4 of Kim is the temperature line that has the value of 0 when the temperature is cold and the value of 1 when the temperature is hot. *See* Ex. 1002 ¶ 130 (Fig. A). There is no explanation of how the modified

teaching of the BIAS signal of Lee (i.e., modified or converted to a digital signal) would have worked in the proposed combination of Figure A.

Nor does Petitioner explain adequately how the digitized BIAS signal of Lee would have been applied to the circuit of Kim to arrive at the subject matter recited in claim 4 and claim 7. *See* Pet. 69–73; Ex. 1002 ¶¶ 136–138. *Cf. Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) ("[T]he Board nowhere clearly explained, or cited evidence showing, *how the combination of the two references was supposed to work*. At least in this case, such a clear, evidence-supported account of the *contemplated workings of the combination* is a *prerequisite* to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so." (emphases added)).

According to the Federal Circuit,

> The amount of explanation needed to meet the governing legal standards—to enable judicial review and to avoid judicial displacement of agency authority—necessarily depends on context. A brief explanation may do all that is needed if, for example, the technology is simple and familiar and the prior art is clear in its language and easily understood. On the other hand, complexity or obscurity of the technology or prior-art descriptions may well make more detailed explanations necessary.

Id. (internal citation omitted). We find that this case falls into the latter category. Given the level of ordinary skill proposed by Petitioner (which we have adopted) and the complexity of the operation and design of the circuits of Kim and Lee, it was incumbent upon Petitioner to explain sufficiently how Lee's method of applying the analog BIAS signal to the NMOS sleep transistors to change the conductivity of the sleep transistor array would

have been adapted and combined with Kim's method of controlling the conductivity of the sleep transistor array by digitally turning on or off each of the sleep transistor P1 to PN to arrive at the subject matter recited in claims 4 and 7.[13] Because Petitioner has failed to do so, we determine that Petitioner has not established sufficiently that a person of ordinary skill in the art would have been motivated to combine the teachings of Kim and Lee to achieve the claimed invention.

Accordingly, for the foregoing reasons and based on the complete record, we determine Petitioner does not demonstrate by a preponderance of the evidence that the subject matter of claim 4 and claim 7 would have been obvious over the proposed combination of Kim and Lee.

7. Dependent Claim 5

Claim 5 depends from claim 2 and further recites "wherein the control circuit is arranged to select a retention value of the control signal when the mode indicator indicates that the power gated circuit is requested to enter a retention mode." Ex. 1001, 15:60–63.

Similar to Petitioner's contentions on claims 4 and 7 discussed above, Petitioner relies on the combination of Lee and Kim to argue obviousness of claim 5 (Pet. 73–79) except that, for claim 5, Petitioner relies on the standby mode of Lee to teach the "retention mode" recited in claim 5. *Id.* at 74. According to Petitioner, in Lee's standby mode, transistors NM1–NMn operate in the transistor's active region and the level of the BIAS signal determines the level of virtual ground Vgnd1, which controls the

[13] To be clear, we are not requiring Petitioner to explain a bodily incorporation of Lee in Kim; rather, our focus is on Petitioner's lack of explanation as to how the teachings would have been combined.

conductivity of sleep transistors NM1–NMn. *Id.* at 75 (citing Ex. 1005 ¶¶ 60–61, 65).

Again, Petitioner cites to the Declaration of Dr. Harris, which provides examples of how a combined system of Lee and Kim would have been designed. Pet. 76–79; Ex. 1002 ¶ 145 (presenting Fig. C). Similar to Petitioner's analysis of claims 4 and 7 discussed above, neither Petitioner nor Dr. Harris explains adequately how the teaching of the BIAS signal of Lee would have worked in the proposed combination of Figure C. Nor does Petitioner explain adequately how the BIAS signal of Lee would have been applied to the circuit of Kim to arrive at the subject matter recited in claim 5. Thus, for the same reasons discussed above with respect to claims 4 and 7, Petitioner does not explain adequately why a person of ordinary skill in the art would have been motivated to combine Kim and Lee in the manner proposed by Petitioner to arrive at the subject matter of claim 5.[14]

Accordingly, based on the complete record, we determine Petitioner does not demonstrate by a preponderance of the evidence that the subject matter of claim 5 would have been obvious over the proposed combination of Kim and Lee.

IV. CONCLUSION

For the foregoing reasons, we conclude that Petitioner has met its burden of proof, by a preponderance of the evidence, in showing that

[14] We do not require Petitioner to explain a bodily incorporation of Lee in Kim; rather, our focus is on Petitioner's lack of explanation as to how the teachings would have been combined.

claims 1 and 2 of the '026 patent are unpatentable.[15] For the reasons discussed above, Petitioner has not demonstrated, by a preponderance of the evidence, claims 4, 5, and 7 of the '026 patent are unpatentable. The chart below summarizes our conclusions.

Claims	35 U.S.C. §	References/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 4, 5, 7	103(a)	Kim, Lee	1, 2	4, 5, 7
Overall Outcome			1, 2	4, 5, 7

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1 and 2 of the '026 patent are determined to be unpatentable;

FURTHER ORDERED that claims 4, 5, and 7 of the '026 patent are not determined to be unpatentable; and

[15] Should Patent Owner wish to pursue amendment of claims 1 and 2 in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, the trial commencing on the entry date of this Decision.

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