UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

_____

Case IPR2019-01198
Patent 7,247,552

_____

PATENT OWNER VLSI TECHNOLOGY LLC'S NOTICE OF APPEAL

via PTAB E2E
Patent Trial and Appeal Board

via Priority Mail Express
Director
Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

via CM/ECF
United States Court of Appeals for the Federal Circuit

Pursuant to 35 U.S.C. §§ 141(c), 142, and 319, 37 C.F.R. §§ 90.2(a) and 90.3(a), Rule 4(a) of the Federal Rules of Appellate Procedure, and 28 U.S.C. § 1295(a)(4)(A), Patent Owner VLSI Technology LLC hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision (Paper 49, Attachment A) entered February 3, 2021 by the Patent Trial and Appeal Board. In particular, Patent Owner identifies the following issues on appeal:

(i) The Board's judgment that claims 1 and 2 of the '552 Patent are unpatentable;

(ii) The Board's claim constructions;

(iii) Any Board finding, determination, judgment, or order supporting or related to the Final Written Decision and decided adversely to Patent Owner; and

(iv) Whether the *inter partes* review determinations in this case by a panel of members of the Board complies with constitutional requirements, including, *inter alia*, the Due Process Clause and Appointments Clause.

Patent Owner is concurrently filing true and correct copies of this Notice of Appeal, along with the required fees, with the United States Court of Appeals for the Federal Circuit, and with the Patent Trial and Appeal Board.

Respectfully submitted,

/Nathan Lowenstein/

Nathan Lowenstein (*pro hac vice*)
Bridget A. Smith, Reg. No. 63,574
Kenneth J. Weatherwax, Reg. No. 54,528
LOWENSTEIN & WEATHERWAX LLP
Counsel for Patent Owner

Date: April 5, 2021

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the following document was served by electronic service, by agreement between the parties, on the date signed below:

PATENT OWNER VLSI TECHNOLOGY LLC'S NOTICE OF APPEAL

The names and address of the parties being served are as follows:

John V. Hobgood	John.Hobgood@wilmerhale.com
Donald R. Steinberg	Don.Steinberg@wilmerhale.com
S. Calvin Walden	Calvin.Walden@wilmerhale.com

Respectfully submitted,

/Jason Linger/

Date: April 5, 2021

CERTIFICATE OF FILING WITH USPTO

The undersigned hereby certifies that, pursuant to 37 C.F.R. § 90.2(a), two copies of the following document were filed by Priority Mail Express or equivalent service with the Director of the United States Patent and Trademark Office via the Office of the General Counsel, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, Virginia 22313-1450, on the date signed below:

PATENT OWNER VLSI TECHNOLOGY LLC'S
NOTICE OF APPEAL

Respectfully submitted,

/Jason Linger/

Date: April 5, 2021

CERTIFICATE OF FILING WITH COURT OF APPEALS

The undersigned hereby certifies that, pursuant to 37 C.F.R. § 90.2, Fed. R. App. Proc. 15(a)(1), Fed. Cir. R. 15(a)(1) & 52, and Manual of Patent Examining Procedure 1216.01, the following document was electronically filed in Portable Document Format (PDF) with the United States Court of Appeals for the Federal Circuit, via electronic CM/ECF, and a paper copy was sent to the Clerk of the Federal Circuit at the U.S. Court of Appeals for the Federal Circuit, 717 Madison Place, N.W., Washington, DC 20439, accompanied by the requisite fee paid on pay.gov, on the date signed below:

PATENT OWNER VLSI TECHNOLOGY LLC'S
NOTICE OF APPEAL

Respectfully submitted,

/Jason Linger/

Date: April 5, 2021

Attachment A

Trials@uspto.gov
571-272-7822

Paper 49
Entered: February 3, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2019-01198
IPR2019-01199
IPR2019-01200[1]
Patent 7,247,552 B2

Before THU A. DANG, LYNNE E. PETTIGREW, and KIMBERLY McGRAW, *Administrative Patent Judges.*

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

[1] We issue one Decision to be filed in each case. The parties are not authorized to use a multi-case caption.

I. INTRODUCTION

Petitioner, Intel Corporation, filed a Petition for *inter partes* review of claims 1 and 2 of U.S. Patent No. 7,247,552 B2 (Ex. 1001[2], "the '552 patent"; Ex. 1009 ("Certificate of Correction"). IPR2019-01198, Paper 3 ("Pet.-1198"). One the same day, Petitioner also filed Petitions for *inter partes* review of claim 11 (IPR2019-01200, Paper 3 ("Pet.-1200")) and of claim 20 (IPR2019-01199, Paper 3 ("Pet.-1199")) of the '552 patent.

In each proceeding, Patent Owner, VLSI Technology LLC, filed a Preliminary Response. IPR2019-01198, Paper 10 ("Prelim. Resp.-1198"); IPR2019-01199, Paper 10 ("Prelim. Resp.-1199"); IPR2019-01200, Paper 10 ("Prelim. Resp.-1200"), to which Petitioner then filed an Reply (IPR2019-01198, Paper 31[3]; IPR2019-01199, Paper 31; IPR2019-01200, Paper 31), and then Patent Owner filed an authorized sur-reply (IPR2019-01198, Paper 16; IPR2019-01199, Paper 16; IPR2019-01200, Paper 16).

In each proceeding, we instituted trial on all asserted grounds of unpatentability. IPR2019-01198, Paper 19 ("Inst. Dec.-1198"); IPR2019-01199, Paper 19 (Inst. Dec.-1199"); IPR2019-01200, Paper 19 (Inst.

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[2] US Patent No. 7,247,552 B2 (the "'552 patent") was filed in IPR2019-01198 as Exhibit 1001, in IPR2019-01199 as Exhibit 1101, and in IPR2019-01200 as Exhibit 1201. For convenience, this decision will refer to the '552 patent as Ex. 1001.

[3] Paper 31 in each proceeding is the Amended Petitioner's Reply to Patent Owner's Preliminary Response, which was filed to correct certain typographical errors that were present in the originally filed replies (IPR2019-01198, Paper 15; IPR2019-01199, Paper 15; IPR2019-01200, Paper 15). IPR2019-01198, Paper 28 (Order Granting Petitioner's Request to file Corrected Reply); IPR2019-01199, Paper 28; IPR2019-01200, Paper 28.

Dec.-1200"). In each proceeding, Patent Owner requested rehearing (IPR2019-01198, Paper 21; IPR2019-01199, Paper 21; IPR2019-01200, Paper 21) and Precedential Opinion Panel ("POP") review (IPR2019-01198, Paper 23; IPR2019-01199, Paper 23; IPR2019-01200, Paper 23) of our decisions to institute. Patent Owner's requests were denied. IPR2019-01198, Paper 25 (Order Denying POP Review); IPR2019-01199, Paper 25; IPR2019-01200, Paper 25; IPR2019-01198, Paper 35 (Decision Denying Requests for Rehearing); IPR2019-01199, Paper 35; IPR2019-01200, Paper 35.

Following institution, in each proceeding, Patent Owner filed a Response (IPR2019-01198, Paper 32, ("PO Resp.-1198"); IPR2019-01199, Paper 32 ("PO Resp.-1199"); IPR2019-01200, Paper 32 ("PO Resp.-1200")); Petitioner filed a Reply (IPR2019-01198, Paper 37 ("Pet. Reply-1198"), IPR2019-01199, Paper 37, ("Pet. Reply-1199"); IPR2019-01200, Paper 37 ("Pet. Reply-1200")), and Patent Owner filed a Sur-reply (IPR2019-01198, Paper 38 ("PO Sur-reply-1198"), IPR2019-01199, Paper 38 ("Sur-reply-1199"); IPR2019-01200, Paper 38 ("PO Sur-reply-1200")). A consolidated oral hearing was held on November 2, 2020 for the three proceedings, a transcript ("Tr.") of which appears in the record of each proceeding. IPR2019-01198, Paper 48; IPR2019-01199, Paper 48; IPR2019-01200, Paper 48.

A. Real Parties-in-Interest

In each proceeding, Petitioner identifies Intel Corporation as the real party-in-interest for Petitioner and Patent Owner identifies VLSI Technology LLC and CF VLSI Holdings LLC as the real parties-in-interest for Patent Owner. *See, e.g.*, Pet.-1198, 1; IPR2019-01198, Paper 9 (Patent

Owner's Second Updated Mandatory Notices), 1. *See* 37 C.F.R. 42.8(b)(1) (2019).

B. Related Matters

The parties indicate that the '552 patent is at issue in *VLSI Technology LLC v. Intel Corp.*, Case No. 18-966 (D. Del.). *See, e.g.*, Pet.-1198, 1–2; Prelim. Resp.-1198, 9.

C. The '552 Patent

The '552 patent, titled "Integrated Circuit Having Structural Support for a Flip-Chip Interconnect Pad and Method Therefor," issued from an application filed on January 11, 2005. Ex. 1001, codes (22), (54). The '552 patent states the invention is directed to a technique for alleviating the problems of defects caused by stress applied to bond pads by "adding dummy metal lines (74, 76) to interconnect layers (18, 22, 26) to increase the metal density of the interconnect layers." *Id.* at code (57); *see also id.* at 2:31–35 (stating "herein [is] provided a method and apparatus for providing structural support for interconnect pad locations in an integrated circuit (IC) by using novel layout techniques in the metallization and dielectric stack underlying the pad"). Examples of an interconnect pad include "a wire bond pad, a probe pad, a flip-chip bump pad . . . or test pad structures that may require underlying structural support." *Id.* at 2:41–45. The interconnect pad region, located physically underneath the interconnect pad, defines the region in which the layout techniques provided herein may be applied. *Id.* at 4:45–48.

Figure 1, reproduced below, illustrates a cross-section of a portion of an exemplary integrated circuit having a bond pad structure underlying a conductive bump. *Id.* at 2:8–13.

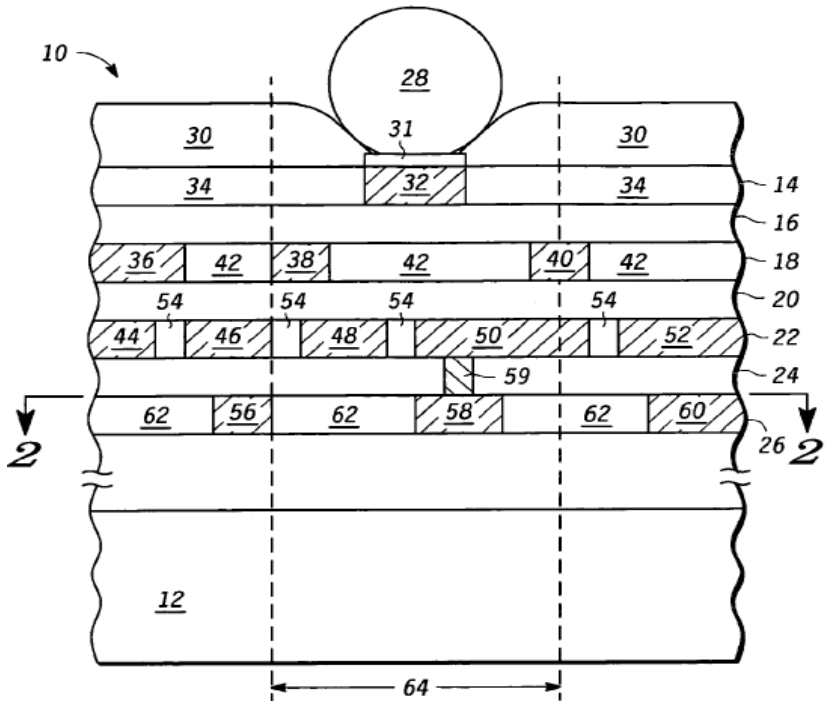


Figure 1 above illustrates an interconnect structure of integrated circuit 10 having conductive bump 28, metal cap 31, conductive bond pad 32, insulating layer 30, metal interconnect layers 14, 18, 22, 26, interlevel dielectric layers 16, 20, 24, and substrate 12. *See id.* at 2:63–64, 3:1–14. Force region 64 spans the interconnect pad region directly underlying conductive bump 28 and extending laterally a limited distance. *See id.* at 3:44–47. Force region 64 is a region within integrated circuit 10 in which forces are exerted on the interconnect structure when a die attach is performed to conductive bump 28. *Id.* at 3:49–53.

The ’552 patent explains that in order to adequately support overlying conductive bump 28, a predetermined minimum amount of metal, or a minimum metal density, must exist within each conductive layer of metal. *Id.* at 3:64–67. To increase the metal density of interconnect layer 26, a plurality of dummy lines (e.g., 75, 77) are added to the surface area of the interconnect layer 26 to reach a minimum metal density. *See id.* at 4:37–43. Figure 3 below, illustrates the top plan view of the conductive layer of the

bond pad structure of Figure 1 after increasing the metal density of the conductive layer by adding dummy metal lines. *See id.* at 2:14–19, 4:37–43.

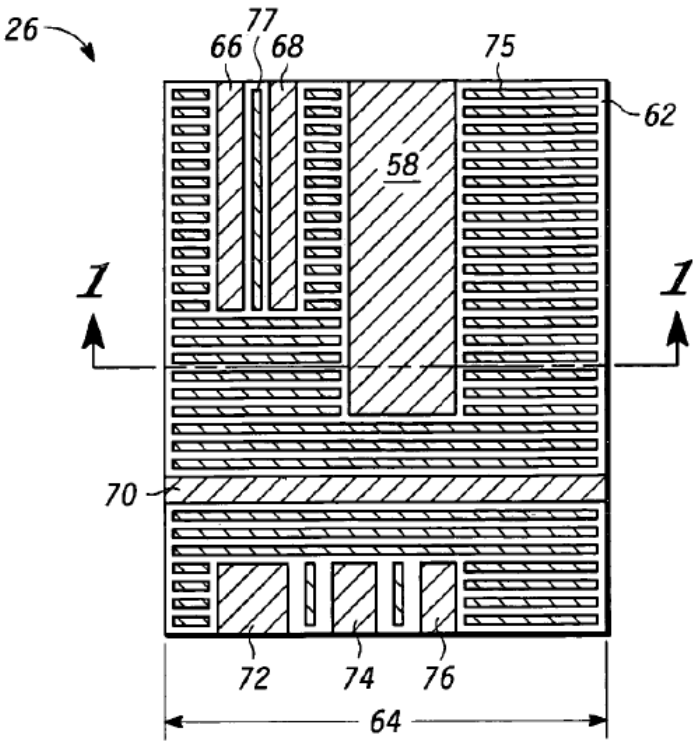


FIG. 3

Figure 3 above is a top plan view of the conductive layer of Figure 2 after increasing the metal density of the conductive layer by adding a plurality of dummy metal lines 75 and 77. *See id.* at 2:17–19, 4:37–43.

D. Challenged Claims

As noted above, Petitioner challenges claims 1, 2, 11, and 20 in these proceedings. Claims 1, 11, and 20 are independent. Independent claims 1, 11, and 20 are reproduced below with formatting and bracketing added for clarity.

1. [a] An integrated circuit comprising:

[b] a substrate having active circuitry;

[c] a bond pad over the substrate;

[d] a force region at least under the bond pad characterized by being susceptible to defects due to stress applied to the bond pad;

[e] a stack of interconnect layers, wherein each interconnect layer has a portion in the force region; and

[f] a plurality of interlayer dielectrics separating the interconnect layers of the stack of interconnect layers and having at least one via for interconnecting two of the interconnect layers of the stack of interconnect layers;

[g.i.] wherein at least one interconnect layer of the stack of interconnect layers comprises a functional metal line underlying the bond pad

[g.ii] that is not electrically connected to the bond pad and is used for wiring or interconnect to the active circuitry,

[h.i] the at least one interconnect layer of the stack of interconnect layers further comprising dummy metal lines in the portion that is in the force region

[h.ii] to obtain a predetermined metal density in the portion that is in the force region.

Ex. 1001, 7:45–65; Ex. 1009 (Certificate of Correction), 2.

11. [a] A method of making an integrated circuit having a plurality of bond pads, comprising:

[b] developing a circuit design of the integrated circuit;

[c] [ii] developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises [i] a plurality of interconnect layers underlying a first bond pad of the plurality of bond pads,

[d] at least one of the plurality of interconnect layers not being electrically connected to the first bond pad and used for wiring or interconnect other than directly to the first bond pad;

[e] [i] defining a force region at least under the first bond pad of the plurality of bond pads, [ii] wherein the force region comprises a first portion of each of the plurality of interconnect layers;

[f] identifying a first interconnect layer of the plurality of interconnect layers in which the first portion of the first interconnect layer has a metal density below a predetermined percentage;

[g] [iii] modifying the layout by [i] adding dummy metal lines to the first portion of the first interconnect layer [ii] to increase the metal density of the first portion of the first interconnect layer, and

[h] making the integrated circuit comprising the dummy metal lines.

Ex. 1001, 8:46–9:2.

20. [a] A method of making an integrated circuit having a plurality of bond pads, comprising:

[b] developing a circuit design of the integrated circuit;

[c] developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads,

[d] at least a portion of the plurality of metal containing interconnect layers underlying the first bond pad and not electrically connected to the first bond pad as a result of being used for electrical interconnection not directly connected to the bond pad;

[e] [ii] modifying the layout by [i] adding dummy metal lines to the plurality of metal-containing interconnect layers to achieve a metal density of at least forty percent for each of the plurality of metal-containing interconnect layers; and

[f] forming the integrated circuit comprising the dummy metal lines.

Ex. 1001, 10:1–21.

E. Prior Art and Asserted Grounds

In IPR2019-01198, Petitioner asserts that claims 1 and 2 are unpatentable under 35 U.S.C. § 103(a) on the following challenges (Pet.-1198, 3–4):

Claim(s) Challenged	35 U.S.C.	References/Basis[4]
1, 2	§ 103(a)[5]	Oda,[6] Cwynar[7]
2	§ 103(a)	Oda, Cwynar, AAPA[8]
1, 2	§ 103(a)	Oda, Owada[9]

In IPR2019-01200 Petitioner asserts that claim 11 is unpatentable under 35 U.S.C. § 103(a) on the following challenges (Pet.-1200, 4–5):

Claim Challenged	35 U.S.C.	References/Basis
11	§ 103(a)	Oda, Cwynar, Reddy[10]
11	§ 103(a)	Oda, Owada, Vuong[11]

[4] Certain references that were cited in different proceedings were assigned different exhibit numbers. For clarity and convenience, this Decision will refer to the cited art references using a single exhibit number as indicated in the associated tables.
[5] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the '552 patent has an effective filing date before September 16, 2012, the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of § 103.
[6] US Pub. No. 2004/0150112 A1, published August 5, 2004 (IPR2019-01198, Ex. 1003; IPR2019-1200, Ex. 1203 (hereinafter "Ex. 1003" or "Oda")).
[7] US Pub. No. 2002/0162082 A1, published Oct. 31, 2002 (IPR2019-1198, Ex. 1004; IPR2019-1200, Ex. 1204 (hereinafter "Ex. 1004" or "Cwynar")).
[8] Petitioner asserts the material at Exhibit 1001, 1:25–28 constitutes Applicant Admitted Prior Art ("AAPA"). *See, e.g.*, Pet.-1198, 57.
[9] US 5,027,188, issued June 25, 1991 (IPR2019-1198, Ex. 1005; IPR2019-01200, Ex. 1206 (hereinafter "Ex. 1005" or "Owada")).
[10] Digital Design Flow Options, Sagar V. Reddy, M.S. Thesis, 2001

In IPR2019-01199, Petitioner asserts that claim 20 is unpatentable under 35 U.S.C. § 103(a) on the following challenges (Pet.-1199, 5):

Claim Challenged	35 U.S.C.	References/Basis
20	§ 103(a)	Kanaoka,[12] Weling,[13] Reddy
20	§ 103(a)	Kanoaka, Weling, Vuong

F. Testimonial Evidence

In each proceeding, Petitioner relies on a declaration by John C. Bravman, Ph.D. (IPR2019-01198, Ex. 1002 (hereinafter "Ex. 1002"); IPR2019-01199, Ex. 1102 (hereinafter "Ex. 1102"); IPR2019-01200, Ex. 1202 (hereinafter "Ex. 1202"). Patent Owner cross-examined Dr. Bravman via deposition. *See* Ex. 2025[14].

In each proceeding, Patent Owner relies on a declaration by Dean Neikirk, Ph.D. (Ex. 2024[15]). Petitioner cross-examined Dr. Neikirk via deposition; the same transcript was filed in each proceeding. *See* IPR2019-01198, Ex. 1024 ("Ex. 1024"); IPR2019-01199, Ex. 1129 ("Ex. 1129"); IPR2019-01220, Ex. 1229 ("Ex. 1229").

(IPR2019-01199, Ex. 1104; IPR2019-01200, Ex. 1205, (hereinafter "Ex. 1205" or "Reddy")).

[11] US Patent Application Publication 2004/0098674 A1, filed Nov. 19, 2002, and published May 20, 2004 (IPR2019-01199, Ex. 1106; IPR2019-01200, Ex. 1207, (hereinafter "Ex. 1207" or "Vuong")).

[12] US 7,102,223 B1, filed August 5, 2003, issued Sept. 5, 2006 (IPR2019-01199, Ex. 1103 (hereinafter "Ex. 1103" or "Kanaoka")).

[13] US 5,639,697, issued June 17, 1997 (IPR2019-01199, Ex. 1105, "Weling").

[14] The same deposition transcript of Dr. Bravman was filed in each proceeding as Ex. 2025.

[15] The same declaration of Dr. Neikirk was submitted in each proceeding as Ex. 2024.

II. DISCUSSION

A. Legal Principles

To prevail on its challenge to Patent Owner's claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). The petitioner "has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC. v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable for obviousness under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co*., 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham,* 383 U.S. at 17. Petitioner contends a person of ordinary skill in the art, at the time the '552 patent was filed, would have had at least a Bachelor of Science or equivalent degree in electrical engineering or materials science (or equivalent experience), and two years of graduate work, work experience, or the equivalent in integrated circuit processing, manufacturing and structures. *See, e.g.*, Pet.-1198, 27 (citing Ex. 1002 ¶ 69).

In our Institution Decisions, we adopted Petitioner's definition of a person of ordinary skill in the art at the time of the claimed invention, except that we deleted the qualifier "at least" to eliminate vagueness as to the appropriate level of education. *See, e.g.*, Inst. Dec.-1198, 14. The qualifier expands the range without an upper bound, i.e., encompassing a Ph.D. degree and beyond, and thus does not meaningfully indicate the level of ordinary skill in the art. *Id.*

Neither party disputes our definition of the level of ordinary skill in the art. We see no reason to change our definition based on the complete record and, thus, maintain our definition for the purposes of this Decision.

C. Claim Construction

For petitions filed on or after November 13, 2018, a claim shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b)

(2018). Petitioner filed its Petitions after November 13, 2018. *See e.g.*, IPR2019-01198, Paper 6 (Notice of Accorded Filing Date), 1. Thus, we apply the claim construction standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

1. "force region"

The term "force region" is recited in independent claims 1 and 11. *See, e.g.*, Ex. 1001, 7:48–52, 7:61–65, 8:56–59. Petitioner asserts, *inter alia*, the term "force region" should be construed as defined in the '552 patent as "a region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed." *See, e.g.*, Pet.-1198, 24–25 (emphasis omitted) (citing Ex. 1001, 3:49–52); Pet.-1200, 36–37 (emphasis omitted) (citing Ex. 1001, 3:49–52; Ex. 1202 ¶ 80). Petitioner states that this construction of "force region" is met by the cited art (i.e., Oda) when a force "is exerted on the interconnect structure directly under the bond pad" "when the integrated circuit is bonded to external connections." Pet.-1198, 30 (citing, *inter alia*, Ex. 1002 ¶ 74); Pet.-1200, 50 (citing, *inter alia*, Ex. 1202 ¶ 111). Petitioner additionally states the cited art also teaches a "force region" under the construction proposed by Patent Owner during the District Court proceeding, namely, "an area in which a defect may occur due to a contact made to the bond pad." Pet.-1198, 35; Pet.-1200, 35–36.

Petitioner asserts that both its proposed construction of the term "force region" and the construction proposed by Patent Owner during the District Court proceeding include "*at least* regions *directly under* the bond pad." Pet.-1198, 27 (emphasis added); Pet.-1200, 37 (emphasis added); *see also, e.g.*, Pet.-1198, 30 (stating its construction of "force region" is met when a force "is exerted on the interconnect structure directly under the bond pad"

"when the integrated circuit is bonded to external connections" and citing, *inter alia*, Ex. 1002 ¶ 74); Pet.-1200, 50 (citing, *inter alia*, Ex. 1202 ¶ 111).

In its Preliminary Responses, Patent Owner did not propose a construction for "force region." *See generally* Prelim. Resp.-1198; Prelim. Resp.-1200. In our Institution Decisions, we did not provide an express construction for this term but stated that the "force region" includes at least the area directly under the bond pad. *See, e.g.*, Inst. Dec.-1198, 23–24; Inst. Dec.-1200, 28–29.

In its Responses, Patent Owner again does not proffer a construction for the term "force region" but instead contends that Petitioner has not shown that the cited art teaches a "force region" under Petitioner's own construction as "a region within the integrated circuit in which forces are exerted on the interconnect structure *when a die attach is performed*." *See, e.g.*, PO Resp.-1198, 51; PO Resp.-1200, 50; *see also* Ex. 1024, 24:14–25:11 (Dr. Neikirk stating that he has not formed an opinion on the construction of the term "force region" as used in the '552 patent but has applied the construction provided by Dr. Bravman).

Based upon a consideration of the full record, we see no reason to modify our construction of the term "force region" as including at least the area directly under the bond pad. A construction of "force region" that includes regions at least under the bond pad is consistent with the plain language of claims. For example, claim 1 requires the integrated circuit to comprise "a force region *at least under the bond pad* characterized by being susceptible to defects due to stress applied to the bond pad." Ex. 1001, 7:48–50 (emphasis added). Similarly, claim 11 recites "defining a force region at least under the first bond pad of the plurality of bond pads." Ex. 1001, 8:56–57.

This construction is also consistent with the Specification, which repeatedly describes "force region" as including regions directly under the bond pad. For example, the '552 patent states that a "force region is identified around *and under* the bond pad characterized by being susceptible to defects due to contacts to the bond pad." *Id.* at 5:55–57 (emphasis added). When describing the method of making an integrated circuit according to the invention, the '552 patent states that a "force region is defined around *and under a first bond pad* of the plurality of bond pads." *Id.* at 6:39–41 (emphasis added); *see also id.* at 6:13–14 ("A force region *under* and around *the bond pad* is defined." (emphasis added)). The Abstract of the '552 patent refers to "force area (64) around and *under each bond pad*" as defining "an area in which a defect may occur due to a contact made to that bond pad." *Id.* at code (57).

We note that the '552 patent description of "force region" as "the region within the integrated circuit 10 in which forces are exerted on the interconnect structure when a die attach is performed" applies to "force region 64" of Figures 1 and 2. Ex. 1001, 3:49–52. Figures 1 and 2, however, depict an exemplary embodiment of the invention. *See* Ex. 1001, 2:8–10 (stating the "present invention is illustrated by way of example and not by limitation in the accompanying figures"); *see also SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (stating "a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment"). We do not see, nor does either party point to, any language in the Specification that expresses an intention to limit the construction of "force region" recited in claims 1 and 11 to the description of force region 64 depicted in Figures 1 and 2, particularly when the '552 patent also describes "force region" as "a

region in which the interconnect layers of the stack of interconnect layers are susceptible to stress from the bond pad *due to assembly or other processes.*" Ex. 1001, 6:25–29; *see also id.* at 2:42–47 (stating that examples of an interconnect pad include, *inter alia*, a "wire bond pad" "a flip-chip bump pad," or "other packaging or test pad structures that may require underlying structural support" and that the "interconnect pad region, located physically underneath the interconnect pad, defines the region in which the layout techniques provided herein may be applied"); *see also* Ex. 1024, 39:11–40:5 (Dr. Neikirk stating that the '552 patent has teachings that would be relevant to wire bonding).

We further note that, even in the exemplary embodiment of Figures 1 and 2, force region 64 also includes the region directly under the bond pad. *See* Ex. 1001, 3:44–47 (stating "force region 64 is illustrated spanning the interconnect pad region *directly underlying the conductive bump 28 and extending laterally a limited distance*" (emphasis added)).

Thus, for the foregoing reasons, we maintain our construction of "force region" as including the region directly beneath the bond pad. No further construction of this term is required to resolve issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that only terms that are in controversy need to be construed, and "only to the extent necessary to resolve the controversy"); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

2. "adding dummy metal lines to the plurality of metal-containing interconnect layers"

Claim 20 recites, *inter alia*, a "layout comprises a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads," and "modifying the layout by adding dummy metal lines to the plurality of metal-containing interconnect layers to achieve a metal density of at least forty percent for each of the plurality of metal-containing interconnect layers." Ex. 1001, 10:1–21.

Petitioner did not provide an express construction for these phrases in its Petition. *See*, *e.g.*, Pet.-1199, 30. In its Preliminary Response, Patent Owner argued claim 20 requires the dummy metal lines be added not just anywhere, but specifically to the portions of the plurality of metal-containing interconnect layers lying directly under the first bond pad. *See* Prelim. Resp.-1199, 28–40; *see also* IPR2019-01199, Paper 16 at 6–10. Specifically, Patent Owner contends because the antecedent basis for the "metal-containing interconnect layers" of claim element 20[e.i] is "a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads" as recited in claim element 20[c], the phrase "adding dummy metal lines to the plurality of metal-containing interconnect layers" requires the dummy metal lines to be added to the portion of the metal-containing interconnect layers that extend under the first bond pad. *See* Prelim. Resp.-1199, 29; *see also id.* at 31 (asserting Petitioner failed to demonstrate dummy lines were added "specifically, to the 'plurality of metal-containing interconnect layers' under PD16"); IPR2019-01199, Paper 16 at 6–10 (stating Petitioner fails to show where Kanaoka teaches "adding any dummy metal lines specifically to the same M1 and M2 [metal

lines] under [bond first pad] PD16, regardless of how far [the lines] extend" (emphasis altered)).

In our Institution Decision, we determined the ordinary and customary meaning of claim 20, as understood by one of ordinary skill in the art, does not require adding dummy metal lines to the region of the metal-containing interconnect layers directly under the first bond pad. IPR1199-Inst. Dec. 14–16. Patent Owner does not challenge this claim construction. Based upon the full record, we see no reason to change our construction.

3. "being used for electrical interconnection not directly connected to the bond pad"

Claim 20 recites, *inter alia, "*at least a portion of the plurality of metal-containing interconnect layers underlying the first bond pad and *not electrically connected to the first bond pad* *as a result of being used for electrical interconnection not directly connected to the bond pad*.*"* Ex. 1001, 10:8–13 (emphases added). Neither party proposed an express construction for this phrase prior to institution.

After institution, Patent Owner asserts the term "used for electrical interconnection" recited in the phrase above does not mean the property of being electrically conductive, but rather "requires actual use for electrical interconnection, that is, connection to active device." PO Resp.-1199, 12 (capitalization altered); *see also id.* at 5 (stating a POSITA "would have understood the recited 'electrical interconnection' to refer to connection to active devices"); *id.* at 37 (stating "ordinary artisans would have understood claim 20's recitation of 'being used for electrical interconnection' to refer to 'being used for connection to active devices'"); *id.* at 14 (stating "not only do the claims require actual use for electrical interconnection, ordinary artisans more specifically would have understood that language to refer to

use for connection to active elements" and citing Ex. 2024 ¶¶ 79, 94–95); *id.* at 15–16 (stating testimony "from both experts support this view that electrical interconnection, in the context of claim 20, refers to connection to active devices" and citing Ex. 1102 ¶¶ 26, 31; Ex. 2024 ¶¶ 78–79); *id.* at 17 (stating a POSITA "would have understood that 'being used for electrical interconnection' requires evidence of actual use for electrical interconnection and, more specifically, connection to active circuitry"). Patent Owner also states that because "the '552 patent uses the term 'interconnection' *only* to describe connection to semiconductor circuitry in the integrated circuit," the '552 patent teaches that the portion of the interconnect layers 'used for electrical interconnection' must provide connection to devices." *Id.* at 15 (citing Ex. 1001, 2:38–42).

Petitioner replies, *inter alia*, that claim 20 does not require connection to active circuitry. Pet. Reply-1199, 3–16. Petitioner argues that during prosecution, claim 20 was amended to address what the metal layers *could not* be attached to (i.e., the bond pad) as opposed to limiting what the layers *must* be connected to. *Id.* at 10; *see also id.* at 5–16 (arguing that unlike claims 1 and 6, claim 20 was not amended during prosecution to recite active circuitry and thus claim 20 should not be construed to require active circuitry and citing, *inter alia*, Ex. 1113, 3–7).

In its Sur-reply, Patent Owner states that its Response did not propose a construction that requires electrical interconnection to active circuity. *See* PO Sur-reply-1199, 4 (stating that although the PO Response "provides context for the term 'electrical connection' and mentions the phrase 'active circuitry' three times, there is no construction in [Patent Owner's Response], as the Reply contends, that 'requires electrical interconnection to active circuitry'"). Patent Owner asserts that it argued that "*used for* electrical

interconnection" requires that "the structures that meet this limitation must actually carry electricity" otherwise there can be no electrical *use*. *Id.* at 5 (citing PO Resp.-1199, 12–14) (emphasis added); *see also id.* at 3 (stating the claim plainly requires "use for" and it requires that the interconnection be electrical"). Patent Owner further states that "interconnects in a semiconductor device . . . serve to connect transistors on the semiconductor chip—whether those transistors are called active circuitry, active devices, transistors, the integrated circuit, or some other term—either to each other or to the outside world." *Id.* at 3 (citing PO Resp.-1198, 14–17; Ex. 1102 ¶¶ 26, 36; Ex. 2024 ¶ 79).

Based upon a consideration of the full record, we do not construe the phrase "used for electrical interconnection not directly connected to the bond pad" to require connection to active circuitry or that the structures that meet this limitation must actually carry electricity. Claim 20 does not recite "active circuitry" and we decline to import this limitation into claim 20. We also do not construe the phrase "used for electrical interconnection" to require the actual carrying of electricity as argued by Patent Owner. Patent Owner does not dispute that two metal layers of an integrated circuit are "electrically connected to each other" if the two layers are connected by a metal via, even if those two metal layers are not connected to any structure other than each other and even if those two layers do not carry electricity. *See generally* PO Resp.-1199; PO Sur-reply-1198; *see also* Ex. 1129, 154:20–155:3 (Dr. Neikirk admitting that Kanaoka's metal layers M1 and M2 (i.e., two structures that do not carry electricity) are "electrically connected to each other" because an "electrically conducted" via connects the two structures).

Rather, we understand the language of claim element 20[d] that requires the integrated circuit layout to comprise metal interconnect layers wherein a "portion of the metal containing interconnect layers [are] not electrically connected to the first bond pad as a result of being used for electrical interconnection not directly connected to the bond pad" to encompass interconnect layers that are "used for electrical interconnection not directly connected to the bond" by virtue of being electrically connected to each other but not electrically connected to the bond pad.

This construction is supported by the specification and prosecution history of the '552 patent. Although the specification does not use the phrase "used for electrical interconnection" or even the term "electrical interconnection," the specification does describe metal layers (e.g., interconnects) that are electrically connected to each other by virtue of being connected through conductive vias. For example, the '552 patent describes prior systems as comprising "metal layers under the bonding pad that are connected together and to the bonding pad by large arrays of vias distributed across a majority of the bond pad area." Ex. 1001, 1:53–58. The '552 patent states that this" via arrangement requires that the majority of portions of the underlying metal layers and the bonding pad are all *electrically connected* together and are thus not functionally independent of each other." *Id*. at 1:58–61. The '552 patent further states that as a result of this arrangement, the underlying "metal layers may not be used for wiring or interconnects unrelated to the bond pad." *Id.* at 1:61–64. As such, we understand the '552 patent to explain that because the underlying metal layers of prior systems *are electrically connected* together and *to the bond pad* by virtue of the vias, these layers may not be used for wiring or interconnects unrelated to the bond pad.

During prosecution, claim 20 was amended to require explicitly "at least a portion of the plurality of metal containing interconnect layers underlying the first bond pad and not electrically connected to the first bond pad as a result of being used for electrical interconnection not directly connected to the bond pad." Ex. 1007, 6–7. The applicant argued that the asserted prior art "is representative of the prior art described at [column 1, lines 53–64 of the '552 patent]." *Id.* at 8 (citing page 2, lines 4–11 of the specification as filed, which corresponds to the disclosure at Ex. 1001, 1:53–64). The applicant stated that the support structure of the asserted prior art has "underlying metal layers *that are connected together and to the bond pad by large arrays of vias* distributed across the bond pad area." *Id.* at 8 (emphasis added). The applicant further stated that all of the metal layers and arrays of vias are *electrically connected together* and are not functionally independent. *Id.* at 8, 10. Thus, we understand applicant to have distinguished the asserted art by addressing what the "portion" of the metal interconnect layers could *not* be attached to (i.e., the bond pad), rather than limiting what the "portion" *must be* connected to.

Thus, we construe the language of claim element 20[d] that recites:

> at least a portion of the plurality of metal containing interconnect layers underlying the first bond pad and not electrically connected to the first bond pad as a result of being used for electrical interconnection not directly connected to the bond pad

to encompass interconnect layers that are "used for electrical interconnection not directly connected to the bond pad" by virtue of being electrically connected to each other but not electrically connected to the bond pad.

No further construction of this term, or any other term of the '552 patent, is required to resolve any disputed issues.

D. Asserted Unpatentability of Claims 1 and 2 over Oda and Cwynar and of Claim 2 over Oda, Cwynar, and AAPA

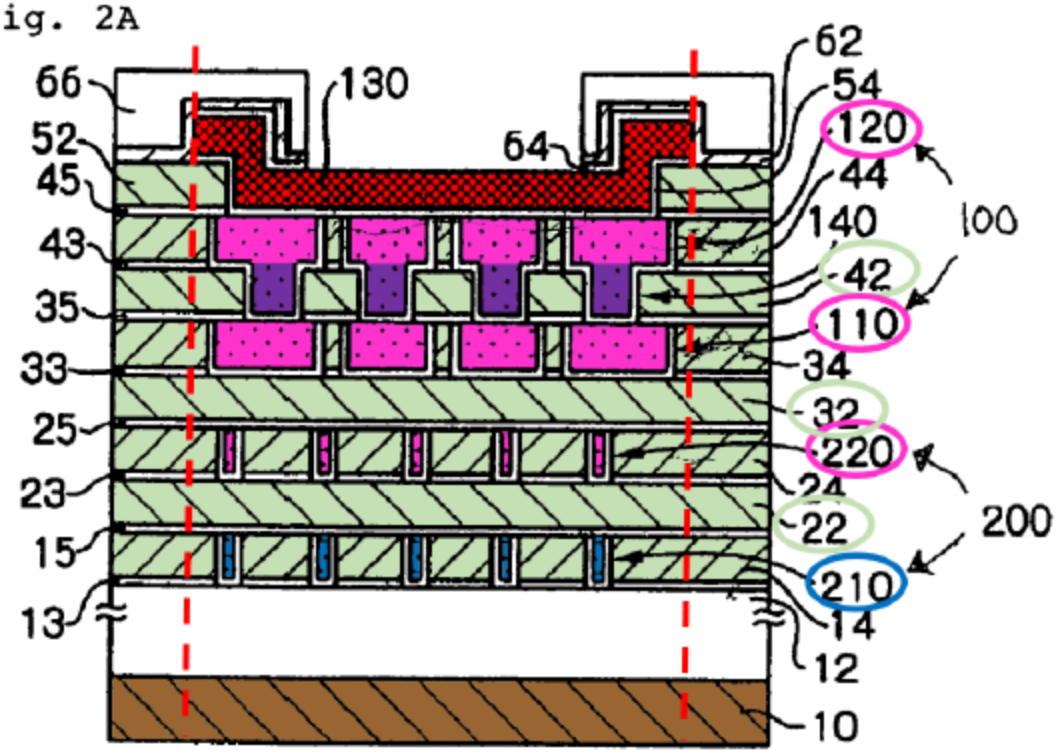
Petitioner contends that claims 1 and 2 would have been obvious under 35 U.S.C. § 103(a) over Oda in view of Cwynar. *See* Pet.-1198, 28–55; Pet. Reply-1198, 1–33. Patent Owner opposes. *See* PO Resp.-1198, 5–24, 35–64; PO Sur-reply-1198, 1–25. For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 1 and 2 are unpatentable over Oda and Cwynar.

1. Overview of Oda (Ex. 1003)

Oda, titled "Semiconductor Device and Method of Fabrication Same," is directed to a semiconductor device having improved shock resistance to the bonding pads during probing and bonding and to a method of fabricating such a device. Ex. 1003, at code (54), ¶ 9. Oda states that the load (i.e., pressure) of a needle during probing or bonding depresses the bonding pads and may cause cracks in the interlevel dielectric film underlying the bonding pad. *See id.* ¶ 8. The upper and lower copper layers below the bonding pads function as shock-resistant layers that impede the transmission of shocks below the bonding pads. *Id.* ¶ 23.

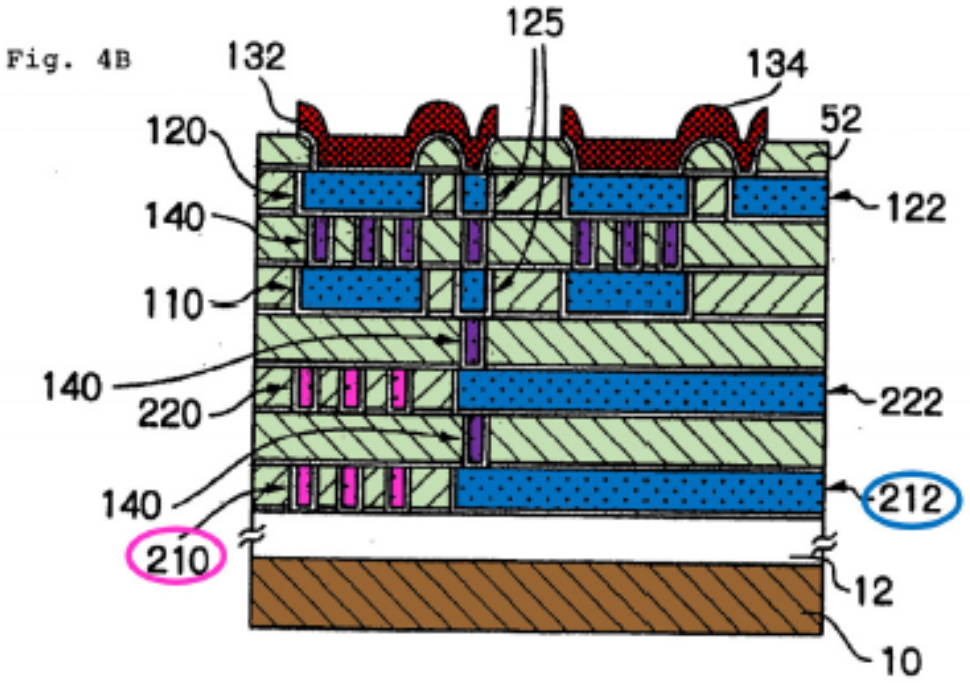
Figure 2A, reproduced below, with colored annotations provided by Petitioner (Pet.-1198, 15), illustrates a sectional view of a region of a semiconductor device of a first working example having upper copper layer 100 and lower copper layer 200 underlying bond pad 130 (red) for improved shock resistance. *See* Ex. 1003 ¶¶ 38, 48, 50, 52.

Fig. 2A



Annotated Figure 2A above depicts a semiconductor device having upper copper layer 100 (composed of first and second upper copper layers 110, 120), lower copper layer 200 (composed of first and second lower copper layers 210, 220), bonding pad 130, and substrate 10. *See id.* ¶¶ 48–49. Circuit interconnects for connecting interconnecting semiconductor elements are formed from conductive layers, such as the copper layers formed on the same layer as either of copper layer 100 and lower copper layer 200. *Id.* ¶ 54. Connections between bonding pad 130 and internal circuits are realized by way of, for example, upper copper layer 100. *Id.* The '552 patent explains that upper and lower copper layer 200 may have "dummy patterns" rather than interconnects for distributing the shock applied to bonding pad 130. *See id.* ¶ 55.

Figure 4B, reproduced below, with colored annotations provided by Petitioner (Pet.-1198, 16), is a sectional view of another working example. *See id.* ¶¶ 42–43.



Annotated Figure 4B, above, depicts outer bonding pad 132 (dark brown), first copper interconnects 212 (blue) for circuit interconnects formed on the same level as first lower copper layer 210 (pink), and second copper interconnects 222 (blue) for circuit interconnects are formed on the same level as first lower copper layer 220 (pink). *Id.* ¶ 89. First and second upper copper layers (110, 120) and first and second lower copper layers (210, 220) are formed as shock resistance layers below outer pads 132. *Id.* ¶ 90.

2. Overview of Cwynar (Ex. 1004)

Cwynar is a U.S. Patent Application Publication titled "Method for Making an Interconnect Layer and a Semiconductor Device Including the Same." Ex. 1004, codes (12), (54). Cwynar is directed to a method for making a layout for an interconnect layer of a semiconductor device to

facilitate uniformity of planarization during manufacture of the semiconductor device. *Id.* at code (57). The method includes "determining an active interconnect feature density" and "adding dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacture of the semiconductor device." *Id.*

Figure 4 of Cwynar, with colored annotations provided by Petitioner, depicts a partial top plan view of an interconnect layer divided into layout regions. *Id.* ¶ 23.

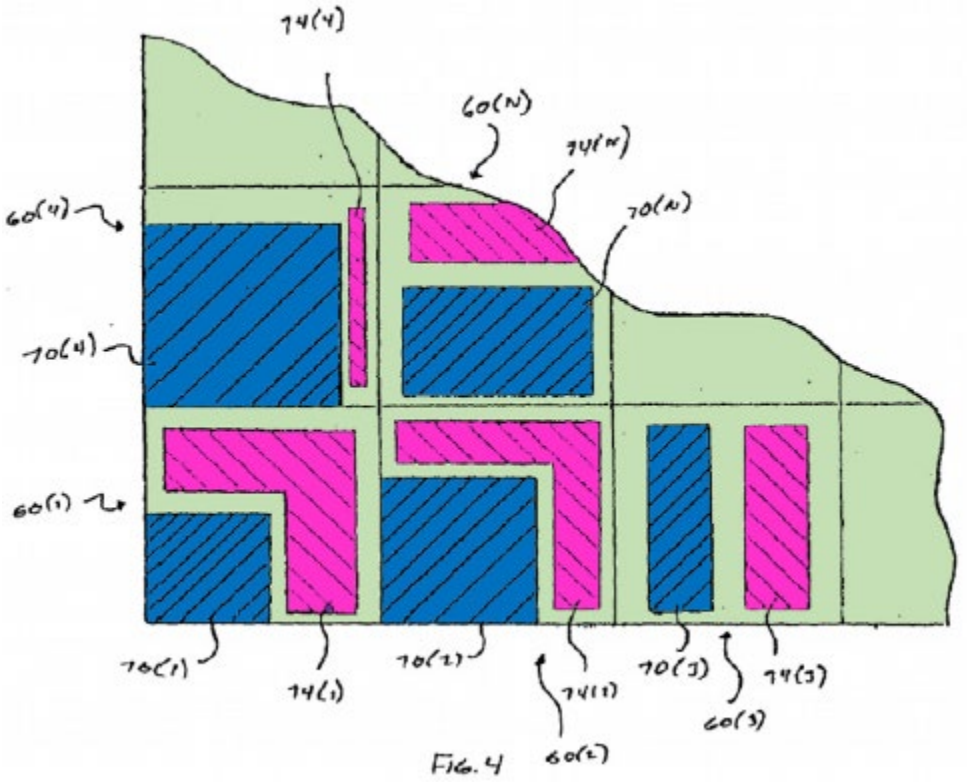


Figure 4 above illustrates layout regions 60(a)–60(n), active interconnect features 70(1)–70(n) in blue, and dummy fill features 74(1)–74(n) in pink. *See id.* ¶¶ 26–27, 29. Dummy fill features 74(1)–74(n) are added "to obtain a desired density of active interconnect features and

dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device." *Id.* ¶ 29.

3. Analysis of Claim 1

a) Preamble and Claim Elements 1[b], [c], and [f]

Petitioner asserts that Oda teaches the subject matter recited in the preamble and in claim elements [b], [c], and [f]. *See* Pet.–1198, 28–29, 33–35. We have reviewed and agree with Petitioner's contentions. For example, we agree with Petitioner that Oda teaches an "integrated circuit" comprising a "substrate having active circuitry" (e.g., a semiconductor having transistors, resistors, capacitors interconnected through metal interconnects), and "a bond pad over the substrate" (bond pad 130 over substrate 10) as recited in the preamble and claim elements 1[b] and [c]. *See id.* at 28–29 (citing Ex. 1003 ¶¶ 54, 65; Ex. 1002 ¶¶ 71–72). We also agree with Petitioner that Oda's disclosure of dielectric films (e.g., dielectric films 22, 32, and 42), interconnect layers (e.g., lower copper interconnect layers 210, 220), and vias (e.g., via 140 in dielectric film 42) teaches the "plurality of interlayer dielectrics separating the interconnect layers of the stack of interconnect layers and having at least one via for interconnecting two of the interconnect layers of the stack of interconnect layers" as recited in claim element 1[f]. *See id.* at 33–35 (citing Ex. 1003 ¶¶ 14, 16, 49–52, 62, Fig. 2A; Ex. 1002 ¶ 79).

Patent Owner does not dispute Petitioner's assertions, and therefore, any such arguments are waived. *See generally* PO Resp.-1198; *see also* IPR2019-01198, Paper 20 (Scheduling Order), 7 (stating that any arguments for patentability not raised in the response may be deemed waived).

We therefore determine that Petitioner has sufficiently shown that Oda teaches the subject matter recited in the preamble[16] and claim elements 1[b], [c], and [f].

b) Element 1[d]

Claim element 1[d] recites "a force region at least under the bond pad characterized by being susceptible to defects due stress applied to the bond pad." Ex. 1001, 7:48–50. Petitioner contends Oda teaches this claim element under both Petitioner's proposed construction of "force region" as well as under the construction proposed by Patent Owner in the concurrent district court proceeding as both proposed constructions of "force region" include the region directly below the bond pad. *See* Pet.-1198, 29–31 (citing Ex. 1002 ¶¶ 74–75; Ex. 1003 ¶¶ 8, 35, 76, Fig. 2A).

Petitioner asserts, *inter alia*, Oda teaches the limitations of claim element 1[d] under Petitioner's proposed construction of "force region" (i.e., "a region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed") because Oda teaches that when the integrated circuit is bonded to external connections, force is exerted "on the interconnect structure directly under the bond pad." *See id.* at 30. For example, Petitioner asserts that Oda teaches that the load of a needle during "bonding depresses the bonding pads and may cause cracks in the interlevel dielectric film that underlies the bonding pads." *Id.* (emphasis omitted) (quoting Ex. 1003 ¶ 8); *see also id.* (quoting Ex. 1003 ¶¶ 35, 76; citing Ex. 1003, Fig. 2A; Ex. 1002 ¶ 74). Petitioner also asserts that Oda teaches a "force region" under Patent Owner's proposed district court

[16] Because we determine that the asserted art teaches the subject of the preamble, we do not reach the issue of whether the preamble is limiting.

construction (i.e., an area in which a defect may occur due to a contact made to the bond pad) by teaching that cracks may occur in the interconnect layers directly below the bond pad and cause "defective connections" when contact is made with the bond pads. *Id.* at 30–31 (citing Ex. 1002 ¶ 75; Ex. 1003 ¶¶ 8, 35, 76).

Petitioner also asserts that because the term "force region" "includes *at least* regions *directly under* the bond pad," it is not necessary to determine the outer boundaries of the claim term. *See id.* at 27.

Patent Owner does not dispute that Oda discloses a region under the bond pad that is susceptible to defects due stress applied to the bond pad. *See* generally PO Resp.-1198. Rather, Patent Owner contends that because Petitioner has not shown that a die attach is performed in Oda, Petitioner failed to apply its own construction of force region (i.e., a region within the integrated circuit in which forces are exerted on the interconnect structure when a *die attach i*s performed) and therefore has not shown that Oda teaches a "force region." *See, e.g.*, *id.* at 51–64. Patent Owner contends that Oda's forces are exerted during a "wire bonding" process, which is different from a "die attach," (*id.* at 58–64) and that Petitioner never explains how the forces described in Oda "are exerted 'when a die attach is performed'" (*id.* at 52).

We have reviewed Petitioner's arguments and evidence and agree with Petitioner that Oda teaches "a force region at least under the bond pad characterized by being susceptible to defects due to stress applied to the bond pad" as recited in claim element 1[d]. *See* Pet.-1198, 66–70, 73; Pet. Reply-1198, 17–23. As stated above in Section II.C.1, we determine that the "force region" includes regions directly under the bond pad. Petitioner has provided persuasive argument and evidence, and Patent

Owner does not dispute, that Oda discloses a region directly under the bond pad and that this region is "susceptible to defects due to stress applied to the bond pad." *See* Pet.-1198, 25, 29–31 (citing Ex. 1002 ¶¶ 74–75; Ex. 1003 ¶¶ 8, 35, 76, Fig. 2A). For example, we agree with Petitioner's contention, supported by the declaration testimony of Dr. Bravman, that Oda teaches "a force region *at least under the bond pad* characterized by being susceptible to defects due to stress applied to the bond pad" by disclosing that, *inter alia*, the load of a needle during wire bonding depresses bonding pads and may cause cracks in the interlevel dielectric film that underlies the bonding pads. *Id.* at 30 (emphasis added); *see also* Ex. 1024, 27:16–2 (stating that a person of skill in the art in the 2005 time frame wound understand that forces are exerted under bond pads during the wire-bonding process); Ex. 1003 ¶¶ 8, 35, 76.

We disagree with Patent Owner's argument that Petitioner fails to show Oda teaches a force region because Petitioner fails to show that forces are exerted on Oda's interconnect structure when a die attach is performed. *See* PO Resp.-1198, 52. As explained above, Petitioner alleges, and sufficiently shows, that Oda teaches the subject matter of claim element 1[d] because Oda teaches a force region directly under the bond pad by disclosing that the region under the bond pad is susceptible to defects (i.e., cracks) as a result of the load of a needle during wire bonding. Moreover, the '552 patent also describes "force region" as "a region in which the interconnect layers of the stack of interconnect layers are susceptible to stress from the bond pad *due to assembly or other processes.*" Ex. 1001, 6:25–29 (emphasis added). Based on the record presented, we see no reason to exclude Oda's wire bonding from the "assembly or other processes" described in the '552 patent.

For the foregoing reasons, we determine Petitioner has sufficiently shown that Oda teaches or suggests the limitations recited in claim element 1[d].

c) Element 1[e]

Petitioner asserts Oda teaches "a stack of interconnect layers, wherein each interconnect layer has a portion in the force region" as recited in claim element 1[e]. Pet.-1198, 31–33 (citing Ex. 1002 ¶¶ 76–77; Ex. 1003 ¶¶ 14, 16, 23, 45, 49, 50, 52, Fig. 2A). For example, Petitioner asserts Oda's upper copper layer 100 (which includes interconnect layers 110 and 120) and lower copper layer 200 (which includes interconnect layers 210 and 220) are "a stack of interconnect layers." *Id.* at 31–32 (citing Ex. 1003 ¶¶ 14, 16, 49–50, 52). Petitioner also asserts that each of these layers has a portion in the "force region" directly below the bond pad. *See id.* at 32 (citing Ex. 1003, Fig. 2A); *see also id.* at 32–33 (stating Oda teaches adding reinforcing structures to the copper interconnect layers under the bond pad to make the copper layers shock resistant layers) (citing Ex. 1003 ¶¶ 23, 45, 49, 50; Ex. 1002 ¶ 77).

Other than contending Oda does not teach a "force region," which we address above, Patent Owner does not dispute Petitioner's assertions. *See generally* PO Resp.-1198. We have reviewed, and agree with, Petitioner's argument and evidence and determine Petitioner has sufficiently shown that Oda teaches a stack of interconnect layers having a portion in the force region as required by claim element 1[e].

d) Element 1[g]

Claim element 1[g] recites "[i] wherein at least one interconnect layer of the stack of interconnect layers comprises a functional metal line underlying the bond pad [ii] that is not electrically connected to the bond pad

and is used for wiring or interconnect to the active circuitry." Ex. 1001, 7:57–61.

Petitioner asserts that either Oda or the combination of Oda and Cwynar teach this claim element. Pet.-1198, 36–43 (citing Ex. 1002 ¶¶ 81–92; Ex. 1003 ¶¶ 11, 21, 45, 49–50, 52, 54–55, 61, 62, 74, 76, 107, Figs. 2A–C; Ex. 1004 ¶¶ 8, 27, Fig. 4; Ex. 1010, 8:22–26, Figs. 3–6; Ex. 1011, 5:20–22). For example, Petitioner asserts Oda's first lower copper layer 210 of lower copper layer 200 is "at least one interconnect layer" of "the stack of interconnect layers" (copper layers 110, 120, 210, 220) underlying the bond pad. *Id.* at 36–37 (citing Ex. 1003 ¶¶ 50, 52, 54, 61, Fig. 2A; Ex. 1002 ¶ 82). Petitioner also asserts that Oda's lower copper layer 210 comprises a functional metal line underlying the bond pad. *Id.* at 36–37 (citing Ex. 1003 ¶¶ 54, 61). In particular, Petitioner points to Oda's teaching that lower copper layer 200, which is referred to as a "dummy layer[] for distributing the shock applied to bonding pad 130" (Ex. 1003 ¶ 55) may *also* be used "as active circuit interconnects rather than as a dummy metal pattern" (Ex. 1003 ¶ 61). *Id.* at 36 (emphasis omitted) (citing Ex. 1003 ¶¶ 54, 61). Petitioner contends that Oda explains that "such a configuration is preferable because '[u]sing lower copper layer 200 as a circuit interconnect layer in this way enables the effective utilization of the area below bonding pad 130.'" *Id.* at 36–37 (quoting Ex. 1003 ¶ 61). Petitioner also points to first lower copper layer 210 of Oda's Figure 2A as being used for circuit interconnects to interconnect active circuit elements found on substrate 10. *Id.* at 37 (citing Ex. 1003 ¶¶50, 52, 54, Fig. 2A).

Petitioner also asserts that Oda teaches a functional metal line that "is not electrically connected to the bond pad and is used for wiring or interconnect to the active circuitry" as required by claim element 1[g.ii]. *Id.*

at 41–43. Petitioner contends that Oda's disclosure that first lower copper layer 210 is insulated from upper copper layers 110 and 120 (and therefore from bond pad 130, which is electrically connected to upper copper layers 110 and 120) teaches that lower copper layer 210 "is not electrically connected to bond pad 130." *Id.* at 42–43 (citing Ex. 1003 ¶¶ 11, 45, 49, 54, 62, Fig. 2A; Ex. 1002 ¶¶ 89–91). Petitioner further contends that Oda's disclosure that lower copper layer 200 can be used as active circuit interconnects to interconnect active semiconductor elements to each other (rather than as a pure dummy metal pattern that only serves as a shock resistant layer) teaches that the functional metal line "is used for wiring or interconnect to the active circuitry." *Id.* at 43 (citing Ex. 1003 ¶¶ 54, 61; Ex. 1002 ¶ 92).

Petitioner also states that although Oda refers to "metal patterns" not to "metal lines," Oda also states that its metal patterns are not limited to shapes that are shown in the Figures and that "other patterns may be applied such that the area density of copper is approximately uniform." *Id.* at 37–38 (emphasis omitted) (quoting Ex. 1003 ¶ 107). Petitioner contends that a POSITA would have understood that Oda's disclosure of metal patterns teaches use of metal lines because, *inter alia*, a pattern of "metal lines" is one of the simplest metal patterns and is ubiquitous in integrated circuits. *Id.* at 38 (citing Ex. 1002 ¶ 83).

Petitioner also contends, *inter alia*, that a POSITA would have used metal lines, as disclosed in Cwynar, as one of Oda's metal patterns because simple metal lines would have been one of the best known and most obvious metal patterns to try to fabricate, metal lines that route signal and power have been widely used, and a POSITA would have had a reasonable

expectation of success in using them. *Id.* at 38–41 (citing Ex. 1004 ¶¶ 8, 27; Ex. 1010 (US 6,448,650 B1), 8:22–26, Figs. 3–6; Ex. 1002 ¶¶ 84–87).

Based upon the full record, we agree with Petitioner's contentions as described herein, which are supported by persuasive evidence including the expert testimony of Dr. Bravman, that Oda teaches a functional metal line underlying the bond pad that is not electrically connected to the bond pad and that is used for wiring or interconnect to the active circuitry as required by claim element 1[g]. *See* Pet.-1198, 41–43 (citing Ex. 1003 ¶¶ 11, 45, 49, 54, 61–62, Fig. 2A; Ex. 1002 ¶¶ 89–92); Pet. Reply-1198, 4–8. Patent Owner makes a number of arguments in response. We have considered each of these arguments and determine that they are not persuasive for the reasons stated below.

We are persuaded by Petitioner's argument that Oda teaches a functional metal line used for wiring or interconnect to the active circuitry by teaching that the dummy pattern of copper layer 200 may also be used as a pattern for circuit interconnects. *See, e.g.*, Pet.-1198, 53 (citing Ex. 1003 ¶¶ 54, 61; Ex. 1002 ¶ 92); Ex. 1003 ¶ 61 (stating "lower copper layer 200 . . . may . . . be used as a pattern for circuit interconnects"); Ex. 1003 ¶ 54 (stating "internal circuits including semiconductor elements such as transistors, resistors, and capacitors and the circuit interconnects for interconnecting these semiconductor elements are also provided on semiconductor substrate 10").

Patent Owner contends that Oda does not teach a *functional* metal line underlying the bond pad that is not electrically connected to the bond pad. *See* PO Resp.-1198, 6–24. Patent Owner contends that Oda's copper layer 210 is not a *functional* metal line because Oda expressly states that lower copper layer 200, which includes copper layer 210, is a "dummy layer" that

does not constitute the interconnects of internal circuits. *Id.* at 9 (citing Ex. 1003 ¶¶ 52, 55, 58). Patent Owner contends that Oda's statement in paragraph 61 that the *dummy pattern of copper layer 200* may be used as a *pattern for circuit interconnects* squarely contradicts Oda's statement in paragraph 55 that *dummy patterns are not used for interconnects*. *Id.* at 11 (citing Ex. 1003 ¶¶ 55, 61) (emphasis omitted). Relying on Dr. Neikirk's testimony, Patent Owner contends that these teachings are "self-contradictory" and that it "is not clear how to reconcile these two statements." *Id.* at 11–12 (quoting Ex. 2024 ¶ 37).

We disagree with Patent Owner that these teachings of Oda are self-contradictory and cannot be reconciled. *See* PO Resp.-1198, 3, 8–13. Rather, we understand Oda to state that a dummy metal pattern that provides structural support (e.g., by distributing "shocks that are exerted upon bonding pad 130") and that is *also* electrically insulated from other interconnect layers, may *also* be used as a "pattern for circuit interconnects. *See, e.g.*, Ex. 1003 ¶¶ 49–50, 52, 61. For example, Oda explains that upper copper layer 100 and lower layer 200 each serve a structural purpose of providing shock resistance as each have a "two-layer structure, whereby shocks that are exerted upon bonding pad 130 are distributed between each of the layers and an improve in shock resistance is obtained." *See* Ex. 1003 ¶ 50 (describing improved shock resistance provided by upper copper layer 100), *id.* ¶ 52 (stating the "use of a plurality of copper layers for lower copper layer 200 provides the same effects as in copper layer 100"); *see also id.* ¶ 55 (stating that the planar patterns of its copper layer 200 "function as dummy layers for distributing the shock applied to bonding pad 130"). However, Oda also states that when "the dummy pattern of lower copper layer 200 is electrically insulated from upper copper layer 100 . . . this

dummy pattern may therefore be used as pattern for circuit interconnects." *Id.* ¶ 61. Oda further explains that using "lower copper layer 200 as a circuit interconnect layer in this way enables the effective utilization of the area below bonding pad 130." *Id.* Thus, we understand paragraph 55 of Oda to state that the planar patterns of copper layer 200, which are called "dummy patterns" when "rather than constituting the interconnects of internal circuits, [they] function as dummy layers for distributing" shock applied to the bond pad. *Id.* ¶ 55. However, when the dummy pattern of lower copper layer 200 is electrically insulated from upper copper layer 100, Oda states this dummy pattern may *also* be used as a pattern for circuit interconnects. *Id.* ¶ 61.

Patent Owner also contends Oda does not teach a functional metal line that is "*not electrically connected*" to a bond pad. PO Resp.-1198, 8–9, 13-24. Patent Owner contends that Petitioner's argument is based on the false premise that a layer that is *electrically insulated* from another layer cannot also be *electrically connected* to that layer (*id.* at 16) and asserts that it is well known that layers that are electrically insulated from each can also be electrically connected to each other by way of, for example, vias. *Id.* at 18–19 (citing, *inter alia*, Ex. 2024 ¶¶ 43–45; Ex. 1003 ¶¶ 32–33). Thus, Patent Owner contends that Oda's teaching that lower copper layer 200 is electrically insulated from upper copper layer 100 does not, in itself, suggest that those elements could not also be electrically connected by vias. *Id.* at 19–24 (citing Ex. 1003 ¶¶ 14, 28, 49, 51, 54, 62, 63, 67). Patent Owner further asserts that a POSITA would have understood that dielectric layer 32 must have vias to allow signals to pass from bond pad 130 to circuits on the surface of substrate 10 and "[t]herefore, any electrical connection between

. . . substrate 10 and bond pad 130 must traverse lower copper layer 200." PO Resp.-1198, 23 (emphasis omitted).

We disagree with Patent Owner's argument and agree with Petitioner that Oda teaches that the functional metal line of copper layer 200 is not electrically connected to the bond pad. Patent Owner's argument that even if a layer is "electrically insulated" from another layer, the layers may still be electrically connected through vias, is not persuasive because it does not take into account the full scope of Oda's teachings or Petitioner's arguments. *See* PO Resp.-1198, 16–24. Petitioner persuasively explains that Oda does not just state that copper layer 200, which includes copper layer 210, is electrically insulated from the layers above it. Rather, Oda also states that it is *because of this electrical insulation* that the dummy pattern of copper layer 200 "may therefore be used as a pattern for circuit interconnects." Ex. 1003 ¶ 61. We are persuaded by Petitioner's argument and evidence that Oda's disclosure—that because copper layer 200 is electrically insulated from the upper layers *and* the dummy patterns of copper layer 200 may be used as a pattern for circuit interconnects and function independently to electrically connect to circuit elements on the substrate below—teaches that copper layer 200 is *not electrically connected to* upper copper layer 100 and bond pad above. Pet.-1198, 41–43; Pet. Reply-1198, 7–8; Ex. 1002 ¶¶ 89–92; Ex. 1003 ¶ 61.

Other than stating "Oda does not teach using metal lines anywhere, let alone dummy lines" and citing to Petitioner's statement that "Oda does not explicitly recite a metal line" (PO Resp.-1198, 36), Patent Owner does not present any particularized argument that Oda does not teach a "functional

metal line" as required by claim element 1[g].[17] Rather, Patent Owner's expert admits that "[l]ines are one of the most common forms of patterns" within interconnect circuits. Ex. 1024, 84:22–85:2.

Accordingly, based on the record presented, Petitioner has shown sufficiently that Oda teaches the limitations recited in claim element 1[g].

e) Element 1[h]

Claim element 1[h] recites "[i] the at least one interconnect layer of the stack of interconnect layers further comprising dummy metal lines in the portion that is in the force region [ii] to obtain a predetermined metal density in the portion that is in the force region." Ex. 1001, 7:61–65. Petitioner asserts Oda either alone or in combination with Cwynar teaches this claim element. *See* Pet.-1198, 43–56 (citing Ex. 1001, 3:44–49; Ex. 1002 ¶¶ 93–115; Ex. 1003 ¶¶ 15, 21, 54–55, 57, 59, 61, 65, 68, 70, 74, 89, 107, Figs. 2A, 4B; Ex. 1004 ¶¶ 8, 27, 29–31, Fig. 4; Ex. 1010, 8:22–29; Ex. 1011, 5:20–22).

Petitioner asserts that Oda alone teaches an integrated circuit having both the recited functional metal lines and dummy patterns (lines) on the same layer directly below the bond pad. *See* Pet.-1198, 44–46 (citing Ex. 1003 ¶¶ 54, 89, 105, Fig. 2A; Ex. 1002 ¶ 94). Petitioner cites to Oda's disclosure that although "not shown in FIG. 2A, . . . internal circuits . . . and circuit interconnects are formed from conductive layers such as copper layers that are formed on the same layer as . . . lower copper layer 200. *Id.* at 44 (quoting Ex. 1003 ¶ 54). Petitioner further asserts that Figure 4B of Oda also illustrates dummy metal patterns (e.g., first lower copper layer 210)

[17] Patent Owner's argument that Oda does not teach dummy metal lines is addressed in Section II.D.3.e.

and functional metal lines (e.g., first lower copper interconnects 212) on the same interconnect layer (copper layer 200) directly under bond pad 132. *See id*. at 44 (citing Ex. 1003 ¶¶ 54, 89, 107, Fig. 4B; Ex. 1002 ¶ 94). Petitioner also asserts Oda teaches that the internal circuits and circuit interconnects can be formed on the same layer as lower copper layer 200 of Figure 2A. *Id.* (citing Ex. 1003 ¶ 54, Fig. 2A).

Petitioner also asserts Oda teaches using different shaped dummy metal patterns, including under the bond pad, to obtain a predetermined metal density of from 15% to 95%. *See id.* at 52 (citing Ex. 1003 ¶¶ 15, 57, 59, 65, 68, 70; Ex. 1002 ¶ 105); *see also id.* at 46–47 (stating it may be desirable to increase metal density beyond 15% to improve shock resistance when the active interconnects themselves provide a metal density of 15% (citing Ex. 1003 ¶ 57; Ex. 1002 ¶ 102)).

Petitioner also asserts the combination of Oda and Cwynar also teaches an integrated circuit having both functional metal lines and dummy lines on the same layer directly below the bond pad. *Id.* at 45. Petitioner contends Cwynar also teaches dummy metal lines (i.e., dummy fill features 74(1)–74(n) region) next to active metal lines (i.e., active interconnect features 70(1)–70(4)). *Id.* at 47–48 (citing Ex. 1004 ¶¶ 27, 29, Fig. 4). Petitioner also asserts Cwynar's teaching to add more dummy lines to region 74(2) to achieve the predetermined target metal density of 50%. *See id.* at 52 (citing Ex. 1004 ¶ 30, Fig. 4; Ex. 1002 ¶ 106).

Patent Owner makes a number of arguments in response.

First, Patent Owner contends that Oda does not teach dummy metal *lines* because Oda merely teaches dummy *patterns,* not dummy metal *lines,* and that it would not have been obvious to replace Oda's patterns with dummy metal lines from Cwynar. PO Resp.-1198, 35–49.

We disagree with Patent Owner's argument and agree with Petitioner's argument and supporting evidence, including testimony of Dr. Bravman, that although Oda does not explicitly recite a dummy metal "line," a person of ordinary skill in the art would have understood Oda to teach the use of dummy metal lines because (1) Oda teaches its metal dummy patterns are not limited to shapes shown in the figures and "other patterns may be applied such that the area density of copper is approximately uniform" and (2) a POSITA would have understood that those patterns include patterns of lines (the simplest of patterns). Pet.-1198, 45, 49–50 (citing Ex. 1003 ¶ 107; Ex. 1002 ¶¶ 94, 96–97); *see also* Ex. 1002 ¶ 97 (Dr. Bravman testifying that Cwynar's synonymous use of "metal lines" and "patterns" further bolsters his opinion that a POSITA would have understood Oda to teach metal lines (citing Ex. 1004 ¶ 8)).

We are also persuaded by Petitioner's additional argument, supported by the testimony of Dr. Bravman, that a POSITA would have been motivated to use Cwynar's metal lines as one of Oda's metal patterns. We agree with Petitioner's contention that regions 70(1) through 70(N) of Cwynar's Figure 4 are active interconnect features that include "a plurality of metal lines" to increase the metal density of the surrounding region and, therefore, Cwynar explicitly teaches using metal lines to increase metal density. *See* Pet.-1198, 38–39 (emphasis omitted) (citing Ex. 1004 ¶ 27, Fig. 4); Ex. 1002 ¶ 84 (stating Cwynar teaches adding metal lines into an active interconnect layer to increase metal density and citing Ex. 1004 ¶¶ 8, 27, Fig. 4). We also agree with Petitioner's contention that it would have been obvious to a POSITA to use Cwynar's metal lines as one of Oda's metal patterns to increase the area density of copper because simple metal

lines are one of the best known and most obvious metal pattern to try and fabricate.

We disagree with Patent Owner's arguments that because Cwynar uses dummy metal lines to improve planarity, not improve shock resistance, it would not have been obvious to replace Oda's metal patterns with metal lines. PO Resp.-1198, 35–41. We are persuaded by Dr. Bravman's testimony that, *inter alia,* a POSITA would have been motivated to combine Cwynar's teaching of proving dummy metal lines as a method to increase metal density, with Oda's teaching that increasing metal density improves shock resistance, to obtain the expected result of more metal density where needed to provide the expected benefit of improved mechanical damage protection. Ex. 1002 ¶¶ 83–88, 100–104, 109–115.

We are not persuaded by Patent Owner's argument, based on Dr. Neikirk's testimony, that a POSITA would not have replaced Oda's metal patterns, specifically designed to maximize the shock resistance of bond pads, with dummy metal lines that provide inferior shock resistance. *See* PO Resp.-1198, 36; *see also id.* at 39–40 (stating two-dimensional dummy lines provide superior shock resistance than dummy metal lines because they strengthen the structure in more than one dimension) (citing Ex. 2024 ¶¶ 56–59). Quoting Dr. Neikirk's testimony, Patent Owner contends that "replacing a dummy pattern with dummy lines would likely reduce the 'shock resistance' of the dummy structure and frustrate the goals of Oda." *Id.* at 40 (emphasis omitted) (quoting Ex. 2024 ¶ 59). Dr. Neikirk's testimony that Oda's dummy metal patterns are superior to dummy metal lines, however, is based on his description of metal lines having a length "normally *much greater* than their other dimensions (width and thickness)" and of Oda's metal patterns as "area patterns, which are

more appropriately thought of as two-dimensional structures (with length and width of *comparable size*)." Ex. 2024 ¶ 56 (emphasis added); *see also id.* ¶ 58 (stating that a POSITA would not expect that a one-dimensional pattern "with lengths in one direction *much larger* than widths" "would necessarily provide similar protection" as two dimensional patterns "i.e., ones with similar cross sectional dimensions of width and length" (emphasis added)); Ex. 2024, 93:3–94:5 (discussing Ex. 2024 ¶ 56). Thus, Patent Owner's contention that metal lines are inferior to metal patterns is based on Dr. Neikirk's comparison of "one dimensional" lines with lengths in one direction *much larger* than widths" with two "dimensional patterns" having "similar cross sectional dimensions of width and length." Oda, however, does not limit its dummy patterns to structures that have length and width of comparable size. *See* Ex. 1003 ¶ 107 (stating the dummy patterns "are not limited to the shapes that are shown in FIG. 2B and FIG. 20, and other patterns may be applied such that the area density of copper is approximately uniform"). Nor does the '552 patent state that its lines must have a length *much* greater or *much* larger than their width. Indeed, Dr. Neikirk admits that the term line "usually refers to something that is longer than it is wide and thick." Ex. 1024, 49:15–19. As such, we are not persuaded by Dr. Neikirk's testimony that "replacing a dummy pattern with dummy lines would likely reduce the 'shock resistance' of the dummy structure and frustrate the goals of Oda." Ex. 2024 ¶ 59.

Patent Owner also asserts that Petitioner has not shown that Oda teaches both dummy metal lines and functional metal lines under the same bond pad. PO Resp.-1198, 41–45. Patent Owner contends Petitioner relies on two discrete embodiments of Oda (i.e., Figs 2A, 4B) without showing a reason to combine the embodiments with a reasonable likelihood of success.

Id. at 42. Patent Owner also contends that Petitioner inconsistently relies on Oda's layer 210 as being both the functional metal line recited in claim element 1[g] and as the dummy metal lines recited in claim element 1[h]. *Id.* at 42–45.

We disagree with Patent Owner because, contrary to Patent Owner's arguments, Oda teaches that lower layer 200, which includes layer 210, can include both dummy and active metals. Oda states that "[a]lthough not shown in FIG. 2A, . . . internal circuits . . . and circuit interconnects are formed from conductive layers such as copper layers that are formed on the same layer as … lower copper layer 200." Ex. 1003 ¶ 54. Thus, the Petition is not inconsistent when referring to portions of Oda's layer 210 as functional metal lines and dummy metal lines. Petitioner relies on Oda's express teaching that metal patterns in Oda's interconnect layer 210 can constitute either dummy patterns (dummy line) or circuit interconnects (active line) and that both dummy and active lines can co-exist on the same layer. *See* Pet.-1198, 41–47. Moreover, we agree that Oda ties these different embodiments together by teaching that dummy metal patterns and circuit interconnects can co-exist on the same interconnect layer, and by expressly stating that the working examples can be "modified as appropriate within the range that does not depart from the gist of the invention." Pet.-1198, 45 (citing Ex. 1002 ¶ 94; Ex. 1003 ¶ 105); Pet. Reply-1198 (citing Ex. 1002 ¶ 105).

Accordingly, based on the record presented, we determine, Petitioner has shown sufficiently that Oda or Oda and Cwynar teach the limitations recited in claim element 1[h] and has also made a sufficient showing of articulated reasoning with rational underpinning for combining the references.

f) Conclusion

For the foregoing reasons, we determine Petitioner has provided persuasive evidence and arguments presented to show by a preponderance of the evidence that claim 1 would have been obvious over Oda in view of Cwynar.

4. Analysis of Claim 2

Claim 2 requires the integrated circuit of claim 1 to further comprise "a conductive ball on the bond pad." Ex. 1001, 7:66–67. Petitioner contends Oda's teaching of a "ball" comprised of a conductive material (i.e., "gold or solder") that sits on the bond pad and is used for wire bonding teaches the limitations of claim 2. Pet.-1198, 56–57 (citing Ex. 1003 ¶¶ 2, 75, 104; Ex. 1002 ¶ 116). Petitioner further asserts that to the extent Oda's conductive material shaped like a ball does not expressly disclose a "conductive ball" as recited in claim 2, the '552 patent admits at column 1, lines 25 through 28 (AAPA) that it was known to attach a conductive ball on a bond pad. *Id.* at 57–59 (citing Ex. 1001, 1:25–28; Ex. 1002 ¶¶ 119–122; Ex. 1003 ¶¶ 3, 8; Ex. 1005, 1:57–61).

Patent Owner does not dispute these assertions by Petitioner. We have reviewed and agree with Petitioner's contentions and evidence that Oda teaches a conductive ball on the bond pad and, further, that AAPA provides evidence that it would have been known to a POSITA to attach a conductive ball on a bond pad. As such, Petitioner has shown by a preponderance of the evidence that claim 2 would have been obvious over the combined teachings of Oda and Cwynar and Oda, Cwynar, and AAPA.

E. Asserted Unpatentability of Claims 1 and 2 over Oda and Owada

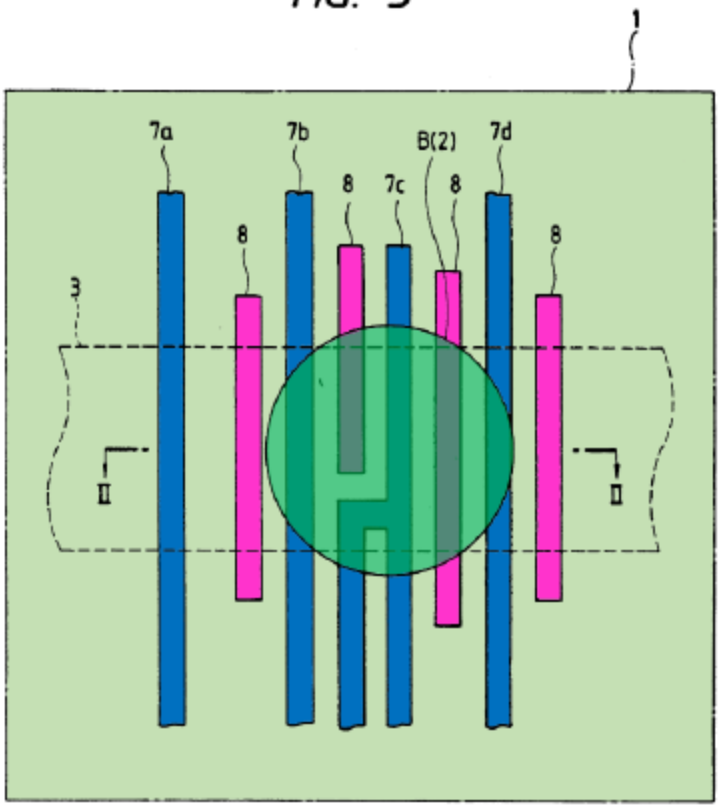
Petitioner contends claims 1 and 2 would have been obvious over Oda and Owada. *See* Pet.-1198, 59–85 (citing Ex. 1002 ¶¶ 123–177). Patent Owner opposes. *See* PO Resp.-1198. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1 and 2 would have been obvious over Oda and Owada.

1. Overview of Owada (Ex. 1005)

Owada is a U.S. Patent titled "Semiconductor Integrated Circuit Device in Which a Semiconductor Chip is Mounted with Solder Bumps for Mounting to a Wiring Substrate." Ex. 1005, code (54). Owada explains that one problem of semiconductor integrated circuits having a multi-layered wiring structure is that differences between regions of high and low wiring density on the same wiring layer can cause the layer underlying the bond pad to not be flat, thereby decreasing the reliability of solder bump connections. *See id.* at 1:34–43, 2:49–3:35, Fig. 10. Owada states adding dummy patterns to the regions below solder bump 2 can increase wire density, resulting in a flat electrode pad and increased connection reliability. *See id.* at 3:59–4:2; *see also id.* at 8:8–14 (stating that by adding dummy metal lines in the same region as the third layer Al wirings 7a–e below solder bumps 2, the wiring density (inclusive of the dummy patterns) becomes higher in this region thereby improving connection reliability of solder bump 2).

Figure 3 of Owada, with color annotations provided by Petitioner, is a plan view of principal portions of a semiconductor chip. Ex. 1005, 4:9–13; Pet.-1198, 69, 72.

FIG. 3



Annotated Figure 3, reproduced above, depicts the layout of metal wirings, including "third layer [aluminum] Al wirings 7a–7d" and "dummy patterns 8" below solder bump 2. Ex. 1005, 5:11–26.

2. Analysis of Claim 1

Petitioner asserts, and we agree, that Oda teaches all of the limitations of claim 1 for the same reasons stated above in Section II.D.3. *See* Pet.-1198, 59–62, 66, 68, 73, 75, 80.

Petitioner further contends, *inter alia*, that to the extent Oda's metal patterns do not expressly teach metal *lines* as required by claim elements 1[g] and [h], Owada teaches metal lines. *See, e.g.*, *id.* at 69–70 (stating Owada describes third layer Al wirings 7a–d as "having substantially the same line width" and citing Ex. 1005, 5:5–46; Ex. 1002 ¶ 149); *id.* at 72 (stating Owada uses the term "patterns" to refer to metal lines within third

layer Al wirings 7a–7d and that Owada's dummy patterns 8 are made of the same material and have substantially the same line width as the third layer Al wirings 7a–7d and citing Ex. 1005, 5:22–27, Fig. 3); *see also id.* at 80 (stating that to the extent Oda's metal 'patterns' do not include metal 'lines,' Owada discloses metal lines).[18] Petitioner contends that Owada uses the term "patterns" to refer to metal lines within third layer Al wirings 7a–7d, thus confirming that a POSITA would have viewed a metal lines as one of the Oda's metal patterns. *Id.* at 72–73 (citing Ex. 1002 ¶ 152); 78–79 (citing Ex. 1002 ¶ 164). Petitioner further contends that it would have been obvious to try Owada's metal lines as a shape of Oda's dummy patterns because simple metal lines would have been one of the best known and most obvious metal patterns to try to fabricate and a POSITA would have had a reasonable expectation of success in using them. *See, e.g.*, *id.* at 71 (citing Ex. 1010, Figs. 3–6).

Petitioner contends that it would have been obvious to combine the teachings of Oda and Owada because, *inter alia*, both references control metal density by adding dummy metal patterns/lines to achieve uniform planarity during manufacture. *See id*. at 80–82 (citing Ex. 1003 ¶¶ 55, 57, 59, 74; Ex. 1005, 3:59–63; Ex. 1002 ¶¶ 171–173). Petitioner also asserts a POSITA would have recognized that adding dummy metals in the manner taught by Owada would increase metal density and therefore improve shock resistance. *See id.* at 81 (citing Ex. 1003 ¶¶ 55, 74; Ex. 1002 ¶ 172). Petitioner also asserts that Oda and Owada teach the well-known technique of adding dummy metal lines next to active metal interconnects and that

[18] Because we find that Oda's metal patterns satisfy the limitations of claim elements 1[g] and [h], we do not reach Petitioner's alternative argument that Owada teaches these limitations. *See* Section II.E.3.d.

combining the teachings would lead to the expected result of more metal density where needed to provide the expected benefit of improved mechanical damage protection. *Id.* at 79 (citing Ex. 1002 ¶ 165; Ex. 1003 ¶ 57).

Patent Owner argues that Oda does not teach dummy metal lines as recited in claim elements 1[g] and [h] because Oda teaches dummy metal *patterns* not metal *lines*. For the same reasons set forth above in Section II.D.3., we disagree with Patent Owner's argument and agree with Petitioner's argument that a POSITA would have understood Oda to teach the use of dummy metal lines.

Patent Owner also argues that it would not have been obvious to replace Oda's patterns with the metal lines of Owada for the same or similar reasons it would not have been obvious to replace Oda's patterns with the metal lines of Cwynar. *See, e.g.,* PO Resp.-1198, 35–41, 45–49; *see also id.* at 26–31 (asserting that Owada and Oda are "wholly incompatible references" that "use dummy metals for different reasons").

Based on a complete review of the record, we are persuaded by Petitioner's additional argument that a POSITA would have been motivated to use Owada's metal lines as one of Oda's patterns. Petitioner persuasively argues that Oda teaches adding dummy metal patterns to increase metal density, that Owada teaches adding dummy metal patterns that are dummy metal lines to increase metal density, and that a POSITA would have looked to the teachings of both Oda and Owada because both teach controlling the amount of metal density by adding dummy metal patterns/lines during manufacture. *See* Pet.-1198, 80. We also agree with Petitioner's argument that Owada uses the term "patterns" to refer to metal lines, thus confirming

that a POSITA would have viewed a metal line as one of Oda's metal patterns. *Id.* at 72–80 (citing Ex. 1005, 5:22–27, Fig. 3; Ex. 1002 ¶ 152).

Patent Owner's contention that a POSITA would not have used Owada's "dummy lines" in place of Oda's dummy patterns because doing so would have thwarted Oda's goals of providing improved shock resistance because metal lines are inferior to metal patterns is not persuasive for the same reasons set forth in Section II.D.3.e. We also disagree with Patent Owner's argument that Owada and Oda are "wholly incompatible references" that "use dummy metals for different reasons." PO Resp.-1198, 3–4, 26, 35–4 (capitalization altered). Petitioner has persuasively shown that both Oda and Owada teach methods of adding dummy features to increase metal density.

Accordingly, based on the record presented, we determine, Petitioner has shown sufficiently that Oda or Oda and Owada teach the limitations recited in claim element 1[h] and has also made a sufficient showing of articulated reasoning with rational underpinning for combining the references.

a) Conclusion

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over Oda in view of Owada.

3. Analysis of Claim 2

Petitioner asserts that to the extent Oda's conductive material shaped like a ball does not disclose the "conductive ball" recited in claim 2, it would have been obvious given Owada's teaching a conductive ball (solder bump 2) on a bond pad (electrode pad 6). Pet.-1198, 83–85 (citing Ex. 1002 ¶¶ 175–177; Ex. 1004, 4:65–68, Fig. 4).

Patent Owner does not dispute Petitioner's contentions. We have reviewed Petitioner's argument and evidence and determine Petitioner has shown by a preponderance of evidence that claim 2 would have been obvious over Oda and Owada.

F. Asserted Unpatentability of Claim 11 over Oda, Cwynar and Reddy

Petitioner contends that claim 11 would have been obvious under 35 U.S.C. § 103(a) over Oda in view of Cwynar and Reddy. Patent Owner opposes. For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claim 11 is unpatentable over Oda, Cwynar, and Reddy.

1. Prior Art Status of Reddy (Ex. 1205)

Under 35 U.S.C. § 311(b), a petitioner in an *inter partes* review may only challenge the claims of a patent based on "prior art consisting of patents or printed publications." Whether a reference qualifies as a printed publication under § 102 is a legal conclusion based on underlying fact findings." *Acceleration Bay, LLC v. Activision Blizzard Inc*., 908 F.3d 765, 772 (Fed. Cir. 2018). A reference is considered publicly accessible if it was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, can locate it. *Id*.

Petitioner asserts Reddy is a master's degree thesis, submitted to the Graduate School of The Ohio State University, that qualifies as a prior art printed publication under pre-AIA § 102(b) because Reddy was publicly accessible as of April 15, 2002, which is more than one year before January 11, 2005, the priority date for the '552 patent. *See* Pet.-1200, 4; Ex. 1211 ¶¶ 21–29; Ex. 1001, code (22). In support of this argument,

Petitioner provides, *inter alia*, (1) a Machine-Readable Cataloging ("MARC") bibliographic record for Reddy from the Ohio State University Library (Ex. 1218, Attachment A) purported to show the Reddy thesis is cataloged at The Ohio State University Library, is held by that institution, and is also available on-line from the CiteSeer website (Ex. 1211 ¶ 23); (2) a MARC bibliographic record for Reddy from OCLC9 (Ex. 1211, Attachment B) purported to show the MARC record for Reddy was created by The Ohio State University Library on April 15, 2002 (Ex. 1211 ¶ 24); (3) a dissertation (Ex. 1208, Attachments C, D (English translation), the "Melo Dissertation") purportedly produced in 2004, which cites to Reddy (Ex. 1211 ¶ 26); and (4) a MARC record for the Melo Dissertation purported to show the dissertation was available to the public as of September 30, 2004 (Ex. 1211 ¶ 27).

Patent Owner does not challenge the prior art status of Reddy. Based on our review of the complete current record, and as described above, we determine Petitioner has provided sufficient evidence and argument to show Reddy qualifies as a prior art printed publication.

2. Overview of Reddy (Ex. 1205)

Reddy, titled "Digital Design Flow Options," is a thesis that discusses aspects of integrated circuit chip design (e.g., "VLSI (Very Large Scale Integration) IC design flow") and how the design can be completed using various computer aided design tools (CAD). *See* Ex. 1205, i–iv.

Figure 1.1 of Reddy, modified by Petitioner to improve text resolution, is reproduced below. *See* Pet.-1200, 13–14; Ex. 1205, 1–2.

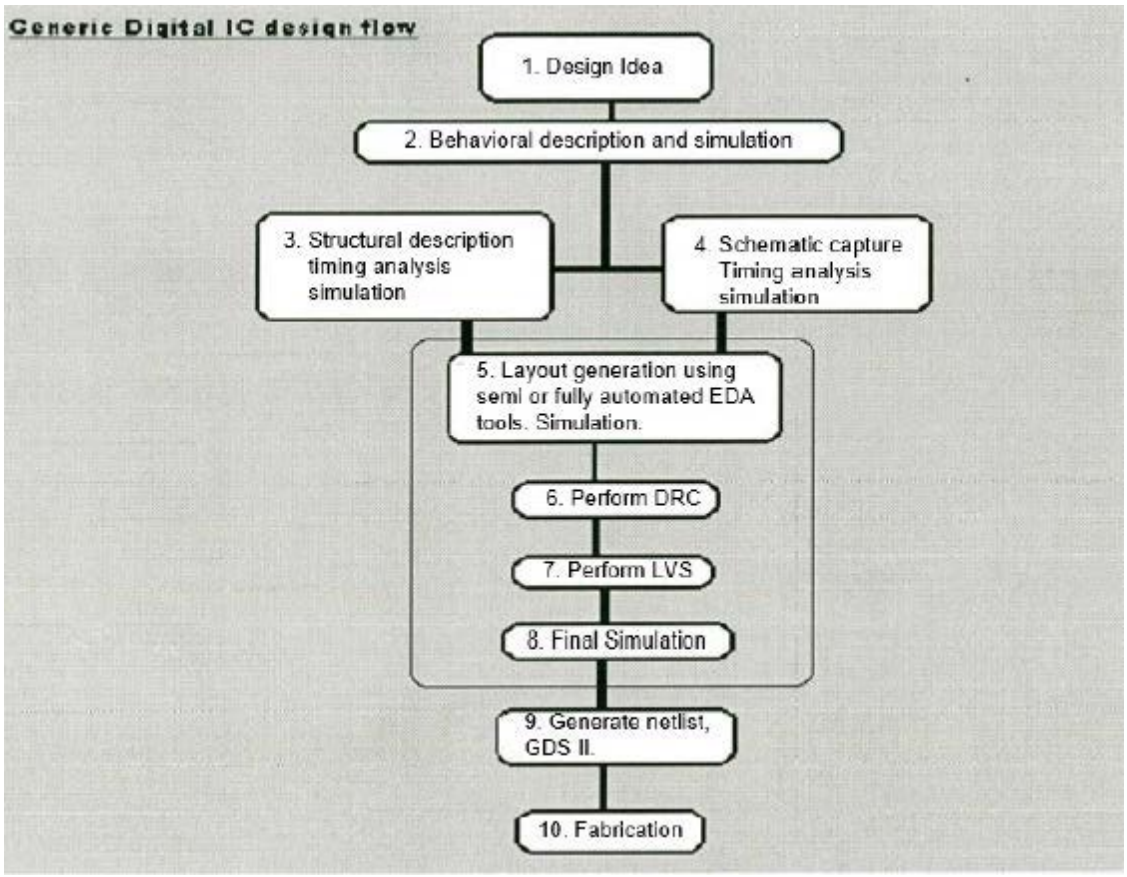


Figure 1.1, reproduced above, illustrates a general approach to various design phases of an integrated circuit design. Ex. 1205, 1–2, Fig. 1.1; *see also id.* at 3–5 (describing phases 1–5).

3. Analysis

Claim 11 is directed to a method of making an integrated circuit. Petitioner contends Oda in combination with Cwynar teaches the features of the integrated circuit recited in claim 11 and that Reddy teaches the well-known design flow phases that a skilled artisan would have implemented in making such an integrated circuit. Pet.-1200, 38–68.

For example, Petitioner asserts that Oda teaches a method of fabricating an integrated circuit having "internal circuits" and "auxiliary copper interconnects that are electrically connected to the internal circuits." *Id.* at 39 (citing Ex. 1003, ¶¶ 2, 19, 54, 63–73; Ex. 1202 ¶ 88). Similar to the

arguments set forth with respect to claim 1, described above, Petitioner asserts Oda's upper copper layer 100 (which includes interconnect layers 110 and 120) and lower copper layer 200 (which includes interconnect layers 210 and 220) underlying bond pad 130 are a plurality of interconnect layers underlying a first bond pad as recited in claim element 11[b]. *Id.* at 42–44 (citing Ex. 1203 ¶¶ 14, 16, 23, 45, 49–50, 52, 54, Fig. 2A; Ex. 1202 ¶¶ 96, 98).

Petitioner further asserts that Reddy's "design flow" for manufacturing an integrated circuit teaches "developing a circuit design of an integrated circuit" according to the circuit design as recited in step 11[b]. *Id.* at 39–40 (citing Ex. 1205, 3–4, 11, 43–64, Fig. 1-1; Ex. 1202 ¶ 89). Petitioner asserts Reddy teaches "developing a layout of the integrated circuit according to the circuit design" and Oda teaches wherein the layout comprises "a plurality of interconnect layers underlying a first bond pad of the plurality of bond pads" as recited in step 11[c]. Pet.-1200, 42–47 (citing Ex. 1001, Fig. 1; Ex. 1203 ¶¶ 5, 10–11, 14, 16, 23, 45, 48–50, 52, Fig. 2A; Ex. 1205, 4–5, 65–116, Fig. 1.1; Ex. 1202 ¶¶ 95–105). Petitioner contends that a POSITA would have been motivated to use Reddy's design phase and layout-phase teachings to manufacture the integrated circuits disclosed in Oda because, *inter alia*, doing so would have merely required combining basic prior art techniques according to known methods to yield predictable results. *Id.* at 40–41, 45–47 (citing Ex. 1202 ¶¶ 90–93, 100–103; Ex. 1213, 1:13–18, 1:43–45; Ex. 1214, 1:23–27, 3:296–31; Ex. 1205, 105, Fig. 5.29).

Patent Owner does not dispute Petitioner's assertions. We are persuaded by Petitioner's contentions and evidence that Oda in combination

with Reddy teaches the subject matter recited in the preamble 11[a][19] and claim elements 11[b]–[c] and has made a sufficient showing of articulated reasoning with rational underpinning for combining the references.

Petitioner also asserts that Oda teaches the limitations of claim elements 11[d], which requires that an interconnect layer not being electrically connected to the first bond pad and used for wiring or other interconnect other than directly to the first bond pad, for reasons similar to those set forth in connection with claim 1. *See* Pet.-1200, 47–49 (citing Ex. 1003, 11, 45, 49, 54, 61, Fig. 2A; Ex. 1202 ¶¶ 107–108). For example, Petitioner asserts that Oda discloses that there is no electrical connection (not being electrically connected) between first copper layers 210 and bonding pad 130 for the same reasons set forth in connection with claim element 1[g.i]. *Id.* at 47–49. Petitioner also asserts that Oda teaches the subject matter of claim element 11[e], for similar reasons as set forth in connection with claim elements 1[d] and [e]. *Id.* at 50–52 (citing Ex. 1202 ¶¶ 110–113; Ex. 1003 ¶¶8, 23, 35, 45, 49, 50, 76, Fig. 2A).

Petitioner also contends that Oda alone or in combination with Cwynar teach "identifying a first interconnect layer of the plurality of interconnect layers in which the first portion of the first interconnect layer has a metal density below a predetermined percentage" as recited in claim element 11[f]. *Id.* at 52–55. Petitioner asserts that Oda teaches providing dummy patterns in upper and lower copper layers under bond pad 130 and that the copper area ratio (i.e., the claimed metal density) in the layers is greater than a predetermined percentage. *Id.* at 52–53 (citing Ex. 1003

[19] Because we determine that the asserted art teaches the subject of the preamble, we do not reach the issue of whether the preamble is limiting.

¶¶ 24, 45, 55; Ex. 1202 ¶ 115). Petitioner further asserts that Cwynar also teaches a layout region having a density less than the desired density of active interconnect features and dummy fill features because Cwynar teaches a two-step process for adding "dummy fill features" of first determining an active interconnect feature density and then adding dummy fill features to each layout region in order to obtain the desired density of interconnect features and dummy fill features. *Id.* at 53 (citing Ex. 1004 ¶ 13, Fig. 3; Ex. 1202 ¶ 116). Petitioner contends that a POSITA would have (1) been motivated to add dummy metal lines as taught by Cwynar as dummy metal patterns in Oda to provide an integrated circuit that is shock resistant because (1) Oda teaches that increased metal density improves shock resistance, (2) Cwynar teaches techniques for providing dummy patterns with the requisite metal density, such as those taught in Cwynar, and (3) both Oda and Cwynar teach controlling the metal density to achieve uniform planarity. *Id.* at 53–55.

Patent Owner responds that claim 11 is patentable for essentially the same reasons set forth with respect to claim 1. *See* PO Resp.-1200, 18–25; PO Sur-reply-1200; *see also* Tr. 5:23–6:3 (noting that the disputes with respect to claims 1 and 2 challenged in IPR2019-01198 and claim 11 challenged in IPR2019-01200 overlap). For example, Patent Owner contends Oda does not teach an interconnect layer that is not electrically connected to the bond bad and is used for wiring or other interconnect other than directly to the first bond pad (Pet.-1200, 8–13). Patent Owner also argues that a POSITA would not have replaced Oda's dummy metal patterns with dummy metal lines because metal lines are inferior for achieving Oda's goals (*id.* at 36–50) and that Petitioner fails to show that Oda teaches a force

region under petitioner's own construction that recites "when a die attached is performed." *Id*. at 50–63.

Patent Owner's arguments are not persuasive for the reasons set forth above in Section II.D.3. We have reviewed and agree with Petitioner's contention the cited art teaches each of the limitations of claim 11 and has made a sufficient showing of articulated reasoning with rational underpinning for combining the references. Thus, we determine Petitioner has shown by a preponderance of evidence that claim 11 would have been obvious over the combined teachings of Oda, Cwynar, and Reddy.

G. Asserted Unpatentability of Claim 11 over Oda, Owada, and Vuong

Petitioner contends that claim 11 would have been obvious under 35 U.S.C. § 103(a) over Oda in view of Owada and Vuong. Pet.-1200, 68–88. Patent Owner opposes. For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claim 11 is unpatentable over Oda, Owada, and Vuong.

1. Overview of Vuong (Ex. 1207)

Vuong, titled "Place and Route Tool that Incorporates a Metal-Fill Mechanism," is directed to the design and manufacture of integrated circuits, and more particularly to methods for implementing metal-fill patterns on an integrated circuit. *See* Ex. 1207, code (54), (57), ¶ 2. Vuong states chemical mechanical polishing processes, which planarize dielectrics and reduce local step height, can be hampered by layout pattern dependent variation in the inter-level dielectric thickness. *See id.* ¶ 3. A common approach to reduce layout pattern dependent dielectric thickness variation is to change the layout pattern itself through the use of "metal-fill patterning." *See id.* For example, if there is an insufficient amount of metal at a particular portion on

the chip, meta-fill is required to increase the proportion of metal in that portion. *See id.* Vuong describes architecture for implementing the metal-fill mechanism in which the metal-fill mechanism is integrated into a "layout/place&route tool." *See id.* ¶ 59. Integrating the metal-fill mechanism into the layout/place&route tool allows the tool to insure sufficient information is available to adequately perform verification of the layout. *Id.* One embodiment calculates the best offset in each area to be filled (e.g., minimum spacing for the existing metal) and then dynamically adjusts shape widths and shape lengths that best fill that area. *See id.* ¶ 26.

2. Analysis

Claim 11 is directed to a method of making an integrated circuit. Petitioner contends Oda in combination with Owada teaches the features of the integrated circuit recited in claim 11 and that Vuong teaches the well-known design flow phases that a skilled artisan would have implemented in making such an integrated circuit. Pet.-1200, 68–88.

Petitioner asserts Oda teaches the limitations of claim 11 for the same reasons asserted above in Section II.F.3 regarding the asserted unpatentability of claim 11 over Oda, Cwynar, and Reddy. For example, Petitioner asserts that Oda teaches a "method of making an integrated circuit having a plurality of bond pads" as recited in the preamble. *See* Pet.-1200, 69; *see also id.* at 39 (citing Ex. 1203 ¶¶ 2, 19, 54, 63–73; Ex. 1201 ¶ 88). Petitioner asserts Oda discloses interconnect layers underlying a bond pad as recited in claim element 11[c]. *See also id.* at 42–44 (citing Ex. 1203 ¶¶ 14, 16, 23, 45, 49–50, 52, 54, Fig. 2A; Ex. 1202 ¶¶ 96, 98).

Petitioner also asserts that Vuong's use of its "Layout/Place&Route Tool" to design and manufacture integrated circuits teaches "developing a circuit design of an integrated circuit" according to the circuit design as

recited in step 11[b] as well as "developing a layout of the integrated circuit according to the circuit design" as recited in step 11[c]. *Id.* at 69–73 (citing Ex. 1207 ¶¶ 2, 59, 164, Fig. 14; Ex. 1202 ¶¶ 155–168). Petitioner contends that a POSITA would have been motivated to use Vuong's design phase and layout-phase teachings to manufacture the integrated circuits taught by Oda because, *inter alia*, doing so would have merely required combining basic prior art techniques according to known methods to yield predictable results. *Id.* at 70–71, 72–73 (citing Ex. 1202 ¶¶ 156–160, 165–168; Ex. 1213, 1:13–18, 1:43–45; Ex. 1214, 1:23–27, 3:29–31); *see also id.* at 86–88 (stating, *inter alia*, it was "ubiquitous" in the art to use CAD (computer aided design) tools to develop circuit and layout designs in fabricating integrated circuits).

Patent Owner does not dispute these contentions. We are persuaded by Petitioner's contentions and evidence that Oda in combination with Vuong teaches the subject matter recited in the preamble 11[a][20] and claim elements 11[b]–[c] and has made a sufficient showing of articulated reasoning with rational underpinning for combining the references.

Petitioner additionally contends that Oda in combination with Owada also teaches, *inter alia*, the limitations of claim elements 11[f]–[h]. Pet.-1200, 74–88. For example, with respect to claim element 11[f], which requires "identifying a first interconnect layer of the plurality of interconnect layers in which the first portion of the first interconnect layer has a metal density below a predetermined percentage," Petitioner asserts that Owada teaches identifying portions of interconnect layers having a density below a predetermined percentage so that dummy patterns can be added to increase

[20] Because we determine that the asserted art teaches the subject of the preamble, we do not reach the issue of whether the preamble is limiting.

metal density. Pet.-1200, 75–76 (citing Ex. 1206, 3:54–63; Ex. 1202 ¶ 175). Petitioner also contends Owada teaches adding dummy metal lines directly below the bond pad to increase metal density as recited in claim element 11[g] and making an integrated circuit "comprising dummy metal lines" as required by claim element 11[h]. *Id.* at 78–82, 85 (citing, *inter alia*, Ex. 1206, 5:5–27, Fig. 3; Ex. 1202 ¶ 199).

Petitioner further asserts that a POSITA would have been motivated to combine Oda with Owada to, *inter alia*, identify portions of an interconnect layer with metal density below a predetermined percentage so that, additional dummy lines can be added, as taught by Owada. *Id.* at 76 (citing Ex. 1202 ¶ 76). Petitioner points to Oda's teaching to add dummy metal patterns to first lower copper layer 210 if the metal density is low in order to improve shock resistance and to Owada's teaching of a particular technique for adding dummy patterns (i.e., adding dummy metal lines) to increase density. Petitioner contends a POSITA would have been motivated to use Owada's technique of adding dummy metal lines as one of Owada's dummy metal patterns because both control the amount of metal density to achieve uniform planarity. *Id.* at 54–55, 76–77 (citing, *inter alia*, Ex. 1203 ¶¶ 57, 59; Ex. 1202 ¶ 178. Petitioner further asserts that replacing a dummy metal pattern with dummy metal lines that serve the same function (increase metal density) would have involved substituting known prior art elements (dummy metal patterns with dummy metal lines) according to known methods (e.g., use of Oda's damascene process to fabricate metal lines) to yield predictable results (e.g., increase metal density). *Id.* at 80 (citing Ex. 1203 ¶ 21; Ex. 1216, 8:22–26; Ex. 1212, 5:20–22; Ex. 1202 ¶ 190).

We have reviewed and agree with these contentions.[21]

Patent Owner responds that claim 11 is patentable over Oda, Owada, and Vuong for essentially the same reasons we have already addressed above. In particular, Patent Owner contends Oda does not teach an interconnect layer that is not electrically connected to the bond bad and is used for wiring or other interconnect other than directly to the first bond pad as required by claim element 11[d] (PO Resp.-1198, 8–25), that Oda does not teach dummy metal lines as required by claim elements 11[g] and [h] and a POSITA would not have replaced Oda's dummy metal patterns with metal lines such as those taught by Owada (*id.* at 37–41), and that Petitioner fails to show that Oda teaches a force region under petitioner's own construction that recites "wherein a die attached is performed" (*id.* at 50–63).

Patent Owner's arguments are not persuasive. As explained above in Section II.D.3.d, we determine that Oda teaches or suggests an interconnect layer that is not electrically connected to the bond pad and is used for wiring or interconnect other than directly to the first bond pad. As explained above in Section II.E.2, we determine that it would have been obvious to a POSITA to use dummy metal lines, such as those taught in Owada, as the dummy metal patterns taught in Oda. As explained above in Section II.D.3.b, Petitioner sufficiently shows that Oda teaches a "force region" as required by the '552 patent.

[21] Because we agree with Petitioner that Oda teaches the subject matter of claim element 11[d], we do not reach Petitioner's alternative argument that Owada also teaches this claim element. *See* Section II.F.3; Pet.-1200, 74–75.

Therefore, for the reasons set forth above, we determine Petitioner has sufficiently shown that the combination of Oda, Owada, and Vuong teaches each of the limitations of claim 11 and has made a sufficient showing of articulated reasoning with rational underpinning for combining the references. Thus, we determine Petitioner has shown by a preponderance of evidence that claim 11 would have been obvious over the combined teachings of Oda, Owada, and Vuong.

H. Asserted Unpatentability of Claim 20 over Kanaoka and Weling further in view of either Reddy or Vuong

Petitioner contends that claim 20 would have been obvious under 35 U.S.C. § 103(a) over the combined teachings of Kanaoka, Weling, and Reddy or over the combined teachings of Kanaoka, Weling, and Vuong. *See generally*, Pet.-1199, 30–80; Pet. Reply-1199, 1–20. Patent Owner opposes, contending Kanaoka does not teach the subject matter of claim element 20[d]. *See generally* PO Resp.-1199; PO Sur-reply-1999. For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claim 20 is unpatentable.

1. Overview of Kanaoka (Ex. 1103)

Kanaoka, titled "Semiconductor Device and a Method of Manufacturing the Same," is directed to a semiconductor device having multiple electrode pads and wiring layers below the electrode pads. *See* Ex. 1103, codes (54), (57). Kanaoka states that the heights of electrode pads within the main surface of a semiconductor chip can differ from one another due to the different structures below the electrode pads and these height differences can cause connection failure between the electrode pads and the corresponding wirings. *Id.* at 1:37–46. Kanaoka states an object of the invention is to make the heights of the electrode pads uniform by making the

shapes, sizes and intervals of wirings below the respective electrode pads similar or equal to each other. *See id.* at code (57), 1:47–49. To accomplish this, dummy wiring is added to regions where the occupation rate of wiring is smaller than those in other regions. *See id.* at code (57). In regions where the occupation rate of wiring is larger than in other regions, slits are formed in the wiring to control the wiring occupation rate. *Id.*

2. Weling (Ex. 1105)

Weling, titled "Dummy Underlayers for Improvement in Removal Rate Consistency during Chemical Mechanical Polishing," is directed to a "method of commonizing the pattern density of topography for different layers of semiconductor wafers" to improve the chemical mechanical polishing process. Ex. 1105, codes (54), (57). Weling states that a predetermined pattern density of topography on the surface of a wafer can be achieved by inserting dummy raised lines into gaps between active conductive traces on a trace layer. *See id.* at code (57). In some embodiments, the predetermined pattern density is in the range of approximately 40% to 80%.

3. Analysis of Claim 20

a) Preamble and Claim Elements 20[b], [c], [e], and [f]

Petitioner asserts, and Patent Owner does not dispute, that the cited art teaches the subject matter recited in the preamble and claim elements [b], [c], [e], and [f] of claim 20. *See* Pet.-1199, 30–44, 48–80; *see generally* PO Resp.-1199. We have reviewed and agree with Petitioner's assertions. For example, we agree that Kanoaka discloses a "method of making an integrated circuit" (a semiconductor device) "having a plurality of bond pads" (PD and dummy pads, including dummy pad PD16) as recited in the

preamble. Pet.-1199, 31–34, 64 (citing Ex. 1103, code (54), 6:1, 10:14–17, 11:28–29, 11:51, 14:19–20, Fig. 25; Ex. 1102 ¶¶ 65–68). We also agree that Kanaoka in combination with either Reddy or Vuong teaches "developing a circuit design of an integrated circuit" as recited in claim element 20[b]. *See id*. at 34–37 (citing Ex. 1104, 3–4, 43–64, Fig. 1.1; Ex. 1102 ¶ 75–86); *id*. at 65–67 (citing Ex. 1106, 2, 59, Fig. 14, claims 6, 13, 20; Ex. 1102 ¶¶ 123–128). We further agree that Kanaoka's layers M1 and M2 are a plurality of metal-containing interconnect layers that extend under PD16 (a first bond pad of the plurality of bond pads PD) as required by claim element 20[c]. *Id*. at 37–44, 67 (citing Ex. 1103, Figs. 25, 45, 9:63–67, 10:9–17, 10:45–64, 11:3–4, 11:59–12:7, 11:3-4, 14:2–3, 14:6–16; Ex. 1102 ¶¶ 75–78, 129).

We also agree with Petitioner's assertion that both Reddy and Vuong disclose "developing a layout of the integrated circuit according to the circuit design," as recited in claim element 20[c]. *Id.* at 40–44, 67–70. We also agree with Petitioner's assertion a POSITA would have used the computer-aided design tools of either Reddy or Vuong to make the integrated circuits disclosed in Kanaoka because doing would have involved using known prior art techniques according to known methods to yield predictable results. *See id*. at 36–37 (citing Ex. 1109, 1:13–18; 1110, 1:23–27, Ex. 1102 ¶¶ 70–74), 40–44 (citing Ex. 1104, Fig. 1.1, 4–5, 65– 116; Ex. 1102 ¶¶ 80–85); *id*. at 67–70 (citing Ex. 1106 ¶ 59, Fig. 14; Ex. 1102 ¶¶ 130–135).

Claim element 20[e] recites "modifying the layout by adding dummy metal lines to the plurality of metal-containing interconnect layers to achieve a metal density of at least forty percent for each of the plurality of metal containing interconnect layers." Ex. 1001, 10:14–18. Petitioner persuasively asserts Kanaoka teaches or suggests adding dummy lines across

the entire interconnect layers M1 and M2 to achieve a metal density greater than or equal 50%. *See* Pet.-1199, 48–52 (citing Ex. 1102 ¶¶ 92–98). For example, Petitioner asserts Kanaoka teaches adding metal dummy wiring lines to the areas of metal wiring layers M1 and M2 where the metal density of layers M1 and M2 is low compared to other regions. *See id.* at 49 (citing Ex. 1103, code (57), 5:42–43, 6:4–12, 8:6–10, 12:52–66; Ex. 1102 ¶¶ 93–95). Petitioner further asserts that Kanaoka teaches making the metal density uniform in the regions below the bond pad across the entire interconnect layer by adding dummy wiring to achieve a "uniform surface" on the main surface of the integrated circuit. *See id*. at 49–50 (citing Ex. 1103, 8:6–10, Fig. 20). Petitioner further asserts the metal density rates for the entire wiring layers M1 and M2 below every bonding pad should be at least 50%. *See id.* at 51 (citing Ex. 1103, 9:13–17, 15:62–64; Ex. 1102 ¶ 97). Thus, Petitioner contends that adding dummy metal lines across the entire interconnect layers M1 and M2 to achieve a metal density greater than or equal to 50% would have been obvious in light of Kanaoka.

Petitioner also contends to the extent Kanaoka does not expressly teach modifying the layout by adding dummy metal lines to achieve a metal density of at least forty percent for each of the plurality of metal-containing interconnect layers, Weling does. *See id.* at 52. Petitioner relies on Weling's teaching of adding metal dummy lines to obtain a metal density in the range "of approximately 40–80% of the entire surface of a semiconductor wafer" and that this density requirement can be applied to different layers in an integrated circuit so that all layers have substantially the same metal density. *Id.* at 52–53 (citing Ex. 1105, 3:26–39, 3:59–61, 4:37–40, 5:48–56, 6:18– 21, Fig. 2B; Ex. 1102 ¶¶ 99–100).

Petitioner also asserts the combination of Kanaoka, Weling, and either Reddy or Vuong teaches forming the integrated circuit comprising the dummy metal lines as recited in claim element 20[f]. *See id.* at 58, 74 (stating Kanaoka teaches "a manufacturing procedure of the semiconductor device illustrated hereinabove" in which an integrated circuit including dummy metal lines is manufactured, including as modified by Weling and using the manufacturing process of Reddy or Vuong (citing Ex. 1103, 14:23–15:34; Ex. 1102 ¶ 111)).

Patent Owner does not dispute these assertions in its Patent Owner Response and therefore, any such arguments are waived. For the reasons described above, Petitioner has provided sufficient evidence to show Kanaoka and Welling in combination with either Reddy or Vuong each the subject matter recited in the preamble 20[a] and claim elements 20[b]–[c], and [e]–[f].

b) Element 20[d]

Claim element 20[d] recites "at least a portion of the plurality of metal-containing interconnect layers underlying the first bond pad and not electrically connected to the first bond pad as a result of being *used for electrical interconnection not directly connected to the bond pad*." Ex. 1001, 10:9–13 (emphasis added).

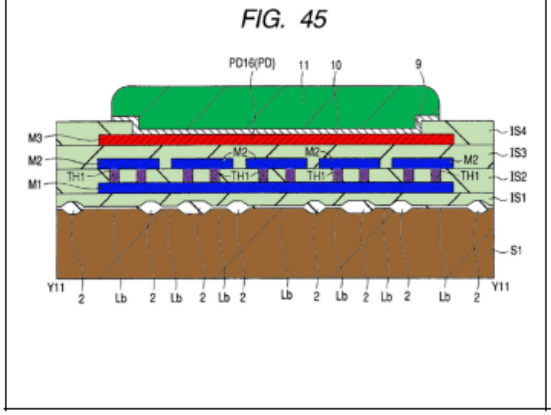
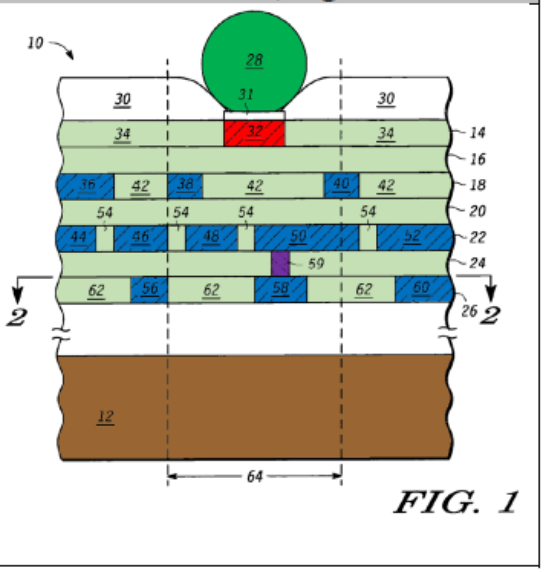
Petitioner contends Figure 45 of Kanaoka teaches "at least a portion of the plurality of metal-containing interconnect layers" (a portion of first layer wiring M1 and second layer wiring M2) "underlying the first bond pad" (underneath dummy bond pad PD16). *See* Pet.-1199, 44–45 (citing Ex. 1103, 9:13–24, 14:10–12, Fig. 45). Petitioner further asserts Kanaoka teaches that metal-containing interconnect layers M1 and M2 are "not electrically connected to the first bond pad" (dummy bond pad 16) because

layer M2 is separated from bond pad PD16 by insulating film IS3 and there are no vias that interconnect M2 to PD16. *Id.* at 44–46 (citing Ex. 1103, 10:14–17, 14:10–12, 22:31–32). Petitioner further contends that because PD16 is a dummy pad, it is not necessary to electrically connect underlying layers M1 and M2 to the bond pad. *Id*. at 45–46 (citing Ex. 1103, 14:10–12).

Patent Owner does not dispute these contentions. *See generally* PO Resp.-1199; PO Sur-reply-1199. We have reviewed, and agree with, Petitioner's contentions as set forth above.

Petitioner also contends that M1 and M2 "are used for electrical interconnect not directly connected to the bond pad" because M1 and M2 are electrically connected through a plurality of through-holes TH1 to each other but not to bond pad PD16. *See id.* at 46–48 (citing Ex. 1001, 3:38–44, Fig. 1; Ex. 1103, 13:16–19, 14:6–10, Fig. 45; Ex. 1102 ¶¶ 87–91).

A table prepared by Petitioner, depicting Figure 45 of Kanaoka and Figure 1 of the '552, with color annotations, is reproduced below.

Ex. 1103, Fig. 45	Ex. 1101, Fig. 1
	

Pet. 47. The table above depicting Figure 45 of Kanaoka and Figure 1 of the '552 patent has been annotated by Petitioner to highlight in blue the layers of each Figure that Petitioner asserts illustrate metal-containing interconnect layers. *Id.* Petitioner contends layers M1 and M2 shown in Kanaoka's Figure 45 above are connected with each other by the ten different vias TH1 (purple). *Id.* at 46–47 (citing Ex. 1103, 13:16–19, 14:6–10; Ex. 1102 ¶ 89). Petitioner states that "this is just like Figure 1 of the '552 patent," which shows metal containing interconnect layers 18, 22, and 26 (blue) electrically separated from bond pad 32, while layers 22 and 26 are electrically connected to each other by via 59 (purple).

We agree with Petitioner's contention that at least a portion of first-layer wiring M1 and second-layer wiring M2 (a plurality of metal-containing interconnect layers) are not electrically connected to bond pad 16 (the first bond pad) as a result of being used for electrical interconnection not directly connected to the bond pad. Pet. 45–46. As noted above, we agree with Petitioner's contention, which Patent Owner does not dispute, that layers M1 and M2 are not electrically connected to the bond pad. We also agree with Petitioner's contention that layers M1 and M2 are not electrically connected to the bond pad "as a result of being used for electrical interconnection not directly connected to the bond pad." Kanaoka expressly states that "second-layer wiring M2 is electrically connected with . . . first layer wiring M1 through a plurality of through-holes TH1." Ex. 1103, 13:16–19. Similarly, Kanaoka also expressly states that "second-layer M2 and . . . first-layer wiring M1, which are respectively, and underlying layer of the dummy pad P[D]16, are electrically connected to each other through a plurality of through-holes TH-1." Thus, Kanaoka teaches that metal-containing interconnect layers M1 and M2 are electrically connected to each other, but

not the first bond, and are thus a plurality of interconnect layers being used for electrical interconnection not directly connected to the bond pad.

Patent Owner contends that Petitioner fails to demonstrate that either of the metal-containing interconnect layers M1 or M2 are "used for electrical interconnection not directly connected to bond pad PD16." PO Resp.-1198, 17–45; PO Sur-reply-1199, 1–20. Patent Owner contends that M1 and M2 are "only connected to each other and, in this regard, have no electrical use at all." PO Resp.-1198 at 19; PO Sur-reply-1198, 1 (stating M1 and M2 carry no electricity, so they are not used for electrical interconnection); PO Sur-reply-1198, 5 (stating used for electrical interconnection requires that the structures that meet this limitation must actually carry electricity). Patent Owner contends that "interconnect layers that are used for electrical connection must provide connection to active devices, such as transistors, and thus are different from dummy portions that are not electrically connected to other metal structures." PO Resp.-1198, 35; *see also id.* at 37–45 (contending Kanaoka's M1 and M2 are not connected to active devices); Ex. 2024 ¶ 79 (stating used for electrical connection "means used to provide electrical connection to active devices, such as transistors, that are part of the integrated circuit").

We disagree with Patent Owner's argument because it is based on a claim construction that we did not adopt. As explained above in Section II.C.3, we do not construe "used for electrical interconnection not directly connected to the bond pad" to either require connection to active circuitry or require the actual carrying of electricity as argued by Patent Owner.

We agree with Petitioner's contention that at least a portion of Kanaoka's layers M1 and M2 are each metal containing interconnect layers underlying a bond pad. We also agree with Petitioner's contention that

Kanaoka's layers M1 and M2 are used for electrical interconnection not directly connected to the bond pad because each layer is electrically connected to another layer that is not directly connected to the bond pad (i.e., M1 is electrically connected to M2, M2 is electrically connected to M1, and neither is electrically connected to the bond pad). Indeed, Kanaoka explicitly states that "second-layer M2 and . . . first-layer wiring M1 . . . are *electrically connected to each* other through a plurality of through-holes." Ex. 1103; 14:6–10 (emphasis added); *see also id.* at 13:17–20 (stating "second-layer wiring M2 is *electrically connected* with . . . first-layer wiring M1 through a plurality of through-holes") (emphasis added); Ex. 1102 ¶ 89. Thus, because layers M1 and M2 are being used to electrically connect with each other through a plurality of through-holes, and neither layer is electrically connected to the bond pad, layers M1 and M2 are being used for electrical interconnection not directly connected to the bond pad.

c) Reason to Combine

Petitioner asserts a person of ordinary skill in the art would have combined Weling's design rule to achieve a 40–80% minimum metal density when making Kanaoka's integrated circuit because, *inter alia*, both references are directed to the same problem of ensuring that sufficient metal density is present in the interconnect layers to achieve uniform surface levels during manufacture and because using the dummy wiring and metal density requirements of Weling in Kanaoka's integrated circuit would have involved combining known and similar prior art techniques according to known methods to yield predictable results. *See* Pet.-1199, 53–54 (citing Ex. 1102 ¶¶ 99–103). Petitioner further contends a person of ordinary skill in the art would have used the well-known design flow steps of either Reddy or Vuong to make the integrated circuit of Kanaoka and Weling. *See id.* at 35–

36 (citing Ex. 1102 ¶¶ 70–74), 58–64 (citing Ex. 1102 ¶¶ 120), 74–79 (citing Ex. 1102 ¶¶ 146– 156).

Patent Owner does not dispute Petitioner's assertions. *See generally,* PO Resp. We have reviewed Petitioner's argument and evidence and determine Petitioner has made a sufficient showing of articulated reasoning with rational underpinning for combining the teachings of Kanaoka and Weling with either Reddy or Vuong.

d) Conclusion

For the foregoing reasons, we determine the evidence and arguments of record demonstrates by preponderance of evidence that claim 20 would have been obvious over the combined teachings of Kanaoka, Weling, and Reddy as well as over the combined teachings of Kanaoka, Weling, and Vuong.

III. CONCLUSION

For the reasons discussed above, we determine Petitioner has proven, by a preponderance of the evidence, that the challenged claims of the '552 patent are unpatentable, as summarized in the following tables:

IPR2019-01198

Claims	35 U.S.C.	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2	§ 103(a)	Oda, Cwynar	1, 2	
2	§ 103(a)	Oda, Cwynar, AAPA	2	
1, 2	§ 103(a)	Oda, Owada	1, 2	
		Overall Outcome	1, 2	

IPR2019-01199

Claim	35 U.S.C.	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
20	§ 103(a)	Kanaoka, Weling, Reddy	20	
20	§ 103(a)	Kanoaka, Weling, Vuong	20	
		Overall Outcome	20	

IPR2019-01200

Claim	35 U.S.C.	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
11	§ 103(a)	Oda, Cwynar, Reddy	11	
11	§ 103(a)	Oda, Owada, Vuong	11	
		Overall Outcome	11	

IV. ORDER

Accordingly, it is

ORDERED that claims 1, 2, 11, and 20 of U.S. Patent No. 7,247,552 B2 have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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