UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION,
Petitioner,

v.

BROADCOM CORPORATION,
Patent Owner.

IPR2019-01040
Patent 8,284,844 B2

RENESAS ELECTRONICS CORPORATION'S NOTICE OF APPEAL

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via E2E
Patent Trial and Appeal Board

via Hand Carry
Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
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via CM/ECF
United States Court of Appeals for the Federal Circuit

INTRODUCTION

Renesas Electronics Corporation's appeal stems from the Patent Trial and Appeal Board's Final Written Decision entered on November 12, 2020, (Paper 35) (the "Final Written Decision") and its Decision Denying Patent Owner's Request for Rehearing of Final Decision entered on April 15, 2021, (Paper 41) (the "Rehearing Decision") in the above-captioned *inter partes* review of United States Patent No. 8,284,844 ("the '844 patent"). This notice is timely filed within 63 days of the Rehearing Decision. 37 C.F.R. § 90.3(b)(1).

RENESAS ELECTRONICS CORPORATION'S APPEAL

Please take notice that under 35 U.S.C. §§ 141(c), 142, 319, 37 C.F.R. §§ 90.2(a), 90.3(a), and Federal Rule of Appellate Procedure/Federal Circuit Rule 15, Renesas Electronics Corporation hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision, the Rehearing Decision, and all underlying decisions and orders in this action on which those decisions are based.

RENESAS ELECTRONICS CORPORATION'S ISSUES ON APPEAL

Renesas Electronics Corporation's issues on appeal include at least (*see* 37 C.F.R. § 90.2(a)(3)(ii)):

(i) the Board's Final Written Decision granting Broadcom Corporation's Motion to Amend for proposed substitute claims 16-19 of the '844 patent;

(ii) the Board's Rehearing Decision maintaining its decision to grant Broadcom's Motion to Amend for those claims; and

(iii) any findings or determinations supporting or related to the aforementioned issues as well as all other issues decided adversely to Renesas Electronics Corporation in any orders, decisions, rulings, or opinions.

Simultaneously with this submission, Renesas Electronics Corporation is filing a true and correct copy of this Notice of Appeal with the Director of the United States Patent and Trademark Office and a true and correct copy (or copies) of the same, along with the required filing fee, with the Clerk of the United States Court of Appeals for the Federal Circuit as set forth in the accompanying Certificate of Filing.

Dated: June 14, 2021

Respectfully submitted,

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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through E2E, a true and correct copy of the above-captioned RENESAS ELECTRONICS CORPORATION'S NOTICE OF APPEAL is being filed by hand with the Director on June 14, 2021, at the following address:

Director of the United States Patent and Trademark Office
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The undersigned also hereby certifies that a true and correct copy of the above-captioned RENESAS ELECTRONICS CORPORATION'S NOTICE OF APPEAL and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on June 14, 2021.

Dated: June 14, 2021

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing RENESAS ELECTRONICS CORPORATION'S NOTICE OF APPEAL was served via electronic mail on June 14, 2021, by agreement of the parties, in its entirety on the following:

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Paper 35
Entered: November 12, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION,
Petitioner,

v.

BROADCOM CORPORATION,
Patent Owner.

Case IPR2019-01040
Patent 8,284,844 B2

Before THOMAS L. GIANNETTI, PATRICK M. BOUCHER, and NORMAN H. BEAMER, *Administrative Patent Judges*.

BEAMER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Denying Patent Owner's Motion to Amend As To Claim 15
Granting Patent Owner's Motion to Amend As To Claims 16–19
35 U.S.C. § 318(a)

I. INTRODUCTION

On May 6, 2019, Renesas Electronics Corporation ("Petitioner") filed a Petition pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1 and 9–14 of U.S. Patent No. 8,284,844 B2 (Ex. 1001, "the '844 patent"). Paper 2 ("Pet."). On August 22, 2019, Broadcom Corporation ("Patent Owner") filed a Preliminary Response. Paper 6. On September 6, 2019, Petitioner filed a Reply To Patent Owner's Preliminary Response. Paper 7. On September 13, 2019, Patent Owner filed a Sur-Reply To Petitioner's Reply. Paper 8.

On November 13, 2020, applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we instituted an *inter partes* review of claims 1 and 9–14. Paper 9 ("Institution Dec."). In the Institution Decision, we determined that Petitioner demonstrated a reasonable likelihood that it would prevail as to the challenged claims, and we instituted trial on all challenged claims and all grounds in the Petition. Institution Dec. 35.

Following institution, Patent Owner did not file a Response to the Petition, but did file, on February 14, 2020, a Motion to Amend, contingent on a finding of unpatentability of the original challenged claims. Paper 15, 1 ("Mot. Amend"). On May 15, 2020, Petitioner filed an Opposition to the Motion to Amend. Paper 18 ("Opp. Amend"). We issued Preliminary Guidance on May 29, 2020. Paper 19. Patent Owner filed a Reply on June 19, 2020, and Petitioner filed a Sur-Reply on July 7, 2020. Paper 25 (Reply Amend); Paper 30 (Sur-Reply Amend).

An oral hearing took place on August 19, 2020. The Hearing Transcript ("Tr.") is included in the record as Paper 33. After considering the parties' arguments and supporting evidence, we determine that Petitioner has proved by a preponderance of the evidence that claims 1 and 9–14 of the '844 patent are unpatentable. 35 U.S.C. § 316(e). We also deny Patent Owner's Motion to Amend as to substitute claim 15 and grant the Motion to Amend as to claims 16–19.

II. BACKGROUND AND SUMMARY

A. The '844 Patent

The '844 patent, titled "Video Decoding System Supporting Multiple Standards," was filed April 1, 2002, and issued October 9, 2012. Ex. 1001. The patent describes systems and methods for decoding digital video data using hardware accelerators that assist a core processor in performing decoding tasks, and which are configurable to support multiple encoding/decoding formats. *Id.* at Abstr. The disclosed hardware accelerators include a programmable entropy decoder, an inverse quantization module, an inverse discrete cosine transform module, a pixel filter, a motion compensation module and a de-blocking filter. *Id.* Exemplary public and proprietary digital video encoding/decoding formats include MPEG-1, MPEG-2 (SD/HD), MPEG-4, H.263, Microsoft Windows Media, RealNetworks, and Apple Quick Time. *Id.* at 1:47–54.

The pertinent logical architecture of the system described in the '844 patent is illustrated in Figure 3 of the patent, reproduced below.

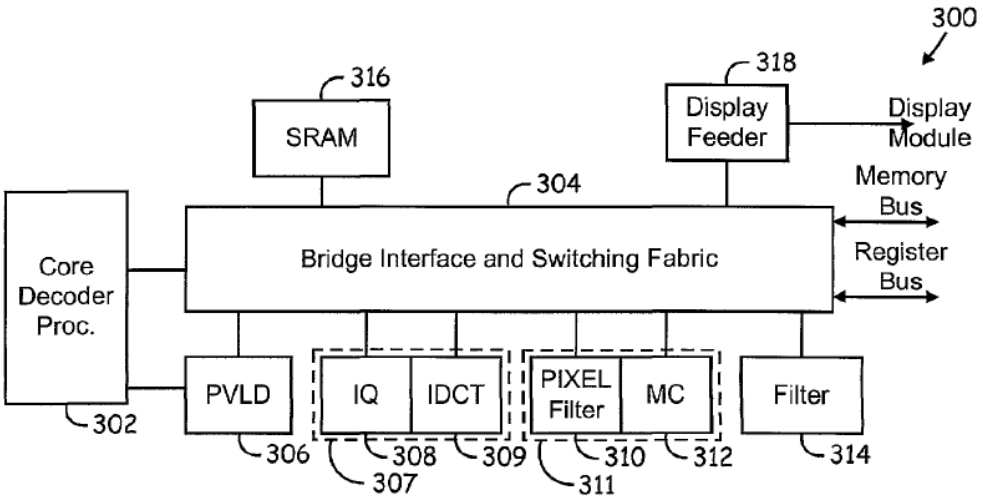

FIG. 3

Figure 3 illustrates a Digital Video Decoder in which Core Decoder Processor 302 controls the decoding of digital video data, including controlling hardware accelerators that perform the various decoding functions: programmable variable length decoding (PLVD 306), inverse quantization (IQ 308), inverse discrete cosine transformation (IDCT 309), pixel filtering (PIXEL filter 310), motion compensation (MC 312), and de-blocking (Filter 314). *Id.* at 5:41–62. The Specification provides for alternative embodiments in which inverse quantization and inverse discrete cosine transformations are performed in a single transform engine (307) "that handles all functionality, but which is conceptually equivalent to the union of **308** and **309**." *Id.* at 5:66–6:1. Similarly, pixel filtering, motion compensation, and de-blocking may be handled in single filter engine 311. *Id.* at 6:1–15; *see also id.* at Fig. 4a, 7:43–54.

The hardware accelerators are programmable to allow changes according to various processing algorithms; the programmability is facilitated by registers and/or memory associated with the accelerators and

programmed by the core processor. *Id.* at 5:62–64, 8:40–57, 9:60–63, 10:20–24, 11:59–63, 12:18–24, 12:42–47, 12:64–66, 19:58–63, 22:5–11. Alternatively, the hardware accelerators may include processors or coprocessors that can be reprogrammed by the core processor, optionally also including reprogrammable registers. *Id.* at 19:64–20:2.

B. Illustrative Claim

Challenged claim 1, which is the only independent claim in the '844 patent, is reproduced below.

> 1. A digital media decoding system comprising:
>
> a processor adapted to control a decoding process; and
>
> a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream, wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.

Ex. 1001, 20:17–23.

C. *Prior Art Relied Upon*

In the Petition, Petitioner relies on the following references. Pet. 24–25.

Fandrianto et al.	US 5,982,459	Issued Nov. 9, 1999	Ex. 1004	("Fandrianto '459")
Fandrianto et al.	US 5,379,351	Issued Jan. 3, 1995	Ex. 1005	("Fandrianto '351")
Reader et al.	US 6,192,073 B1	Issued Feb. 20, 2001	Ex. 1010	("Reader")
Harrand et al.	US 5,995,513	Issued Nov. 30, 19996	Ex. 1006	("Harrand")

In opposing the Motion to Amend, Petitioner additionally relies on the following references. Opp. Amend 11–12.

Kopet et al.	US 5,699,460	Issued Dec. 16, 1997	Ex. 1024	("Kopet")
Malladi et al.	US 5,815,206	Issued Sep. 29, 1998	Ex. 1025	("Malladi")
Wise et al.	US 6,697,930 B2	Issued Feb. 24, 2004	Ex. 1026	("Wise")

In addition, both parties also rely on declaration testimony. Petitioner provides expert declarations of Dr. Alan C. Bovik. Ex. 1003 ("Bovik Decl."); Ex. 1023 ("Bovik 2nd Decl.). Patent Owner provides expert declarations of Scott T. Acton and Dr. Joseph P. Havlicek. Ex. 2009 ("Acton Decl."); Ex. 2015 ("Havlicek Decl.").

D. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1 and 9–14 of the '844 patent on the following grounds.[1] Pet. 24–25.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 9, 10	103(a)	Fandrianto '459
11–13	103(a)	Fandrianto '459, Fandrianto '351, Reader
14	103(a)	Fandrianto '459, Fandrianto '351, Reader, Harrand

In opposition to the Motion to Amend, Petitioner asserts the following grounds of unpatentability. Opp. Amend 12–35.

[1] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the filing of the application for the '844 patent. Therefore, we apply the pre-AIA versions of these sections.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
15	§ 103(a)	Fandrianto '459, Kopet, Malladi
16–18	§ 103(a)	Fandrianto '459, Kopet, Malladi, Wise
19	§ 103(a)	Fandrianto '459, Kopet, Malladi, Wise, Harrand
15	§ 103(a)	Kopet, Malladi
16–18	§ 103(a)	Kopet, Malladi, Wise
19	§ 103(a)	Kopet, Malladi, Wise, Harrand

E. Real Parties in Interest

Petitioner identifies itself and Renesas Electronics America, Inc. as real parties in interest. Pet. 72. Patent Owner identifies itself as the real party in interest. Paper 5, 2.

F. Related Matters

The parties state that the following investigation at the International Trade Commission is a related matter: *Certain Infotainment Systems, Components Thereof, and Automobiles Containing the Same*, Inv. No. 337-TA-1119 ("the ITC-1119 proceeding").[2] Pet. 72; Paper 5, 2. Patent Owner also identifies *Broadcom Corporation v. Toyota Motor Corporation et al.*, 2-18-cv- 00190-JRG (E.D. Tex. 2018) as a related matter. Paper 5, 2.

Petitioner has also filed petitions for *inter partes* review of other of Patent Owner's patents in IPR2019-01039 and IPR2019-01041.

[2] The ITC-1119 proceeding has been terminated. Opp. Amend 4. Also, as discussed below, a previous ITC proceeding is also related: *In the Matter of Certain Semiconductor Devices & Consumer Audiovisual Prods. Containing the Same*, No. 337-TA-1047 ("the ITC-1047 proceeding").

In addition, we have previously considered the '844 patent in several prior *inter partes* review proceedings: *Amazon.com, Inc. v. Broadcom Corporation*, IPR2017-01111 ("IPR1111"); *LG Electronics, Inc. v. Broadcom Corporation*, IPR2017-01624 ("IPR1624"); *VIZIO, Inc. v. Broadcom Corporation,* IPR2019-00013 ("IPR0013"); and *LG Electronics, Inc. v. Broadcom Corporation*, IPR2018-00477 ("IPR0477"). For IPR1111 and IPR0013, petitioners Amazon and VIZIO relied on the same principal reference (Fandrianto '459) as is relied on in this proceeding, and we instituted *inter partes* review proceedings. Ex. 1002, 306–336, 355–384. Those proceedings were subsequently terminated due to settlement. *Id.* at 337–340, 390–394. IPR0477 also involved Fandrianto '459, but was terminated due to settlement prior to institution. *Id.* at 385–388. In IPR1624, petitioner LG Electronics relied on other references, and we denied institution. *Id.* at 341–354. Thus, this is the first Final Written Decision concerning the '844 patent.

III. ANALYSIS — PETITIONER'S ORIGINAL GROUNDS

A. Legal Standards — Obviousness

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called

secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results ("the *Graham* factors").[3] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *KSR*, 550 U.S. at 418. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary skill in the art would employ" when presented with the teachings of the prior art. *KSR*, 550 U.S. at 415–18. Under this flexible approach, it can be important to identify "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements" in the way claimed. *Takeda Chem. Ind., Ltd. v. Alphapharm Pty., Ltd.,* 492 F.3d 1350, 1356–57 (Fed. Cir. 2007). Such reason may be found "explicitly or implicitly in market forces; design incentives; the interrelated teachings of multiple patents; any need or problem known in the field of endeavor at the time of invention and addressed by the patent; and the background knowledge, creativity, and common sense of the person of ordinary skill." *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (internal quotations and citations omitted); *see also KSR*, 550 U.S. at 419–20.

[3] Patent Owner does not rely on any secondary considerations.

Moreover, "'if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.'" *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (quoting *KSR*, 550 U.S. at 417).

"[A] combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 416. "[I]n many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id.* at 420–421.

"The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . . Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). "Combining the *teachings* of references does not involve an ability to combine their specific structures." *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973).

B. Level of Ordinary Skill in the Art

Petitioner contends that "a person of ordinary skill in the art (POSITA) would have had a Bachelor's Degree in Electrical Engineering or similar discipline, with at least four years of experience in implementing hardware and software-based video decoders." Pet. 13 (citing Bovik Decl. ¶ 69).

Patent Owner's expert opines:

> It is my opinion that a person of ordinary skill in the art ("POSA") at the time of the invention of the '844 patent would have had a Bachelor's Degree in Electrical Engineering, Computer Science, or a similar discipline, with one to two years of experience in this or a related field. The POSA would have been familiar with software or hardware related to digital signal, image and video processing.

Acton Decl. ¶ 37.

We find both proposals, which differ from each other only in years of experience, to be consistent with the level of ordinary skill in the art reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Neither party explores how or if the difference in years of experience would impact the issues here. It is sufficient for our analysis to consider the person of ordinary skill as having had between two and four years of the experience in the field as described by the parties — our Decision is not affected by the two-year difference in experience in the proposals.

C. Claim Construction

The Petition was accorded a filing date of May 6, 2019. Paper 3, 1. In an *inter partes* review for a petition filed on or after November 13, 2018, a claim "shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b); *see* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,340, 51,358 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)).

Phillips v. AWH Corp., 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Under that standard, claim terms are generally given their ordinary and customary meaning, which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1312–13. "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* at 1313. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). However, in construing the claims, care should be taken to avoid improperly importing a limitation from the specification into the claims. *See Cont'l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797–798 (Fed. Cir. 2019) ("[m]ere criticism of a particular embodiment . . . is not sufficient to rise to the level of clear disavowal"; "use of the phrase 'present invention' or 'this invention' is not always . . . limiting, such as where the references . . . are not uniform, or where other portions of the intrinsic evidence do not support applying the limitation to the entire patent" (citations omitted)). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Claim terms need only be

construed to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).

Petitioner proposes several claim constructions, discussed below. Pet. 14–24. Patent Owner had no claim construction proposals prior to institution. In the Decision To Institute, we provided our preliminary construction conclusions in response to Petitioner's proposals. Institution Dec. 11–20. As discussed further below, Patent Owner responded to our preliminary conclusions in its Motion To Amend, and has not explicitly raised any additional claim construction issues. Mot. Amend 10–12. We further discuss the claim construction issues below.

1. "a processor adapted to control a decoding process"

Petitioner proposes that the claim 1 requirement, "a processor adapted to control a decoding process," should mean "a core processor adapted to control a decoding process according to a processing pipeline." Pet. 14–15. Petitioner relies on the fact that the ITC so construed this phrase in a September 19, 2018 Commission Opinion in the prior ITC-1047 proceeding. Ex. 1013 ("the ITC-1047 Opinion"), 463.[4] Petitioner also asserts that the parties in the ITC-1119 proceeding have agreed to this construction, and furthermore that it is supported by the intrinsic record. Pet. 14.

We do not adopt this construction. The Specification does refer to the processor that controls the decoding process as a "core processor." *E.g.*, Ex.

[4] Citations to Exhibit 1013 are to the page numbers applied to the exhibit by Petitioner. Petitioner incorrectly cites to an earlier, different claim construction in the May 11, 2018 Final Initial Determination entered by the Administrative Law Judge in the ITC-1047 proceeding. Pet. 14; Ex. 1013, 194. That construction was modified by the subsequent Commission Opinion, in the form now espoused by Petitioner. Ex. 1013, 463.

1001, Abstr. However, upon review of the Specification in its entirety, it appears that "core" is used to differentiate the claimed processor, which controls the decoding process, from the one or more claimed accelerators, which may also be processors, and which are controlled by the claimed processor. *E.g.*, *id.* at 19:64–20:2. Because the claims already specify that the processor controls the decoding process and is separate from the accelerators, the addition of the word "core" is an unnecessary redundancy that would add uncertainty to the claim.

We also do not adopt Petitioner's proposal to require the decoding process of the claims to be "according to a processing pipeline," at least insofar as it would require multiple pipelined accelerators. Again, Petitioner is correct that illustrative embodiments described in the Specification decode the digital data using a pipeline process. For example, as stated in the Abstract:

> The hardware accelerators function in a decoding pipeline wherein at any given stage in the pipeline, while a given function is being performed on a given macroblock, the next macroblock in the data stream is being worked on by the previous function in the pipeline.

Id. at Abstr. Petitioner also relies on a statement during the prosecution of the application that led to the '844 patent: "FIG. 3 shows a processor 302 that, among other things, '***orchestrates the macroblock (MB) processing pipeline*** for all modules.'" Pet. 15 (quoting Ex. 1002, 133). But neither the descriptions of illustrative embodiments in the Specification, nor statements made during prosecution, unequivocally disavow non-pipeline embodiments. To adopt Petitioner's construction would be to improperly import a limitation from the Specification. *Cont'l Circuits*, 915 F.3d at 797.

Significantly, '844 patent claim 1 only requires one accelerator. *Id.* at 20:19–23. The above-quoted description of pipelining establishes that, in order for the described pipelining to occur in a particular embodiment, there must be multiple accelerators, with a first accelerator performing one function on a first macroblock, a second accelerator performing a different function on a different macroblock, etc.[5] *Id.* at Fig. 6. Thus, the claim construction adopted by the ITC excludes an embodiment that has only one accelerator — which embodiment is covered by the plain language of claim 1. For this reason alone we are not inclined to adopt the proposed construction. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (a claim interpretation that excludes a preferred embodiment is "rarely, if ever, correct").

Confirming this view, the Specification specifically provides for an alternative embodiment in which more than one decoding function may be combined in a single pipeline stage. Ex. 1001, 16:64–17:11. In such case, all the functions of that stage are performed on a given macroblock, one function at a time, before that macroblock proceeds to the next stage. *Id.* As stated in the Specification, this embodiment "include[s] fewer pipeline stages, fewer buffers and possibly simpler control for the pipeline." *Id.* at

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[5] As explained in the ITC-1047 Opinion:

> The '844 patent explains that "decoding according to a pipeline" means that a first decoding function is performed on a first data block of a data stream, then a second decoding function is performed on the first block while the first decoding function is performed on a second block, and so on until all necessary decoding functions are performed on each block.

Ex. 1013, 465.

17:9–11. Given that claim 1 only requires one accelerator, this example must encompass a case in which "fewer pipeline stages" means "one stage" — *i.e.*, one accelerator. In such case, all the accelerated decoding functions are performed in that accelerator, acting as a single stage. The single stage is a pipeline stage only to the extent it operates in parallel with the core processor — the entire decoding process (other than what may be performed by the core processor) is performed in the accelerator on a given macroblock before the decoding of the next macroblock begins.[6]

The ITC-1047 Opinion rejected this argument, stating that a "rearranged pipeline . . . is still a pipeline," and referred to the fact that even this alternative embodiment "still consists of multiple stages." Ex. 1013, 468. We disagree with this reasoning, which does not account for the circumstance where the rearrangement is such that all the accelerator decoding functions are performed in a single stage. As defined in the Specification, "the term 'stage' can refer to all of the decoding functions performed during a given time slot, or it can refer to a functional step, or group of functional steps, in the decoding process." Ex. 1001, 15:27–31. Therefore, in a single-accelerator embodiment, each stage serially handles all the decoding functions for a macroblock in that accelerator, and

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[6] The ITC-1047 Opinion held in the context of finding noninfringement of '844 claim 1:

> [T]he Commission finds that Broadcom's "single-stage" argument is an admission that the [accused product] . . . does not operate according to a processing pipeline at all. A pipeline necessarily requires multiple stages, and Broadcom itself acknowledges that "a single stage is not a pipeline."

Ex. 1013, 469.

successive stages each process subsequent macroblocks, one at a time, in the same manner.

The ITC-1047 Opinion also relied on statements in the Specification, including a description of established decoding techniques in the background section, and a discussion comparing "fine-granularity" to "high-level granularity" approaches in the detailed description of the invention:

> The plain and ordinary meaning of "a processor adapted to control a decoding process" would encompass any processor that controls a decoding process in any manner, but the '844 patent specification disclaims such scope. The specification disclaims several types of prior art processor control [in the "Background of the Invention"] . . . and specifically disclaims a processor controlling decoding through "fine-granularity acceleration" . . . . But under the plain and ordinary meaning, claim 1 would cover a processor performing fine-granularity acceleration, as long as it also controls a configurable hardware accelerator . . . .
>
> . . . . Here, the specification describes the "present invention" as "high-level granularity acceleration," in which a core processor controls a decoding process by instructing hardware accelerators to run according to a processing pipeline . . . .

Ex. 1013, 463–464 (citing Ex. 1001, 1:59–2:31 (from "Background Of The Invention"), 5:7–29 (from "Detailed Description")). However, nothing in these portions of the '844 Specification disclaimed coverage of a non-pipelined approach.

The various techniques described in the "Background Of The Invention" section of the Specification included hardware architectures that were limited to a specific video standard, software solutions using a general-purpose processor that was inadequate for real time operation, special purpose digital signal processors with programming difficulties, or multiple

hardware components each dedicated to a single algorithm. Ex. 1001, 1:59–2:31. These portions of the Specification do not support a claim construction requiring the decoding process of the claims to be "according to a processing pipeline." The literal language of claim 1 as a whole, which requires a processor and a separate configurable accelerator coupled to the processor, sufficiently distinguishes these techniques without the embellishment of requiring decoding to be "according to a processing pipeline."

In addition, the discussion in the Specification favoring a "high-level granularity acceleration" approach over a "fine-granularity acceleration" approach does not relate to whether or not pipelining is part of the process. This comparison of "fine-granularity acceleration" to "high-level granularity acceleration" is significant in different claim construction contexts discussed below, in regard to the construction of "configurable" and "hardware accelerator." But that distinction does not support Petitioner's asserted claim construction requiring "pipelining" with multiple accelerators, because the high-level granularity approach can be realized with or without such pipelining, as demonstrated by the above-discussed single-stage embodiment described in the Specification, which adopts the high-level granularity approach.

Therefore we do not adopt Petitioner's proposed construction of "a processor adapted to control a decoding process," and agree with Patent Owner that no construction of this phrase is required. Mot. Amend 11.

2. "wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods"

Petitioner proposes that the claim 1 requirement, "wherein the accelerator is configurable to perform the decoding function according to a

plurality of decoding methods," should mean "wherein the accelerator is internally programmable by the processor to perform its decoding function according to a plurality of decoding methods." Pet. 16–17. Petitioner relies on the construction of this phrase in the prior ITC-1047 proceeding, and the agreement of the parties in the ITC-1119 proceeding. Pet. 16; Ex. 1013, 203. Patent Owner agrees with Petitioner's proposed construction. Mot. Amend 11.

We also agree with this interpretation, which we adopted in the prior IPR1625 proceeding for the reasons discussed in the decision denying institution in that proceeding. IPR1625, Ex. 1002, 346–348. In particular, this construction is supported by the above-discussed preference for "high-level granularity acceleration" *versus* "fine-granularity acceleration" stated in the '844 Specification:

> The decoding system of the present invention employs high-level granularity acceleration *with internal programmability or configurability*. . . . This contrasts with a system employing fine-granularity acceleration . . . [where] the decompression algorithm has to be implemented with firmware that uses individual low-level instructions . . . to implement a high-level function, and each instruction runs on the core processor. In the high-level granularity system of the present invention, *the firmware configures each hardware accelerator . . . without intervention from the main core processor*."

Ex. 1001, 5:7–24; Ex. 1002, 346 (emphasis added).

In addition, during prosecution of the application that led to the '844 patent, Applicants distinguished prior art based on the fact that configuration was performed externally of the accelerators, whereas the accelerators of the claimed invention were configured internally. Ex. 1002, 347–348.

Accordingly, we construe "configurable" in this context to mean "internally programmable by the processor."

3. "hardware accelerator(s)"

The term "hardware accelerator" appears in the claims of the '844 patent: for example, independent claim 1 requires a "hardware accelerator coupled to the processor," dependent claim 10 requires "a plurality of hardware accelerators coupled to the processor," and dependent claim 11 requires hardware accelerators that perform five specifically designated functions. Ex. 1001, 20:19, 20:63, 21:1–12. Petitioner proposes "accelerator" should mean a "hardware component that performs one or more operations separately from the processor to perform decoding faster than the processor alone." Pet. 18–20. Again, Petitioner relies on the construction of this phrase in the prior ITC-1047 proceeding, and the agreement of the parties in the ITC-1119 proceeding. Pet. 18; Ex. 1013, 198. Patent Owner agrees with Petitioner's proposed construction. Mot. Amend 11.

We also agree with this interpretation, which we already adopted in the prior IPR1111 proceeding for the reasons discussed in the decision granting institution in that proceeding. Ex. 1002, 311–313; *see also* Ex. 2002, 361–362. In particular, the claims provide for hardware accelerators that are "coupled" to the processor. The Specification provides that the hardware accelerators "accelerate special decoding tasks that would otherwise be bottlenecks for real-time video decoding if these tasks were

handled by the core processor **302** alone," and "help the core processor achieve the required performance." Ex. 1001, 5:59–62, 7:65–66.[7]

In addition, as discussed above, the Specification draws a distinction between "fine-granularity acceleration" and "high-level granularity acceleration." *Id.* at 5:7–29. The former involves hardware components controlled by firmware instructions run on the processor, while the latter involves components with internal programmability that are programmed by the processor but which run without intervention of the processor. *Id.* The preferred embodiment of the '844 patent uses high-level granularity acceleration, where high-level decoding functions are run "without intervention from the main core processor." *Id.* at 5:19–24. Regardless of whether the claims distinguish between these two approaches, in both, the accelerators operate separately from the processor.

Based on these aspects of the claims and Specification of the '844 patent, we construe "hardware accelerator" to mean "a hardware component that performs one or more operations separately from the processor to perform the operations faster than the processor alone."

4. "pixel filtering"

Petitioner proposes that the claim 11 term, "pixel filtering," should be construed as "the process of interpolation necessary when a reference block is translated (motion compensated) by a vector that cannot be represented by an integer number of whole-pixel locations." Pet. 20–21. Petitioner relies on the construction of this phrase in the prior ITC-1047 proceeding, and the

[7] *See also* IEEE 100, The Authoritative Dictionary of IEEE Standards Terms (7th Ed., 2000) ("hardware accelerator . . . (B) A circuit that performs hardware operations much faster than the original hardware"). Ex. 1008, 4.

agreement of the parties in the ITC-1119 proceeding. Pet. 20; Ex. 1013, 247.

As Petitioner points out, the Specification discloses that "the pixel filter **310** performs pixel filtering and interpolation as part of the motion compensation process . . . . The pixel filter **310** performs the interpolation necessary when a reference block is translated (motion-compensated) by a vector that cannot be represented by an integer number of whole-pixel locations." Ex. 1001, 11:1–19.

Patent Owner submits that it is not necessary to construe "pixel filtering." Mot. Amend 11. We agree. Although the term "pixel filtering" encompasses the above-described interpolation of fractional pixel locations during motion compensation, it is not necessary for purposes of our Decision to explicitly limit the term "pixel filtering" as proposed, and we therefore do not adopt any express construction.

5. "programmable entropy decoder"

Petitioner proposes that the claim 11 phrase, "programmable entropy decoder," should be construed as "a processor that performs variable length decoding, arithmetic decoding, or variations on either of these." Pet. 21–24. Patent Owner does not agree that the claim requires a processor. Mot. Amend 12.

As explained in the Specification, "'entropy decoding' may be used generically to refer to variable length decoding, arithmetic decoding, or variations on either of these." Ex. 1001, 4:61–64. To this extent, we agree with Petitioner's construction — *i.e.*, we construe "entropy decoding" to mean "variable length decoding, arithmetic decoding, or variations on either of these."

In regard to the argument that the programmable entropy decoder must be a processor, Petitioner relies on the fact that an illustrative embodiment of the programmable entropy decoder disclosed in the Specification is designed as a coprocessor. Pet. 23; Ex. 1001, 6:28–31.

However, we are not persuaded that claim 11 should be limited to a feature of one embodiment disclosed in the Specification, and so do not agree that the phrase "programmable entropy decoder" requires a processor to perform that decoding function. The term "programmable" applies generally to all the hardware accelerators described in the Specification, whether or not implemented as a processor: "[e]ach hardware module **306** [the programmable entropy decoder], **308**, **309**, **310**, **312** and **314** is internally configurable or programmable to allow changes according to various processing algorithms." Ex. 1001, 5:62–64.

D. Obviousness Of Claims 1, 9, and 10 Over Fandrianto '459

Petitioner challenges claims 1, 9, and 10 as unpatentable under pre-AIA 35 U.S.C. § 103(a) over Fandrianto '459. Pet. 26–43.

1. Fandrianto '459

Fandrianto '459, titled "Integrated Multimedia Communications Processor and Codec," issued November 9, 1999. Ex. 1004, codes [54], [45]. Because Fandrianto '459 issued more than one year before the filing date of the application for the '844 patent, this reference is prior art to the '844 patent under pre-AIA 35 U.S.C. § 102(b). Fandrianto '459 discloses a multimedia processor that includes a general purpose RISC (reduced instruction set computer) processor and video processors that decode video and audio bit streams. *Id.* at Abstr. Figure 2 of Fandrianto '459 is reproduced below.

Fig. 2

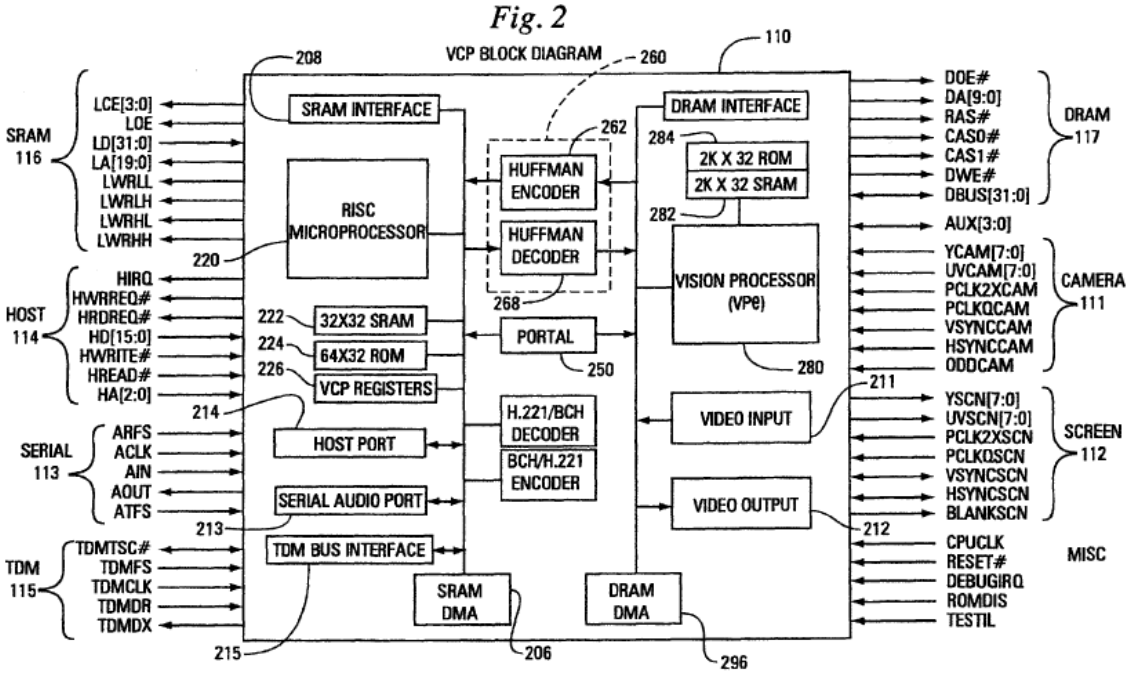

Figure 2 is a block diagram of "Video Communications Processor (VCP)" 110, including RISC microprocessor 220, "Vision Processor" 280 (also referred to as a "Video Processor"), Huffman decoder 260, and H.221/BCH decoder (referred to in the Specification with reference number 240). Ex. 1004, 2:16–17, 4:14–17, 9:19–22.

As discussed in the Decision to Institute, unlike the illustrative embodiment of the '844 patent, RISC microprocessor 220 does *not* control a decoding process according to a processing pipeline. Institution Dec. 23–24. Rather, in the Fandrianto '459 system, each compressed macroblock of data is completely decoded one block at a time — RISC microprocessor 220 programs and activates video processor 280 to perform a sequence of subroutines by downloading a queue of subroutines for execution in the video processor. Ex. 1004, 12:63–13:11. The subroutines are each executed in the video processor one at a time, in a serial fashion, on a given macroblock, without any parallel processing of any other macroblocks. *Id.*

2. Independent Claim 1

a) Claim 1 Preamble

Petitioner relies on Fandrianto '459 Figure 1 and the accompanying description (which includes a high-level representation of VCP 110) as illustrating "a digital media decoding system," as recited in the preamble of independent claim 1. Pet. 26–27 (citing Bovik Decl. ¶ 102). Patent Owner does not address whether Fandrianto '459 would have taught the preamble of claim 1. If the preamble of claim 1 is limiting, based on our review of the record and the parties' submissions, we determine that the record establishes that Fandrianto '459 would have taught the preamble.[8]

b) Claim 1 Processor Limitation

Petitioner relies on RISC microprocessor 220 of Figure 2 and related description as disclosing the claim 1 limitation, "a processor adapted to control a decoding process." Pet. 28–30 (citing Bovik Decl. ¶¶ 105–109). RISC microprocessor 220 "supervises hardware resources for input and output of compressed [audio and video] data," including "supervis[ing] operation[s] of [the] VCP," as well as Huffman decoder 260 and H.221/BCH decoder 240. Ex. 1004, 4:21–24, 5:11–16, 9:19–28. The RISC microprocessor controls the hardware accelerators by writing control information to registers or memory located in the accelerators. *Id.* at 4:46–50, 9:50–54, 11:44–47, 13:1–5. Patent Owner argues that RISC microprocessor 220 does not control Huffman decoder by writing control information to registers or memory. Mot. Amend 17–21. As discussed

[8] Because Petitioner has shown that the recitation in the preamble is satisfied by the prior art, there is no need to determine whether the preamble is in fact limiting. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

below in Section III.D.2.c)(2), we are not persuaded by that argument. Otherwise, Patent Owner does not address whether Fandrianto '459 would have taught the processor limitation of claim 1. Based on our review of the record and the parties' submissions, we determine that the record establishes that the disclosure and description of RISC microprocessor 220 in Fandrianto '459 would have taught the "processor" limitation of claim 1.

c) Claim 1 Accelerator Limitation

The second limitation of claim 1 requires:

> a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream, wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.

Ex. 1001, 20:19–23. Petitioner relies on the above Figure 2 and its description in Fandrianto '459 as rendering this limitation obvious. Pet. 30–41 (citing Bovik Decl. ¶¶ 110–135). In particular, Petitioner submits any one of Video Processor 280, Huffman decoder 260, and H.221/BCH decoder 240, each shown in Figure 2, satisfies the hardware accelerator requirement, including the above-discussed claim construction requiring that the component "performs one or more operations separately from the processor to perform decoding faster than the processor alone." *Id.* at 30–36 (citing Bovik Decl. ¶¶ 111–122). Video Processor 280 decompresses video, implementing video decoding procedures including loop filters, inverse discrete cosine transforms (DCTs), inverse quantization, and de-blocking.[9] Ex. 1004, Abstract, Fig. 9, 4:46–48, 12:48–64, 16:33–36. The Huffman

[9] As discussed in Section III.E.2 below, when taking into account the disclosure of Fandrianto '351, which is incorporated by reference into Fandrianto '459, the Video Processor also performs pixel filtering and motion compensation.

decoder 260 is a "high-speed engine" that performs variable length decoding. *Id*. at Fig. 7, 11:40–63. The H.221/BCH decoder 240 helps the RISC processor with byte alignment and bit stream parsing, and is "particularly suited for H.221 but can also be applied in decoding bit streams according to other protocols." *Id*. at Fig. 5, 9:13–28, 9:52–54. Petitioner relies on the testimony of its expert Dr. Bovik that each of these hardware components satisfies the requirement of a hardware accelerator, because each performs decoding operations separately from the RISC microprocessor, and performs those operations faster than the processor alone. Pet. 32–34 (citing Bovik Decl. ¶¶ 114–117).

In addition, Petitioner cites evidence that each of these hardware components is "configurable to perform the decoding function according to a plurality of decoding methods," as required by this limitation of claim 1, and in addition is "internally programmable by the processor" as required by the above claim construction in Section C.2. Pet. 36–41 (citing Bovik Decl. ¶¶ 123–135). The overall video communications processor (VCP) of Figure 2, "[w]ith appropriate software . . . encodes or decodes video and audio data in compliance with H.261, MPEG 1, MPEG 2, or custom proprietary compression standards." Ex. 1004, 4:17–20. Within the VCP, Video Processor 280 "is a programmable signal processor which implements video coding and decoding procedures . . . as may be required by a software selected video protocol" — for example, "decompression operations required by the MPEG, JPEG and H.261 standards as well as proprietary video compression processes." *Id.* at 12:48–57. Huffman decoder 260 employs "[l]ook-up tables [that] . . . can be volatile memory which are easily changed [as] . . . defined by the MPEG, JPEG, and H.261 standards." *Id.* at

11:44–47. H.221/BCH decoder 240 accommodates the H.221 standard or "other protocols" as a result of the RISC processor "chang[ing] templates . . . according to the protocol being employed in the bit stream." *Id.* at 9:50–54.

Patent Owner argues that none of Video Processor 280, Huffman decoder 260, or H.221/BCH decoder 240 meet the hardware accelerator limitation of claim 1. Mot. Amend 12–21. We consider those arguments for each component below.

(1) Video Processor 280 is configurable

Patent Owner argues Video Processor 280 is not "configurable to perform the decoding function according to a plurality of decoding methods," as required by the claim. Mot. Amend 13 (citing Acton Decl. 66). Patent Owner bases this on the testimony of its expert, Dr. Acton, that in order to accommodate different standards, RISC processor 220 loads new software into the internal memory of video processor 280 for each different standard. Acton Decl. ¶ 67. Dr. Acton opines that this operation is similar to that of Sullivan U.S. Patent Pub. No. 2002/0085021, prior art distinguished by a Panel Decision in an *ex parte* appeal during the prosecution of the '844 patent, and is "directly in contrast to the configurable hardware accelerators taught in the '844 Patent." *Id.* at ¶¶ 66–67 (citing Exs. 2012, 2013).

We are not persuaded by this argument. As explained in that *ex parte* appeal, the prior art Sullivan reference disclosed an API (Application Programming Interface) that could select different accelerators in order to perform different decoding functions, but none of the disclosed accelerators were themselves programmable or configurable by a processor. Ex. 2013,

5–6. In contrast, Video Processor 280 of Fandrianto '459 is itself programmed by RISC processor 220 to decode in accord with different standards. Ex. 1004, 4:45–50, 13:1–5. This is an example of the embodiment disclosed in the '844 patent, discussed further below in Section IV.B.2, in which accelerators may "comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors. . . ."[10] Ex. 1001, 19:65–20:2.

(2) Huffman decoder 260 is internally programmable by the processor

Patent Owner also argues Huffman decoder 260 is not a claimed accelerator because it is not internally programmable by the processor and does not perform the decoding function according to a plurality of decoding methods. Mot. Amend 17–21 (citing Acton Decl. ¶¶ 70–75); *see also* Reply Amend 5 (citing Havlicek Decl. ¶ 46). As discussed above, Fandrianto '459 discloses that Huffman decoder 260 employs "[l]ook-up tables [that] . . . can be volatile memory which are easily changed [as] . . . defined by the MPEG, JPEG, and H.261 standards." Ex. 1004, 11:44–47. However, as Patent Owner's expert Dr. Acton points out, Fandrianto '459 does not explicitly state that RISC processor 220 changes the look-up tables to accommodate different standards. Acton Decl. ¶ 71. Also, Dr. Acton testifies that "the operation of the Huffman decoder is the same for MPEG-1 and H.261," and

[10] As discussed in Section IV below, the proposed substitute claims are amended to explicitly exclude embodiments in which processors are configured to operate according to different encoding/ decoding formats by changing the software executed by those processors, and accordingly Video Processor 280 is excluded by those substitute claims. By the same token, as a matter of logic Video Processor 280 is *not excluded* by the original challenged claims.

therefore there would be no reason to change the look-up tables of that decoder. *Id.* at ¶ 72. In addition, Dr. Acton argues that the Huffman decoder is only capable of storing a single VLC table, and therefore is not configurable "even if that single table can be changed." *Id.* at ¶¶ 73–74.

We are not persuaded by these arguments. As discussed, Fandrianto '459 specifically teaches that "[w]ith appropriate software, VCP 110 [which includes Huffman decoder 260] encodes or decodes video and audio data in compliance with H.261, MPEG 1, MPEG 2, or custom proprietary compression standards," and further teaches that the look-up tables of Huffman decoder 260 can be volatile memory which can be changed to accommodate different video standards. Ex. 1004, 4:17–20, 11:44–47. By the time of the 2002 filing date of the '844 patent, one of ordinary skill would have known that, in addition to H.261, MPEG 1, and MPEG 2 standards explicitly mentioned in Fandrianto '459, MPEG-4 as well as "private standards . . . developed by Microsoft Corporation (Windows Media), RealNetworks, Inc., Apple Computer, Inc. (QuickTime), and others" were available to be accommodated by a decoder such as VCP 110 designed to handle different standards. Ex. 1001, 1:48–54; Bovik Decl. ¶ 27. As Dr. Acton testifies, those additional standards require different look-up tables for Huffman decoding as compared to H.261, MPEG 1, and MPEG 2. Acton Decl. ¶ 72. Therefore, one of ordinary skill, as of the filing date of the '844 patent, would have known that the look-up tables of Huffman decoder 260 would have to be changed in order to accommodate the different, then-available standards. Bovik Decl. ¶¶ 131–134. Moreover, Dr. Acton's argument (at Acton Decl. ¶ 73) that a component is not configurable "even if [the look-op] table can be changed" makes no sense —

changing the contents of the look-up table reconfigures the Huffman decoder 260 for a different standard corresponding to the new contents of the table.

Given that Fandrianto '459 teaches that VCP 110 is configurable to decode different video standards, and given that the RISC processor 220 configures the other hardware accelerators in VCP 110 — *viz.*, Video Processor 280 and H.221/BCH decoder 240 — we agree with Petitioner's expert Dr. Bovik that, to the extent that Fandrianto '459 does not explicitly state that the look-up tables of the Huffman decoder are programmable by the RISC processor, it would have been obvious to do so. Bovik Decl. ¶¶ 132–134.

(3) H.221/BCH decoder 240 performs a decoding function on a digital media data stream

Patent Owner further argues H.221/BCH decoder 240 is not a claimed accelerator because it does not "perform a decoding function on a digital media data stream." Mot. Amend 13–17 (citing Acton Decl. ¶¶ 58–63); *see also* Reply Amend 4–5 (citing Havlicek Decl. ¶ 45). In particular, Patent Owner argues that the bit stream parsing performed by H.221/BCH decoder 240, on which Petitioner relies, is not involved in decoding a digital media data stream, as required by the claim, because it only separates video data from audio and other data in the digital media data stream. Mot. Amend 14–15 (citing Acton Decl. ¶ 60). Patent Owner infers that bit stream parsing is not decoding based on the fact that, in the embodiments described in the '844 patent, the corresponding bit stream parsing is performed in Transport Processor 102, and only after the video data is separated out from the other data is it input to Digital Video Decoder 116. Acton Decl. ¶ 60 (citing Ex. 1001, Fig. 1, 4:3–7, 4:55–65).

Petitioner, relying on its expert Dr. Bovik's testimony, responds that Fandrianto '459 provides that "[b]it stream parser 510 is particularly suited for H.221 but can also be applied in ***decoding bit streams according to other protocols***," which would include different parsing functionality for MPEG-2, for example, and thus one of ordinary skill "would have understood . . . that decoding bit streams 'according to the protocol being employed in the bit stream' is a part of decoding processing." Opp. Amend 14 (citing Bovik 2nd Decl. ¶¶ 99–101, Ex. 1004, 9:52–54).

We agree with Petitioner that "separating video data from audio data is a decoding function because decoding video includes isolating the video from other signals." Sur-Reply Amend 6–7. The parties have not proposed a construction for the term "decoding," and the record does not support a narrow interpretation that would rule out the bit stream parsing as part of the decoding process. As Dr. Bovik testifies, "a person of skill in the art would have understood that parsing and decoding bit streams is part of video decoding." Bovik 2nd Decl. ¶ 99. Although the '844 patent does not describe the Transport Processor 102 as an example of a decoding accelerator, there is nothing in the patent that defines "decoder" or disavows bit stream parsing as a decoding function. Fandrianto '459 specifically uses the label H.221/BCH *decoder* 240, and includes this component in the "video communications processor (VCP)" which "decodes the MPEG system protocol and MPEG 1 and MPEG 2 standard video." Ex. 1004, Fig. 2, 2:63, 3:9–11. We conclude that the bit stream parsing performed by H.221/BCH decoder 240 is reasonably characterized, and would have been understood by the skilled artisan, as a "decoding function on a digital media data stream," as required by claim 1.

Accordingly, based on our review of the record and the parties' submissions, we determine that the record establishes that each of Video Processor 280, H.221/BCH decoder 240, and Huffman decoder 260 disclosed in Fandrianto '459 are hardware accelerators as claimed, and that Fandrianto '459 would have taught the second limitation of claim 1.

d) Claim 1 Summary

In sum, based on our review of the record and the parties' submissions, we determine that the record establishes that RISC microprocessor 220 disclosed in Fandrianto '459 is a "processor," as required by claim 1, and each of Video Processor 280, H.221/BCH decoder 240, and Huffman decoder 260 disclosed in Fandrianto '459 are hardware accelerators as required by that claim. Accordingly, we determine that Petitioner has proved by a preponderance of the evidence that claim 1 of the '844 patent would have been obvious in light of Fandrianto '459.

3. Dependent Claims 9 and 10

Claim 9 depends from claim 1 and requires "the digital media decoding system is a video decoding system and wherein the hardware accelerator is adapted to perform the decoding function on a video data stream." Ex. 1001, 20:58–61. As discussed above for claim 1, Fandrianto '459 discloses that VCP 110 of Figures 1 and 2 decodes video data using accelerators. Pet. 41–42 (citing Bovik Decl. ¶¶ 137–138).

Claim 10 depends from claim 9 and repeats the "hardware accelerator" limitation of claim 1, except it requires "a plurality of hardware accelerators" rather than "a hardware accelerator." Ex. 1001, 20:62–67. As discussed above for claim 1, Video Processor 280, Huffman decoder 260,

and H.221/BCH decoder 240 disclosed in Fandrianto '459 are hardware accelerators. Pet. 42–43 (citing Bovik Decl. ¶¶ 140–141).

Other than its arguments directed to the hardware accelerator limitation of claim 1, Patent Owner does not raise additional arguments directed to claims 9 and 10. Based on our review of the record and the parties' submissions, we determine that Petitioner has proved by a preponderance of the evidence that claims 9 and 10 of the '844 patent would have been obvious in light of Fandrianto '459.

E. Obviousness Of Claims 11–13 Over Fandrianto '459, Fandrianto '351, and Reader

Petitioner challenges dependent claims 11–13 as unpatentable under pre-AIA 35 U.S.C. § 103(a) over the combination of Fandrianto '459, Fandrianto '351, and Reader.[11] Pet. 43–64 (citing Bovik Decl. ¶¶ 142–194).

1. Fandrianto '351

Fandrianto '351, titled "Video Compression/Decompression Processing and Processors," issued January 3, 1995. Ex. 1005, codes [54], [45]. Because Fandrianto '351 issued more than one year before the filing date of the application for the '844 patent, this reference is prior art to the '844 patent under pre-AIA 35 U.S.C. § 102(b). Fandrianto '351 is "incorporated by reference [in Fandrianto '459] . . . in [its] entirety," for the

[11] Petitioner only relies on a combination including Reader for an alternative argument regarding the "programmable entropy decoder" requirement of claim 11. *See* Pet. 46–49. As discussed below, we have determined that it is unnecessary to consider that alternative. Therefore, it is unnecessary to analyze Petitioner's arguments that one of ordinary skill would have been motivated to combine Reader with Fandrianto '459 and Fandrianto '351, or that there would have been a reasonable expectation of success in implementing that combination.

purpose of "describ[ing] architectures for embodiments of video processor **280**." Ex. 1004, 13:25–34. For purposes of this Decision, we consider Fandrianto '351 as part of the single Fandrianto '459 reference.[12] (Therefore, it is unnecessary to consider the issue of motivation to combine Fandrianto '459 and Fandrianto '351.)

Fandrianto '351 discloses a "Vision Processor" for compressing and decompressing video. Ex. 1005, Abstr. The Vision Processor is shown in Figures 4, 4A, and 4B, a composite, annotated version of which is reproduced below.[13]

[12] The language incorporating Fandrianto '351 into Fandrianto '459 identifies with sufficient "detailed particularity what specific material it incorporates and clearly indicate[s] where that material is found." *Husky Injection Molding Sys. Ltd. v. Athena Automation Ltd.*, 838 F.3d 1236, 1248 (Fed. Cir. 2016); *see also Harari v. Lee*, 656 F.3d 1331, 1335–36 (Fed. Cir. 2011) (finding that prior art applications were incorporated in their entirety based on the following "broad and unequivocal language": "The disclosures of the two applications are hereby incorporate[d] by reference").

[13] This annotated version is taken from an identical figure of Fandrianto U.S. Patent 6,441,842 B1, which was provided by petitioner in IPR1111. Ex. 1002, 325. The annotations correctly describe Fandrianto '351.

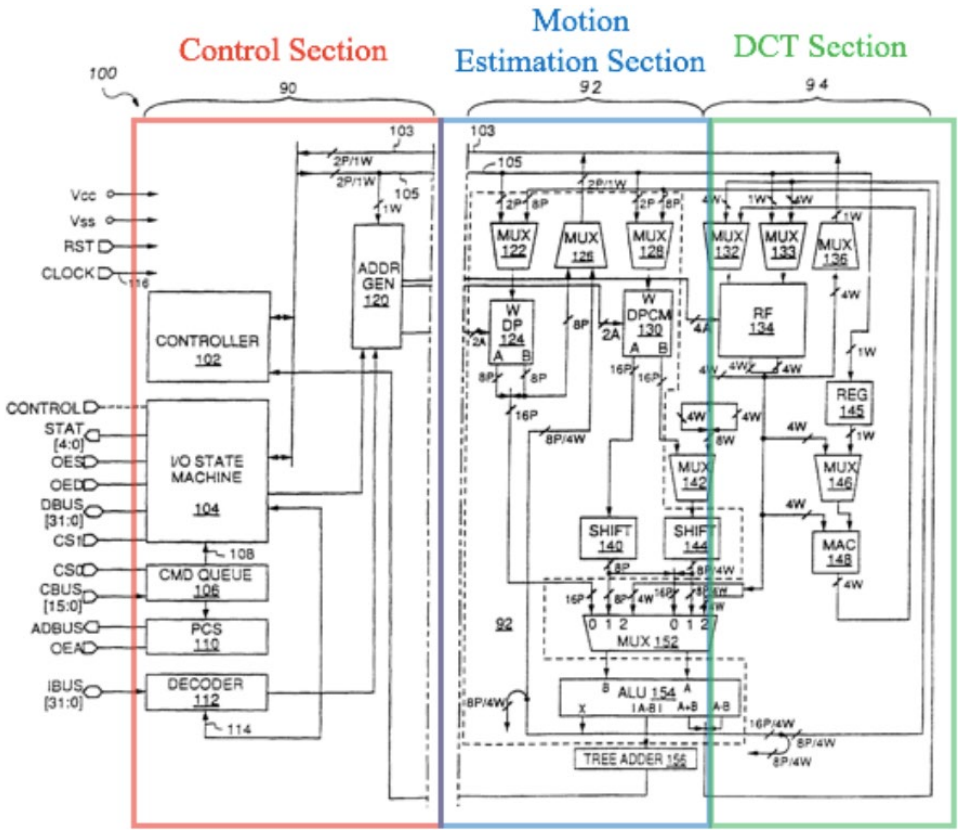

Figure 4 shows Vision Processor 100 including three sections: Control Section 90, Motion Estimation Section 92, and Discrete Cosine Transform ("DCT") Section 94. Ex. 1005, 6:17–21. Vision Processor 100 may be configured for a "variety of adopted and proposed international standards for video image compression," and performs various encoding and decoding functions depending on the particular algorithm in effect. *Id.* at 4:9–16.

2. Dependent Claim 11

Claim 11 depends from claim 10 and requires the plurality of hardware accelerators to include:

> a programmable entropy decoder adapted to perform entropy decoding on the data stream;
>
> an inverse quantizer adapted to perform inverse quantization on the data stream;

an inverse transform accelerator adapted to perform inverse transform operations on the data stream;

a pixel filter adapted to perform pixel filtering on the data stream; and

a motion compensator adapted to perform motion compensation on the data stream.

Ex. 1001, 21:1–12.

Petitioner relies on the Huffman decoder 260 disclosed in Fandrianto '459 for the programmable entropy decoder. Pet. 43–44 (citing Bovik Decl. ¶ 146). As discussed for claim 1, the Huffman decoder performs variable length decoding. Ex. 1004, Fig. 7, 11:40–63. As explained in the '844 patent, "[t]he term 'entropy decoding' may be used generically to refer to variable length decoding. . . ." Ex. 1001, 4:61–63. Patent Owner argues that Huffman decoder 260 is not internally programmable by the processor and does not perform the decoding function according to a plurality of decoding methods. Mot. Amend 17–18. As discussed in Section III.D.2.c)(2) above, we are not persuaded by that argument, and have determined that that the record establishes that Huffman decoder 260 is a programmable entropy decoder adapted to perform entropy decoding on the data stream, as claimed.[14]

For the inverse quantizer and inverse transform accelerator requirement of claim 11, Petitioner relies on the Fandrianto '459 Video

[14] As discussed in claim construction Section III.C.5, we have not adopted Petitioner's proposed construction requiring the programmable entropy decoder to be a processor. Accordingly, we need not consider Petitioner's arguments that it would have been obvious to implement Huffman decoder 260 as a processor, whether considering Fandrianto '459 alone or in combination with Reader. *See* Pet. 44–49.

Processor 280. Pet. 50–52 (citing Bovik Decl. ¶¶ 158–164). As discussed for claim 1, Fandrianto '459 discloses that the Video Processor decompresses video, implementing video decoding procedures including inverse quantization and inverse discrete cosine transforms (DCTs). Ex. 1004, 12:48–53. Patent Owner does not specifically address whether Video Processor 280 teaches these two limitations of claim 11. Accordingly, based on our review of the record and the parties' submissions, we determine that the record establishes that the Video Processor 280 disclosure of Fandrianto '459 would have taught the inverse quantizer and inverse transform accelerator limitations of claim 11.

For the pixel filter and motion compensator of claim 11, Petitioner relies on the fact that the Video Processor of Fandrianto '459 performs motion estimation, and on the description of the motion estimation section 92 in Fandrianto '351, which is incorporated by reference into the disclosure of Fandrianto '459. Ex. 1004, 12:48–50; Ex. 1005, 6:41–7:57; Pet. 55–59 (citing Bovik Decl. ¶¶ 170–182). Indeed, Fandrianto '459 specifically states that Fandrianto '351 "describe[s] architectures for embodiments of video processor 280." Ex. 1004, 13:25–30. Thus, Video Processor 280 includes the Fandrianto '351 disclosure of a motion estimation section that performs half-pixel and quarter-pixel interpolation as part of the motion estimation process. Ex. 1005, 6:64–7:3. As discussed in the claim construction section, this describes pixel filtering. Bovik Decl. ¶ 170. Also, motion compensation is the decoding counterpart to motion estimation, and therefore the discussion in Fandrianto '351 of the latter

teaches or suggests the former.[15] As stated in Fandrianto '351, "[t]he terms 'motion estimation[],' 'motion compensation,' and 'motion prediction' are used interchangeably." Ex. 1005, 6:26–28; Bovik Decl. ¶ 178. Moreover, Fandrianto '351 implicitly refers to motion compensation in describing decoding a frame in "predictive mode":

> The prediction error is added to the appropriate block, as determined by the decoded motion vector, to obtain a block of the reconstructed picture, which is stored in an external memory in step **193**.

Ex. 1005, 12:20–32; Bovik Decl. ¶ 179.

Patent Owner does not specifically address whether Video Processor 280, including the pertinent portions of Fandrianto '351 incorporated by reference into the description of Video Processor 280, teaches the pixel filter and motion compensator limitations of claim 11. Accordingly, based on our review of the record and the parties' submissions, we determine that the record establishes that the Video Processor 280 disclosure of Fandrianto '459 and Fandrianto '351 would have taught these limitations of claim 11.[16]

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[15] Both Fandrianto references establish that it is well known in the art that the various functional steps that take place when video data is compressed (encoded) necessarily have corresponding inverse operations when that video data is subsequently decompressed (decoded): e.g., Huffman coding/decoding (i.e., variable length encoding/decoding); discrete cosine transforms (DCTs)/inverse DCTs; and quantization/inverse quantization. Ex. 1004, 11:40–42, 12:48–52; Ex. 1005, Figs. 4A, 4B, 11:3–12:32. Likewise, motion compensation is the decoding counterpart to motion estimation. Ex. 1005, 12:20–32.

[16] Although Patent Owner does not raise the issue, we note that Petitioner appropriately relies on Video Processor 280 of Fandrianto '459 as teaching or suggesting, in whole or in part, each of the required inverse quantizer, inverse transform accelerator, pixel filter, and motion compensator hardware accelerators of claim 11. As we determined in IPR1111, this reliance is

In sum, based on our review of the record and the parties' submissions, we determine that Petitioner has proved by a preponderance of the evidence that claim 11 of the '844 patent would have been obvious in light of Fandrianto '459, including the pertinent material incorporated by reference from Fandrianto '351. *Ipso facto*, Petitioner has proved by a preponderance of the evidence that claim 11 would have been obvious in light of the combination of Fandrianto '459 and Fandrianto '351.[17]

3. Dependent Claims 12 and 13

Claim 12 depends from claim 11, and adds a de-blocking filter as an additional required hardware accelerator. Ex. 1001, 21:13–16. Fandrianto '459 discloses a de-blocking filter as part of the functionality of Video Processor 280. Ex. 1004, 16:33–36; Pet. 63–64 (citing Bovik Decl. ¶¶ 188–192).

Claim 13 depends from claim 11 and additionally requires "the processor is adapted to configure each of the accelerators to perform the decoding function according to a format of the media data to be decoded." Ex. 1001, 22:2–4. Petitioner relies on the disclosure in Fandrianto '459, including the incorporation of Fandrianto '351, of the RISC processor 220 configuring the Video Processor 280, Huffman decoder 260, and H.221/BCH decoder 240, as discussed above for claim 1. Pet. 64 (citing Bovik Decl. ¶ 193). One of ordinary skill in the art would have understood

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consistent with the requirements of claim 11, which does not exclude a single hardware accelerator component successively performing these four required decoding functions. *See* Ex. 1002, 328–329.

[17] As stated above, it is unnecessary to consider the combination of Fandrianto '459, Fandrianto '351, and Reader, given Petitioner's alternative arguments.

that the reference in the claim to "format of the media data to be decoded" was a reference to the various digital video standards referred to in the '844 patent — indeed, the '844 patent describes such standards as "public *format* standards." Bovik Decl. ¶ 194; Ex. 1001, 1:48–52 (emphasis added).

Patent Owner does not address whether claims 12 and 13 would have been obvious in light of Fandrianto '459 and Fandrianto '351. Based on our review of the record and the parties' submissions, we determine that Petitioner has proved by a preponderance of the evidence that claims 12 and 13 of the '844 patent would have been obvious in light of that combination.[18]

F. Obviousness Of Claim 14 Over Fandrianto '459, Fandrianto '351, Reader, and Harrand

Petitioner challenges dependent claim 14 as unpatentable under pre-AIA 35 U.S.C. § 103(a) over the combination of Fandrianto '459, Fandrianto '351, Reader, and Harrand. Pet. 65–72 (citing Bovik Decl. ¶¶ 195–209).[19]

Harrand, titled "Multitask Processing System," issued November 30, 1999. Ex. 1006. Because Harrand issued more than one year before the filing date of the application for the '844 patent, this reference is prior art to the '844 patent under pre-AIA 35 U.S.C. § 102(b).

Harrand is directed to a multitask processing system, applicable to picture processing, that includes a multitask processor supplying command instructions to control operators, which include status registers that can be read by the processor to determine, for example, if the operator is ready to

[18] Again, it is unnecessary to consider a combination including Reader.

[19] As explained in the previous sections, it is only necessary to consider the combination of Fandrianto '459, Fandrianto '351, and Harrand.

receive data. Ex. 1006, Abstr., Fig. 2, 1:60–61, 3:2–8, 28–39, 4:5–11, 4:34–40.

> Claim 14 depends from claim 11 and additionally requires:
>
> wherein each of the accelerators includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator and wherein the processor programs the registers or the memory in order to configure the accelerator and wherein the processor reads the registers or the memory in order to derive operational status of the accelerator.

Ex. 1001, 22:6–13. In addition to the above-discussed memory and look-up tables controlling the operations of Video Processor 280 and Huffman decoder 260, Petitioner relies on the disclosure in Fandrianto '459 of VCP registers associated with these accelerators which control their operations and are programmed by RISC processor 220. Pet. 65–67 (citing Bovik Decl. ¶¶ 196–200); Ex. 1005, 4:24–28, 4:38–42, 4:64–5:10, 5:16–20 12:64–13:11.

For the claim 14 requirement, "the processor reads the registers or the memory in order to derive operational status of the accelerator," Petitioner relies on the combination of Fandrianto '459 and Harrand, and in particular on the status registers of Harrand that are read by a processor to derive operational status. Pet. 68–70 (citing Bovik Decl. ¶¶ 202–205). Petitioner's expert Dr. Bovik first testifies that RISC processor 220 of Fandrianto '459 can access the address space of VCP registers 226, and therefore one of ordinary skill would have understood that the RISC processor was able to read and write from and to the VCP registers. Bovik Decl. ¶ 202. Dr. Bovik further opines that it would have been obvious in light of Harrand to modify RISC processor 220 so that it would derive operational status of the hardware accelerators, in order that it could be aware of what the

accelerators are doing and when operations are completed. Bovik Decl. ¶¶ 203, 206–207.

Patent Owner does not address whether claim 14 would have been obvious in light of Fandrianto '459, Fandrianto '351, and Harrand. Based on our review of the record and the parties' submissions, we determine that Petitioner has proved by a preponderance of the evidence that one of ordinary skill would have been motivated to apply the register read functionality of Harrand to the system of the Fandrianto patents, and has proved by a preponderance of the evidence that claim 14 of the '844 patent would have been obvious in light of that combination.

IV. ANALYSIS — MOTION TO AMEND

Patent Owner's Motion to Amend seeks to substitute new claims 15–19 for claims 10–14, respectively, contingent on a finding of unpatentability of the original challenged claims. Mot. Amend 1. The proposed substitute claims 15 and 16 are set forth below, with the proposed amendments indicated.

> 15. The video decoding system of claim 9 comprising a plurality of hardware accelerators coupled to the processor, each accelerator adapted to perform a decoding function on the video data stream, wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods, and wherein the plurality of hardware accelerators do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors.
>
> 16. The video decoding system of claim [10] 15 wherein the plurality of hardware accelerators comprise at least four of:

a programmable entropy decoder adapted to perform entropy decoding on the data stream;

an inverse quantizer adapted to perform inverse quantization on the data stream;

an inverse transform accelerator adapted to perform inverse transform operations on the data stream;

a pixel filter adapted to perform pixel filtering on the data stream; and

a motion compensator adapted to perform motion compensation on the data stream.

Mot. Amend Appx. 1–2. Proposed substitute claims 17–19 change only the dependency of claims 12–14 to depend from claim 16 instead of claim 11. *Id.* at Appx. 2.

A. The Applicable Law

In an *inter partes* review, amended claims are not added to a patent as of right, but rather must be proposed as a part of a motion to amend. 35 U.S.C. § 316(d). The Board must assess the patentability of proposed substitute claims "without placing the burden of persuasion on the patent owner." *Aqua Prods., Inc. v. Matal*, 872 F.3d 1290, 1328 (Fed. Cir. 2017) (en banc); *see* "Guidance on Motions to Amend in view of *Aqua Products*" (Nov. 21, 2017) (https://www.uspto.gov/sites/default/files/documents/guidance_on_motions_to_amend_11_2017.pdf) ("Guidance"). Subsequent to the issuance of *Aqua Products* and the Board's Guidance, the Federal Circuit issued a decision in *Bosch Automotive Service Solutions, LLC v. Matal*, 878 F.3d 1027 (Fed. Cir. 2017) ("*Bosch*"), as well as a follow-up Order amending that decision on rehearing. *See Bosch Auto. Serv. Sols., LLC v. Iancu*, Order on Petition for Panel Rehearing, No. 2015-1928 (Fed. Cir. Mar. 15, 2018).

In accordance with *Aqua Products*, the Board's Memorandum, and *Bosch*, Patent Owner does not bear the burden of persuasion to demonstrate the patentability of the substitute claims presented in the motion to amend. Rather, ordinarily, "the petitioner bears the burden of proving that the proposed amended claims are unpatentable by a preponderance of the evidence." *Bosch*, 878 F.3d at 1040 (as amended on rehearing); *see Lectrosonics, Inc. v. Zaxcom, Inc.*, IPR2018-01129, Paper 15 at 4 (PTAB Feb. 25, 2019) (precedential). In determining whether a petitioner has proven unpatentability of the substitute claims, the Board focuses on "arguments and theories raised by the petitioner in its petition or opposition to the motion to amend." *Nike, Inc. v. Adidas AG*, 955 F.3d 45, 51 (Fed. Cir. 2020). "The Board itself also may justify any finding of unpatentability by reference to evidence of record in the proceeding." *Lectrosonics*, Paper 15 at 4 (citing *Aqua Products*, 872 F.3d at 1311 (O'Malley, J.)).[20] Thus, the Board determines whether substitute claims are unpatentable by a preponderance of the evidence based on the entirety of the record, including any opposition made by the Petitioner.

Notwithstanding the foregoing, Patent Owner's proposed substitute claims must meet the statutory requirements of 35 U.S.C. § 316(d) and the procedural requirements of 37 C.F.R. § 42.121. *See Lectrosonics*, Paper 15 at 4–8. Patent Owner must demonstrate: (1) the amendment proposes a

[20] *But see Hunting Titan, Inc. v. DynaEnergetics Europe GmbH*, IPR2018-00600, Paper 67 at 4–5, 25–26 (PTAB July 6, 2020) (precedential) (concluding that the Board may itself raise grounds of unpatentability only in "rare circumstances . . . limited to situations in which the adversarial process fails to provide the Board with potential arguments of patentability with respect to the proposed substitute claims")

reasonable number of substitute claims; (2) the proposed claims are supported in the original disclosure; (3) the amendment responds to a ground of unpatentability involved in the trial; and (4) the amendment does not seek to enlarge the scope of the claims of the patent or introduce new subject matter. *See* 35 U.S.C. § 316(d); 37 C.F.R. § 42.121.

B. Predicate Requirements

1. Reasonable Number of Substitute Claims

By statute, in a motion to amend, a patent owner may propose a reasonable number of substitute claims for each challenged claim. 35 U.S.C. § 316(d)(1)(B). There is a rebuttable presumption that a reasonable number of substitute claims per challenged claim is one substitute claim. 37 C.F.R. § 42.121(a)(3). Patent Owner proposes a single substitute claim per original challenged claim, and therefore is presumed to meet this requirement. Mot. Amend 3. Petitioner does not contest that Patent Owner has met this requirement. Accordingly, we determine that Patent Owner has proposed a reasonable number of substitute claims for each challenged claim.

2. Support in the Original Disclosure

A motion to amend may not present substitute claims that introduce new subject matter. 35 U.S.C. § 316(d); 37 C.F.R. § 41.121(a)(2)(ii). New matter is any addition to the claims without support in the original disclosure. *See TurboCare Div. of Demag Delaval Turbomach. v. Gen. Elec. Co.*, 264 F.3d 1111, 1118 (Fed. Cir. 2001) ("When [an] applicant adds a claim . . . the new claim[] . . . must find support in the original specification."). Patent Owner provides citations to the application from which the '844 patent issued to show written description support for each limitation in the proposed substitute claims, and additionally provides

explanation for the newly added limitations in proposed substitute claims 15 and 16. Mot. Amend 4–10 (citing Ex. 2008; Acton Decl. ¶¶ 49–51).

Petitioner first argues Patent Owner fails to meet this requirement because, for many of the claim limitations of the proposed substitute claims, Patent Owner provides "bare citations . . . coupled with its scant explanation," and "provides nothing but bare string cites to show written description support for the majority of the claims." Opp. Amend 2–3.

We are not persuaded by the argument that string cites, in general, are insufficient to set forth written description support. For the limitations of the proposed substitute claims that are common to the cancelled claims, we find that the citations provided by Patent Owner provide sufficient support. We note, for example, that all of the limitations carried over from the original challenged claims were unchanged during prosecution and were submitted with the original application. *C.f.*, Ex. 1001, 20:17–22:13, *with* Ex. 2008, 33–35; *see Mentor Graphics Corp. v. EVE-USA, Inc.*, 851 F.3d 1275, 1297 (Fed. Cir. 2017) ("Original claims are part of the original specification and in many cases will satisfy the written description requirement").

With respect to the newly added negative limitation in proposed substitute claim 15, Petitioner not only challenges the sufficiency of Patent Owner's support for the limitation, but also alleges that the proposed substitute claim is invalid as lacking written description pursuant to 35 U.S.C. § 112, first paragraph. Opp. Amend 6–9. Petitioner contends that the negative limitation — "and wherein the plurality of hardware accelerators do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors" — fails to satisfy the support

requirements of *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350, 1355 (Fed. Cir. 2015) (quoting *Santuarus, Inc. v. Par Pharm.*, 694 F.3d 1344, 1351 (Fed. Cir. 2012)), which holds that "[n]egative claim limitations are adequately supported when the specification describes a reason to exclude the relevant limitation," and that "properly describing alternative features – without articulating advantages or disadvantages can constitute a 'reason to exclude.'" *Id.* at 6–7.

Petitioner points out that some of the citations offered by Patent Owner to support the negative limitation of claim 15 — paragraphs 4, 5, and 28 of the originally filed '798 application (Exhibit 2008) — are not pertinent, but rather describe the disadvantages of using a single processor to decode video without using accelerators, or generally describe the use of accelerators without specifying whether or not the accelerators are implemented with programmable processors. Opp. Amend 7–8 (citing Bovik Decl. ¶¶ 32–37). Petitioner also argues that Patent Owner's reliance on paragraph 84 of the '798 application, although more related to the issue, is nonetheless insufficient. Opp. Amend 6–9. That paragraph states:

> In another illustrative embodiment, some or all of the hardware accelerators comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors, in addition to programming registers as appropriate to the design.

Ex. 2008 ¶ 84. Petitioner argues that this citation does not provide details on the structure and operation of the disclosed hardware accelerators sufficient to determine whether or not any of those accelerators satisfy this negative limitation. Opp. Amend 7 (citing Bovik 2nd Decl. ¶¶ 30–31). Petitioner also argues that this paragraph "does not provide a reason to exclude 'software

based' accelerators nor does it 'properly describe alternative features' to the software based embodiment," as required by *Inphi*. *Id.* at 8 (citing Bovik 2nd Decl. ¶¶ 38–40). Dr. Bovik testifies that the '798 application "does not specify or explain how to implement the '844 patent's hardware accelerator without programmable processors," or "provide any reason why a person of skill in the art would implement a hardware accelerator without a processor." Bovik 2nd Decl. ¶ 39. Dr. Bovik states that "[i]t is not apparent from the disclosure . . . how a hardware accelerator that did not include programmable processors, would be able to handle future encoding/decoding formats." *Id.*

Petitioner also argues proposed substitute claims 16–19 lack support. Opp. Amend 10–11 (citing Bovik 2nd Decl. ¶¶ 45–71).[21] Petitioner not only relies on its arguments directed to claim 15, but further argues that the '798 application does not provide any reason why any of the specifically enumerated accelerators of proposed substitute claims 16 and 17 — programmable entropy decoder, inverse quantizer, inverse transform

[21] Petitioner devotes one conclusory paragraph addressing proposed substitute claims 16–19 in the opposition brief, and cites to 23 paragraphs of its expert's declaration in support. This does not comply with the requirement of 37 C.F.R. § 42.6(a)(3), that "Arguments must not be incorporated by reference from one document into another document." *Cisco Systems, Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12 at 8 (PTAB Aug. 29, 2014) (informative) ("The practice, here, of using footnotes to cite large portions of another document, without sufficient explanation of those portions, amounts to incorporation by reference"). Accordingly, we will not consider arguments that are not made in the Petition, but instead appear only in the cited paragraphs of Dr. Bovik's second declaration.

accelerator, pixel filter, motion compensator, and de-blocking filter — would satisfy the negative limitation.[22] *Id.*

Patent Owner responds that it meets the requirements of the applicable authorities, which provide that a negative limitation may be supported if the subject matter excluded by the limitations is one of "*alternative elements . . . positively recited in the specification*." Reply Amend 1 (citing *Inphi Corp.*, 805 F.3d at 1356). Patent Owner asserts that the '798 application positively recites, as one alternative, hardware accelerators that satisfy the negative limitation because they are described as "configured to operate according to different encoding/decoding formats 'through register read/write,' where '[t]he core processor programs registers in each module to modify the operational behavior of the module.'" *Id.* at 2 (citing Ex. 2008, ¶ 83; Havlicek Decl. ¶ 38). Patent Owner further submits that the '798 application positively recites, as "another illustrative embodiment," hardware accelerators that do not meet the negative limitation, because they include "programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors." *Id.* (citing Ex. 2008, ¶ 84). Patent Owner relies on the grammatical force of the statement in the '798 application that "some or all of the hardware accelerators" may be processors that are configured via changing their software, which according to Patent Owner, supports

[22] We note that proposed substitute claim 16 requires only four out of five enumerated accelerators to satisfy the negative limitation of proposed substitute claim 15, and accordingly proposed substitute claim 17 does not additionally require the sixth enumerated accelerator — the de-blocking filter — to satisfy that limitation.

embodiments in which some accelerators satisfy the negative limitation and some do not. *Id.* at 2–3; Havlicek Decl. ¶ 40.

We find that the '798 application supports the proposed negative limitation. As stated above, under 35 U.S.C. § 112, first paragraph, the written description requirement is satisfied when "the description 'clearly allow[s] persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed.'" *Inphi Corp.*, 805 F.3d at 1355 (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1562–63 (Fed. Cir. 1991)). "In particular, '[n]egative claim limitations are adequately supported when the specification describes a reason to exclude the relevant limitation.'" *Id.* Such a reason to exclude may be provided "by properly describing alternative features of the patented invention." *Id.* at 1356. As Patent Owner argues, and as Petitioner ultimately agrees in its Sur-Reply Brief, under the authority of *Inphi*, negative claim limitations are supported by such alternative disclosures "without articulating advantages or disadvantages." Reply Amend 1; Sur-Reply Amend 3–4 (quoting *Inphi Corp.,* 805 F.3d at 1356). That is, "[i]f alternative elements are positively recited in the specification, they may be explicitly excluded in the claims." *Inphi Corp.,* 805 F.3d at 1356.

In arriving at our finding, we note that the bulk of the application describes various alternative embodiments that have hardware accelerators that meet the negative limitation — *viz.*, hardware accelerators that "do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors." Instead, the hardware accelerators are

configured by core processor 302 writing control parameters to registers associated with each hardware accelerator:

> For the programmable entropy decoder:
>
> In an illustrative embodiment of the present invention, the PVLD 306 includes *a register that the core processor can program* to guide the PVLD 306 to search for the VLC table of the appropriate encoding/decoding algorithm.

Ex. 2008, ¶ 42 (emphasis added).[23]

> For the inverse quantizer:
>
> In an illustrative embodiment of the present invention, the IQ module 308 includes one or more registers that are used to program the scan pattern, quantization matrix and mismatch control method. These *registers are programmed by the core processor* 302 to dictate the mode of operation of the IQ module.

Id. ¶ 47 (emphasis added).

> For the inverse transform accelerator:
>
> In an illustrative embodiment of the present invention, the inverse transform module 309 includes a register that is used to program the matrix size. This *register is programmed by the core processor* 302 according to the appropriate matrix size for the encoding/decoding format of the data stream being decoded.

Id. ¶ 48 (emphasis added).

> For the pixel filter:
>
> In an illustrative embodiment of the present invention, the pixel filter 309 includes one or more registers that are used to program the filter algorithm and the block size. These *registers are programmed by the core processor* 302 according to the

[23] PVLD 306 also can include random access memory that can be configured by the core processor with different tables of variable length codes. Ex. 2008, ¶¶ 42–43.

> motion compensation technique employed with the encoding/decoding format of the data stream being decoded.

Id. ¶ 53 (emphasis added).

For the motion compensator:

> In an illustrative embodiment of the present invention, the motion compensation module 312 includes one or more registers that are configurable to select the block size and format. These *registers are programmed by the core processor* 302 according to the motion compensation technique employed with the encoding/decoding format of the data stream being decoded.

Id. ¶ 54 (emphasis added).

For the de-blocking filter:

> In an illustrative embodiment, the filter module 314 (or loop filter 313 and post filter 315) has a register that controls whether a loop filter or post filter scheme is employed. *The core processor 302 programs the filter module register(s)* according to the bitstream semantics. . . . The core processor 302 can program operational parameters into loop filter 313 and post filter 315 registers at any time.

Id. ¶ 55 (emphasis added).

In sum:

> Each hardware module 306, 308, 309, 310, 312, 313, 315 is independently controllable by the core processor 302. The core processor 302 drives a hardware module by issuing a certain start command after checking the module's status. In one embodiment, the *core processor 302 issues the start command by setting up a register in the hardware module*.

Id. ¶ 76 (emphasis added).

Towards the end of the written description in the '798 application, all of the previously-described embodiments are collectively characterized in terms that meet the negative limitation:

> As is described above with respect to the individual hardware accelerators of Figures 3 and 4, in one illustrative embodiment the programming for different decoding formats is done through register read/write. *The core processor programs registers in each module* to modify the operational behavior of the module.

Id. ¶ 83 (emphasis added). Hereafter we refer to these embodiments as the "register-based embodiments."

In contrast to these disclosures of register-based embodiments that meet the negative limitation, the '798 application closes with disclosure of a different alternative approach:

> In another illustrative embodiment, some or all of the hardware accelerators comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors, in addition to programming registers as appropriate to the design.

Id. ¶ 84. Hereafter we refer to this embodiment as the "software change" embodiment."

As elaborated below, we agree with Patent Owner that this statement, taken together with the disclosure as a whole, supports the negative limitation of proposed substitute claim 15.[24] Mot. Amend 6–7.

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[24] We agree with Petitioner that the other portions of the '798 application cited by Patent Owner in the Motion to Amend (Ex. 2008 ¶¶ 4, 5, 28) are less pertinent to this inquiry. *See* Opp. Amend 7–8. However, although support for a negative limitation does not require "articulating advantages or disadvantages" of a disclosed alternative (per *Inphi Corp.,* 805 F.3d at 1356), we note that these portions of the '798 application do in fact suggest to one of ordinary skill the speed advantages of hardware approaches that avoid "intervention from the main core processor." Ex. 2008 ¶ 28. This at least suggests that the register-based alternative has a speed advantage over the software change alternative.

In particular, one of ordinary skill would thus have understood that the inventors described two basic approaches: (i) the register-based embodiments, in which hardware accelerators were configured by the core processor writing control parameters to registers associated with the accelerator; and (ii) the software change embodiment, in which hardware accelerators were configured by the core processor by changing the software executed by those processors (with the possibility, but not the requirement, that registers would also be programmed.) Havlicek Decl. ¶¶ 38–40.

Petitioner disputes the above reasoning on several grounds, none of which are persuasive. First, Petitioner relies on its expert testimony to the effect that the '798 application "does not specify or explain how to implement the '844 patent's hardware accelerator without programmable processors." Bovik 2nd Decl. ¶ 39. However, this is not to the point — the negative limitation does not rule out hardware accelerators that use programmable processors — rather, it excludes accelerators that are configured *by changing the software* executed by those processors. As Petitioner admits: "The substitute claims do not exclude hardware accelerators that include processors. It excludes hardware accelerators that comprise 'programmable processors which are configured to operate to different encoding/decoding formats by changing the software executed by those processors.'" Sur-Reply Amend 10.

Indeed, four out of six of the above enumerated accelerators comprise programmable processors, but are configured by registers and thus are register-based embodiments which satisfy the negative limitation:

> [M]odules 310 and 312 [de-blocking filter; pixel filter] are implemented in the form of a filter engine 311 which consists

> of an internal SIMD (single instruction multiple data) processor. . . .

Ex. 2008 ¶ 31.

> [M]odule 314 [motion compensator] is implemented in the form of another filter engine similar to 311 which consists of an internal SIMD (single instruction multiple data) processor. . . .

Id.

> In an illustrative embodiment of the present invention, the PVLD [programmable entropy decoder] module 306 is designed as a coprocessor. . . .

Id. ¶ 32.

Although these hardware accelerators use programmable processors, they are configured by the core processor via programming registers, and there is no suggestion in the '798 application that the core processor also changes the software executed by those processors as part of configuration.[25]

Petitioner challenges the above reasoning, on the ground that merely stating that the accelerators are configured by programming registers does not rule out that they are *also* configured by changing the software executed by those processors. Sur-Reply Amend 2. We also made this point in the Preliminary Guidance. Paper 19, 7. However, on further consideration, we

[25] Some of Petitioner's arguments apparently assume that the negative limitation of proposed substitute claim 15 precludes all hardware accelerators that comprise programmable processors, even if only configured by the core processor via programming registers. *E.g.*, Sur-Reply 1. We conclude otherwise, but note that under Petitioner's narrower interpretation, two of the hardware accelerators disclosed in the '798 application are not implemented with programmable processors — *viz.*, inverse quantizer 308 and inverse transform module 309. Ex. 1001, 9:29–10:46. Thus, even under this interpretation, the '798 application discloses a "plurality" of hardware accelerators that satisfy the negative limitation of proposed substitute claim 15, as required.

are no longer of that view. As discussed above, after providing detailed disclosure of the register-based embodiments that are described solely in the context of configurability via register programming, the '798 application then follows with a separate disclosure of the software change embodiment in which "programmable processors which are configured . . . by changing the software executed by those processors, *in addition to programming registers as appropriate to the design.*" Ex. 2008, ¶ 84 (emphasis added). From this, we determine that one of ordinary skill, considering the '798 application as a whole, would have understood the description of register-based embodiments to consist of accelerators programmed only by registers, in contrast to the description of the software change embodiments, which are programmed *either* by changing software alone, *or* by a combination of register programming and software changes.[26] One of ordinary skill would have realized as a matter of straightforward logic that the inventors did not intend to include the possibility that the register-based embodiments would ***also*** include software changes, given that the software change embodiment already included the option of having *both* software changes *and* register programming.

Petitioner's expert Dr. Bovik argues that, given that the '798 application contemplates accommodating future video decoding standards, processors in the hardware accelerators of the invention would have to be reprogramed with modified software to handle the new techniques of those

[26] Petitioner also suggests that the changing register contents can result in changing software. Sur-Reply Amend 2. We are not persuaded by this unsupported attorney argument. We understand that the value of a register parameter may dictate which branch or module of software is executed, but that does not change the software that is programed in the processor.

standards. Bovik 2nd Decl. ¶ 39. But the negative limitation of proposed substitute claim 15 does not rule out reprogramming processors as part of a redesign to accommodate new standards. As discussed above in Section III.C.2, we construe claim 1 to require the hardware accelerator to be internally programmable *by the processor* of claim 1 (meaning the "core processor" as referred to in the'798 application (Ex. 2008, Fig. 3)). Therefore, the negative limitation of proposed substitute claim 15 only excludes changes to a hardware accelerator processor made by the processor of claim 1 — *i.e.*, during operation of the system. It is irrelevant to the claim whether or not a designer or some other agent reprograms the hardware accelerator processors, whether to accommodate new decoding standards or for some other reason.

Petitioner also argues that the '798 application does not provide sufficient detail on the structure and operation of the disclosed hardware accelerators, and in particular that the scope of proposed substitute claim 15 is not commensurate with the scope of the disclosure of the '798 application. Sur-Reply Amend 2–3 (citing *Centocor Ortho Biotech, Inc. v. Abbott Labs.*, 636 F.3d 1341, 1353 (Fed. Cir. 2011)). Petitioner points out that the scope of proposed substitute claim 15 encompasses embodiments in which *none* of the accelerators "comprise programmable processors which are configured . . . by changing the software executed by those processors" — *i.e.*, in which all of the accelerators satisfy the negative limitation. *Id.* at 2. Petitioner argues that the '798 application does not support an embodiment in which every accelerator meets this limitation. *Id.*

To the contrary, as discussed above, *all* of the accelerators of the register-based embodiments discussed above satisfy the negative limitation

of proposed substitute claim 15. The statement in paragraph 84 of the '798 application, that "some or all of the hardware accelerators" are configurable through software change, is the alternative to the register-based embodiments, in which none of the hardware accelerators are configurable through software change.

Moreover, Petitioner's reliance on *Centocor* is misplaced. That case involved a patent directed to pharmaceutical antibodies used to treat arthritis. 636 F.3d at 1343. The written description issue in that case concerned whether a parent patent, which disclosed partly human and partly mouse-based antibodies, provided adequate written description for claims directed to "fully-human" antibodies. *Id.* at 1343, 1347–48. In finding lack of written description support, the Court distinguished other cases that involved "well developed and mature" technologies. *Id.* at 1352. Indeed, "the level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology," and the requirements of detailed disclosure are "particularly acute in the biological arts." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351, 1353 (Fed. Cir. 2010). In contrast, when the field of the invention is a "predictable art," involving a mature technology such as electrical or mechanical arts, and where the knowledge and level of skill in the art is high, a lower level of detail is required to satisfy the written description requirement. *Hologic, Inc. v. Smith & Nephew, Inc.*, 884 F.3d 1357, 1361 (Fed. Cir. 2018).

We find that the level of ordinary skill in the art applicable to the subject matter of the proposed substitute claims is high, and the technology involved is mature and predictable. The art of record establishes that the

technology of hardware accelerators at the time of the '798 application was well established. *E.g.*, Exs. 1004, 1005, 1024, 1026. Patent Owner has met the predicate requirement of showing support in the original disclosure for those claims.

3. Responding to a Ground of Unpatentability

As stated in 37 C.F.R. § 42.121(a)(2)(i), "[a] motion to amend may be denied where . . . [t]he amendment does not respond to a ground of unpatentability involved in the trial." In considering the motion, the entirety of the record is reviewed to determine whether a patent owner's amendments respond to a ground of unpatentability involved in the trial.

Proposed substitute claim 15 amends claim 10 to add the above-discussed negative limitation, "wherein the plurality of hardware accelerators do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors" — the amendment is proposed in order to distinguish the claimed subject matter over Fandrianto '459. Mot. Amend 3. Indeed, as Petitioner concedes, Video Processor 280 of Fandrianto '459 does not satisfy this negative limitation, because it executes successive subroutines, as controlled by RISC processor 220, to perform different video decoding functions. Ex. 1004, Fig. 9, 12:48–13:5; Paper 33, 19:16–20. Patent Owner additionally argues that neither Huffman decoder 260 nor H.221/BCH decoder 240 of Fandrianto '459 is a claimed accelerator. Mot. Amend. 13–21. Although, as set forth in Sections III.D.2.c)(2) and (3), we are not persuaded by the latter arguments, Patent Owner's assertion of them together with the negative limitation of proposed

substitute claim 15 is responsive the Petitioner's reliance on Fandrianto '459 as a ground for invalidating claim 10.

Proposed substitute claim 16 depends from claim 15, amends original claim 11, and additionally requires that at least four of the specified accelerators satisfy the negative limitation of claim 15. Petitioner argues that proposed substitute claim 16 is not responsive to a ground of unpatentability because it is broader than original challenged claim 11. Opp. Amend 4–6. However because proposed substitute claim 16 depends from substitute claim 15, and thus requires at least four of the enumerated accelerators to comply with the negative limitation, it is narrower than original challenged claim 11, which does not require any of the accelerators to so comply.

The amendment thus addresses the invalidity ground raised in the Petition for claim 11, because, as set forth in Section III.E.2 above, the Video Processor 280 of Fandrianto '459, as further disclosed in Fandrianto '351, is asserted by Petitioner to teach all but one of the enumerated accelerators of original claim 11. With the addition of the negative limitation by virtue of dependency on proposed substitute claim 15, claim 16 is further distinguished from that combination, because at most only one accelerator of Fandrianto '459 (Huffman decoder 260) satisfies the negative limitation requirement. Accordingly, we determine that proposed substitute claim 16 responds to a ground of unpatentability.

Likewise, proposed substitute claims 17–19, by virtue of their dependency on proposed substitute claim 16, are responsive to a ground of patentability.

4. Not Enlarging the Scope of the Claims

As stated in 35 U.S.C. § 316(d)(3), an "amendment . . . may not enlarge the scope of the claims of the patent." *See also* 37 C.F.R. § 42.121(a)(2)(ii) ("A motion to amend may be denied where . . . [t]he amendment seeks to enlarge the scope of the claims of the patent."). "A new claim enlarges if it includes within its scope any subject matter that would not have infringed the original patent." *Thermalloy, Inc. v. Aavid Eng'g, Inc.*, 121 F.3d 691, 692 (Fed. Cir. 1997).

Proposed substitute claim 15 includes the narrowing negative limitation as compared to original claim 10. Mot. Amend Appx. 1. Petitioner does not contest that claim 15 narrows claim 10.

Petitioner argues that proposed "substitute claim 16 is nothing more than an attempt to broaden claim 11." Opp. Amend 4. However, as discussed above, claim 16 is narrower than claim 11 by virtue of its dependency on claim 15. Moreover, because original challenged claim 11 depends from, and is narrower than, claim 1, so is its substitute, claim 16. *See Lectrosonics*, IPR2018-01129, Paper 15, at 6–7 ("A substitute claim will meet the requirements of § 42.121(a)(2)(i) and (ii) if it narrows the scope of at least one claim of the patent . . . .").

5. Summary — Predicate Requirements

In sum, as set forth above, we determine that Patent Owner has met the predicate requirements for its Motion to Amend.

C. Indefiniteness

Petitioner asserts the recitation in proposed substitute claim 16, "wherein the hardware accelerators comprise at least four of," is indefinite pursuant to 35 U.S.C. § 112, 2nd paragraph, because it is open to multiple

interpretations that make the scope of the claim unclear. Opp. Amend 9. For example, argues Petitioner, the "at least four" requirement could be met by a system comprised of four programmable entropy decoders, or some other such combination, rather than one each of four of the five enumerated accelerators. *Id.* at 9–10.

"[A] patent is invalid for indefiniteness if its claims . . . fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014); *see also In re Packard*, 751 F.3d 1307, 1311 (Fed. Cir. 2014) (finding claims are properly rejected for indefiniteness when the USPTO makes unrebutted findings that claim language is "ambiguous, vague, incoherent, opaque, or otherwise unclear").

Upon review of the '844 patent as a whole, we conclude that one of ordinary skill in the pertinent art would understand that proposed substitute claim 16 requires the system to include, at a minimum, four out of the five different types of hardware accelerators recited — *i.e.*, "a programmable entropy decoder," "an inverse quantizer," "an inverse transform accelerator," "a pixel filter," and "a motion compensator" — to satisfy the negative limitation of proposed substitute claim 15. We agree with Patent Owner's expert that one of ordinary skill would not consider the other combinations imagined by Petitioner, to the extent they do not encompass this minimum requirement, as reasonably within the scope of the claim. Reply Amend 3–4 (citing Havlicek Decl. ¶ 41). For example, merely requiring multiple instances of any one accelerator is inconsistent with the fact that the claim is directed to a "video decoding system," as opposed to arbitrary aggregations of individual hardware accelerators. Mot. Amend Appx. 1.

D. Ground 1: Obviousness of Proposed Substitute Claim 15

Petitioner argues, as Ground 1, that substitute claim 15 would have been obvious in light of Fandrianto '459, Kopet, and Malladi. Opp. Amend 12–19. Petitioner actually makes two separate arguments under this ground: that proposed substitute claim 15 would have been obvious in light of Fandrianto '459 alone (*id.* at 12–14), and that would have been obvious over the combination of Fandrianto '459, Kopet, and Malladi (*id.* at 14–19).

1. Obviousness of Proposed Substitute Claim 15 Over Fandrianto '459 Alone

Petitioner relies on its proofs set forth in the Petition to demonstrate that Fandrianto '459 teaches the limitations of claims 1 and 9, from which proposed substitute claim 15 depends, and of claim 10, which recites the requirements of claim 15 other than the negative limitation added by amendment. Opp. Amend 12. For the negative limitation of claim 15, which requires a plurality of hardware accelerators that "do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors," Petitioner relies on the H.221/BCH decoder 240 and Huffman decoder 260 of Fandrianto '459. *Id.* at 12–13. Petitioner's expert Dr. Bovik testifies that these accelerators do not comprise programmable processors that are configured to operate by changing their executed software. Bovik 2nd Decl. ¶¶ 95–98, 102–104.

As discussed above in Sections III.D.2.c)(2) and (3), Patent Owner argues that neither H.221/BCH decoder 240 nor Huffman decoder 260 satisfy the claim requirements of original claim 1. *See* Mot. Amend 13–21; Reply Amend 4–5. For the reasons set forth in those sections, we do not find those arguments supported by the preponderance of the evidence.

Patent Owner does not otherwise dispute that H.221/BCH decoder 240 and Huffman decoder 260 meet the additional requirements of claim 9 and proposed substitute claim 15, including satisfying the negative limitation — it being undisputed that those components are not programmable processors. *See* Mot. Amend 12–21; Reply Amend 4–5.

Accordingly, we determine that Petitioner has proved by a preponderance of the evidence that proposed substitute claim 15 would have been obvious in light of Fandrianto '459. Therefore, the Motion to Amend is denied as to proposed substitute claim 15.

2. Obviousness of Proposed Substitute Claim 15 Over Fandrianto '459, Kopet, and Malladi

Because we determine that proposed substitute claim 15 would have been obvious in light of Fandrianto '459 alone, our evaluation of Petitioner's alternative reliance on the combination of Fandrianto '459, Kopet, and Malladi is not required for our denial of the Motion to Amend as to substitute claim 15. However, Petitioner also relies on the combination of Fandrianto '459, Kopet, and Malladi (as well as additional references) in opposing the Motion to Amend as to proposed substitute claims 16–19. Opp. Amend 19–31. Therefore, we discuss the merits of Petitioner's alternative argument below.

a) Kopet

Kopet, titled "Image Compression Coprocessor With Data Flow Control and Multiple Processing Units," issued December 16, 1997. Ex. 1024, codes [54], [45]. Because Kopet issued more than one year before the filing date of the application for the '844 patent, this reference is prior art to the '844 patent under pre-AIA 35 U.S.C. § 102(b).

Kopet describes a system that compresses or decompresses image data in accord with the JPEG, H.261, and MPEG standards. *Id.* at Fig. 2, 4:58–62, 7:5–7, 14:45–48. Kopet describes an image compression/decompression coprocessor integrated on a single chip that includes different, special purpose processing units each designed to handle only certain steps in the compression and decompression processes. *Id.* at Abstr. Figure 4 of Kopet is reproduced below.

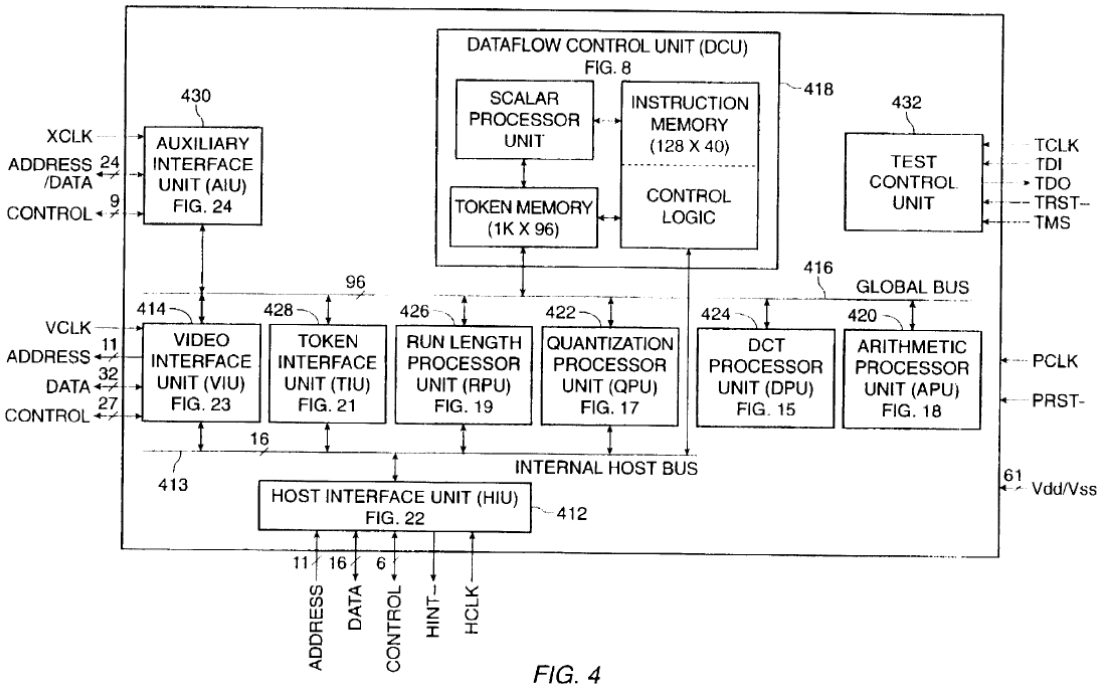

FIG. 4

Figure 4 is a block diagram of Image Compression Coprocessor (ICC) 410, which "performs all video compression functions in a typical system except motion estimation, Huffman encoding and decoding, and bit stream management." *Id.* at 4:9–10, 5:3–6. ICC 410 includes a Dataflow Control Unit (DCU) 418, which is a "standard microprogrammed control unit of the type in a standard microprocessor" controlling the operation of ICC 410. *Id.* at 8:29–30, 9:6–8. DCU 418 is connected by an internal, global bus to various processing units, including Auxiliary Interface Unit (AIU) 430, Run

Length Processor Unit (RPU) 426, Quantization Processor Unit (QPU) 422, DCT Processor Unit (DPU) 424, and Arithmetic Processor Unit (APU) 420. *Id.* at Fig. 4, 3:20–24, 3:40–42, 8:33–45. In particular, DPU 424 executes forward and inverse DCTs (Discrete Cosine Transforms), QPU 422 performs forward and inverse quantization, and APU 420 performs loop filter calculations. *Id.* at 1:58–59, 6:49–52, 33:5–7. These processing units can either be identical in hardware, with custom programming, or specialized in hardware. *Id.* at 8:37–39.

The motion estimation function is performed by a separate motion estimation coprocessor, MEC 212. *Id.* at 4:62, 5:7–8. ICC 410 and MEC 212 are supported by a RISC host processor, which also handles Huffman encoding and decoding and bit stream management. *Id.* at Fig. 2, 4:67–5:7.

In operation, ICC 410 operates as a "slave" to the RISC host microprocessor, with the host programming the software into DCU 418 of ICC 410 for the particular type of compression or decompression required. *Id.* at 8:46–50, 15:2–6. DCU 418 then operates ICC 410 under control of that program to perform the compression or decompression according to the program, with the different steps in the particular compression or decompression algorithm performed by the appropriate processing units of ICC 410 — *e.g.*, QPU 422, DPU 424, or APU 420. *Id.* at 8:50–55. The program loaded into ICC 410 by the host processor consists of a series of "ICC instructions," with specific instructions designated for controlling each of the processing units. *Id.* at Table 3, 12:30–14:27, 16:9–11, 16:30–36. For example, "IQUANT" commands QPU 422 to perform inverse quantization; "IDCT" commands DPU 424 to perform inverse DCT; and

"FILTER" commands APU 420 to perform loop filtering. *Id.* at 12:50 ("FILTER" command), 12:52 ("IDCT" command), 12:64 ("IQUANT" command). When the host processor loads the program into ICC 410, parameters in the commands specify whether the compression or decompression is performed in accord with the JPEG, H.261, or MPEG standards (if the particular command is standard dependent). *E.g.*, *id.* at Fig. 9, Appx. 1, col. 40 ("Each instruction description begins with the instruction's Opcode mnemonic (in bold caps) and list of applicable parameters (in italics)").

Like the illustrative embodiment of the '844 patent, ICC 410 uses a pipelined process, in which each processing unit (such as QPU 422, DPU 424, and APU 420) performs its respective step of the compression or decompression algorithm in parallel on successive "tokens" of image data (such as macroblocks). *Id.* at 3:40–44, 6:31–34, 8:21, 8:53–56, 9:48–50, 9:58–61, 14:42–44. DCU 418 schedules the token traffic between the various processing units in accord with this pipelining process. *Id.* at 15:30–31.

b) Malladi

Malladi, titled "Method For Partitioning Hardware And Firmware Tasks In Digital Audio/Video Decoding," issued September 29, 1998. Ex. 1025, codes [54], [45]. Because Malladi issued more than one year before the filing date of the application for the '844 patent, this reference is prior art to the '844 patent under pre-AIA 35 U.S.C. § 102(b).

Malladi discloses a partitioning procedure for designing MPEG decoders, AC-3 decoders, and decoders for other audio/video standards, including partitioning between decoding functionality implemented in

hardware and functionality implemented in firmware or software. *Id.* at Abstr. Malladi provides for headers in blocks of data that include parameters that control the decoding process. *Id.* at Fig. 1B, 7:63–8:53.

c) The Combination of Fandrianto '459, Kopet, and Malladi as Applied to Proposed Substitute Claim 15

(1) Petitioner's Arguments

Relying on Figure 4 of Kopet, Petitioner argues that "Kopet discloses a video encoder/decoder architecture that is identical to the '844 patent, and uses 'hardware based' accelerators to decode video data." Opp. Amend 15. In particular, Petitioner identifies DCU 418 as a "processor" and the various processing units (also referred to as "functional units"), including AIU 430, RPU 426, QPU 422, DPU 424, and APU 420, as "accelerators." *Id.* at 15–16. Petitioner asserts that the processing units "can adapt to different encoding/decoding formats without changing software executed by a processor," and relies on a statement in Kopet that those units can be "***specialized in hardware***." *Id.* at 16 (citing Bovik 2nd Decl. ¶¶ 107–110; Ex. 1024, 8:33–39). Petitioner's expert, using processing unit QPU 42 as an example, testifies that, rather than changing the software of QPU 422, "control unit DCU 418 internally programs how QPU 422 operates by sending [a] control/instruction token to QPU 422." Bovik 2nd Decl. ¶ 109.[27]

[27] In their description of how DCU 418 controls the operation QPU 422 and the other processing units, Petitioner and its expert confuse "tokens" with "instructions," as those terms are used in Kopet. *See* Bovik 2nd Decl. ¶¶ 113–116. DCU 418 sends *instructions* to the processing units to cause them to perform their compression or decompression functions. Ex. 1024, Fig. 9, 12:30–14:60. DCU 418 controls the flow of *tokens*, which contain the image data being compressed or decompressed, between the processing units as the compression or decompression process takes place. *Id.* at Fig. 7,

Petitioner further argues that it would have been obvious, in view of Kopet, to substitute Fandrianto '459's video processor 280, which executes software to implement multiple decoding functions, with multiple separate hardware accelerators that are not programmable processors. Opp. Amend 17 (citing Bovik 2nd Decl. ¶ 111). Petitioner argues that a person of ordinary skill would have been motivated to make this modification because Fandrianto '459 and Kopet "describe similar decoding system architectures," and the Kopet approach would improve the speed of decoding, because a dedicated hardware approach is faster than a software-based approach. *Id.* at 17 (citing Bovik 2nd Decl. ¶¶ 78–81, 112; Ex. 1024, 2:38–59).

Petitioner additionally relies on Malladi "to the extent that Kopet does not explicitly disclose how its control unit 418 would generate control tokens with the parameters that the accelerators use to change its decoding method." Opp. Amend 18. Petitioner argues that it would have been obvious to one of ordinary skill to incorporate into Kopet the parsing and decoding of video stream headers disclosed in Malladi to generate control tokens.[28] *Id.* at 18–19 (citing Bovik 2nd Decl. ¶¶ 92, 117–119).

9:48–12:29. Thus, the instructions determine how the processing units process the tokens.

[28] "Control tokens" in Kopet are:

> [U]sed to convey boolean and/or numeric scalar data between instructions. Common usages of control tokens include the holding of memory addresses for video memory read instructions and the holding of boolean data which are used to gate program dataflow.

Ex. 1024, 10:47–51. As discussed in the previous footnote, Petitioner confuses tokens with instructions.

(2) Patent Owner's Reply

Patent Owner argues that Petitioner has not established that one of ordinary skill would have been motivated to combine Fandrianto '459 with Kopet, because the proposed combination would "not necessarily result in a faster decoding system." Reply Amend 10. Patent Owner points out that the support provided by Petitioner consists of statements in the background section of Kopet that programming a general microprocessor to perform compression and decompression is a slower approach than using dedicated hardware. *Id.* at 9 (citing Ex. 1024, 2:38–59; Bovik 2nd Decl. ¶¶ 79–80). However, argues Patent Owner, this background discussion in Kopet is irrelevant to the motivation issue because "neither of these two historical ways of decoding are performed by Fandrianto or the proposed combination of Fandrianto with Kopet." *Id.* at 9–10 (citing Havlicek Decl. ¶ 61). Patent Owner relies on its expert's testimony that one of ordinary skill "would not necessarily expect that replacing Fandrianto's video processor 280 with Kopet's ICC would increase the speed of the decoding process because such a modification would replace Fandrianto's video processor with another processor, Kopet's DCU, and add additional hardware." Havlicek Decl. ¶ 62. Patent Owner also challenges Petitioner's proposed combination as lacking a showing that one of ordinary skill would have had a reasonable expectation of success in making the combination. Reply Amend 10–11.

Aside from motivation to combine, Patent Owner argues that Petitioner's obviousness argument is flawed because it offers conflicting versions of the combination it relies on: replacing Fandrianto '459's video processor 280 with the entirety of Kopet's ICC 410, which includes the DCU 418 processor as well as the processing units (AIU 430, RPU 426,

QPU 422, DPU 424, and APU 420), *versus* only replacing video processor 280 with the processing units. Reply Amend 7–9 (*comparing* Opp. Amend 13, 29 (relying on Fandrianto '459's RISC processor 220 as the processor), *with* Opp. Amend 17 (relying on Kopet's DCU 418 as the processor)); Havlicek Decl. ¶¶ 55–56. Patent Owner argues that this conflict establishes that Petitioner has not demonstrated that either video processor 280 or DCU 418 satisfies the requirements of the processor of claim 1 and proposed substitute claim 15. Reply Amend, 8–9 (citing Havlicek Decl. ¶¶ 57–58).

In addition to challenging whether Petitioner's proposed combination meets the processor requirement of the claims, Patent Owner also challenges whether the accelerator requirements of claim 1, which are incorporated in proposed substitute claim 15, are satisfied. *Id.* at 6–7. Patent Owner argues that Petitioner has made no showing that the processing units of Kopet, which under any version of Petitioner's proposed combination would allegedly serve as the claimed accelerators, are "adapted to perform a decoding function on a digital media data stream," are "internally programmable by the processor," or "configurable to perform the decoding function according to a plurality of decoding methods," as required by claim 1, and as construed in Section III.C.2 above, and thus also required by dependent proposed substitute claim 15. *Id.* at 6. In particular, Patent Owner argues that RPU 426 and AIU 430 do not perform any decoding function, and APU 420 and DPU 424 do not perform their decoding function according to a plurality of decoding methods because APU 420 only performs filtering for the H.261 standard, and DPU 424 performs inverse DCT operations the same way for each of the standards it accommodates. *Id.* at 6–7 (citing Havlicek Decl. ¶¶ 51–53). Patent Owner does not address

QPU 422 of Kopet, and so, even assuming that processing unit is an accelerator that decodes according to a plurality of decoding methods, proposed substitute claim 15 requires a plurality of such accelerators. *Id.* at 5–7.

(3) Petitioner's Sur-Reply

Petitioner responds that Patent Owner mischaracterizes Petitioner's proposed combination, and that Petitioner does not argue that the entirety of Kopet's ICC 410, including DPU 418, would have been incorporated into Fandrianto '459, but rather Kopet and Malladi would have taught or suggested "implementing Video Processor 280 of Fandrianto as a plurality of hardware accelerators that do not include 'programmable processors.'" Sur-Reply Amend 5 (citing *Allied Erecting and Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) ("The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, but rather whether 'a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention'")).

Petitioner also argues that it has met the proposed substitute claim 15 requirement of a *plurality* of accelerators given Huffman decoder 268 and H.221/BCH decoder 240 of Fandrianto '459, and given the processing units of Kopet. Sur-Reply Amend 6–7.

(4) Analysis

As set forth in Section IV.D.1 above, we agree with Petitioner that Huffman decoder 268 and H.221/BCH decoder 240 of Fandrianto '459 satisfy the claim requirements for accelerators, and therefore Petitioner has proved by a preponderance of the evidence that substitute claim 15 would

have been obvious in light of Fandrianto '459 alone. However, we agree with Patent Owner that Petitioner has not sufficiently demonstrated that one of ordinary skill would have been motivated to replace Fandrianto '459's video processor 280 with separate the processing units of Kopet. Nor, with the possible exception of QPU 422, do we agree that the Kopet processing units would satisfy the accelerator requirements of proposed substitute claim 15 even if Fandrianto '459 were to be modified as Petitioner proposes.

We agree with Patent Owner that Petitioner has not sufficiently established that there would have been a motivating speed advantage that would have suggested replacing Fandrianto's video processor 280 with Kopet's processing units. The statement in Kopet that Petitioner relies on, which explains that a dedicated hardware approach is faster than a software-based approach, is comparing two "historical[]" techniques, neither of which corresponds to the approaches in Fandrianto '459 or Kopet. Ex. 1024, 2:38–48; Opp. Amend 17; Bovik 2nd Decl. ¶¶ 79–80; Reply Amend 9–10; Havlicek Decl. ¶¶ 59–61. Comparing Fandrianto '459 with Kopet does not present the speed difference of software-based approach versus dedicated hardware approach as Petitioner would have it. Rather, both references adopt a similar balance between the use of software and hardware, and we agree with Patent Owner's expert that the record does not establish that one of ordinary skill would have perceived a speed advantage in adapting Fandrianto '459 to the Kopet approach. Havlicek Decl. ¶ 62.

In particular, Fandrianto '459 discloses that RISC microprocessor 220 programs video processor 280 to perform its video compression or decompression steps in accord with a particular video standard. Ex. 1004, 5:14–15, 12:48–13:11. Once programmed, video processor 280 receives

commands from RISC microprocessor 220 to successively perform the various subroutines corresponding to the decoding steps of the particular video standard. *Id.* at 13:2–11. Video processor 280 has its own Command Processor 960 which executes the programmed subroutines, making use of dedicated hardware such as an arithmetic logic unit, adders, multipliers, and registers. *Id.* at Fig. 9, 13:5–24.

Similarly, Kopet discloses that a RISC host microprocessor programs Dataflow Control Unit (DCU) 418 of Image Compression Coprocessor (ICC) 410 to perform its video compression or decompression steps in accord with a particular video standard. Ex. 1024, 8:46–50, 15:2–6. ICC 410 is a standard microprocessor that, in accord with how it is programmed, issues instructions to the processing units, such as QPU 422, DPU 424, or APU 420, which perform the various decoding steps of the particular video standard. *Id.* at Table 3, 8:50–55, 12:30–14:27, 16:9–11, 16:30–36. In turn, the processing units each have their own programmed processor that carries out a processing step according to the instruction sent to it. *Id.* at Figs. 15 ("DCT Processor" 1514), 17 ("Q Processor" 1714), 18 ("Filter/Arithmetic Processor" 1820), 30:48–64, 32:17–43, 32:65–33:9.

Thus, the conclusory testimony of Petitioner's expert concerning motivation to combine Fandrianto '459 with Kopet is unpersuasive in the face of this record, which suggests, if anything, that there is greater use of processors, and thus more processing delays, in Kopet than in Fandrianto '459 — the former having three levels of processors (RISC host, DCU 418, processing units) versus the latter having two levels (RISC microprocessor 220, Command Processor 960). Havlicek Decl. ¶ 62. Accordingly, we find that Petitioner has not established sufficiently that a

person of ordinary skill in the art would have been motivated to combine the teachings of Fandrianto '459 and Kopet to achieve the invention of claim 15.

Moreover, even if one of ordinary skill were motivated to modify Fandrianto '459 in light of Kopet, the addition of the processing units of Kopet would not result in a plurality of accelerators as required by proposed substitute claim 15 (beyond the already-included Huffman decoder 268 and H.221/BCH decoder 240 of Fandrianto '459). Sur-Reply Amend 5. We agree with Patent Owner that Petitioner has not shown that the Kopet processing units included in such a combination (possibly excepting QPU 422) would satisfy the limitations of claim 1, which are also limitations of proposed substitute claim 15 by dependency. Reply Amend 6–7; Havlicek Decl. ¶ 49. We discuss our analysis of this issue in connection with proposed substitute claim 16, below. Thus, setting aside the H.221/BCH decoder 240 and Huffman decoder 260 of Fandrianto '459, discussed in Section IV.D.1 above, the record supports at most only one processing unit of Kopet — QPU 422 — qualifying as a claimed accelerator of proposed substitute claim 15, whereas, as Patent Owner points out, claim 15 requires a plurality of such accelerators. Reply Amend 5.

As noted above, Petitioner additionally relies on Malladi as teaching modification of Kopet to parse and decode video stream headers to generate control tokens. Opp. Amend 18 (citing Bovik 2nd Decl. ¶¶ 92, 117–119). However, control tokens do not command the operations of the processing units. Ex. 1024, 10:47–51. As discussed above, the host processor of Kopet programs control unit 418 to compress or decompress image data in accord with a particular standard, and control unit 418 issues instructions to the processing units accordingly. We are not persuaded that one of ordinary

skill would have been motivated to bypass or substantially alter this approach by incorporating the techniques of Malladi.

In sum, we determine that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claim 15 would have been obvious over Petitioner's proposed combination of Fandrianto '459, Kopet, and Malladi. Nonetheless, because we determine that Petitioner has proved by a preponderance of the evidence that proposed substitute claim 15 would have been obvious in light of Fandrianto '459 alone, we deny the Motion to Amend as to proposed substitute claim 15.

E. Ground 2: Obviousness of Proposed Substitute Claims 16–18 Over Fandrianto '459, Kopet, Malladi, and Wise

Petitioner argues, as Ground 2, that proposed substitute claims 16–18 would have been obvious in light of Fandrianto '459, Kopet, Malladi, and Wise. Opp. Amend 19–29. As discussed above, we determine that Petitioner has not established sufficiently that a person of ordinary skill in the art would have been motivated to combine the teachings of Fandrianto '459, Kopet, and Malladi to achieve the invention of proposed substitute claim 15, from which proposed substitute claim 16 depends. Nonetheless, below, we consider Petitioner's arguments regarding claim 16 based on the addition of Wise as part of the combination relied on.

1. Wise

Wise, titled "Multistandard Video Decoder And Decompression Method For Processing Encoded Bit Streams According To Respective Different Standards," was filed February 7, 2001, and claims priority to U.S. Application No. 08/082,291, filed June 24, 1993. Ex. 1026, codes [54], [62]. Petitioner argues this priority date is more than one year before the '844 patent's earliest possible effective filing date and thus Wise qualifies as prior

art under pre-AIA 35 U.S.C. § 102(e). Opp. Amend 12. Patent Owner does not dispute the prior art status of Wise, and we treat it as such.

Wise discloses a pipelined video decoder and decompression system employing a series of interconnected stages to decode and decompress a serial video bit stream. *Id.* at Abstr. The system can be configured to process data in accordance with "JPEG, MPEG, and/or H.261, or any other standards and any combination of such picture standards. . . ." *Id.* at 11:38–45. Among the decoding stages is a Temporal Decoder to handle motion compensation, a Huffman decoder to handle entropy decoding, an inverse quantizer, an inverse discrete cosine transformer, and a prediction filter to perform pixel filtering. *Id.* at Figs. 11, 12, 51:18–26, 52:32–46, 62:9–14, 82:64–83:19, 282:65–283:30.

2. Claim 16

Claim 16 requires:

> The video decoding system of claim 15 wherein the plurality of hardware accelerators comprise at least four of:
>
> a programmable entropy decoder adapted to perform entropy decoding on the data stream;
>
> an inverse quantizer adapted to perform inverse quantization on the data stream;
>
> an inverse transform accelerator adapted to perform inverse transform operations on the data stream;
>
> a pixel filter adapted to perform pixel filtering on the data stream; and
>
> a motion compensator adapted to perform motion compensation on the data stream.

Mot. Amend Appx. 1–2.

As discussed in Section IV.D.1 above, Huffman decoder 260 of Fandrianto '459 is an accelerator that satisfies the requirements of proposed substitute claim 15, and thus also satisfies the programmable entropy decoder element of proposed substitute claim 16. Petitioner offers an alternative argument that it would have been obvious to incorporate the Huffman decoder of Wise into the combination of Fandrianto '459 and Kopet discussed above with respect to proposed substitute claim 15. *Id.* at 21 (citing Bovik 2nd Decl. ¶¶ 129–130). Because we have determined that Fandrianto '459 alone teaches the programmable entropy decoder element of proposed substitute claim 16, there is no need to analyze this alternative argument, other than to observe that, because the Kopet RISC host processor already handles Huffman decoding, Petitioner does not establish, by a preponderance of the evidence, that the person of ordinary skill would have been motivated to incorporate the Huffman decoder of Wise. Ex. 1024, 5:4–7.

Petitioner relies on Quantization Processor Unit (QPU) 422 for the inverse quantizer requirement of claim 16. Opp. Amend 22. Petitioner argues that QPU 422 is configurable because "processing control tokens received from the control unit, DCU 418 . . . may include a field that specif[ies] quantization parameters specific to different compression algorithms such as MPEG and Px64 quantization algorithms." *Id.* (citing Bovik 2nd Decl. ¶¶ 108–109, 132–133). Petitioner also argues that, in light of Malladi, it would have been obvious to use the processor of the control unit in Kopet to decode headers in the video data to extract the required information for the control tokens. *Id.* (citing Bovik 2nd Decl. ¶¶ 134–137). Patent Owner does not challenge Petitioner's argument that QPU 422 is

configurable as required by claim 16. However, because we have determined that Petitioner has not established motivation to combine Fandrianto '459, Kopet, and Malladi, the fact that QPU 422 is arguably configurable is not sufficient to satisfy the inverse quantizer requirement of claim 16.

For the inverse transform accelerator requirement of proposed substitute claim 16, Petitioner concedes that Kopet does not explicitly disclose that its DCT unit 424 is configurable to perform inverse transform operations according to multiple decoding methods, but argues that it would have been obvious to one of ordinary skill that it would be adapted to do so. Opp. Amend 23–24 (citing Bovik 2nd Decl. ¶¶ 138–143).

For the pixel filter requirement of proposed substitute claim 16, Petitioner argues that it would have been obvious to replace Fandrianto '459's video processor 280 with a prediction filter such as that disclosed in Wise. Opp. Amend 24–25 (citing Bovik 2nd Decl. ¶¶ 144–145).

For the motion compensator requirement of proposed substitute claim 16, Petitioner argues that it would have been obvious to replace Fandrianto '459's video processor 280 with the motion estimation coprocessor (MEC 212) disclosed in Kopet, or the temporal decoder disclosed in Wise. Opp. Amend 25–26 (citing Bovik 2nd Decl. ¶¶ 146–148).

As to the inverse transform accelerator, pixel filter, and motion compensator requirements of proposed substitute claim 16, Patent Owner argues that no combination of Fandrianto '459, Kopet, Malladi, and Wise teaches or suggests the claimed *configurable* accelerators that perform these functions. Reply Amend 12–14 (citing Havlicek Decl. ¶¶ 67–70). Patent Owner also argues that half pel or integer pel interpolation, performed by

Wise's prediction filter 103, is not pixel filtering. *Id.* at 13 (citing Havlicek Decl. ¶ 69).

Because we have determined that Petitioner has not established motivation to combine Fandrianto '459, Kopet, and Malladi, for the same reasons we further determine that Petitioner has not established motivation to combine Fandrianto '459, Kopet, Malladi, and Wise. Petitioner cites nothing disclosed or taught in Wise that would alter our analysis in regard to motivation to combine Fandrianto '459 with Kopet, or to combine Fandrianto '459 with Kopet and Malladi. For this reason, Petitioner has not proved by a preponderance of the evidence that the combination of Fandrianto '459, Kopet, Malladi, and Wise would have taught or suggested the inverse transform, pixel filtering, or motion compensation requirements of claim 16.

In addition, we agree with Patent Owner that Petitioner has not established by a preponderance of the evidence that the combination of Fandrianto '459, Kopet, Malladi, and Wise, even if made, would have taught or suggested to one of ordinary skill implementing accelerators in the combination to perform the inverse transform, pixel filtering, or motion compensation requirements of proposed substitute claim 16. In particular, claim 1, from which proposed substitute claim 16 ultimately depends, as construed in Section III.C.2 above, requires the accelerator to be "internally programmable by the processor to perform its decoding function according to a plurality of decoding methods."

For the inverse transform requirement of proposed substitute claim 16, Petitioner's expert asserts that it was well known that different video standards have different mathematical algorithms for inverse transforms, and

one of ordinary skill would have been motivated to modify the DCT Processor Unit (DPU) 424 of Kopet to be configurable to accommodate the additional video standards that were introduced after Kopet's filing date. Bovik 2nd Decl. ¶¶ 138–148. However, this conclusory testimony is unpersuasive. Havlicek Decl. ¶¶ 67–68. To the extent one of ordinary skill would have modified the approach of Kopet to implement inverse transform algorithms of video standards beyond JPEG, H.261, and MPEG (the only standards mentioned in Kopet), the record does not support the assertion that the Kopet processing units would be modified so as to be configurable by a separate processor, as required by claim 1 (and thus by proposed substitute claim 16). As discussed in Section IV.D.2.c)(4) above, in Kopet a RISC host microprocessor programs Dataflow Control Unit (DCU) 418 of Image Compression Coprocessor (ICC) 410 to perform its video compression or decompression steps in accord with a particular video standard. Ex. 1024, 8:46–50, 15:2–6. For inverse transforms, ICC 410 issues instructions to DPU 424, which performs the inverse transform operation. *Id.* at Table 3, 8:50–55, 12:30–14:27, 16:9–11, 16:30–36. ICC 410 has its own preprogrammed processor — DCT Processor 1514 —that performs inverse transforms according to the instructions sent to it. *Id.* at Fig. 15, 30:48–64. DPU 424 is not configurable — it is preprogrammed to simply function according to the instructions it receives. *Id.* To the extent one of ordinary skill would have been motivated to adapt Kopet to handle inverse transforms of new video decompression standards developed after the filing date of Kopet, the teachings of Kopet would point towards *the designer of the system* modifying the programming of DCT Processor 1514, and the

instructions it receives, as required — rather than being configured on-the-fly by a separate processor during operation of the system. *Id.*

In addition, as to the pixel filter requirement of proposed substitute claim 16, we are not persuaded that it would have been obvious to replace Fandrianto '459's video processor 280 with a prediction filter such as that disclosed in Wise. Opp. Amend 24–25 (citing Bovik 2nd Decl. ¶¶ 144–145). Petitioner provides only conclusory testimony regarding this asserted substitution, and the record does not provide any persuasive reason why this modification would be made, or how Fandrianto '459 would have been modified to incorporate the Wise prediction filter. *Id.* In particular, there is no evidence that such a modification would include a provision for configurability of such a prediction filter by Fandrianto '459's RISC Microprocessor 220, or any other processor. Reply Amend 6; Havlicek Decl. ¶¶ 49, 69.

For the motion compensator requirement of proposed substitute claim 16, the record does not support replacing Fandrianto '459's video processor 280 with the motion estimation coprocessor (MEC 212) disclosed in Kopet, or the temporal decoder disclosed in Wise. Opp. Amend 25–26 (citing Bovik 2nd Decl. ¶¶ 146–148). Petitioner has not explained how MEC 212 of Kopet or the temporal decoder of Wise would satisfy the limitations of proposed substitute claim 16. Havlicek Decl. ¶ 70.

In sum, we determine that Petitioner has not proved by a preponderance of the evidence that the subject matter of substitute claim 16 would have been obvious over the combination of Fandrianto '459, Kopet, Malladi, and Wise.

3. Proposed Substitute Claims 17 and 18

Because we have determined that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claim 16 would have been obvious over the combination of Fandrianto '459, Kopet, Malladi, and Wise, and because proposed substitute claims 17 and 18 depend from claim 16, we also determine that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claims 17 and 18 would have been obvious over the combination of Fandrianto '459, Kopet, Malladi, and Wise.

F. Ground 3: Obviousness of Proposed Substitute Claim 19 Over Fandrianto '459, Kopet, Malladi, Wise, and Harrand

As discussed above, we have determined that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claim 16 would have been obvious over the combination of Fandrianto '459, Kopet, Malladi, and Wise. For Ground 3, Petitioner argues that proposed substitute claim 19 would have been obvious in light of Fandrianto '459, Kopet, Malladi, Wise, and Harrand. Opp. Amend 29–31. Petitioner relies on the additional reference, Harrand, for the teaching of readable status registers, as discussed in Section III.F above. Petitioner's arguments concerning Harrand do not alter our analysis with respect to the failure of the record to establish motivation to combine Fandrianto '459 with Kopet, or with Kopet and Malladi. Therefore, because proposed substitute claim 19 depends from proposed substitute claim 16, we also determine that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claim 19 would have been obvious over the combination of Fandrianto '459, Kopet, Malladi, Wise, and Harrand.

G. Ground 4: Obviousness of Claim 15 Over Kopet, and Malladi

Petitioner argues, as Ground 4, that proposed substitute claim 15 would have been obvious in light of Kopet and Malladi. Opp. Amend 31–32. For the requirement of proposed substitute claim 15 of a plurality of hardware accelerators that "do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors," Petitioner relies on the processing units of Kopet. *Id.* However, as discussed above, at most Kopet discloses only one processing unit — DCU 418 — that is configurable as required by claim 1 and also satisfies the negative limitation of proposed substitute claim 15. Reply Amend. 16–17. Accordingly, we determine that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claim 15 would have been obvious over the combination of Kopet and Malladi.

H. Ground 5: Obviousness of Proposed Substitute Claims 16–18 Over Kopet, Malladi, and Wise; and Ground 6: Obviousness of Proposed Substitute Claim 19 Over Kopet, Malladi, Wise, and Harrand

Petitioner argues, as Ground 5, that proposed substitute claims 16–18 would have been obvious in light of Kopet, Malladi, and Wise, and as Ground 6, proposed substitute claim 19 would have been obvious in light of Kopet, Malladi, Wise, and Harrand. Opp. Amend 32–35.

Petitioner's arguments for these grounds are essentially similar to those of Grounds 2 and 3, discussed above, and to that extent are unpersuasive for the reasons stated above. In addition, instead of relying on the Huffman decoder 260 of Fandrianto '459, Petitioner argues that the Huffman decoder of Wise would have been incorporated into the Kopet

system. *Id.* at 33. This argument is unpersuasive because the Kopet RISC host processor already handles Huffman decoding. Ex. 1024, 5:4–7.

Accordingly, we determine that Petitioner has not proved by a preponderance of the evidence that the subject matter of proposed substitute claims 16–18 would have been obvious over the combination of Kopet, Malladi, and Wise, or that the subject matter of proposed substitute claim 19 would have been obvious over the combination of Kopet, Malladi, Wise, and Harrand.

I. Summary — Invalidity Grounds

As stated above, we have determined that Petitioner has proved by a preponderance of the evidence that proposed substitute claim 15 would have been obvious in light of Fandrianto '459 alone. Therefore, the Motion to Amend is denied as to proposed substitute claim 15.

In addition, we have determined that Petitioner has not proved by a preponderance of the evidence that proposed substitute claims 16–19 would have been obvious under any of its Grounds 2, 3, 5, or 6, and therefore the Motion to Amend is granted as to proposed substitute claims 16–19.

V. CONCLUSION[29]

In summary:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 9, 10	103(a)	Fandrianto '459	1, 9, 10	
11–13	103(a)	Fandrianto '459, Fandrianto '351, Reader[30]	11–13	
14	103(a)	Fandrianto '459, Fandrianto '351, Reader,[30] Harrand	14	
Overall Outcome			1, 9–14	

Motion to Amend Outcome	Claim(s)
Original Claims Cancelled by Amendment	
Substitute Claims Proposed in the Amendment	15–19
Substitute Claims: Motion to Amend Granted	16–19
Substitute Claims: Motion to Amend Denied	15
Substitute Claims: Not Reached	

[29] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[30] As explained above, we do not consider Reader in our Decision.

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 9–14 of the '844 patent are unpatentable; and

FURTHER ORDERED that Patent Owner's Motion to Amend is denied as to proposed substitute claim 15 and granted as to proposed substitute claims 16–19;

FURTHER ORDERED that, because this is a Final Written Decision, any party to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Paper 41
Entered: April 15, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION,
Petitioner,

v.

BROADCOM CORPORATION,
Patent Owner.

Case IPR2019-01040
Patent 8,284,844 B2

Before THOMAS L. GIANNETTI, PATRICK M. BOUCHER, and NORMAN H. BEAMER, *Administrative Patent Judges*.

BEAMER, *Administrative Patent Judge*.

DECISION
Denying Patent Owner's Request for Rehearing of Final Decision
37 C.F.R. § 42.71(d)

I. INTRODUCTION

Renesas Electronics Corporation ("Petitioner") has filed a Request for Rehearing (Paper 36, "Request") of the Final Written Decision (Paper 35, "Final Decision"), which determined Petitioner had shown that claims 1 and 9–14 of U.S. Patent No. 8,284,844 B2 ("the '844 patent") were unpatentable, denied Broadcom Corporation's ("Patent Owner's") Motion to Amend as to proposed substitute claim 15, and granted the Motion to Amend as to proposed substitute claims 16–19. The Request seeks "rehearing to . . . deny Patent Owner Broadcom Corporation's motion to amend" as to proposed substitute claims 16–19. Request 1. In particular, Petitioner asserts "Patent Owner's amendments did not address unpatentability, but just attempted to improve its infringement position in district court," and the Board "misapprehended 37 C.F.R. § 42.121(a)(2)'s requirements for a motion to amend [and] overlooked the precedential standards for applying those requirements in *Lectrosonics* . . . ."[1] *Id.* For the reasons that follow, Petitioner's Request for Rehearing is denied.

II. THE REQUEST FOR REHEARING

In pertinent part, 37 C.F.R. § 42.71(d) states:

> The burden of showing a decision should be modified lies with the party challenging the decision. The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply.

[1] *Lectrosonics, Inc. v. Zaxcom, Inc.*, IPR2018-01129, Paper 15 (PTAB Feb. 25, 2019) (precedential).

Thus, a request for rehearing is not an opportunity merely to disagree with the Board's assessment of the arguments or weighing of the evidence, or to present new arguments or evidence.

Petitioner argues that reconsideration is appropriate because, but for the Board's misapprehension, Patent Owner's proposed substitute claims 16–19 should have been denied pursuant to 37 C.F.R. § 42.121(a)(2), providing that "[a] motion to amend may be denied where: (i) [t]he amendment does not respond to a ground of unpatentability involved in the trial; or (ii) [t]he amendment seeks to enlarge the scope of the claims of the patent . . . ." Request 1.

We have reviewed Petitioner's Request and carefully considered all of the arguments presented. For the following reasons, we are not persuaded that we misapprehended or overlooked any arguments or evidence. We, therefore, deny the Request.

III. DISCUSSION

Petitioner starts with the fact that challenged claim 11 required "all five recited hardware accelerators," whereas proposed substitute claim 16 would "require only 'at least four of' the five." Request 3 (citing Paper 19, 4–5). Petitioner further argues that this "broadening modification" did not respond to a ground of unpatentability involved in the trial, as required by 37 C.F.R. § 42.121(a)(2)(i).[2] *Id.*

[2] Petitioner does not dispute that all the proposed substitute claims are narrower than challenged claim 1, and therefore, as we determined in the Final Decision, those claims comply with the requirement to not enlarge the scope of the claims. Final Decision 62 (citing *Lectrosonics, Inc. v. Zaxcom, Inc.*, IPR2018-01129, Paper 15 at 6–7 (PTAB Feb. 25, 2019) (Precedential) ("A substitute claim will meet the requirements of § 42.121(a)(2)(i) and (ii)

A. Alleged Broadening of Claim 16

Petitioner asserts that the amendment to proposed substitute claim 16 broadened the claim "to try to improve its infringement position in a pending district court matter." *Id.* at 4. Petitioner argues "allowing patent owners to add claims and use amendments in an *inter partes* review to improve their infringement positions serves only patent owners' private interests, not any public ones." *Id.* at 6. Therefore, argues Petitioner, we should have denied the motion to amend as to proposed substitute claim 16, as well as proposed substitute claims 17–19, which depend therefrom. *Id.* at 9.

We disagree. As stated in our Final Decision, proposed substitute claim 16 depends from proposed substitute claim 15, which narrows challenged claim 10 to require, "wherein the plurality of hardware accelerators do not comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors." Final Decision 60.

B. Alleged Failure to Respond to a Ground of Unpatentability

This amendment to claim 15 attempted to further distinguish the claim as patentable over the references asserted in the instituted grounds. *Id.* In particular, because Patent Owner expressly addressed the Fandrianto '459, Fandrianto '351, and Reader references, which underlay our Institution Decision, the amendment to proposed substitute claim 15 responded to the grounds of unpatentability involved in the trial. *Id.*

Thus, as we determined in the Final Decision, we disagree with Petitioner's contention that proposed substitute claim 16 does not respond to

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if it narrows the scope of at least one claim of the patent . . . .").

any ground of unpatentability, because the claim includes the responsive features in the claim 15 amendment, based on claim 16's dependence on claim 15. Final Decision 61. Claims 17–19 also include the responsive features, based on their dependence on claim 16. Final Decision 61.

Petitioner asserts that, in determining whether proposed substitute claim 16 responds to a ground of unpatentability, it was error to take into account the above amendment of proposed substitute claim 15. Request 3–4. There is no basis for Petitioner's argument. Petitioner cites *Lectrosonics* as requiring that the responsiveness analysis must be "made on a claim-by-claim basis." *Id.* at 2. Actually, the quotation from *Lectrosonics* that Petitioner refers to deals with the requirement that the Motion to Amend propose a reasonable number of substitute claims, not whether the proposed substitute claims respond to a ground of unpatentability. *Lectrosonics*, Paper 15 at 5. *Lectrosonics* requires "review[ing] the entirety of the record to determine whether a patent owner's amendments respond to a ground of unpatentability involved in the trial." *Id.* Nonetheless, our analysis is made on a claim-by-claim basis — as is the case with any dependent claim, proposed substitute claim 16 includes all the limitations of the claim from which it depends, including the limitation that unquestionably is in response to Petitioner's original invalidity grounds. *See* 35 U.S.C. § 112(d) ("A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.").

Petitioner also relies on the statement in *Lectrosonics* that "once a proposed claim includes amendments to address a prior art ground in the trial, a patent owner also may include additional limitations." Request 4 (citing *Lectrosonics*, Paper 15 at 6). From this statement, Petitioner would

draw the inference that only the language in proposed substitute claim 16 itself can include the responsive amendment before a non-responsive amendment would be permitted. *Id.* at 4–5. Again, there is no basis for this, because by definition a dependent claim includes the limitations of the claim it refers to.[3]

Petitioner further argues in the alternative, that even if it were proper to consider the responsive amendment of proposed substitute claim 15 (and, as we have determined, it is proper), the additional amendment to proposed substitute claim 16 requiring only four out of five accelerators still should not be permitted. Request 5–6. Petitioner cites the statement in *Lectrosonics* that, once a responsive amendment is proposed, additional non-responsive "modifications that address potential 35 U.S.C. § 101 or § 112 issues, for example, are not precluded by rule or statute." *Id.* at 5 (citing *Lectrosonics*, Paper 15 at 6). Petitioner interprets this statement to mean that additional non-responsive amendments are *limited* to those that address Section 101 or 112 issues. *Id.* at 6. However, as the quoted statement indicates, addressing Section 101 or 112 issues are examples of permitted non-responsive amendments, not an exclusive list. *See, e.g.*, *SZ DJI Tech. Co., Ltd. v. Drone-Control LLC*, IPR2018-00207, Paper 44 at 38 (PTAB June 11, 2019). There is no *per se* rule that would deny such additional

[3] Petitioner relies on the non-precedential opinion in *Apple Inc. v. Valencell, Inc.*, IPR2017-00317, Paper 46 at 54–55 (PTAB June 1, 2018), which, it argues, supports its position that a dependent claim must include a responsive amendment in the four corners of the claim itself, rather than in the claim it refers to. Request 8. Our decision, however, applies the precedential *Lectrosonics* decision and 35 U.S.C. § 112.

amendments based on speculation as to the motives of Patent Owner that led to the amendment.

In sum, we are not persuaded that the Final Decision overlooked or misapprehended the arguments with respect to the Panel's grant of the Motion to Amend as to proposed substitute claims 16–19.

IV. CONCLUSION

We have reviewed and considered the arguments in Petitioner's Rehearing Request and conclude that Petitioner has not carried its burden of demonstrating that the Board misapprehended or overlooked any matters in rendering the Final Written Decision. 37 C.F.R. § 42.71(d).

Thus, Petitioner's challenge does not meet the standard set forth for a request for rehearing.

The Request for Rehearing is *denied*.

Outcome of Decision on Rehearing:

Claims	**35 U.S.C. §**	**References**	**Claims Shown Unpatentable**	**Claims Not shown Unpatentable**
1, 9, 10	103(a)	Fandrianto '459	1, 9, 10	
11–13	103(a)	Fandrianto '459, Fandrianto '351, Reader	11–13	
14	103(a)	Fandrianto '459, Fandrianto '351, Reader, Harrand	14	
Overall Outcome			1, 9–14	

Motion to Amend Outcome	Claim(s)
Original Claims Cancelled by Amendment	
Substitute Claims Proposed in the Amendment	15–19
Substitute Claims: Motion to Amend Granted	16–19
Substitute Claims: Motion to Amend Denied	15
Substitute Claims: Not Reached	

Final Outcome of Final Written Decision after Rehearing:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 9, 10	103(a)	Fandrianto '459	1, 9, 10	
11–13	103(a)	Fandrianto '459, Fandrianto '351, Reader	11–13	
14	103(a)	Fandrianto '459, Fandrianto '351, Reader, Harrand	14	
Overall Outcome			1, 9–14	

Motion to Amend Outcome	Claim(s)
Original Claims Cancelled by Amendment	
Substitute Claims Proposed in the Amendment	15–19
Substitute Claims: Motion to Amend Granted	16–19
Substitute Claims: Motion to Amend Denied	15
Substitute Claims: Not Reached	

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