UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner

Case No. IPR2017-00901
Patent No. 7,405,993

PATENT OWNER'S AMENDED NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141(c) and 319 and the February 10, 2022 order from the United States Court of Appeals for the Federal Circuit (CM/ECF Dkt. # 87), the patent owner, Polaris Innovations Limited ("Polaris") hereby provides this ***amended*** notice of appeal. Polaris intends to continue its appeal (no. 2019-1484) at the court following the recent limited remand for the purpose of Director rehearing pursuant to *United States v. Arthrex, Inc.*, 141 S. Ct. 1970 (2021).

In particular, Polaris continues to appeal from the Final Written Decision entered by the Patent Trial and Appeal Board on December 19, 2018 (Paper 45, copy attached) and from all underlying orders, decisions, rulings and opinions. In addition, Polaris now gives notice that it wishes to appeal from (1) the January 14, 2022 decision (Paper 54, "Rehearing Decision," copy attached) of Andrew Hirshfeld, Commissioner for Patents, Performing the Functions and Duties of the Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office, denying Polaris's request for Director rehearing and (2) the Board's refusal to grant the parties' joint motion to terminate (Paper 48) following the parties' settlement.

This notice of appeal is timely filed within seven days of the court's February 10, 2022 order.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Polaris indicates that the issues on appeal include (1) all of the issues identified in Polaris's original notice of appeal

filed January 25, 2019 (Paper 4) except the constitutionality of the appointments of the Board judges who rendered the Final Written Decision and (2) the Board's refusal to grant the parties' joint motion to terminate and the Board's failure to terminate this *inter partes* review after the parties settled this case.

Polaris's original notice of appeal, which is incorporated by reference herein, noted, *inter alia*, the following issues for appeal:

(A) The Board's determinations of unpatentability of claims 2-6 of U.S. Patent No. 7,405,993, including the determinations that (1) claims 2-6 are unpatentable under 35 U.S.C. § 103 as obvious over LaBerge (U.S. Patent Appl. Publ. No. 2005/0177690, Ex. 1005) in view of Bhakta (U.S. Patent Appl. Publ. No. 2005/0281096, Ex. 1010), (2) claims 2 and 4 are unpatentable under 35 U.S.C. § 103 as obvious over Kinsley (U.S. Patent Appl. Publ. No. 2006/0044860, Ex. 1006) in view of Swanson (U.S. Patent Appl. Publ. No. 2003/0046507, Ex. 1007), and (3) claims 2-4 are unpatentable under 35 U.S.C. § 103 as obvious over Kinsley in view of Swanson and further in view of Stave (U.S. Patent Appl. Publ. No. 2005/0283671, Ex. 1011);

(B) The Board's interpretations of claims 1 and 2 of the '993 Patent, including by way of example and not limitation, the phrases "memory chips," "semiconductor memory component," and "wherein the

semiconductor memory component comprises a plurality of memory chips"; and

(C) The Board's determinations that the references, particularly LaBerge, Bhakta, and Kinsley, disclose the recited semiconductor memory component comprising a plurality of memory chips.

Polaris also objects to the Director participating in this appeal as an intervenor regarding the patentability issues (A)-(C) above for lack of constitutional standing.

Respectfully submitted,

Date: 2022 Feb. 17

By: /M.C. Phillips/

Matthew C. Phillips
Registration No. 43,403
Lead Counsel for Patent Owner

CERTIFICATE OF SERVICE AND FILING

I hereby certify that on February 17, 2022, copies of the foregoing PATENT OWNER'S AMENDED NOTICE OF APPEAL and all documents filed with it were served via electronic mail, as agreed to by counsel, upon the following counsel for the Petitioner:

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I further certify that on February 17, 2022, the foregoing PATENT OWNER'S AMENDED NOTICE OF APPEAL was sent by Priority Mail Express® to the Director of the United States Patent and Trademark Office, at the following address:

Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel
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I further certify that on February 17, 2022, the foregoing PATENT OWNER'S AMENDED NOTICE OF APPEAL and a copy of the Final Written Decision and the Rehearing Decision were filed with the United States Court of Appeals for the Federal Circuit via its CM/ECF electronic filing system.

/ M.C. Phillips /
Matthew C. Phillips
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Paper 45
Entered: December 19, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

Case IPR2017-00901
Patent 7,405,993 B2

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and MONICA S. ULLAGADDI, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

NVIDIA Corporation ("Petitioner") filed a Petition for *inter partes* review of claims 1–14 of U.S. Patent No. 7,405,993 B2 (Ex. 1001, "the '993 patent"). Paper 2 ("Pet."). Polaris Innovations Limited ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). On August 30, 2017, we instituted an *inter partes* review of all of the challenged claims 1–14 of the '993 patent on several, but not all, grounds raised in the Petition. Paper 9, 28 ("Dec."). Thereafter, Patent Owner filed a Patent Owner Response. Paper 13 ("PO Resp."). Petitioner filed a Reply to the Patent Owner Response. Paper 20 ("Reply").[1]

On April 24, 2018, the Supreme Court issued its decision in *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018). In light of *SAS* and "Guidance on the Impact of SAS on AIA Trial Proceedings," issued by the Office, April 26, 2018 ("Office Guidance"), we instituted review of all challenged claims and all grounds presented in the Petition and authorized further briefing. Paper 29. Subsequently, the Chief Administrative Patent Judge extended the one-year period for issuing a Final Written Decision in the present proceeding. Papers 30, 31.

Patent Owner filed a Supplemental Response. Paper 35 ("Supp. Resp."). Petitioner filed a Supplemental Reply. Paper 37 ("Supp. Reply"). An oral hearing was held on September 28, 2018. A transcript of the hearing has been entered into the record. Paper 44 ("Tr.").

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[1] Patent Owner filed a listing of alleged improper reply content. Paper 24. Petitioner filed a response to the listing. Paper 26. We have considered both submissions.

In its briefs, Patent Owner only provides arguments regarding claim 2, which depends from claim 1. PO Resp. 2, 23–36; Supp. Resp. 3–4, 6, 17–18, 25, 31. Claims 3–6 depend directly or indirectly from claim 2, but Patent Owner does not provide arguments with respect to any of the additional elements claimed in claims 3–6. *Id*. However, because claims 3–6 ultimately depend from claim 2, Patent Owner is contesting the unpatentability showing by Petitioner of claims 2–6. *Id*.

Per our Scheduling Order, we notified the parties that "any arguments for patentability not raised in the [Patent Owner] response will be deemed waived."[2] During oral hearing, Patent Owner confirmed that it is "only defending claims 2 through 6." Tr. 28:17–29:8. Nonetheless, Petitioner bears the burden to show, by a preponderance of the evidence, that the challenged claims are unpatentable. For the reasons that follow, Petitioner has shown by a preponderance of the evidence that claims 1–14 of the '993 patent are unpatentable.

A. Related Matters

According to the parties, the '993 patent was the subject of a pending lawsuit that was transferred from the United States District Court for the Western District of Texas to the United States District Court for the Northern District of California. Pet. 105; Paper 4 ("Patent Owner's Initial Mandatory Notices"), 2–3. Patent Owner identifies the lawsuit pending in the Northern District of California, i.e., *Polaris Innovations Ltd. v. Dell Inc.*,

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[2] *See* Paper 10, 3; *see also* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012) (a patent owner's "response should identify all the involved claims that are believed to be patentable and state the basis for that belief").

Case No. 4:16–cv-07005 (N.D. Cal.). Patent Owner's Initial Mandatory Notices, 2–3. The lawsuit has been stayed pending this proceeding. Tr. 15:23–16:4, 30:4–8.

B. The '993 Patent

The '993 patent is directed to a control component for controlling a semiconductor memory component in a semiconductor memory module. Ex. 1001, [57], 2:57–59. Depending on the storage capacity and rank configuration of the semiconductor memory module, address terminals are actuated through selection circuits either with address or control signals. *Id.*, [57]. Control terminals are actuated with different control signals. *Id.* Multiplexing of address and control signals allows the control component to control semiconductor memory components with different memory configurations without requiring an increased number of control terminals. *Id.* Figure 4 of the '993 patent is reproduced below.

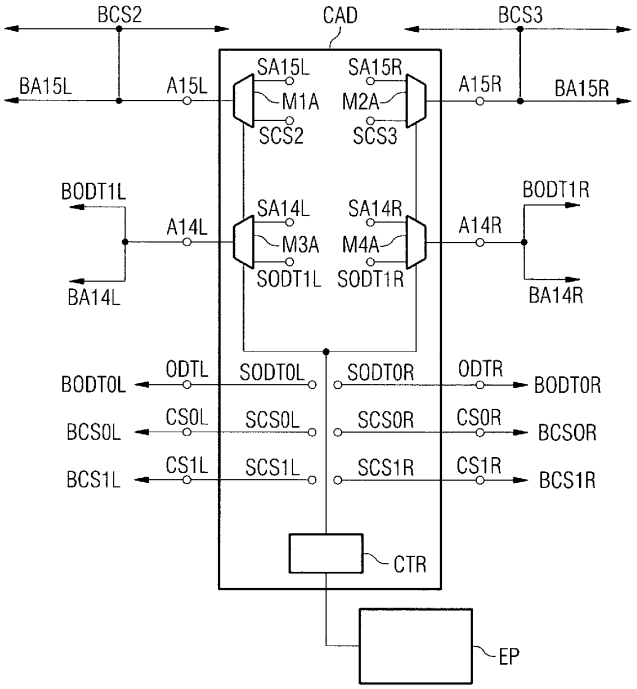

Figure 4 shows a control unit in a control component for controlling semiconductor memory components in a semiconductor memory module. *Id.* at 3:39–41.

Address terminals A14L, A14R, A15L, and A15R may be used to supply address or control signals. *See id*. at 6:5–14. To control whether address or control signals are provided, selection circuits (labeled M1A–M4A) select between "address" or "control" signals. *Id*. at 6:15–60. The selection circuits are described as multiplexers and are controlled via a control circuit CTR based on a stored module configuration (stored in memory circuit EP). *Id*. at 6:61–67.

C. Illustrative Claim

Petitioner challenges claims 1–14 of the '993 patent. Claim 1 and claim 2, both reproduced below, are illustrative of the claimed subject matter (italicizing added for emphasis):

> 1. A control component for controlling a *semiconductor memory component* in a semiconductor memory module, comprising:
>
> a control unit for generating control signals for controlling read and write access to the semiconductor memory component and for generating address signals for addressing memory cells in the semiconductor memory component for read and write access;
>
> a plurality of address terminals for providing the address signals; and
>
> a selection circuit for supplying one of the address terminals with a selected signal selected between one of the address signals and one of the control signals.

Id. at 11:24–37.

> 2. The control component as claimed in claim 1,
>
> *wherein the semiconductor memory component comprises a plurality of memory chips*; and
>
> wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access.

Id. at 11:38–43.

D. Instituted Grounds of Unpatentability

We instituted trial based on all asserted claims and grounds of unpatentability as follows (Dec. 28; Paper 29):

References	Basis	Challenged Claims
Ajanovic[3]	§ 103(a)	1, 2, 4, 7, and 8
LaBerge[4]	§ 103(a)	1–10
Kinsley[5] and Swanson[6]	§ 103(a)	1, 2, 4, 7, and 8
Kinsley, Swanson, Hung[7], and Holman[8]	§ 103(a)	9, 10, and 12–14
LaBerge and Bhakta[9]	§ 103(a)	1–11 and 14

[3] U.S. Patent No. 6,298,426, issued Oct. 2, 2001 (Ex. 1004) ("Ajanovic").
[4] U.S. Patent Application Publication No. 2005/0177690 A1, filed Feb. 5, 2004, published Aug. 11, 2005 (Ex. 1005) ("LaBerge").
[5] U.S. Patent Application Publication No. 2006/0044860 A1, filed Sep. 1, 2004, published Mar. 2, 2006 (Ex. 1006) ("Kinsley").
[6] U.S. Patent Application Publication No. 2003/0046507 A1, filed Aug. 30, 2001, published Mar. 6, 2003 (Ex. 1007) ("Swanson").
[7] U.S. Patent No. 7,023,719, issued Apr. 4, 2006 (Ex. 1008) ("Hung").
[8] U.S. Patent No. 6,968,419, issued Nov. 22, 2005 (Ex. 1009) ("Holman").
[9] U.S. Patent Application Publication No. 2005/0281096 A1, filed Mar. 7, 2005, published Dec. 22, 2005 (Ex. 1010) ("Bhakta").

References	Basis	Challenged Claims
Ajanovic and Stave[10]	§ 103(a)	1–4, 7, and 8
Kinsley, Swanson, and Stave	§ 103(a)	1–4, 7, and 8

II. DISCUSSION

A. Principles of Law

To prevail in its challenge to Patent Owner's claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are

[10] U.S. Patent Application Publication No. 2005/0283671 A1, filed June 21, 2004, published Dec. 22, 2005 (Ex. 1011) ("Stave").

made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citation omitted). Petitioner's declarant, Dr. Harry L. Tredennick, testifies that a person with ordinary skill in the art "would have a Bachelor's degree in Electrical Engineering and at least 2 years of experience working in the field of semiconductor logic design." Ex. 1003 ¶ 13. Dr. Steven A. Przybylski, Patent Owner's declarant, applies the same definition. Ex. 2002 ¶ 31.

Therefore, we adopt Dr. Tredennick's assessment of a person with ordinary skill in the art. We further note that the prior art of record in the instant proceeding reflects the appropriate level of ordinary skill in the art. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (holding the Board may omit specific findings as to the level of ordinary skill in the art "where the prior art itself reflects an appropriate level and the need for testimony is not shown").

C. Claim Interpretation

In an *inter partes* review, claim terms in an unexpired patent are given their "broadest reasonable construction in light of the specification of the patent in which they appear."[11] 37 C.F.R. § 42.100(b) (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Only terms which are in controversy need to be construed, and only to the extent necessary to resolve

[11] We would construe the claim terms discussed below the same under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). It is improper to add an extraneous limitation into a claim, i.e., one that is added wholly apart from any need for the addition to accord meaning to a claim term. *See, e.g.*, *Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 950 (Fed. Cir. 1993); *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988). There is a presumption that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). To overcome this presumption, the patentee must "clearly set forth" and "clearly redefine" a claim term away from its ordinary meaning. *Bell Atlantic Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1268 (Fed. Cir. 2001). The disavowal must be "unmistakable" and "unambiguous." *Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1322 (Fed. Cir. 2012).

Petitioner proposes claim interpretations for "address terminal" and "control terminal." Pet. 18–19. In our Decision to Institute, we interpreted these terms. Dec. 6–7. Neither party has indicated that our interpretations were improper and we do not perceive any reason or evidence that now compels any deviation from our initial interpretations. Accordingly, the following constructions apply to this Decision: "address terminal" means "a terminal that is capable of providing an address signal," and "control terminal" means "a terminal that is capable of providing a control signal."

Patent Owner proposes claim interpretations for "semiconductor memory component," "memory chips," and "wherein the semiconductor memory component comprises a plurality of memory chips," recited in claim 2. PO Resp. 8–23. Petitioner opposes Patent Owner's proposed interpretations and proposes its own interpretations. Reply 12, 15. As explained below, we do not adopt Patent Owner's proposed interpretations for "semiconductor memory component," "memory chips," and "wherein the semiconductor memory component comprises a plurality of memory chips," but adopt Petitioner's proposed interpretations.

Claim 1 recites in the preamble, "[a] control component for controlling a semiconductor memory component in a semiconductor memory module." Ex. 1001, 11:24–37. Claim 2 recites "wherein the semiconductor memory component comprises a plurality of memory chips." *Id*. at 11:39–40.

Patent Owner argues that "semiconductor memory component" means "one discrete packaged semiconductor memory device." PO Resp. 15–20. And although it is not in dispute that the ordinary meaning of "memory chip" can refer to either a packaged integrated circuit or a single die (PO Resp. 20 (citing Ex. 2002 ¶¶ 38, 48); Reply 12 (citing Ex. 2002 ¶ 38; Ex. 1019, 43:17–21)), Patent Owner argues that the '993 patent specification only contemplates the latter and not the former, such that a "memory chip" means "a single memory IC die." PO Resp. 20–22. Putting it all together, Patent Owner argues that "wherein the semiconductor memory component comprises a plurality of memory chips," recited in claim 2 means a

"discrete, packaged semiconductor memory device ha[ving] a plurality of single memory IC die within the same package." *Id*. at 22; Supp. Resp. 7.[12]

Petitioner argues that Patent Owner is imposing constructions that would require memory ICs (dies) to be packaged in a single piece of plastic, as opposed to chips that are themselves packaged integrated circuits, any number of which comprise a "semiconductor memory component." Reply 5–6; Supp. Reply 1, 3–4.[13] Petitioner further argues that to the extent "semiconductor memory component" should be construed, the phrase is limited only by the number of memory chips that make up the "semiconductor memory component." Reply 12; Ex. 1001, 1:33–34. Petitioner argues that to the extent "memory chip" should be construed, that term means "a packaged integrated circuit or a single die." Reply 15.[14]

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[12] The parties sometimes refer to Patent Owner's proposed construction as a "multi-die package." *See, e.g.*, Tr. 12:11–14, 16:8–9, 34:18, 45:8–10.

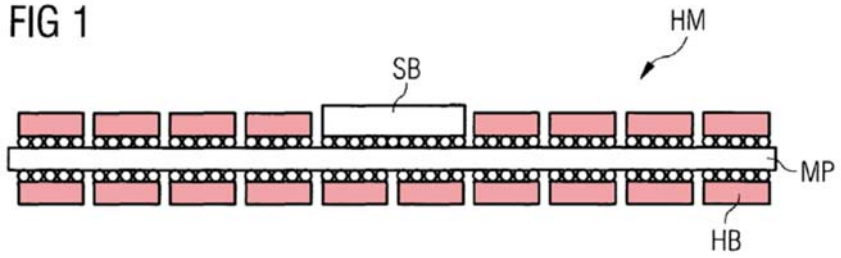
[13] Our citations to the unnumbered pages begins with page 1 on the page with the "INTRODUCTION."

[14] Petitioner alternatively argues that the claims are directed to a "control component" for controlling memory, not the memory being controlled, such that the specific configuration of the "memory component" does not matter by design for the purpose of patentability. Reply 18, 21–23; Tr. 8:18–9:15 (arguing for the "appropriate weight" we should give the disputed terms). We agree with Patent Owner that Petitioner's appropriate weight argument, which we understand to mean that little or no patentable weight should be given to the disputed terms, was not presented in the Petition and comes too late in the Reply. Paper 24, 1; Tr. 34:3–8. In the Petition, Petitioner clearly gives full patentable weight to the disputed terms by showing where in the prior art those terms are met. *See, e.g.*, Pet. 70–71, 94–96. Petitioner's "appropriate" or "little" patentable weight argument was not necessitated by the arguments presented by Patent Owner's Response. Rather, Petitioner's appropriate weight theory could have and should have been presented in the Petition. As such, the argument comes too late. *See* 37 C.F.R. § 42.23(b).

Semiconductor Memory Component

Although Patent Owner argues that "semiconductor memory component" means "one discrete packaged semiconductor memory device" (PO Resp. 15–20), nowhere in the claims or the specification of the '993 patent is the phrase "discrete package[d]," the individual words of that phrase, or the phrase "semiconductor memory device." Tr. 29:9–18. Moreover, Patent Owner does not direct us to anything in the prosecution history that would support a construction of the phrase "semiconductor memory component" to mean "one discrete packaged semiconductor memory device." *Id*. at 29:18–21. We do not find anything in the prosecution history to support Patent Owner's construction. The first Office Action from the Examiner was "A Notice of Allowability." Ex. 1002, 12–14.

Patent Owner argues, however, that certain figures of the '993 patent, for example Figure 1 annotated below, describe the "semiconductor memory component" as "one discrete packaged semiconductor memory device." PO Resp. 15–18; Supp. Resp. 7.



Patent Owner's annotated Figure 1 from the '993 patent, shown above, is described in the "BACKGROUND" section. Ex. 1001, 1:21–38.

Patent Owner reproduces Figure 1, with shading, and also refers to Figures 5, 7, and 9, and concludes that no other form of a "semiconductor memory component," labeled "HB" in pink shading above, is described and

that the '993 Patent never discloses or contemplates a "semiconductor memory component" formed of more than one separately packaged memory chip. PO Resp. 15–16 (citing Ex. 2002 ¶ 55; Ex. 2004, 27:12–16). That argument, however, is misplaced. The specification of the '993 patent need not explicitly show or describe two separately packaged memory chips together as a memory component for the broad claim language to encompass such an arrangement. Patent Owner has not directed us to anything in the specification or prosecution history that indicates that Patent Owner disclaimed a "semiconductor memory component" formed of more than one separately packaged memory chip, one which Patent Owner readily acknowledges is a possibility. *See, e.g.*, PO Resp. 20 (admitting that the term "chip" can refer to either *a packaged integrated circuit* or a single die). The specification of the '993 patent describes that a semiconductor memory component "includes one or more memory chips," which is a broad description, meeting the broad claim language. Ex. 1001, 1:33–35. Neither Patent Owner nor Dr. Przybylski address this description. *See, e.g.*, Ex. 2002 ¶ 55 (asserting that "[n]o broader interpretation of the term [semiconductor memory component] is reasonable" despite not addressing the description that a semiconductor memory component "includes one or more memory chips").

Moreover, there are other descriptions in the '993 patent specification that undermine Patent Owner's proposed construction and its argument that the specification makes a "distinction between a 'memory chip' and a 'semiconductor memory component.'" PO Resp. 21. The specification sometimes uses the two terms interchangeably. For instance, the specification describes that "the control component SB actuates the relevant

semiconductor memory component *or the memory chip* of the memory component via a control signal." Ex. 1001, 1:54–56 (emphasis added). And although Figure 1 shows semiconductor memory components HB arranged on a module board, the specification describes "memory chips" being "situated on the module board," and that "the module board holds a total of 72 memory chips." *Id*. at 2:6–8, 2:36–38; *see also id*. at 8:42–53, 9:25–31 (interchanging the term "memory chips" located on a particular side of the control component with "semiconductor memory components" located on a particular side of the control component). Such descriptions would have indicated to a person having ordinary skill in the art that the specification of the '993 patent does not necessarily make a distinction between a "memory chip" and a "semiconductor memory component" insofar as the exact physicality of those elements is concerned. Such descriptions would have further indicated that the "semiconductor memory component" is limited by the number of memory chips that make up the "semiconductor memory component." *Id*. at 1:33–35. We note, however, neither Patent Owner nor its expert address these other passages.

Because there are descriptions in the '993 specification, not addressed by Patent Owner, that support a broader construction than the one proposed by Patent Owner, we decline to read limitations from the few figures into the claim language. Indeed, our reviewing court consistently has not construed claims as being limited to particular embodiments. *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) (holding that it is not enough that the only embodiment, or all of the embodiments, contain a particular limitation to limit a claim to that particular limitation); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111,

1117 (Fed. Cir. 2004); *see, e.g., SRAM Corp. v. AD-II Eng'g, Inc.*, 465 F.3d 1351, 1359 (Fed. Cir. 2006) ("While SRAM strongly urges the court to interpret the claim to encompass the innovative precision indexing shifting feature it contends it has invented, we are powerless to rewrite the claims and must construe the language of the claim at issue based on the words used" (citing *Hoganas AB v. Dresser Indus., Inc.,* 9 F.3d 948, 951 (Fed. Cir. 1993)); "In this case, the words are clear and the claim covers no more than the recited method of taking up lost motion and effecting a shift.").

Furthermore, the court "has repeatedly cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1346–47 (Fed. Cir. 2015); *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (noting that "it is important not to import into a claim limitations that are not a part of the claim"). "[I]t is the *claims*, not the written description, which define the scope of the patent right." *Williamson*, 792 F.3d at 1346–47; *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (noting that "[i]t is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude"). Here we decline the invitation to limit the claim language of claim 2 by importing limitations, to the extent they even exist, from the specification into the claim.

We next address Patent Owner's argument that the Petition's implied interpretation of "semiconductor memory component" is unreasonably broad and would include anything with semiconductor memory in it. PO Resp. 17 (citing Ex. 2002 ¶¶ 50–53). We disagree that Petitioner has applied such a broad construction to the phrase. Claim 1 requires the "semiconductor

memory component" be in a "semiconductor memory module." Petitioner acknowledges as much. Reply 10–11. The term "semiconductor memory component" is not untethered from it being a part of the "semiconductor memory module." Petitioner has correctly applied it that way. *Id.*; *see also* Pet. 70, 94–95.

Patent Owner additionally argues that its proposed construction is consistent with the art-recognized meaning of the phrase, because the term "component" in the electrical arts typically refers to a "discrete packaged electronic element." PO Resp. 18 (citing Ex. 2007; Ex. 2002 ¶ 39). Patent Owner's dictionary definition for "component" is "[a] discrete packaged electronic element, such as a resistor, that performs one electrical function." Ex. 2007, 95. Patent Owner fails to explain the relevance of this definition, which is directed to a single electronic element, such as a resistor, to the term "semiconductor memory component," which as described in the specification "includes one or more memory chips," and is broadly described. Ex. 1001, 1:33–34. Accordingly, we give little weight to Patent Owner's dictionary definition of "component." Nor are we persuaded by Patent Owner's arguments that Bhakta confirms the meaning of the phrase "semiconductor memory component" to mean a discrete packaged semiconductor device. PO Resp. 18–19 (citing Ex. 1010 ¶¶ 3, 88, Abstract, Fig. 10A; Ex. 2002 ¶¶ 68, 72). Patent Owner fails to explain how Bhakta's use of the term "memory component" is used to narrowly mean a discrete packaged semiconductor device only.

We also have considered Dr. Przybylski's testimony that "the most common use of 'component' is to refer to a discrete packaged integrated circuit or comparable circuit element." Ex. 2002 ¶ 39. In support of that

assertion, Dr. Przybylski relies on Exhibit 2005, which has a date of 2008. The effective filing date of the '993 patent, however, is no later than October 31, 2006. Yet, Patent Owner and Dr. Przybylski fail to explain how a book that is dated well after the effective filing date of the patent is relevant to show what a person of ordinary skill in the art knew at the time of the invention. Tr. 43:19–44:2. Thus, Dr. Przybylski's testimony is entitled to little weight.

Moreover, Dr. Przybylski's reliance on Exhibit 2005 in support of his testimony that "the most common use of 'component' is to refer to a discrete packaged integrated circuit or comparable circuit element" does not withstand further scrutiny, because Dr. Przybylski also acknowledges that a component means a thing that is a part of something else. Ex. 2002 ¶¶ 39, 53. We do not know why, based on the record before us, we should assume that the narrower, and not the broader meaning of "component" applies here. The same applies to how Bhakta uses the term "component." If anything, the broader meaning would comport with the broad claim language and the description in the specification of the '993 patent that the semiconductor memory component "includes one or more memory chips." Ex. 1001, 1:33–34.

For all of the above reasons, we are not persuaded that "semiconductor memory component" means "one discrete packaged semiconductor memory device." Rather, we agree with Petitioner that "semiconductor memory component," in light of the specification, is limited only by the number of memory chips that make up the "semiconductor memory component." Reply 12; Ex. 1001, 1:33–34.

Memory Chip

Claim 2 recites "wherein the semiconductor memory component comprises a plurality of *memory chips*." *Id*. at 11:39–40. It is not in dispute that the ordinary meaning of a "memory chip" can refer to either a packaged integrated circuit or a single die. PO Resp. 20 (citing Ex. 2002 ¶¶ 38, 48); Reply 12 (citing Ex. 2002 ¶ 38; Ex. 1019, 43:17–21). It is Patent Owner's position, however, that only the latter is consistent with the "patent's clear use of the phrase 'semiconductor memory component' to mean a packaged integrated circuit." PO Resp. 20. Patent Owner's proposed construction for the term "memory chip" is "a single memory IC die." *Id*. 20–22.

In support of its argument, Patent Owner directs attention to Figure 2A from the '993 patent, reproduced below.

FIG 2A

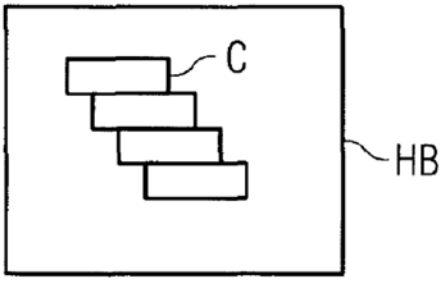


Figure 2A from the '993 patent shows "an embodiment of a semiconductor memory component comprising memory chips." Ex. 1001, 3:32–33. Patent Owner argues that Figure 2A shows four chips C and that each chip is an individual die within the semiconductor memory component HB, and that the arrangement is a "stack arrangement" within "one packaged IC." PO Resp. 20–21 (citing Ex. 1001, 1:33–38; Ex. 2002 ¶¶ 48, 49). We have reviewed Dr. Przybylski's testimony in support of the proposed construction. Neither he nor Patent Owner discusses any other passage in

the specification of the '993 patent besides Figure 2A and column 1, lines 33 to 38 regarding memory chips. *Id*. Rather, his explanation for why we should construe narrowly "memory chips" focuses solely on that one embodiment of the specification. Ex. 2002 ¶¶ 48, 49.

In the '993 patent specification, only one other passage describes stacked chips. In particular, the specification of the '993 patent describes "an embodiment of a control component SB for controlling semiconductor memory components." Ex. 1001, 5:13–15. In that embodiment, "[t]he external terminals CS0, . . . , CSn can carry control signal SCS, e.g., for selecting memory chips arranged in stacked form in the semiconductor memory components." Ex. 1001, 5:18–21. The usage of "*e.g.*" would have indicated to a person having ordinary skill in the art that this is just an example. Patent Owner does not discuss this, or any other passage in any way. Additionally, and as explained above, the specification sometimes uses the terms "semiconductor memory component" and "memory chip" interchangeably and certainly does not limit the terms as Patent Owner argues. For all of the above reasons, we do not adopt Patent Owner's proposed construction for "memory chip." Rather, we agree with Petitioner that a memory chip means "a packaged integrated circuit or a single die." Reply 15.

"wherein the semiconductor memory component comprises a plurality of memory chips"

Claim 2 recites "wherein the semiconductor memory component comprises a plurality of memory chips." Patent Owner argues that the phrase means the discrete, packaged semiconductor memory device has a plurality of single memory IC die within the same package. PO Resp. 22.

For the reasons provided above, we do not adopt Patent Owner's proposed constructions for "semiconductor memory component" and "memory chip." Accordingly, we do not adopt Patent Owner's proposed construction for "wherein the semiconductor memory component comprises a plurality of memory chips."

D. Asserted Obviousness over LaBerge and Bhakta

Petitioner contends claims 1–11 and 14 are unpatentable under 35 U.S.C. § 103(a) as obvious over LaBerge and Bhakta. Pet. 2, 31–60, 93–100. In support of its showing, Petitioner relies upon the declaration of Dr. Nick Tredennick. *Id.* (citing Ex. 1003).

1. LaBerge

LaBerge describes a memory module including a memory hub that couples signals to memory devices mounted on opposite first and second surfaces of a memory module substrate. Ex. 1005, Abstract. The memory hub alters the configuration of address and/or command signals coupled to the memory devices depending on whether the memory devices on the first surface of the substrate or the memory devices on the second surface of the substrate are accessed. *Id.* Figure 4 of LaBerge is reproduced below.

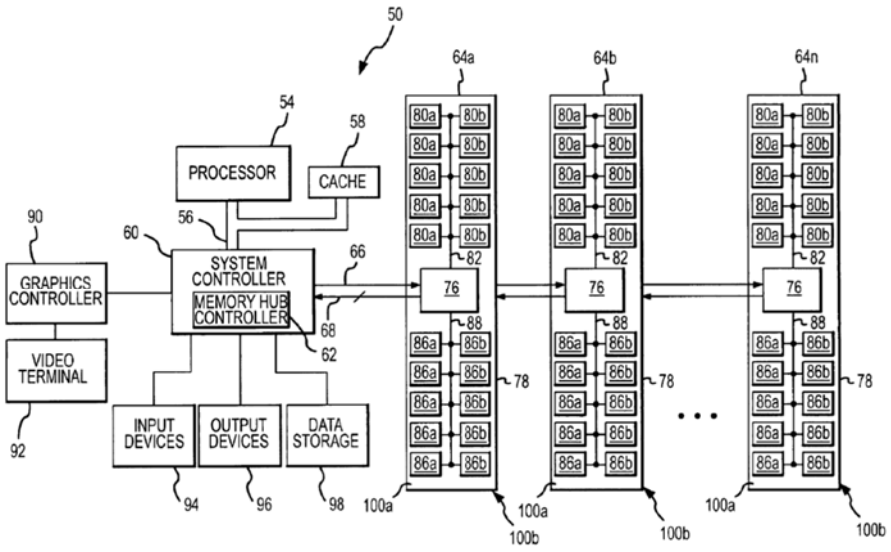


FIG.4

Figure 4 of LaBerge is a block diagram of a computer system including several memory modules.

As shown in Figure 4, computer system 50 includes a processor 54 and a processor bus 56 coupled to cache memory 58 and system controller 60. *Id.* ¶ 22. System controller 60 contains a memory hub controller 62 that is coupled to processor 54. *Id.* ¶ 23. Memory hub controller 62 is coupled to memory modules 64*a-n* which are coupled to each other through a downstream bus 66 and an upstream bus 68, which couple data, address, and/or control signals away from or toward memory hub controller. *Id.* Each memory module 64*a-n* includes a memory hub 76 that is coupled to several memory devices 80*a,b* on one side of memory module 64 through a first set of command, address, and data buses 82, and coupled to several identical memory devices 86*a,b* on the other side of memory module 64 through a second set of command, address, and data buses 88. *Id.* Memory hub 76 routes requests and responses between memory hub controller and memory devices 80, 86. *Id.*

Address and control signals are coupled to the proper terminals of memory devices 80, 86 by memory hub 76 coupling different signals to the same lines of buses 82, 88 depending upon which memory device is being accessed. *Id.* ¶ 27. Different address and control signals also are coupled to the same lines of bus 88 depending on whether memory device 86*a* or 86*b* is being accessed. *Id.* Memory devices 80, 86 have different terminal assignments depending on which mode of operation is used by memory devices 80, 86 (e.g., DDR2 or DDR3). *Id.* ¶ 28.

Memory hub 76 includes a memory controller 200 which receives high-level macro commands, such as ACTIVATE, ROW, COLUMN, and PRECHARGE, converts these commands to DRAM commands, schedules DRAM commands for outputting at the proper time, and routes scheduled DRAM commands to the correct terminals of memory hub 76. *Id.* ¶ 34. Memory controller 200 includes multiplexers (e.g., 230, Figure 5) which route command and address signals to terminals of memory hub 76. *Id.* ¶ 37, Fig. 5, Tables 1 and 2. A portion of Table 1, reproduced below, shows that terminal location D_{13}, for example, provides signal ODT_1 in DDR2 and address signal A_0 in DDR3. *Id.* ¶ 29, Table 1.

TABLE 1-continued

Hub Left Terminal Location	Hub Right Terminal Location	82a, 86a DDR2 CS_0	82b, 86b DDR2 CS_1	82a, 86a DDR3 CS_0	82b, 86b DDR3 CS_1
A_7	A_{28}	A_{15}	A_{14}	A_{14}	A_4
A_{10}	A_{23}	A_{16}	A_{16}	A_{16}	A_{16}
D_7	D_{27}	BA_0	BA_0	BA_1	BA_0
E_{13}	D_{20}	BA_1	CASZ	A_{10}	WEZ
E_7	E_{25}	BA_2	BA_2	CSZ_1	CSZ_1
F_{12}	F_{22}	BA_3	BA_3	ODT_1	ODT_1
D_8	D_{26}	CASZ	BA_1	CASZ	RASZ
D_6	D_{28}	CSZ_0	CSZ_O	WEZ	A_{10}
D_{11}	D_{21}	CSZ_1	CSZ_1	BA_0	BA_1
C_9	E_{28}	ODT_0	ODT_0	ODT_0	ODT_0
D_{13}	C_{20}	ODT_1	ODT_1	A_0	A_3
F_9	E_{22}	RASZ	WEZ	CSZ_0	CSZ_0
E_{10}	D_{22}	WEZ	RASZ	RASZ	CASZ

2. Bhakta

Bhakta describes memory modules comprising a plurality of memory components or integrated circuits. Ex. 1010 ¶ 2. Figure 3 of Bhakta is reproduced below.

FIGURE 3

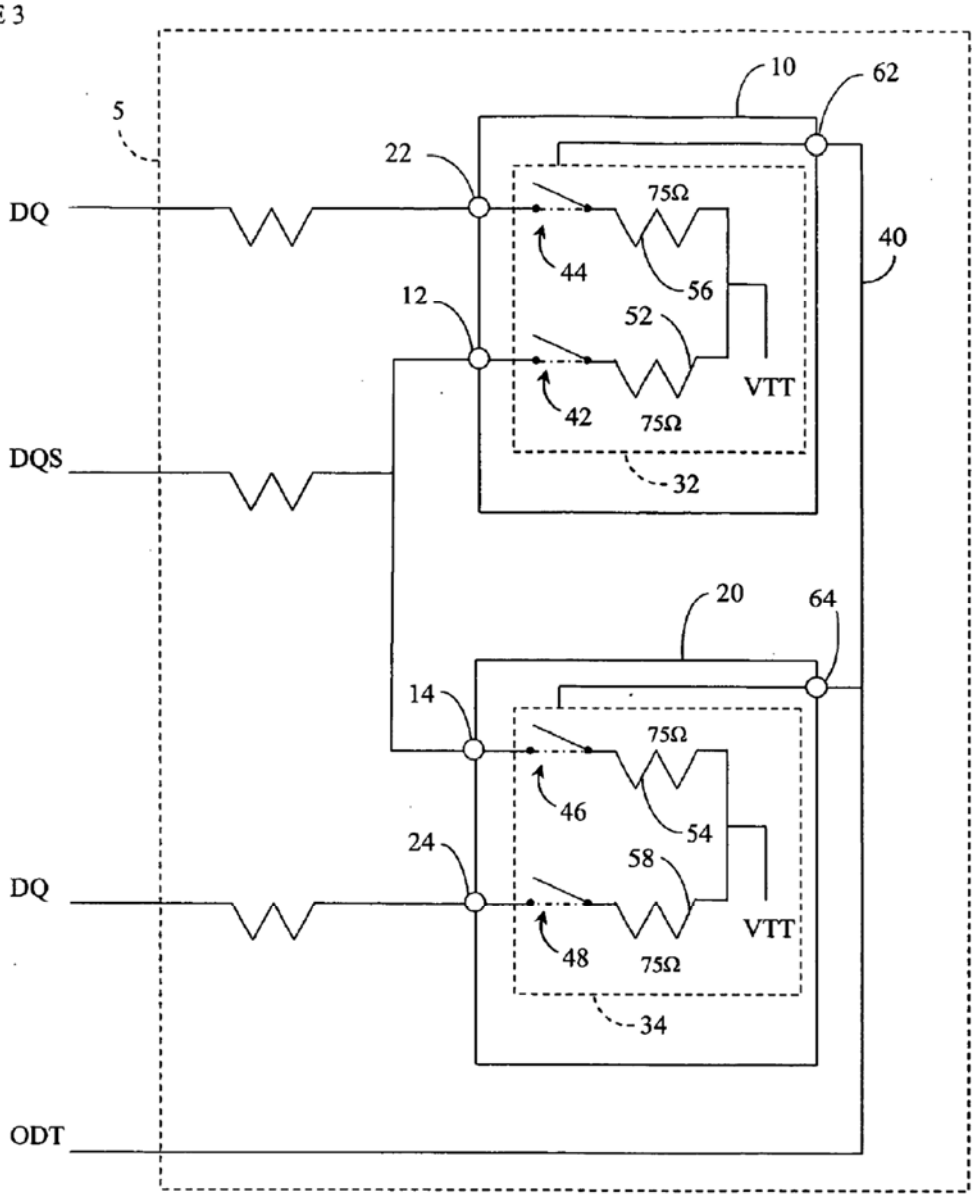


Figure 3 of Bhakta shows memory components 10, 20 with a respective on-die termination or "ODT" circuit 32, 34, which as termination resistors internal to memory components 10, 20 provide signal termination. *Id.* ¶ 34. Each memory component 10, 20 has a corresponding ODT signal pin 62, 64 which is electrically connected to a memory controller via an ODT bus 40. *Id.* Bhakta describes examples of memory components 10, 20,

which include ODT circuits 32, 34, such as DDR-2 memory components. *Id.* ¶ 35.

Figure 10A of Bhakta is reproduced below.

FIGURE 10A

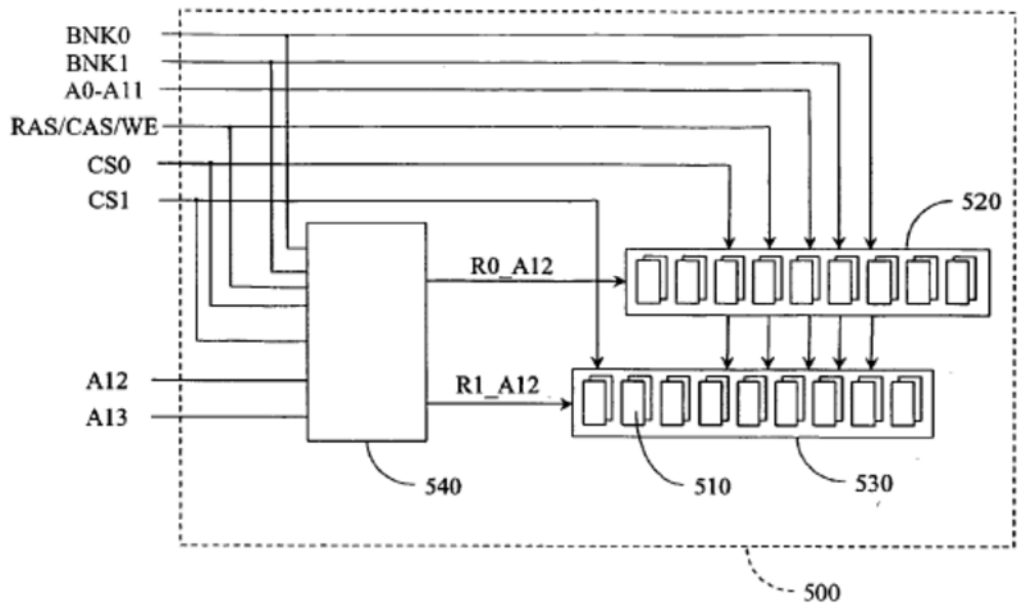


Figure 10A of Bhakta schematically illustrates an exemplary memory module 500 which doubles the rank density. *Id.* ¶ 88. Memory module 500 comprises a plurality of substantially identical memory components 510 configured as a first rank 520 and a second rank 530. *Id.* Memory components 510 of first rank 520 are configured in pairs with their respective DQS pins tied together. *Id.* Memory components 510 of second rank 530 are configured in pairs with their respective DQS pins tied together. *Id.* Memory module 500 comprises logic element 540 that receives a first set of address and control signals from a memory controller. *Id.*

Bhakta describes embodiments where two lower-density memory components are used to simulate one higher-density memory component.

Id. ¶ 77. In such embodiments, the serial-presence-detect (SPD) device of the memory module is programmed to describe the combined pair of lower-density memory components as one virtual or pseudo-higher-density memory component. *Id.*

3. Discussion

Petitioner asserts that the combination of LaBerge and Bhakta describe all of the elements of claims 1–11 and 14, and that it would have been obvious to combine LaBerge and Bhakta. Pet. 2, 31–60, 93–100.

Claim 1

Claim 1 recites "[a] control component for controlling a semiconductor memory component in a semiconductor memory module." Petitioner contends, and we are persuaded, that LaBerge's memory hub 76 is a control component that controls memory devices 80, 86 (semiconductor memory component) of memory module 64 (semiconductor memory module) as claimed. Pet. 31 (citing Ex. 1005 ¶¶ 23, 34; Ex. 1003 ¶ 56).

Claim 1 further recites "a control unit for generating control signals for controlling read and write access to the semiconductor memory component and for generating address signals for addressing memory cells in the semiconductor memory component for read and write access." Petitioner contends, and we are persuaded, that LaBerge's memory controller 200 receives commands from memory hub controller 62 and translates received commands to generate DRAM command signals, such as RASZ, CASZ, WEZ, etc., which are applied to terminals of memory hub 76 for operation of memory devices 80, 86, and that such DRAM command signals are control signals that control read and write access to memory devices 80, 86. Pet. 31–32 (citing Ex. 1005 ¶¶ 27, 28, 34–38; Ex. 1003

¶ 57). Petitioner explains that, although LaBerge describes row and column addresses for accessing memory devices 80, 86, LaBerge does not explicitly disclose address signals for addressing memory cells. Pet. 32–33 (citing Ex. 1005 ¶¶ 26–29, 34–41; Ex. 1003 ¶ 58). Petitioner relies on Bhakta to teach the "address signals for addressing memory cells" limitation. Pet. 93–94. In particular, Petitioner contends, and we agree, that Bhakta's DRAM memory components (e.g., DDR-2 memory components) include memory cells arranged in rows and columns and that row and column signals are used to address the memory cells during read and write cycles. Pet. 94 (citing Ex. 1010 ¶¶ 5–7, 12–14, 30, 88, 95, 97; Ex. 1003 ¶ 181; Ex. 1005 ¶ 29).

Claim 1 recites "a plurality of address terminals for providing the address signals." We agree with Petitioner's contentions that LaBerge's memory hub 76 has externally accessible terminals and that the terminals are used for providing address signals as shown in Table 1. Pet. 35 (citing Ex. 1005 ¶¶ 29–31; Ex. 1003 ¶ 61). Claim 1 also recites "a selection circuit for supplying one of the address terminals with a selected signal selected between one of the address signals and one of the control signals." Petitioner contends, and we agree, that to select appropriate signals for the memory hub terminals, multiplexers 230 (selection circuit) of memory controller 200 route command and address signals to terminals of memory hub 76 by selecting between an address signal [A10, BA2, or A0 and A3] and a control signal [WEZ, CSZ0, CSZ1, or ODT1]. Pet. 36–39 (citing Ex. 1005 ¶¶ 28–30, 37, Table 1; Ex. 1003 ¶¶ 62–64).

Lastly, Petitioner provides a rationale for combining LaBerge and Bhakta by explaining that Bhakta describes explicitly what LaBerge implicitly describes, such that a person having ordinary skill in the art would

have found it obvious to use Bhakta's memory components with memory cells in LaBerge, where address signals provide addressing for read and write access. Pet. 93–94 (citing Ex. 1003 ¶¶ 178–181).

Based on the record before us, we are persuaded by Petitioner's showing, which we adopt as our own, that claim 1 would have been obvious in view of LaBerge and Bhakta. As explained above, Patent Owner does not make any arguments with respect to claim 1. *See* PO Resp.; *see also* Supp. Resp.

Claims 7–11 and 14

We have reviewed the Petition for dependent claims 7–11 and 14 and determine that Petitioner has shown by a preponderance of the evidence that claims 7–11 and 14 would have been obvious in view of LaBerge and Bhakta.

Claim 7 depends from claim 1 and recites "wherein the control unit is supplied with a configuration signal and the selection circuit selects the selected signals based on the configuration signal." Petitioner contends that LaBerge's memory controller 200 is supplied with "a CONFIG command" through bus 232, and that the CONFIG command indicates whether memory devices 80, 86 are of the type operating in the DDR2 or DDR3 modes. Pet. 52 (citing Ex. 1005 ¶¶ 34, 37). Petitioner further contends that LaBerge's multiplexers 230 receive the CONFIG command as input and based on the command, select signals according to Table 1. Pet. 53 (citing Ex. 1005 ¶¶ 28–30, 37). We are persuaded by Petitioner's showing, which we adopt, that claim 7 would have been obvious in view of LaBerge and Bhakta.

Claim 8 depends from claim 1 and recites "wherein the selection circuit comprises a multiplexer." Petitioner contends that multiplexers 230

are the claimed selection circuit, and therefore the selection circuit comprises a multiplexer. Pet. 53 (citing Ex. 1005 ¶ 37). For the reasons discussed above for claim 1, we are persuaded by Petitioner's showing, which we adopt, that claim 8 would have been obvious in view of LaBerge and Bhakta.

Claim 9 recites a control component "as claimed in claim 1," along with a plurality of semiconductor memory components, a module board, and a bus connecting each of the address terminals of the control component to the semiconductor memory components. The claim also specifies that the semiconductor memory components are arranged on the module board and to the left and right of the control component. Petitioner has accounted sufficiently for the elements of claim 9. Specifically, Petitioner shows this through LaBerge Figure 4, reproduced below, as annotated by Petitioner.

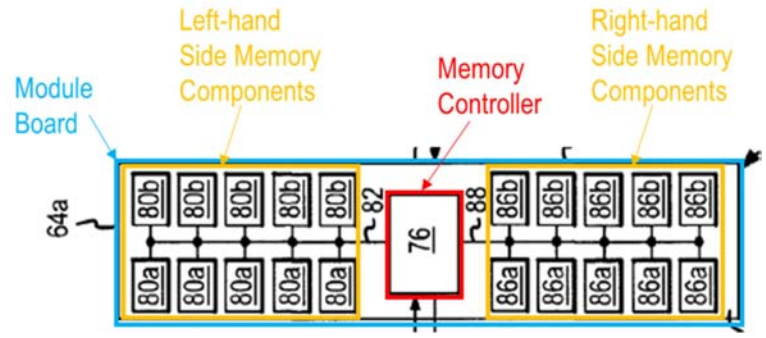


Figure 4 of LaBerge describes module board 64a with memory components (80/86) on the module board, located on both sides of memory controller 76. Pet. 54–55 (citing Ex. 1005 ¶¶ 23, 38, Fig. 4). In light of this disclosure in LaBerge, we are persuaded by Petitioner's showing, which we adopt, that claim 9 would have been obvious in view of LaBerge and Bhakta.

Claim 10 depends from claim 9 and recites "a bus connecting each of the control terminals of the control component to the semiconductor memory components" and that the semiconductor memory components "are connected to the control component via a bus connected to a second of the control terminals." Petitioner contends that LaBerge's buses 82, 88 connect terminals of memory hub 76 to the memory devices 80, 86, and that from Table 1, the terminals that supply control signals are control terminals which connect to memory devices 80, 86 over command buses 82, 88. Pet. 58 (citing Ex. 1005 ¶¶ 23, 25, 27, 30, 31). Petitioner further contends that because each of the control terminals of the memory controller are connected to the memory components over the bus, the memory components of LaBerge are connected to the memory controller via a bus connected to a second of the control terminals. Pet. 58 (citing Ex. 1003 ¶ 90). We are persuaded by Petitioner's showing, which we adopt, that claim 10 would have been obvious in view of LaBerge and Bhakta.

Claim 11 depends from claim 9 and recites "wherein a terminating resistor is arranged at a respective end of the buses." Petitioner contends that it would have been obvious to include Bhakta's activatable terminating resistors in LaBerge's memory chips. Pet. 99 (citing Ex. 1003 ¶ 191). Petitioner further contends that Bhakta's terminating resistors are arranged at a respective end of a bus because they are provided at "DQ (data input/output)" pins that are each electrically connected to the memory controller by the DQ bus. Pet. 99 (citing Ex. 1010 ¶¶ 33, 34). Petitioner argues that a person having ordinary skill in the art would have found it obvious to arrange terminating resistors at a respective end of LaBerge's buses to achieve Bhakta's goal of eliminating signal reflections at the bus-

die interface. Pet. 99 (citing Ex. 1010 ¶ 35; Ex. 1003 ¶ 191). We are persuaded by Petitioner's showing, which we adopt, that claim 11 would have been obvious in view of LaBerge and Bhakta.

Claim 14 depends from claim 9 and recites "wherein the semiconductor memory components are operated in a 4Rx4 or 4Rx8 module configuration." Petitioner contends that Bhakta describes DRAM devices with "x4" or "x8" and four-rank (4R) configurations. Pet. 100 (citing Ex. 1010 ¶¶ 8, 14, 42, 62, 90–93, 97, 99, Table 1, Fig. 11A). Petitioner further contends that because Bhakta's 4Rx4 or 4Rx8 configuration advantageously provides additional memory density, a person having ordinary skill in the art would have found it obvious to use a 4Rx4 or 4Rx8 module configuration in LaBerge. Pet. 100 (citing Ex. 1010 ¶¶ 87, 90–91, 97–100; Ex. 1003 ¶ 192). We are persuaded by Petitioner's showing, which we adopt, that claim 14 would have been obvious in view of LaBerge and Bhakta.

As explained above, Patent Owner does not make any arguments with respect to claims 7–11 and 14. *See* PO Resp.; *see also* Supp. Resp.

Claim 2

Claim 2 recites "wherein the semiconductor memory component comprises a plurality of memory chips; and wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access." Petitioner contends that Bhakta describes pairs of memory components with each pair being a virtual memory component with two memory chips (plurality of memory chips). Pet. 94 (citing Ex. 1010 ¶¶ 9, 12, 13, 29, 40, 42, and 87–93, Fig. 10A; Ex. 1003 ¶ 184). Petitioner further contends that both LaBerge and Bhakta describe select

signals for read and write access. Pet. 41–42 (citing Ex. 1005 ¶¶ 29, Table 1; Ex. 1003 ¶ 66); Pet. 95 (citing Ex. 1010 ¶¶ 30, 87, 100, 103). Petitioner contends that it would have been obvious to use Bhakta's pairs of lower-density DRAM chips in LaBerge's memory component to reduce costs or increase performance. Pet. 95 (citing Ex. 1003 ¶ 185). We agree that Bhakta meets the claimed "semiconductor memory component comprising a plurality of memory chips" because Bhakta describes a virtual memory component, which we find meets the "semiconductor memory component" with two memory chips, which we find meets the "plurality of memory chips." Pet. 94 (citing Ex. 1010 ¶¶ 9, 12, 13, 29, 40, 42, and 87–93, Fig. 10A; Ex. 1003 ¶ 184). Notwithstanding Patent Owner's arguments, which we address below, we are persuaded by Petitioner's showing explained above, which we adopt as our own, that LaBerge in combination with Bhakta describes "wherein the semiconductor memory component comprises a plurality of memory chips; and wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access."

Patent Owner argues that neither LaBerge, Bhakta, nor the combination of the two, discloses a "semiconductor memory component comprising a plurality of memory chips." PO Resp. 25–36. Patent Owner's arguments are premised on its proposed constructions for "semiconductor memory component," "memory chips," and "wherein the semiconductor memory component comprises a plurality of memory chips," recited in claim 2. *Id*. As explained above, we adopt Petitioner's proposed broader constructions for these terms and do not adopt Patent Owner's proposed narrower constructions. During oral hearing, Patent Owner confirmed that

should we adopt Petitioner's proposed constructions and not adopt Patent Owner's proposed constructions for claim 2, then claim 2 is unpatentable based on the combination of LaBerge and Bhakta. Tr. 45:14–22.[15]

Claims 3–6

Claim 3 recites that "each of the memory chips comprises an activatable terminating resistor that is activated for write access" and that "the control unit generates a second control signal for activating the activatable terminating resistor." The present record supports the contention that Bhakta Figure 3 describes that each memory chip has a terminating resistor that is activated for write access. Pet. 96–97 (citing Ex. 1010 ¶¶ 33–36, Fig. 3; Ex. 1003 ¶¶ 188–192). Petitioner contends, with supporting evidence, that a person having ordinary skill would have found LaBerge's ODT signals applicable to the ODT pins of Bhakta's memory chips 10, 20 and that Bhakta's memory chips 10, 20 and ODT circuits 32, 34 apply to the same DDR-2 memory components used in LaBerge. Pet. 97–98 (citing Ex. 1010 ¶ 35, Fig. 3; Ex. 1003 ¶¶ 188–192). Petitioner further provides a reason to combine LaBerge with Bhakta's internal termination resistors, because a person having ordinary skill would have understood that selectively enabling/disabling termination resistors preserves signal strength on active memory component while continuing to eliminate signal

[15] In its Supplemental Response, Patent Owner argues that several of the challenges in the Petition are incomplete obviousness challenges. Supp. Resp. 13–17, 23–25. Patent Owner, however, does not make the "incomplete obviousness" type argument for the LaBerge and Bhakta challenge. *See* PO Resp. As explained above, we are persuaded that the Petitioner has shown by the preponderance of the evidence standard, that claim 2 would have been obvious based on LaBerge and Bhakta.

reflections at the bus-die interface of the inactive memory components. Pet. 98 (citing Ex. 1010 ¶ 35; Ex. 1003 ¶¶ 188–192). We are persuaded by Petitioner's showing, which we adopt, that claim 3 would have been obvious in view of LaBerge and Bhakta. As explained above, Patent Owner does not make any arguments with respect to the additional elements of claim 3. *See* PO Resp.; *see also* Supp. Resp.

Claim 4 depends from claim 2 and recites "a second selection circuit" that "supplies one of the address signals and a first of the control signals to a first of the address terminals." The claim also requires that the second selection circuit "supplies one of the address signals and a second of the control signals to a second of the address terminals." Claim 5 depends from claim 4 and recites "further comprising a third selection circuit which supplies a first of the control signals and a second of the control signals to a first of the control terminals." Claim 6 depends from claim 5 and recites "further comprising a fourth selection circuit which supplies a second of the control terminals with one of a plurality of second control signals for selecting respective different ones of the memory chips for read and write access."

Petitioner has sufficiently accounted for the second, third, and fourth selection circuits recited in respective claims 4, 5, and 6, along with their corresponding functions. Pet. 45–52. In particular, Petitioner explains, with supporting evidence, that LaBerge's multiplexers 230 include at least four multiplexers that map to the claimed selection circuits and that perform the corresponding function of the claimed selection circuit. *See, e.g.*, Pet. 52 (showing annotated LaBerge Table 1; citing Ex. 1003 ¶¶ 71–76). We have reviewed Petitioner's showing spanning pages 45 to 52 of the Petition, along

with the supporting evidence to which we are directed, and are persuaded by Petitioner's showing, which we adopt, that claims 4–6 would have been obvious in view of LaBerge and Bhakta. As explained above, Patent Owner does not make any arguments with respect to the additional elements of claims 4–6. *See* PO Resp.; *see also* Supp. Resp.

E. Asserted Obviousness Challenges based on Kinsley

Petitioner contends (1) claims 1, 2, 4, 7, and 8 are unpatentable under 35 U.S.C. § 103(a) as obvious over Kinsley and Swanson (Pet. 61–76); (2) claims 1–4, 7, and 8 are unpatentable under 35 U.S.C. § 103(a) as obvious over Kinsley, Swanson, and Stave (Pet. 100–103); and (3) claims 9, 10, and 12–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Kinsley, Swanson, Hung, and Holman (Pet. 76–85, 88–92).

1. Kinsley

Kinsley describes a method of forming a stacked memory module from a plurality of memory devices. Ex. 1006 ¶ 11. The plurality of memory devices are modified to include a logic block for decoding a plurality of chip select signals. *Id*. Figure 2 of Kinsley is reproduced below.

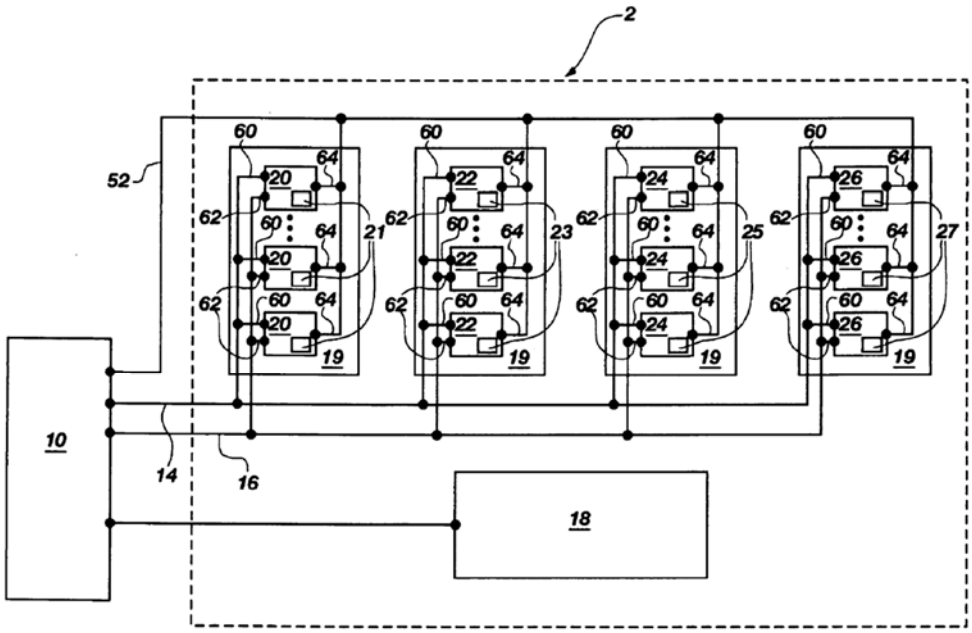


FIG. 2

Figure 2 of Kinsley shows a block diagram of a four-stacked memory module.

Kinsley describes a stacked memory module as two or more like memory devices with address, data, and power pins wired in parallel, but with the characteristic that one or more memory device may be selected for read/write operations while the other memory devices are not selected. *Id.* ¶ 25. Figure 2 shows a four-stacked memory module 2 with a first or rank one memory device 20, a second or rank two memory device 22, a third or rank three memory device 24, and a fourth or rank four memory device 26. *Id.* ¶ 28. Multiple rank one memory devices 20 are mounted on a single memory device mounting board 19, along with memory devices 22, 24, and 26. *Id.* Each of the memory devices 20, 22, 24, and 26 include a chip select pin 60 and at least one no-connect pin 62. *Id.* Chip select pins 60 are connected with a first chip select signal 14 originating from memory

controller 10. *Id*. The no-connect pins of the memory devices 20, 22, 24, and 26 are connected to a second chip select signal 16. *Id*.

Memory devices 20, 22, 24, and 26 include logic blocks 21, 23, 25, and 27 respectively that activate the respective memory device depending on the state combinations of first and second chip select signals 14 and 16. *Id*. ¶¶ 29–31. A serial presence detect device 18 is updated to indicate to memory controller 10 that memory module 2 has four stacked memory devices 20, 22, 24, and 26 and that the memory devices require two chip select signals 14 and 16 properly encoded to select any one of the four memory devices. *Id*. ¶ 33. Kinsley describes using an unused address pin 64 for receiving a third chip select signal 52. *Id*. ¶ 34.

2. Swanson

Swanson is directed to memory controllers with different signal functionality on the same pins of memory controller circuits. Ex. 1007 ¶ 1. Pins can be used to drive clock signals or chip select signals. *Id*. at Abstract. Memory controller 104 can provide either clock signals 118 or chip select signals 218 at pins 117 and 119. *Id*. ¶ 18, Figs. 1 and 2. Clock and chip select signals are preferably multiplexed. *Id*.

3. Hung

Hung describes a memory module including a printed circuit board. Ex. 1008, Abstract. Semiconductor memory devices are mounted on respective surfaces of the printed circuit board. *Id*. The memory devices are preferably DDR SDRAMs connected to each other as well as a memory controller, each of which are placed and maintained upon a single printed circuit board. *Id*. Figure 5 of Hung, annotated by Petitioner, is reproduced below.

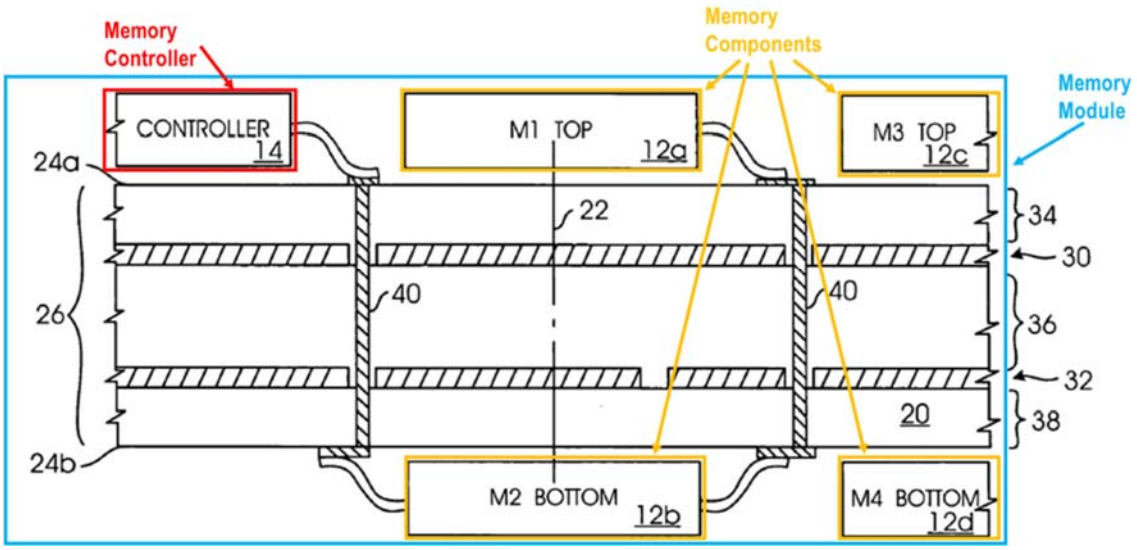


Figure 5, annotated by Petitioner, shows memory devices 12 coupled to slots of printed circuit board (PCB) 20. *Id*. at 7:13–15. By mirroring devices M1–2, a signal sent from controller 14 can be sent to both M1 and M2 with the only trace conductor difference being substantially the thickness 26 of PCB 20. *Id*. at 7:18–21.

4. Holman

Holman describes a memory module that has a plurality of memory devices and a memory module controller configured to receive a memory transaction from a first memory bus and to control access to the plurality of memory devices. Ex. 1009, Abstract. Figure 5 of Holman, annotated by Petitioner, is reproduced below.

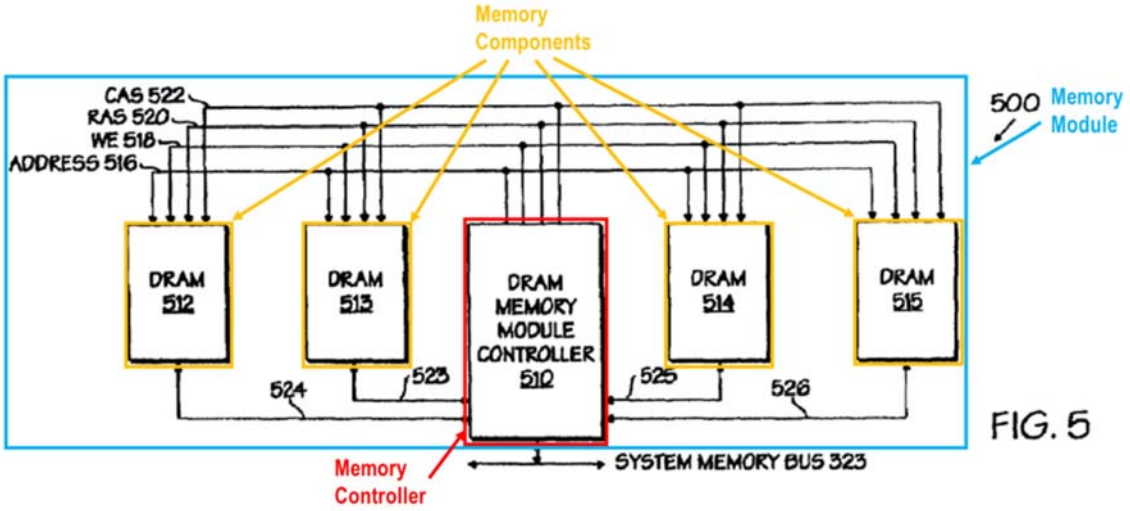


Figure 5 of Holman, annotated by Petitioner, shows a dynamic random access memory (DRAM) module including a DRAM memory module controller.

5. Stave

Stave describes a system and method to test semiconductor memory chips. Ex. 1011 ¶ 2. A memory module has a plurality of memory devices and a memory module controller is configured to receive a memory transaction from a first memory bus and to control access to the plurality of memory devices. Ex. 1009, Abstract.

6. Discussion

Claim 1

Petitioner asserts that the combination of Kinsley and Swanson describe all of the elements of claim 1. Pet. 60–69. Petitioner relies on Kinsley to meet essentially all of the recited claim 1 elements, but relies on Swanson to teach the claimed selection circuit. *Id*. at 15–16. Petitioner alternatively adds Stave to the Kinsley/Swanson combination for its specific description of addressing memory cells. Pet. 100.

Claim 1 recites "[a] control component for controlling a semiconductor memory component in a semiconductor memory module." Petitioner contends that Kinsley's memory controller 10 (control component) controls a plurality of memory devices (semiconductor memory component) in a stacked memory module. Pet. 61 (citing Ex. 1006 ¶¶ 7, 11–13, 24–26, 28, 29, 32–39; Ex. 1003 ¶ 106).

Claim 1 further recites "a control unit for generating control signals for controlling read and write access to the semiconductor memory component and for generating address signals for addressing memory cells in the semiconductor memory component for read and write access." Petitioner contends that Kinsley's memory controller 10 generates a plurality of chip select signals that provide control of stacked DRAM devices and that the chip select signals select memory device rank for reading and writing operations. Pet. 62–63 (citing Ex. 1006 ¶¶ 5, 7, 9, 11–13, 25, 28, 34, and 36–38; Ex. 1003 ¶¶ 109–110). We find that Kinsley describes generating address signals because Kinsley's memory devices have address pins and recite address signals from memory controller 10. *Id*. Petitioner contends that Kinsley's memory controller 10 includes "a high order . . . address pin such as trace A15," and that by describing trace "A15" as a "high order" address pin, Kinsley suggests existence of lower order address pins used to provide lower order address signals. Pet. 62–63 (citing Ex. 1006 ¶ 34; Ex. 1003 ¶ 110). Petitioner further contends that a person having ordinary skill in the art would have understood that using address signals A0–A15 was a well-known technique for addressing DRAM devices disclosed by Kinsley. *Id*. Petitioner also contends that Swanson's memory controller also

generates control and address signals. Pet. 63 (citing Ex. 1007 ¶¶ 12, 16, and 17; Ex. 1003 ¶ 111).

Alternatively, Petitioner relies on Stave for addressing memory cells. Pet. 100. In particular, Petitioner contends that Stave's memory chips each include a plurality of memory cells arranged in rows and columns to store data in rows and columns. Pet. 101 (citing Ex. 1011 ¶¶ 4–7). Petitioner further contends that to perform memory read/write operations, row decode circuit 28 and column decode circuit 30 select rows and columns in memory cells 26 in response to decoding an address, provided on the address bus 17, which communicates address signals such that data to/from memory cells is then transferred over data bus 18. *Id*. Petitioner argues that a person having ordinary skill in the art would have found it obvious to use Stave's memory chips with memory cells in Kinsley/Swanson, where address signals address memory cells for read and write access. Pet. 101 (citing Ex. 1003 ¶ 201). We are persuaded by Petitioner's showing and agree that Kinsley and Swanson with or without Stave meet the claimed phrase of "a control unit for generating control signals for controlling read and write access to the semiconductor memory component and for generating address signals for addressing memory cells in the semiconductor memory component for read and write access."

Claim 1 recites "a plurality of address terminals for providing the address signals." Petitioner contends that Kinsley's memory devices have address pins that receive address signals from memory controller 10. Pet. 64 (citing Ex. 1006 ¶¶ 5, 9, 25, 32, and 34; Ex. 1003 ¶ 114). We agree with Petitioner's showing.

Claim 1 also recites "a selection circuit for supplying one of the address terminals with a selected signal selected between one of the address signals and one of the control signals." Petitioner contends that Kinsley describes utilization of an unused address pin that is used to transmit either an A15 address signal or a chip select signal (CS). Pet. 65–66 (citing Ex. 1006 ¶ 34; Ex. 1003 ¶ 117). Petitioner argues that Kinsley fails to provide details in circuitry used to perform the selection between A15 or CS, but that a person having ordinary skill in the art would have been motivated to use Swanson's multiplexer 302 to perform the selection. Pet. 67–69 (citing Ex. 1007 ¶¶ 1, 2, 4, 6, 11, 14–18; Ex. 1003 ¶ 119). We are persuaded by Petitioner's showing and agree that a person having ordinary skill in the art would have been motivated to use Swanson's multiplexer circuit to achieve the selectable pin functionality described by Kinsley, as such a modification would have achieved the goals of both Kinsley and Swanson to leverage unused pins to provide additional chip select signals. Pet. 69 (citing Ex. 1003 ¶ 121).

Based on the record before us, we are persuaded by Petitioner's showing, which we adopt as our own, that claim 1 would have been obvious in view of Kinsley and Swanson, with or without Stave. As explained above, Patent Owner does not make any arguments with respect to claim 1. *See* PO Resp.; *see also* Supp. Resp.

Claims 7 and 8

Claims 7 and 8 depend from claim 1. As explained above, we determine that Petitioner has shown by a preponderance of the evidence that claims 7 and 8 would have been obvious in view of LaBerge and Bhakta. Patent Owner does not contest the unpatentability of claims 7 and 8.

Accordingly, we need not and do not decide whether Petitioner has shown by a preponderance of the evidence that claims 7 and 8 would have been obvious based on Kinsley and Swanson, with or without Stave.

Claims 9, 10, and 12–14

Claim 9 depends directly from claim 1. Claims 10, 12, and 14 depend directly from claim 9. Claim 13 depends directly from claim 12. Petitioner contends that claims 9, 10, and 12–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Kinsley, Swanson, Hung, and Holman (Pet. 76–85, 88–92).

Claim 9 recites "[a] semiconductor memory module, comprising." Petitioner contends that any of Kinsley, Swanson, Hung, and Holman describe a semiconductor memory module. Pet. 76. Claim 9 further recites "a control component as claimed in claim 1." Petitioner argues that the "memory controller of Kinsley/Swanson is not located on a memory module." Pet. 77. Petitioner relies on Hung to show "a memory controller mounted on the memory module." *Id*. (citing Ex. 1008, 2:52–55, FIG. 5; Ex. 1003 ¶ 144). Petitioner contends that Hung would have motivated a person having ordinary skill in the art to locate the memory controller of Kinsley/Swanson on a memory module to optimize inter-memory and controller-to-memory routing lengths. Pet. 78 (citing Ex. 1003 ¶ 145).

Claim 9 further recites "a plurality of semiconductor memory components." Petitioner contends that each of Hung and Holman include a memory controller and a plurality of semiconductor memory components. Pet. 79 (citing Ex. 1008, 7:13–31; Ex. 1009, 7:32–49; Ex. 1003 ¶ 147). Claim 9 further recites "a module board on which the control component and the plurality of semiconductor memory components are arranged such that

the plurality of semiconductor memory components are arranged on a left-hand and a right-hand side of the control component." Petitioner relies on the combination of Hung and Holman to meet this limitation. In particular, Petitioner contends that Figures 5 of Hung and Holman (both annotated by Petitioner above) describe a module board (PCB) on which the control component and plurality of semiconductor memory components are arranged. Pet. 80 (citing Ex. 1008, Abstract, 2:22–65, 4:52–64, 7:13–31, 9:11–44, Fig. 5; Ex. 1009, Abstract, 1:35–47, 2:62–64, 3:39–64, 4:36–52, 5:34–40, 7:32–49, FIG. 5; Ex. 1003 ¶ 148).

Petitioner contends that a person having ordinary skill in the art would have been motivated by Hung to locate the memory controller of Kinsley/Swanson on a memory module and in doing so, the person would have had a finite number of options to consider in locating the controller on the module, including left, right, or center of the memory components. Pet. 81–82 (citing Ex. 1003 ¶ 149). Petitioner contends that Holman describes the arrangement of locating the memory controller in the middle of memory components and that a person having ordinary skill would have understood that such an arrangement promotes Hung's goal of optimizing and matching controller-to-memory routing lengths. Pet. 82 (citing Ex. 1009, Abstract, 2:62–64, 3:39–64, 4:36–52, 5:34–40, 7:32–49, FIG. 5; Ex. 1008, 2:61–65; Ex. 1003 ¶¶ 149–150).

Claim 9 further recites "a bus connecting each of the address terminals of the control component to the semiconductor memory components." Petitioner sufficiently accounts for this limitation. For example, Petitioner contends that Hung's first and second memory devices share the same address bus such that whatever address signals are sent to and

from the memory controller, arrive at the top and bottom memory devices. Petitioner contends that because Hung's memory devices receive address signals from memory controller over an address bus, Hung's memory module includes a bus connecting each of the address terminals of the control component to the semiconductor memory components. Pet. 83 (citing Ex. 1008, 3:4–26, 7:13–31; Ex. 1003 ¶ 151).

Claim 9 further recites "wherein the semiconductor memory components, arranged on the left-hand and right-hand sides of the control component, are connected to the control component via a bus connected to a first of the address terminals." Petitioner sufficiently accounts for this limitation. For example, Petitioner argues that because each of the address terminals of the memory controller are connected to the memory components over the bus, the memory components of Hung and Holman are connected to the memory controller via a bus connected to a first of the address terminals. Pet. 84 (citing Ex. 1003 ¶ 154).

We are persuaded by Petitioner's showing, which we adopt as our own, that Kinsley in combination with Swanson, Hung, and Holman would have suggested the limitations of claim 9 and that the combination would have been obvious for the reasons provided by Petitioner. Patent Owner does not raise any specific arguments relating to claim 9. *See* PO Resp.; *see also* Supp. Resp.

Claim 10 depends from claim 9. As explained above, we determine that Petitioner has shown by a preponderance of the evidence that claim 10 would have been obvious in view of LaBerge and Bhakta. Patent Owner does not contest the unpatentability of claim 10. Accordingly, we need not and do not decide whether Petitioner has shown by a preponderance of the

evidence that claim 10 would have been obvious based on Kinsley, Swanson, Hung, and Holman.

Claim 12 depends from claim 9 and claim 13 depends from claim 12. Claims 12 and 13 are directed to a memory circuit that stores a configuration state based on ranks arranged on the semiconductor memory module. Petitioner contends that Kinsley includes a serial presence detect device 18 that indicates to memory controller 10 how many ranks exist on stacked memory module 4 and how many chip select signals are required. Pet. 88–89 (citing Ex. 1006 ¶¶ 26, 33, 34, 39, 43). Petitioner further contends that Kinsley's device 18 stores this configuration state using an electrically erasable programmable read-only memory ("EEPROM") located on one of the dual inline memory modules ("DIMMs"). Pet. 89 (citing Ex. 1006 ¶¶ 33, 43; Ex. 1003 ¶ 163). We agree with Petitioner that Kinsley includes a memory circuit for storing a configuration state based on ranks arranged on the semiconductor memory module. Pet. 89 (citing Ex. 1003 ¶ 164). We have further reviewed and agree that Kinsley combined with Swanson teaches that the "control circuit controls the selection circuit based on the configuration state stored in the memory circuit, such that one of the signals supplied to the selection circuit is selected" as claimed in claim 12. Pet. 89–92 (citing Ex. 1006 ¶¶ 26, 33, 34, 39, 43, Fig. 2; Ex. 1007 ¶¶ 6, 19, Claim 1; Ex. 1003 ¶¶ 165–169). Claim 13 recites "wherein the memory circuit is an electrically programmable memory." As stated above, Kinsley describes an electrically erasable programmable read-only memory ("EEPROM") located on one of the dual inline memory modules ("DIMMs"). Pet. 92 (citing Ex. 1006 ¶¶ 33, 43; Ex. 1003 ¶ 170).

We are persuaded by Petitioner's showing, which we adopt as our own, that Kinsley in combination with Swanson, Hung, and Holman would have suggested the limitations of claims 12 and 13 and that the combination would have been obvious for the reasons provided by Petitioner. Patent Owner does not raise any specific arguments relating to claims 12 and 13. *See* PO Resp.; *see also* Supp. Resp.

Claim 14 depends from claim 9. As explained above, we determine that Petitioner has shown by a preponderance of the evidence that claim 14 would have been obvious in view of LaBerge and Bhakta. Patent Owner does not contest the unpatentability of claim 14. Accordingly, we need not and do not decide whether Petitioner has shown by a preponderance of the evidence that claim 14 would have been obvious based on Kinsley, Swanson, Hung, and Holman.

Claims 2–4

Claim 2 recites "wherein the semiconductor memory component comprises a plurality of memory chips; and wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access." Petitioner contends that Kinsley's "stacked memory module" (semiconductor memory component) with memory devices physically stacked on top of each other in different ranks (memory chips) meets "the semiconductor memory component comprises a plurality of memory chips" phrase. Pet. 70 (citing Ex. 1006 ¶¶ 4, 5–11, 25, 28, 35, Fig. 2; Ex. 1007 ¶¶ 6, 19, Claim 1; Ex. 1003 ¶¶ 165–169). Petitioner further contends that Kinsley's memory controller generates chip select signals that select memory device rank for reading and writing operations. Pet. 70–71 (citing Ex. 1006 ¶¶ 6, 25, 34; Ex. 1003 ¶ 124).

Notwithstanding Patent Owner's arguments, which we address below, we are persuaded by Petitioner's showing explained above, which we adopt as our own, that Kinsley in combination with Swanson, with or without Stave, describes "wherein the semiconductor memory component comprises a plurality of memory chips; and wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access."

Both parties agree that "one solution" for memory stacking taught by Kinsley is disclosed in figure 2 of a related patent referenced in paragraph 8 of Kinsley. Supp. Resp. 27; Supp. Reply 7. Figure 2 of the related patent is reproduced below.

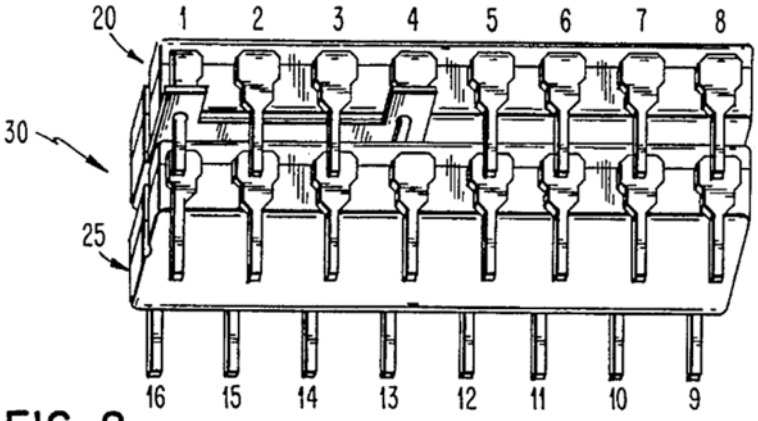


FIG. 2

Figure 2 from Exhibit 2001 shows a plurality of stacked chips.

Exhibit 2001 describes that top chip 20 is placed on bottom chip 25. Ex. 2001, 4:66–67. We find that Kinsley describes stacked chips like the ones described in figure 2 of Exhibit 2001, shown above. We further find that Kinsley's "stacked memory module" that includes stacked chips is a semiconductor memory component. Ex. 1006 ¶¶ 4, 5–11, 25, 28, 35.

Patent Owner agrees that Kinsley teaches multiple packaged memory ICs stacked on top of each other over the same area on a memory

module/board, like the ones shown above. Supp. Resp. 27. Patent Owner argues that Kinsley, however, does not teach a plurality of *dies stacked together in the same package*. *Id*. Rather, according to Patent Owner, Kinsley describes individual packaged devices stacked on top of each other. *Id*. Patent Owner's arguments are premised on its proposed constructions for "semiconductor memory component," "memory chips," and "wherein the semiconductor memory component comprises a plurality of memory chips," recited in claim 2. *Id*. at 7, 27. As explained above, we adopt Petitioner's proposed broader constructions for these terms and do not adopt Patent Owner's proposed narrower constructions.

Claim 3 recites that "each of the memory chips comprises an activatable terminating resistor that is activated for write access" and that "the control unit generates a second control signal for activating the activatable terminating resistor." Petitioner contends, and we find, that Stave's memory chips each include an on die termination ("ODT") circuit 40 that includes termination resistors RT 48–49. Pet. 101 (citing Ex. 1011 ¶¶ 4–7, 10, 12–14). Petitioner further contends, and we find, that during a memory write operation to one of the chips 12, Stave's ODT circuit 40 in the other chip (which is not receiving data) is activated to absorb any signal propagations or reflections received on the lines of that inactive chip, and thus, Stave's memory chips include an activatable terminating resistor that is activated for write access. Pet. 101–102 (citing Ex. 1011 ¶ 13; Ex. 1003 ¶ 202). Petitioner provides reasons for adding Stave's on-chip ODT circuit in the memory chips of Kinsley/Swanson and we agree that a person having ordinary skill in the art would have been motivated to apply Stave's ODT circuit 40 to the memory chips in Kinsley/Swanson to improve signal

integrity. Pet. 102–103 (citing Ex. 1011 ¶¶ 4–7, 12–14, 41, 43; Ex. 1003 ¶ 203). We are persuaded by Petitioner's showing, which we adopt, that claim 3 would have been obvious in view of Kinsley, Swanson, and Stave. As explained above, Patent Owner does not make any arguments with respect to the additional elements of claim 3. *See* PO Resp.; *see also* Supp. Resp.

Claim 4 depends from claim 2 and recites "a second selection circuit" that "supplies one of the address signals and a first of the control signals to a first of the address terminals." The claim also requires that the second selection circuit "supplies one of the address signals and a second of the control signals to a second of the address terminals." Petitioner contends, and we agree, that Swanson's memory controller includes two multiplexers (two selection circuits) to provide additional chip select signals. Pet. 71 (citing Ex. 1007 ¶¶ 6, 10, 19; Ex. 1003 ¶ 126). Petitioner provides reasoning with rational underpinnings for utilizing Swanson's second selection circuit to provide address and control signals as claimed. Pet. 72–73 (citing Ex. 1006 ¶¶ 5, 7, 9, 25, 41; Ex. 1007 ¶¶ 6, 11, 17, 21; Ex. 1003 ¶¶ 127–129). We are persuaded by Petitioner's showing, which we adopt, that claim 4 would have been obvious in view of Kinsley and Swanson with or without Stave. As explained above, Patent Owner does not make any arguments with respect to the additional elements of claim 4. *See* PO Resp.; *see also* Supp. Resp.

F. Remaining Grounds Challenging the Claims of the '993 Patent

For the reasons discussed above, Petitioner has shown, by a preponderance of the evidence that all challenged claims 1–14 of the '993 patent are unpatentable. In particular, Petitioner has shown, by a

preponderance of the evidence that (1) claims 1–11 and 14 would have been obvious based on LaBerge and Bhakta; (2) claims 1, 2, and 4 would have been obvious based on Kinsley and Swanson, with or without Stave; (3) claims 9, 12, and 13 would have been obvious based on Kinsley, Swanson, Hung, and Holman; and (4) claim 3 would have been obvious based on Kinsley, Swanson, and Stave. In addressing these grounds, we have addressed all challenged claims. *See SAS*, 138 S. Ct. at 1359 (holding that a petitioner "is entitled to a final written decision addressing all of the claims it has challenged"); *see also* 35 U.S.C. § 318(a). Accordingly, we need not and do not decide whether Petitioner has shown by a preponderance of the evidence that claims 1–10 also would have been obvious based on LaBerge alone; whether claims 1, 2, 4, 7, and 8 would have been obvious based on Ajanovic alone; or whether claims 1–4, 7, and 8 would have been obvious based on Ajanovic and Stave.[16] *Cf. In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009) (not reaching other grounds of unpatentability after affirming the anticipation ground); *see also Beloit*

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[16] Our decision is based on Petitioner's proposed constructions for "semiconductor memory component" and "plurality of chips." Petitioner argues in its Reply that "even if Polaris's construction were correct (which it's not), Ajanovic still discloses the disputed limitation." Supp. Reply 11. As pointed out by Patent Owner during oral hearing, Petitioner "never made the argument that it would have been obvious to modify these references to bring it within the scope of our proffered claim construction." Tr. 54:6–16. We agree with Patent Owner that Petitioner did not explain with sufficient supporting evidence why it would have been obvious to replace any of the memory components of the prior art with a "discrete, packaged semiconductor memory device ha[ving] a plurality of single memory IC die within the same package." PO Resp. 22. Accordingly, we need not and do not consider the challenges based on Ajanovic, because those challenges appear redundant, if not inferior to, the challenges decided. Tr. 6:23–7:24.

Corp. v. Valmet Oy, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (once a dispositive issue is decided, there is no need to decide other issues).

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–14 of the '993 patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–14 of the '993 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2017-00901
Patent 7,405,993 B2

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Paper 54
Entered: January 14, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE OFFICE OF THE UNDERSECRETARY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

NVIDIA CORPORATION,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2017-00901 (Patent 7,405,993 B2)
IPR2017-01500 (Patent 6,532,505 B1)

Before ANDREW HIRSHFELD, *Commissioner for Patents, Performing the Functions and Duties of the Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office*.

ORDER

The Office has received a request for Director review of the Final Written Decision in each of the above-captioned cases. *See, e.g.*, IPR2017-00901, Ex. 3100. The requests were referred to Mr. Hirshfeld, Commissioner for Patents, Performing the Functions and Duties of the Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office.

It is ORDERED that the request for Director review in each case is denied; and

FURTHER ORDERED that the Patent Trial and Appeal Board's Final Written Decision in each case is the final decision of the agency.

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