UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD.,
Petitioner,

v.

ANALOG DEVICES, INC.,
Patent Owner.

Case No. IPR2020-01219
U.S. Patent No. 8,487,659

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141-144 and 319, and 37 C.F.R. § 90.2-90.3, notice is hereby given that Patent Owner, Analog Devices, Inc., appeals to the U.S. Court of Appeals for the Federal Circuit from the Final Written Decision entered January 10, 2022 (Paper 39) in IPR2020-01219, attached as Exhibit A, and all prior and interlocutory rulings related thereto or subsumed therein.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner indicates that the issues on appeal include, but are not limited to:

i. whether the Board erred in determining that Yoshioka is prior art to the ’659 patent;

ii. the Board’s determination that claims 5, 6, and 9 are anticipated by Yoshioka;

iii. the Board’s determination that claim 10 is obvious over Yoshioka;

iv. whether the Board erred in relying on applicant admitted prior art (“AAPA”) that improperly formed the basis of Petitioner’s challenges;

v. the Board’s determination that claims 1 and 2 are obvious over Yoshioka and AAPA;

vi. the Board’s determination that claims 7 and 8 are obvious over Yoshioka and Fiscus;

vii. the Board’s determination that claims 3 and 4 are obvious over Yoshioka, AAPA, and Fiscus;

viii. the Board's determination that claims 9–11 are anticipated by Ajit;

ix. the Board's determination that claims 1 and 5 are obvious over Ajit and AAPA;

x. any further findings or determinations by the Director or the Board supporting or relating to the issues above; and

xi. all other issues decided adversely to Analog Devices or the '659 patent in any order, decisions, rulings, or opinions, whether written or oral, of the Board, on its own or on another's behalf in this proceeding.

Pursuant to 37 C.F.R. § 90.3, this Notice of Appeal is timely, having been duly filed within 63 days after the date of the Final Written Decision.

A copy of this notice of Appeal is being filed simultaneously with the Patent Trial and Appeal Board, the clerk's Office for the United States Court of Appeals for the Federal Circuit, and the Director of the U.S. Patent and Trademark Office.

Dated: March 14, 2022

Respectfully submitted,

/Scott Bertulli/

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 90.2(a)(1) and 104.2(a), I hereby certify that, in addition to being filed electronically through the Patent Trial and Appeal Board's End to End (PTAB E2E) system, a true and correct original version of the forgoing PATENT OWNER'S NOTICE OF APPEAL is being filed by Priority Mail Express on this 14th day of March, 2022, with the Director of the Untied States Patent and Trademark Office, at the following address:

Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to 37 C.F.R. § 90.2(a)(2) and Federal Circuit Rule 15(a)(1), and Rule 52(a), (e), I hereby certify that a true and correct copy of the foregoing PATENT OWNER'S NOTICE OF APPEAL is being filed in the United States Court of Appeals for the Federal Circuit using the Court's CM/ECF filing system on this 14th day of March , 2022, and the filing fee is being paid electronically using pay.gov.

I hereby certify that on March 14, 2022, I caused a true and correct copy of the PATENT OWNER'S NOTICE OF APPEAL to be served via electronic service, to the Petitioners by serving the correspondence address of record as follows:

Xilinx-ADI-IPR@mofo.com

/Scott Bertulli/

Scott Bertulli, Reg. No. 75,886

EXHIBIT A

Trials@uspto.gov
571-272-7822

Paper 39
Entered: January 10, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC. and XILINX ASIA PACIFIC PTE. LTD.,
Petitioner,

v.

ANALOG DEVICES, INC.,
Patent Owner.

IPR2020-01219
Patent 8,487,659 B2

Before JEFFREY S. SMITH, SCOTT A. DANIELS, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Claims Unpatentable
35 U.S.C. § 318(a)

Denying Motion to Exclude
37 C.F.R § 42.64(c)

I. INTRODUCTION

A. Background and Summary

Petitioner filed a Petition requesting *inter partes* review of claims 1–11, which are all claims of U.S. Patent No. 8,487,659 B2 (Ex. 1001, the "'659 patent"). Paper 2 ("Pet."). Patent Owner filed a Response. Paper 13 ("PO Resp."). Petitioner filed a Reply. Paper 21 ("Reply"). Patent Owner filed a Sur-Reply. Paper 25 ("PO Sur-Reply). A hearing was held on October 27, 2021. A transcript of the hearing has been entered as Paper 38 ("Tr."). Petitioner filed a Motion to Exclude Evidence, which Patent Owner opposes. Papers 30, 31, 33.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). We determine that claims 1–11 are unpatentable. We deny Petitioner's Motion to Exclude Evidence.

B. Related Proceedings

The parties identify the following district court proceeding concerning the '659 patent: *Analog Devices, Inc. v. Xilinx, Inc*., No. 1:19-cv-02225-RGA (D. Del.). Pet. 91; Paper 5.

C. Real Party-in-Interest

The Petition identifies Xilinx, Inc. and Xilinx Asia Pacific Pte. Ltd. (collectively, "Petitioner") as Real Parties-in-Interest. Pet. 91. Patent Owner identifies itself as the Real Party-in-Interest. Paper 5.

D. The '659 Patent

The '659 patent discloses an adaptive delay device that provides a delay to a signal based on variations of circuit properties and conditions such as fabrication process, supply voltage, or temperature (PVT). Ex. 1001,

code [57], 1:5–8. The adaptive delay device is incorporated into a comparator to provide adaptive timing. *Id.* at code [57]. Figure 3 below illustrates a comparator with an adaptive delay. *Id.* at 3:1.

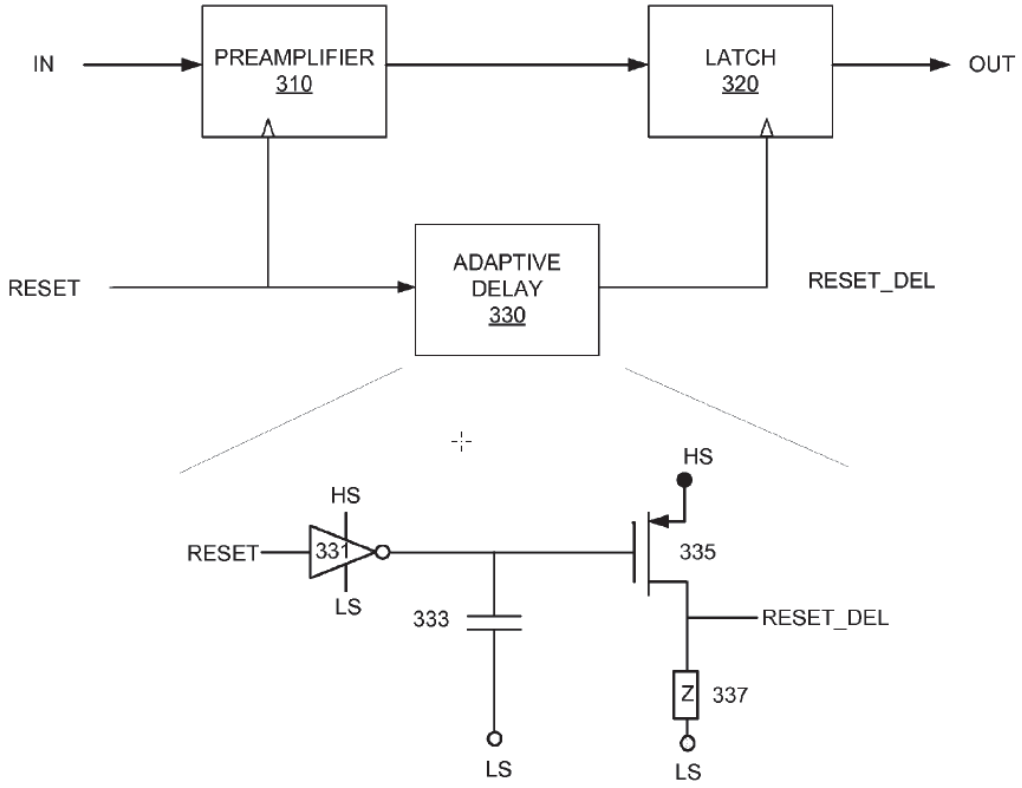


FIG. 3

Figure 3 above shows comparator 300 including preamplifier 310, latch 320, and adaptive delay element 330. Ex. 1001, 3:1–4. Adaptive delay element 330 has a circuit structure that inverts the PVT effects that occur in preamplifier 310 and latch 320. *Id.* at 3:19–22. Thus, if the switches of preamplifier 310, latch 320, and adaptive delay element 330 operate faster in response to PVT effects such as decreased temperature or increased supply voltage, the adaptive delay element adds a delay to counteract the PVT effects and stabilize throughput of comparator 300. *Id.* at 3:22–29.

E. Illustrative Claim

The '659 patent has 11 claims, all of which are challenged in the Petition. Device claims 1 and 5, and method claim 9, are the independent claims. Claim 5 is illustrative:

> 5. A successive approximation register analog-to-digital converter on an integrated circuit chip configured with a plurality of on-chip circuit components, comprising:
>
> a comparator for determining whether an input signal is representative of a digital high or low signal; and
>
> an adaptive delay device having an input for receiving a control signal and an output connected to the comparator,
>
> wherein the adaptive delay device is configured to respond inversely to the response of other circuit components forming the successive approximation register analog-to-digital converter, and output the control signal to the comparator based on the inverse response of the adaptive delay device.

F. Level of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art would have at least a Bachelor of Science degree in electrical engineering with either two years of experience in circuit design, or three to four years of experience in circuit design. Pet. 14 (citing Ex. 1002 ¶¶ 28–30). Patent Owner does not address the level of ordinary skill in its Response. *See generally* PO Resp. Patent Owner's declarant, Dr. Pavan Hanumolu, testifies that Petitioner's proposed level of education and experience for a person of ordinary skill is reasonable. Ex. 2001 ¶ 10.

For purposes of this decision, we adopt Petitioner's formulation because it is consistent with the '659 patent and the asserted prior art and not disputed by Dr. Hanumolu.

G. Claim Construction

For *inter partes* reviews filed on or after November 13, 2018, we apply the same claim construction standard used by district courts and the ITC, both of which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 83 Fed. Reg. 51340 (Oct. 11, 2018). Because the instant Petition was filed on July 17, 2020, we apply that standard here. Accordingly, we construe each challenged claim of the '250 patent to generally have "the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b).

We construe claim terms to the extent necessary for our analysis on whether to institute a trial. *See, e.g.*, *Nidec Motor Corp. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Petitioner states it "does not believe any claim construction is necessary here." Pet. 14. Patent Owner agrees "the terms of the challenged claims can be understood based on their plain and ordinary meanings." PO Resp. 10. We find there is no need to explicitly construe any claim terms.

H. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 15):

Claims Challenged	35 U.S.C. §[1]	Reference(s)/Basis
5, 6, 9	102(a)	Yoshioka[2]
10	103	Yoshioka
1, 2	103	Yoshioka, Applicant's Admitted Prior Art (AAPA)
7, 8	103	Yoshioka, Fiscus[3]
3, 4	103	Yohioka, AAPA, Fiscus
9–11	102(b)	Ajit[4]
1, 5	103	Ajit, AAPA

II. ANALYSIS

A. Anticipated by Yoshioka (Claims 5, 6, 9)

1. Overview of Yoshioka (Ex. 1004)

Yoshioka discloses a system-on-a-chip with an analog-to-digital converter (ADC) that includes an internal clock Φ_c to compensate for PVT variations. Ex. 1004, 18. The internal clock is generated by a loop, which includes a comparator and an internal clock generator that has a delay controller, as shown in Figure 8 below. *Id.* at 22.

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103, effective March 16, 2013. Because the application from which the '659 patent issued was filed before this date, the pre-AIA version of §§ 102, 103 applies.
[2] Masato Yoshioka, et al., *A 10-b 50-MS/s 820-μW SAR ADC With On-Chip Digital Calibration*, IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, VOL. 4, NO. 6 (2010) (Ex. 1004).
[3] U.S. Patent No. 6,628,558 B2, issued Sept. 30, 2003 (Ex. 1006).
[4] U.S. Patent No. 7,268,595 B2, issued Sept. 11, 2007 (Ex. 1005).

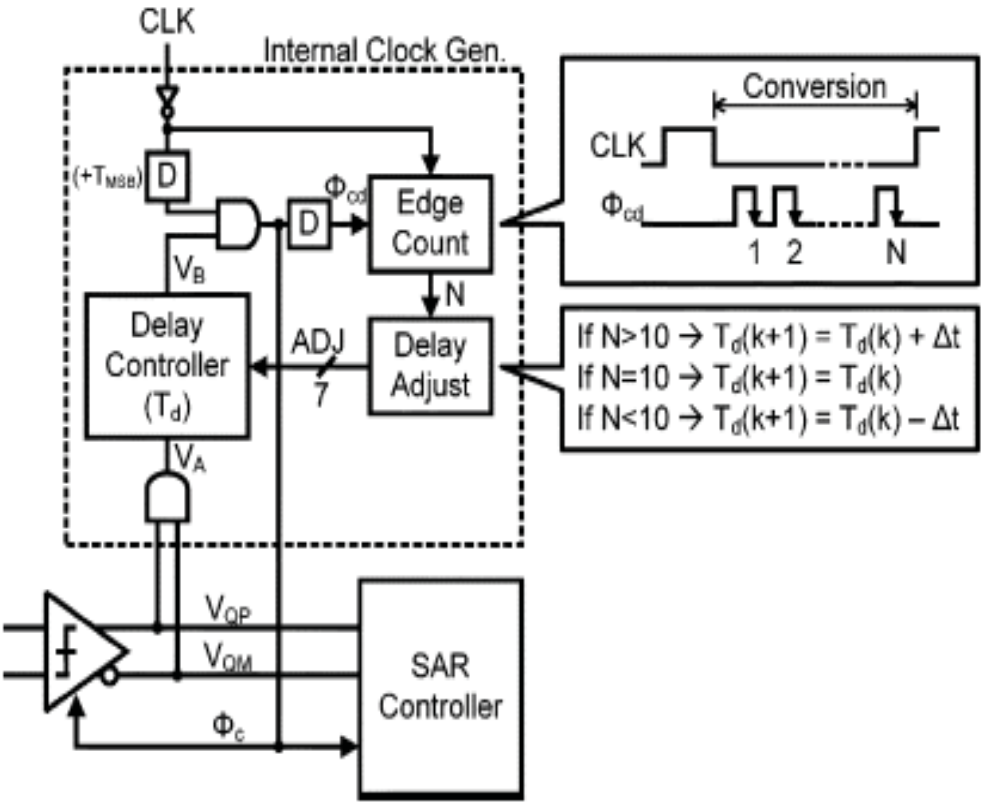


Fig. 8. T_d control implementation.

Figure 8 above shows the comparator, the internal clock generator, and an algorithm to adjust the delay T_d to compensate for PVT variations. *Id.* The internal clock generator adjusts the delay within a conversion period delivered by the external clock CLK. *Id.* The delay is calibrated to make the number of internal cycles during the conversion period N equal to 10, in order for the comparator to make ten comparisons in this period. *Id.*; *see id.* at 19. The internal clock generator counts the internal clock cycles using the transition point of the comparator as it starts to reset. *Id.* The delay T_d is made longer if N is greater than 10, and shorter if N is less than 10. *Id.* The delay is chosen so that all PVT conditions can be covered. *Id.*

2. Claims 5, 6, and 9

Petitioner, relying on the testimony of Dr. Douglas Holberg, contends that claims 5, 6, and 9 are anticipated by Yoshioka. Pet. 16–37; Ex. 1002. Patent Owner contends that Yoshioka is not prior art to the '659 patent, and that Yoshioka does not disclose a delay element that is configured to adjust its delay inversely in response to the PVT effects on other components. PO Resp. 10–57.

The preamble of claim 5 recites a "successive approximation register analog-to-digital converter on an integrated chip configured with a plurality of on-chip circuit components." Petitioner contends Figure 1 of Yoshioka discloses this limitation in showing a block diagram of a successive approximation register analog-to-digital converter configured with several on-chip circuit components. Pet. 21 (citing Ex. 1004, Abstract, Fig. 1).

Claim 5 recites "a comparator for determining whether an input signal is representative of a digital high or low signal." Petitioner contends Figure 1 of Yoshioka shows this limitation. Pet. 22–23 (citing Ex. 1004, Fig. 1, 18–19; Ex. 1002 ¶ 55).

Claim 5 recites "an adaptive delay device having an input for receiving a control signal and an output connected to the comparator." Petitioner contends Figure 3 of Yoshioka shows this limitation. Pet. 23–24 (citing Ex. 1004, Fig. 3).

Claim 5 recites "wherein the adaptive delay device is configured to respond inversely to the response of other circuit components forming the successive approximation register analog-to-digital converter, and output the control signal to the comparator based on the inverse response of the adaptive delay device." Petitioner contends Yoshioka discloses this

limitation in describing a delay controller that implements an algorithm that increases the delay when PVT conditions cause the circuit to run faster, and decreases the delay when PVT conditions cause the circuit to run slower. Pet. 24–26 (citing Ex. 1004, Figs. 3, 8, Abstr., 22; Ex. 1002 ¶¶ 58–60).

Whether Yoshioka is Prior Art[5]

Patent Owner contends that Yoshioka is not prior art because the inventor of the '659 patent conceived of the invention prior to Yoshioka's publication date and diligently reduced it to practice. PO Resp. 10. Patent Owner contends that the invention was conceived on July 20, 2010, as shown by a Design Review document that describes components of the invention (Ex. 2006), and was also conceived also on October 29, 2010, as shown by schematic diagrams produced by the inventor Mr. Kapusta (Exs. 2015, 2016, 2017) for a circuit embodying the invention. PO Resp. 12 (citing Ex. 2006), 17 (citing Ex. 2006; Ex. 2015; Ex. 2016; Ex. 2017).

Patent Owner contends that the inventor showed diligence by finalizing the schematic diagrams and checking the schematic diagrams into a revision management system on October 29, 2010. PO Resp. 34–36. Patent Owner contends that the inventor showed diligence by performing a standard test, generating a tapeout file for a sample chip, and sending the tapeout file to a manufacturer on November 9, 2010; receiving sample chips from the manufacturer on January 13, 2011; and completing tests of the sample chips by February 1, 2011. PO Resp. 37–40. Patent Owner contends

[5] Although this section of the decision includes an analysis of the anticipation ground against independent claims 5, 9, and dependent claim 6, Yoshioka is also asserted in other grounds against independent claim 1 and dependent claims 2, 3, 4, 7, and 8. Therefore, our determination that Yoshioka is prior art applies to all grounds that rely on Yoshioka.

that the invention was reduced to practice on January 13, 2011. PO Resp. 39.

Because Patent Owner relies on both the Design Review and the schematic diagrams to establish conception, and asserts that the inventor "conceived his invention no later than October 29, 2010," we determine October 29, 2010 is the asserted date of conception. PO Resp. 34, 40; *see generally* PO Resp. 12–34, 40. Because Patent Owner asserts that both conception and diligence occurred on or before October 29, 2010 (PO Resp. 12–36), and we determine that October 29, 2010 is the asserted date of conception, we determine that the activities performed by the inventor on or before October 29, 2010 show evidence of the asserted conception, not evidence of diligence. *See* PO Resp. 40 ("Mr. Kapusta conceived his invention no later than October 29, 2010 . . . and was diligent in reducing it to practice from October 29, 2010 . . . to January 12, 2011.").

Conception Each of independent claims 1, 5 and 9 requires a delay element that is configured to adjust its delay inversely in response to the PVT effects on components other than the delaly element. *See* claim 1 ("the delay element having a circuit structure to adaptively increase or decrease delay propogation of the first control signal in a manner that counteracts PVT effects present in other components."), claim 5 ("the adaptive delay device is configured to respond inversely to the response of other circuit components."), claim 9 ("delays between the state change of the input signal and the generated output voltage vary inversely in response to PVT effects on other components."); PO Resp. 40 (quoting claims 1, 5, and 9).

Petitioner contends that the Design Review and schematic diagrams do not show conception, because the circuit shown in the Design Review

and schematic diagrams does not show a delay element that is configured to adjust its delay inversely in response to the PVT effects on components other than the delaly element as required by independent claims 1, 5, and 9. Reply 1–2 (citing Ex. 1018 ¶¶ 6–8). In particular, Petitioner contends that (a) the reset signal to the latch shown in the Design Review is not delayed, (b) the q_{TIMER} signal shown in Figure 8 is not a delayed reset signal, (c) the circuit components of the Design Review and schematic diagrams that are different than the components of the circuit in the '659 patent add additional proportional, rather than inverse, delays, and (d) the simulations depicted in the Design Review show that the circuit does not respond inversely to PVT effects of other components. Reply 1–17.

With respect to the reset signal, Petitioner contends that the reset signal is applied to Pre-Amp 1, Pre-Amp 2, and the Regenerative Latch at the same time, as shown in Figure 1 of the Design Review. Reply 4 (citing Ex. 1018 ¶¶ 11–12; Ex. 1016, 52:23–56:18). Petitioner contends that, as a result, there is no delay between when the reset signal is applied to the two Pre-Amps and when it is applied to the latch. Reply 4.

With respect to the q_{TIMER} signal, Petitioner contends that the q_{TIMER} signal applied to the regenerative latch, as shown in Figure 7 of the Design Review, does not correspond to the claimed second control signal, because q_{RESET}, not q_{TIMER}, controls latching by the regenerative latch. Reply 5–6 (citing Ex. 1018 ¶¶ 13–14). Petitioner contends that q_{TIMER} shown in Figure 8 of the Design Review does not correspond to RESET_DEL shown in Figure 4 of the '659 patent, because q_{TIMER} is output by an inverter, and is a delayed version of qrst_time, which is the signal that corresponds to the

RESET_DEL signal in Figure 4 of the '659 patent. Reply 6–7 (citing Ex. 1018 ¶¶ 15–17; Ex. 2044 ¶ 26).

With respect to the additional circuit components shown in the Design Review, Petitioner contends that the inverter shown in Figure 8 corresponds to two inverters followed by a NOR gate shown in Patent Owner's schematics. Reply 7 (citing Ex. 1018 ¶ 17). Petitioner contends that the two inverters and NOR gate would respond proportionally to PVT effects and would impact the overall delay of the signal. Reply 11–12 (citing Ex. 1018 ¶ 25; Ex. 2044 ¶ 26). Petitioner's declarant, Dr. Holberg, testifies that the tunable capacitor in Figure 8 of the Design Review, unlike the fixed capacitor shown in Figure 4 of the '659 patent, will affect the delay of the timer circuit. Ex. 1018 ¶ 26. Dr. Holberg testifies that the differences between Figure 4 of the '659 patent and Figure 8 of the Design Review show that the Design Review timer does not counteract PVT effects as required by the claims. Ex. 1018 ¶ 29.

With respect to the simulations, Petitioner contends that Patent Owner's simulation data shows that the Design Review circuit does not respond inversely to the response of other circuit components, as required by independent claims 1, 5, and 9. Reply 12 (citing Ex. 1018 ¶¶ 34–47). For example, Petitioner contends that a comparison of cases 63 and 67 as illustrated in Table 6 and Figure 28 of the Design Review shows a proportional relationship to PVT effects, not an inverse relationship. Reply 16–17 (citing Ex. 2006, 28, 32; Ex. 1018 ¶¶ 38–43).

In response, Patent Owner contends that q_{TIMER} corresponds to the second control signal, because it causes the latch to regenerate quickly when it goes high. PO Sur-Reply 4. Patent Owner contends that the differences

between the timer circuit shown in Figure 4 of the '659 patent and Figure 8 of the Design Review are immaterial, and not reflected in the claims. PO Sur-Reply 4–5. Patent Owner contends that even though the qrst_time3b signal is generated after the output of the circuit passes through two inverters and a NOR gate, which have a proportional response, the signal input to the inverters and NOR gate is more inverse to PVT effects in order to make up for the additional delay, causing the overall response to be inverse. PO Sur-Reply 5. Patent Owner contends that the simulations depicted in Figure 28 of the Design Review show that when comparing the response of the comparator and latch to variations in voltage, the comparator response is always inverse to the latch response. PO Sur-Reply 5–7.

We are not persuaded that Patent Owner has established that the Design Review discloses a delay element that is configured to adjust its delay inversely in response to the PVT effects on components other than the delaly element as required by independent claims 1, 5, and 9 of the '659 patent. We agree with Petitioner and Dr. Holberg, that the circuits shown in the Design Review are different than the circuits shown in the '659 patent. In particular, we agree with Dr. Holberg that the comparator architecture shown in Figure 1 of the Design Review does not include the comparator with an adaptive delay shown in Figure 3 of the '659 patent, because the pre-amplifiers and the latch shown in Figure 1 of the Design Review, unlike those shown in Figure 3 of the '659 patent, receive the reset signal at the same time. Ex. 1018 ¶¶ 10–11.

We agree with Dr. Holberg, that the timer clock generation circuit shown in Figure 8 of the Design Review, unlike the adaptive delay device shown in Figure 4 of the '659 patent, includes two inverters followed by a 3-

input NOR gate, as shown by the corresponding structure in Mr. Kapusta's schematic diagrams. Ex. 1018 ¶¶ 15–18. We agree with Dr. Holberg and Dr. Hanumolu, that the response of the two inverters and the NOR gate of the timer circuit shown in Figure 8 of the Design Review is directly proportional, not inversely proportional, to PVT effects. Ex. 1018 ¶¶ 25 (quoting Ex. 2044 ¶ 26), 29.

Further, we are not persuaded by Patent Owner's contention that the response at the signal input to the two inverters and the NOR gate of the schematic would be even more inverse to make up for the additional delay from the additional circuit elements, causing the overall response to be inversely proportional. *See* PO Sur-Reply 5. Patent Owner has not provided sufficient evidence to show that the overall response of the timer clock generation circuit is inverse. We are persuaded by Dr. Holberg's testimony that the inventor's simulation data does not show conception of a circuit that responds inversely to PVT effects, as required by the claims. Ex. 2006, 28, 32; Ex. 1018 ¶¶ 34–47. In particular, we are persuaded by the table shown in paragraph 46 of Dr. Holberg's second declaration, which compares corresponding cases from the simulation data. Ex. 1018 ¶ 46. As shown by the boxes containing an X, there are a significant number of instances of a directly proportional response, not an inversely proportional response, of the circuit in the Design Review to PVT effects. Ex. 1018 ¶ 46.

We are also not persuaded by Patent Owner's contention that the Design Review and schematic documents show conception because, according to Patent Owner, the comparator response is always inverse to the latch response when voltage varies, and voltage variations are one type of PVT effect. PO Sur-Reply 5–7. Even accepting Patent Owner's contention

that the comparator response is always inverse to that of the latch when voltage varies, showing an inverse response to a voltage effect alone does not persuasively show an inverse response to PVT effects, which include process and temperature effects, in addition to the voltage effect. Patent Owner has not persuasively shown a delay element that is configured to adjust its delay inversely in response to the PVT effects on components other than the delaly element as required by independent claims 1, 5, and 9 of the '659 patent.

Patent Owner further contends that adjusting delay due only to the effect of voltage is consistent with Petitioner's grounds, because, according to Patent Owner, Dr. Holberg admits that under some variations in PVT conditions, Yoshioka does not make any delay adjustments. PO Sur-Reply 7, n. 1 (citing Ex. 2047, 38:23–41:12). However, Dr. Holberg, when asked whether Yoshioka "could have a variation, for example, in temperature or voltage that would not cause it to tip over into a different number of cycles," answered "I guess within the resolution of the control, which I think is about 3.78 picoseconds, so . . . that's a quanitization that . . . you can live with." Ex. 2047, 41:3–12. Contrary to Patent Owner's contention, Dr. Holberg did not testify that Yoshioka adjusts delay due to the effect of voltage alone. Rather, Dr. Holberg testified that Yoshioka adjusts delay due to PVT effects within a quantization of 3.78 picoseconds, which would be acceptable to a person of ordinary skill in the art. Ex. 2047, 20:9–16, 21:16–18; Ex. 1002 ¶¶ 57–60; Ex. 1018 ¶¶ 57–67.

Patent Owner further contends that Petitioner's Reply barely addresses Patent Owner's evidence of conception based on the schematics. PO Sur-Reply 7–8. We do not agree. Petitioner and Dr. Holberg have

provided contentions and persuasive evidence to show that the additional components in the schematic diagrams that are not present in the '659 patent would respond proportionally to PVT effects, and that Patent Owner has not shown that the overall delay would be inversely proportional to PVT effects. Reply 11–12; Ex. 1018 ¶¶ 25, 29.

We agree with Dr. Holberg that the evidence provided by Patent Owner does not show that the inventor conceived of a a delay element that is configured to adjust its delay inversely in response to the PVT effects on components other than the delaly element as required by independent claims 1, 5, and 9 of the '659 patent on October 29, 2010. Ex. 1018 ¶¶ 28, 31–32, 34–47. Therefore, we find that the Design Review and schematic documents do not show that the "inventor must have formed in his or her mind a definite and permanent idea of the complete and operative invention, as it is hereafter to be applied in practice." *Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1577 (Fed. Cir. 1996); *Burroughs Wellcome Co. v. Barr Labs, Inc.*, 40 F.3d 1223, 1228 (Fed. Cir. 1994).

Diligence

Even if Patent Owner showed conception, Patent Owner has not shown diligence. The person "who first conceives . . . may date his patentable invention back to the time of its conception, if he connects the conception with its reduction to practice by reasonable diligence on his part, so that they are substantially one continuous act." *Mahurkar*, 79 F.3d at 1577. "Issues of diligence concern the period just preceding the effective date of the adverse reference, to the actual or constructive reduction to practice." *In re Steed*, 802 F.3d 1311, 1317 (Fed. Cir. 2015); *Mahurkar*, 79 F.3d at 1578 (The inventor "must demonstrate reasonable diligence toward

reduction to practice from a date just prior to [the effective date of the reference] to it's reduction to practice."). "An inventor's testimony regarding his reasonable diligence must be corroborated with evidence." *ATI Technologies ULC v. Iancu*, 920 F.3d 1362, 1370 (Fed. Cir. 2019) (citing *Perfect Surgical Techniques, Inc. v. Olympus Am., Inc.*, 841 F.3d 1004, 1006 (Fed. Cir. 2016).

Patent Owner contends that the inventor "conceived his invention no later than October 29, 2010." PO Resp. 40. Patent Owner contends that the inventor showed diligence on November 9, 2010 by performing a standard test, generating a tapeout file for a sample chip, and sending the tapeout file to a manufacturer. PO Resp. 37; *see id.* at 11–12. However, November 9, 2010 is the publication date of Yoshioka, which is also Yoshioka's effective date. Ex 1004, 18. The date "just preceding the effective date of the [Yoshioka] reference" is November 8, 2010. *See Steed*, 802 F.3d 1317; *Mahurkar*, 79 F.3d at 1578. The inventor's activities performed on November 9, 2010 were not performed on a date "just preceding the effective date of the [Yoshioka] reference," and therefore do not show diligence from a date just prior to the effective date of the Yoshioka reference.

The inventor testifies that after he uploaded the schematic diagrams on October 29, 2010, he worked diligently to reduce the invention to practice. Ex. 2043 ¶ 41. The inventor testifies that over the next ten days (from October 29 to November 9, 2010), other parts of the chip design were integrated together to form a complete ADC and a complete AFE (analog front-end). *Id.* The inventor testifies that the digital portion of the chip was integrated at the chip top-level, and final verifications took place. *Id*.

However, the inventor's testimony regarding the activities described in paragraph 41 of his declaration are not corroborated with evidence. Ex. 2043 ¶ 41. For example, the inventor testifies that "I worked diligently to reduce my invention to practice." *Id.* In the next sentence, the inventor then uses the passive voice, stating that "[o]ver the next ten days, other parts of the chip were integrated together" and that "final verifications took place." *Id.* Mr. Kapusta does not say that he personally integrated other parts of the chip together, does not say that he performed final verifications, and does not specify dates when this work was performed. Further, this paragraph does not identify evidence that corroborates this testimony. The testimony of the inventor regarding his diligence "must be corroborated with evidence." *ATI Technologies ULC v. Iancu*, 920 F.3d at 1370. We do not discern any corroborating evidence of the inventor's diligence "from a date just prior" to the effective date of Yoshioka.

As another example, the inventor testifies about the practice of preparing a tapeout file when developing a chip. Ex. 2043 ¶ 42. However, the inventor does not provide corroborating evidence showing the actual work that was done in preparing the tapeout file of the inventor's circuit, whether work was done on the date just preceding the publication date, and whether he or someone else performed the work. The inventor does provide testimony discussing his use of a verification tool on November 9, 2010. Ex. 2043 ¶ 43. However, as discussed above, November 9, 2010 is the effective date of Yoshioka, not the date "just preceding the effective date."

The date just preceding Yoshioka's effective date is November 8, 2010. The inventor has not provided any corroborating evidence of diligence from the date just preceding the effective date of Yoshioka. *ATI*

Technologies, 920 F.3d at 1370; *Steed*, 802 F.3d 1317; *Mahurkar*, 79 F.3d at 1578. Nor has the inventor provided corroborating evidence of his diligence on any date between the alleged conception date of October 29, 2010, and Yoshioka's effective date of November 9, 2010. Even accepting Patent Owner's contention that the inventor performed work on the effective date of November 9, 2010, Patent Owner does not establish diligence by the inventor on the date just preceding the effective date of Yoshioka. Patent Owner has failed to establish "diligence concern[ing] the period just preceding the effective date of the adverse reference, to the actual or constructive reduction to practice." *Steed*, 802 F.3d at 1317.

Reduction to Practice

"To establish an actual reduction to practice . . . the inventor must prove that: (1) he constructed an embodiment or performed a process that met all the limitations of the claim; and (2) he determined that the invention would work for its intended purpose." *Du Pont v. Unifrax I LLC*, 921 F.3d 1060, 1075 (Fed. Cir. 2019). "Depending on the character of the invention and the problem it solves, this showing may require test results." *Mahurkar*, 79 F.3d at 1578.

Patent Owner contends that the inventor performed tests on the sample chips that included the comparator circuit allegedly embodying the claimed invention, and that the tests show that the comparator worked in accordance with its intended purpose. PO Resp. 37–39. Patent Owner contends that test plots of the INL (integral non-linearity) and DNL (differential non-linearity) shown in Exhibit 2030 show that the integral non-linearity of the ADC on the chip indicates that the comparator with the ADC was functioning within normal parameters. PO Resp. 38 (citing Ex. 2030;

Ex. 2043 ¶¶ 59–61). Patent Owner contends that a person of ordinary skill would have appreciated that the test results showed the ADC worked satisfactorily, and correspondingly that all components in the comparator worked as intended. PO Sur-Reply 8 (citing Ex. 2044 ¶ 34).

Petitioner contends that the INL/DNL tests cited by Patent Owner do not show that the timer circuit responds inversely to PVT effects, but rather, show how closely actual chip components match schematics. Reply 18–19 (citing Ex. 1018 ¶¶ 50–51; Ex. 1016 26:9–15, 32:12–16, 43:8–25, 52:12–17). Dr. Holberg testifies that "[n]one of the testing of the Gecko chip ADI relies on shows comparator performance, let alone that an adaptive delay device within the comparator responds inversely to PVT effects." Ex. 1018 ¶ 50. Dr. Holberg testifies that a person of ordinary skill "would not be able to determine or infer, from INL/DNL, a circuit component's response to PVT or any delay through circuit components." Ex. 1018 ¶ 51. Dr. Holberg testifies that the results "do not show that the ADC by itself was functioning properly" because "the results are combined INL/DNL measurements." Ex. 1018 ¶ 54. Dr. Holberg testifies that "[o]ne part of the system may contribute to INL/DNL positively, but another part of the system may contribute . . . negatively." *Id.* Dr. Holberg testifies that the "combined result, which is what ADI presented, can be deceiving and is not an indicator of ADC block performance." *Id*. Dr. Holberg testifies that "the INL/DNL results do not even show a properly functioning ADC," because the DNL plot in Exhibit 2030 shows a DNL of -1, which indicates that the chip was not properly functioning. *Id*. ¶ 55.

We agree with Dr. Holberg. Ex. 1018 ¶¶ 50–55. We find Dr. Holberg's testimony persuasive that a person of ordinary skill would not be

able to determine or infer a circuit component's response to PVT, nor any delay through circuit components, from the INL/DNL measurements shown in Exhibit 2030. We credit Dr. Holberg's testimony in determining that the INL/DNL measurements do not indicate whether the ADC by itself was functioning properly, nor whether an adaptive delay device within the comparator responds inversely to PVT effects. We further credit Dr. Holberg's testimony in determining that the DNL plot shown in Exhibit 2030 does not show that the chip was properly functioning. Patent Owner has not established actual reduction to practice. Considering all the evidence of record in this proceeding, we determine that Yoshioka is prior art to the '659 patent.

Whether Yoshioka discloses inversely adjusting delay

Claim 5 recites "the adaptive delay device is configured to respond inversely to the response of other circuit components." Patent Owner contends that this limitation of claim 5 requires a delay element that is configured to adjust its delay inversely in response to the PVT effects on components other than the delaly element. PO Resp. 40 (quoting claim 5). We agree with Patent Owner on this point.

Petitioner, citing Patent Owner's Response, contends that the delay of Yoshioka's comparator will indisputably change with PVT. Reply 23 (citing PO Resp. 14–15 (showing comparator performance and tau vary with PVT); *see* Ex. 1018 ¶¶ 59–60. Petitioner, citing testimony of Patent Owner's declarant Dr. Hanumolu, contends that PVT affects input voltages to the comparator of Yoshioka and the delay of the comparator. Reply 23–24 (citing Ex. 1017, 51:7–10, 51:12–53:12, 57:16–58:16, 65:16–24; Ex. 2044 ¶ 25). We credit the testimony of Dr. Hanumolu and Dr. Holberg in

determining that a person of ordinary skill would have recognized that the delay of the comparator would change as PVT conditions change.

Petitioner contends that Figure 3 of Yoshioka discloses the internal clock generator, which includes the comparator in its loop. Reply 24 (citing Ex. 1004, 19). Petitioner contends that Yoshioka discloses that this loop is dependent on PVT conditions. Reply 24 (citing Ex. 1004, 22). Petitioner contends that Yoshioka discloses that T_d is a function of comparator speed, as shown by the cycle period during the conversion, Φ_c, which is $T_{c1} + T_{c2} + 2T_d$. Reply 24 (citing Ex. 1004, 19, 22). Petitioner contends that to maintain the number of Φ_c cycles N at 10, when T_d changes in response to PVT, so must T_{c1} and T_{c2}. Reply 24 (citing Ex. 1018 ¶¶ 60–61).

In contrast, Patent Owner contends that Yoshioka describes calibrating T_d to keep internal clock Φ_c at approximately 700 MHz, to ensure that 10 comparison operations are performed during the conversion period. PO Resp. 49 (citing Ex. 1004, 19). Patent Owner contends that Yoshioka describes adapting the delay inversely to compensate for PVT effects on the delay controller, but does not describe adapting the delay inversely to compensate for the PVT effects on other components. PO Resp. 49–51 (citing Ex. 2044 ¶¶ 51–54); PO Sur-Reply 12. According to Patent Owner, the delay T_d is not a function of the speed of the comparator. PO Sur-Reply 14.

We agree with Petitioner and Dr. Holberg that T_d is a function of the delay of the comparator, T_{c1} and T_{c2}, and that T_d changes inversely to changes in T_{c1} and T_{c2}. Yoshioka discloses that the internal clock Φ_c is generated by a loop, which includes a comparator and a delay controller. Ex. 1004, 19, 22, Fig. 3. Yoshioka discloses that this loop is dependent on

PVT conditions. Ex. 1004, 19. Yoshioka discloses that the frequency of the internal clock Φ_c depends on the comparator response delay (which is T_{c1} and T_{c2} as shown in Figure 3) and T_d. Ex. 1004, 19–20, 22; Ex. 1018 ¶ 61. We agree with Petitioner and Dr. Holberg, that in order to keep the cycle period Φ_c constant, for example at approximately 700 MHz, when the delays of the comparator T_{c1} and T_{c2} change due to PVT variations, T_d must change inversely, as shown by the cycle period of $\Phi_c = T_{c1} + T_{c2} + 2T_d$. Ex. 1004, 22; *see id*. at 19–20; Ex. 1018 ¶ 61.

Patent Owner also contends that adjusting the delay inversely to the PVT effects on the comparator would hurt Yoshioka's performance, because Yoshioka discloses that the capacitor digital-to-analog converter (CDAC) performs its settling operation during T_d, and if the CDAC is running slower, then T_d should be made longer, not shorter. PO Resp. 51–52 (citing Ex. 2044 ¶¶ 55–56); PO Sur-Reply 14. In contrast, Petitioner contends that Yoshioka discloses that testing proved that even when adjusting the delay inversely to PVT effects of the comparator, CDAC settling performance still allowed the ADC to complete 10 trials for the provided T_d range. Reply 24–25 (citing Ex. 1004, 22–23; Ex. 1018 ¶ 62). We agree with Dr. Holberg, that Yoshioka's test results show that the performance of the successive approximation register (SAR) ADC with the adjustable delay completes 10 bit trials for the tunable range of T_d, even considering the settling performance of the CDAC. Ex. 1004, 22–23; Ex. 1018 ¶ 62.

Patent Owner contends that Dr. Holberg did not analyze the comparator circuit of Yoshioka to determine how its performance would change in response to process, temperature, and voltage. PO Resp. 53–54 (citing Ex. 2042, 113:8–21, 112:11–19, 92:21–93:10, 95:15–96:25, 101:1–8;

Ex. 2044 ¶ 59); PO Sur-Reply 13, 15 (citing Ex. 2047, 30:8–21). Patent Owner contends that, absent any analysis of the comparator circuit, Petitioner has no basis to allege that the clock generator circuit of Yoshioka responds inversely to PVT effects on other components. PO Resp. 54 (citing Ex. 2044 ¶ 60).

We are not persuaded by those contentions. Dr. Holberg testifies that a person of ordinary skill would recognize that comparator delay of Yoshioka indisputably will change with PVT. Ex. 2047, 16:13–14; Ex. 1018 ¶ 60. Dr. Holberg testifies that Yoshioka discloses that the internal clock generator includes the comparator in its loop, and this loop that generates Φ_c is dependent on the PVT conditions, so its frequency is controlled during the conversion. Ex. 2047, 16:21–17:13. Dr. Holberg testifies that the adaptive delay device of Yoshioka is thus responding to PVT effects on other components, such as the comparator. Ex. 2047, 17:14–16. When asked "how does [the disclosure of Yoshioka] explain how an increase in temperature impacts whether the delay through the comparator is increased or decreased," Dr. Holberg answered that "[i]t really doesn't matter which direction as long as you're correcting for it." Ex. 2047, 20:4–16. Dr. Holberg testified that the internal clock period is $T_{c1} + T_{c2} + 2T_d$, where T_{c1} and T_{c2} are the comparator delays, and the control loop adjusts T_d to maintain the control frequency. Ex. 2047, 22:1–5; Ex. 1018 ¶ 61. Dr. Holberg testified that "[i]f the comparator delay goes up as a function of temperature going up, it will adjust accordingly. If the comparator delay goes down as a result of temperature going up, it will adjust accordingly. Yoshioka's internal clock generator . . . adjusts regardless of which direction the comparator goes as a function of temperature." Ex. 2047, 22:5–12; *see*

id. at 23:1–4, 23:8–10, 24:5–9, 25:9–14, 30:23–31:21, 32:16–19; Ex. 1018 ¶ 61.

We are persuaded by Dr. Holberg's testimony that the comparator delay of Yoshida will change with PVT variations, and whether the delay of the comparator increases or decreases due to PVT variations does not matter, because the adjustable delay of Yoshioka will adjust accordingly. Ex. 1004, 19–20, 22; Ex. 1018 ¶¶ 57–61. Yoshioka discloses that (a) the internal clock generator that generates the frequency of Φ_c includes a comparator and a delay controller in its loop, (b) "[t]he frequency of Φ_c depends on the comparator response delay" (which is $T_{c1} + T_{c2}$) "and T_d" (that is, the period of $\Phi_c = T_{c1} + T_{c2} + 2T_d$), and (c) the "loop" (which includes the comparator) "is dependent on PVT conditions, so its frequency is controlled during the conversion." Ex. 1004, 19–20, 22. We agree with Dr. Holberg, that when the delays of the comparator, T_{c1} and T_{c2}, change due to variations in PVT conditions, the delay of the delay controller will adapt accordingly to maintain the number of Φ_c cycles N at 10. Ex. 1018 ¶ 61; Ex. 1004, 19, 22. Therefore, contrary to Patent Owner's contentions, Dr. Holberg's testimony that the adaptive delay device of Yoshioka responds inversely to PVT effects on other components is supported by persuasive evidence.

Patent Owner further contends that even if there are PVT effects on the comparator circuit, the effects are too small to cause the delay controller to adjust the delay. PO Resp. 54–56 (citing Ex. 2044 ¶¶ 62–64). Patent Owner's contention is inconsistent with Yoshioka's disclosure that the loop of the internal clock generator includes a comparator, that this loop is dependent on the PVT conditions, and that the frequency of Φ_c depends on the comparator response delay and T_d. Ex. 1004, 19.

Patent Owner's contention is also inconsistent with the testimony of Dr. Holberg and the testimony of Dr. Hanomolu. Ex. 1018 ¶¶ 59–60, 63–67; Ex. 2044 ¶¶ 25–26; Ex. 1017, 51:7–10, 51:12–53:12, 57:16–58:16, 65:16–24. For example, Dr. Holberg testifies that variations in comparator regeneration time constants, caused by effects of a 65 mm process, range from 27 ps to 55 ps, and that the comparator of Yoshioka is fabricated using a 65 mm process and would experience such process effects. Ex. 1018 ¶¶ 66–67. Dr. Holberg testifies that the T_d resolution of 3.75 ps allows Yoshioka's controller to appropriately adjust and compensate for PVT effects on the comparator. *Id*. We are persuaded by Dr. Holberg's testimony that the comparator in the loop of Yoshioka would experience PVT effects that would impact the time for each cycle period of Φ_c, and that the resolution of 3.75 ps would allow the delay controller to adjust and compensate for the PVT effects on the comparator.

For the reasons set forth by Petitioner and explained above, we are persuaded that Yoshioka discloses all of the limitations of claim 5. The Petition and supporting testimony of Dr. Holberg has shown by a preponderance of the evidence that claim 5 is anticipated by Yoshioka.

Claim 6 depends from claim 5 and recites "a capacitive element for supplying a threshold voltage to a control input of an output switch." Petitioner contends that Yoshioka discloses this limitation in describing a capacitive element with an output voltage of V_B, and that when the output from the capacitive element, V_B, reaches the switching threshold of the AND gate shown in Figure 3, the output voltage Φ_c transitions from low to high. Pet. 27–28 (citing Ex. 1004, Figs. 3 and 9; Ex. 1002 ¶ 63).

Claim 6 recites "an intermediate switch for selectively delivering a current to the capacitive element." Petitioner contends that Yoshioka discloses this limitation in describing an intermediate switch in the delay controller that selectively delivers current to the capacitive element. Pet. 29 (citing Ex. 1004, 414, Fig. 9).

Claim 6 recites "wherein the capacitive element charges to a threshold voltage that actuates the output switch which changes an output signal." Petitioner contends that Yoshioka discloses this limitation in describing that during the conversion period, when the capacitive element shown in Figure 9 charges such that V_B reaches the switching threshold of the AND gate, the output voltage Φ_c changes from low to high. Pet. 29–30 (citing Ex. 1003, Figs. 3, 9).

Claim 6 recites "wherein a time required to charge the capacitive element to the threshold voltage varies in response to circuit conditions of the converter." Petitioner contends that Yoshioka discloses this limitation in disclosing an ADJ code that includes 3-bit fine tuning to control the rate that the variable capacitor of the delay controller charges. Pet. 30–31 (citing Ex. 1004, 22, Fig. 9; Ex. 1002 ¶¶ 66–67).

Patent Owner does not argue separately dependent claim 6, but instead relies on arguments presented for claim 5, which we find unpersuasive as discussed in our analysis of claim 5. Petitioner's analysis for claim 6, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 61–67), which we credit, is persuasive that Yoshioka describes the limitations of claim 6.

The preamble of independent claim 9 recites a "method of controlling PVT effects in a circuit system." Petitioner contends that Figure 1 of the

AAPA discloses this limitation in showing a comparator. Pet. 43 (citing Ex. 1001, 1:16–34, Fig. 1).

Claim 9 recites "responsive to a state change in an input signal, charging a capacitive element with reference to a first supply voltage." Petitioner contends Yoshioka discloses this limitation in describing a 3-b-controlled MOS variable capacitor. Pet. 32 (citing Ex. 1004, Fig. 9; Ex. 1002 ¶ 69). Petitioner contends that the capacitive element first charges with reference to its ground voltage. *Id*. Petitioner contends that the capacitive element begins to charge when input signal V_A transitions from low to high , and the series of inverter pairs shown in Figure 9 outputs a high signal, causing the capacitive element to charge with reference to ground. Pet. 33 (citing Ex. 1002 ¶ 70).

Claim 9 recites "when the capacitive element's output voltage reaches a voltage threshold, generating an output voltage." Petitioner contends that the output voltage of the capacitive element shown in Figure 9 is V_B, and that when V_B reaches the threshold of the AND gate during the conversion phase, output voltage Φ_c transitions from low to high. Pet. 33–34 (citing Ex. 1004, Figs. 3 and 9).

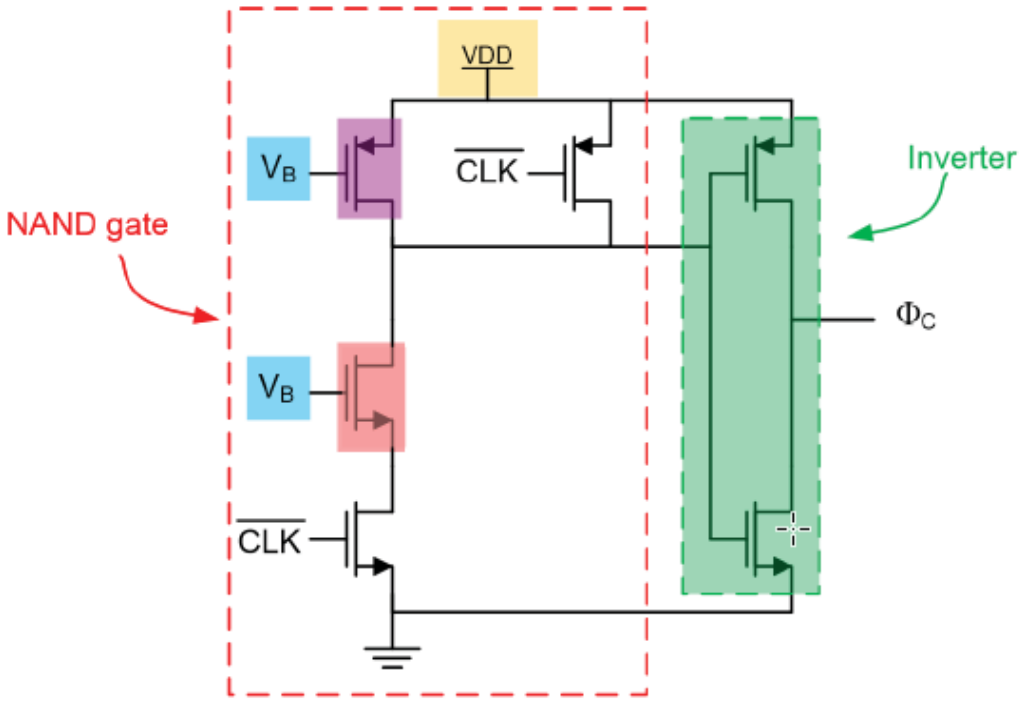
Claim 9 recites "wherein the method is performed in an integrated circuit, and delays between the state change of the input signal and the generated output voltage vary inversely in response to PVT effect on other components of the integrated circuit." Petitioner contends that Yoshioka discloses "performed in an integrated circuit" in describing an ADC with on-chip digital calibration. Pet. 35 (citing Ex. 1004, 18; Fig. 10). Petitioner contends that Yoshioka discloses this limitation in describing a delay controller in the internal clock control that increases the delay between input

signal V_A and generated output voltage Φ_c when PVT effects on circuit components other than the delay element cause the components to run faster, and decreases the delay when PVT effects cause the other components to run slower. Pet. 35–37 (citing Ex. 1004, 18, 22, Fig. 3; Ex. 1002 ¶¶ 75–77).

Patent Owner does not argue separately independent claim 9, but instead relies on arguments presented for claim 5, which we find unpersuasive as discussed in our analysis of claim 5. *See* PO Resp. 58. Petitioner's analysis for claim 9, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 68–78), which we credit, is persuasive that Yoshioka describes all the limitations of claim 9.

B. Obvious over Yoshioka (Claim 10)

Claim 10 depends from claim 9 and recites "wherein the voltage threshold is set by determining when an output voltage of the capacitive element is within a voltage threshold of a second supply voltage, opposite from the first supply voltage." Petitioner contends that the claimed "first supply voltage" is ground, and that the output voltage of the capacitive element of the delay controller, V_B, is input to an AND gate. Pet. 37–38 (citing Ex. 1004, Fig. 3). Petitioner contends that a person of ordinary skill would have understood that the AND gate shown in Figure 3 would be implemented at a transistor level using a NAND gate followed by an inverter because that is the most robust and cost effective transistor implementation of an AND gate in CMOS. Pet. 39 (citing Ex. 1002 ¶¶ 81–82; Ex. 1009, 286; Ex. 1010, 16–17; Exs. 1011–1013). Petitioner provides an example of the transistor level implementation of an AND gate in the figure below.



Pet. 39; Ex. 1002 ¶ 81. The figure above shows an example of the transistor level implementation of an AND gate provided by Petitioner.

Referring to the figure above, Petitioner contends that during the conversion phase, when V_B transitions from low to high and reaches VDD less the threshold voltage of a PMOS transistor (shaded purple), the PMOS transistor will turn off and the NMOS transistor (shaded red) will turn on. Pet. 40 (citing Ex. 1002 ¶ 81). Petitioner contends that the NAND gate then transitions from high to low, causing the output voltage Φ_c following the inverter (shaded green) to transition from low to high. Pet. 40 (citing Ex. 1002 ¶ 83; Ex. 1004, Fig. 3).

Petitioner contends that VDD in Yoshioka constitutes the second supply voltage opposite of the first supply voltage of ground. Pet. 40 (citing Ex. 1004, 19, 21, Fig. 5; Ex. 1002 ¶¶ 84–85). Petitioner contends that because the voltage threshold is set by determining when V_B reaches VDD (the second supply voltage) – V_{th} (the threshold voltage of the PMOS

transistor in the AND gate), a person of ordinary skill would have understood that Yoshioka teaches "the voltage threshold [being] set by determining when an output voltage of the capacitive element is within a voltage threshold of a second supply voltage, opposite from the first supply voltage" as claimed. Pet. 40.

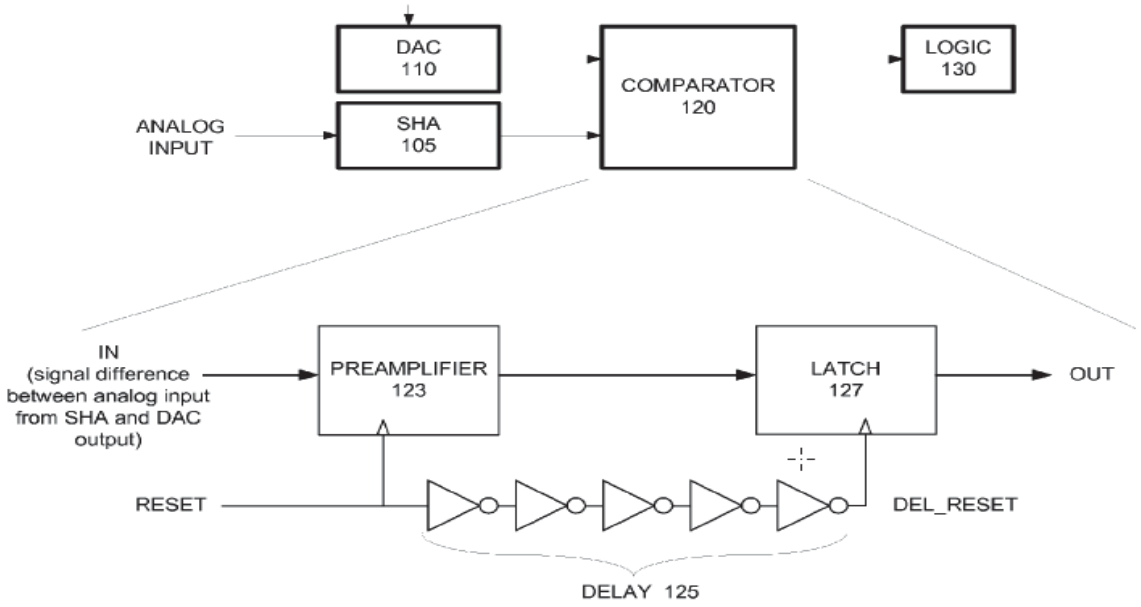
Patent Owner does not argue separately claim 10, but instead relies on arguments presented for claim 5, which we find unpersuasive as discussed in our analysis of claim 5. Petitioner's analysis for claim 10, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 79–86), which we credit, is persuasive that claim 10 would have been obvious over Yoshioka.

C. Obvious over Yoshioka and the AAPA[6] (Claims 1 and 2)

1. Overview of the AAPA

Figure 1 of the '659 patent illustrates a conventional comparator configuration within a successive approximation register (SAR) analog-to-digital converter (ADC) and is shown below. Ex. 1001 2:9–10.

[6] *See* USPTO Memorandum, Treatment of Statements of the Applicant in the Challenged Patent in *Inter Partes* Reviews Under § 311 (Aug. 18, 2020) at 9 (AAPA can be used to (1) supply missing claim limitations that were generally known in the art prior to invention, (2) support a motivation to combine, or (3) demonstrate the knowledge of the ordinarily skilled artisan at the time of invention).



100
FIG. 1
(PRIOR ART)

Figure 1 above is labeled prior art and shows conventional SAR ADC 100 including an analog input, sample and hold amplifier 105, digital-to-analog converter 110, comparator 120, and logic 130. Ex. 1001, 1:16–20. Comparator 120 includes preamplifier 123, delay device 125, and latch 127. Ex. 1001, 1:20–21. The preamplifier amplifies the input signal and outputs the amplified input signal to the latch, improving the input referred noise and linearity of the comparator. Ex. 1001, 1:21–24. In order to allow the preamplifier time to amplify the input signal, a control signal RESET is delayed before going into the latch, so that the latch is held in a known reset state while the preamplifier is amplifying. Ex. 1004, 1:24–27. Once the delayed reset signal is released, the latch will regenerate and the comparator will make its decision. Ex. 1004, 1:27–29. The delay of the delay device is fixed by inserting an inverter or series of inverters in the circuit path. Ex. 1004, 1:29–31. A delayed output signal DEL_RESET from the delay device is provided to the latch. Ex. 1001, 1:31–32.

2. Claims 1 and 2

The preamble of independent claim 1 recites a comparator. Petitioner contends that Figure 1 of the AAPA discloses this limitation in showing a comparator. Pet. 43 (citing Ex. 1001, 1:16–34, Fig. 1).

Claim 1 recites "a preamplifier responsive to a first control signal." Petitioner contends the AAPA teaches this limitation in disclosing a preamplifier responsive to a RESET signal. Pet. 43 (citing Ex. 1001, 1:16–34, Fig. 1).

Claim 1 recites "a latch responsive to a second control signal." Petitioner contends the AAPA teaches this limitation in disclosing a latch responsive to a DEL_RESET signal. Pet. 44 (citing Ex. 1001, 1:16–34, Fig. 1).

Claim 1 recites "a delay element having an input for the first control signal and output for the second control signal." Petitioner contends Yoshioka teaches this limitation in disclosing an adaptive delay element that includes a delay controller, an AND gate that outputs Φ_c, a CLK input to the AND gate, and edge count and delay adjust blocks that generate the ADJ code that adjusts delay T_d. Pet. 44–45 (citing Ex. 1004, Fig. 3).

Claim 1 recites "the delay element having a circuit structure to adaptively increase or decrease delay propagation of the first control signal in a manner that counteracts PVT effects present in other components of the comparator." Petitioner contends that this limitation mirrors the language of independent claim 9, except that this limitation refers to a delay that "counteracts PVT effects," while claim 9 refers to delays that "vary inversely to PVT effects." Pet. 45. Petitioner contends that Yoshioka teaches this limitation for the reasons given in Petitioner's analysis of

claim 9. Pet. 45 (citing Ex. 1002 ¶¶ 95–96). In contrast, Patent Owner contends that Yoshioka does not disclose this limitation, relying on arguments presented for claim 5, which we find unpersuasive as discussed in our analysis of claim 5. PO Resp. 58–59.

Petitioner contends that the AAPA discloses a conventional comparator configuration with a delay element that provides a fixed delay to the latch signal (RESET), so that the latch will capture the input signal from the preamplifier at an appropriate time. Pet. 41 (citing Ex. 1001, 1:9–34). Petitioner contends that Yoshioka provides an adaptive delay element with an adjustable, rather than a fixed, delay for the latch signal. Pet. 41–42 (citing Ex. 1004, 18). Petitioner contends that a person of ordinary skill in the art would have recognized that providing a variable delay yields the predictable benefit of counteracting PVT variations. Pet. 41–42 (citing Ex. 1004, 18, 22; Ex. 1005, 1:33–36; Ex. 1002 ¶¶ 87–88). Petitioner also contends that replacing the fixed delay element of the AAPA with the adaptive delay element of Yoshioka would have been the simple substitution of one known element for another to obtain the predictable result of the AAPA circuit with an adaptive delay element that compensates for PVT variations. Pet. 42 (citing Ex. 1004, 18, 22; Ex. 1002 ¶¶ 89–90).

Patent Owner contends that the Petition relies on impermissible hindsight from the ’659 patent, and improperly relies on Ajit, to provide a motivation to combine the AAPA and Yoshioka. PO Resp. 59. We start by considering the teachings in the prior art to evaluate this contention. “The presence or absence of a motivation to combine references in an obviousness determination is a pure question of fact.” *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). Evidence of a motivation to combine prior art

references "may flow from the prior art references themselves. *See Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1125 (Fed. Cir. 2000).

We find that persuasive evidence of motivation for a person of ordinary skill in the art to combine the references, namely, to compensate for PVT variations, flows from Yoshioka itself. Yoshioka explains that "prior ADCs use a fixed T_d and provide no means to control it." Ex. 1004, 22. To address this concern, and as discussed previously, Yoshioka's Figure 8 illustrates a loop including the comparator and the internal clock generator that generates internal clock Φ_c and implements an algorithm to adjust the delay T_d to compensate for PVT variations. *Id.* at 19, 21–22. Yoshioka discloses that "[t]he frequency of Φ_c depends on the comparator response delay and T_d" and that the "loop is dependent on PVT conditions, so its frequency is controlled during the conversion." *Id*. at 19–20, 22. The internal clock generator adjusts the delay T_d to compensate for PVT variations. *Id*. at 18–19, 22. We agree with Petitioner, that a person of ordinary skill in the art would have replaced the fixed delay element of the AAPA with the adaptive delay element of Yoshioka to yield the predictable benefit of compensating for PVT variations as taught by Yoshioka. Ex. 1001, 1:16–34, Fig. 1; Ex. 1004, 18–19, 22.

Further, the Supreme Court has stated that "[t]he obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007); *see id.* at 415. Engagement with the question of obviousness requires an "expansive and flexible approach" where "a court *must* ask whether the improvement is more than the predictable use of prior art

elements according to their established functions. *Id.* at 415, 417 (emphasis added). "[W]hen a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result." *Id.* at 416.

Dr. Holberg testifies that combining the teachings of the AAPA with the variable delay of Yoshioka "would have been the simple substitution of one known element (i.e., the series of inverters providing fixed delay in AAPA) for another (i.e., the adaptive delay element of Yoshioka discussed below) to obtain predictable results (i.e., AAPA circuit with an adaptive delay element that compensates for PVT variations)." Ex. 1002 ¶ 90. We credit the testimony of Dr. Holberg in determining that altering the known circuit of the AAPA by substituting its fixed delay element with the known adaptive delay element of Yoshioka would have done no more than yield the predictable result of causing the AAPA circuit with the adaptive delay element of Yoshioka to compensate for PVT variations as taught by Yoshioka.

Patent Owner contends that the circuit of Yoshioka generates a delayed signal calibrated to output ten pulses of Φ_c for ten comparison cycles within the fixed conversion period, but the AAPA generates a single delayed signal for a single comparison cycle. PO Resp. 59–60 (citing Ex. 2044 ¶ 71); PO Sur-Reply 15–16. We are not persuaded by this contention. Dr. Holberg testifies that (a) Yoshioka's Φ_c signal, which is generated after a single comparison cycle, goes to a latch, just as the AAPA's delay signal and (b) a person of ordinary skill would have understood that the AAPA's successive approximation register ADC would

perform more than one comparison cycle, therefore, Dr. Hanumolu's statement about the AAPA only making one comparison is not true. Ex. 1018 ¶ 69. We credit Dr. Holberg's testimony in determining that both Yoshioka's Φ_c signal and the AAPA's delay signal go to a latch. We also credit Dr. Holberg's testimony in determining that the successive approximation register ADC of the AAPA would perform more than one comparison cycle in order to perform successive approximations using successive comparison cycles such as those taught by Yoshioka.

Patent Owner contends that using the internal clock generator of Yoshioka, which generates ten pulses, would change the principle of operation of the AAPA, which does not seek to generate a fixed number of pulses within a predetermined time period. PO Resp. 61. We are not persuaded by this contention. We agree with Dr. Holberg, that the successive approximation register DAC of the AAPA would generate successive comparison cycles in order to perform successive approximations. Ex. 1018 ¶ 69. We also agree with Dr. Holberg, that the number of cycles, whether 10 or 1, does not matter, because a person of ordinary skill would have recognized that Yoshioka's teaching of adaptively adjusting delay in response to PVT effects on a comparison cycle would apply to what Patent Owner alleges is the AAPA's single comparison. *Id*. A person of ordinary skill would have looked to the teachings of Yoshioka to compensate for the PVT variations of the AAPA. *Id*.; Ex. 1002 ¶¶ 88–90.

Patent Owner contends that a person of ordinary skill would not have had a reason to use the internal clock generator of Yoshioka in place of the fixed delay of the AAPA, because the comparator of Yoshioka generates two output signals that are logically combined with other signals to generate

the clock signal Φ_c, which has edges that can be counted, but the AAPA preamplifier outputs an analog signal, not a signal that has countable edges. PO Resp. 60–61. Patent Owner also contends that adding the clock generator of Yoshioka to the AAPA would result in including additional logic modules, and that it is not clear how such a combination would work. PO Resp. 61.

We are not persuaded by this contention. The test for obviousness is what the combined teachings of the references would have suggested to those of ordinary skill in the art. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981). The AAPA discloses an SAR ADC with a fixed delay. Ex. 1001, 1:16–34. Yoshioka discloses an SAR ADC that, different from a known fixed delay, adaptively adjusts the delay in response to PVT effects. Ex. 1004, 18–19, 22; Ex. 1002 ¶ 88; Ex. 1018 ¶ 69. Both Dr. Holberg and Dr. Hanumolu testify that designers add additional components to a circuit to compensate for PVT variations when the circuit would be impacted by PVT variations. Ex. 1018 ¶¶ 69–71; Ex. 2044 ¶ 53. Dr. Holberg testifies that replacing the fixed delay of the AAPA with the adaptive delay element of Yoshioka would have been a simple substitution of one known element for another that yields the predictable result of causing the AAPA circuit with the adaptive delay element of Yoshioka to compensate for PVT variations. Ex. 1002 ¶ 90.

We credit Dr. Holberg's testimony in determining that replacing the fixed delay element of the AAPA with the adjustable delay element of Yoshioka was not "uniquely challenging or difficult for one of ordinary skill in the art." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 419). Ex. 1002 ¶¶ 88–90. The

Petition and supporting evidence persuasively shows that claim 1 of the '659 "patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement," therefore, "the combination is obvious." *KSR*, 550 U.S. at 417.

For the reasons set forth by Petitioner and explained above, we are persuaded that Yoshioka and the AAPA teach all of the limitations of claim 1, and that a person of ordinary skill would have combined the teachings of the references to achieve the comparator recited in the claim and would have had a reasonable expectation of success in doing so. Dr. Holberg's testimony provides sufficient evidence of motivation that a person of ordinary skill would have used the adaptive delay within the circuit of the AAPA and would have had a reasonable expectation of success in doing so. Dr. Holberg's testimony also provides persuasive evidence that the combination of Yoshioka and the AAPA teaches that the '659 "patent claims a structure already known in the prior art (the AAPA circuit shown in Figure 1 of the '659 patent) that is altered by the mere substitution of one element (the fixed delay) for another known in the field (Yoshioka's clock circuit with an adjustable delay)" and does no more "than yield a predictable result" of a comparator with an adjustable delay to compensate for PVT effects. Petitioner has proven by a preponderance of the evidence that claim 1 would have been obvious over Yoshioka and the AAPA.

Claim 2 depends from claim 1 and recites "a capacitive element for supplying a threshold voltage to a control input of an output switch." Petitioner contends that Yoshioka teaches this limitation in disclosing a capacitive element with an output voltage V_B. Pet. 46 (citing Ex. 1004,

Fig. 9). Petitioner contends that V_B and an inverted CLK signal are inputs to an AND gate, which outputs Φ_c. Pet. 46–47. Petitioner contends that during the conversion phase, when the output from the capacitive element, V_B, reaches the switching threshold of the AND gate, output voltage Φ_c transitions from low to high. *Id*. (citing Ex. 1004, Fig. 3).

Claim 2 recites "an intermediate switch for selectively delivering a current to the capacitive element." Petitioner contends that Yoshioka teaches this limitation in disclosing a series of inverter delay selectors that provide 4-b coarse delay control to a 3-b-controlled MOS variable capacitor that provides fine delay control. Pet. 47–48 (citing Ex. 1004, 22, Fig. 9).

Claim 2 recites "wherein the capacitive element charges to a threshold voltage that actuates the output switch which changes an output signal." Petitioner contends that Yoshioka teaches this limitation in disclosing that when the capacitive element charges such that the output of the capacitive element in the delay controller, V_B, reaches the switching threshold of the AND gate, the output voltage Φ_c changes from low to high. Pet. 48–49 (citing Ex. 1004, Fig. 3).

Claim 2 recites "wherein a time required to charge the capacitive element to the threshold voltage varies in response to the circuit conditions of the comparator." Petitioner contends that Yoshioka teaches this limitation for the reasons given in Petitioner's analyses of claims 6 and 9. Pet. 49–50.

Patent Owner does not argue separately claim 2, but instead relies on arguments presented for claim 1, which we find unpersuasive as discussed in our analysis of claim 1. PO Resp. 58–59. Petitioner's analysis for claim 2, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 97–104), which we credit, is persuasive that claim 2 would have been obvious over Yoshioka

and the AAPA.

D. Obvious over Yoshioka and Fiscus (Claims 7 and 8)

1. Fiscus

Fiscus discloses a circuit that generates a signal having a frequency that is proportional to absolute temperature (PTAT). Ex. 1006, Abstract, 4:37–40. The signal changes the refresh rate of a memory in response to a temperature change. Ex. 1006, 4:40–42. For example, the signal causes the refresh rate to increase as the temperature increases. Ex. 1006, 4:45–48.

2. Claims 7 and 8

Claim 7 depends from claim 6 and recites "wherein the current is proportional to the temperature of circuit components of the converter, and provided by a current source." Petitioner contends that the combination of Yoshioka and Fiscus teaches this limitation. Pet. 57–58. Petitioner contends that by modifying the inverters in Yoshioka's delay controller to implement the PTAT controlled delay stage in Fiscus yields a current through delay controller that is proportional to the temperature of the circuit components. Pet. 57–58 (citing Ex. 1006, 2:49–52). Petitioner contends that modifying a series of inverters as shown in Figure 9 of Yoshioka to implement a PTAT circuit as shown in Figure 3 of Fiscus yields the predictable benefit of an adaptive delay element that is responsive to temperature variations as taught by Fiscus. Pet. 53–57 (citing Ex. 1002 ¶¶ 109–116; Ex. 1006, 2:39–58, 4:26–51).

Patent Owner does not argue separately claim 7, but instead relies on arguments presented for claim 5, which we find unpersuasive as discussed above in our analysis of claim 5. PO Resp. 47. Petitioner's analysis for claim 7, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 106–118),

which we credit, is persuasive that claim 7 would have been obvious over the combination of Yoshioka and Fiscus.

Claim 8 depends from claim 7 and recites "a first pair of transistors configured as a current mirror." Petitioner contends that Fiscus teaches this limitation in disclosing a pair of transistors 112, 114 configured as a current mirror as shown in Figure 2. Pet. 59–60 (citing Ex. 1006, 3:37–40, Fig. 2; Ex. 1002 ¶¶ 121–122).

Claim 8 recites "a second pair of transistors with commonly connected control inputs connected to a drain terminal of one transistor of the first pair of transistors." Petitioner contends Fiscus teaches this limitation in disclosing a second pair of transistors 116, 118 with a commonly connected control input at node 132, where the control input at node 132 is connected to the drain terminal of transistor 112 of the first pair of transistors 112, 114. Pet. 60–61 (citing Ex. 1006, 3:19–21, Fig. 2).

Claim 8 recites "a single transistor with a control input connected to a terminal of a resistive element." Petitioner contends that Fiscus teaches this limitation in disclosing resistor 124 connected to transistor 122. Pet. 62 (citing Ex. 1006, 2:67–3:2, 3:7–8, Fig. 2).

Patent Owner does not argue separately claim 8, but instead relies on arguments presented for claim 5, which we find unpersuasive as discussed above in our analysis of claim 5. PO Resp. 47. Petitioner's analysis for claim 8, supported by testimony of Dr. Holberg (Ex. 1002 ¶¶ 119–124), which we credit, is persuasive that claim 8 would have been obvious over Yoshioka and Fiscus.

E. Obvious Over Yoshioka, AAPA, and Fiscus (Claims 3 and 4)

Claim 3 depends from claim 2 and recites "wherein a current source provides the current to the capacitive element, and the current is proportional to the temperature of circuit components of the comparator." Petitioner contends that Fiscus teaches this limitation in disclosing a PTAT current source configured to generate a temperature dependent reference signal that varies linearly with temperature. Pet. 64 (citing Ex. 1006, 2:47–52; Ex. 1002 ¶ 129). Petitioner contends that a person of ordinary skill would have combined the inverter delay stage of Yoshioka with the PTAT controlled delay stage of Fiscus to yield the predictable benefit of an adaptive delay element that is responsive to temperature variations. Pet. 63 (citing Ex. 1002 ¶ 126). Petitioner contends that replacing the delay element of the AAPA with the adaptive delay element of Yoshioka implementing the PTAT controlled delay stage of Fiscus is the substitution of one known element for another that yields predictable results. Pet. 63–64 (citing Ex. 1002 ¶ 127).

Patent Owner does not argue claim 3 separately, but instead relies on arguments presented for claim 1 which we find unpersuasive as discussed above in our analysis of claim 1. PO Resp. 58. Petitioner's analysis of claim 3, supported by testimony of Dr. Holberg (Ex. 1002 ¶¶ 125–129), which we credit, is persuasive that claim 3 would have been obvious over Yoshioka, AAPA, and Fiscus.

Claim 4 depends from claim 3 and recites "a first pair of transistors configured as a current mirror; a second pair of transistors with commonly connected control inputs connected to a drain terminal of one transistor of the first pair of transistors; and a signal transistor with a control input connected to a terminal of a resistive element." Petitioner contends that

Fiscus teaches the limitations of claim 4 for the reasons given in Petitioner's analysis of claim 8. Pet. 65.

Patent Owner does not argue claim 4 separately, but instead relies on arguments presented for claim 1 which we find unpersuasive as discussed above in our analysis of claim 1. PO Resp. 47. Petitioner's analysis of claim 4, supported by testimony of Dr. Holberg (Ex. 1002 ¶¶ 130–133), which we credit, is persuasive that claim 4 would have been obvious over Yoshioka, AAPA, and Fiscus.

F. Anticipated by Ajit (Claims 9–11)

Claim 9 recites "responsive to a state change in an input signal, charging a capacitive element with reference to a first supply voltage." Petitioner contends that Ajit discloses this limitation in describing an input signal p0_gate that falls low, causing current to charge capacitor 204 shown in Figure 2A of Ajit. Pet. 78–79 (citing Ex. 1005, 3:57–58, 4:15–19, Fig. 2A). Petitioner contends that Ajit discloses that the capacitor charges with reference to V_{SSC}, which is connected through a transistor to p0_gate, and p0_gate is received by circuit input port 224 connected to capacitor 204. Pet. 79–80 (citing Ex. 1005, Figs. 1 and 2A). Petitioner contends that p0_gate is the output of inverter 108. Pet. 80 (citing Ex. 1005, Fig. 1). Petitioner contends that when pre-driver-p is high, p0_gate is low because the NMOS transistor of inverter 108 is on; thus p0_gate is connected to V_{SSC}, corresponding to the claimed "first supply voltage," when p0_gate is low. *Id.*

Claim 9 recites "when the capacitive element's output voltage reaches a voltage threshold, generating an output voltage." Petitioner contends that the voltage at node 222 of Figure 2A, which is a connection point between

gates of active devices 216 and 218 and a first end of capacitor 204, discloses the claimed "capacitive element's output voltage." Pet. 80 (citing Ex. 1005, 4:2–4, Fig. 2A). Petitioner contends that "generating an output voltage" as claimed occurs when capacitor 204 sufficiently charges and the voltage at node 222 reaches the switching threshold of transistors 216 and 218, causing NMOS transistor 216 to turn on and PMOS transistor 218 to turn off, allowing p2_gate to be pulled low to V_{SSC}. Pet. 80–81 (citing Ex. 1004, Fig. 2A; Ex. 1002 ¶ 162).

Claim 9 recites "wherein the method is performed in an integrated circuit." Petitioner contends that Ajit discloses this limitation in describing a system and method for compensating for process, voltage, and temperature variations in a circuit." Pet. 82 (citing Ex. 1005, Abstract). Petitioner contends that a person of ordinary skill would have understood that the circuit is an integrated circuit. Pet. 82 (citing Ex. 1002 ¶ 164; Ex. 1005, 1:19–25, 1:27–31).

Claim 9 recites "delays between the state change of the input signal and the generated output voltage vary inversely in response to PVT effects on other components of the integrated circuit." Petitioner contends that Ajit's disclosure of the fall of p0_gate from high to low describes the claimed "state change of the input signal." Pet. 82. Petitioner contends that Ajit's disclosure of p2_gate pulled low to V_{SSC} describes the "generated output voltage." Pet. 82. Petitioner contends that Ajit discloses the "PVT effect on other components of the integrated circuit" in describing how quickly p0_gate falls. Pet. 82. Petitioner contends that Ajit discloses that the delay between input signal p0_gate falling from high to low, and output signal p2_gate falling from high to low, varies inversely to how quickly

p0_gate falls according to PVT effects. Pet. 81–83 (citing Ex. 1005, 3:19–24, 2:9–24, 4:13–33); *see id.* at 66–78.

Petitioner contends that Ajit discloses that "[w]hen the PVT condition is such that the fall of the p0_gate signal is fast, the PMOS PVT compensator circuit 116 produces a slowly falling p2_gate signal." Pet. 71 (citing Ex. 1005, 3:21–24). Petitioner contends that this disclosure describes that it takes longer for p2_gate signal to fall when p0_gate falls quickly, resulting in a longer delay. Pet. 71 (citing Ex. 1002 ¶¶ 144–145). Petitioner relies on annotated images of Figure 2A of Ajit to explain how PVT compensator circuit 116 accomplishes this inverse relationship between p2_gate delay and the PVT effect of a quickly falling p0_gate. Pet. 71–74 (citing Ex. 1005, 4:17–20, Fig. 2A; Ex. 1002 ¶¶ 146–150). Petitioner contends that "[t]hus, when PVT condition is such that p0_gate falls quickly causing a large drop in voltage at node 222 below the switching threshold of NMOS transistor 216 and PMOS transistor 218, p2_gate will fall slowly, resulting in a longer delay for the p2_gate state change." Pet. 75 (citing Ex. 1002 ¶ 151). Petitioner contends that "[t]his is because p2_gate remains high until the capacitor 204 charges sufficiently and allows the voltage at node 222 to return to the switching threshold of NMOS transistor 216 and PMOS transistor 218, thus allowing discharge through 216 and pulling p2_gate low." Pet. 75 (citing Ex. 1002 ¶ 151; *see id.* ¶ 149).

Petitioner provides a similar analysis about the p2_gate signal when the PVT condition is such that the fall of the p0_gate signal is slow. Pet. 75–78 (citing Ex. 1005, 3:19–21, Fig. 2A; Ex. 1002 ¶¶ 152–156). Petitioner contends that in this condition, PVT compensator circuit 116 produces a quickly falling p2_gate signal. Pet. 75 (citing Ex. 1005, 3:19–21).

Petitioner contends that this disclosure describes that "the longer it takes for p0_gate to fall, the shorter the state change delay for p2_gate from high to low." Pet. 75–76 (citing Ex. 1002 ¶ 152). Petitioner relies on annotated images of Figure 2A to explain how PVT compensator circuit 116 accomplishes this inverse relationship between p2_gate delay and the PVT effect of a slowly falling p0_gate. Pet. 76–78 (citing Ex. 1005, 4:24–28, Fig. 2A; Ex. 1002 ¶¶ 153–156). Petitioner contends that "[b]ecause voltage at node 222 remains high and NMOS transistor 216 stays on (rather than turn off and then back on as when p0_gate falls quickly), p2_gate will quickly be pulled low once NMOS transistor 214 turns on and allows discharge through 216." Pet. 77 (citing Ex 1002 ¶ 155).

Patent Owner contends that (a) a change in slew rate of an output signal does not necessarily result in a change in delay of the output signal; (b) Dr. Holberg's sketched waveforms (i) do not include underlying assumptions, (ii) prevent a person of ordinary skill from determining actual delays between transitions, and (iii) are incorrect; (c) Petitioner's argument is based on inherency; and (d) Dr. Hanumolu's simulations show that the delay circuit of Ajit does not adapt the delay inversely to the PVT effects on other components. PO Resp. 64–86. We address these contentions below.

(a) change in slew rate does not necessarily result in change in delay

Patent Owner contends that a change in slew rate does not necessarily result in a change in delay of the output signal. PO Resp. 65. Patent Owner, relying on sketches from Dr. Hanumolu, contends that an adapted output signal with a higher slew rate than a reference signal can have either more or less delay. PO Resp. 65–66 (citing Ex. 2044 ¶ 77).

Petitioner contends that Dr. Hanumolu admits that his sketches are unrelated to Ajit's circuits, and that Patent Owner does not offer any evidence of a circuit that could generate the waveforms shown in Dr. Hanumolu's sketches. Reply 29–30 (citing Ex. 1017, 80:5–82:1; Ex. 1018 ¶¶ 73–74). Petitioner, relying on simulations performed by Dr. Holberg, contends that slew rate cannot be divorced from delay. Reply 30 (citing Ex. 1018 ¶¶ 75–78). Dr. Holberg testifies that his "simulation results . . . clearly show that adjusting the slew rate results in adjusting delay." Ex. 1018 ¶ 78.

Patent Owner contends that Dr. Holberg's simulations, showing that changes to the slew rate of a circuit's input signal are always directly related to the delay through the circuit, apply to the simulated inverter circuit, not to circuits more generally. PO Sur-Reply 21. Patent Owner contends that Dr. Holberg agreed that delay through a circuit can be influenced by both the slew rate of an input signal and by PVT effects on the circuit. PO Sur-Reply 20 (citing Ex. 2047, 44:22–25). Patent Owner contends that this alone establishes that slew rate can be divorced from delay, and that one cannot predict how the delay through a circuit would change based only on the slew rate of the input signal. PO Sur-Reply 20–21.

We are persuaded by Dr. Holberg's testimony, that Dr. Hanumolu's sketches inexplicably divorce slew rate from delay, and that it is likely that no circuit could possibly generate the waveforms in Dr. Hanumolu's sketches. Ex. 1018 ¶¶ 73–74. We are persuaded by Dr. Holberg's testimony that Dr. Holberg's simulation shows that adjusting the slew rate results in adjusting the delay. Ex. 1018 ¶ 78. Patent Owner's contention that effects other than slew rate can influence the delay does not countermand Dr.

Holberg's testimony that adjusting the slew rate results in adjusting the delay.

(b) Dr. Holberg's timing diagrams

Patent Owner contends that the Petition did not provide any explanation regarding how Dr. Holberg's timing diagrams were produced. PO Resp. 68. Patent Owner contends that the timing diagrams depict the relative ordering of signal transitions, but prevent a person of ordinary skill from determining the actual delays between signal transitions. PO Resp. 70–71. Patent Owner contends that Dr. Holberg's timing diagrams are incorrect. PO Resp. 74–80. Patent Owner contends that Dr. Hanumolu corrected the error in Dr. Holberg's timing diagrams, and contends that Dr. Hanumolu's correction shows that the delay through Ajit's circuit does not respond inversely to PVT effects on other components. PO Resp. 81–83. According to Patent Owner, Dr. Holberg's timing diagrams should not be given any weight. PO Resp. 72.

Petitioner contends that Dr. Hanumolu's correction to Dr. Holberg's timing diagrams is incorrect. Reply 30–31. Petitioner acknowledges that Dr. Holberg made a minor error in his timing diagrams, but that the timing diagrams were not meant to be precise. Reply 31, n.1. Petitioner contends that the timing diagrams were meant as aids to the audience to illustrate the relationship between p0_gate and p2_gate and to show that voltage at node 222 would dip lower for quickly falling p0_gate than slowly falling p0_gate. *Id.*

Patent Owner contends that Petitioner relied heavily on Dr. Holberg's timing diagrams as a basis to show the claimed inverse response. PO Sur-Reply 17–18. Patent Owner contends that when the error is corrected using

Dr. Hanumolu's simulations, Ajit performs exactly opposite of Petitioner's characterizations. PO Sur-Reply 18.

We do not agree with Patent Owner that Petitioner relied heavily on Dr. Holberg's timing diagrams as a basis to show the claimed inverse response. Rather, as discussed above, the Petition relied heavily on the disclosure of Ajit to show the claimed inverse response. Pet. 66–83 (citing Ex. 1005, Abstract, 1:19–25, 1:27–31, 2:9–24, 3:19–24, 3:57–58, 4:2–4, 4:13–33, Fig. 2A). For example, support for the contention that "[w]hen the PVT condition is such that the fall of the p0_gate signal is fast . . . it takes longer for p2_gate signal to fall . . . resulting in a longer delay" relies on an extensive analysis of PVT compensator circuit 116 shown in Figure 2A of Ajit. Pet. 71–75. Similarly, support for the contention that "when PVT condition is such that the fall of the p0_gate is slow . . . the shorter the state change delay for p2_gate from high to low" relies on an extensive analysis of PVT compensator circuit 116 shown in Figure 2A of Ajit. Pet. 75–78. Patent Owner did not challenge the Petition's extensive analysis of the PVT compensator circuit shown in Figure 2A of Ajit.

We agree with Dr. Holberg that Dr. Holberg's timing diagrams are sketches summarizing and illustrating the relationship between p0_gate and p2_gate, and showing that voltage at node 222 would dip lower for quickly falling p0_gate than for slowly falling p0_gate. Ex. 1018 ¶ 80. We agree with Dr. Hanumolu, that such sketches are used to illustrate and explain definitions and relationships in a general way, and are not intended as a quantitative measure that requires thorough analysis. Ex. 1017, 42:3–45:14. We rely on the Petition's extensive analysis of the PVT compensator circuit

shown in Figure 2A in determining that Ajit teaches the inverse response as claimed, as discussed above and below.

(c) Petitioner's argument is based on inherency

Patent Owner contends that Petitioner relies on timing diagrams created by Dr. Holberg to argue that the circuits in Ajit must operate in a manner that adapts the delay inversely based on PVT effects of other components. PO Resp. 67. Patent Owner contends that reliance on the timing diagrams is an argument that Ajit inherently describes the delay of p2_gate based on PVT effects of other components. PO Resp. 67–68.

Petitioner contends that the Petition relies on the express disclosures of Ajit, and that Patent Owner's inherency argument is an attempt to cherry pick circuit simulations that allegedly do not show an inverse response to PVT. Reply 28–29. Dr. Holberg testifies that he relied on express disclosures of Ajit. Ex. 1018 ¶ 72.

We agree with Petitioner and Dr. Holberg, that the Petition relies on express disclosures of Ajit. Pet. 66–83 (citing Ex. 1005, Abstract, 1:19–25, 1:27–31, 2:9–24, 3:19–24, 3:57–58, 4:2–4, 4:13–33, Fig. 2A). With respect to the timing diagrams of Dr. Holberg cited in the Petition, as discussed above, we determine that the Petition did not rely on the timing diagrams to show that the output signal varies inversely to effects of PVT on the input signal. Rather, Petitioner and Dr. Holberg mainly rely on the express disclosure of Ajit to show the inverse relationship. For example, the Petition's analysis that "when PVT condition is such that p0_gate falls quickly . . . p2_gate will fall slowly resulting in a longer delay for the p2_gate state change," relies on the disclosure of the PVT compensator circuit shown in Figure 2A of Ajit and persuasively shows the inverse

relationship. Pet. 71–75 (citing Ex. 1005, Fig. 2A; Ex. 1002 ¶¶ 144–151). Patent Owner did not challenge Dr. Holberg's analysis of the PVT compensator circuit described by Ajit. We are not persuaded by Patent Owner's contention that because the Petition cites Dr. Holberg's timing diagrams, the Petition relies on inherency.

(d) Dr. Hanumolu's simulations show that the delay circuit of Ajit does not adapt the delay inversely to the PVT effects on other components.

Patent Owner contends that Dr. Hanumolu's simulations of the delay circuit of Ajit show an increased delay of the p2_gate signal caused by a slowly falling p0_gate signal, in contrast to Dr. Holberg's sketches, which show a reduced delay. PO Resp. 80–86 (citing Ex. 2044 ¶¶ 92–98). Petitioner contends that Dr. Hanumolu "cherry-picked self-serving and unreasonable values to fabricate simulations that intentionally contradict the purpose of Ajit, i.e., to keep the slew rate at PAD 102 in Fig. 1 constant over PVT." Reply 33 (citing Ex. 1018 ¶ 82; Ex. 1017, 83:2–86:13); *see id*. at 33–34 (citing Ex. 1005, 2:21–23, 3:19–24, 4:13–23, Fig. 1; Ex. 1018 ¶¶ 83–84; Ex. 1017, 74:16–75:7). Petitioner also contends that Dr. Hanumolu was silent on transistor sizing. Reply 34 (citing Ex. 1018 ¶¶ 85–86; Ex. 2044 ¶ 93).

Petitioner, relying on simulations from Dr. Holberg, contends Dr. Hanumolu's simulation results are incorrect. Reply 30–37. Petitioner contends that Dr. Holberg used the same LTspice simulator as Dr. Hanumolu, and the values disclosed by Dr. Hanumolu, to perform his own simulations. Reply 34 (citing Ex. 1018 ¶¶ 87–90; *see id.* ¶¶ 85–86). Petitioner contends that Dr. Holberg selected transistor sizing to generate simulations consistent with the express disclosures of Ajit. *Id*. Petitioner

contends that Dr. Holberg's simulations, when measured at 50%, show that the delay between p0_gate and p2_gate for a fast falling p0_gate signal is longer than the delay for a slow falling p0_gate signal, which is an inverse response. Reply 34–36 (citing Ex. 1018 ¶¶ 87–92). Petitioner contends that even Dr. Hanumolu's simulation results show an inverse response when comparing the delay between input and output as measured at 50%. Reply 37–38 (citing Ex. 1018 ¶ 93).

Patent Owner contends that Dr. Holberg has no basis to allege that Dr. Hanumolu's simulations are inconsistent with Ajit's teachings on the pad voltage. PO Sur-Reply 22. Patent Owner contends that Dr. Hanumolu's simulations used the input waveforms that Dr. Holberg used in his original declaration. *Id*. Patent Owner contends that Petitioner did not provide transistor sizes in the Reply. PO Sur-Reply 22–23. Patent Owner contends that the Reply changes the way the delay is measured as compared to the Petition. PO Sur-Reply 23. Patent Owner contends that its simulations do not model Ajit under all conditions, but show that under one set of conditions Ajit's delay circuit does not adjust delay inversely. PO Sur-Reply. 23–24. Patent Owner contends that Dr. Holberg relied on unreasonable values for the ratio between the PMOS and NMOS transistors. PO Sur-Reply. 25. Patent Owner contends that the Petition measured delay from when the p0_gate signal starts to fall to when the p2_gate signal starts to fall. PO Sur-Reply 25–26. Patent Owner contends that Dr. Holberg's measuring of delay at 50% is arbitrary and unsubstantiated as a proper point of measurement. PO Sur-Reply 25–29. According to Patent Owner, to determine the most accurate approach is to use a voltage level that causes the transistor that receives the signal to change state. PO Sur-Reply 29–30.

We do not need to resolve the issues of whether Dr. Holberg or Dr. Hanumolu used more accurate values in their respective simulations, because both simulations provide evidence to support Petitioner's contentions if we measure delay at 50%, and both simulations provide evidence to support Patent Owner's contentions if we measure delay when the signals start to fall. We find Petitioner's contention that delay is measured at 50% more persuasive, because it is consistent with the knowledge of a person of ordinary skill, it is consistent with evidence provided by the inventor of the '659 patent, and it is consistent with Patent Owner's contention that "[t]o determine when an analog signal changes state, the most accurate approach is to use a voltage level that causes the transistor that receives the signal to change state." Ex. 1018 ¶¶ 90, 93 (citing Ex. 1019, 207; Ex. 2006, 32; Ex. 2035, 32); Ex. 1019, 207; Ex. 2006, 32, Fig. 28; PO Sur-Reply 29–30.

We agree with Dr. Holberg, that a person of ordinary skill would have "measure[d] delay time at 50% input and output level." Ex. 1018 ¶ 90. Dr. Holberg cites to a textbook which defines the delay time as the "time difference between input transition (50%) and the 50% output level. (This is the time taken for a logic transition to pass from input to output.)." Ex. 1019, 207. We also agree with Dr. Holberg, that the inventor of the '659 patent measured the delay of the q_{TIMER} circuit at 50%, as shown by the blue and red triangular markers and vertical lines in Figure 28 of the Design Review document. Ex. 2006, 32, Fig. 28. Dr. Holberg provides persuasive evidence that a person of ordinary skill would have used the voltage level at 50% of the p0_gate signal and the voltage level at 50% of p2_gate signal when measuring the delay.

We are not persuaded by Patent Owner's contention that Dr. Holberg measured delay in the sketches of his original declaration from when the input and output signals began to fall. We agree with Dr. Holberg that "these sketches were not meant to be precise." Ex. 1018 ¶ 80; *see* Ex. 2047, 66:18–67:25 ("I didn't measure delay. I'm showing the relationship between the p0 and p2 gates." "I have no time scale on here. It's just trying to indicate the relationship in the two signal(s)." "I didn't state a delay value or an amount. I'm just simply showing that one occurred before the other in time."). We agree with Dr. Hanumolu, that such sketches are used to illustrate and explain definitions and relationships in a general way, and are not intended as a quantitative measure that requires thorough analysis. Ex. 1017, 42:3–45:14.

Further, Patent Owner's contention is inconsistent with Figure 28 of the Design Review introduced by Patent Owner, which measures delay at 50%. Ex. 2006, 32; Ex. 1018 ¶¶ 90, 93. Patent Owner's contention that delay is measured from when the input and output signals begin to fall is also inconsistent with Patent Owner's contention that a more accurate approach is to use a voltage level that causes the transistor that receives the signal to change state. PO Sur-Reply 29–30.

Dr. Holberg's testimony is consistent with Patent Owner's contention that a more accurate approach is to use a voltage level that causes the transistor that receives the signal to change state. Dr. Holberg testifies that "when the PVT condition is such that p0_gate falls quickly . . . p2_gate will fall slowly, resulting in a longer delay for the *p2_gate state change*." Ex. 1002 ¶ 151. Dr. Holberg also testifies that "[w]hen PVT condition is such that the fall of p0_gate signal is slow . . . the shorter the *state change*

delay for p2_gate from high to low." Ex. 1002 ¶ 152; *see id.* ¶ 143 ("It is well known to a POSITA that NMOS transistors turn on when the gate voltage is above the threshold of the transistor plus V_{SSC}, whereas PMOS transistors turn on when the gate voltage is below V_{DDO} less the threshold voltage."); *see generally* ¶¶ 142–156 (discussing when the transistors of Figure 2A of Ajit turn on and off, thus changing state). Thus, contrary to Patent Owner's contention, the Petition and Dr. Holberg measure delay using voltage levels that cause the transistors to change state. As discussed above, Dr. Holberg provides persuasive evidence that a person of ordinary skill would have used 50% as the voltage level that causes a transistor to change state when reading the simulations provided by Dr. Holberg and Dr. Hanumolu to measure the delay between the input and output signals.

Similarly, we are not persuaded by Patent Owner's contention that measuring delay at 50% is a new argument. As discussed above, the Petition relied on the express disclosure of Ajit to show the claimed "output voltage vary inversely in response to PVT effects on other components of the integrated circuit." Dr. Holberg, when evaluating Dr. Hanumolu's simulations, as well as his own, provided testimony and evidence showing that a person of ordinary skill would have measured delay at 50%. Ex. 1018 ¶¶ 90, 93. This is not new argument, but instead is appropriately responsive to Patent Owner's arguments and legitimately serves to document the knowledge that skilled artisans would bring to bear in reading the simulations provided by Dr. Holberg and Dr. Hanumolu. *See Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015).

We are not persuaded by Patent Owner's contention that Dr. Holberg's simulations do not respond to any inherency argument made by

Patent Owner in the Response. PO Sur-Reply 23–24. Contrary to Patent Owner's contention, the Petition relies on express disclosures of Ajit, not inherency, to show the inverse response. Pet. 66–83. Thus, we are not persuaded by Patent Owner that Patent Owner's Response was merely addressing an inherency argument by Petitioner. Further, Petitioner provided Dr. Holberg's simulations to rebut Patent Owner's contention that Dr. Hanumolu's revised sketches of Dr. Holberg's sketches were accurate, and to rebut Patent Owner's contention that Dr. Hanumolu's simulations were accurate and consistent with Ajit's express disclosures. *See* Reply 28–38.

We agree with Dr. Holberg, that both Dr. Holberg's simulations and Dr. Hanumolu's simulations show that Ajit discloses "output voltage vary inversely in response to PVT effects on other components of the integrated circuit." Reply 35–38 (citing Ex. 1018 ¶¶ 87–93); Ex. 1018 ¶¶ 90, 93 (citing Ex. 2044 ¶ 96). We rely on the testimony of Dr. Holberg in determining that Ajit describes the claimed "output voltage vary inversely in response to PVT effects on other components of the integrated circuit."

For the reasons set forth by Petitioner and explained above, we are persuaded that Ajit discloses all of the limitations of claim 9. The Petition and supporting testimony of Dr. Holberg has shown by a preponderance of the evidence that claim 9 is anticipated by Ajit.

Claim 10 recites "the voltage threshold is set by determining when an output voltage of the capacitive element is within a voltage threshold of a second supply voltage, opposite from the first supply voltage." Petitioner contends that Ajit discloses this limitation. Pet. 83–84 (citing Ex. 1005, Fig. 2A; Ex. 1002 ¶ 168). Patent Owner does not argue claim 10 separately,

but instead relies on arguments presented for claim 9 which we find unpersuasive as discussed above in our analysis of claim 9. PO Resp. 63–86. Petitioner's analysis of claim 10, supported by testimony of Dr. Holberg (Ex. 1002 ¶ 168), which we credit, is persuasive that claim 10 is anticipated by Ajit.

Claim 11 recites "the generated output voltage is a same voltage as the input signal." Petitioner contends that Ajit discloses this limitation for the reasons given on pages 66–78 of the Petition. Pet. 85 (citing Ex. 1005, Fig. 2A; Pet. 66–78). Patent Owner does not argue claim 11 separately, but instead relies on arguments presented for claim 9 which we find unpersuasive as discussed above in our analysis of claim 9. PO Resp. 47. Petitioner's analysis of claim 11, supported by testimony of Dr. Holberg (Ex. 1002 ¶ 170), which we credit, is persuasive that claim 11 is anticipated by Ajit.

G. Obvious over Ajit and AAPA (Claims 1 and 5)

Claim 1 recites "a preamplifier responsive to a first control signal." Petitioner contends that this limitation is taught by Figure 1 of the AAPA. Pet. 87 (citing Ex. 1001, 1:16–34, Fig. 1).

Claim 1 recites "a latch responsive to a second control signal." Petitioner contends that this limitation is taught by Figure 1 of the AAPA. Pet. 88 (citing Ex. 1001, 1:16–34, Fig. 1).

Claim 1 recites "a delay element having an input for the first control signal and output for the second control signal." Petitioner contends this limitation is taught by Ajit in disclosing a PVT compensator circuit having an input for the first control signal p0_gate and an output for the second control signal p2_gate. Pet. 88 (citing Ex. 1005, Fig. 1 element 116).

Claim 1 recites "the delay element having a circuit structure to adaptively increase or decrease delay propagation of the first control signal in a manner that counteracts PVT effects present in other components of the comparator." Petitioner contends Ajit teaches this limitation for the reasons given in Petitioner's analysis of claim 9 as anticipated by Ajit. Pet. 89.

Petitioner contends that a person of ordinary skill would have replaced the delay element shown in the AAPA with the adaptive delay element shown by PVT compensator circuit 116 of Ajit to yield the predictable benefit of using an adjustable delay to counteract PVT effects as taught by Ajit. Pet. 86 (citing Ex. 1005, 1:33–36; Ex. 1002 ¶¶ 171–172), 88. Dr. Holberg testifies that "when the PVT condition is such that p0_gate falls quickly . . . p2_gate will fall slowly, resulting in a longer delay for the p2_gate state change." Ex. 1002 ¶ 151. Dr. Holberg also testifies that "[w]hen PVT condition is such that the fall of p0_gate signal is slow . . . the shorter the state change delay for p2_gate from high to low." Ex. 1002 ¶ 152. Dr. Holberg further testifies that replacing the fixed delay of the AAPA with the PVT compensator circuit of Ajit is the simple substitution of one known element for another that yields the predictable result of compensating for PVT variations. Ex. 1002 ¶¶ 171–173. We are persuaded by Dr. Holberg's testimony that a person of ordinary skill would have replaced the fixed delay circuit of the AAPA with the adjustable delay circuit of Ajit to yield the predictable benefit of counteracting PVT effects as taught by Ajit.

Patent Owner contends that Ajit does not disclose the elements of claim 1 for the reasons given in Patent Owner's analysis of claim 9. PO

Reply 86–87. We are not persuaded by Patent Owner's contentions for the reasons given in our analysis of claim 9 above.

Patent Owner contends that the Petition has not established a motivation to combine the teachings of the AAPA and Ajit. PO Resp. 87. Patent Owner contends that (a) a person of ordinary skill would not recognize that Ajit teaches an adaptive delay because Ajit does not describe the benefits of an adaptive delay nor describe providing an adaptive delay, (b) Ajit is non-analogous to claim 1, because Ajit compensates for slew rate but claim 1 adjusts delay propagation of a timing signal, and (c) operating Ajit's PVT compensator circuit to result in an inverse adjustment of delay based on PVT effects would be unpredictable, because Ajit's circuit responds to PVT in a correlated manner, not inversely. PO Resp. 87–89; PO Sur-Reply 30.

We find Petitioner's arguments the most persuasive. We agree with Dr. Holberg, that a person of ordinary skill would have recognized that Ajit discloses an adaptive delay device, and would have recognized the relationship between p0_gate and p2_gate slew rates and delay. Ex. 1002 ¶¶ 134–170; Ex. 1018 ¶ 94. We also agree with Petitioner, that Ajit is analogous art because it is in the same field of endeavor as the '659 patent, namely, compensating for PVT effects in a circuit. Ex. 1001, 1:5–8; Ex. 1005, Abstract; Ex. 1018 ¶ 95. We agree with Dr. Holberg, that Ajit's circuit adjusts delay inversely to PVT. Ex. 1002 ¶¶ 134–170; Ex. 1018 ¶ 96.

For the reasons set forth by Petitioner and explained above, we are persuaded that Ajit and the AAPA teach all of the limitations of claim 1, and that a person of ordinary skill would have combined the teachings of the references to achieve the comparator recited in the claim and would have

had a reasonable expectation of success in doing so. Dr. Holberg's testimony provides sufficient evidence of motivation that a person of ordinary skill would have used the adaptive delay within the circuit of the AAPA and would have had a reasonable expectation of success in doing so. Dr. Holberg's testimony also provides persuasive evidence that the combination of Ajit and the AAPA teaches that the '659 "patent claims a structure already known in the prior art (the AAPA circuit shown in Figure 1 of the '659 patent) that is altered by the mere substitution of one element (the fixed delay) for another known in the field (Ajit's PVT compensator circuit with an adjustable delay)" and does no more "than yield a predictable result" of a comparator with an adjustable delay to compensate for PVT effects. Petitioner has proven by a preponderance of the evidence that claim 1 would have been obvious over Ajit and the AAPA.

Claim 5 recites "a comparator for determining whether an input signal is representative of a digital high or low signal." Petitioner contends that Ajit teaches this limitation in disclosing a comparator. Pet. 89–90 (citing Pet. 87, Ex. 1001, 1:16–34, Fig. 1).

Claim 5 recites "an adaptive delay device having an input for receiving a control signal and an output connected to the comparator." Petitioner contends that Ajit teaches this limitation in disclosing PVT compensator circuit 116. Pet. 90 (citing Ex. 1002 ¶ 182).

Claim 5 recites "the adaptive delay device is configured to respond inversely to the response of other circuit components forming the successive approximation register analog-to-digital converter, and output the control signal to the comparator based on the inverse response of the adaptive delay device." Petitioner contends that Ajit teaches the adaptive delay device

configured to respond inversely to the response of other circuit components, and that Figure 1 of the AAPA teaches a comparator configuration within a SAR ADC. Pet. 91 (citing Ex. 1001, 2:9–10, Fig. 1).

Petitioner contends that a person of ordinary skill would have connected the adaptive delay circuit of Ajit to the comparator of the AAPA to yield the predictable benefit of compensating for PVT effects. Pet. 85–86, 90 (citing Ex. 1002 ¶¶ 171–173, 182). Dr. Holberg testifies that a person of ordinary skill would have connected the adaptive delay device of Ajit to the comparator of the AAPA to yield the predictable result of compensating for PVT effects. Ex. 1002 ¶ 182 (citing Ex. 1008; Ex. 1004).

Patent Owner does not argue separately claim 5, but instead relies on arguments presented for claim 1, which we find unpersuasive as discussed in our analysis of claim 1. PO Resp. 86–89. Petitioner's analysis for claim 5, supported by the testimony of Dr. Holberg (Ex. 1002 ¶¶ 179–183), which we credit, is persuasive that claim 5 would have been obvious over Ajit and the AAPA.

IV. MOTION TO EXCLUDE EVIDENCE

Petitioner filed a Motion to Exclude Evidence seeking to exclude Exhibit 2030 in its entirety, paragraphs 20–22 of Exhibit 2001, and paragraphs 92–98 of Exhibit 2044. Paper 30. Even without excluding this evidence, we have determined that Petitioner has established, based on a preponderance of the evidence, the unpatentability of claims 1–11 of the '659 patent. Furthermore, Petitioner's arguments on these items go to the weight to be accorded to the evidence. The Board is capable of determining and assigning the appropriate weight to the evidence.

For these reasons, we *deny* Petitioner's motion.

V. CONCLUSION

As summarized in the table below, the Petition and supporting evidence has shown by a preponderance of the evidence that claims 1–11 of the '659 patent are unpatentable.[7]

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
5, 6, 9	102(a)	Yoshioka	5, 6, 9	
10	103	Yoshioka	10	
1, 2	103	Yoshioka, Applicant's Admitted Prior Art (AAPA)	1, 2	
7, 8	103	Yoshioka, Fiscus	7, 8	
3, 4	103	Yohioka, AAPA, Fiscus	3, 4	
9–11	102(b)	Ajit	9–11	
1, 5	103	Ajit, AAPA	1, 5	
Overall Outcome			1–11	

[7] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

VI. ORDER

Upon consideration of the record before us, it is:

ORDERED that claims 1–11 of the '659 patent are unpatentable;

FURTHER ORDERED that Petitioner's motion to exclude is denied; and

FURTHER ORDERED because this is a final written decision, the parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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