UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, CAVIUM, LLC, and DELL INC.,

Petitioners,

v.

ALACRITECH, INC.,

Patent Owner.

Case No. IPR2017-01410[1]
U.S. Patent No. 8,131,880

PETITIONER CAVIUM, LLC'S NOTICE OF APPEAL

[1] Cavium, LLC, which filed a Petition in Case IPR2017-01737, and Dell Inc., which filed a Petition in Case IPR2018-00339, have been joined as petitioners in this proceeding.

Pursuant to 35 U.S.C. §§ 141(c) and 319, and 37 C.F.R. § 90.2(a), notice is hereby given that Petitioner Cavium, LLC appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision on Remand, entered July 20, 2021 (Paper 88) in IPR2017-01410, attached as Exhibit A, the Decision Denying Petitioner's Request on Rehearing of Final Written Decision on Remand, entered June 13, 2022 (Paper 93), and all prior and interlocutory rulings related thereto or subsumed therein.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Petitioner states that the issues for appeal include the ruling that claims 41-43 of U.S. Patent No. 8,131,880 are not unpatentable and all other issues decided adversely to Petitioner in any orders, decisions, rulings, and opinions underlying or supporting the Final Written Decision on Remand and Decision Denying Petitioner's Request on Rehearing of Final Written Decision on Remand.

Pursuant to 37 C.F.R. § 90.3, this Notice of Appeal is timely, having been duly filed within 63 days after the date of the Decision Denying Petitioner's Request on Rehearing of Final Written Decision on Remand.

A copy of this Notice of Appeal is being filed simultaneously with the Patent Trial and Appeal Board, the Clerk's Office for the United States Court of Appeals for the Federal Circuit, and the Director of the U.S. Patent and Trademark Office.

Dated: August 2, 2022

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that, on August 1st, 2022, the foregoing PETITIONER CAVIUM, LLC'S NOTICE OF APPEAL was:

(1) electronically filed through PTAB E2E

(2) filed by Express Mail with the Director of the United States Patent and Trademark Office, at the following address:

Office of the General Counsel
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

(3) filed in the U.S. Court of Appeals for the Federal Circuit using the Court's CM/ECF filing system and pay.gov to pay the filing fee electronically

(4) provided as a courtesy copy via electronic mail to the following attorneys of record for the Patent Owner listed below:

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EXHIBIT A

Trials@uspto.gov
571-272-7822

Paper No. 88
Date: July 20, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, CAVIUM, LLC, and DELL, INC.,
Petitioner,

v.

ALACRITECH, INC.,
Patent Owner.

Case IPR2017-01410
Patent 8,131,880 B2

Before CHARLES J. BOUDREAU, STEVEN M. AMUNDSON, and JASON M. REPKO, *Administrative Patent Judges*.

BOUDREAU, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision on Remand
Determining Some Challenged Claims Unpatentable
35 U.S.C. §§ 144, 318

I. INTRODUCTION

We address this case on remand after a decision by the U.S. Court of Appeals for the Federal Circuit in *Alacritech, Inc. v Intel Corp.*, 966 F.3d 1367 (Fed. Cir. 2020).

A. Background and Summary

Intel Corporation filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 32, 34, 35, 37–39, and 41–43 ("the challenged claims") of U.S. Patent No. 8,131,880 B2 (Ex. 1001, "the '880 patent") on the following grounds:

Claim(s) Challenged	35 U.S.C. §[1]	Reference(s)/Basis
32, 34, 35, 39, 41–43	103(a)	Thia,[2] Tanenbaum[3]
37, 38	103(a)	Thia, Tanenbaum, Nahum[4]

Pet. 14. Alacritech, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7). On November 21, 2017, based on the record before us at that

[1] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the '135 patent issued from an application filed before March 16, 2013, we apply the pre-AIA version of the statutory basis for unpatentability.

[2] Y.H. Thia and C.M. Woodside, "A Reduced Operation Protocol Engine (ROPE) for a Multiple-Layer Bypass Architecture," 1995 ("Thia," Ex. 1015).

[3] Andrew S. Tanenbaum, Computer Networks, Third Edition, 1996 ("Tanenbaum" or "Tanenbaum96," Ex. 1006).

[4] Erich M. Nahum et al., "Performance Issues in Parallelized Network Protocols," Proceedings of the First Symposium on Operating Systems Design and Implementation, November 1994 ("Nahum," Ex. 1079).

time, we[5] instituted an *inter partes* review of the challenged claims on the asserted grounds. Paper 8, 19 ("Decision on Institution" or "Dec. on Inst.").

In response to petitions and requests for joinder filed in IPR2017-01737 and IPR2018-00339, we joined Cavium, Inc. and Dell, Inc., respectively, as petitioners in this proceeding. *See* IPR2017-01737, Paper 8; IPR2018-00339, Paper 9. According to an updated mandatory notice filed in this proceeding, Cavium, Inc. subsequently was converted to Cavium, LLC. Paper 72. Intel Corporation, Cavium, LLC, and Dell, Inc. are identified herein collectively as "Petitioner."

Patent Owner filed a Patent Owner Response on February 24, 2018 (Paper 32, "Response" or "PO Resp."), and Petitioner filed a Reply on May 15, 2018 (Paper 42, "Pet. Reply"). Patent Owner also filed a Contingent Motion to Amend under 37 C.F.R. § 42.121, proposing amended claims 79–87 to be substituted in place of original claims 32, 34, 35, 37–39, and 41–43, respectively, should any of the latter be found unpatentable. Paper 20. Petitioner filed an Opposition to the Contingent Motion to Amend, Patent Owner filed a Reply to Petitioner's Opposition, and Petitioner filed a Sur-reply. Papers 38, 43, 50.

An oral argument was held on September 13, 2018, and a transcript has been entered into the record as Paper 73 ("Tr.").

On November 14, 2018, following consideration of the full record developed during trial, we issued a Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. Paper 77 ("Final Dec."). In that

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[5] Due to unavailability, original panel members Stephen C. Siu and Daniel N. Fishman have been replaced by Administrative Patent Judges Steven M. Amundson and Jason M. Repko. *See* Paper 84.

decision, we concluded that Petitioner had established by a preponderance of the evidence that all the challenged claims are unpatentable on the asserted grounds, and we also denied Patent Owner's Contingent Motion to Amend after determining that the proposed substitute claims also were unpatentable. *Id.*

Patent Owner appealed to the Federal Circuit, alleging error in our holding the challenged claims unpatentable.[6] *Alacritech*, 966 F.3d at 1369. In a decision issued on July 31, 2020, the Federal Circuit affirmed our conclusion that claims 32, 34, 35, and 37–39 are unpatentable, but held that the Final Written Decision did not adequately support the finding that the asserted prior-art combination teaches or suggests the "re-assembler" limitations recited in claims 41–43 that "require that reassembly take place in the network interface as opposed to a central processor." *Id.* at 1369–74. Accordingly, the Court vacated the determination of unpatentability as to claims 41–43 and remanded for further proceedings regarding those claims. *Id.* at 1373.

We held a conference call with counsel for the parties on January 29, 2021, to discuss the procedure on remand. A transcript of that call has been filed as Exhibit 1262. In an Order entered February 23, 2021, we authorized the parties to file simultaneous supplemental briefs limited to addressing the sufficiency of Intel's showing at trial as to whether the asserted prior art teaches or suggests the limitation identified by the Federal Circuit. Paper 85.

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[6] In its appeal briefing, Patent Owner also asserted, but subsequently withdrew and waived, a challenge to the appointment of the Board's Administrative Patent Judges under the Appointments Clause of the Constitution. *Alacritech*, 966 F.3d at 1370 n.3.

In compliance with that Order, the parties filed their respective briefs on March 5, 2021. Paper 86 ("PO Remand Br."); Paper 87 ("Pet. Remand Br.").

As we explain above, claims 32, 34, 35, and 37–39 are not at issue on remand because the Federal Circuit upheld our determination of unpatentability with respect to those claims. Accordingly, the only claims that remain for our consideration are claims 41–43. For the reasons discussed below, we conclude, in view of the Federal Circuit's decision, the record previously developed during trial, and the post-remand briefing, that Petitioner has not shown by a preponderance of the evidence that claims 41–43 of the '880 patent are unpatentable.[7]

B. Related Matters

The parties have indicated that the '880 patent is asserted in *Alacritech, Inc. v. CenturyLink, Inc.*, 2:16-cv-00693-JRG-RSP (E.D. Tex.); *Alacritech, Inc. v. Wistron Corp.*, 2:16-cv-00692-JRG-RSP (E.D. Tex.); and *Alacritech, Inc. v. Dell Inc.*, 2:16-cv-00695-RWS-RSP (E.D. Tex.). Paper 69, 2; Paper 70, 2. Additionally, claims 1, 5–10, 12, 14, 16, 17, 20–23, 27, 28, 45, and 55 of the '880 patent were challenged in separate petitions for *inter partes* review filed by Intel Corporation in IPR2017-01409;

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[7] As noted above, we denied Patent Owner's Contingent Motion to Amend in the Final Written Decision following determination that the proposed substitute claims were unpatentable. *See* Final Dec. 24–26. We do not understand Patent Owner to have appealed the denial of that Motion. Nonetheless, in view of our conclusion herein that claims 41–43 have not been shown to be unpatentable, we conclude that Patent Owner's Contingent Motion to Amend is not properly reached to the extent it relates to substitute claims 85–87, i.e., the claims contingently proposed as substitutes for claims 41–43 in the event claims 41–43 had been shown unpatentable. The denial of the Motion as it relates to substitute claims 79–84 is unaffected by this Decision.

Cavium, Inc. in IPR2017-01736; and Dell, Inc. in IPR2018-00338. Following institution of *inter partes* review in IPR2017-01409, Cavium, Inc. and Dell, Inc. were joined as petitioners therein, pursuant to motions for joinder filed with the petitions in IPR2017-01736 and IPR2018-00338. In a final written decision entered on November 14, 2018, the Board held all challenged claims to be unpatentable. IPR2018-01409, Paper 79. Patent Owner appealed that decision to the Federal Circuit, which affirmed the Board's decision. *Alacritech*, 966 F.3d at 1373–74.

C. The '880 Patent

The '880 patent describes a system and method for performing network processing tasks on a network interface card. Ex. 1001, 3:45–47.

D. Claims on Remand

Claims 41–43 are reproduced below, with limitations at issue on remand italicized:

> 41. An apparatus for transferring a packet to a host computer system, comprising:
>
> a traffic classifier, disposed in a network interface for the host computer system, configured to classify a first packet received from a network by a communication flow that includes said first packet;
>
> a packet memory, disposed in the network interface, configured to store said first packet;
>
> a packet batching module, disposed in the network interface, configured to determine whether another packet in said packet memory belongs to said communication flow;
>
> *a flow re-assembler, disposed in the network interface, configured to re-assemble a data portion of said first packet with a data portion of a second packet in said communication flow*; and

a processor, disposed in the network interface, that maintains a TCP connection for the communication flow, the TCP connection stored as a control block on the network interface.

42. The apparatus of claim 41, wherein said traffic classifier comprises:

a parser configured to parse a header portion of said first packet;

a flow database configured to store a flow key identifying said communication flow; and

a flow database manger configured to manage said flow database;

wherein said flow key is generated from an identifier of a source of said first packet and an identifier of a destination of said first packet.

43. A computer system for receiving a packet from a network, comprising:

a memory configured to store packets received from a network; and

a network interface for the computer system, the network interface configured to receive a first packet from said network, *the network interface comprising*:

a parser configured to extract information from a header portion of a first packet;

a flow manager configured to examine said information;

a flow database configured to store an identifier of a first communication flow comprising multiple packets, including said first packet; and

a re-assembler for storing data portions of said multiple packets without header portions in a first portion of said memory; and

> a processor for processing said first packet and for maintaining a TCP connection for the communication flow, the TCP connection stored as a control block on the network interface.

Ex. 1001, 93:60–94:45 (emphasis added).

E. Asserted Ground on Remand

As stated in Section I.A above, the Petition asserts that claims 41–43 are unpatentable over Thia and Tanenbaum, and that is the only ground before us on remand.

II. ANALYSIS

A. Legal Standards

In an *inter partes* review, the petitioner has the burden of proving unpatentability by a preponderance of the evidence. 35 U.S.C. § 316(e). That burden never shifts to the patentee. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The legal question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;[8] and (4) when in evidence, objective

[8] Petitioner contends that a person having ordinary skill in the art ("POSA") with respect to the technology described in the '880 patent "would be a person with at least the equivalent of a B.S. degree in computer science,

evidence of obviousness or nonobviousness, i.e., secondary considerations.[9] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). One seeking to establish obviousness based on more than one reference also must articulate sufficient reasoning with rational underpinnings to combine teachings. *See KSR*, 550 U.S. at 418.

We analyze the asserted grounds with the principles stated above in mind.

B. Brief Overview of the Cited References

1. Thia

Thia discloses a reduced operation protocol engine ("ROPE") that "offloads critical functions of a multiple-layer protocol stack, based on the

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computer engineering or electrical engineering with at least five years of industry experience including experience in computer architecture, network design, network protocols, software development, and hardware development." Pet. 24. Patent Owner proposes a slightly different assessment (i.e., "a person with a Bachelor's degree in Computer Science, Computer Engineering, or the equivalent, and several years' experience in the fields of computer networking and/or networking protocols"), but argues that "[a]ny differences between this and Petitioners' proposed level of ordinary skill would have no bearing on the analysis presented." PO Resp. 25. To the extent necessary for purposes of this Decision, we have adopted Petitioner's assessment.

[9] As discussed in the Final Written Decision, Patent Owner in its Patent Owner Response alleged that long-felt but unsolved need, commercial success, industry praise, failure of others, and expert and industry skepticism provide objective evidence of nonobviousness. *See* Final Dec. 15–19 (citing PO Resp. 58–63). Petitioner presented counterargument in its Reply. Pet. Reply. 20–24. After considering the parties' respective arguments, we explained in the Final Written Decision that we were not persuaded by Patent Owner's argument in this regard. Final Dec. 15–19. Patent Owner does not appear to have challenged that determination in its appeal to the Federal Circuit, and we see no reason to revisit it at this time.

'bypass concept' of a fast path for data transfer." Ex. 1015, 1. Thia explains that the ROPE is designed as an integrated circuit applicable to processing of Open Systems Interconnection ("OSI") Session and Transport layer protocols. *Id.* According to Thia, the ROPE architecture provides a bypass to selectively process certain send or receive operations in the ROPE circuit, thereby bypassing normal processing within the software protocol stack of the host processor reducing the processing load on the host. *Id.* at 2.

Figure 1 of Thia is reproduced below.

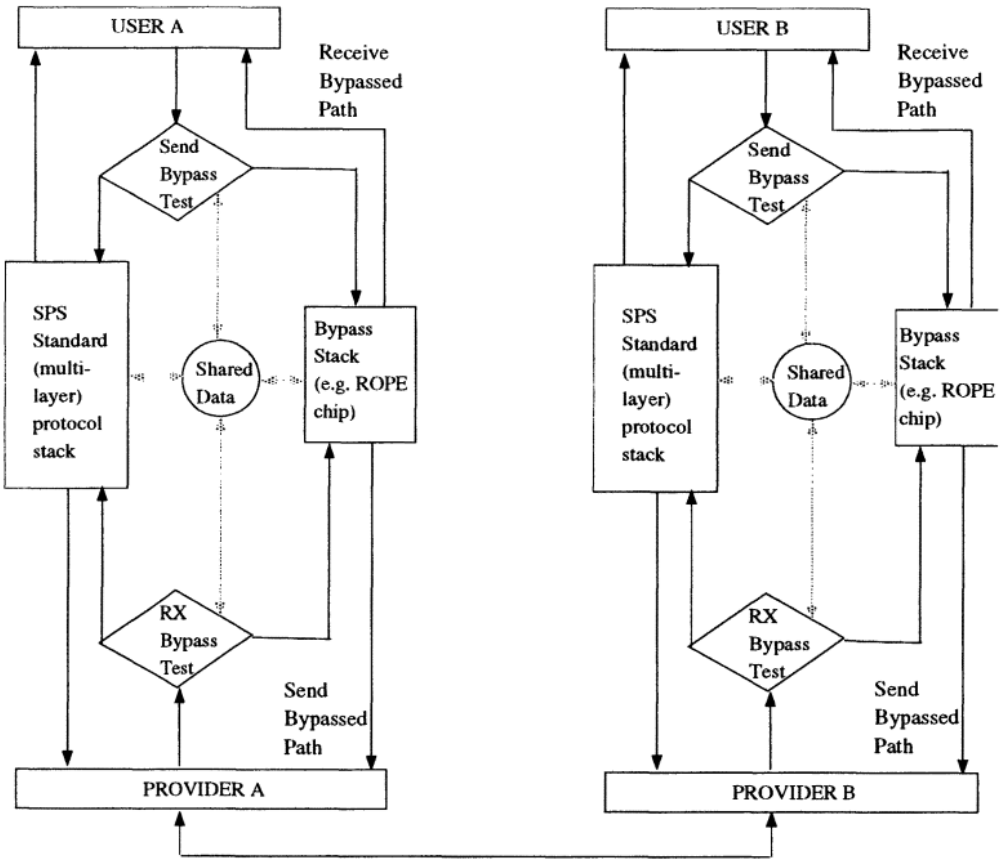

Figure 1 Bypass Architecture

Figure 1 of Thia, above, depicts a bypass architecture in which USER A and USER B communicate through a network. Ex. 1015, 3. The host processor for each user provides a standard protocol stack ("SPS"), a bypass stack (ROPE chip), a send bypass test, a receive ("RX") bypass test, and shared

data shared by all the above elements to coordinate processing between the SPS and the ROPE chip. *Id.* The send bypass test identifies outgoing packets that may be transmitted through the bypass stack, and the receive bypass test identifies an incoming protocol data unit ("PDU") that may be processed through the ROPE circuit. *Id.* When bypassable headers are identified (i.e., fast path data transfer is to be performed), the bypass stack (ROPE chip) "performs all the relevant protocol processing" for transfer of the data for such identified packets/PDUs that may bypass host processor (SPS) processing. *Id.* Without bypass, the SPS path is taken, including a single or multiple layers of a layered protocol stack. *Id.* The shared data is used to maintain state consistency between the SPS and bypass stack processing. *Id.*

Figure 2 of Thia is reproduced below.

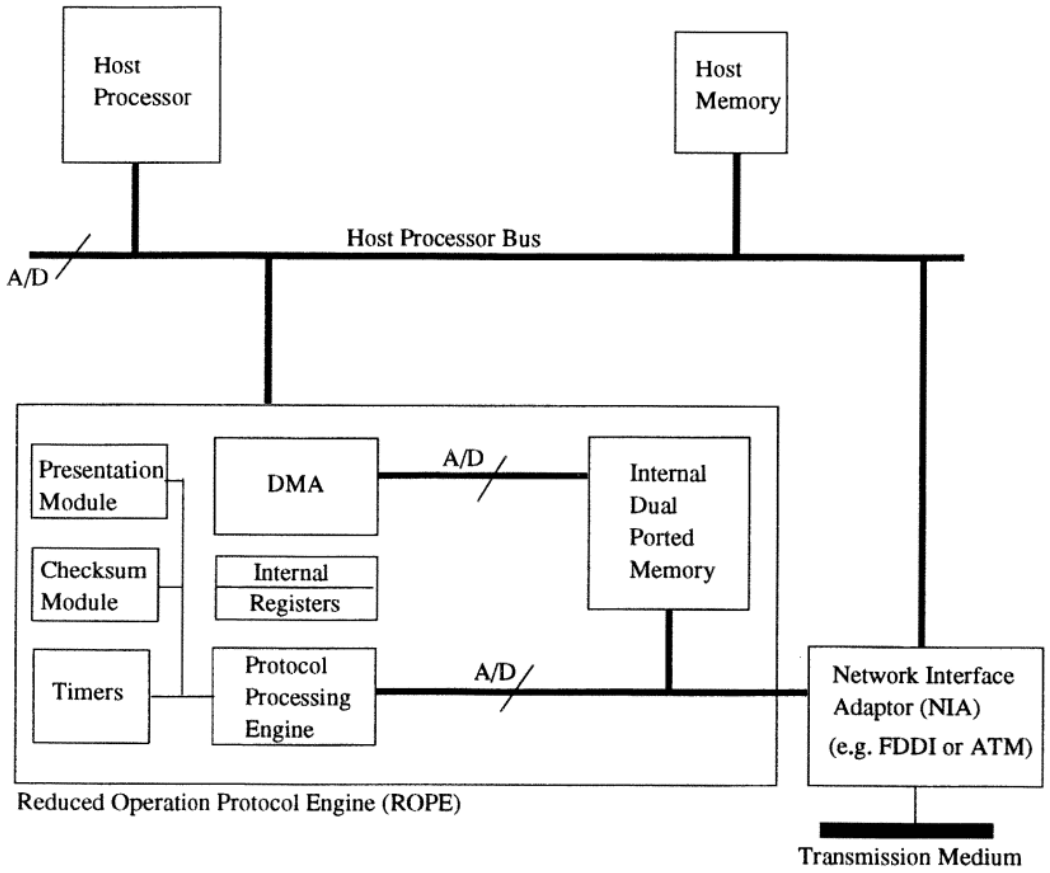

Figure 2 Block Diagram of VLSI bypass system

Figure 2 of Thia, above, is a block diagram of a VLSI bypass system incorporating a ROPE chip. Ex. 1015, 7. With reference to Figure 2, a host processor is coupled with host memory and a network interface adapter via its host processor bus. *Id.* The ROPE chip is coupled to the host processor bus and to the network interface adapter. *Id.* The ROPE chip includes a protocol processing engine, a direct memory access ("DMA") controller, and a dual ported memory (coupled with the network interface adapter and coupled with the DMA controller). *Id.* The DMA controller is used by the ROPE chip to efficiently move data (packets/PDUs) to/from the host memory, thereby minimizing movement of data across the host bus interface. *See id.* Packets/PDUs being processed by the ROPE chip are stored in the dual ported memory of the chip. *See id.*

2. Tanenbaum

Tanenbaum describes general principles of data transmission in computer networks including TCP/IP and UDP/IP protocols. *See generally* Ex. 1006. Tanenbaum discloses, *inter alia*, a "fast path" processing solution for reducing overhead processing on a host system processor. *See* Ex. 1006, 583–586.

C. Obviousness of Claims 41–43 over Thia and Tanenbaum

1. Prior Proceedings

Petitioner argues in the Petition that Thia discloses the preambles of claims 41 and 43 and that Thia in combination with Tanenbaum teaches the remaining limitations of claims 41–43. Pet. 69–88. With respect specifically to the limitation "a flow re-assembler, disposed in the network interface" recited in claim 41, Petitioner argues:

> Thia in combination with Tanenbaum96 discloses this claim limitation. This limitation reflects standard TCP protocol

> operation. Tanenbaum96 discloses that the TCP protocol processes packets and re-assembles the data portions without the header in the correct order together into a buffer. *See* limitation [32.h].[10]
>
> While Tanenbaum96 suggests that the re-assembler is provided on a network interface (Ex.1006.498), Thia provides an express disclosure. Thia discloses copying the data portions of packets from the network interface to the host, and thus discloses a flow re-assembler on the network interface to re-assemble data portions of packets within a communication flow. *See* Ex.1015.005 ("The data portion of a PDU may be physically moved for the following reasons: • Copying between the adaptor buffer and the host system memory."). Like Tanenbaum96, Thia also discloses block data transfers to host memory, but Thia adds that the transfer is from the network interface. *See id.* at .007 ("The architectural considerations involved in the chip design can be summarized as follows: □ Movement of data across the host bus interface are minimized using an on-chip DMA for fast block data transfer to … the host system memory.").
>
> In sum, Thia in combination with Tanenbaum96 discloses "*a flow reassembler ... configured to re-assemble a data portion of said first packet with a data portion of a second packet in said communication flow*" (Tanenbaum's reassembly of data into a buffer for block copy transfers to host memory, Thia's reassembly of data into a buffer for block copy transfers to host memory), wherein the re-assembler is "*disposed in the network interface*" (Thia's network interface that places data in on-chip memory).

Pet. 77–78.

With respect specifically to the limitations now at issue on remand, Patent Owner argues in its Response that the Thia-Tanenbaum combination does not teach or suggest "a flow re-assembler, disposed in the network

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[10] *See* Pet. 57–58.

interface, configured to re-assemble a data portion of said first packet with a data portion of a second packet in [a] communication flow," as recited in claim 41, or a "network interface . . . comprising . . . a re-assembler for storing data portions of . . . multiple packets without headers in a first portion of . . . memory," as recited in claim 43. PO Resp. 42–50. First, according to Patent Owner, "Petitioners admit Tanenbaum does not disclose a flow re-assembler disposed in the network interface," and "[t]hus, it is undisputed that Tanenbuam does not teach or suggest the instant limitation." *Id.* at 43 (regarding claim 41; citing Pet. 77), 47 (regarding claim 43; citing Pet. 87). Second, Patent Owner contends, "Petitioners incorrectly allege that 'Thia provides an express disclosure' of such a re-assembler based on Thia's disclosure of copying data between the ROPE chip and the host." *Id.* at 43 (regarding claim 41; citing Pet. 77), 47 (regarding claim 43; citing Pet. 87).

While conceding that "Thia describes performing certain protocol processing functions on a ROPE chip separate from the host," such as "processing checksums, timer management, generating ACK packets, decoding headers, and the like," Patent Owner contends that "[o]nce relevant bypassable operations have been performed by the ROPE chip, the PDU is copied ***to the host*** for reassembly." PO Resp. 43–44 (citing Ex. 1015, 6, 7, 9, 13–14; Ex. 2026 ¶ 154), 47–48 (same). Indeed, according to Patent Owner, "Thia explicitly states that its bypass ***does not*** perform reassembly of PDUs." *Id.* at 43–44 (citing Ex. 1015, 14), 47 (same). Further, Patent Owner contends, Thia's "[direct memory access ("DMA")] procedure, which is responsible for transferring data between the host and [network interface adapter ("NIA")], copies the entire PDU—not just the data portion." *Id.* at 44 (citing Ex. 1015, 7, 9; Ex. 2026 ¶¶ 155–156), 48 (citing Ex. 1015, 7, 9;

Ex. 2026 ¶¶ 155–157). According to Patent Owner, "[i]f Thia intended to disclose copying just the data, and not the header, to the host, then it could have easily referred to the DMA procedure setting the starting address pointer to the Data Pointer (shown in Figure 4 of Thia), as opposed to the entire PDU," but "[i]ndeed, Thia explicitly stores both data ***and*** header portions of received TPUs." *Id.* at 44 (citing Ex. 2026 ¶¶ 155–156), 48–49 (citing Ex. 1015, 11; Ex. 2026 ¶¶ 155–157).

Still further, Patent Owner contends,

> Petitioners rely solely on Thia's disclosure that "[t]he data portion of a PDU may be physically moved for the following reasons: • Copying between the adaptor buffer and the host system memory" to argue the ROPE chip performs reassembly of the data portions of received PDUs in a communication flow. (Pet[.] 77.) However, the cited passage merely states that the data portion of a packet may be copied between the host and the NIA—which is true; the data portion of a PDU is copied between the host and NIA, just as the header portion is. The cited passage does not disclose or even suggest that the ROPE chip is performing reassembly of the data portions of the two packets. Rather, as mentioned previously, Thia expressly states that reassembly ***is not*** performed in the bypass path. (Ex.1015[,]14.)
>
> Accordingly, neither Thia nor Tanenbaum teaches this claim element and cannot render the claim obvious.

PO Resp. 44–45; *see also id.* at 49–50 (citing Pet. 87; Ex. 1015, 9, 14; Ex. 2026 ¶¶ 159–160).

In response to Patent Owner's contention that "it is undisputed that Tanenbaum does not teach or suggest the instant limitation," Petitioner points out in its Reply that "[t]he Petition expressly states that 'Tanenbaum[] discloses that the TCP protocol processes packets and re-assembles the data portions without the header in the correct order into a buffer'" and "further

identifies that 'Tanenbaum[] suggests that the re-assembler is provided on the network interface.'" Pet. Reply 17 (quoting Pet. 77). Further, Petitioner contends, Patent Owner "does not explain why Tanenbaum[] fails to disclose reassembly." *Id.*

Responding to Patent Owner's further assertion that "Thia explicitly states that its bypass ***does not*** perform reassembly of PDUs," Petitioner argues that the portion of Thia relied upon by Patent Owner is referring to a different type of reassembly. Pet. Reply 17–18 (citing PO Resp. 43–44). In particular, relying on the testimony of its expert, Bill Lin, Ph.D., Petitioner contends that a person of ordinary skill in the art would have understood Thia's statement that "[t]here is no segmentation/reassembly within the bypass path" "addresses lower-layer (*i.e.*, network and data-link layer) segmentation/reassembly that is implemented on the Network Interface Adaptor (NIA)" and "does not contradict [Thia's] disclosures, as described in the Petition, of a different re-assembler on the ROPE chip for higher protocol layers." *Id.* (quoting Ex. 1015, 14) (citing Pet. 77; Ex. 1015, 5, 7; Ex. 1223 ¶¶ 24–28 (Dr. Lin's Reply Declaration)).

Lastly, responding to Patent Owner's contention that Thia discloses host reassembly because it sends the starting address of the PDU, Petitioner argues that the portion of Thia relied upon by Patent Owner concerns transmission of packets from the host computer to the network, rather than receipt of packets. Pet. Reply 18 (citing PO Resp. 44; Ex. 1015, 9; Ex. 1223 ¶¶ 29–31). Thus, according to Petitioner, Patent Owner's conclusion that 'the PDU is copied **to the host** for reassembly' is contrary to Thia's explicit teachings." *Id.* (quoting PO Resp. 43).

In the Final Written Decision, following consideration of the record developed during trial, we concluded that Petitioner had demonstrated by a preponderance of the evidence that all challenged claims are unpatentable. With respect specifically to claims 41–43, we explained that Patent Owner had "fail[ed] to demonstrate that Petitioner, in fact 'admitted' that Tanenbaum fails to disclose the disputed claim limitation or how the re-assembly of data portions of packets of Tanenbaum (relied upon by Petitioner) differs from the reassembly of data portions of packets, as recited in claim 41," and we concluded that "[i]n both cases, data portions of packets are reassembled." Final Dec. 11.

In its decision on appeal, the Federal Circuit held that "[t]he Board's analysis of the disclosure of the reassembly limitations in claims 41–43 falls short of that which the [Administrative Procedure Act] and our precedent require." *Alacritech*, 966 F.3d at 1371. The Court pointed out in particular that "[t]he claim limitations at issue require that reassembly take place in the network interface, as opposed to a central processor," and "the crux of the [parties'] dispute was *where* reassembly takes place in the prior art and whether that location satisfies the claims limitations," not merely *whether* reassembly is disclosed by the asserted prior art. The Court further explained that "[t]he Board's analysis does not acknowledge that aspect of the parties' dispute, much less explain how the prior art teaches or suggests reassembly in the network interface," and "[a]s such, we cannot reasonably discern whether the Board followed a proper path in determining that the asserted prior art teaches or suggests the reassembly limitations, and by extension, that the subject matter of claims 41–43 would have been obvious." *Id.* Further, the Court explained, "the parties' briefing focuses on the disclosure

of the reassembly limitations by one reference (Thia), but the Board appears to have relied on a different reference (Tanenbaum) to support its finding." *Id.* at 1372. "Because the Board's reasoning appears to be untethered to either party's position," the Court explained, "we cannot infer from the Board's rejection of one of [Patent Owner's] arguments regarding Tanenbaum that the Board necessarily adopted [Petitioner's] position regarding Thia." *Id.*

Explaining that the precedent is clear that "under the APA, '[the Court's] review of a patentability determination is confined to the grounds upon which the Board actually relied,'" and that "the Board is obligated to 'articulate a satisfactory explanation for its action including a rational connection between the facts found and the choice made,'" the Court vacated the Board's obviousness determination as to claims 41–43 and remanded for reconsideration whether the asserted prior art teaches or suggests the entirety of the reassembly limitations, including the requirement that reassembly takes place in the network interface. *Id.* at 1372–73 (quoting *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019); *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016)).

2. Post-remand Briefing

a. Petitioner's Arguments

Petitioner argues in its post-remand brief that "[b]ecause reassembly is the responsibility of the transport layer," the combination of "Tanenbaum96's teachings of fast-path TCP/IP processing and offloading transport layer processing to a [NIC] with Thia's NIC that offloads fast-path transport layer processing" "teaches reassembly by a NIC that performs transport layer processing." Pet. Remand Br. 1. According to Petitioner, "[t]he Petition explains that Tanenbaum96 teaches that the TCP transport

layer reassembles data from received packets into the original byte stream and that the transport layer processing can be done on the NIC; and therefore, that Tanenbaum96 teaches reassembly by a NIC during transport layer processing." *Id.* (citing Pet. 29, 57–58, 77; Reply 17–18; Ex. 1006, 498, 540–41). Petitioner contends that "[t]he Federal Circuit's footnote 5 does not indicate otherwise," as "[i]t does not address Tanenbaum96's teaching that the transport layer performs reassembly (explained at limitation 32.h, cross-referenced at 41.d) or that Tanenbaum96 teaches that the transport entity can be on the NIC," both of which Petitioner contends "are explained in the Petition" and "clearly teach a reassembler on the NIC." *Id.* at 1–2 (citing Pet. 29, 57, 77; Ex. 1006, 498).

Further, Petitioner contends, "[t]he Petition also explains that Thia teaches a NIC with a bypass stack that performs transport layer processing for packets with predicted headers" and that "Thia teaches the NIC reassembling packet data portions within a communication flow into host memory." Pet. Remand Br. 2 (citing Pet. 25–27, 77, 87; Ex. 1015, 3, 5, 7). According to Petitioner, "[Patent Owner] did not argue, nor do the claims require, that the NIC must reassemble data into a memory on the NIC (as opposed to the host)," and "[Patent Owner's] arguments in opposition regarding segmentation/reassembly in Thia's bypass path point 'to different type of reassembly in Thia' as rebutted in Pet. Reply at 17–18 (citing Ex. 1223 ¶¶ 24–31)." *Id.* Petitioner further contends that "[t]he Petition further explains that Tanenbaum96's 'fast path' TCP/IP processing for packets on established connections works similarly to Thia's bypass stack" and that the combination of Thia and Tanenbaum "thus teaches a NIC that performs *all* transport layer processing for connections in the

ESTABLISHED (data transfer) state, including the reassembly limitations of claims 41–43." *Id.* at 2–3 (citing Pet. 25–27, 57–58, 77–78, 87).

Finally, Petitioner contends

> Other now-final Board findings also compel this conclusion, including a finding that the Combination teaches reassembling the data portions of a first and a second packet of substitute claim 79 (Paper 77 at 25–26) and a finding that the Combination teaches a network interface device that transfers the data portions of packets to host memory without their header portions of claims 1 and 55. IPR2017-1409 (880 Patent), Paper 79 at 10-11. The Petition relies on the same disclosures for claims 41–43. *See* Paper 38 at 12–15, 17–18; *see also* IPR2017-1409, Paper 1 at 86–87. These rulings went unchallenged on appeal.
>
> The sufficiency of this evidence is also confirmed by other now-final Board decisions. *See Alacritech Inc. v. Intel. Corp.,* Case No. 19-1443 (205 Patent), slip op. at 6 (July 16, 2020) (affirming that "Thia expressly discloses bypassing the entire transport layer using a bypass stack" including reassembly); *Alacritech Inc. v. Intel. Corp.,* Case No. 19-1444 (072, 241 and 036 Patents), slip op. at 6 n.4 (July 16, 2020) (affirming that "Tanenbaum *expressly discloses* that transport layer protocol processing may be offloaded to a network interface card."). These final rulings bind both Alacritech and the Board. *Papst v. Samsung,* 924 F.3d 1243, 1250–53 (Fed. Cir. 2019). They demonstrate that the Combination teaches the reassembly limitations.

Pet. Remand Br. 3.

b. Patent Owner's Arguments

In its post-remand brief, Patent Owner contends that "[i]n view of the [Federal Circuit's] clear admonition . . . and the dearth of analysis or evidence in the Petition[] regarding these limitations, the Board should uphold the patentability of claims 41–43." PO Remand Br. 1.

First, with respect to Tanenbaum, Patent Owner argues that Petitioner's allegation is "limited to a sentence fragment: 'While Tanenbaum96 suggests that the re-assembler is provided on a network interface (Ex. 1006.498).'" *Id.* (quoting Pet. 77). Pointing to Petitioner's argument that "[l]ike Tanenbaum96, Thia also discloses block data transfers to host memory, but Thia adds that the transfer is from the network interface," Patent Owner further contends that, "[p]lainly, if Thia supposedly ***adds*** that the reassembler is in the network interface, then Tanenbaum96 does not disclose it." *Id.* at 1–2 (quoting Pet. 77). In any event, Patent Owner argues, although Tanenbaum enumerates transport layer functions performed by a "transport entity" that may be located on the network interface card, Tanenbaum does not list reassembly as one of those functions. *Id.* at 2 (citing Ex. 1006, 498, 506–528).

As to Thia, Patent Owner argues that the Petition's citations to disclosure in Thia of "[c]opying between the adaptor buffer and the host system memory" and use of "on-chip DMA for fast block data transfer to . . . the host system memory" do not disclose reassembly. PO Remand Br. 2 (citing Pet. 77; Ex. 1015, 5, 7). Patent Owner contends, "Thia explicitly discloses offloading only some but not all transport layer functions, and nowhere lists reassembly or header removal as one of those functions." *Id.* As in the Patent Owner Response, Patent Owner points to Thia's statement that "[t]here is no segmentation/reassembly within the bypass path" and contends, "[t]here could be no clearer expression of a lack of support for reassembly on the ROPE chip." *Id.* at 2–3 (quoting Ex. 1015, 14). Patent Owner further argues that Petitioner's Reply misconstrues Thia by alleging that Thia's disclosure relates only to transmitting, nor receiving, packets,

whereas Thia expressly states that "[o]n ***receiving*** the first bypassable PDU, the BYPASS_START procedure is called . . . ." *Id.* at 3 (quoting Ex. 1015, 9 (emphasis Patent Owner's)) (citing Reply 18). Finally, according to Patent Owner, as previously explained in the Patent Owner Response, "Thia's ROPE chip performs some but not all transport layer processing, the host processor performing the remainder"; and "[a]lthough 'resequencing' is mentioned in Thia, this disclosure was not cited in the Petition," and resequencing is not the same as reassembly. *Id.* (citing PO Resp. 43–45).

3. Discussion

Having considered the parties' arguments and evidence anew in light of the Federal Circuit's decision on appeal, we agree with Patent Owner that Petitioner has not established that the combination of Thia and Tanenbaum teaches or suggests "a flow re-assembler, disposed in the network interface," as recited in claim 41, or a "network interface comprising . . . . a re-assembler," as recited in claim 43. Accordingly, we conclude that Petitioner has not shown by a preponderance of the evidence that claims 41–43 are unpatentable.

Contrary to Petitioner's assertion in the Petition, we find no "express disclosure" in Thia of a "re-assembler . . . provided on a network interface." *See* Pet. 77. As Patent Owner points out, Thia explicitly identifies certain transport layer procedures for implementation in the bypass chip—namely, checksum, timer management, generation of acknowledgment packets, and resequencing procedures—but does not identify re-assembly among them. Ex. 1015, 6; *see* PO Resp. 43–45; PO Remand Br. 2. Although we find no indication that the identified procedures constitute an exhaustive list of bypassable procedures, we find that Thia's statement that "[t]here is no

segmentation/reassembly within the bypass path," cited by Patent Owner (*see* PO Resp. 43–44 (quoting Ex. 1015, 14); PO Remand Br. 2–3 (same)), strongly counsels against a finding that Thia suggests, let alone "express[ly] disclos[es]," re-assembly on a network interface. We have considered Petitioner's argument, supported by the testimony of Dr. Lin, that the quoted statement refers to network and data-link layer segmentation/reassembly, rather than reassembly in the transport layer (Pet. Reply 17–18 (citing Ex. 1223 ¶¶ 24–28)). However, as Dr. Lin acknowledges, the remainder of the quoted paragraph of Thia further states that the lack of segmentation/ reassembly within the bypass path is "not see[n] . . . as a major restriction, as research suggests that fragmentation of PDUs should be restricted only to the lower layers and should occur only once in the protocol stack" and that "[t]he Segmentation and Reassembly sublayer of the ATM adaptation layer is a good place for such functions." Ex. 1015, 14 (cited by Ex. 1223 ¶ 28).[11] In other words, to the extent that Thia's statement that "[t]here is no segmentation/reassembly within the bypass path" is properly understood to refer to lower-level segmentation/reassembly, it is also reasonably understood in that case that there would not additionally be segmentation/ reassembly in the transport layer.

Further, although Tanenbaum discloses that transport entities, in general, can reside in various locations, including "the operating system kernel, in a separate user process, in a library package bound into network

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[11] *See also* Tr. 99:18–100:7 (Petitioner's counsel arguing that "the ATM layer . . . is the lower level that includes network-styled processing in the OSI system" and that Thia "deals with situations where lower-level packets get broken up somewhere along the network path between the sender and the receiver and reassembling those network layer packets").

applications, or on the network interface card," or "even . . . on special interface machines at the edge of the subnet to which hosts connect" (Ex. 1006, 498), in the Petition, Petitioner does not cite any persuasive evidence that shows that a person of ordinary skill in the art would understand Tanenbaum to suggest specifically that a re-assembler is provided on a network interface (*cf.* Pet. 77). In this regard, Tanenbaum's statement that a TCP entity in an unspecified location can "reconstruct" a byte stream from received IP datagrams does not lead us to the conclusion that the combination of Thia and Tanenbaum suggests a re-assembler on the network interface, particularly in view of Thia's disclosures addressed above. Ex. 1015, 14; *cf.* Pet. 57–58 (citing Ex. 1006, 540–41), 77; Pet. Remand Br. 1–3. Notwithstanding any other similarities that may exist between Tanenbaum's "fast path" TCP/IP processing and Thia's bypass stack (*see* Pet. Remand Br. 2–3), Thia's statement that "[t]here is no segmentation/reassembly within the bypass path," when read in light of Dr. Lin's testimony and Thia's further disclosure that "fragmentation of PDUs should be restricted only to the lower layers and should occur only once in the protocol stack," suggests that any reassembly in Thia occurs only in a lower layer (e.g., the network layer), not in the transport layer. Ex. 1015, 14; 1223 ¶¶ 24–28.

Moreover, although Thia discloses "copying" data between an adaptor buffer and host system memory (Ex. 1015, 5), we are not persuaded by Petitioner's argument that Thia teaches a network adaptor "reassembling packet data portions within a communication flow into host memory" (Pet. Remand Br. 2). Irrespective of whether the claims do or do not "require[] that the NIC must reassemble data into a memory of the NIC (as opposed to

the host)" (*see id.*), Thia's statement that "[t]here is no segmentation/ reassembly within the bypass path" is not specific to reassembly of data into a memory on the NIC, and, in any event, we are not persuaded that "copying" suggests reassembly.

Finally, we are not persuaded that other decisions cited by Petitioner compel a different conclusion. Contrary to Petitioner's argument, we do not find that the Federal Circuit "affirm[ed] that 'Thia expressly discloses bypassing . . .' . . . reassembly" in Appeal No. 19-1443. Pet. Remand Br. 3. Rather, although the Court stated that "Thia expressly discloses bypassing the entire transport layer using a bypass stack," the Court went on to clarify that "*[a]side from Thia's disclosure that 'there is no segmentation/ reassembly within the bypass path,'* Alacritech has not identified any transport layer functionality that would not be offloaded from the host computer in any of Thia's embodiments." *Alacritech Inc. v. Intel Corp.*, No. 19-1443, slip op at 6 (Fed. Cir. July 16, 2020) (emphasis added).

Petitioner's citation of Appeal No. 19-1444 is similarly unavailing. Pet. Remand 3. The *inter partes* review proceedings at issue in that appeal did not involve Thia, and although, as noted by the Court, the Board found in IPR2017-01392 that "Tanenbaum expressly discloses that transport layer protocol processing may be offloaded to a network interface card," neither the Board nor the Court addressed whether the combination of Thia and Tanenbaum teaches or suggests a reassembler on the network interface. *Alacritech Inc. v. Intel Corp.*, No. 19-1444, slip op at 6 n.4 (Fed. Cir. July 16, 2020) (quoting IPR2017-01392, Paper 81 at 21–22 (PTAB Nov. 26, 2018)); *see generally* IPR2017-01391, Paper 81 (PTAB Nov. 26, 2018);

IPR2017-01392, Paper 81 (PTAB Nov. 26, 2018); IPR2017-01406, Paper 83 (Nov. 26, 2018).

Lastly, although IPR2017-01409 cited by Petitioner also involved the combination of Thia and Tanenbaum directed to the '880 patent, claims 1, 5–10, 12, 14, 16, 17, 20–23, 27, 28, 45, and 55 at issue in that case do not recite a "re-assembler," and the Board accordingly made no finding that the Thia-Tanenbaum combination teaches or suggests a re-assembler as recited in claims 41 and 43 at issue in the present case. *See* IPR2017-01409, Paper 79 at 10–11 (PTAB Nov. 14, 2018) (cited at Pet. Remand Br. 3).

III. CONCLUSION

After reviewing the record developed during trial anew and taking into account the Federal Circuit's decision, we are not persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 41–43 of the '880 patent are unpatentable over Thia and Tanenbaum.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 41–43 of the '880 patent have not been proven by a preponderance of the evidence to be unpatentable;

FURTHER ORDERED that we do not reach Patent Owner's Contingent Motion to Amend with respect to substitute claims 85–87; and

FURTHER ORDERED that, because this Decision on Remand amounts to a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Outcome of Decision on Remand:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
41–43	103(a)	Thia, Tanenbaum		41–43

Final Outcome of Final Written Decision After Remand:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
32, 34, 35, 39, 41–43	103(a)	Thia, Tanenbaum	32, 34, 35, 39	41–43
37, 38	103(a)	Thia, Tanenbaum, Nahum	37, 38	
Overall Outcome			32, 34, 35, 37–39	41–43

Motion to Amend Outcome	Claim(s)
Original Claims Cancelled by Amendment	
Substitute Claims Proposed in the Amendment	79–87
Substitute Claims: Motion to Amend Granted	
Substitute Claims: Motion to Amend Denied	79–84
Substitute Claims: Not Reached	85–87

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