UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.,
Petitioner,

v.

Qualcomm Incorporated,
Patent Owner

Case IPR2018-01315
U.S. Patent No. 8,063,674

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 37 C.F.R § 90.2(a), Patent Owner Qualcomm Incorporated ("Qualcomm" or "Patent Owner") hereby appeals to the United States Court of Appeals for the Federal Circuit the Patent Trial and Appeal Board's Final Written Decision on Remand in IPR2018-01315, entered on November 10, 2022 (Paper No. 40) and from all underlying orders, decisions, rulings and opinions that are adverse to Qualcomm.

In accordance with 37 C.F.R § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, the determination of unpatentability of claims 1, 2, and 5–7 of U.S. Patent No. 8,063,674 under 35 U.S.C. § 103(a); the determination that alleged Applicant Admitted Prior Art (AAPA) is not the basis of Petitioner's challenge, and is therefore eligible for use in the *inter partes* review proceeding; the determination that the answer to this issue is resolved by the June 9, 2022 Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311; any finding or determination supporting or related to those issues; as well as all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions.

Simultaneous with this submission, a copy of this Notice of Appeal is being filed with the United States Patent and Trademark Office by way of hand delivery to the Office of General Counsel to:

Office of the General Counsel
United States Patent and Trademark Office
Madison Building East, Room 10B20
600 Dulany Street
Alexandria, Virginia 22314

In addition, this Notice of Appeal, along with a copy of the Final Written Decision, is being filed electronically with the United States Court of Appeals for the Federal Circuit along with the required docketing fees.

Respectfully submitted,

Date: November 17, 2022

/ David B. Cochran /
David B. Cochran, Reg. No. 39,142
JONES DAY
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Counsel for Patent Owner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that on November 17, 2022, a complete and entire copy of this **PATENT OWNER'S NOTICE OF APPEAL** has been served in its entirety by e-mail on the following counsel of record for petitioner:

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Paper 40
Date: November 10, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01315, IPR2018-01316
Patent 8,063,674 B2[1]

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* SCOTT B. HOWARD.

Opinion Concurring filed by *Administrative Patent Judge* DANIEL J. GALLIGAN.

HOWARD, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision on Remand
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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[1] The parties may not use this style heading in any subsequent papers without prior authorization.

I. INTRODUCTION

In these *inter partes* reviews, instituted pursuant to 35 U.S.C. § 314, Apple Inc. ("Petitioner" or "Apple") challenges claims 1, 2, 5–9, 12, 13, and 16–22 ("the challenged claims") of U.S. Patent No. 8,063,674 B2 (Ex. 1001, "the '674 patent"), owned by Qualcomm Incorporated ("Patent Owner").

The references applied against the challenged claims are identical in each of the cases. A joint hearing was held for these cases. The parties rely on the same declarants submitting identical declarations in each case for testimonial evidence. The briefing on remand is substantially the same. Under these circumstances, we determine that a combined Final Decision will promote a just, speedy, and inexpensive resolution of these proceedings.

A. IPR2018-01315 Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 1, 2, and 5–7 of the '674 patent pursuant to 35 U.S.C. §§ 311–319. Paper 2[2] ("Petition" or "Pet."). Patent Owner filed a Preliminary Response. Paper 6. We instituted an *inter partes* review of claims 1, 2, and 5–7 on all grounds of unpatentability alleged in the Petition. Paper 7 ("Institution Decision" or "Inst. Dec.").

After institution of trial, Patent Owner filed a Response (Paper 12, "PO Resp."), Petitioner filed a Reply (Paper 16, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 19, "PO Sur-reply").

A joint hearing for IPR2018-01315 and IPR2018-01316 was held on October 11, 2019. Paper 25 ("Tr.").

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[2] Unless otherwise noted, all citations are to IPR2018-01315. We note that identical exhibits and substantially identical papers were filed in each of the proceedings.

B. IPR2018-01316 Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 8, 9, 12, 13, and 16–22 of the '674 patent pursuant to 35 U.S.C. §§ 311–319. IPR2018-01316, Paper 2 ("1316 Pet."). Patent Owner filed a Preliminary Response. IPR2018-01316, Paper 6. We instituted an *inter partes* review of claims 8, 9, 12, 13, and 16–22 on all grounds of unpatentability alleged in the Petition. IPR2018-01318, Paper 7 ("1316 Inst. Dec.").

After institution of trial, Patent Owner filed a Response (IPR2018-01316, Paper 12, "1316 PO Resp."), Petitioner filed a Reply (IPR2018-01316, Paper 16, "1316 Pet. Reply"), and Patent Owner filed a Sur-reply (IPR2018-01316, Paper 19, "1316 PO Sur-reply").

C. The Final Written Decision, the Federal Circuit Appeal, and the Remand Proceeding

We issued a consolidated Final Written Decision which held all of the challenged claims unpatentable. Paper 26 ("Final Decision," "Final Dec."). In particular, we concluded that, based on the language of 35 U.S.C. § 311(b) and our rules, applicant admitted prior art could form the basis of an *inter partes* review petition. Final Dec. 18–22. Based on the combination of AAPA[3] and Majcherczak, we determined that Petitioner had proven by a preponderance of the evidence that the challenged claims were unpatentable as obvious. *Id.* at 22–54. Additionally, we held that Petitioner failed to prove the challenged claims were unpatentable as obvious in view of Steinacker, Doyle, and Park. *Id.* at 59–81.

[3] AAPA refers to the specific applicant admissions identified by Petitioner in the '674 Patent. *See* footnote 9, *infra*.

Patent Owner filed a Notice of Appeal of the Final Written Decision with the United States Court of Appeals for the Federal Circuit. Paper 27. In that Notice of Appeal, Patent Owner indicated that the issues on appeal may include, *inter alia*, the "determination that alleged Applicant Admitted Prior Art (AAPA) is eligible for use in *inter partes* review proceedings." *Id.* at 1.

On February 1, 2022, the Federal Circuit issued a decision in the appeal vacating our Final Decision and remanding for further proceedings. *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367 (Fed. Cir. 2022). Specifically, the Federal Circuit held that we "incorrectly interpreted § 311(b)'s 'prior art consisting of patents or printed publications' to encompass [applicant admitted prior art] contained in the challenged patent." *Id.* at 1376–77. However, because "the use of [applicant admitted prior art] can be permissible in an *inter partes* review," the Federal Circuit remanded with instructions "to determine whether Majcherczak forms the basis of Apple's challenge, or whether the validity challenge impermissibly violated the statutory limit in Section 311." *Id.* at 1377.

With regard to the ground involving Steinacker, Doyle, and Park, the Federal Circuit held that "there was no error in the Board's finding that Apple made an insufficient showing of a motivation to combine Doyle with Steinacker—a prerequisite to its proposed three-way combination of Doyle with Steinacker and with Park." 24 F.4th at 1377.

Following the remand from the Federal Circuit, we held a conference call with the parties. *See* Paper 28, 2 (Order on Conduct of Proceedings on Remand). During the conference, we authorized the parties to submit two rounds of simultaneous briefing. *See id.* Petitioner and Patent Owner,

respectively, submitted Opening Briefs on Remand. Paper 31 ("Pet. Remand Br."); Paper 32 ("PO Remand Br."). The parties also each submitted a Responsive Brief on Remand. Paper 37 ("Pet. Resp. Remand Br."); Paper 39 ("PO Resp. Remand Br.").

Patent Owner requested an oral hearing on remand, which we took under advisement. *See* Paper 28 at 2–3. Given the nature of the issue on remand, no additional oral argument was held. *See* Patent Trial and Appeal Board, Standard Operating Procedure 9[4] at 7 ("In most cases, an additional oral hearing will not be authorized. Normally, the existing record and previous oral argument will be sufficient."), 8 (indicating no additional oral argument when there was an "Erroneous Application of Law").

The Board has jurisdiction under 35 U.S.C. § 6(b). This Final Written Decision on Remand issues pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.

D. Real Party in Interest

Petitioner identified Apple Inc. as the real party in interest. Pet. 64.

Patent Owner identified Qualcomm Incorporated as the real party in interest. Paper 3, 2 (Patent Owner's Mandatory Notices).

E. Related Proceedings

The parties identified the following patent litigation proceedings in which the '674 patent was asserted: *In re Certain Mobile Electronic*

[4] Available at https://www.uspto.gov/sites/default/files/documents/sop_9_%20procedure_for_decisions_remanded_from_the_federal_circuit.pdf.

Devices and Radio Frequency and Processing Components Thereof (ITC Inv. No. 337-TA-1093) and *Qualcomm Inc. v. Apple Inc.*, Case No. 3:17-cv-02398 (S.D. Cal.). Pet. 64–65; Paper 3, 2.[5]

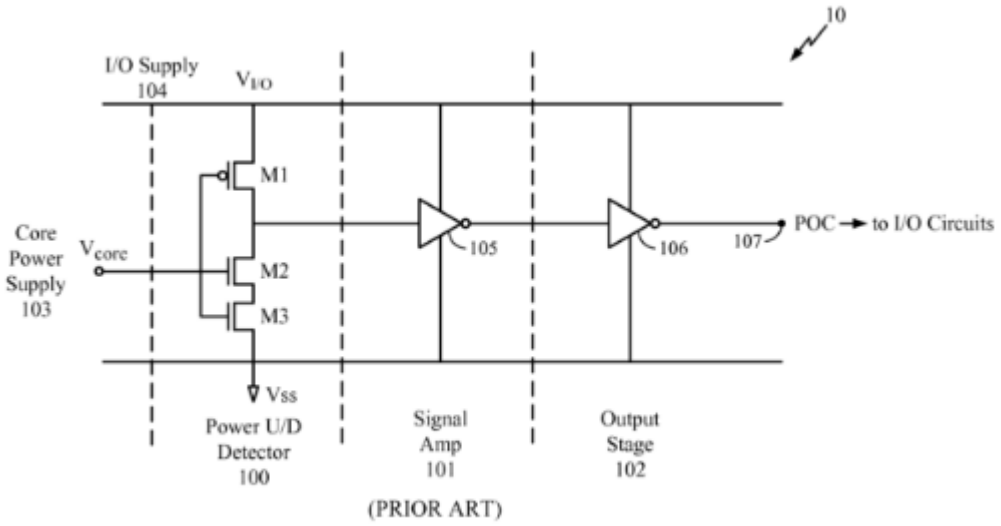
F. The '674 Patent

The '674 patent is titled "Multiple Supply-Voltage Power-Up/Down Detectors." Ex. 1001, code (54). According to the '674 patent, "many newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices." *Id.* at 1:22–25.

The '674 patent further states that "[i]n order to facilitate communication between the core and I/O devices, level shifters are employed." *Id.* at 1:28–29. "Because the I/O devices are connected to the core devices through level shifters, problems may occur when the core devices are powered-down." *Id.* at 1:29–32. An example of such a problem described in the '674 patent is how stray currents while the core is powering down can cause the level shifters to "send a signal to the I/O devices for transmission" resulting in the I/O devices "transmit[ting] the erroneous signal into the external environment." *Id.* at 1:34–40.

One prior art solution identified in the '674 patent is the use of "power-up/down detectors to generate a power-on/off-control (POC) signal internally [which] instructs the I/O devices when the core devices are shut down." Ex. 1001, 1:55–58. Figure 1 of the '674 patent is reproduced below.

[5] According to Petitioner, the district court proceeding and the ITC investigation have been dismissed. Paper 15, 1 (Petitioner's Updated Mandatory Notices).



(PRIOR ART)
FIG. 1

Figure 1 "is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices" which is identified as being prior art. *Id*. at 4:18–19, Fig. 1.

The '674 patent identifies a number of issues associated with the Figure 1 design. For example, when I/O power supply 104 is on and core power supply 103 is off, powering on the core power supply results in "a period in which all three transistors within power up/down detector 100 are on," resulting in a virtual short "to ground causing a significant amount of current to flow from I/O power supply 104 to ground." Ex. 1001, 2:21–29. "This 'glitch' current consumes unnecessary power." *Id*. at 2:29–30. Although the glitch current can be reduced by reducing the size of transistors M1-M3, such a reduction limits "the actual amount of current that can pass through the transistors" and reduces their switching speeds, which "translates into less sensitivity in detecting power-up/down of core supply voltage 103 or longer processing time for power-up/down events." *Id*. at 2:31–39; *see also id*. at 2:63–3:11.

According to the '674 patent, these problems can be solved by using "one or more feedback circuits coupled to the up/down detector" that "are configured to provide feedback signals to adjust a current capacity of said up/down detector." Ex. 1001, 3:31–34. An example of such a feedback circuit is shown in Figure 4, reproduced below:

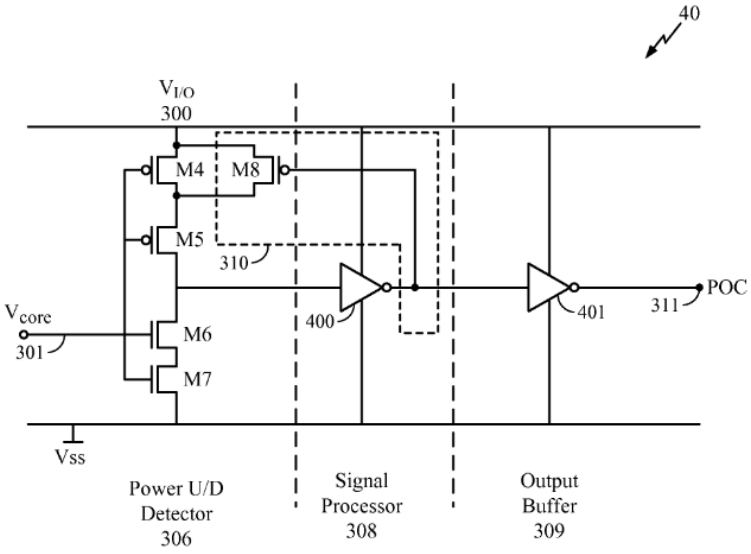


Figure 4 "is a circuit diagram illustrating another POC network configured according to the teachings of the present disclosure." *Id*. at 4:28–30. The '674 patent describes the operation of the feedback circuit in Figure 4 as follows:

> The feedback network 310 comprises a transistor M8 connected in parallel to the transistor M4. The transistor M8 is also configured as a p-type transistor, such that when the feedback signal from the inverting amplifier 400 is high, the transistor M8 is switched off, and when the feedback signal is low, the transistor M8 is switched on. Thus, when the V_{core} 301 is off, producing a high detection signal, the inverting amplifier 400 inverts that signal to a logic low which causes the transistor M8 to switch on. As the V_{core} 301 is powered-on, the detection signal changes to a logic low, which changes the feedback signal from the inverting amplifier 400 to a logic high, which, in turn, turns the transistor M8 off. While the transistor M8 is

> off, the power up/down detector 306 has a decreased current capacity, i.e., smaller current will flow through the transistor M8 because of the amplified low signal. The voltage level caused by the V_{core} 301 on the gate terminals of M4 and M5 could in some glitch or stray signal situations, cause leakage through M4 and M5. Because the feedback signal for the transistor M8 is received from the inverting amplifier 400, when the V_{core} 301 powers-down, the feedback signal will switch quickly from a logic high to a logic low, which will then switch the transistor M8 on. Thus, in the circuit configuration depicted in FIG. 4, the power up/down detector 40 will detect the V_{core} 301 powering down more quickly than the existing POC networks.

Id. at 6:4–28.

G. Illustrative Claim

Petitioner challenges claims 1, 2, and 5–9, 12, 13, and 16–22 of the '674 patent. Pet. 1; 1316 Pet. 1. Claim 1 is independent, is illustrative of the subject matter of the challenged claims, and reads as follows:

> 1. A multiple supply voltage device comprising:
>
> a core network operative at a first supply voltage; and
>
> a control network coupled to said core network wherein said control network is configured to transmit a control signal, said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state;
>
> one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/down detector;
>
> at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to

> switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on;
>
> at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down;
>
> at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor.

Ex. 1001, 8:44–9:3 (the '674 patent).

H. Prior Art and Asserted Grounds

Petitioner asserts that claims 1, 2, and 5–9, 12, 13, and 16–22 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1, 2, 5–9, 12, 13, 16–22	103(a)[6]	Steinacker,[7] Doyle,[8] and Park[9]
1, 2, 5, 6, 8, 9, 12, 13, 17–21	103(a)	AAPA,[10] Majcherczak[11]

[6] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 102, 103 that became effective on March 16, 2013. Because the '674 patent issued from an application filed before March 16, 2013, we apply the pre-AIA versions of the statutory bases for unpatentability.

[7] Steinacker, US 7,279,943 B2, issued Oct. 9, 2007 (Ex. 1005).

[8] Doyle, US 4,717,836, issued Jan. 5, 1988 (Ex. 1006).

[9] Park, J. C. & Mooney, V. J. (Nov. 2006). Sleepy Stack Leakage Reduction. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 14*(11), 1250–1263 (Ex. 1007).

[10] Petitioner identifies Figure 1 and the text at column 1, line 22 through column 2, line 39 of the '674 patent as Applicant Admitted Prior Art. *See* Pet. 37, 43, 46.

[11] U.S. Pub. No. US 2002/0163364 A1, published Nov. 7, 2002 (Ex. 1008).

Claims Challenged	35 U.S.C. §	References/Basis
7, 16, 22	103(a)	AAPA, Majcherczak, Matthews[12]

Additionally, Petitioner relies on the testimony of Robert W. Horst, Ph. D. (Ex. 1003; Ex. 1018) and Jacob Robert Munford (Ex. 1016). Patent Owner filed Dr. Horst's cross-examination as Exhibits 2003 and 2006. Patent Owner relies on the testimony of Dr. Massoud Pedram (Ex. 2002). Petitioner filed Dr. Pedram's cross-examination as Exhibit 1017.

II. ANALYSIS

A. Legal Principles

In *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under 35 U.S.C. § 103 that requires consideration of four factors: (1) the "level of ordinary skill in the pertinent art," (2) the "scope and content of the prior art," (3) the "differences between the prior art and the claims at issue," and (4) "secondary considerations" of non-obviousness such as "commercial success, long-felt but unsolved needs, failure of others, etc." *Id.* at 17–18.[13] "While the sequence of these questions might be reordered in any particular case," *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the U.S. Court of Appeals for the Federal Circuit has repeatedly emphasized that "it is error to reach a conclusion of obviousness until all those factors are considered," *WBIP, LLC v. Kohler*, 829 F.3d 1317, 1328 (Fed. Cir. 2016).

[12] U.S. Patent No. 6,646,844 B1, issued Nov. 11, 2003 (Ex. 1009).

[13] Neither party presented objective evidence of non-obviousness. *See* Pet.; PO Resp. Accordingly, we do not consider that factor in the following analysis.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is "a prism or lens" through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Factors pertinent to a determination of the "level of ordinary skill in the art include (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of workers active in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.,* 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, "[t]hese factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art." *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

Dr. Horst testifies that a person having ordinary skill in the art would have had "at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in circuit and system design." Ex. 1003 ¶ 33. Additionally, Dr. Horst testifies that "a person of ordinary skill with less than the amount of experience noted above could have had a correspondingly greater amount of educational training such a graduate degree in a related field." *Id*.

In our Institution Decisions, "we adopt[ed] Dr. Horst's definition of the level of ordinary skill in the art, with the exception of the language 'at least.'" Inst. Dec. 13; 1316 Inst. Dec. 13. Patent Owner agrees with our

formulation, *see* PO Resp. 9; 1316 PO Resp. 9, and Petitioner did not address it in its Reply. *See generally* Pet. Reply; 1316 Pet. Reply.

Accordingly, we find on the record as a whole that a person of ordinary skill in the art would have an undergraduate degree in electrical engineering, or a related field, and three years of experience in circuit and system design. Additionally, a person of ordinary skill with less than the amount of experience noted above could have had a correspondingly greater amount of educational training such a graduate degree in a related field.

C. Claim Construction

In this *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2017).[14] "Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016). In addition, the Board may not "construe claims during [an *inter partes* review] so broadly that its constructions are unreasonable under general claim construction principles." *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (emphasis omitted), *overruled on other grounds by Aqua Products, Inc. v. Matal*, 872

[14] We apply the district court claim construction standard to petitions filed on or after November 13, 2018. *See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51340 (Oct. 11, 2018) (to be codified at 37 C.F.R. pt. 42). Because Petitioner filed its petitions before November 13, 2018 (*see* Pet.; 1316 Pet.), we apply the broadest reasonable interpretation (BRI) standard.

F.3d 1290 (Fed. Cir. 2017) (en banc). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Use of the word *means* in a claim gives rise to a rebuttable presumption that 35 U.S.C. § 112, sixth paragraph, analysis applies to interpret the claim. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015). Construing a means-plus-function claim term is a two-step process, wherein we first identify the claimed function and then determine what structure, if any, disclosed in the specification corresponds to the claimed function. *Id.* at 1348–51. Our rules specifically require that a petition for *inter partes* review identify how each challenged claim is to be construed, including identification of the corresponding structure for means-plus-function limitations. *See* 37 C.F.R. § 42.104(b)(3) ("Where the claim to be construed contains a means-plus-function . . . limitation as permitted under 35 U.S.C. 112[(6)], the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function."). [15] "[S]tructure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Med. Instrumentation & Diagnostics Corp. v. Elekta*

[15] 37 C.F.R. § 42.104(b)(3) refers to § 112(f). Section 4(c) of the AIA redesignated 35 U.S.C. § 112, sixth paragraph as 35 U.S.C. § 112(f). Because the '674 patent has a filing date before the effective date of this provision of the AIA, we use the citation § 112, sixth paragraph.

AB, 344 F.3d 1205, 1210 (Fed. Cir. 2003) (quoting *B. Braun Med. Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997)).

Petitioner proposes a claim construction for "processing circuitry." Pet. 10; 1316 Pet. 5. Petitioner also contends that the claims contain several means-plus-function limitations. 1316 Pet. 6–9.

Patent Owner does not believe the term "processing circuitry" or the means-plus-function limitations need to be construed. PO Resp. 8; 1316 PO Resp. 8–9.

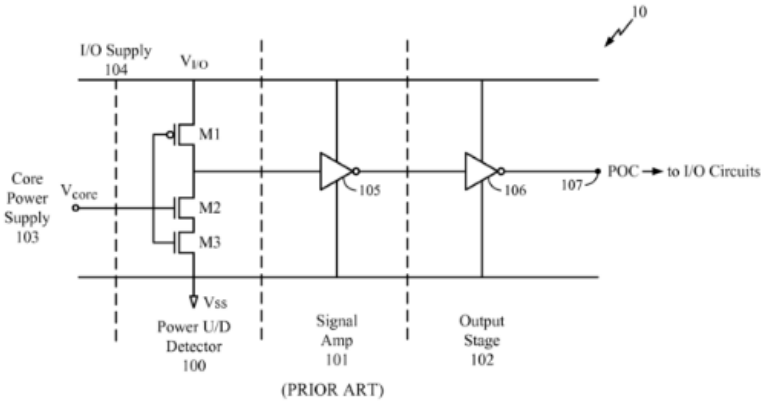
Having considered the evidence presented, we conclude that, with the exception of the means-plus-function limitations, no express claim construction of any term is necessary. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating that "we need only construe those claim limitations 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

With regard to the means-plus-function limitations, we are persuaded by Petitioner's identification of both the function set forth in the claim and the structure in the written description that is linked to the function, and adopt them as our own. *See* 1316 Pet. 6–9.

D. Obviousness over AAPA in View of Majcherczak

1. Overview of AAPA

The '674 patent describes a prior art "power-up/down detector[] to generate a power-on/off-control (POC) signal internally." Ex. 1001, 1:55–57, Fig. 1. The prior art design is shown in Figure 1, reproduced below.



(PRIOR ART)
FIG. 1

Id. at Fig. 1. "FIG. 1 is a circuit diagram illustrating a conventional POC system for multiple supply voltage devices" and is identified as prior art. *Id*. at 4:18–19, Fig. 1. According to the '674 patent, the POC "is made up of three functional blocks: power-up/down detector 100, signal amplifier 101, and output stage 102. Power-up/down detector 100 has PMOS transistor M1 and NMOS transistors M2-M3." *Id*. at 1:60–63.

2. Overview of Majcherczak

Majcherczak is titled "Power Supply Detection Device" and relates "to a power supply detection device for an integrated circuit using at least two power supply voltages." Ex. 1008, code (54), ¶ 1. Majcherczak describes a voltage detection device that detects when the core voltage is powered down or there is an excessively slow build-up of the voltage. Ex. 1008, code (57), ¶¶ 8–11.

Figure 2 of Majcherczak is shown below.

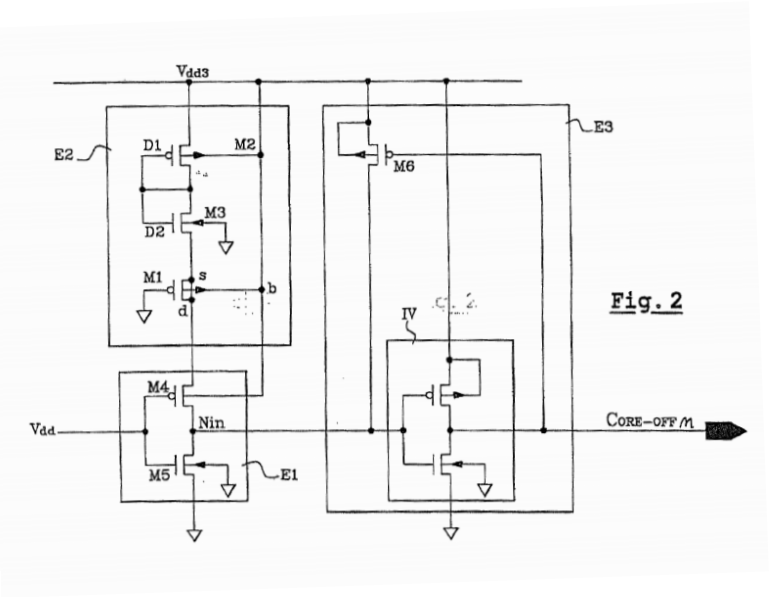


Figure 2 shows a detection device "compris[ing] an output stage E3 following the input stage E1, to obtain the desired output levels for the inverse detection signal CORE-OFF_n." Ex. 1008 ¶¶ 35–37.

3. Using Applicant Admitted Prior Art During an Inter Partes Review

a. The Updated Guidance and the Use of Applicant Admitted Prior Art in Inter Partes Review Proceedings

Prior to briefing on remand, the Director issued guidance discussing how the PTAB will treat a petitioner's reliance on statements made in the specification of a challenged patent. *See* June 9, 2022 USPTO Memorandum Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in *Inter Partes* Reviews Under § 311 ("Updated Guidance").[16] The Updated Guidance supersedes prior guidance (Updated Guidance, 1); accordingly, we apply the Director's Updated

[16] Available at https://www.uspto.gov/sites/default/files/documents/2022060912updatedAAPAmemo.pdf.

Guidance. *See* Updated Guidance, 1 ("The guidance in this Memorandum shall be followed by all members of the Patent Trial and Appeal Board (PTAB or Board)."); 35 U.S.C. § 3(a)(2)(A) (authorizing the Director to "provid[e] policy and management supervision for the Office"), cited by Updated Guidance at 2; *Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320, 1331 (Fed. Cir. 2019), *rev'd on other grounds*, *United States v. Arthrex*, 141 S.Ct. 1970 (2021) (The Director may "issue policy directives and management supervision of the Office" including "instructions that include exemplary applications of patent laws to fact patterns, which the Board can refer to when presented with factually similar cases.").

Section 311(b) of Title 35 of the U.S. Code limits the "basis" of an *inter partes* review to "prior art consisting of patents or printed publications." 35 U.S.C. § 311(b) (2018); *accord* Updated Guidance 2. "[B]ecause admissions are not prior art, and therefore cannot form the basis of an IPR, it is 'impermissible for a petition to challenge a patent relying on solely AAPA without also relying on a prior art patent or printed publication.'" Updated Guidance 2 (quoting *Qualcomm*, 24 F.4th at 1377). However, "[i]f an IPR petition relies on admissions in combination with reliance on one or more prior art patents or printed publications, those admissions do not form 'the basis' of the ground and *must be considered by the Board in its patentability analysis*." *Id.* at 4 (emphasis added).

The Updated Guidance further provides guidance on how to determine if the challenged patent contains an admission:

> Admissions may include statements in the specification of the challenged patent such as "It is well known that . . . ," "It is well understood that . . . ," or "One of skill in the art would

> readily understand that . . .," or may describe the technology as "prior art," "conventional," or ,"well-known."

Updated Guidance 4 (citing *McCoy v. Heal Sys., LLC*, 850 F. App'x 785, 789 (Fed. Cir. 2021) (non-precedential)). The Updated Guidance further provides that the patent owner may dispute whether the statement constitutes an admission: "Of course, parties may dispute the significance or meaning of statements in the specification or other evidence, including disputing whether specification statements constitute admissions or evidence of the background knowledge possessed by a person of ordinary skill in the art." *Id.* at 4–5.

b. Petitioner's Arguments

Petitioner argues that the '674 patent describes AAPA as "conventional." Pet. Remand Br. 1–3. Petitioner further argues that Majcherczak teaches both the alleged invention of the '674 patent—a feedback network—and a number of other claim limitations. *Id.* at 3–6; Pet. Resp. Remand Br. 2.

Petitioner also argues that "[t]he Petition's use of [Patent Owner]'s admissions to show what was known to a skilled artisan before the alleged invention falls squarely within permissible use of AAPA under the Guidance and relevant Federal Circuit precedent." Pet. Remand Br. 6. Specifically, Petitioner argues that "Majcherczak is at the heart of the Petition's relevant obviousness argument for every challenged claim" and no claim is challenged relying solely on AAPA. *Id.* According to Petitioner, "[b]oth the Federal Circuit's decision and the Guidance explicitly permit such use. [Updated] Guidance, 3 ('Admissions are "permissible evidence in an *inter partes* review for establishing the background knowledge possessed by a

person of ordinary skill in the art."' (quoting *Qualcomm*, 24 F.4th at 1376))." *Id.* at 7.

Petitioner further argues that the number of limitations taught by AAPA is not relevant. Pet. Remand Br. 8; Pet. Resp. Remand Br. 2–3. According to Petitioner, "there is no basis for treating admissions any differently than other sources of proof of a skilled artisan's knowledge, such as expert testimony, background references, and so on." Pet. Remand Br. 8 (citing *Koninklijke Philips v. Google, LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020); *Dow Jones & Co. v. Ablaise Ltd.*, 606 F.3d 1338, 1349-50 (Fed. Cir. 2010)). Petitioner further argues that "as the [Updated] Guidance explains, 'the order in which the petition presents the obviousness combination (e.g., prior art modified by admission or admission modified by prior art)' is not relevant." *Id.* (citing Updated Guidance 5; *see also In re Mouttet*, 686 F.3d 1322, 1333 (Fed. Cir. 2012)); *see also* Pet. Resp. Remand Br. 1 (arguing how the ground is styled is irrelevant). According to Petitioner, if the stylization of the grounds or use of the short hand "AAPA grounds" had been determinative, the Federal Circuit would not have remanded the proceeding. Pet. Resp. Remand Br. 1–2.

Petitioner also argues that if we adopt Patent Owner's test that "the 'basis' of a thing is something fundamental to it, or on which the thing rests," Majcherczak is the "basis" of Ground 2.[17] Pet. Resp. Remand Br. 3–5 (quoting PO Remand Br. 5–7). Specifically, Petitioner argues that the Petition "relies on (i.e., rests on) Majcherczak for every single challenged

[17] Ground 2 refers to what the Petitions identify as ground 2a (AAPA in view of Majcherczak) and ground 2b (AAPA in view of Majcherczak and Matthews).

claim." *Id.* at 4. According to Petitioner, because its theory that the addition of one or more feedback networks—the alleged improvement—to the standard system would have been obvious given Majcherczak's teachings, "[i]t defies credibility to suggest that this theory does not rest on Majcherczak, or that Majcherczak is not 'fundamental' to it." *Id.; see also id.* at 5 (expanding on argument).

c. Patent Owner's Arguments

Patent Owner argues that Petitioner has repeatedly conceded that Majcherczak is not the basis of its Petition. PO Remand Br. 4–5. Specifically, Patent Owner argues that Petitioner states that the basis for rejection is "*Applicants Admitted Prior Art (AAPA)* in view of Majcherczak." *Id.* at 4 (citing Pet. 2). Patent Owner further argues that Petitioner uses AAPA "for almost every claim element" while Petitioner relies on "Majcherczak for only a limited aspect of the claims." *Id.*; *see also* PO Resp. Remand Br. 1–3 (arguing "whole swaths of arguments [in the Petition] do[] not mention Majcherczak"). Patent Owner further argues that Petitioner made similar statements in its appeal brief and rehearing petition. PO Remand Br. 5.

Patent Owner also argues that Petitioner's admissions that AAPA is the basis of the *inter partes* reviews are consistent with the statutory language. PO Remand Br. 5–8. Patent Owner argues that "the plain meaning of the 'basis' of a thing is something fundamental to it, or on which the thing rests, as numerous standard dictionary definitions demonstrate." *Id.* at 6 (citing dictionaries). Patent Owner further argues that "[t]he substance of Apple's petition makes clear that AAPA, not Majcherczak, was the 'foundation,' 'main constituent,' 'principal component,' and

'fundamental' and 'underlying fact' of Ground 2; Majcherczak played an ancillary role." *Id.*; *see also id.* at 6–8 (explaining how AAPA was the foundation of the grounds). According to Patent Owner, Petitioner "[b]arely acknowledg[es] § 311(b), [and] never purports to apply the statutory text or even attempts to define 'the basis'—the key provision on remand." PO Resp. Remand Br. 5.

Patent Owner also argues that the Federal Circuit's "specific holding and its discussion of the proper and improper uses of AAPA" when "applied to the circumstances here compels a finding that Ground 2 is impermissible." PO Remand Br. 8. According to Patent Owner, "[b]ecause Apple did not raise Majcherczak as 'the basis,' the Federal Circuit's decision confirms that Ground 2 is impermissible." *Id.* (footnote added).

Patent Owner also argues that "[t]he Updated Guidance on the treatment of AAPA in IPRs does not (and could not) compel a contrary conclusion." PO Remand Br. 9. Specifically, Patent Owner argues that "[i]t does not address the Federal Circuit's narrow directive for remand for this case to determine what is the basis of ground 2." *Id.* Although Patent Owner "recognizes that statements in the Updated Guidance, and its recent application by the Director, would suggest" that the AAPA grounds are permissible because they include a prior art patent, Patent Owner argues "Congress did not use such language; rather, it expressly limited IPRs to grounds 'only on the basis of prior art consisting of patents or printed publications.'" *Id.* at 9–10.

Patent Owner also argues that the Petition does not use AAPA as evidence of general knowledge. PO Resp. Remand Br. 3–4. Instead, Patent Owner argues that Petitioner uses AAPA as a reference and Petitioner

cannot rewrite the Petition at this late date. *Id.* (citing *Koninklijke Philips*, 948 F.3d 1330; *Yeda Research & Development Co. v. Mylan Pharmaceuticals Inc.*, 906 F.3d 1031 (Fed. Cir. 2018)).

Patent Owner also argues that Petitioner "cannot defend Ground 2 by saying Majcherczak teaches the '674 Patent's purported 'novel feature.'" PO Resp. Remand Br. 4. According to Patent Owner, Petitioner took the opposite position in its Reply and such an analysis is inconsistent with the language of 35 U.S.C. § 103(a). *Id.* at 4–5.

d. Our Analysis

By statute, *inter partes* review proceedings can only be requested "on a ground that could be raised under section 102 or 103 and *only on the basis* of prior art consisting of patents or printed publications." 35 U.S.C. § 311(b) (emphasis added); *see also Qualcomm*, 24 F.4th at 1374. Thus, the issue before us is whether AAPA improperly formed the "basis" of Petitioner's challenge. *See Qualcomm*, 24 F.4th at 1376–77 (remanding to determine "whether AAPA improperly formed the 'basis' of Apple's challenge").

The answer to this question is found in the Updated Guidance: "If an IPR petition relies on admissions in combination with reliance on one or more prior art patents or printed publications, those admissions do not form 'the basis' of the ground and *must be considered by the Board in its patentability analysis*." Updated Guidance 4 (emphasis added). Because Petitioner's grounds involve a combination of AAPA and prior art patent(s), AAPA does not form the basis of the ground. *See* Pet. 2 (setting forth the grounds); 1316 Pet. 2 (same). Instead, it is the prior art patents—Majcherczak and, when used, Matthews—that form the basis of the

challenge and AAPA is simply being used to provide missing limitations. *See MED-EL Elektromedizinische Geräte Ges.M.B.H. v. Advanced Bionics AG,* IPR2020-01016, Paper 44 at 4 (PTAB Aug. 22, 2022) (Director Review Decision) ("As discussed above, the Petition relies on AAPA in combination with either Petersen, Zilberman and/or Saaski. Accordingly, AAPA "do[es] not form 'the basis' of the ground and must be considered by the Board in its patentability analysis." (quoting Updated Guidance 4) (modifications in original)).

This is consistent with Federal Circuit case law discussing the use of admissions in proceedings. Specifically, the Federal Circuit "has held 'it is appropriate to rely on admissions in a patent's specification when assessing whether that patent's claims would have been obvious' in an *inter partes* review proceeding." *Qualcomm*, 24 F.4th at 1375 (quoting *Koninklijke Philips*, 948 F.3d at 1339); *see also PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1362 (Fed. Cir. 2007) ("Admissions in the specification regarding the prior art are binding on the patentee for purposes of a later inquiry into obviousness."); *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1998) ("A statement in a patent that something is in the prior art is binding on the applicant and patentee for determinations of anticipation and obviousness."). Indeed, in *Koninklijke Philips* the Federal Circuit "rejected an argument that the general knowledge of a skilled artisan may not be relied on in an *inter partes* review because it does not constitute 'prior art consisting of patents or printed publications' under § 311(b)." *Qualcomm*, 24 F.4th at 1376. Thus, AAPA can be used to, *inter alia*, "supply[] a missing claim limitation." *Id.* (citing *Koninklijke Philips*, 948 F.3d at 1337–38) (alteration in original). Although, in these

proceedings, AAPA is supplying the missing claim limitation not taught in a prior art patent or printed publication, it does not form the basis of the *inter partes* review. *See id.* (recognizing that "even though evidence such as expert testimony and party admissions are not themselves prior art references, they are permissible evidence in an *inter partes* review for establishing the background knowledge possessed by a person of ordinary skill in the art.").

Although we agree with Petitioner that either (1) Majcherczak or (2) Majcherczak and Matthews form the basis for the challenges under Ground 2, we disagree with Petitioner's focus on Majcherczak as teaching the alleged invention of the '674 patent. *See* Pet. Remand Br. 3–6. As the Supreme Court has recognized, "there is no legally recognizable or protected 'essential' element, 'gist' or 'heart' of the invention in a combination patent." *Aro Mfg. Co. v. Converible Top Replacement Co.*, 365 U.S. 336, 345 (1961); *see also Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1345 (Fed. Cir. 2002) (citing *Aro*). Indeed, based on the language of 35 U.S.C. § 103(a), the Federal Circuit has explicitly held that the point of novelty test is "erroneous[]"; instead, the proper focus is on "the subject matter of the invention 'as a whole.'" *Rosemount, Inc. v. Beckman Instruments, Inc.*, 727 F.2d 1540, 1543 n.3 (Fed. Cir. 1984); *accord* 35 U.S.C. § 103(a) ("A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are *such that the subject matter as a whole* would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." (emphasis added)). Because the point of

novelty/gist of the invention test is inappropriate in an obviousness analysis and Petitioner cites no legal authority in support of its argument, we are not persuaded it is appropriate to use it in determining whether an admission in a specification forms the basis of an obviousness challenge in an *inter partes* review. Instead, we focus on the claimed subject matter as a whole. *See* Update Guidance, 5 ("Board panels should review whether the asserted ground *as a whole* as applied to each challenged claim *as a whole* relies on admissions in the specification in combination with reliance on at least one prior art patent or printed publication."). But the disagreement does nothing to detract from our conclusion that Petitioner properly used AAPA in combination with prior art patents or printed publications.

We do not agree with Patent Owner's argument that Petitioner has conceded that AAPA forms the basis of the Ground 2 challenge. Although Petitioner identifies the relevant challenge as being based on AAPA and Majcherczak (with or without Matthews), Patent Owner does not point to a concession that AAPA forms the basis of the ground. *See* PO Remand Br. 4–5. At most, the statements describe how the grounds include both AAPA and a prior art patent, Majcherczak. *Id.* But the fact that a ground relies on both applicant admissions and a prior art patent is not determinative. As the Federal Circuit recognized, "petitioner may rely on evidence beyond prior art documents in an *inter partes* review, even if such evidence itself may not qualify as the 'basis' for a ground set forth in a petition." *Qualcomm*, 24 F.4th at 1375–76. Furthermore, because "a patentee's admissions about the scope and content of the prior art provide a factual foundation as to what a skilled artisan would have known at the time of invention, it follows that AAPA may be used in similar ways in an *inter partes* review." *Id.* at 1376

(citation omitted). Thus, stating that a ground includes both AAPA and Majcherczak is not determinative as to what the ground is based on.

Moreover, the Updated Guidance clearly prohibits the very argument that Patent Owner presents. According to the Updated Guidance, "Board panels should not exclude the use of admissions based on . . . the order in which the petition presents the obviousness combination (e.g., prior art modified by admission or admission modified by prior art)." Updated Guidance 5. Instead, the Updated Guidance mandates that we "should review whether the asserted ground as a whole as applied to each challenged claim as a whole relies on admissions in the specification in combination with reliance on at least one prior art patent or printed publication." *Id.* Consistent with the Updated Guidance, we have reviewed the challenge as a whole and not how the challenge was stated.

We also disagree with Patent Owner's use of the foundation test. *See* PO Remand Br. 5–6. Although a previous Guidance Memo[18] directed that the Board examine the "foundation or starting point" of the ground (Guidance Memo 6 & n.6), that language is removed from and inconsistent with the Updated Guidance (Updated Guidance 5). Moreover, although the Federal Circuit was aware of the Guidance Memo when it issued the *Qualcomm* decision (24 F.4th at 1373), the Court did not direct us to apply the Guidance Memo and its foundation or starting point test in this remand.

[18] August 18, 2020 USPTO Memorandum Addressing Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews under § 311 ("Guidance Memo"), available at https://www.uspto.gov/sites/default/files/documents/signed_aapa_guidance_memo.pdf.

We also disagree with Patent Owner's argument that prohibiting the use of AAPA in this proceeding is consistent with the Federal Circuit's decision. As discussed above, the Federal Circuit repeatedly held that it is appropriate to rely on evidence that is not prior art patents or printed publications in an *inter partes* review, including to supply missing elements. And it did so again in *Qualcomm*. 24 F.4th at 1375–76. Indeed, the entire point of the remand is to determine whether AAPA was the basis for these *inter partes* reviews. If the *Qualcomm* court determined, as Patent Owner argues, that AAPA was the basis, there would have been no need for the remand.

Nor do we see any inconsistency between the Updated Guidance and the Federal Circuit's decision. Notably, although the Federal Circuit remanded the cases to the Board to determine if AAPA was the basis for the *inter partes* reviews, it did not indicate a specific test to use. *See Qualcomm*, 24 F.4th at 1376–77 ("Having determined that (i) the Board incorrectly interpreted § 311(b)'s 'prior art consisting of patents or printed publications' to encompass AAPA contained in the challenged patent, but (ii) the use of AAPA can be permissible in an *inter partes* review, the next contested issue is whether AAPA improperly formed the 'basis' of Apple's challenge. Because the Board did not address this question in its final written decision, we remand to allow the Board to address this issue in the first instance."). Moreover, the Director explicitly relied on *Qualcomm* and the cases it cited in the Updated Guidance.

We also disagree with Patent Owner's argument that Petitioner is attempting to rewrite the Petition. In the Petition, and throughout the current briefing, Petitioner uses AAPA to supply missing claim limitations. There

has been no change in formulation of Ground 2 or what evidence is being used by Petitioner to prove unpatentability. Indeed, there has been no change during the remand as our application of the prior art patent(s) and AAPA to the claims in subsections 4–7, *infra*, is substantially identical to that in the Final Decision.[19] Thus, *Koninklijke Philips*'s admonition that it is an error to institute an *inter partes* review based on "a combination of prior art references [Petitioner] did not advance in its petition" is inapposite. *See* 948 F.3d at 1336.

Similarly inapplicable is *Yeda*. In that case, the Board considered a non-prior art study that started before the filing date of the challenged patent but which was not prior art. *Yeda*, 906 F.3d at 1041. It has no bearing on the use of an applicant's admission. Moreover, the sentence cited by Patent Owner limiting the use of non-prior art references is actually a quote from a Board decision, not a holding of the Federal Circuit:

> The Board has recognized that non-prior art evidence of what was known "cannot be applied, independently, as teachings separately combinable" with other prior art, but "can be relied on for their proper supporting roles, e.g., indicating the level of ordinary skill in the art, what certain terms would mean to one with ordinary skill in the art, and how one with ordinary skill in the art would have under-stood a prior art disclosure." *Dominion Dealer Sols., LLC v. AutoAlert, Inc.*, IPR2014-00684, 2014 WL 5035359, at *5 (P.T.A.B. Oct. 6, 2014).

Id. At most, it is dicta. And to the extent it is inconsistent with Federal Circuit cases that directly address the use of non-prior art such as admissions (*see Qualcomm* and *Koninklijke Philips*), that dicta is neither persuasive nor controlling.

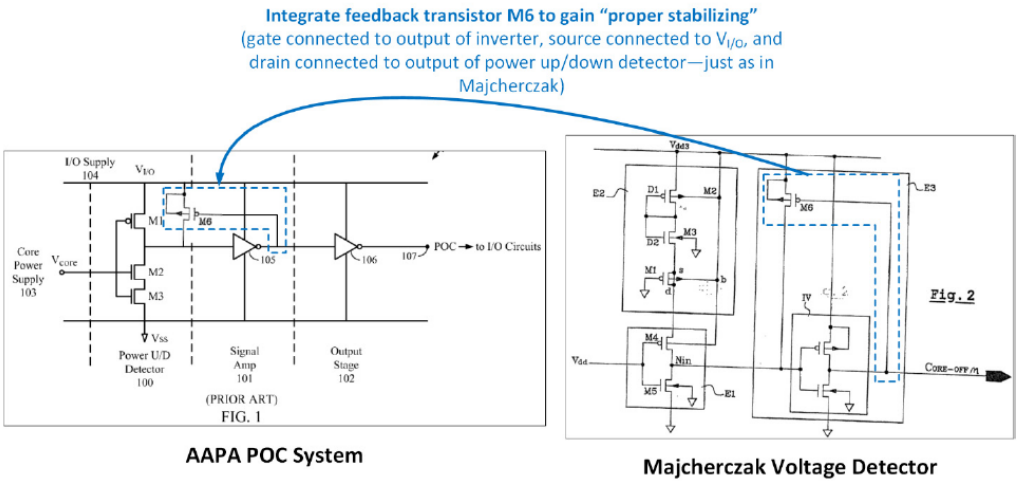
[19] The only changes are the correction of obvious typographical errors.

Accordingly, Petitioner has presented challenges on the "basis of prior art consisting of patents or printed publications," 35 U.S.C. § 311(b), namely Majcherczak and Matthews, and these references are appropriately considered in combination with AAPA.

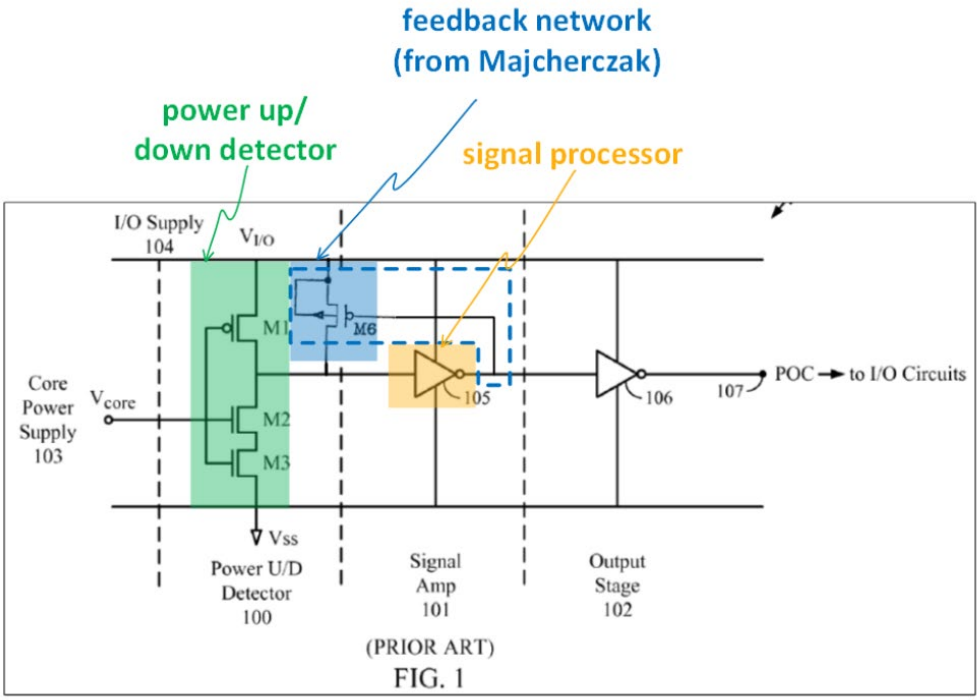
4. Claim 1

a. Undisputed Limitations

Petitioner argues that the combination of AAPA and Majcherczak teaches all of the limitations recited in claim 1. *See* Pet. 37–56. Specifically, Petitioner argues a person of ordinary skill in the art would have combined the feedback circuit of Majcherczak with the POC described in AAPA as shown in the annotated figure reproduced below.



Pet. 44. The figure reproduced above shows Majcherczak's Figure 2 annotated by Petitioner (right) and a version of Figure 1 of the '674 patent (AAPA) modified by Petitioner to integrate the feedback transistor M6 from Majcherczak's Figure 2 (left). *Id.* Petitioner also provides a differently annotated version of its proposed combination as reproduced below.



AAPA + Majcherczak POC System

Pet. 50. The figure above shows what Petitioner contends is the combination of the feedback network of Majcherczak with the POC of AAPA. *Id.* Petitioner's annotations show what Petitioner argues is the power up/down detector in green, the signal processor in yellow, and the feedback network from Majcherczak in blue. *Id.*

Petitioner argues that AAPA in combination with Majcherczak teaches "[a] multiple supply voltage device" as recited in claim 1. Pet. 46. According to Petitioner, "AAPA describes that the prior art POC system 10 is useful in 'newer integrated circuit devices include dual power supplies: one lower-voltage power supply for the internally operating or core applications, and a second higher-voltage power supply for the I/O circuits and devices.'" *Id.* (quoting Ex. 1001, 1:22–25).

Petitioner also argues that AAPA in combination with Majcherczak teaches "a core network operative at a first supply voltage" as recited in claim 1. Pet. 46–47. Specifically, Petitioner argues AAPA includes power up/down detector 100 which is connected to the core power supply, which is a "lower-voltage power supply for the internally operating or core applications." *Id.* (citing Ex. 1001, 1:22–25, 1:60–64).

Petitioner further argues that AAPA in combination with Majcherczak teaches "a control network coupled to said core network wherein said control network is configured to transmit a control signal" as recited in claim 1. Pet. 47. Specifically, Petitioner argues "[t]he prior art power-on/off-control (POC) system 10 is a control network coupled to said core network (via core power supply V_{core}), and the POC system 10 is configured to transmit a power-on/off-control (POC) signal 107." *Id.* (citing Ex. 1001, 1:55–58, 1:65–2:13).

Petitioner also argues that AAPA in combination with Majcherczak teaches "said control network comprising: an up/down (up/down) detector configured to detect a power state of said core network; processing circuitry coupled to said up/down detector and configured to generate said control signal based on said power state" as recited in claim 1. *Id.* at 48–49. Specifically, Petitioner directs us to a comparison of Figure 4 of the '674 patent and the combination of AAPA and Majcherczak, both of which show a power/up down detector and a signal amplifier portion. Pet. 48. Petitioner further argues that "[t]he signal amplifier 101 and output stage 102 are processing circuitry coupled to said up/down detector and configured to generate the power-on/off-control (POC) signal 107 based on said power state." *Id.* at 49.

Petitioner argues the combination of AAPA and Majcherczak teaches "one or more feedback circuits coupled to said up/down detector, said one or more feedback circuits configured to provide feedback signals to adjust a current capacity of said up/ down detector" as recited in claim 1. *See* Pet. 49–52. Specifically, Petitioner argues that, when the teachings of AAPA and Majcherczak are combined as shown in the figure reproduced above, "the feedback transistor M6 is a feedback circuit coupled to the up/down detector 100 via its output." Pet. 51 (citing Ex. 1003 ¶ 141); *see also* Pet. 51–52 (citing Ex. 1003 ¶¶ 142–143). That is, according to Petitioner, "when both transistors M1 and M6 are 'on' (i.e., V_{core} is off), the transistor M6 increases the current capacity of the power up/down detector 100" but "when both transistors M1 and M6 are 'off' (i.e., V_{core} is on), the transistor M6 decreases the current capacity of the power up/down detector 100." Pet. 51–52 (citing Ex. 1003 ¶¶ 142–143).

Petitioner also argues that AAPA in combination with Majcherczak teaches "at least one first transistor coupled to a second supply voltage, the at least one more first transistor being configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on" as recited in claim 1. *See* Pet. 52–53. More specifically, Petitioner argues M1—a first transistor—is coupled to $V_{I/O}$—the I/O power supply or second supply voltage. *Id*. (citing Ex. 1003 ¶ 141; Ex. 1001, 1:62–2:1, 2:8–9). Petitioner further argues that "AAPA explains that the transistor M1 is configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on." Pet. 53 (citing Ex. 1001, 1:65–67, 2:8–9).

Petitioner further argues that AAPA in combination with Majcherczak teaches "at least one second transistor coupled in series with the at least one first transistor and coupled to said first supply voltage, the at least one second transistor being configured to switch on when said first supply voltage is powered on and to switch off when said first supply voltage is powered down" as recited in claim 1. *See* Pet. 54–55. More specifically, Petitioner argues transistor M3 is a second transistor and "AAPA explains that the transistor M3 is configured to switch on when said first supply voltage is powered down and to switch off when said first supply voltage is powered on." *Id*. (citing Ex. 1003 ¶¶ 141, 144–147; Ex. 1001, 1:65–67, 2:8–9).

Petitioner also argues that AAPA in combination with Majcherczak teaches "at least one third transistor coupled in series between the at least one first transistor and the at least one second transistor" as recited in claim 1. Pet. 55–56. Specifically, Petitioner points to transistor M2,[20] which, according to Petitioner, "is coupled in series between transistor M1 (i.e., the first transistor) and transistor M3 (i.e., the second transistor)." Pet. 56 (citing Ex. 1003 ¶ 144).

Patent Owner does not dispute Petitioner's contention that the combination of AAPA and Majcherczak teaches each of the limitations recited in claim 1. *See generally* PO Resp. 20–31; *see also* Pet. Reply 2

[20] The Petition interchangeably refers to transistor M2 and M3 as the third transistor. Pet. 56. However, the Petition specifically refers to the transistor highlighted in brown, which is transistor M2. We stated in the Institution Decision that we would "treat the reference to transistor M3 as a typographical error." Inst. Dec. 19 n.10. Neither party addressed this point in any subsequent briefing. *See generally* PO Resp.; Pet. Reply.

("Beyond this procedural issue [on whether applicant admitted prior art could be considered], Patent Owner's only substantive argument challenging Ground 2 is a purported lack of motivation to combine."); PO Sur-reply 2–19 (not disputing Petitioner's characterization of Patent Owner's argument).

We previously instructed Patent Owner that "any arguments for patentability not raised in the [Patent Owner Response] may be deemed waived." Scheduling Order, Paper 8, 5; *see also In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016) (determining Patent Owner waived arguments made only in its Preliminary Response but not raised in the Patent Owner Response after institution).

Based on the undisputed evidence before us and the reasons set forth in the Petition, Pet. 37–56, we find that the combination of AAPA and Majcherczak teaches all of the limitations recited in claim 1.

b. Whether a Person of Ordinary Skill in the Art Would Have Combined AAPA and Majcherczak

(1) Petitioner's Arguments

Petitioner argues that a person of ordinary skill in the art "would have been motivated to integrate the feedback transistor M6 from Majcherczak's voltage detector into the POC system 10 of AAPA in order to 'enable[] the proper stabilizing of the detection device.'" Pet. 45 (quoting Ex. 1008 ¶ 37) (citing Ex. 1003 ¶ 150). According to Petitioner, the "combination would result in AAPA's POC system 10 observing the 'hysteresis detection' described by Majcherczak, facilitating controlled operation of the I/O devices instructed by the POC signal on communications from the core devices when the core supply voltage is stably on." *Id*. (citing Ex. 1003 ¶ 150); *see also* Pet. Reply 2–5.

Petitioner further argues that "[i]t is undisputed in the [Patent Owner's Reponse] or by Dr. Pedram that adding Majcherczak's feedback transistor M6 to the AAPA as described in the Petition achieves the advantageous hysteresis described in Majcherczak." Pet. Reply 5 (citing PO Resp. 20–31; Ex. 2002 ¶¶ 67–85). According to Petitioner, "Dr. Pedram admits that it was possible to add hysteresis to the AAPA circuit shown in FIG. 1 of the '674 [p]atent, and that such an addition could help improve noise immunity of the circuit." *Id.* (citing Ex. 1017, 46:22–47:10).

Petitioner further argues that "it is irrelevant whether the prior art's explicit motivation to integrate Majcherczak's feedback transistor M6 into the AAPA matches the problem statement of the '674 [p]atent." Pet. Reply 6 (citing *Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1323 (Fed. Cir. 2005)). According to Petitioner, "[i]t is not necessary that the prior art suggest the combination to achieve the same advantage or result purportedly discovered by the Patent Owner." *Id.* (citing *In re Kahn*, 441 F.3d 977, 987 (Fed. Cir. 2006); *Cross*, 424 F.3d at 1323).

Moreover, according to Petitioner, a person of ordinary skill in the art would have a reasonable expectation of success:

> A POSITA would have perceived a reasonable expectation of success in making this modification to the POC system 10 of AAPA, because the POC system 10 and Majcherczak's voltage detector share many functionally commensurate elements, operate in a corresponding manner, and are used in the similar types of multiple supply voltage devices. [Ex. 1003] ¶ 151. Indeed, the integration of the feedback transistor M6 from Majcherczak's voltage detector would have simply been the use of a known technique (a feedback transistor to improve hysteresis) to improve similar devices (detection circuits in multiple supply voltage devices) in the same way. *Id.*

Pet. 45.

Petitioner also argues that any potential disadvantages with the modification identified by Patent Owner and Dr. Pedram—additional leakage current compared to AAPA or Majcherczak, glitch current, and DC fighting condition (*see* PO Resp. 21–31)—"fail to demonstrate the absence of motivation." Pet. Reply 8; *see also id.* at 7–12. Specifically, Petitioner argues that "[i]t is well understood that 'a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.'" *Id.* at 8 (citing *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006)). According to Petitioner, in this case, "the explicit benefit articulated in Majcherczak is not undone or outweighed by the vague and unsupported disadvantages described in the [Patent Owner's Response] and by Dr. Pedram." *Id.*

Petitioner also argues that there is no evidentiary support for any of the potential disadvantages articulated by Patent Owner and Dr. Pedram. Pet. Reply 7–12. Specifically, Petitioner argues neither Patent Owner nor Dr. Pedram cite to any references to support the list of disadvantages and Dr. Pedram admitted that the list is hypothetical and "that he never simulated any of the prior art or proposed combinations to determine what, if any, performance issues would arise from the proposed combination." *Id.* at 7–8 (citing Ex. 1017, 40:15–41:13, 45:9–15, 59:4–8, 61:4–10, 65:7–14, 167:20–23, 170:13–171, 171:20–172:1, 180:6–16, 187:25–188:9) (footnote omitted). Petitioner further argues that "[w]ithout corroborating evidence to contradict the explicit motivating teaching of Majcherczak, Dr. Pedram's statements are unsupported, exposing them as insufficient to establish substantial evidence addressing or confronting the affirmative proof offered by

Petitioner." *Id.* at 8 (citing *Ericsson Inc. v. Intellectual Ventures I LLC*, 890 F. 3d 1336, 1346 (Fed. Cir. 2018)).

Petitioner further argues that the problems of the asserted combination alleged by Patent Owner are "not inherent in the proposed architectural combination. Rather, such issues would only potentially arise due to an improper selection of design characteristics such as the transistor sizes, threshold voltages, and values of $V_{I/O}$ and V_{core}." Pet. Reply 9 (citing Ex. 1018 ¶¶ 7–9, 74–77); *see also id.* at 12 ("Even assuming a POSITA would have considered these as potential disadvantages in implementing the proposed combination, the POSITA would nevertheless have been motivated for reasons cited within Majcherczak to make the combination, as the POR's alleged disadvantages and their potential adverse impacts either would not have been observed or a POSITA would have been able to minimize them." (citing Ex. 1018 ¶¶ 50–64)).

With regard to additional leakage current (PO Resp. 21–27), Petitioner argues that "Dr. Pedram acknowledged that it is the unclaimed design details—transistor sizes, threshold voltages, and values of $V_{I/O}$ and V_{core}—that will determine the amount of leakage present in the proposed combination." Pet. Reply 10 (citing Ex. 1017, 63:22-65:20). Petitioner further argues that "Dr. Horst shows through simulation of these designs" that the proper selection of design details result in "mitigat[ing] any potentially problematic increase in leakage current, leaving the power consumption due to leakage current to be relatively the same or even better than either the AAPA or Majcherczak alone." *Id.* (citing Ex. 1018 ¶¶ 50–64, 68–73).

With regard to glitch current (PO Resp. 27–30), Petitioner argues that because the '674 patent acknowledges that glitch current was an issue with AAPA, "the addition of Majcherczak's feedback transistor would not have created a new problem in the circuit." Pet. Reply 10 (citing Ex. 1001, 2:25–30; Ex. 1018 ¶¶ 31, 56, 57, 75–77). Petitioner further argues that Dr. Horst's simulation shows that the glitch current can be mitigated by a proper selection of threshold voltages. *Id.* at 11 (citing Ex. 1018 ¶¶ 21–31, 50–64).[21]

With regard to the DC fighting condition (PO Resp. 27–30), Petitioner argues that Dr. Pedram states that this "'could happen' only on 'rare occasions,' making any assessment of a hypothetical DC fighting condition a 'complicated task.'" Pet. Reply 11 (quoting Ex. 1017, 181:10–24). Petitioner further argues that "[t]he condition is so complicated and rare, in fact, that Dr. Pedram believes that a POSITA would not even see or be aware of this disadvantage when analyzing the proposed combinations." *Id.* (citing Ex. 1017, 175:11–15). According to Petitioner, a person of ordinary skill in the art "cannot have been dissuaded by a potential 'rare' problem he/she would not have even been aware of." *Id.* Petitioner further argues that the condition is dependent on the selection of design details and "this alleged problem did not arise in Dr. Horst's simulations." *Id.* at 11–12 (citing Ex. 1017, 172:10–173:16, 178:9–181:24; Ex. 1018 ¶¶ 30, 32, 33).

[21] Petitioner's Reply cites to Exhibit 2018. Based on the context of the sentence, this appears to be a typographical error and that Petitioner intended to cite Exhibit 1018.

(2) Patent Owner's Arguments

Patent Owner argues that, because "Petitioner's proposed combination results in a circuit with numerous operational flaws" that "would operate significantly worse than either the AAPA or Majcherczak had they been left unmodified," a person of ordinary skill in the art would "have had no reason to combine the alleged AAPA and Majcherczak as Petitioner proposes." PO Resp. 21; *see also id.* at 21–31; PO Sur-reply 2–19.

First, Patent Owner argues that "Petitioner's proposed addition of Majcherczak's transistor M6 to Fig. 1 of the '674 Patent (the alleged AAPA) results in *increased* leakage current, and the POSA would not be motivated to make Petitioner's proposed combination for at least this reason." PO Resp. 22 (citing Ex. 2002 ¶ 70); *see also id.* at 21–25; PO Sur-reply 4–5. Specifically, Patent Owner argues when the core power supply voltage (V_{core}) is on, "PMOS transistor M1 and feedback transistor M6 will be 'off,' and NMOS transistors M2 and M3 will be 'on' providing a path between the output of the power U/D detector 100 and ground." PO Resp. 23–24. Patent Owner further argues that "[b]ecause [V_{core}] is less then $V_{I/O}$, however, PMOS transistor M1 will be quite leaky, providing a high leakage path from $V_{I/O}$ to the output terminal of the power U/D detector 100." *Id.* at 24 (citing Ex. 2002 ¶ 72). Patent Owner further argues that "NMOS transistors N2 and M3 will be 'on,' providing a very low resistance path from the output terminal to Vss." *Id.* According to Patent Owner, as a consequence, "a high leakage DC path will exist between $V_{I/O}$ and Vss," which will result in more leakage current than would be present in the unmodified AAPA. *Id.* (citing Ex. 2002 ¶¶ 72–73).

Second, Patent Owner argues that the modified design "would also operate less effectively than Majcherczak alone." PO Resp. 25; *see also id.* at 25–27. Specifically, Patent Owner argues that "a [person having ordinary skill in the art] would have recognized that Majcherczak's power supply stage (E2) operates to reduce leakage current through the pull-up PMOS transistor (M4) in the input stage (E1) and thus helps to offset any additional leakage current introduced by the feedback transistor (M6)." *Id.* at 26 (citing Ex. 2002 ¶¶ 76–78). According to Patent Owner, because Petitioner does not suggest incorporating Majcherczak's power supply stage (E2) into the AAPA, "[t]he power detection circuit depicted in Fig. 2 of Majcherczak would thus operate with significantly less leakage current than Petitioner's proposed combination." *Id.* at 26–27 (citing Ex. 2002 ¶¶ 76–79).

Third, Patent Owner argues that Petitioner's proposed combination "would also introduce substantial operational problems during the process of powering on the core voltage supply (Vcore), causing increased glitch (i.e., crowbar) current and circuit instability." PO Resp. 27; *see also id.* at 27–30. More specifically, Patent Owner argues that "switching delays of the power up/down detector 100 and inverter 105 . . . will cause the feedback transistor M6 . . . to remain on for at least some delay period after the core power supply voltage (Vcore) turns on." *Id.* at 28 (citing Ex. 2002 ¶¶ 81–82). Patent Owner further argues that this can cause an unstable DC fighting condition during the inverter delay period. *Id.* (citing Ex. 2002 ¶ 83). According to Patent Owner, the DC fighting condition "can cause a downstream ripple effect such that Inverter 105 . . . becomes unstable, causing further instability in the 'feedback network' . . ., and potentially

resulting in a complete circuit breakdown" or, at the very least, worsen the glitch current. *Id.* at 28–30 (citing Ex. 2002 ¶¶ 83–84).

Patent Owner further argues that, contrary to Petitioner's arguments, a person of ordinary skill in the art would not seek to add hysteresis. PO Sur-reply 2–4. According to Patent Owner, a person having ordinary skill in the art would, instead, focus on how to solve the problems articulated in AAPA—high leakage current and slow switching times. *Id.* More specifically, Patent Owner argues that (1) a person having ordinary skill in the art would have avoided adding hysteresis because it would make the problems identified in the '674 patent worse, (2) in light of the switching-speed problem articulated in the AAPA, the addition of hysteresis involves impermissible hindsight, and (3) AAPA does not suggest that stability is a problem in AAPA's circuit. *Id.* at 4–6.

Patent Owner further argues that Petitioner's argument (Pet. Reply 7) that Dr. Pedram does not cite to any references to support his list of disadvantages is misplaced. PO Sur-reply 7. According to Patent Owner, no references are needed because the disadvantages "are all well-known phenomena that would be immediately apparent to the [person having ordinary skill in the art] upon considering the proposed combination" and "Petitioner sets forth no argument that the disadvantages described by Dr. Pedram are obscure or not generally understood, and such an assertion would be wrong." *Id.* Patent Owner further argues that "the reply cites no statute, rule, or caselaw to support the proposition that an expert's opinion must be corroborated by independent references." *Id.*

Patent Owner also argues that Petitioner's citation to "*Medichem, S.A. v. Rolabo, S.L.* that 'a given course of action often has simultaneous

advantages and disadvantages, and this does not necessarily obviate motivation to combine'" is misplaced because "the purported advantage of Majcherczak is no advantage at all." PO Sur-reply 7–8.

Finally, Patent Owner presents six arguments explaining why Dr. Horst's simulations do not prove that a person of ordinary skill in the art would have been motivated to combine AAPA and Majcherczak. *See* PO Sur-reply 8–18.

First, Patent Owner argues that "Petitioner's argument misunderstands the proper inquiry for obviousness." *Id.* at 8. According to Patent Owner, "[t]he relevant question is whether the [person of ordinary skill in the art] would be motivated to combine the alleged AAPA and Majcherczak to reach the claimed invention," not whether the person of ordinary skill in the art would combine the references and then use a simulation to determine a set of parameters that would avoid the problems identified by Dr. Pedram. *Id.* at 8–9.

Second, Patent Owner argues that the simulations are unreliable because Dr. Horst's supplemental declaration contained numerous errors. *See* PO Sur-reply 9–11. For example, Patent Owner points out how the results in the simulation of two different circuits were identical. *Id.* at 9 (comparing Ex. 1018 ¶ 12 with Ex. 1018 ¶ 23). Patent Owner points out that a corrective declaration with a new set of graphs intended to replace page 15 of the supplemental declaration introduced a new error in the results of Figure 4. *Id.* at 9–11 (citing Ex. 2007).

Third, Patent Owner argues that Dr. Horst selected unrealistic parameter values that the person of ordinary skill in the art would never use in the proposed combination of AAPA and Majcherczak. *See* PO Sur-

reply 11–16. Specifically, Patent Owner argues Dr. Horst selected a high FET threshold voltage that results in the problem of slow switching speed discussed in the '674 patent, the selected channel length and width parameters were selected from the Voss reference (Exhibit 1022) that is not from the field related to the technology of AAPA, and that the values are divorced from real world considerations. *Id.*

Fourth, Patent Owner argues Dr. Horst "cherry picked" parameter values without providing a sufficient rationale for their selection. PO Sur-reply 16–17. Specifically, Patent Owner criticizes Dr. Horst for using the values of the Voss reference for most transistors but provides no explanation for why the Voss reference was not used for all transistors. *Id.* Patent Owner further argues that Dr. Horst explained at his deposition that he changed the width of the feedback transistor from that given in Voss because if the Voss parameters were used consistently, the simulation would fail. *Id.* at 17 (citing Ex. 2006, 101:24–102:17).

Fifth, Patent Owner argues that Dr. Horst's simulation does not show that the combination of AAPA and Majcherczak does not result in increased leakage current. PO Sur-reply 17–18. Specifically, Patent Owner argues that ramping the V_{core} to max value and then immediately pulling back—as done in the simulation—is not an accurate way of measuring leakage current. *Id* at 18. Patent Owner argues that leakage power is primarily a problem when V_{core} is high and, if the simulation was addressing leakage, it should have left V_{core} voltage at 3.3V for at least some time. *Id.* at 18.

Sixth, Patent Owner argues that a single simulation is not sufficient. PO Sur-reply 18–19. More specifically, Patent Owner argues that a typical engineer will perform thousands of computer simulations and that "a single

simulation result cannot provide an accurate indication of whether a circuit would operate correctly under realistic, real-world conditions." *Id.* at 19. Patent Owner further argues that, although Dr. Horst's testimony discusses a single simulation, Dr. Horst executed many more simulations, but did not save the results of those simulations. *Id.* at 18–19.

(3) Our Analysis

A conclusion of unpatentability based on obviousness must be supported by "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Kahn*, 441 F.3d at 988 (citations omitted), *cited with approval in KSR*, 550 U.S. at 418. The requirement for a reason to combine the reference acts as a check on the potential for the improper use of hindsight. *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (holding that an articulated reasoning "is especially important to guard against the dangers of hindsight bias").

Based on the entirety of the record, we find Petitioner has shown sufficiently articulated reasoning with rational underpinning to support the legal conclusion of obviousness. Petitioner provides detailed analysis of the prior art and explains why, based on the teachings of the references, a person of ordinary skill in the art would have combined the references. *See* Pet. 37–45; Pet. Reply 3–6.

It is undisputed that Majcherczak identifies a problem with circuits with multiple supply voltage devices when the core voltage is powered down or slow to power up. *See* Ex. 1008 ¶¶ 7–8; *see also* Pet. 39. Specifically, Majcherczak states that

> [w]hen the core supply voltage disappears, the two logic voltages DATA and /DATA fall to zero. The two control transistors are then off. The voltage at an output of the

> translator becomes uncontrollable and dependent on the leakage currents in the transistors of the translator, or on a contradiction between two logic signals.

Ex. 1008 ¶ 7.

Majcherczak teaches using an output stage E3 which includes a "transistor M6 for pulling the output node Nin of the inverter of the input stage to the interface [I/O] power supply voltage Vdd3." Ex. 1008 ¶ 37. Majcherczak describes that "transistor M6 enables the proper stabilizing of the detection device. It maintains the node Nin at Vdd3, by feedback." *Id.* Majcherczak further describes how this allows for a hysteresis detection:

> With the output stage E3, a hysteresis detection is obtained with a low threshold of switching from a state of the presence of a core power supply to a state of the absence of a core power supply, and a high threshold of switching of the detection circuit from a state of absence of the core supply to a state of presence of the core supply. In particular, if the output node Nin of the input stage is at Vdd3, then the signal IN applied to its input rises sufficiently to force the output node Nin downwards, and consequently, cut off the pull-down transistor M6. In a practical example, for integrated circuits using 0.18 μ technology with a core supply voltage of 1.8 volts, the high threshold may thus be equal to 0.98 volts and the low threshold may be equal to 0.33 volts.

Id. ¶ 38. "[H]ysteresis detection is useful for ensuring that the level shifters only operate to facilitate communications between the core network and the I/O network when the core supply voltage is stably on." Ex. 1003 ¶ 138 (Horst Decl.).

We are persuaded by the evidence in the record that a person having ordinary skill in the art would have "integrate[d] feedback transistor M6 from Majcherczak's voltage detector into the POC system 10 of the AAPA in order to 'enable[] the proper stabilizing of the detection device.'"

Ex. 1003 ¶ 150 (Horst Decl.) (quoting Ex. 1008 ¶ 37). The person having ordinary skill of the art would have made such a modification to add hysteresis detection to AAPA's POC system 10, thereby "ensuring that the I/O devices instructed by the POC signal only operate on communications from the core devices when the core supply voltage is stably on." *Id.*

It is inapposite that the reason for the modification is different from the problem being addressed in the '674 patent. In *KSR*, the Supreme Court rejected the application of rigid rules, such as considering only the problem the patentee was trying to solve:

> The first error of the Court of Appeals in this case was to foreclose this reasoning by holding that courts and patent examiners should look only to the problem the patentee was trying to solve. *The Court of Appeals failed to recognize that the problem motivating the patentee may be only one of many addressed by the patent's subject matter*. The question is not whether the combination was obvious to the patentee but whether the combination was obvious to a person with ordinary skill in the art. *Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed*.

KSR, 550 U.S. at 420 (emphases added, citations omitted). Instead, the Supreme Court applied a flexible approach, holding that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 417; *see also id.* ("When a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an

arrangement, the combination is obvious.") (internal quotation and citation omitted).

Consistent with the Supreme Court's *KSR* holding, the Federal Circuit has similarly rejected arguments based on a reason to combine that were different from the one identified by the patentee. For example, in *Samsung Electronics Co. v. UUSI, LLC*, the Federal Circuit reversed a PTAB decision that required the reason to combine the references to be directed to the same problem as identified in the challenged patent:

> UUSI next argues that the Board was correct in finding that Gerpheide was addressed to a different problem, referring us to its expert's testimony regarding the fact that Gerpheide and the '183 patent were directed to different problems and solved those problems in different ways. **Samsung argues that under *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 127 S.Ct. 1727, 167 L.Ed.2d 705 (2007), the Board's decision was legally erroneous because it required the proffered motivation to combine Gerpheide with Ingraham/Caldwell to be the same as the one that animated the patentee in arriving at the claimed invention. We agree with Samsung**. The Board's categorical rejection of the teachings from a single input device to those of a multi input device is not supportable. "[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 417, 127 S.Ct. 1727.

Samsung Electronics Co. v. UUSI, LLC, 775 F. App'x 692, 695 (Fed. Cir. 2019) (emphasis added); *see also In re Conrad*, 759 F. App'x 982, 985 (Fed. Cir. 2019) ("The Supreme Court and this court, however, have repeatedly held that the motivation that a person of ordinary skill in the art would have had to combine prior art references need not be the same motivation that inspired the patent owner." (citation omitted)); *In re Beattie*, 974 F.2d 1309,

1312 (Fed. Cir. 1992) ("As long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not required that the references be combined for the reasons contemplated by the inventor.").

Furthermore, the evidence shows that a person having ordinary skill in the art would have had a reasonable expectation of success. *See* Ex. 1003 ¶ 151 (Horst Decl.). Specifically we are persuaded by Dr. Horst's testimony that "the integration of feedback transistor M6 from Majcherczak's voltage detector would have simply been the use of a known technique (a feedback transistor to provide hysteresis) to improve similar devices (detection circuits in multiple supply voltage devices) in the same way." *Id.*

We disagree with Patent Owner's arguments, discussed below.

Explicit Motivation: As a preliminary matter, for the reasons discussed above with regard to reason to combine, we are not persuaded by Patent Owner's argument that an explicit motivation to combine the references is required for obviousness. *See* PO Sur-reply 2–6. Moreover, Patent Owner's argument that Majcherczak's hysteresis detection does not provide an explicit motivation to combine the references is not timely and waived. *See* PO Sur-reply 2–6. Petitioner made its hysteresis argument in the Petition and Patent Owner did not address the arguments in its Response. *Compare* Pet. 45 (relying on hysteresis detection for the reason to combine the references), *with* PO Resp. 20–31 (not discussing hysteresis); *see also* Tr. 74:13–18 (acknowledging the argument was not raised in the Patent Owner's Response). Although Patent Owner addresses this argument in its Sur-reply, "arguments for patentability not raised in the response may be deemed waived." Scheduling Order, Paper 8, 5; *see also Nuvasive*, 842 F.3d

at 1380–81 (holding that an argument not presented in Patent Owner's response is waived); *Dell Inc. v. Acceleron, LLC*, 884 F.3d 1364, 1369 (Fed. Cir. 2018) (holding that the Board was not obligated to consider an "untimely argument"). Because Patent Owner did not address Petitioner's argument regarding an explicit motivation in the Patent Owner's Response, that argument is waived.

Potential Issues: We do not agree with Patent Owner that a person having ordinary skill in the art would not have combined AAPA with Majcherczak because of the following potential issues identified by Dr. Pedram: additional leakage current compared to AAPA, glitch current, and a DC fighting condition. *See* PO Resp. 21–25, 27–31. Patent Owner's argument relies exclusively on Dr. Pedram's testimony as support for why a person having ordinary skill in the art would not make the proposed modification due to the identified "problems." *See id.* (citing Ex. 2002 ¶¶ 70–74, 81–85). However, Dr. Pedram does not cite to any evidence to support his opinions. *See* Ex. 2002 ¶¶ 70–74, 81–85. That is, Dr. Pedram does not cite to any tests, references, or simulations that support his opinion. *Id.*; Ex. 1017, 41:6–13, 171:20–171:3 (Pedram Dep.).

This stands in marked contrast to Dr. Horst's testimony. In response to Dr. Pedram's argument that the combination of AAPA and Majcherczak would result in increased leakage current, glitch current, or a DC fighting condition, Dr. Horst conducted a computer simulation to demonstrate that, with the appropriate selection of design details, those potential problems

could be managed. *See* Ex. 1018 ¶¶ 21–33 (Horst Supp. Decl.); Ex. 2007 (Horst Corrective Decl.).[22]

Our rules provide that "[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight." 37 C.F.R. 42.65(a). In light of the failure to provide any corroboration, such as a simulation, we give Dr. Pedram's conclusory, unsupported testimony little weight. *See In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *Verlander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) (noting that the Board has discretion to accord little weight to broad conclusory statements from expert witness); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985) (noting that the "[l]ack of factual support" for an expert opinion "may render the testimony of little probative value").

In contrast to the potential issues discussed in the preceding paragraphs, Dr. Pedram provides some factual support for his testimony that the proposed modification would result in an increased leakage current compared to Majcherczak alone. *See* Ex. 2002 ¶¶ 75–80 (citing Ex. 1008). However, although Dr. Pedram may have established that "[t]he power detection circuit depicted in Fig. 2 of Majcherczak would thus operate with significantly less leakage current than Petitioner's proposed combination, which omits the power supply stage (E2) of Majcherczak," (Ex. 2002 ¶ 79), that is not the relevant issue. Instead, the issue is whether a person of

[22] We address Patent Owner's arguments regarding Dr. Horst's simulation *infra*.

ordinary skill in the art would have improved AAPA by "integrat[ing] feedback transistor M6 from Majcherczak's voltage detector into the POC system 10 of the AAPA in order to 'enable[] the proper stabilizing of the detection device.'" Ex. 1003 ¶ 150 (Horst Decl.) (quoting Ex. 1008 ¶ 37).

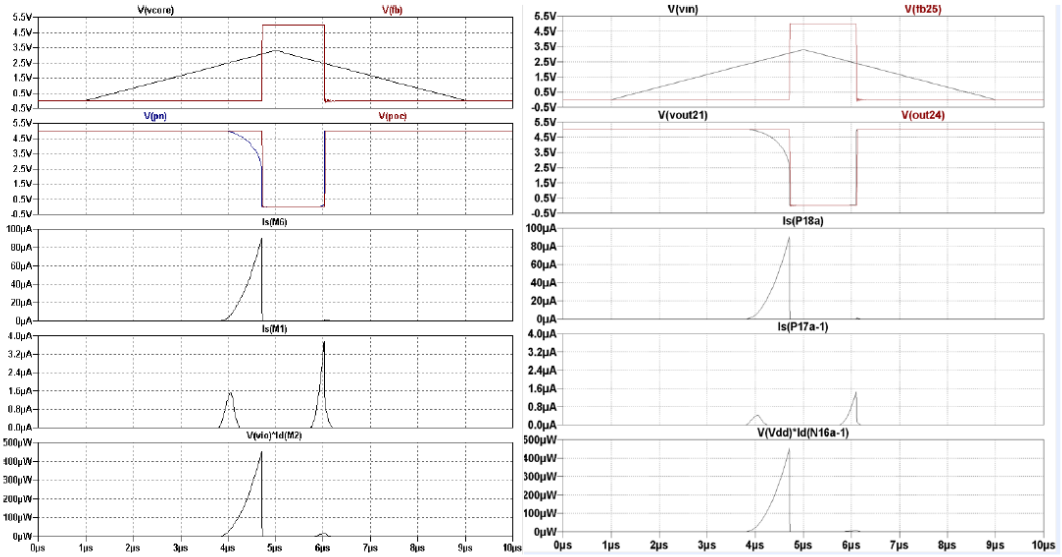
Moreover, merely identifying potential problems that could arise with a combination of references is not, by itself, enough to demonstrate that the combination would not have been obvious. Rather, "a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine." *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (citing *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n. 8 (Fed. Cir. 2000)). Accordingly, "[t]he fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another." *Winner*, 202 F.3d at 1349 n.8. Although Patent Owner and Dr. Pedram identify potential problems with the combination of AAPA and Majcherczak, they do not weigh the relative advantages and disadvantages. Considering only one half of the analysis is not sufficient. This is especially true in light of (1) the explicit benefit discussed in Majcherczak and (2) the unsupported identification of potential issues in the Patent Owner's Response and Dr. Pedram's testimony.

Additionally, we are persuaded by Dr. Horst's testimony that any potential problems in the combination would have been addressed by the person having ordinary skill in the art by the selection of appropriate design characteristics such as the transistor sizes, threshold voltages, and values of

$V_{I/O}$ and V_{core}. *See* Ex. 1018 ¶¶ 74–77; *see also id.* ¶¶ 50–73. That is, the simulation performed by Dr. Horst shows that, under at least one set of design characteristics, the problems identified by Dr. Pedram do not exist. *Id.* ¶¶ 21–31 (Horst Supp. Decl.); Ex. 2007 ¶¶ 2–4 (Horst Corrective Decl.). Although the evidence does not show that every permutation of design characteristics will work, the evidence does show that it would have been within the ability of a person having ordinary skill in the art to determine appropriate design values to minimize or eliminate the potential problems identified by Dr. Pedram.

Reliability of Dr. Horst's Simulations: We do not agree with Patent Owner that Dr. Horst's simulation is unreliable because the results for two different circuits are identical. *See* PO Sur-reply 9 (citing Ex. 1018, ¶¶ 12, 23). As Patent Owner concedes, prior to his deposition, Dr. Horst prepared a corrective declaration pointing out the mistake and replacing the erroneous charts from page 15. *Id.* at 9–10; *see also* Ex. 2007 (Horst Corrective Decl). In light of Dr. Horst's recognition that he "inserted the wrong set of graphs when preparing [his] supplemental report" and timely provided a correction prior to cross examination, *see* Ex. 2007, ¶ 2, we do not find that the original mistake renders the simulation unreliable. To the contrary, we credit Dr. Horst for recognizing his mistake and providing the correct graphs.

Nor are we persuaded that the introduction of a second mistake in the corrective declaration renders the simulation unreliable. *See* PO Sur-reply 9–11. A comparison of the results of Dr. Horst's simulation relating to Figure 4 of the '674 patent and the combination of AAPA and Majcherczak from his Supplemental Declaration—the original simulation report—is reproduced below.



Simulations of the '674 Figure 4 circuit (left) and AAPA+ Majcherczak (right). Waveforms are nearly identical.

Ex. 1018 ¶ 23 (Horst Supp. Decl.). The figure above shows the results of Dr. Horst's simulation of the circuit of Figure 4 of the '674 patent (left) and the circuit that is the result of the combination of AAPA and Majcherczak (right). *Id.* Relevant to our analysis, the third graph for the Figure 4 circuit is labeled Is(M6). Patent Owner has not alleged any error in the labeling of this chart. *See generally* PO Sur-reply.

However, in the replacement graph of the Corrective Declaration, that graph is relabeled as Is(M2). Ex. 2007, ¶ 2 (Horst Corrective Decl.); *see also* PO Sur-reply. As Patent Owner points out in the Sur-reply, there is no transistor M2 in the Figure 4 embodiment. *See* Ex. 1018 ¶ 22. Because the labeling was correct in the original version and the correction focused on the graphs on the right side, not the left, this appears to be no more than a typographical error. As such, it does not have a substantial impact on Dr. Horst's credibility.

In conclusion, we have considered Patent Owner's arguments. However, based on the entirety of the record, we find Dr. Horst's simulations and Dr. Horst's discussion of those simulations reliable.

Selection of Simulation Values: Additionally, we are not persuaded by Patent Owner's argument that the values selected by Dr. Horst are divorced from real world considerations. First, Patent Owner argues that "Dr. Horst conceded, however, that his simulations enabled him to choose any desired threshold voltage, even if that voltage was inconsistent with the transistor's minimum feature size and the supply voltage." PO Sur-reply 15–16 (citing Ex. 2006, 93:3–13). However, Patent Owner's characterization is not consistent with Dr. Horst's testimony. Instead, during the cited cross-examination, Dr. Horst simply testified that "you can directly set the threshold value . . . not dependent on the – on that minimum feature size parameter"; he never stated that it was inconsistent with the minimum feature size, as argued by Patent Owner. Ex. 2006, 93:3–13.

Second, although Patent Owner argues that "when asked whether his selected threshold voltage of 2.3V would be typical for transistors having a 5V supply voltage and a minimum feature size of 0.8 μm, Dr. Horst conceded that he chose the 2.3V value simply because it 'gave good results,'" that is also not supported by the actual testimony. *See* PO Sur-reply 16 (citing Ex. 2006, 94:5–13). Dr. Horst was not asked whether the value was typical but instead stated that he made the selection because it gave expected results for the '674 patent Figure 4—the patented design. Ex. 2006, 94:5–13. Although the results may have been unreliable had Dr. Horst selected values designed to make AAPA/Majcherczak circuit provide good results, Patent Owner has not sufficiently explained why it is improper

to pick design parameters that would make the reference circuit (Figure 4 of the '674 patent) work in the manner described in the '674 patent. For the same reason, we are unpersuaded by Patent Owner's argument that Dr. Horst "cherry picked" design parameters so that the circuit would work; rather, Dr. Horst simply testified that he adjusted the parameters to make reference '674 patent Figure 4 circuit work. *Compare* PO Sur-reply 17, *with* Ex. 2006, 101:24–102:17.

Third, Patent Owner's arguments that Dr. Horst used unrealistic parameter values, that the simulation fails to show that the combination does not result in increased leakage current, or that the simulation consisted of only a single simulation are not sufficient to rebut Petitioner's persuasive evidence on why a person having ordinary skill in the art would have combined AAPA and Majcherczak. *See* PO Sur-reply 11–15, 17–19. Petitioner did not offer the simulation and testimony to demonstrate that a person having ordinary skill in the art would combine the references. Instead, Petitioner offered the simulation and Dr. Horst's accompanying testimony to rebut Dr. Pedram's testimony regarding potential problems with the circuit. *See* Pet. Reply 10–12. Because we are not persuaded by Dr. Pedram's testimony regarding the potential problems, even if we accepted Patent Owner's criticisms and discounted Dr. Horst's simulation and accompanying testimony, Dr. Horst's original testimony regarding the benefits of hysteresis detection is sufficient to demonstrate why a person having ordinary skill in the art would have been motivated to combine Majcherczak and AAPA.

Accordingly, for the reasons discussed above, Petitioner provided "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See Kahn*, 441 F.3d at 988.

c. Conclusion

We have considered the entirety of the evidence submitted by the parties, both for and against obviousness, and determine that Petitioner has shown by a preponderance of the evidence that claim 1 of the '674 patent would have been obvious over the combined teachings of AAPA and Majcherczak.

5. Claims 2, 5, and 6

Petitioner presents persuasive arguments and evidence regarding claims 2, 5, and 6, each of which depends from claim 1. *See* Pet. 57–62.

Claim 2 recites "wherein said one or more feedback circuits comprise: one or more first feedback transistors coupled in parallel with said one or more first transistors and coupled to receive feedback from said processing circuitry, wherein said one or more first feedback transistors are configured to switch off when said processing circuitry indicates that said first supply voltage is powered on." Ex. 1001, 9:4–11. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claim 2. Pet. 57–59; *see also* Ex. 1003 ¶¶ 141, 146 (Horst Decl.).

Claim 5 recites "further comprising: an input/output (I/O) network operative at a second supply voltage, wherein said I/O network is coupled to said core network and said control network, and wherein said I/O network is configured to receive said control signal." Ex. 1001, 9:34–39. Petitioner argues that the combination of AAPA and Majcherczak teaches the

additional limitation recited in claim 5. Pet. 59–60; *see also* Ex. 1003 ¶¶ 148–149 (Horst Decl.).

Claim 6 recites that "the device is integrated into a semiconductor die." Ex. 1001, 9:40–41. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claim 6. Pet. 61–62; *see also* Ex. 1003 ¶¶ 124, 125 (Horst Decl.).

Patent Owner does not separately address the additional limitations recited in claims 2, 5, and 6. *See generally* PO Resp.

Having considered the entirety of the evidence submitted by both parties, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 2, 5, and 6 of the '674 patent would have been obvious to a person of ordinary skill in the art based on the combined teachings of AAPA and Majcherczak.

6. Claims 8 and 17

Claims 8 and 17 are independent claims. Ex. 1001, 9:48–10:3, 11:14–12:5. Petitioner relies on the same combination of AAPA and Majcherczak discussed above in subsection 4(a), and makes similar arguments regarding the limitations of claims 8 and 17. *Compare* Pet. 43–44, 46–56, *with* 1316 Pet. 51–52, 54–63. That is, Petitioner relies on the same combination of AAPA and Majcherczak and maps the limitations recited in method claim 8 and system claim 17 to the operation of the circuit. *See* 1316 Pet. 51–52, 54–63.

Patent Owner does not dispute that the combination of AAPA and Majcherczak teaches each of the limitations recited in claims 8 and 17. *See generally* 1316 PO Resp. 20–31; *see also* 1316 Pet. Reply 2 ("Beyond this procedural issue [on whether applicant admitted prior art could be

considered], Patent Owner's only substantive argument challenging Ground 2 is a purported lack of motivation to combine."); 1316 PO Sur-reply 2–19 (not disputing Petitioner's characterization of Patent Owner's argument).

We previously instructed Patent Owner that "any arguments for patentability not raised in the [Patent Owner Response] may be deemed waived." 1316 Paper 8, 5 (Scheduling Order); *see also NuVasive*, 842 F.3d at 1380–81 (determining Patent Owner waived arguments made only in its Preliminary Response but not raised in the Patent Owner Response after institution).

Based on the undisputed evidence before us and the reasons set forth in the Petition (Pet. 45–63), we find that the combination of AAPA and Majcherczak teaches all of the limitations recited in claims 8 and 17.

Petitioner and Patent Owner rely on the same arguments and evidence discussed above in subsections D(4)(b)(1) and (2) as to whether a person having ordinary skill in the art would have combined AAPA and Majcherczak. *Compare* Pet. 45; PO Resp. 20–31; Pet. Reply 2–12; PO Sur-reply 2–19, *with* 1316 Pet. 53; 1316 PO Resp. 20–31; 1316 Pet. Reply 2–12; 1316 PO Sur-reply 2–19.

For the reasons discussed above in subsection D(4)(b)(3), Petitioner provided "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See Kahn*, 441 F.3d at 988.

Accordingly, having considered the entirety of the evidence submitted by the parties, both for and against obviousness, we determine that Petitioner has shown by a preponderance of the evidence that claims 8 and 17 of the '674 patent would have been obvious over the combined teachings of AAPA and Majcherczak.

7. Claims 9, 12, 13, 16, and 18–21

Claims 9, 12, 13, and 18–21 depend, directly or indirectly, from claim 8 or 17. Ex. 1001, 10:4–10, 10:34–52, 11:7–13. 12:6–30.

Claims 9 and 13 recite "wherein said [decreasing/increasing] said current capacity comprises: receiving a first feedback signal from said signal processor at one or more first feedback transistors coupled in parallel with said one or more first transistors; and switching [off/on] said one or more first feedback transistors in response to said first feedback signal." Ex. 1001, 10:4–10, 10:45–51. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claims 9 and 13. 1316 Pet. 63–65; *see also* Ex. 1003 ¶¶ 142, 145 (Horst Decl.).

Claim 12 recites

> wherein said detecting said power-down comprises:
>
> > receiving a logic-low signal at said control gate of said one or more first and second transistors, wherein said one or more first transistors are configured to switch on in response to said logic-low signal, and wherein said one or more second transistors are configured to switch off in response to said logic-low signal; and
> >
> > transmitting a detection signal to a signal processor from said one or more first transistors based on said received logic-low signal.

Ex. 1001, 10:33–44. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitations recited in claim 12. 1316 Pet. 66–68; *see also* Ex. 1003 ¶¶ 141, 144–146 (Horst Decl.).

Claim 18 recites a "means for providing a feedback signal associated with at least one of: said detected power-on or said detected power-down, wherein said feedback signal is used in said means for decreasing and said means for increasing." Ex. 1001, 12:6–10. Petitioner argues that the

combination of AAPA and Majcherczak teaches the additional limitation recited in claim 18. 1316 Pet. 68–70; *see also* Ex. 1003 ¶¶ 141, 145, 146 (Horst Decl.).

Claims 19 and 20 recite "wherein said means for [decreasing/increasing] said current capacity comprises: means, responsive to said feedback signal, for switching [off/on] one or more transistors of a plurality of transistors, wherein said plurality of transistors define said current capacity of said power on/off detector." Ex. 1001, 12:11–22. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claims 19 and 20. 1316 Pet. 70–72; *see* Ex. 1003 ¶¶ 141–143, 145, 146 (Horst Decl.).

Claim 21 recites that "the device is integrated into a semiconductor die." Ex. 1001, 12:23–24. Petitioner argues that the combination of AAPA and Majcherczak teaches the additional limitation recited in claim 21. 1316 Pet. 73; *see also* Ex. 1003 ¶¶ 124, 125 (Horst Decl.).

Patent Owner does not separately address the additional limitations recited in claims 9, 12, 13, 16, and 18–21. *See generally* 1316 PO Resp.

Having considered the entirety of the evidence submitted by both parties, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 9, 12, 13, 16, and 18–21 of the '674 patent would have been obvious to a person having ordinary skill in the art based on the combined teachings of AAPA and Majcherczak.

E. Obviousness over AAPA, Majcherczak, and Matthews

1. Overview of Matthews

Matthews is titled "Apparatus for Power-on Disable in a Multiple Power Supply System and a Method Therefor" and is directed "to a system

such as an embedded system that has multiple power supplies that are synchronized during initialization of the system." Ex. 1009, code (54), 1:9–12. More specifically, Matthews teaches an apparatus "for disabling portions of a system, circuit, etc. having multiple power supplies," which provides the advantages of disabling "certain portions of a system" "during system power-on or other times when power supply voltage levels may be changing," in order to prevent those portions "from generating erroneous data." *Id*. at 1:63–2:10.

2. Claim 7, 16 and 22

Claim 7 depends from claim 6 and recites that "the semiconductor die is incorporated in a device selected from a group consisting of a mobile phone, personal data assistant (PDA), navigation device, fixed location data unit, set-top box, music player, video player, entertainment unit, and computer." Ex. 1001, 9:42–47. Claims 16 and 22 recite a substantially similar limitation. *See id.* at 11:7–13, 12:25–30.

Petitioner argues Matthews teaches the additional limitation recited in claims 7, 16, and 22. *See* Pet. 62–64; 1316 Pet. 74–76; *see also* Ex. 1003 ¶¶ 152–155. Specifically, Petitioner argues Matthews teaches that the system in which its "power-on disable module is integrated 'may be a wireless communication device [e.g., a mobile phone] or a system board or component thereof, or a computer system, a system board or peripheral device thereof." Pet. 63 (quoting Ex. 1009, 5:35–37); 1316 Pet. 75 (quoting Ex. 1009, 5:35–37) (emphasis in original). Petitioner further argues that a person having ordinary skill in the art "would have found it obvious to utilize the POC system 10 described in the AAPA to be used in 'wireless communication device [e.g., a mobile phone] or a system board or

component thereof, or a computer system, a system board or peripheral device thereof.'" Pet. 63–64 (quoting Ex. 1003 ¶ 155); 1316 Pet. 76 (quoting Ex. 1003 ¶ 155).

Patent Owner does not separately address the additional limitations recited in claims 7, 16, and 22. *See generally* PO Resp.; 1316 PO Resp. Instead, Patent Owner argues that "the addition of Matthews does not remedy any of the deficiencies noted above for the combination of the alleged AAPA and Majcherczak (Ground 2a), and Petitioner's obviousness argument as to claim 7 fails for the same reasons that its arguments for claims 1, 2, 5, and 6 fail." PO Resp. 31; *see also* 1316 PO Resp. 32 (for claims 16 and 22).

Patent Owner's arguments about AAPA and Majcherczak are not persuasive for the reasons given above. We are persuaded by Petitioner's analysis of the evidence cited in the Petition and find Petitioner has shown that the combination of AAPA, Majcherczak, and Matthews teaches the additional limitation recited in claims 7, 16, and 22. Additionally, for the reasons given in the Petition, we are also persuaded by Petitioner's arguments that a person having ordinary skill in the art would have combined the teachings of Matthews with the teachings of AAPA and Majcherczak and that there would have been a reasonable expectation of success.

Having considered the entirety of the evidence submitted by both parties, we determine that Petitioner has demonstrated by a preponderance of the evidence that claims 7, 16, and 22 of the '674 patent would have been obvious to a person of ordinary skill in the art based on the combined teachings of AAPA, Majcherczak, and Matthews.

III. CONCLUSION[23]

For the foregoing reasons, and taking into account the Federal Circuit's decision, we conclude that Petitioner has demonstrated by a preponderance of the evidence the unpatentability of claims 1, 2, 5–9, 12, 13, and 16–22 of the '674 patent. Specifically, Petitioner has demonstrated by a preponderance of the evidence that (1) claims 1, 2, 5, 6, 8, 9, 12, 13, and 17–21 would have been obvious under 35 U.S.C. § 103 in light of AAPA and Majcherczak and (2) claims 7, 16, and 22 would have been obvious under 35 U.S.C. § 103 in light of AAPA, Majcherczak, and Matthews.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1, 2, 5–9, 12, 13, and 16–22 of the '674 patent are held unpatentable; and

FURTHER ORDERED that because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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[23] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

IPR2018-01315

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 2, 5–7	103(a)	Steinacker, Doyle, Park[24]		
1, 2, 5, 6	103(a)	AAPA, Majcherczak	1, 2, 5, 6	
7	103(a)	AAPA, Majcherczak, Matthews	7	
Overall Outcome			1, 2, 5–7	

IPR2018-01316

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
8, 9, 12, 13, 16–22	103(a)	Steinacker, Doyle, Park[25]		
8, 9, 12, 13, 17–21	103(a)	AAPA, Majcherczak	8, 9, 12, 13, 17–21	
16, 22	103(a)	AAPA, Majcherczak, Matthews	16, 22	
Overall Outcome			8, 9, 12, 13, 16–22	

[24] Because this ground was not subject to the remand, we do not address it in this Decision.

[25] Because this ground was not subject to the remand, we do not address it in this Decision.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01315, IPR2018-01316
Patent 8,063,674 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*, concurring.

I agree with the majority that the challenged claims are unpatentable, and I join with all of the majority decision except for the discussion in Section II.D.3, which I join in part. In particular, I join Section II.D.3.a and the first two paragraphs of Section II.D.3.d. As the second paragraph of Section II.D.3.d states, the answer to the question we must decide on remand is found in the Director's Updated Guidance. Therefore, the remaining discussion in Section II.D.3 is unnecessary in my view, and I express no opinion on it.

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