UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-01283
U.S. Patent No. 11,342,998 B2

PETITIONER'S NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

via P-TACTS
Patent Trial and Appeal Board

via Email
Director of the United States Patent and Trademark Office
efileSO@uspto.gov

via CM/ECF
United States Court of Appeals for the Federal Circuit

Pursuant to 28 U.S.C. § 1295(a)(4)(A), 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a), 90.3, 5 U.S.C. §§ 701–706, and Federal Circuit Rule 15(a)(1), Petitioner Cisco Systems, Inc. ("Petitioner") provides notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered February 20, 2024 (Paper 32) and from all underlying and related orders, decisions, rulings, and opinions regarding U.S. Patent No. 11,342,998 B2 ("the '998 patent") in *Inter Partes* Review IPR2022-01283.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), the expected issues on appeal include, but are not limited to: the Board's error(s) in determining that Petitioner has failed to demonstrate that challenged claims 1–63 of the '998 patent are unpatentable, and any finding or determination supporting or related to that determination, as well as all other issues decided adversely to Petitioner in any orders, decisions, rulings, or opinions in *Inter Partes* Review IPR2022-01283.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the United States Patent and Trademark Office and with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF.

Respectfully submitted,

Dated: April 22, 2024

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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PTAB P-TACTS, a true and correct copy of the above-captioned PETITIONER'S NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT is being filed by email with the Director on April 22, 2024, at efileSO@uspto.gov.

The undersigned also hereby certifies that a true and correct copy of the above-captioned PETITIONER'S NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on April 22, 2024.

Respectfully submitted,

Dated: April 22, 2024

/Theodore M. Foster/
Theodore M. Foster
Counsel for Petitioner
Registration No. 57,456

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, this is to certify that a true and correct copy of the foregoing "Petitioner's Notice of Appeal to the United States Court of Appeals for the Federal Circuit" was served on counsel for Patent Owner Ramot At Tel Aviv University Ltd. as detailed below:

Date of service	April 22, 2024
Manner of service	Email: bentzminger@bdiplaw.com cjohanningmeier@bdiplaw.com BDIP_RamotIPRService@bdiplaw.com
Documents served	**Petitioner's Notice of Appeal to the United States Court of Appeals for the Federal Circuit**
Persons served	Brenda Entzminger Corey Johanningmeier (Pro Hac Vice) Bunsow De Mory LLP 701 El Camino Real Redwood City, CA 94063

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Paper 32
Date: February 20, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-01283
Patent 11,342,998 B2

Before MONICA S. ULLAGADDI, CHRISTOPHER L. OGDEN, and JASON M. REPKO, *Administrative Patent Judges.*

Opinion for the Board filed by Administrative Patent Judge ULLAGADDI

Opinion concurring filed by Administrative Patent Judge OGDEN

ULLAGADDI, *Administrative Patent Judge*.

JUDGEMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
Dismissing Patent Owner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

Cisco Systems, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 1–63 ("the challenged claims") of U.S. Patent No. 11,342,998 B2 (Ex. 1001, "the '998 patent"), accompanied by the supporting Declaration of Dr. Daniel J. Blumenthal (Ex. 1003). The assignee of the '998 patent, Ramot at Tel Aviv University Ltd. ("Patent Owner"), filed a Preliminary Response (Paper 7), accompanied by the supporting Declaration of Dr. John Dallesasse (Ex. 2005). With our authorization, Petitioner filed a pre-institution Reply (Paper 10) and Patent Owner filed a Sur-Reply (Paper 11).

Upon review of the preliminary record, we instituted *inter partes* review, pursuant to 35 U.S.C. § 314, as to the challenged claims based on the challenges set forth in the Petition. Paper 12 ("Institution Decision" or "Inst. Dec.").

Patent Owner filed a Response (Paper 16, "Patent Owner's Response" or "PO Resp.") accompanied by the supporting Declaration of Dr. John Dallesasse (Ex. 2022), Petitioner filed a Reply to Patent Owner's Response (Paper 18, "Petitioner's Reply" or "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 21, "Patent Owner's Sur-Reply" or "PO Sur-Reply").

On November 22, 2023, we held an oral hearing. A transcript of the hearing is of record. Paper 31 ("Tr.").

For the reasons that follow, we conclude that Petitioner has not established, by a preponderance of the evidence, that the challenged claims of the '998 patent are unpatentable.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies Cisco Systems, Inc. and its subsidiary, Acacia Communications, Inc. as the real parties-in-interest. Pet. 88.

Patent Owner identifies Ramot at Tel Aviv University Ltd. as the real party-in-interest. Paper 3, 2.

B. Related Matters

The parties indicate that the '998 patent is involved in the following district court cases: *Cisco Systems, Inc. et al. v. Ramot at Tel Aviv University Ltd.*, Case No. 1-21-cv-00674 (D. Del.) and *Ramot at Tel Aviv University Ltd. v. Cisco Systems, Inc.*, Case No. 2-22-cv-00168 (E.D. Tex.). Pet. 88; Paper 4, 2.

The parties further indicate that the '998 patent is also related to four patents that were/are the subject of the following administrative proceedings:

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2020-00122 (PTAB) (institution denied);

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2020-00123 (PTAB) (institution denied);

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2020-00484 (PTAB) (institution denied);

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2022-00575 (PTAB) (final written decision entered);

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2022-00576 (PTAB) (final written decision entered) ("the '576 FWD");

Ex Parte Reexamination, Control No. 90/014,526, merged with 90/014,608 (reexamination certificate issued);

Ex Parte Reexamination, Control No. 90/014,527, merged with 90/014,606 (reexamination certificate issued); and

Ex Parte Reexamination, Control No. 90/014,528, merged with 90/014,607 and 90/014,728 (reexamination certificate issued)

Pet. 88–89; Paper 4, 2–3.

Patent Owner further indicates that the '998 patent is also related to three patents that are the subject of the following district court proceedings:

Ramot at Tel Aviv University Ltd. v. Cisco Systems, Inc., 2:19-cv-00225 (E.D. Tex.) (pending);

Ramot at Tel Aviv University Ltd. v. Acacia Communications, Inc., 1:21-CV-00295 (D. Del.) (pending); and

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., 1:21-cv-01365-(VAC)-CJB (D. Del.) (pending).

Paper 4, 2–3.

C. The '998 Patent

The '998 patent, entitled "Linearized Optical Digital-to-Analog Modulator," issued May 24, 2022 and claims priority to provisional application No. 60/943,559, filed June 13, 2007. Ex. 1001, codes (45), (54), (60). The '998 patent discloses a system for converting digital data into a modulated optical signal, where an electrically controllable device having M actuating electrodes provides an optical signal that is modulated in response to binary voltages applied to the actuating electrodes. *Id.* at code (57). A digital-to-digital converter provides a mapping of input data words of N bits to binary actuation vectors of M bits and supplies the binary actuation vectors as M bits of binary actuation voltages to the M actuating electrodes, where M is larger than the number of bits in each input data word. *Id.* The digital-to-digital converter maps each digital input data word to a binary

actuation vector by selecting a binary actuation vector from a subset of binary actuation vectors available to represent each of the input data words. *Id.* at code (57). Referring to FIG. 1, reproduced below, the '998 patent discloses modulator device 10 that has electronic input 12 for receiving input data word D of N bits and electrically controllable modulator 14 for modulating the intensity of an optical signal represented by arrow 16. Ex. 1001, 7:17–21.

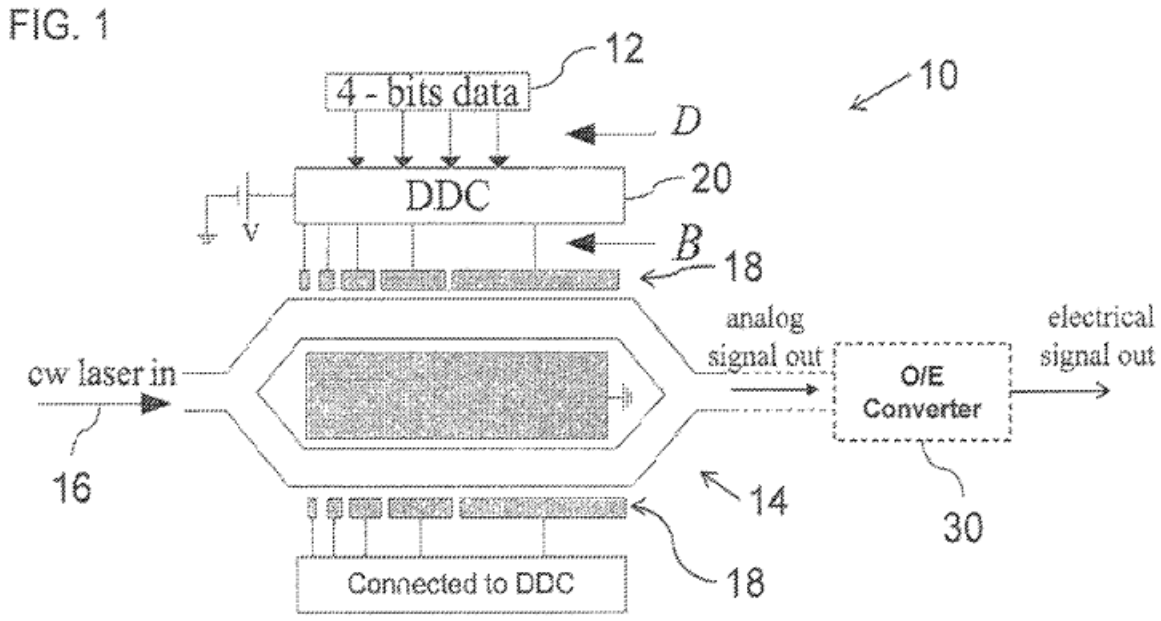


Figure 1 of the '998 patent is a schematic representation of a modulator device for converting digital data into analog modulation of an optical or electrical signal.

Modulator 14 includes M actuating electrodes 18 where M≥N. *Id.* at 7:21–22. Modulator device 10 also includes an electrode actuating device 20 responsive to the input data word D to supply an actuating voltage to the actuating electrodes 18. *Id.* at 7:22–25. Thus, electrode actuating device 20 actuates at least one of actuating electrodes 18 as a function of values of more than one bit of the input data word D. *Id.* at 7:26–29. In other words, at least one of the electrodes is actuated in a manner differing from a simple

one-to-one mapping of data bits to electrode voltage, thereby providing freedom to choose the electrode actuation pattern which best approximates a desired ideal output for the given input. *Id.* at 7:29–33.

D. Illustrative Claim

Of challenged claims 1–63, claims 1, 16, 32, 45, and 58 are independent. For purposes of the issues raised at this stage of the proceeding, claim 1 is illustrative and is reproduced below.

> 1. An optical modulation system, the system comprising:
>
> an input for a plurality of N digital input data bits;
>
> an input optical signal;
>
> a modulator for modulating the input optical signal responsively to the plurality of N digital input data bits to output a modulation of the input optical signal, thereby generating one or more modulated optical signal outputs for transmission over one or more optical fibers; and
>
> wherein a digital-to-digital mapping maps the plurality of N digital input data bits to a set of M digital output data bits associated with a plurality of voltage values;
>
> wherein the input optical signal is modulated based on the plurality of voltage values;
>
> wherein the digital-to-digital mapping comprises, for each digital input value included in a set of possible digital input values for the plurality of N digital input data bits, a set of corresponding digital output values from a set of possible digital output values;
>
> wherein, within the digital-to-digital mapping, for a first subset of successively increasing digital input values specified in the digital-to-digital mapping, deltas between numerical values of successive digital outputs in the set of digital output values corresponding respectively to the successively increasing digital input values in the first subset, decrease; and

> wherein, within the digital-to-digital mapping, for a second subset of successively increasing digital input values specified in the digital-to-digital mapping, deltas between numerical values of successive digital outputs in the set of digital output values corresponding respectively to the successively increasing digital input values in the second subset, increase.

Ex. 1001, 17:23–55.

E. Asserted Grounds

Petitioner presents the following challenges as summarized in the chart below. Pet. 17. Petitioner supports its challenges with the Declaration of Dr. Daniel J. Blumenthal. Ex. 1003.

Claims Challenged	35 U.S.C. §	References
1–63	103(a)[1]	Roberts[2], Taraschuk[3]
1–63	103(a)	Roberts, Taraschuk, Wright[4]

III. ANALYSIS

A. Legal Standards

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the effective filing date of the challenged claims. The earliest possible filing date is June 13, 2007. Ex. 1001, code (60). Therefore, we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103(a).
[2] U.S. Patent No. 7,277,603 B1, filed February 22, 2006 and issued October 2, 2007, to Roberts et al. (Ex. 1005, "Roberts").
[3] U.S. Patent No. 6,781,537 B1, issued August 24, 2004, to Taraschuk et al. (Ex. 1006, "Taraschuk").
[4] U.S. Patent No. 7,058,369 Bl, issued June 6, 2006, to Wright et al. (Ex. 1009, "Wright").

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective indicia of obviousness or nonobviousness.[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). According to Petitioner,

> [a] Person of Ordinary Skill in The Art ("POSITA") in June of 2007 would have had a working knowledge of optical modulators and modulation schemes. A POSITA would have had a master's degree in electrical engineering, or an equivalent, and two years of professional experience relating to optical communications, and in particular, optical signal modulation. Lack of professional experience can be remedied by additional education, and vice versa.

Pet. 9–10 (citing Ex. 1003 ¶¶ 21–23). According to Patent Owner,

> a person of ordinary skill in the art as of the effective priority date in 2007 would have had a Master of Science Degree in Electrical Engineering, or Electrical and Computer Engineering, and at least two years of academic or professional experience in

[5] Patent Owner does not present objective evidence of nonobviousness.

> engineering, specifically in the analysis and design of optoelectronic systems for optical communications.

PO. Resp. 27 (citing Ex. 2022 ¶¶ 22–26).

We do not discern a substantial difference between the parties' definitions for the level of ordinary skill in the art. Instead, we determine that the parties' definitions are substantially similar. We adopt Petitioner's definition of the level of skill in the art, which is consistent with the disclosure of the '998 patent and asserted prior art of record. The findings and conclusions rendered in this Decision would not change under either definition.

C. Claim Construction

In *inter partes* review proceedings based on petitions filed on or after November 13, 2018, such as this one, we construe claims using the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. *See* 37 C.F.R. § 42.100(b).

Petitioner contends the Petition "analyzes the claims consistent with their ordinary and customary meaning as would be understood by a [person of ordinary skill in the art] in light of the specification." Pet. 10. According to Petitioner, the '998 patent explicitly defines the terms "digital," "digital-to-digital mapping," and "modulator," but argues that "regardless of whether these express definitions are read into the claims, the [cited art] teaches the limitations recited in the claims." *Id*. (citing Ex. 1003 ¶¶ 93–97).

Patent Owner contends construction of the aforementioned terms is "not necessary to the resolution of any issues presented in the Petition." Prelim. Resp. 44. As contended by Patent Owner, "[t]he Board did not need to and did not address claim construction in dismissing Cisco's three prior

IPRs challenging related patents with shared specifications." *Id.* at 43–44 (citing Ex. 2004).

We need not construe any claim term to resolve the issues before us, and therefore, do not expressly define any claim term in our Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (explaining that construction is needed only for terms that are in dispute, and only as necessary to resolve the controversy).

D. Obviousness over Roberts, Taraschuk, and Wright

Petitioner argues that claims 1–63 would have been obvious in view of Roberts, Taraschuk, and Wright. Pet. 85–86. Patent Owner disagrees. *See generally* PO Resp.

Petitioner's first challenge "presents the combination of Roberts and Taraschuk as teaching the claimed limitations in light of the background knowledge" of a person of ordinary skill in the art, as "evidenced by Wright." Pet. 85. For example, Wright allegedly "provides an example of a 'known manner' for determining the values for a nonlinear compensation look-up table. *Id*. But "[t]o the extent Patent Owner argues that calculating such look-up table values would not have been within the background knowledge," Petitioner's second challenge "is presented to show that calculating such values would have been obvious to a [person of ordinary skill], as evidenced by Wright." Ex. 1003 ¶ 349.

Petitioner's challenge applying Roberts, Taraschuk, and Wright refers, in large part, back to its analysis in the challenge applying Roberts and Taraschuk. As such, we refer to Petitioner's challenge applying Roberts and Taraschuk for the element-by-element analysis of the claims. Pet. 27–85.

1. Overview of Roberts

Roberts is entitled "Integrated Optical Waveform Modulation." Ex. 1005, code (54). Roberts discloses a method of modulating an optical carrier. *Id.* at code (57). A target carrier modulation is computed based on an input data signal. *Id.* An effective length of an optical modulator is then controlled based on the target carrier modulation. *Id.* Figure 4 of Roberts, reproduced below, depicts principal components and operation of a complex optical synthesizer.

Figure 4

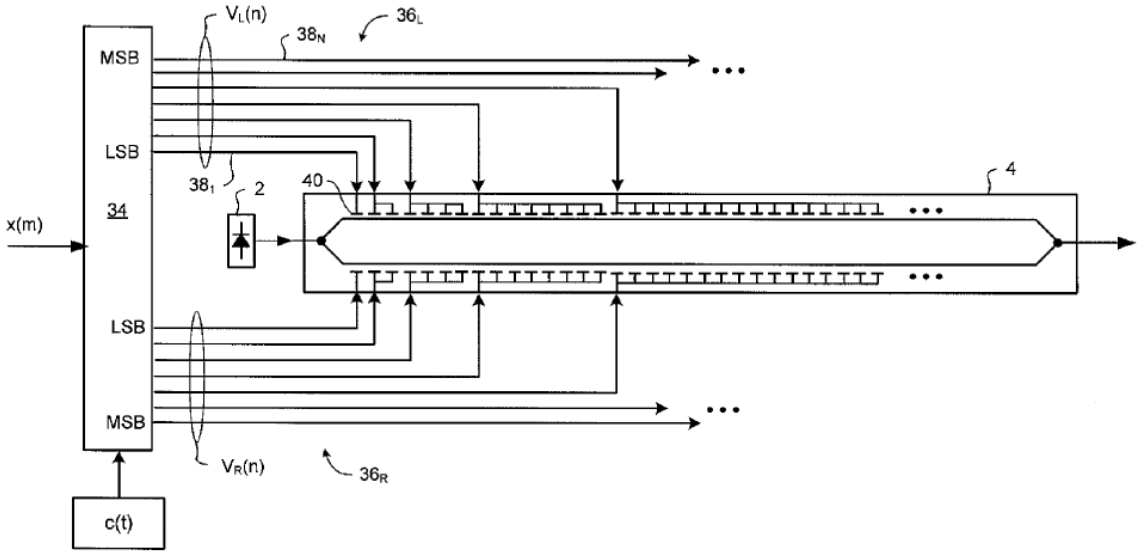


Figure 4 of Roberts depicts "principal components and operation of a complex optical synthesizer." *Id.* at 5:20–21, Fig. 4.

In general, the optical modulator operates by computing a target carrier modulation, and then varying the effective length of the control region of the optical modulator in accordance with the target modulation. *Id.* at 5:47–50. The electrodes of the modulator are configured such that the drive signals are the binary logic states output by the driver IC with no

signal conditioning or power amplification required between the driver IC and the optical modulator. *Id.* at 5:50–54.

As illustrated in Figure 4, the driver IC is implemented as a digital signal processor (DSP) 34, which generates a pair of multi-bit sample streams $V_X(n)$ which are representative of the desired phase modulation to be applied to each branch of an MZ modulator 4. *Id.* at 5:56–60. Each multi-bit sample stream $V_X(n)$ may be an N-bit parallel binary signal output from the DSP 34 on a corresponding N-bit data bus 36. *Id.* at 6:40–42. In such a case, each line 38_i of the N-bit bus 36 is connected to control a number of electrodes 40 corresponding to its binary weight. *Id.* at 6:42–44.

2. Overview of Taraschuk

Taraschuk is entitled "High Speed Digital to Analog Converter." Ex. 1006, code (54). Taraschuk discloses a high-speed D/A converter that includes a phase aligner and a vector summation block (*i.e.*, vector addition block). *Id.* at code (57). The phase aligner operates to ensure precise phase alignment between corresponding bits of a parallel N-bit digital signal having a data rate of at least 2 GHz. *Id.* The vector addition block performs a vector addition of the phase-aligned bits of the parallel N-bit digital signal. *Id.* Figure 5 of Taraschuk, reproduced below, depicts principal elements in a high-speed digital-to-analog converter.

Figure 5

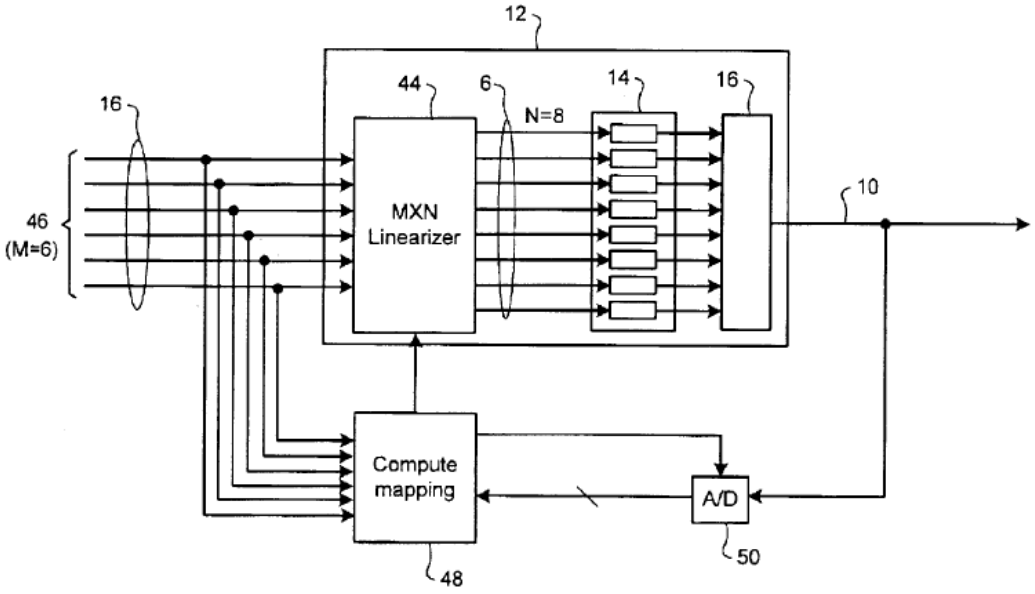


Figure 5 of Taraschuk depicts "principal elements in a high-speed digital-to-analog converter." *Id.* at 3:16–17, Fig. 5.

Figure 5 illustrates an M=6-bit D/A converter 12 having a linearizer 44 connected upstream of the phase aligner 14 and vector addition blocks 16. *Id.* at 6:58–61. The linearizer 44 is designed to map an M-bit digital signal into an N-bit parallel digital signal 6 for processing by the phase aligner 14 and vector summation block 16. *Id.* at 6:61–65. In general, the number (M) of bits of the input digital signal 46 will be less than the number (N) of bits of the parallel digital signal 6 processed by the phase aligner 14 and vector summation block 16. *Id.* at 6:65–7:1.

Figure 5 further illustrates a system for periodically re-calculating the mapping implemented in the linearizer 44. *Id.* at 7:23–25. "[T]he M-bit digital signal 46 is tapped and provided to a signal processor 48." *Id.* at 7:26–27. "The analog output signal (S) is sampled by an analog-to-digital converter 50 and supplied to the signal processor 48." *Id.* at 7:27–29. "By

controlling the timing of the sample detected by the analog-to-digital converter 50, the signal processor 48 can receive an M-bit word of the input digital signal 46 and obtain a sample of the corresponding analog signal level (S) generated by the D/A converter 12 based on that M-bit word." *Id.* at 7:29–34. "By calculating a difference between the received M-bit word and the sampled analog output signal level (S), the signal processor 48 can readily compute a mapping between the received M-bit word of the input digital signal 46 and an N-bit word required to obtain the desired output analog signal level." *Id.* at 7:34–39.

3. Overview of Wright

Wright is entitled "Constant Gain Digital Predistortion Controller for Linearization of Non-Linear Amplifiers." Ex. 1009, code (54). Wright discloses methods and an apparatus for controlling and adapting a digital predistortion linearizer for amplification of bandlimited signals using non-linear amplifiers. *Id.* at code (57). The control method permits the predistortion function applied by a predistortion entity to provide a relatively constant gain. *Id.* Figure 6A, reproduced below, depicts input versus output response curves.

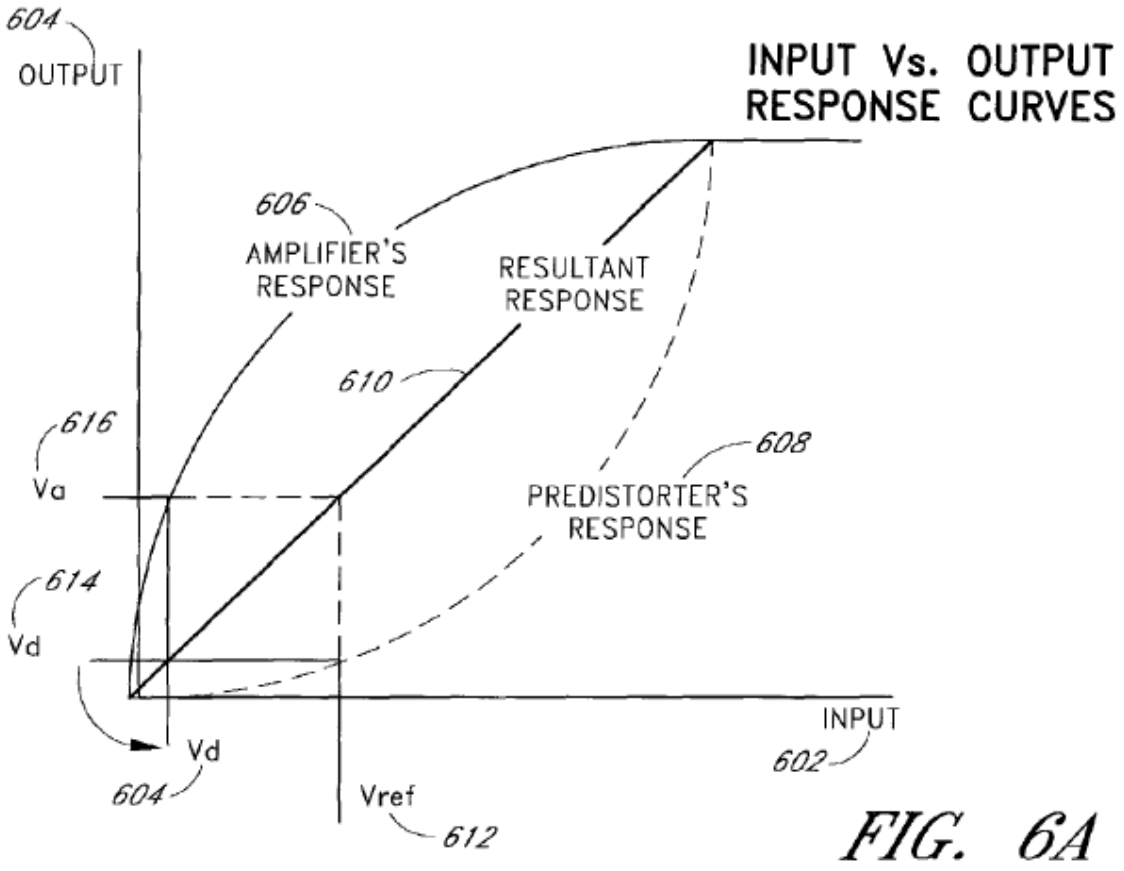


FIG. 6A

Figure 6A of Wright depicts "a chart of input vs. output response curves." Ex. 1009, 13:9–10, Fig. 6A.

As depicted in Figure 6A, an input magnitude 602 is indicated along a horizontal axis, where the "input" in Figure 6A corresponds to the input of a predistorter, as well as to the input to a power amplifier. *Id.* at 13:10–14. As also depicted in Figure 6A, an output magnitude 604 is indicated along a vertical axis, where the "output" in Figure 6A corresponds to the output of the predistorter, as well as to the output of the power amplifier. *Id.* at 13:14–17. Figure 6A illustrates a convex amplifier response 606, which eventually reaches a saturated value, where no additional output power can be supplied/generated by the amplifier irrespective of how hard the input signal level is driven. *Id.* at 13:17–22. "The . . . diagram also illustrates how

a cascade of a concave predistortion response 608 can result in an overall linear response 610. *Id.* at 13:22–24.

As further depicted in Figure 6A, "an input reference signal V_{ref} 612 is mapped by the concave predistortion response 608 to a significantly lower level predistortion signal V_d 614." *Id.* at 13:26–29. "The signal level of the input reference signal V_{ref} 612 is mapped by the concave predistortion response 608 to a value shown by the vertical axis of Figure 6A." *Id.* at 13:29–32. "The predistortion signal V_d 614 is then applied as an input to the amplifier as represented by the convex amplifier response 606, which transfers to an output level V_a 616." *Id.* at 13:32–35. "This output level V_a 616 is approximately identical to that provided by a pure linear response driven with the original input reference signal V_{ref} 612. *Id.*" at 13:35–37.

4. Independent Claim 1

[1.0] "An optical modulation system, the system comprising:"

Petitioner contends that, "[t]o the extent the preamble is limiting, Roberts renders it obvious" because "Roberts teaches optical waveform modulation for optical communication systems." Pet. 27–28.

[1.1] "an input for a plurality of N digital input data bits,"

Petitioner contends that, "[f]irst, Roberts teaches a digital signal processor (DSP) with an "input" that receives an "input digital data signal x(m)." Pet. 28 (citing Ex. 1005, 1:32–33, Fig. 4; Ex. 1003 ¶¶ 124–125) (emphasis omitted). Petitioner further contends that it would have been "obvious for Roberts' input data signal x(m) to include '*a plurality of N digital input data bits*' as claimed" because Roberts' x(m) signal "is used to 'generate[] a pair of multi-bit sample streams V(n) which are representative of the desired phase modulation to be applied to each branch of an MZ modulator 4,'" which "suggests that the x(m) signal is a plurality of data

bits." *Id.* at 29 (citing Ex. 1005, 6:57–59; Ex. 1003 ¶ 127). Petitioner further contends that "Roberts describes the x(m) signal as providing 'input data'" and "[b]ecause 'data' is the plural form of 'datum,' a [person of ordinary skill in the art] would have understood x(m) to include a plurality of bits." *Id.* (citing Ex. 1005, 1:58–59; Ex. 1003 ¶ 127). According to Petitioner, when implementing "a non-linear compensation function as taught by Taraschuk," it would have been obvious for the DSP to include a plurality of input bits as "explicitly taught by Taraschuk," and "Taraschuk's input digital signal is a 6-bit signal." *Id.* at 29–30 (citing Ex. 1006, 6:56–7:4).

Petitioner contends that because "Roberts teaches that the DSP includes a 'non-linear compensator 18' that, like Taraschuk's linearizer, is used to compensate for non-linearities of a Mach-Zehnder optical modulator," it would have been "obvious for Roberts' DSP to receive a 6-bit digital input signal as taught by Taraschuk." *Id.* at 31 (citing Ex. 1005, 6:34–37; Ex. 1006, 6:56–58, 7:59–67; Ex. 1003 ¶ 130).

[1.2] "an input optical signal"

Petitioner contends that Roberts describes "a laser 2 coupled to an external optical modulator 4" that generates an optical carrier signal to the modulator." Pet. 31 (citing Ex. 1005, 1:24–30, Fig. 4).

[1.3] "a modulator for modulating the input optical signal responsively to the plurality of N digital input data bits to output a modulation of the input optical signal;"

Petitioner contends that Roberts teaches a Mach-Zehnder modulator 4 that operates to "modulate the amplitude and/or phase [of] the carrier signal" from laser 2 (an input optical signal), as shown in Figure 4. Pet. 32–33 (citing Ex. 1005, 1:26–30, 5:56–60, Fig. 4). Roberts also allegedly "teaches that the output signal is modulated responsive to the x(m) signal," which is a

plurality of N digital input data bits. *Id.* at 33 (citing Ex. 1005, 1:32–33, Fig. 4). And Petitioner argues that a person of ordinary skill in the art "would have recognized that modulating the amplitude and/or phase of the optical carrier signal as taught by Roberts would effect a modulation of the input optical signal," and thus output a modulation of the input optical signal, because it was well-known that "inputting an optical signal into an optical modulator would output a modulated optical signal." *Id*. at 34–35 (citing Ex. 1003 ¶ 140). Based on this analysis, Petitioner contends that this claim limitation would have been obvious. *Id*. at 35 (citing Ex. 1003 ¶¶ 135–42).

[1.4] "generating one or more modulated optical signal outputs for transmission over one or more optical fibers"

Petitioner contends that Roberts teaches that modulation by the optical modulator "generate[s] the optical communications signal," and that Figure 4 shows "optical communications signal being transmitted from the optical modulator." Pet. 35–36 (citing Ex.1005, 1:26–30, Fig. 4). According to Petitioner, a person of ordinary skill "would have found it obvious to transmit Roberts' output optical communications signal over an optical fiber because . . . optical fibers had long been used to communicate optical signals." *Id.* at 36 (citing Ex. 1003 ¶ 145; Ex. 1011).

[1.5] "wherein a digital-to-digital mapping maps the plurality of N digital input data bits to a set of M digital output data bits associated with a plurality of voltage values,"

Petitioner contends that:

> **First**, Taraschuk describes a linearizer (which may be implemented within Roberts' DSP) that maps ("*digital-to-digital mapping*") a 6-bit digital input signal ("*maps the plurality of N digital input data bits*") to an 8-bit digital output signal ("*to a set of M digital output data bits*"). "**The linearizer 44** is designed in

> a known manner (e.g., using a random access memory look-up table) **to map an M-bit digital signal 46 into an N-bit parallel digital signal 6 … M=6 and N=8**."
>
> Taraschuk describes both the 6-bit and 8-bit signals as "digital" signals. A POSITA would have therefore recognized that the mapping between the input and output signals is a digital-to-digital mapping. Fig. 5 of Taraschuk illustrates that the linearizer outputs the 8-bit digital signal. Accordingly, a POSITA would have recognized that the 6-bit digital input signal is converted into the 8-bit digital output signal based on the mapping.
>
> . . .
>
> **Second**, Roberts teaches that the DSP outputs VR(n) and VL(n) signals (generally referred to as VX(n)) and explains that the bits of such signals are representative of voltages to be applied to respective electrodes: "Each multi-bit sample stream VX(n) may be an N-bit parallel binary signal output from the DSP 34 on a corresponding N-bit data bus 36. In such a case, each line 38, of the N-bit bus 36 is connected to control a number of electrodes 40 corresponding to its binary weight." "Since each active electrode receives the same voltage (corresponding to logic State 1), it follows that the total phase delay experienced by light traversing each branch will vary directly with the number of active electrodes on that branch, and thus the value of the corresponding multi-bit sample stream VX(n)."
>
> Accordingly, each electrode is provided with a voltage based on the binary values of the VX(n) signal, which is a multi-bit parallel binary signal. The binary values of the VX(n) signal are "*a plurality of voltage values*" because each "1" corresponds to the voltage to be applied to each electrode of the optical modulator.

Pet. 36–40 (citing Ex. 1005, 1:49–52, 6:40–54, 7:35–44; 7:60–65; Ex. 1006, 6:56–7:4; Ex. 1003 ¶¶ 147–55).

> *[1.6] "wherein the input optical signal is modulated based on the plurality of voltage values,"*

Petitioner refers us to its prior analysis, discussed above, that Roberts describes a laser that generates an optical carrier signal that is input to an

optical modulator. Pet. 40 (citing Ex. 1005, 1:24–30, Fig. 4). According to Petitioner, Roberts' DSP outputs "parallel binary signals including binary values," which it contends is a "plurality of voltage values" that are then used to modulate the input optical signal. *Id*. (citing Ex. 1005, 7:39–40, Fig. 4). Petitioner contends that this disclosure renders limitation 1.6 obvious. *Id*. at 41 (citing Ex. 1003 ¶¶ 156–59).

> *[1.7] "wherein the digital-to-digital mapping comprises, for each digital input value included in a set of possible digital input values for the plurality of N digital input data bits, a set of corresponding digital output values from a set of possible digital output values,"*

Petitioner contends that a person of ordinary skill in the art "would have found it obvious for Roberts' DSP to map digital input bits to digital output bits ('*digital-to-digital mapping*') using a look-up table," such as those taught by Taraschuk: "The linearizer 44 is designed in a known manner (e.g., using a random access memory look up table)." Pet. 41 (citing Ex. 1006, 6:61–31; Ex. 1003 ¶ 161). According to Petitioner, the person of ordinary skill would have understood "look-up table" in Taraschuk to refer to "multiple rows and columns of entries, e.g., separate columns for input and output bit words where each column includes a series of entries documenting different combinations of possible bit values." *Id*. at 41–42 (citing Ex. 1003 ¶ 162). Petitioner alleges that a person of ordinary skill in the art would have understood Taraschuk's lookup table to be useful to compensate for a non-linear response of the modulator by permitting "the input to the modulator [to] be adjusted in a complementary non-linear fashion to counteract non-linear response curve of the modulator." *Id*. at 43 (citing Ex. 1008, 12:14–16, Ex. 1003 ¶ 165).

Petitioner points to Wright and contends that it "provides an overview of the basic concepts that were well-understood and generally known by electrical engineers about the operation of non-linear compensation circuits." *Id*. at 43 (citing Ex. 1003 ¶¶ 166–168). Petitioner continues:

> Wright refers to this linearizer as a "predistorter" and explains how the predistorter's response curve is configured to counteract the natural response of the amplifier such that, in tandem, they produce a linear amplifier response to an input voltage. Those of skill in the art were familiar with using a "predistortion lookup table" to store information mapping input and output values for a nonlinear compensation circuit.

Id. at 44 (citing Ex. 1009, 5:27–30; Ex. 1003 ¶ 167). According to Petitioner, "[a] POSITA would have been familiar with the design of non-linear compensation devices and associated lookup tables," which "had long been used in linearizing the output of other nonlinear devices—including RF amplifiers." *Id.* at 44–45 (citing Ex. 1003 ¶ 168).

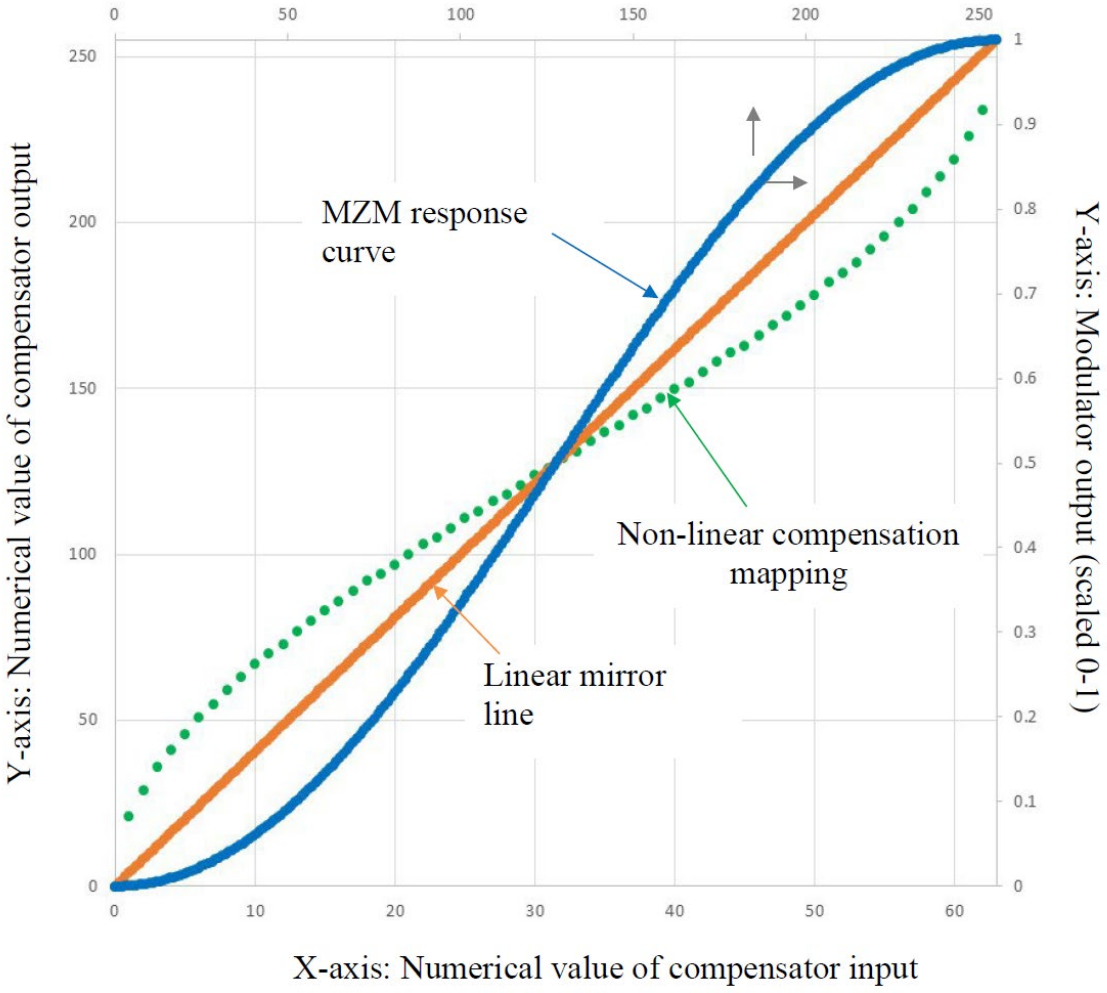
Petitioner cites Dr. Blumenthal's modeling of the natural sinusoidal response curve of an MZM and "calculating [of] a non-linear compensation function to counteract the sinusoidal response curve." *Id.* at 45–46 (citing Ex. 1003 ¶¶ 167–185). According to Petitioner, "Dr. Blumenthal's analysis produces a mapping table based on a generic sinusoidal response curve and Taraschuk's example of a 6-bit to 8-bit linearizer." *Id.* at 46.

According to Petitioner, "[i]t would have been obvious for a POSITA implementing a nonlinear compensation lookup table, as suggested by Taraschuk, to use such known techniques for computing non-linear compensator look-up table values." *Id.* at 47 (citing Ex. 1003 ¶ 186).

> *[1.8] "wherein, within the digital-to-digital mapping, for a first subset of successively increasing digital input values specified in the digital-to-digital mapping, deltas between numerical values of successive digital outputs in the set of digital output values*

corresponding respectively to the successively increasing digital input values in the first subset, decrease;"

Petitioner cites Dr. Blumenthal's graph of "compensator mapping . . . (in green), with compensator input values on the lower horizontal axis, and compensator output values on the left vertical axis." Pet. 48 (citing Ex. 1003 ¶ 190). According to Petitioner "[i]t is immediately apparent that the curve of the compensation mapping appears as a mirror-image of the natural MZM response curve." *Id.* (citing Ex. 1003 ¶ 190). Reproduced below is Dr. Blumenthal's graph of compensator mapping and the natural MZM sinusoidal responsive curve.



Dr. Blumenthal's graph depicting a natural, sinusoidal MZM response curve, as well as input and output values of a non-linear compensation mapping curve. *Id.* at 49 (citing Ex. 1003 ¶ 191).

According to Petitioner, the graph "shows the natural MZM response curve (in blue) using the upper horizontal axis and the right vertical axis." *Id.* at 48 (citing Ex. 1003 ¶ 190).

Petitioner also presents a chart, reproduced below, which is a portion of the mapping table "arranged to show '*increasing*' numerical input values (corresponding to the '*digital input values*')" in which the "final column shows the numerical absolute value difference between successive output values" decreasing. *Id*. at 50 (citing Ex. 1003 ¶ 192).

Numerical value of linearizer 6-bit input	Numerical value of linearizer 8-bit output	Delta
0	0	21
1	21	8
2	29	7
3	36	

Petitioner's chart depicting decreasing delta values between output values mapped with successively increasing input values. *Id*.

Petitioner explains that "Between successive inputs corresponding to the numerical values 0 to 3 ("*first subset*"), the numerical values of the "*deltas . . . decrease*" from 21 to 8 to 7." *Id.* Petitioner contends that "[t]his characteristic is a natural consequence of the nonlinear compensation response curve being a reflection of the MZM sinusoidal response curve across the desired linear output line." *Id.* According to Petitioner, "[i]t would

have been obvious for a POSITA implementing a nonlinear compensation lookup table, as suggested by Taraschuk, to follow a process substantially similar to what is explained" by Dr. Blumenthal, and that "testing an MZM and gathering response curve information was within the ordinary knowledge and skill of engineers" at the time of the invention. *Id.* at 51–52 (citing Ex. 1003 ¶ 195).

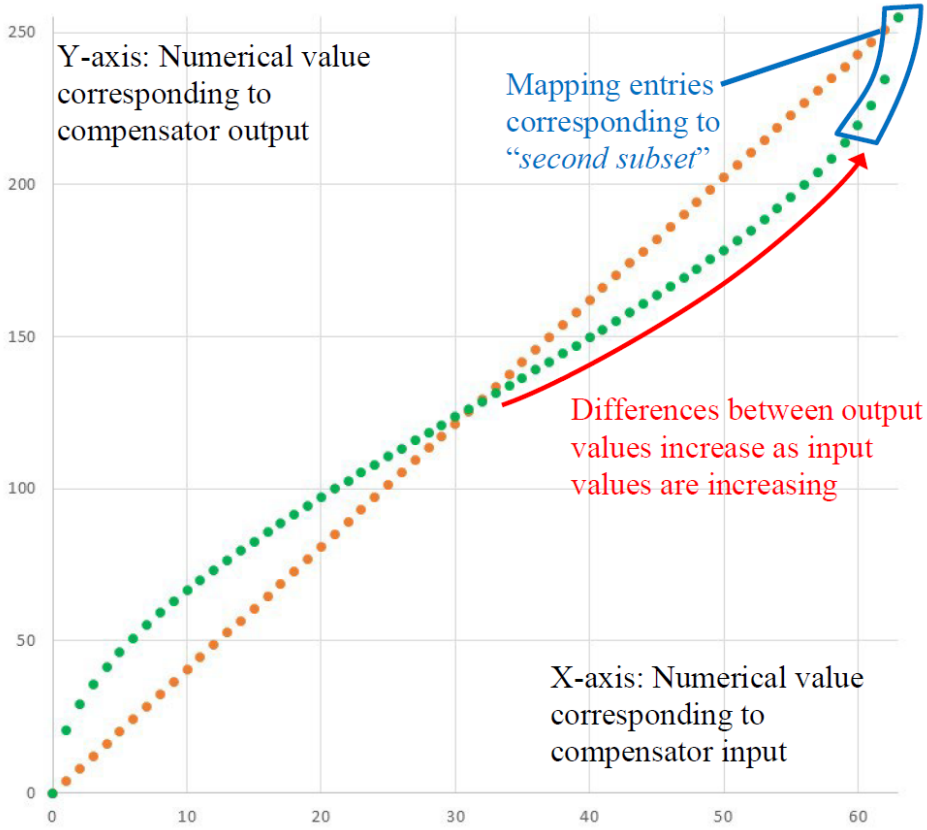
> *[1.9] "wherein, within the digital-to-digital mapping, for a second subset of successively increasing digital input values specified in the digital-to-digital mapping, deltas between numerical values of successive digital outputs in the set of digital output values corresponding respectively to the successively increasing digital input values in the second subset, increase"*

Petitioner contends that "the portion of the mapping table in [1.7] with numerical input values 60 to 63 ('*second subset*') shows that the corresponding deltas between numerical output values increase from 7 to 8 to 21." Pet. 53–54 (citing Ex. 1003 ¶ 199).

Numerical value of linearizer 6-bit input	Numerical value of linearizer 8-bit output	Delta
60	219	7 8 21
61	226	
62	234	
63	255	

Petitioner's chart depicting increasing delta values between output values mapped with successively increasing input values. *Id.*

Petitioner contends that "[t]his increasing delta feature is similarly visible in the response curve of the nonlinear compensation mapping." *Id.* (citing Ex. 1003 ¶ 200).



Dr. Blumenthal's graph depicting non-linear compensator input values that are mapped to output values.
Id. at 55 (citing Ex. 1003 ¶ 200).

Patent Owner's Arguments

With respect to limitations 1.8 and 1.9 (frequently referred to as the "deltas" limitations by the parties), Patent Owner argues that Petitioner "fail[s] to show that Roberts discloses or suggests the 'deltas' mapping elements as disclosed and claimed." PO Resp. 31 (citing Ex. 1001, 17:42–55 (claim 1)). According to Patent Owner, "only Dr. Blumenthal's calculations, allegedly inspired from background knowledge and/or Wright, is alleged to suggest the claimed 'deltas' mapping calculation" and Petitioner "does not

rely on Roberts' or Taraschuk's teaching for the values of the 'deltas' mapping elements." *Id.* at 29 (citing Pet. 47–55; Paper 12, 32–33). Patent Owner argues that, "in its only substantive discussions of these independent 'deltas' claim elements, the Petition . . . merely refer[s] to an empty look-up table from Taraschuk, allegedly importable into Roberts, and a complicated and lengthy example derivation of an alleged 'known manner' for mapping." *Id.* at 32 (citing Pet. 47–55). According to Patent Owner, "[Petitioner] mentions the 'look-up table' of Taraschuk repeatedly without citing to the corresponding disclosure . . . perhaps because that disclosure is so sparse and it plainly does not support the weight of alleged obvious understanding and background knowledge [Petitioner] is attempting to put on it." *Id.* at 34 (citing Pet. 53). Patent Owner further asserts that "[t]he only disclosure of this look-up table in Taraschuk merely states that it exists: 'The linearizer 44 is designed in a known manner (e.g., using a random access memory look-up table)' to perform the mapping." *Id.* (citing Ex. 1006, 6:61–65; *see id.* at 32 (citing Pet. 55), 33 (citing Exs. 2003, 2018, 2019, 2022 ¶¶ 41–42).

Patent Owner further argues that

> Taraschuk does have its own brief description of its mapping—but Cisco doesn't cite it because it points away from Dr. Blumenthal's analysis. EX2022, ¶¶49, 86-90 ("Reading Taraschuk, they would eventually be told to use sampled analog feedback to pre-distort the input words. EX1006 at 7:67-8:5. This also points away from attempts to mathematically pre-calculate a complementary function."). For example, Taraschuk's disclosures are directed to compensating "for the combined non-linear effects of ***logic level mismatches through the D/A converter 12 and*** the sinusoidal response of the modulator 52." EX1006, 7:61-67 (emphasis added); EX2022, ¶86. When Cisco quotes this disclosure with respect to earlier elements, it pointedly omits the text emphasized above. Petition at 42.

PO Resp. 36. Patent Owner asserts that "[t]he omitted disclosure suggests a combined compensation that accounts for logic level mismatches in the D/A converter as well as the real response curve of the modulator, not the separate idealized sinusoidal graphs Dr. Blumenthal calculates." *Id.* at 36–37 (citing Ex. 2022 ¶¶ 51 ("There is no disclosure in *Taraschuk* about the possibility of compensating the 'sinusoidal response of the modulator' alone, as Dr. Blumenthal does in his calculations in his declaration. See EX1003 ¶¶ 170-76. And of course, there is no disclosure of any of the approach or math that Dr. Blumenthal uses there."), 86–87, 105–106).

Patent Owner also asserts that "[Petitioner] and Dr. Blumenthal also completely ignore the mention in Taraschuk of 'computation of the suitable mapping,' which involves receiving an input and 'comparing it to a detected sample' of the analog modulator output." PO Resp. 37 (citing Ex. 1006, 7:67–8:5, Fig. 6). According to Patent Owner, however, "[w]hat *Taraschuk* actually describes as an input into its mapping computation is an analog sample detected and fed back from the modulator output—**not** graphs drawn by and derived table values calculated by Dr. Blumenthal." *Id.* at 38 (citing Ex. 1006, 7:34–38, ("sampled analog signal level (S)"), 7:67–8:5 Figs. 5, 6); Ex. 2022 ¶¶ 49, 86–87, 90).

Petitioner's Reply Arguments

Petitioner asserts that "[t]he '*deltas*' limitations in the challenged claims result naturally from performing non-linear compensation of an optical modulator—such as a Mach-Zehnder modulator—whose output varies sinusoidally." Pet. Reply 7 (citing Pet. 41–57). According to Petitioner, "[t]he Petition demonstrated the obviousness of the '*deltas*' limitations through Dr. Blumenthal's application of Wright's look-up table

construction techniques to 'a generic sinusoidal response curve and Taraschuk's example of a 6-bit to 8-bit linearizer.'" *Id.* (citing Pet. 46).

Petitioner also argues that "[w]hile calculating the *deltas* between a given mapping's values is necessary to determine whether the mapping is within the claim scope, performing those calculations is not itself a claimed process step." *Id.* at 11 (citing Ex. 1029, 139:4–12). "Thus," according to Petitioner, "it is sufficient for the prior art to render obvious a mapping exhibiting the *deltas* features; the prior art need not calculate the *deltas* themselves." *Id.*

Petitioner further argues that "Patent Owner faults Dr. Blumenthal's modeled sinusoidal response curve because it doesn't factor in the 'logic level mismatches' described by Taraschuk." *Id.* at 12 (citing PO Resp. 36–37). "But Dr. Dallesasse agrees that modeling a Mach-Zehnder modulator as exhibiting a sinusoidal response—as Dr. Blumenthal did—was 'reasonable' 'to a first order.'" *Id.* (citing Ex. 1029, 116:7–117:4). "Any other sources of non-linearity would merely be less significant, 'second order effects.'" *Id.* at 12–13 (citing Ex. 1019, 117:4–5). Petitioner also argues that "Taraschuk also describes embodiments *without* logic level mismatches, and Dr. Dallesasse agrees that they can be eliminated (rather than simply compensated for)." *Id.* at 13 (citing Ex. 1029, 58:1–10).

Analysis of the Parties' Arguments

In our Institution Decision, we preliminarily determined, *inter alia*, that

> Petitioner has provided sufficient evidence that "[i]t would have thus been obvious to a POSITA for an MZM's nonlinear compensation lookup table to include a range of outputs whose successive differences are decreasing" because "[t]his result ***follows naturally*** from the observation that the nonlinear

> compensation must counteract the nonlinear response of the MZM, which is sinusoidal." We further agree that "[t]his characteristic is a natural consequence of the nonlinear compensation response curve being a reflection of the MZM sinusoidal response curve across the desired linear output line."

Inst. Dec. 41–42 (citing Ex. 1003 ¶ 193; Pet. 56–57).

Based on our review of the complete record developed during trial, we are persuaded to modify our preliminary determinations because we are persuaded Petitioner does not sufficiently rebut Patent Owner's contentions that Dr. Blumenthal's idealized sinusoidal compensation curves are not representative of Taraschuk's teachings. In our Institution Decision we also stated that

> [i]t remains a factual issue to be developed during trial as to whether the idealized, natural sinusoidal response curves derived by Dr. Blumenthal are representative of "the combined non-linear effects of logic level mismatches through the D/A converter 12 and the sinusoidal response of the modulator 52" disclosed by Taraschuk. We invite the parties to fully brief this issue during trial.

Inst. Dec. 34–35 (citing Prelim. Resp. 52 (quoting Ex. 1006, 7:61–67)). Petitioner responded that "[a]s the petition pointed out, however, Taraschuk does make that suggestion, describing a linearizer for 'compensating non-linearities of the A/D converter (and/or the optical modulator 52).'" Pet. Reply 14 (quoting Ex. 1006, 8:49–53) (citing Pet. 20; Ex. 1003 ¶ 118) (Petitioner's emphasis omitted). But this portion of Taraschuk is only cited in the sections of the Petition summarizing Taraschuk (Pet. 20 (Section X.B.2, "Summary of Taraschuk")) and discussing the Rationale for Combining (*id.* at 26 (Section X.B.3, "Reasons to Combine Roberts and Taraschuk")). Petitioner does not cite column 8, lines 49–53 of Taraschuk in its limitation-by-limitation analysis of independent claim 1.

Instead, Petitioner cites column 7, lines 61–67 of Taraschuk, which discloses that a "mapping can be defined between the M-bit input digital signal 46 and an N-bit signal 6 . . . which compensates for the combined non-linear effects of logic level mismatches through the D/A converter 12 and the sinusoidal response of the modulator 52. Ex. 1006, 7:61–67; *see* Pet. 42 (citing Ex. 1006, 7:61–67, 8:13–15 ("The combined response of the D/A converter and optical modulator is more nearly linear, and can more easily be corrected by an MxN mapping in the linearizer 44."); Ex. 1003 ¶¶ 163, 164). As such, we do not consider Petitioner's citation to column 8, lines 49–53 of Taraschuk with respect to limitations 1.8 and 1.9.

We agree with Patent Owner's argument that the portions of Taraschuk in column 7, lines 61–67 and column 8, lines 13–15 cited by Petitioner in its challenge to claim 1 teach "an end-to-end approach" "because Taraschuk's disclosed calculation involves predistortion of the input M-bit word by subtracting a digitized analog sample of the ultimate output," and as such, teach "an approach that necessarily does one combined correction for all of the non-linearities that occur in-between those ends—whether bit mismatches in the digital logic or non-linearities in the Mach-Zehnder modulator." PO Sur-reply 24 (citing PO Resp. 34–39; Ex. 2022 ¶¶ 49, 50, 86–88, 90, 104; Ex. 1006, 7:61–67). We further agree that

> [Patent Owner] and Prof. Dallesasse are not suggesting that Dr. Blumenthal should model the logic-level mismatches. But rather pointing out that calculating an idealized sinusoidal response in isolation is not obvious (or flowing naturally) from a reference that can only deal with compensating the combined response of the modulator and digital logic mismatches ***together***—via real-time pre-distortion fed back from the ultimate output and subtracted from the input.

Id. at 25 (citing Ex. 2022 ¶¶ 50, 86–88). In support, Dr. Dallesasse testifies that

> Dr. Blumenthal starts with the premise that all that is required is deriving a complementary function to the sinusoidal response. . . . But this ignores that the disclosure of *Taraschuk* describes compensating "the sinusoidal response of the modulator" ***and*** "logic level mismatches through the D/A converter" ***together***. . . . Dr. Blumenthal's complementary sinusoidal correction curve won't do that. The combined non-linearity from the multiple sources likely won't simply be evenly sinusoidal. *Taraschuk* does not disclose, or in my opinion render obvious, any pre-calculation solution. (*Taraschuk* mentions a real-time analog feedback loop to pre-distort, which would not involve pre-calculation.) And it certainly does not suggest one that could deal with the combined and likely complex non-linearities described.

Ex. 2022 ¶ 86 (citing Ex. 1003 ¶ 163; Ex. 1006, 7:61–67).

Even assuming, *arguendo*, we were to consider Petitioner's citation to column 8, lines 49–53—disclosing "an instance of 'and/or' in the Taraschuk specification" with respect to "compensating non-linearities of the A/D converter (and/or the optical modulator 52)"—in the sections of the Petition summarizing Taraschuk and setting forth reasons for combining Roberts and Taraschuk, Patent Owner persuasively argues that "that disclosure refers to Fig. 7, which has the same end-to-end predistortion calculation as Figs. 5 and 6, none of which are able to isolate and correct for modulator non-linearity effects alone." PO Sur-reply 25, n.2 (citing Pet. Reply 15; Ex. 1006, 8:29–30, 8:49–53, Fig. 7; '576 FWD, 29 (finding persuasive Patent Owner's substantially similar argument) (emphasis omitted). As Petitioner fails to sufficiently support its position that Dr. Blumenthal's idealized sinusoidal curves are representative of Taraschuk's teachings, Petitioner does not sufficiently carry its burden to show that the combination of Roberts,

Taraschuk, and Wright teaches or even suggests either limitation 1.8 or limitation 1.9. This is because the idealized sinusoidal curves that form the basis of Dr. Blumenthal's analysis lack a sufficient showing of relevance to the teachings of Taraschuk cited by Petitioner. Patent Owner persuades us that Petitioner does not point to any basis for a LUT having the recited deltas except for Dr. Blumenthal's analysis. Although Wright generally teaches compensating for mismatches, Dr. Blumenthal's analysis fills in limitations 1.8 and 1.9—Petitioner does not set forth a sufficiently supported reason for using the specific values recited in limitations 1.8 and 1.9.

Even assuming, *arguendo*, we were to credit Petitioner's arguments that "it is sufficient for the prior art to render obvious a mapping exhibiting the *deltas* features; the prior art need not calculate the *deltas* themselves" (Pet. Reply 11) and that "Dr. Dallesasse agrees that modeling a Mach-Zehnder modulator as exhibiting a sinusoidal response—as Dr. Blumenthal did—was 'reasonable' 'to a first order'" and "[a]ny other sources of non-linearity would merely be less significant, 'second order effects,'" (*id.* at 12–13), Petitioner does not sufficiently show that the sinusoidal response curve would look like the one Dr. Blumenthal proposes. Dr. Blumenthal asserts, without specifically or credibly explaining why, that a person of ordinary skill in the art would have selected a region of the sinusoidal response curve that includes an inflection point such that deltas both decrease and increase over some portion of the curve being linearized. *See* Ex. 1003 ¶¶ 173–174 (scaling and shifting a sinusoidal response curve so that the curve contains an inflection point within the linearized region, but without adequately explaining the evidentiary basis for these selections); *id.* ¶ 52 (opining that "in the close vicinity of the center of the positive or negative inflection regions, otherwise known as the Quadrature point, the modulator is almost

linear," but without explaining why a person of ordinary skill in the art would have included regions on both sides of an inflection point). If a person of ordinary skill would have selected a region of the sinusoidal response curve on only one side of an inflection point, the evidence does not suggest that such a mapping would satisfy both limitations 1.8 and 1.9.

At best, Petitioner presents an "obvious to try rationale":

> In addition to the reasons mentioned above, a POSITA would have found it obvious to try a mapping scheme in which entries in the look-up table as taught by Taraschuk are selected such that successively decreasing inputs correspond to digital output entries with either decreasing, increasing, or similar deltas between their values. Doing so would have involved choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success. In that regard, the deltas between values of the corresponding digital outputs can either increase, decrease, or stay the same. Accordingly, there are only three possible relationships between deltas of successive digital outputs. With so few possibilities, a POSITA would have found it obvious to try each of them.

Pet. 52 (citing Ex. 1003 ¶ 196). The analysis for 13.8 is incorporated by reference in 13.9. *See* Pet. 53–54.

Although there are three possible relationships between two, consecutive deltas, there are many possible sequences of deltas—Petitioner does not sufficiently show a finite number of solutions in its challenge. Petitioner's obvious-to-try rationale is insufficient to show that a person of ordinary skill would have used a digital-to-digital-mapping in which there are regions in which the deltas are both decreasing and increasing. Moreover, Petitioner's Reply includes positions not supported by a Reply Declaration from Dr. Blumenthal and thus, constitute attorney argument that is not sufficiently supported by evidence. *See*, *e.g.*, Pet. Reply 14–15 (Petitioner arguing "Roberts' design obviates the need for a separate,

discrete DAC (*compare* Ex.1005, Fig. 2 *to* Fig. 4), reinforcing that Patent Owner's arguments about logic level mismatches in a DAC are a red herring"); *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984) (lawyer arguments and conclusory statements which are unsupported by factual evidence are entitled to little probative value).

Separate and independent of the analysis set forth above, there is another reason that Petitioner's challenge fails. In our Institution Decision, we determined that

> [a]t the time when Taraschuk's M-bit input digital signal 46 enters the digital-to-analog converter 12, the signal is in digital format and when it is converted to N-bit digital signal 6, it is still in digital format. Even assuming, *arguendo*, that Patent Owner is correct that Taraschuk teaches "analog pre-distortion based on an analog sample feedback loop," the claim does not require a digital feedback loop or exclude an analog feedback loop, and thus, Patent Owner's argument is unavailing.

Inst. Dec. 35 (citing Ex. 1006, 8:2, 8:8). Based on our review of the complete record developed during trial, we are persuaded to modify our preliminary determinations. For the reasons discussed below, we are persuaded that the scope of claim 1 does not encompass linear compensation methods effected by analog pre-distortion because the '998 patent specification distinguishes analog pre-distortion (*see* Ex. 1001, 1:64–2:36) and the prosecution history specifically distinguishes analog pre-distortion from the claimed approach (*see* Ex. 3001, 172).[6]

We find persuasive Dr. Dallesasse's testimony that "a person of ordinary skill in the art reading the ['998] patent would understand that th[e] [claimed] approach of mapping, based on the converter output pattern differs

[6] Ex. 3001 is a portion of the prosecution history of U.S. Patent No. 11, 133, 872, a parent of the '998 patent.

from pre-distortion based on real-time measured analog modulator output." Ex. 2022 ¶ 34 (citing Ex. 1001, 2:5–9 ('998 patent disclosing common, prior art solutions such as "an analog pre-distortion circuit to feed the modulator"); Ex. 1005, 2:53; Ex. 1006, 7:67–8:5, Fig. 6); Ex. 1001, 2:35–37(the '998 patent describing the need for a "digital to analog converter" that would "improve[] linearity of response without sacrificing efficiency or dynamic range" as in the common, prior art solutions). Dr. Dallesasse explains how "the prosecution history of the parent '872 patent [illustrates] that when [Patent Owner] changed 'correct for non-linearities' to the more specific language 'determined based on a pattern for actuating drive voltages that alters the linearity of an optical response of the modulator,'" "the Examiner then allowed the claims over a rejection based on *Roberts*," which "suggests that there are ways to 'correct for non-linearities' that do not meet the amended claims, as the '998 Patent itself admits." *Id.* ¶ 79 (citing Ex. 1001, 2:5–9; Ex. 2009, 2; Ex. 1010, 16–48). During prosecution, Patent Owner argued:

> Roberts does not disclose a "digital-to-digital mapping," where, "for a given plurality of N digital input data bits, the mapping to the corresponding M digital output data bits is determined based on a pattern for actuating drive voltages that alters the linearity of an optical response of the modulator," as recited in amended claim 1. *Instead*, the linear compensation in Roberts is performed pursuant to a compensation function c(t) when the $V_x(n)$ multi-bit sample streams are generated. *Importantly*, this linear compensation in Roberts occurs *before* the mapping of $V_x(n)$ to $S_x(n)$. As a result, the mapping between $V_x(n)$ to $S_x(n)$ in Roberts, such as the mapping shown in Table 1 of Roberts, is not a part of the linear compensation operation performed in Roberts.

Ex. 3001, 172 (emphasis added). We interpret the quoted passage to exclude analog pre-distortion because we interpret the argument distinguishing

Robert's compensation as happening "before the mapping" to refer to pre-distortion techniques—in particular, those accomplished by analog compensation function, c(t). *Id.* Both the '998 patent and Patent Owner's arguments during prosecution support Dr. Dallesasse's testimony and Patent Owner's position that the scope of claim 1 does not encompass linear compensation methods effected by analog pre-distortion.

We find persuasive the distinction between analog pre-distortion and the invention recited in claim 1:

> This mapping could compensate for modulator non-linearity or other undesirable signal characteristics in a way that was both simpler and faster than prior solutions. A person of skill in the art would have understood that the approach of the '998 Patent was advantageous because it did not require the output range restrictions, complicated analog signal conditioning, or other undesirable configurations of previous known systems. The digital-to-digital mapping solution of the '998 Patent could improve "linearity of response without sacrificing efficiency or dynamic range" as prior solutions required.

Ex. 2022 ¶ 21 (citing Ex. 1001, 2:5–9, 7:67–8:3).

We agree with Patent Owner that "*Taraschuk* does not generate or choose a digital output word or constellation point at the output of a converter, but instead applies an analog feedback correction from the ***modulator*** output to the ***input*** word in order to make the intended input appear at the modulator output." PO Resp. 25–26 (citing Ex. 1006, 7:67–8:5, 7:7–11, 7:34–39, Fig. 6). Dr. Dellesasse's testimony supports Patent Owner's position by explaining that

> the only explanatory discussion of *Taraschuk*'s mapping suggests that it is instead determined based on "calculating a difference between the received M-bit word and the sampled analog output signal level (S)." In other words, if the *Taraschuk*

> mapping is "determined based on" anything, it is the real-time sampled analog modulator output.
>
> A person of ordinary skill reading this explanation of the mapping in *Taraschuk*, consisting of a sample of the analog modulator output fed back to alter the input, would likely equate it with the prior art "use of an analog pre-distortion circuit to feed the modulator" solution mentioned in the '998 Patent background.
>
> Finally, beginning at column 7, line 53 of *Taraschuk*, there is a paragraph on using the "analog signal output from the D/A converter" to drive an optical modulator. That discussion states that "in principle" a mapping can be defined to compensate for "the combined non-linear effects" of logic level mismatches and "the sinusoidal response of the modulator." These two sentences say only that the mapping can be obtained by comparing the *input* word to a sample of the *analog output* of the modulator. In other words, this particular embodiment of *Taraschuk* applies a pre-distortion to the input word, based on feedback of an analog sample of the output of the modulator.

Ex. 2022 ¶¶ 80, 81, 49 (citing Ex. 1006, 7:34–39, 7:61–8:5, Fig. 6; Ex. 1001, 2:5–9). We disagree with Petitioner that the testimony of Dr. Dallesasse, Patent Owner's expert, should be afforded little weight because the point raised by Petitioner, that "Dr. Dallesasse provides no evidence as to why a POSITA would understand the '998 patent as seeking to optimize the output of the digital-to-digital **converter** rather to than correct (linearize) the inherent sinusoidal response of the **modulator** as stated in the '998 patent," is not the dispositive inquiry. Pet. Reply 28 (citing Ex. 1001, 1:35–37, Title). Rather, the dispositive inquiry is whether the cited portions of Taraschuk support Dr. Dallesasse's testimony and Patent Owner's position that "because Taraschuk's disclosed calculation involves pre-distortion of the input M-bit word by subtracting a digitized analog sample of the ultimate output—it teaches an end-to-end approach." PO Sur-reply 24 (citing Ex.

1006, 7:34–39); Ex. 2022 ¶¶ 49, 86–90 ("Reading Taraschuk, they would eventually be told to use sampled analog feedback to pre-distort the input words. EX1006 at 7:67-8:5. This also points away from attempts to mathematically pre-calculate a complementary function."). Taraschuk discloses, with respect to Figure 5, that "calculating a difference between the received M-bit word and the sampled analog output signal level (S), the signal processor 48 can readily compute a mapping between the received M-bit word of the input digital signal 46 and an N-bit word required to obtain the desired output analog signal level." Ex. 1006, 7:34–39. Taraschuk further discloses that

> the process of sampling analog output signal level (S); determining a difference between the sampled signal level (S) and the corresponding M-bit word; recalculation of the mapping, and loading the new mapping into the linearizer 44 can be performed at a rate that is significantly slower than the line rate of the M-bit input digital signal 46.

Id. at 7:46–52. Taraschuk also describes a similar process with respect to Figure 6: "computation of the suitable mapping can be obtained by receiving an M-bit word of the input digital signal and comparing it to a detected sample of the modulator output 56 in a manner directly analogous to that described above with reference to FIG. 5." *Id.* at 7:67–8:5.

Petitioner does not sufficiently address the cited teachings and in particular, Taraschuk's teachings of calculating a difference between a sampled analog output signal (S) and corresponding M-bit word to a calculate a mapping "required to obtain the desired output analog signal level." Ex. 1006, 7:34–39. We are persuaded Petitioner does not sufficiently rebut Patent Owner's contention that Roberts' and Taraschuk's teachings of linear compensation are implemented by analog pre-distortion. As Petitioner

fails to sufficiently explain why analog pre-distortion should be encompassed by the invention recited in independent claim 1, Petitioner does not sufficiently carry its burden.

For the foregoing reasons, we determine that Petitioner does not establish obviousness of independent claim 1 over the combination of Roberts, Taraschuk, and Wright by a preponderance of the evidence.

5. Independent Claims 16, 32, 45, and 58

With respect to independent claims 16, 32, 45, and 58, Petitioner cites, in large part, its analysis for independent claim 1. *See, e.g.,* Pet. 73–74 (noting that claim 16 requires digital input values in decreasing order, which makes its scope "not meaningfully different" than claim 1); *id.* at 75–81 (analyzing claim 32 by reference to claim 1). Patent Owner appears to address the independent claims together. *See generally* PO Resp. For these reasons, our analysis for the remaining independent claims is substantially similar to the analysis of independent claim 1, outlined above. Accordingly, we determine that Petitioner does not establish obviousness by preponderance of the evidence with respect to the challenge to independent claims 16, 32, 45, and 58 applying Roberts, Taraschuk, and Wright for substantially the same reasons set forth with respect to claim 1.

6. Dependent Claims

We have reviewed Petitioner's showing as to dependent claims 2–15, 17–31, 33–44, 46–57, and 59–63 and note that it does not cure the deficiencies noted above with respect to any of independent claims 1, 16, 32, 45, and 58. Accordingly, we determine that Petitioner does not establish obviousness by preponderance of the evidence with respect to the challenge to dependent claims 2–15, 17–31, 33–44, 46–57, and 59–63 applying Roberts, Taraschuk, and Wright.

E. Obviousness over Roberts and Taraschuk

Petitioner argues that claims 1–63 would have been obvious in view of Roberts and Taraschuk. Pet. 27–85. For this ground of unpatentability, Petitioner does not include Wright in the combination of prior art references, instead relying on Wright as evidence of the background knowledge of the person of ordinary skill in the art. *Id*. Patent Owner disputes Petitioner's showing. *See generally* PO Resp. With respect to claims 1–63, we reach the same conclusion as set forth above with respect to the challenge applying Roberts, Taraschuk, and Wright and incorporate our analysis herein. Accordingly, we determine that Petitioner does not establish obviousness by preponderance of the evidence with respect to the challenge to claims 1–63 applying Roberts and Taraschuk for substantially the same reasons set forth in Sections III.D.4–6 *supra*.

IV. MOTION TO EXCLUDE

Patent Owner requests that we exclude Petitioner's Exhibits 1031 through 1038 submitted with Petitioner's Reply. Paper 25, 1. Petitioner opposes. Paper 27. As we do not rely on any of these exhibits in rendering the findings and conclusions in this Decision, Patent Owner's motion is moot.

V. CONCLUSION

In summary:

Claims Challenged	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–63	103(a)	Roberts, Taraschuk		1–63
1–63	103(a)	Roberts, Taraschuk, Wright		1–63

Claims Challenged	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
Overall Outcome				1–63

VI. ORDER

For the reasons given, it is:

ORDERED that Petitioner has not established, by a preponderance of evidence, that any of claims 1–63 of the ’998 patent are unpatentable as obvious under 35 U.S.C. § 103;

FURTHER ORDERED that Patent Owner’s Motion to Exclude is dismissed as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-01283
Patent 11,342,998 B2

OGDEN, *Administrative Patent Judge*, concurring.

I concur in the result, and would determine that Petitioner has failed to meet its burden of persuasion to show that the asserted prior art explicitly, implicitly, or inherently teaches a digital-to-digital mapping in which the deltas between increasing digital input values both decrease and increase as per limitations 1.8 and 1.9, respectively. *See* Ex. 1001, 17:42–55.

On the one hand, I find Petitioner's arguments persuasive that limitations 1.8 and 1.9 would be a natural consequence of compensating for an idealized sinusoidal response curve like the one Dr. Blumenthal has generated. *See* Ex. 1003 ¶¶ 174–202; Pet. Reply 11–12. I also consider persuasive Petitioner's argument that, when a sinusoidal response curve is linearized using a lookup table as in Taraschuk, any logic-level mismatches and other errors would be relatively small and, even if compensated for,

would not change the response curve's overall sinusoidal nature. *See* Pet. Reply 12–13 (citing Ex. 1029, 116:7–117:5 (cross-examination testimony of Dr. Dallesasse)); *but see* Ex. 2022 ¶¶ 86–87 (Dr. Dallesasse opining that a response curve taking into consideration logic-level mismatches would not "simply be evenly sinusoidal" and would be "complex"—which is not to say that it would not be generally sinusoidal).

On the other hand, I agree with the majority that Petitioner has not adequately proven that the sinusoidal response curve would look like the one Dr. Blumenthal proposes. I further agree with the majority that Petitioner's obvious-to-try rationale is insufficient to show that a person of ordinary skill would have used a digital-to-digital-mapping in which there are regions in which the deltas are both decreasing and increasing.

Therefore, I concur in the result of the decision determining that Petitioner has not established, by a preponderance of evidence, that any of claims 1–63 of the '998 patent are unpatentable as obvious under 35 U.S.C. § 103.

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