UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-00576
U.S. Patent No. 11,133,872 B2

PETITIONER'S NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

via P-TACTS
Patent Trial and Appeal Board

via Email
Director of the United States Patent and Trademark Office
efileSO@uspto.gov

via CM/ECF
United States Court of Appeals for the Federal Circuit

Pursuant to 28 U.S.C. § 1295(a)(4)(A), 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a), 90.3, 5 U.S.C. §§ 701–706, and Federal Circuit Rule 15(a)(1), Petitioner Cisco Systems, Inc. ("Petitioner") provides notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered October 3, 2023 (Paper 41), the Board's Decision Denying Petitioner's Request on Rehearing of the Final Written Decision entered February 29, 2024 (Paper 46), and from all underlying and related orders, decisions, rulings, and opinions regarding U.S. Patent No. 11,133,872 B2 ("the '872 patent") in *Inter Partes* Review IPR2022-00576.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), the expected issues on appeal include, but are not limited to: the Board's error(s) in determining that Petitioner has failed to demonstrate that challenged claims 13, 14, and 23-29 of the '872 patent are unpatentable, that Petitioner's Request for Rehearing should be denied, and any finding or determination supporting or related to that determination, as well as all other issues decided adversely to Petitioner in any orders, decisions, rulings, or opinions in *Inter Partes* Review IPR2022-00576.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), this Notice is being filed with the Director of the United States Patent and Trademark Office and with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of

Appeals for the Federal Circuit via CM/ECF.

Respectfully submitted,

Dated: April 22, 2024

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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PTAB P-TACTS, a true and correct copy of the above-captioned PETITIONER'S NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT is being filed by email with the Director on April 22, 2024, at efileSO@uspto.gov.

The undersigned also hereby certifies that a true and correct copy of the above-captioned PETITIONER'S NOTICE OF APPEAL TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on April 22, 2024.

Respectfully submitted,

Dated: April 22, 2024

/Theodore M. Foster/
Theodore M. Foster
Counsel for Petitioner
Registration No. 57,456

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, this is to certify that a true and correct copy of the foregoing "Petitioner's Notice of Appeal to the United States Court of Appeals for the Federal Circuit" was served on counsel for Patent Owner Ramot At Tel Aviv University Ltd. as detailed below:

Date of service	April 22, 2024
Manner of service	Email: bentzminger@bdiplaw.com cjohanningmeier@bdiplaw.com BDIP_RamotIPRService@bdiplaw.com
Documents served	**Petitioner's Notice of Appeal to the United States Court of Appeals for the Federal Circuit**
Persons served	Brenda Entzminger Corey Johanningmeier (Pro Hac Vice) Bunsow De Mory LLP 701 El Camino Real Redwood City, CA 94063

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Paper 41
Date: October 3, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-00576
Patent 11,133,872 B2

Before CHRISTOPHER L. CRUMBLEY, MONICA S. ULLAGADDI, and JASON M. REPKO, *Administrative Patent Judges.*

ULLAGADDI, *Administrative Patent Judge*.

JUDGEMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
Dismissing as Moot Patent Owner's Motion to Exclude Evidence and Patent Owner's Objections to Petitioner's Demonstratives
35 U.S.C. § 318(a)

I. INTRODUCTION

Cisco Systems, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 13, 14, and 23–29 ("the challenged claims") of U.S. Patent No. 11,133,872 B2 (Ex. 1001, "the '872 patent"), accompanied by the supporting Declaration of Dr. Daniel J. Blumenthal (Ex. 1003). Ramot at Tel Aviv University Ltd. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Prelim. Resp.").

Upon review of the record, we instituted *inter partes* review, pursuant to 35 U.S.C. § 314, as to the challenged claims based on the challenges set forth in the Petition. Paper 10 ("Institution Decision" or "Inst. Dec.").

After institution of trial, Patent Owner filed a combined Request for Rehearing and Request for Precedential Opinion Panel (POP) Review. Paper 12 ("Req. Reh'g"). On February 22, 2023, the Request for POP Review was denied. Paper 20. On May 22, 2023, we denied Patent Owner's Request for Rehearing. Paper 28.

Patent Owner filed a Response (Paper 18, "Patent Owner's Response" or "PO Resp.") accompanied by the supporting Declaration of Dr. John Dallesasse (Ex. 2018), Petitioner filed a Reply to Patent Owner's Response (Paper 24, "Petitioner's Reply" or "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 31, "Patent Owner's Sur-reply" or "PO Sur-reply").

Patent Owner timely objected to Petitioner's evidence (Paper 25) and thereafter filed a Motion to Exclude Exhibits 1026–1033. Paper 33 ("Mot. Ex.").[1] Petitioner opposed Patent Owner's Motion to Exclude (Paper 34, "PO Opp. Ex."), and Patent Owner replied to Petitioner's Opposition (Paper

[1] Although Patent Owner also moved to exclude Exhibit 1024 (Mot. Ex. 1), that request was later withdrawn. *See* Paper 35, 1. Accordingly, we do not address Patent Owner's objections to Exhibit 1024.

35, "Pet. Reply Ex."). Patent Owner also objected to certain portions of Petitioner's demonstratives. Paper 36.

On July 5, 2023, we held an oral hearing. A transcript of the hearing is of record. Paper 39.

For the reasons that follow, we conclude that Petitioner has not established, by a preponderance of the evidence, that the challenged claims of the '872 patent are unpatentable.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies Cisco Systems, Inc. and its subsidiary, Acacia Communications, Inc. as the real parties-in-interest. Pet. 82.

Patent Owner identifies Ramot at Tel Aviv University Ltd. as the real party-in-interest. Paper 4, 2.

B. Related Matters

The parties indicate that the '872 patent is involved in the following district court case: *Cisco Systems, Inc. et al. v. Ramot at Tel Aviv University Ltd.*, Case No. 1-21-cv-01365 (D. Del.) (pending). Pet. 82; Paper 4, 2.

The parties further indicate that the '872 patent is also related to three patents that were/are the subject of the following administrative proceedings:

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2020-00122 (PTAB) (institution denied);

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2020-00123 (PTAB) (institution denied);

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2020-00484 (PTAB) (institution denied);

Ex Parte Reexamination, Control No. 90/014,526, merged with 90/014,608 (reexamination certificate issued);

Ex Parte Reexamination, Control No. 90/014,527, merged with 90/014,606 (decision on appeal reverses examiner's rejections); and

Ex Parte Reexamination, Control No. 90/014,528, merged with 90/014,607 and 90/014,728 (notice of intent to issue reexamination certificate issued). Pet. 82–83; Paper 4, 2–3.

The parties additionally indicate that the '872 patent is the subject of a concurrently filed petition in IPR2022-00575. Pet. 83; Paper 4, 2.

Petitioner further indicates that the '872 patent is related to a patent that is the subject of the following administrative proceeding:

Cisco Systems, Inc. v. Ramot at Tel-Aviv University Ltd., IPR2022-01283 (PTAB) (instituted). Paper 15, 2.

Patent Owner further indicates that the '872 patent is also related to three patents that are the subject of the following district court proceedings:

Ramot at Tel Aviv University Ltd. v. Cisco Systems, Inc., 2:19-cv-00225 (E.D. Tex.) (pending); and

Ramot at Tel Aviv University Ltd. v. Acacia Communications, Inc., 1:21-CV-00295 (D. Del.) (pending). Paper 4, 2–3.

C. The '872 Patent

The '872 patent is titled "Linearized Optical Digital-to-Analog Modulator." Ex. 1001, code (54). The '872 patent discloses a system for converting digital data into a modulated optical signal, where an electrically controllable device having M actuating electrodes provides an optical signal that is modulated in response to binary voltages applied to the actuating electrodes. *Id.* at (57). A digital-to-digital converter provides a mapping of input data words to binary actuation vectors of M bits and supplies the binary actuation vectors as M bits of binary actuation voltages to the M actuating electrodes, where M is larger than the number of bits in each input

data word. *Id.* The digital-to-digital converter maps each digital input data word to a binary actuation vector by selecting a binary actuation vector from a subset of binary actuation vectors available to represent each of the input data words. *Id.*

Referring to FIG. 1, reproduced below, the ’872 patent discloses a modulator device 10 that has an electronic input 12 for receiving an input data word D of N bits and an electrically controllable modulator 14 for modulating the intensity of an optical signal represented by arrow 16. Ex. 1001, 7:5–13.

FIG. 1

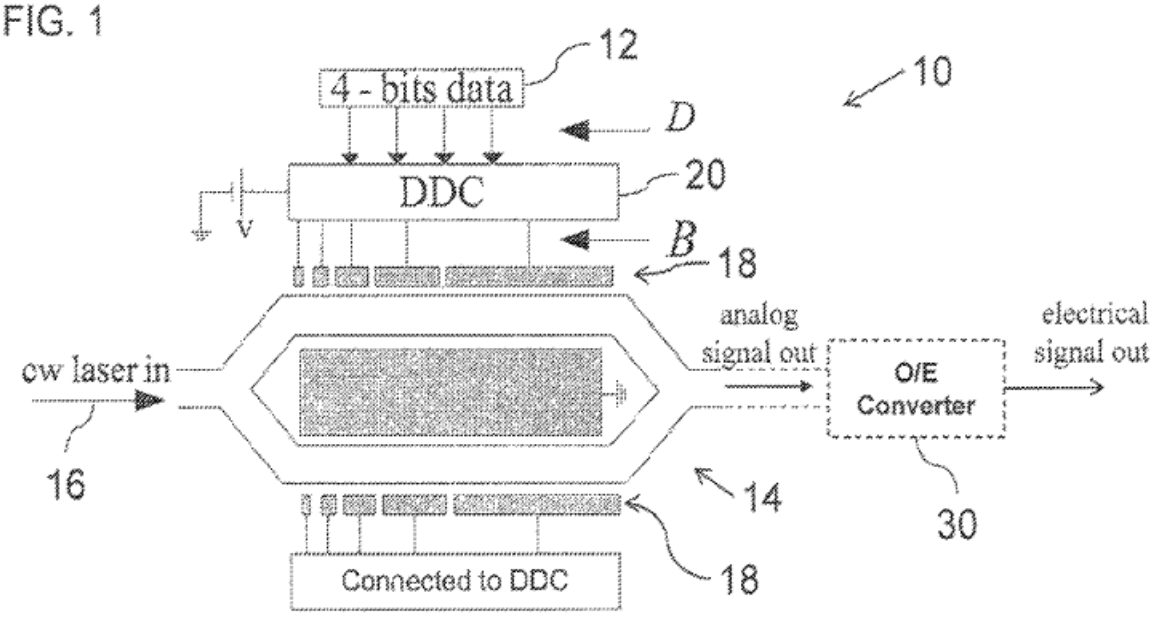


Figure 1 of the ’872 patent is a schematic representation of a modulator device for converting digital data into analog modulation of an optical or electrical signal.

Modulator 14 includes M actuating electrodes 18 where M≥N.[2] *Id.* at 7:13–14. Modulator device 10 also includes an electrode actuating device 20 responsive to the input data word D to supply an actuating voltage to the actuating electrodes 18. *Id.* at 7:14–17. Thus, electrode actuating device 20 actuates at least one of actuating electrodes 18 as a function of values of more than one bit of the input data word D. *Id.* at 7:17–21. In other words, at least one of the electrodes is actuated in a manner differing from a simple one-to-one mapping of data bits to electrode voltage, thereby providing freedom to choose the electrode actuation pattern which best approximates a desired ideal output for the given input. *Id.* at 7:21–25.

D. Illustrative Claim

Of challenged claims 13, 14, and 23–29, claims 13 and 23 are independent. Claim 13 is illustrative and is reproduced below.

> 13. A method for converting digital inputs of N bits in parallel into modulated optical streams, comprising:
>
> inputting into an optical modulator a digital input, wherein the digital input is one from a set of 2^N digital inputs that each has N bits of digital data, and wherein N>l; and
>
> mapping, based on a digital-to-digital mapping, the digital input to a first digital output associated with M drive voltages, wherein the first digital output is one from a set of digital outputs that each has M bits of digital data, wherein the set of digital outputs comprises 2^M digital outputs, and wherein M>=N,
>
> wherein the digital-to-digital mapping comprises, for each digital input included in the set of 2^N digital inputs, a mapping to a corresponding digital output included in the set of digital outputs,

[2] The ’872 patent actually recites “M N,” but it appears from the context of the rest of the disclosure of the ’872 patent that “M≥N” was intended.

> wherein, for a first subset of successively decreasing digital inputs in the set of 2^N digital inputs specified in the digital-to-digital mapping, deltas between numerical values of digital outputs in the set of digital outputs corresponding to the successively decreasing digital inputs in the first subset decrease, and
>
> wherein, for a second subset of successively decreasing digital inputs in the set of 2^N digital inputs specified in the digital-to-digital mapping, deltas between numerical values of digital outputs in the set of digital outputs corresponding to the successively decreasing digital inputs in the second subset increase.

Ex. 1001, 18:40–67.

E. Asserted Grounds

Petitioner presents the following challenges as summarized in the chart below. Pet. 24. Petitioner supports its challenges with the Declaration of Dr. Daniel J. Blumenthal. Ex. 1003.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
13, 14, 23–29	103(a)[3]	Roberts[4], Taraschuk[5]
13, 14, 23–29	103(a)	Roberts, Taraschuk, Wright[6]

[3] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the effective filing date of the challenged claims. The earliest possible filing date is June 13, 2007. Ex. 1001, code (60). Therefore, we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103(a).
[4] U.S. Patent No. 7,277,603 B1, filed February 22, 2006 and issued October 2, 2007, to Roberts et al. (Ex. 1005, "Roberts").
[5] U.S. Patent No. 6,781,537 B1, issued August 24, 2004, to Taraschuk et al. (Ex. 1006, "Taraschuk").
[6] U.S. Patent No. 7,058,369 Bl, issued June 6, 2006, to Wright et al. (Ex. 1009, "Wright").

III. ANALYSIS

A. Legal Standards

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). According to Petitioner,

> [a] Person of Ordinary Skill in The Art ("POSITA") in June of 2007 would have had a working knowledge of optical modulators and modulation schemes. A POSITA would have had a master's degree in electrical engineering, or an equivalent, and two years of professional experience relating to optical communications, and in particular, optical signal modulation. Lack of professional experience can be remedied by additional education, and vice versa.

Pet. 14–15 (citing Ex. 1003 ¶¶ 21–23). According to Patent Owner,

> a person of ordinary skill in the art as of the effective priority date in 2007 would have had a Master of Science degree in Electrical Engineering or Electrical and Computer Engineering, and at least two years of academic or professional experience in engineering, specifically in the analysis and design of optoelectronic systems for optical communications.

PO Resp. 24–25 (citing Ex. 2018 ¶¶ 22–26).

We do not discern a substantial difference between the parties' definitions for the level of ordinary skill in the art. Instead, we determine that the parties' definitions are substantially similar. We adopt Petitioner's definition of the level of skill in the art, which is consistent with the disclosure of the '872 patent and asserted prior art of record. The findings and conclusions rendered in this Decision would not change had we adopted Patent Owner's definition.

C. Claim Construction

In *inter partes* review proceedings based on petitions filed on or after November 13, 2018, such as this one, we construe claims using the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. *See* 37 C.F.R. § 42.100(b).

We need not construe any claim term in our Decision in order to resolve the issues before us. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (explaining that construction is needed only for terms that are in dispute, and only as necessary to resolve the controversy).

D. Obviousness over Roberts, Taraschuk, and Wright

Petitioner argues that claims 13, 14, and 23–29 would have been obvious in view of Roberts, Taraschuk, and Wright. Pet. 77–80. Patent

Owner disagrees. PO Resp. 54–59. For the reasons that follow, we are not persuaded that Petitioner establishes that claims 13, 14, and 23–29 would have been obvious in view of Roberts, Taraschuk, and Wright by a preponderance of the evidence.

Petitioner's first challenge "presents the combination of Roberts and Taraschuk as teaching the claimed limitations related to increasing or decreasing deltas" and "relies on the Wright reference as evidence of the background knowledge of a POSITA with respect to calculating the values for a non-linear compensation lookup table." Pet. 77. According to Petitioner, "[t]o the extent Patent Owner argues that calculating such values would not have been within the background knowledge of a POSITA," Petitioner's second challenge "is presented to show that calculating such values would have been obvious to a POSITA, as evidenced by Wright." *Id.* at 78 (citing Ex. 1003 ¶ 324).

Petitioner's challenge applying Roberts, Taraschuk, and Wright refers, in large part, back to its analysis in the challenge applying Roberts and Taraschuk. As such, we refer to Petitioner's challenge applying Roberts and Taraschuk for the element-by-element analysis of the claims. Pet. 25–77.

1. Overview of Roberts

Roberts is entitled "Integrated Optical Waveform Modulation." Ex. 1005, code (54). Roberts discloses a method of modulating an optical carrier. *Id.* at code (57). A target carrier modulation is computed based on an input data signal. *Id.* An effective length of an optical modulator is then controlled based on the target carrier modulation. *Id.* Figure 4 of Roberts, reproduced below, depicts principal components and operation of a complex optical synthesizer.

Figure 4

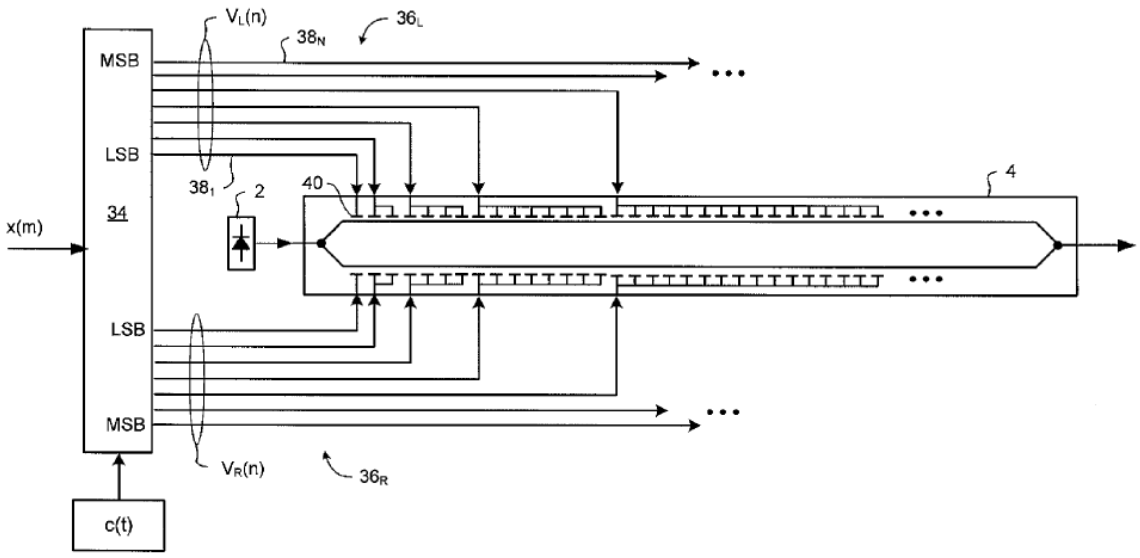


Figure 4 of Roberts depicts "principal components and operation of a complex optical synthesizer." *Id.* at 5:20–21, Fig. 4.

In general, the optical modulator operates by computing a target carrier modulation, and then varying the effective length of the control region of the optical modulator in accordance with the target modulation. *Id.* at 5:47–50. The electrodes of the modulator are configured such that the drive signals are the binary logic states output by the driver IC with no signal conditioning or power amplification required between the driver IC and the optical modulator. *Id.* at 5:50–54.

As illustrated in Figure 4, the driver IC is implemented as a digital signal processor (DSP) 34, which generates a pair of multi-bit sample streams $V_X(n)$ which are representative of the desired phase modulation to be applied to each branch of an MZ modulator 4. *Id.* at 5:56–60. Each multi-bit sample stream $V_X(n)$ may be an N-bit parallel binary signal output from the DSP 34 on a corresponding N-bit data bus 36. *Id.* at 6:40–42. In such a case,

each line 38_i of the N-bit bus 36 is connected to control a number of electrodes 40 corresponding to its binary weight. *Id.* at 6:42–44.

2. Overview of Taraschuk

Taraschuk is entitled "High Speed Digital to Analog Converter." Ex. 1006, code (54). Taraschuk discloses a high-speed D/A converter that includes a phase aligner and a vector summation block (i.e., vector addition block). *Id.* at code (57). The phase aligner operates to ensure precise phase alignment between corresponding bits of a parallel N-bit digital signal having a data rate of at least 2 GHz. *Id.* The vector addition block performs a vector addition of the phase-aligned bits of the parallel N-bit digital signal. *Id.* Figure 5 of Taraschuk, reproduced below, depicts principal elements in a high-speed digital-to-analog converter.

Figure 5

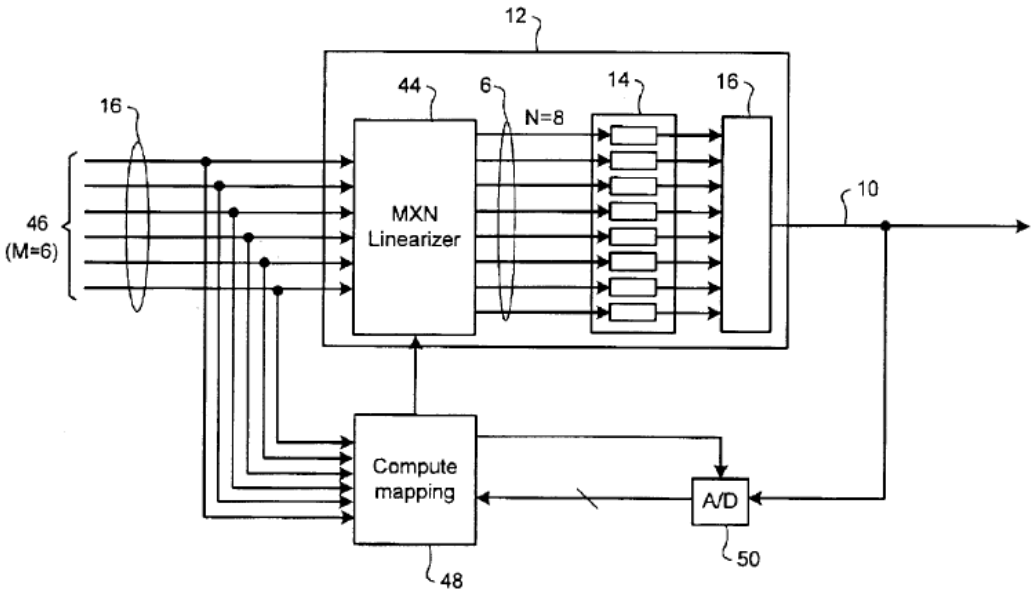


Figure 5 of Taraschuk depicts "principal elements in a high-speed digital-to-analog converter." *Id.* at 3:16–17, Fig. 5.

Figure 5 illustrates an M=6-bit D/A converter 12 having a linearizer 44 connected upstream of the phase aligner 14 and vector addition blocks 16. *Id.* at 6:58–61. The linearizer 44 is designed to map an M-bit digital signal into an N-bit parallel digital signal 6 for processing by the phase aligner 14 and vector summation block 16. *Id.* at 6:61–65. In general, the number (M) of bits of the input digital signal 46 will be less than the number (N) of bits of the parallel digital signal 6 processed by the phase aligner 14 and vector summation block 16. *Id.* at 6:65–7:1.

Figure 5 further illustrates a system for periodically re-calculating the mapping implemented in the linearizer 44. *Id.* at 7:23–25. "[T]he M-bit digital signal 46 is tapped and provided to a signal processor 48." *Id.* at 7:26–27. "The analog output signal (S) is sampled by an analog-to-digital converter 50 and supplied to the signal processor 48." *Id.* at 7:27–29. "By controlling the timing of the sample detected by the analog-to-digital converter 50, the signal processor 48 can receive an M-bit word of the input digital signal 46 and obtain a sample of the corresponding analog signal level (S) generated by the D/A converter 12 based on that M-bit word." *Id.* at 7:29–34. "By calculating a difference between the received M-bit word and the sampled analog output signal level (S), the signal processor 48 can readily compute a mapping between the received M-bit word of the input digital signal 46 and an N-bit word required to obtain the desired output analog signal level." *Id.* at 7:34–39.

3. Overview of Wright

Wright is entitled "Constant Gain Digital Predistortion Controller for Linearization of Non-Linear Amplifiers." Ex. 1009, code (54). Wright discloses methods and an apparatus for controlling and adapting a digital predistortion linearizer for amplification of bandlimited signals using

non-linear amplifiers. *Id.* at code (57). The control method permits the predistortion function applied by a predistortion entity to provide a relatively constant gain. *Id.* Figure 6A, reproduced below, depicts input versus output response curves.

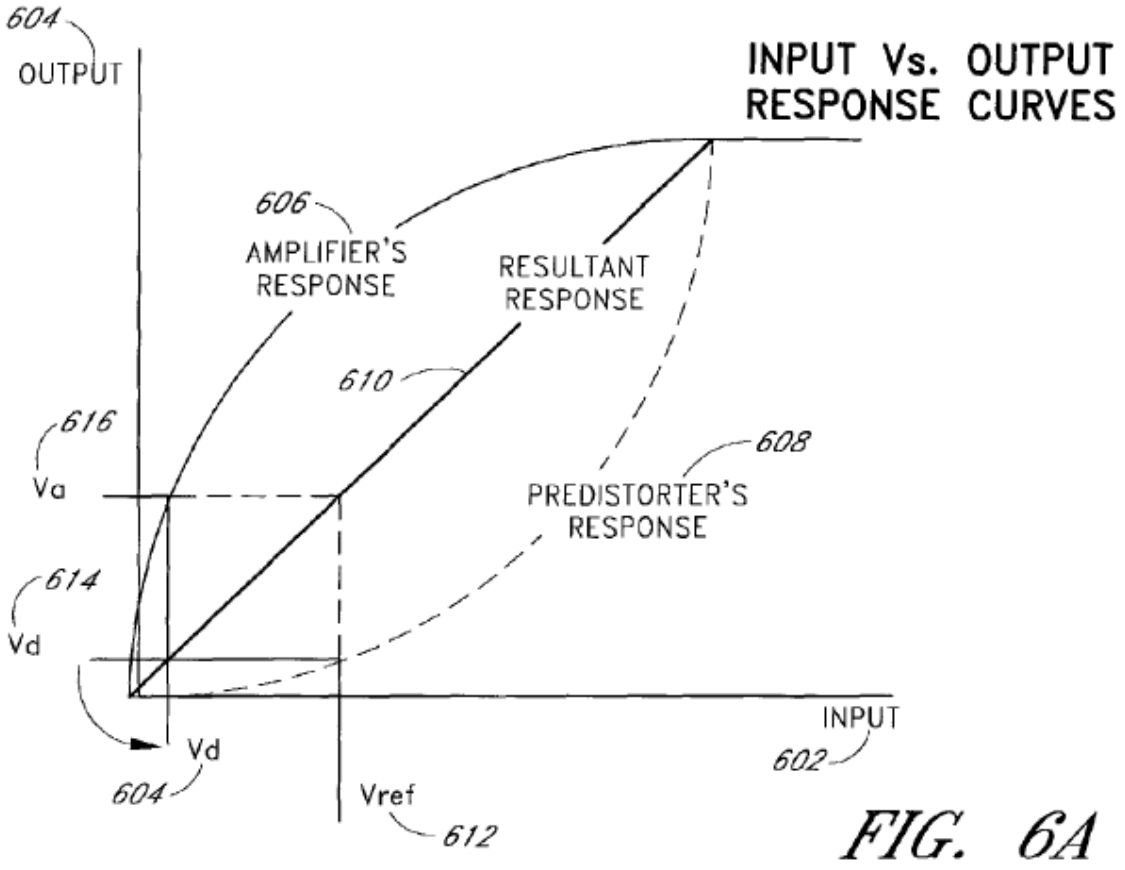


Figure 6A of Wright depicts "a chart of input vs. output response curves." *Id.* at 13:9–10, Fig. 6A.

As depicted in Figure 6A, an input magnitude 602 is indicated along a horizontal axis, where the "input" in Figure 6A corresponds to the input of a predistorter, as well as to the input to a power amplifier. *Id.* at 13:10–14. As also depicted in Figure 6A, an output magnitude 604 is indicated along a vertical axis, where the "output" in Figure 6A corresponds to the output of the predistorter, as well as to the output of the power amplifier. *Id.* at

13:14–17. Figure 6A illustrates a convex amplifier response 606, which eventually reaches a saturated value, where no additional output power can be supplied/generated by the amplifier irrespective of how hard the input signal level is driven. *Id.* at 13:17–22. "The [ ] diagram also illustrates how a cascade of a concave predistortion response 608 can result in an overall linear response 610." *Id.* at 13:22–24.

As further depicted in Figure 6A, "an input reference signal V_{ref} 612 is mapped by the concave predistortion response 608 to a significantly lower level predistortion signal V_d 614." *Id.* at 13:26–29. "The signal level of the input reference signal V_{ref} 612 is mapped by the concave predistortion response 608 to a value shown by the vertical axis of Figure 6A." *Id.* at 13:29–32. "The predistortion signal V_d 614 is then applied as an input to the amplifier as represented by the convex amplifier response 606, which transfers to an output level V_a 616." *Id.* at 13:32–35. "This output level V_a 616 is approximately identical to that provided by a pure linear response driven with the original input reference signal V_{ref} 612. *Id.*" at 13:35–37.

4. Independent Claim 13

a. Petitioner's Initial Contentions

[13.0] "A method for converting digital inputs of N bits in parallel into modulated optical streams, comprising:"

Petitioner contends that, "[t]o the extent the preamble is limiting, Roberts renders it obvious" because "Roberts teaches a method for using an optical modulator to convert an input digital data signal x(m) ('*digital inputs of N bits*') into an optical communications signal ('*modulated optical streams*')." Pet. 34; *see id.* at n.4.

According to Petitioner, "[a] POSITA would have found it obvious for Roberts' input digital data signal x(m) to include '*digital inputs of N bits*

in parallel' as claimed." *Id.* at 35 (citing Ex. 1003 ¶ 216). Petitioner contends that "Roberts's x(m) signal used to 'generate[] a pair of **multi-bit** sample streams V(n) which are representative of the desired phase modulation to be applied to each branch of an MZ modulator 4,' which suggests that x(m) includes a plurality of bits." *Id.* (citing Ex. 1005, 6:57–59).

Petitioner contends that, "[i]n the case where Roberts's DSP implements a non-linear compensation function as taught by Taraschuk, it would have been obvious for the input to the DSP to include a plurality of input bits in parallel as explicitly taught by Taraschuk." *Id.* at 36. Petitioner further contends that "Taraschuk teaches a 'linearizer 44' that receives 'input digital signal 46' that is an 'M-bit digital signal' where 'M=6.'" *Id.* (citing Ex. 1006, 6:56–7:4); *see id.*, n.5. Petitioner further contends that, "[b]ecause Roberts teaches that the DSP includes a 'non-linear compensator 18' that, like Taraschuk's linearizer, is used to compensate for non-linearities of a Mach-Zehnder optical modulator, a POSITA would have found it obvious for Roberts' DSP to receive a 6-bit digital input signal as taught by Taraschuk." *Id.* at 37 (citing Ex. 1005, 6:34–37; Ex. 1006, 6:56–58, 7:59–67, Fig. 5; Ex. 1003 ¶¶ 217, 219, 220).

[13.1] "inputting into an optical modulator a digital input,"

In Roberts' Figure 4, Petitioner points out that "the *optical modulator* receives a *digital input* by way of 'input digital data signal x(m).'" Pet. 38 (citing Ex. 1005, 1:32–33; Fig. 4; Ex. 1003 ¶ 217). According to Petitioner, "[i]t would have been obvious to a POSITA for Roberts' input digital data signal x(m) to include various digital inputs depending on how many bits comprise the x(m) signal." *Id.* at 38–39 (citing Pet. 39, n.6). Petitioner further contends that "[i]n the case of Taraschuk's six-bit input example, as

described above in [13.0], a '*digital input*' may be a six-bit value." *Id.* at 39 (citing Ex. 1003 ¶ 222).

[13.2] "wherein the digital input is one from a set of 2^N digital inputs that each has N bits of digital data, and"

Petitioner contends that "a POSITA would have found it obvious for a digital input provided by the x(m) signal to be *from a set of 2^N digital inputs* since Roberts describes x(m) as a 'digital' signal." Pet. 40 (citing Ex. 1005, 1:33). "Roberts recognizes that binary signals were a known type of digital signal." *Id.* (citing Ex. 1005, 1:61–64; 6:40–41 ("variously referring to sample streams Vx(n) as 'digital' and 'binary signal[s]')). According to Petitioner, "[a] POSITA would have therefore found it obvious for input digital signal x(m) to be a binary signal." *Id.* Petitioner contends that "[t]he set of possible inputs is calculated by raising two (the number of possible values for each bit) to a power of N (the number of bits in the signal)." *Id.* According to Petitioner, "[a] six-bit input, such as the one described by Taraschuk, would have $2^6 = 64$ possible inputs," and thus, "it is an obvious mathematical concept that a binary digital input having N bits is *one from a set of 2^N digital inputs*." *Id.* (citing Ex. 1003 ¶ 225); *see id.* at 39–40 (citing Ex. 1003 ¶¶ 224–226).

[13.3] "wherein N>l; and"

According to Petitioner, "[a]s discussed at [13.0], Taraschuk teaches a linearizer that maps a 6-bit input signal ($N = 6$) to an 8-bit output signal ($M = 8$)." Pet. 40–41 (citing Ex. 1006, 6:56–7:4); *see id.* at 41, n.7.

[13.4] "mapping, based on a digital-to-digital mapping, the digital input to a first digital output associated with M drive voltages,"

Petitioner contends that

First, Roberts describes a digital signal processor (DSP) 34 that receives an input digital data signal x(m) and produces two multi-bit sample streams $V_L(n)$ and $V_R(n)$, identified generically as $V_X(n)$. . . . Roberts teaches that the DSP comprises a non-linear compensator: "If desired, the DSP 34 may incorporate the functionality of the digital filter 16 and **non-linear compensator 18** of the complex driver 14 described above with reference to FIG. 2."

Second, Taraschuk teaches that a linearizer (i.e., non-linear compensator) maps ("*digital-to-digital mapping*") a 6-bit digital input signal ("*digital input*") to an 8-bit digital output signal ("*a first digital output*"). "**The linearizer 44** is designed in a known manner (e.g., using a random access memory look-up table) **to map an M-bit digital signal 46 into an N-bit parallel digital signal 6** for processing by the phase aligner 14 and vector summation block 16."

Taraschuk describes both the 6-bit and 8-bit signals as "digital" signals. . . . A POSITA would have therefore recognized that the mapping between the two is a *digital-to-digital mapping*. Fig. 5 of Taraschuk illustrates that the linearizer outputs the 8-bit digital signal. Accordingly, a POSITA would have recognized that the 6-bit digital input signal is converted into the 8-bit digital output signal based on the mapping.

. . . .

Third, a POSITA would have found it obvious for the bits of the digital output signal to be associated with *drive voltages*, as evidenced by Roberts. Roberts teaches that the DSP outputs multi-bit $V_R(n)$ and $V_L(n)$ signals (generically referred to as $V_X(n)$) and explains that the bits of such signals are representative of voltages to be applied to respective electrodes. "Each multi-bit sample stream $V_X(n)$ may be an N-bit parallel binary signal output from the DSP 34 on a corresponding N-bit data bus 36. In such a case, each line 38, of the N-bit bus 36 is connected to control a number of electrodes 40 corresponding to its binary weight." . . . "Since each active electrode receives the same voltage (corresponding to logic state '1'), it follows that the

> total phase delay experienced by light traversing each branch will vary directly with the number of active electrodes on that branch, and thus the value of the corresponding multi-bit sample stream $V_X(n)$."

Pet. 41–44 (citing Ex. 1005, 1:58–63, 5:56–60, 6:31–33, 6:40–54, 7:35–44; Ex. 1006, 6:56–7:4; Ex. 1003 ¶¶ 228–231, 233) (footnote omitted).

> *[13.5] "wherein the first digital output is one from a set of digital outputs that each has M bits of digital data, wherein the set of digital outputs comprises 2^M digital outputs,"*

Petitioner contends that "Roberts teaches outputting $V_R(n)$ and $V_L(n)$ signals (generically referred to as $V_X(n)$), where $V_X(n)$ is a multi-bit parallel binary signal ('*first digital output … has M bits of digital data*')." Pet. 46 (citing Ex. 1003 ¶ 237). Petitioner further contends that "a POSITA would have found it obvious for the signal $V_X(n)$ to be *one from a set of digital outputs … wherein the set of digital outputs comprises 2^M digital outputs* since Roberts describes $V_X(n)$ as a 'multi-bit … parallel binary signal.'" *Id.* (citing Ex. 1005, 6:40–42). According to Petitioner, "it is an obvious mathematical concept that a binary digital output having M bits is *one from a set of … 2^M digital outputs*." *Id.* (citing Ex. 1003 ¶¶ 238, 239).

> *[13.6] "and wherein M>=N,"*

Petitioner contends that "Taraschuk teaches a linearizer that maps a 6-bit input signal ($N = 6$) to an 8-bit output signal ($M = 8$)." Pet. 46 (citing Ex. 1006, 6:56–7:4; Pet. 46, n.9); *see id.* at 47 (citing Ex. 1003 ¶ 240).

> *[13.7] "wherein the digital-to-digital mapping comprises, for each digital input included in the set of 2^N digital inputs, a mapping to a corresponding digital output included in the set of digital outputs,"*

Petitioner contends that

> A POSITA would have considered it obvious for Roberts to map between digital inputs and digital outputs using a look-up table as taught by Taraschuk, where the look-up table includes entries for a set of inputs ("*set of 2^N digital inputs specified in the digital-to-digital mapping*") are mapped to a respective set of outputs ("*digital outputs corresponding to … digital inputs*"). . . . Taraschuk teaches that "a mapping can be defined between the M-bit input digital signal 46 and an N-bit signal … which compensates for the combined non-linear effects of … the sinusoidal response of the modulator 52" such that the response of the optical modulator is "more nearly linear."
>
> . . . [A] POSITA would have understood that the lookup table described by Taraschuk would have mapped a linear set of inputs to a non-linear set of outputs designed to exactly counteract the non-linear, sinusoidal response of the modulator.

Pet. 48–49 (citing Ex. 1006, 7:61–67, 8:13–15; Ex. 1003 ¶¶ 243–244 ("explaining a POSITA's understanding of the sinusoidal response curve and desired linear output"), 245).

Petitioner points to Wright and contends that

> Wright explains how the linearizer's response curve is configured to counteract the natural response of the amplifier such that, in tandem, they produce a linear amplifier response to an input voltage. . . . As Wright confirms, those of skill in the art were also familiar with using a "predistortion lookup table" to store information mapping input and output values for a nonlinear compensation circuit.

Id. at 50 (citing Ex. 1009, 5:27–30, 13:9–37; Ex. 1003 ¶¶ 80–83; Ex. 1024, Fig. 4). According to Petitioner, "[a] POSITA would have been familiar with the design of non-linear compensation devices and associated lookup tables," which "had long been used in linearizing the output of other nonlinear devices—including RF amplifiers." *Id.* (citing Ex. 1003 ¶ 248).

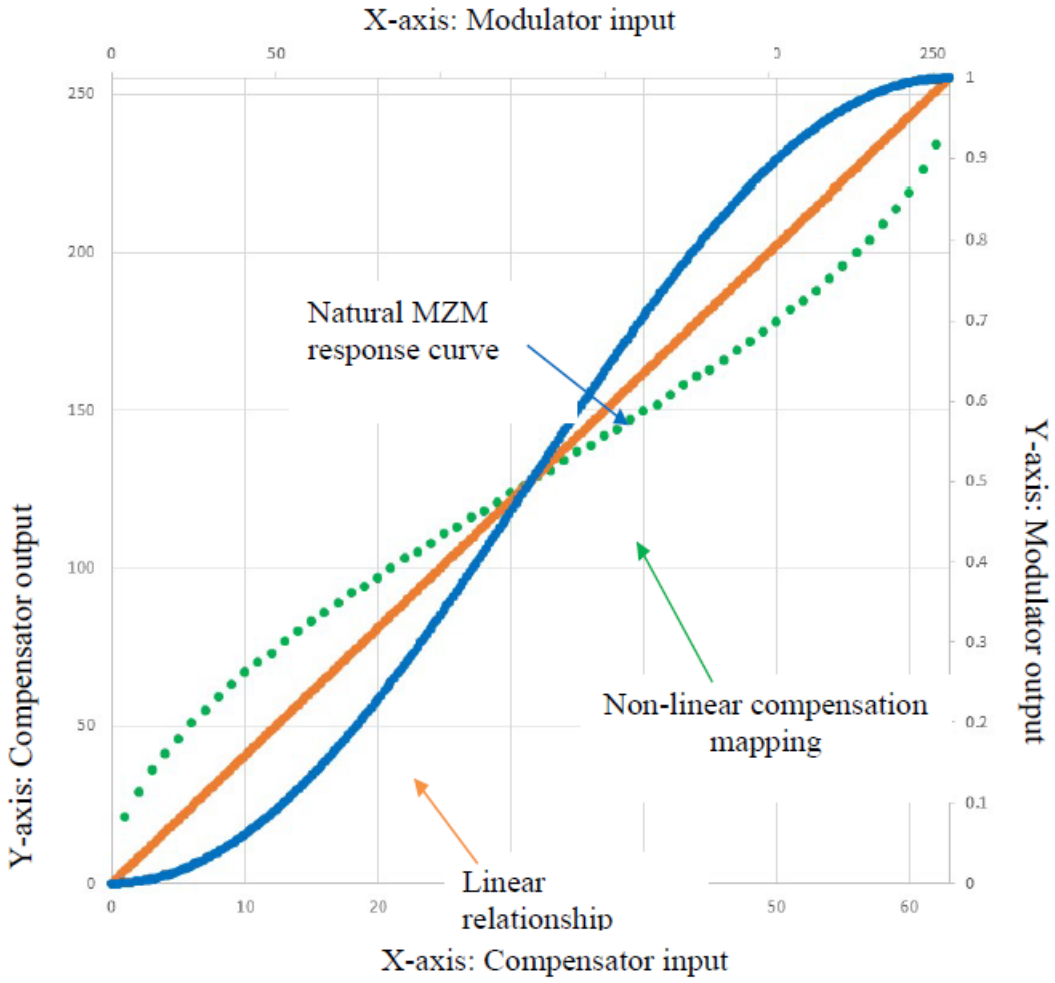
Petitioner cites Dr. Blumenthal's modeling of the natural sinusoidal response curve of an MZM and "calculating [of] a non-linear compensation function to counteract the sinusoidal response curve." *Id.* at 50–51 (citing Ex. 1003 ¶¶ 249–256). According to Petitioner, "Dr. Blumenthal's analysis produces . . . [a] mapping table based on a generic sinusoidal response curve and Taraschuk's example of a 6-bit to 8-bit linearizer." *Id.* at 51; *see id.* at 52–53 (showing a looking up table mapping 2^6 input values, 0 to 63, to 2^8 output values, 0 to 255).

According to Petitioner, "[i]t would have been obvious for a POSITA implementing a nonlinear compensation lookup table, as suggested by Taraschuk, to use such known techniques for computing non-linear compensator look-up table values." *Id.* at 54 (citing Ex. 1003 ¶ 257). Petitioner explains that "[w]hile a POSITA implementing an actual compensator for a real MZM would have used measurements from that MZM, testing an MZM and gathering response curve information was within the ordinary knowledge and skill set of engineers in the prior art period." *Id.*

> *[13.8] "wherein, for a first subset of successively decreasing digital inputs in the set of 2N digital inputs specified in the digital-to-digital mapping, deltas between numerical values of digital outputs in the set of digital outputs corresponding to the successively decreasing digital inputs in the first subset decrease, and"*

Petitioner cites Dr. Blumenthal's graph of "compensator mapping . . . (in green), with compensator input values on the lower horizontal axis, and compensator output values on the left vertical axis." Pet. 55 (citing Ex. 1003 ¶ 261). According to Petitioner "[i]t is immediately apparent that the curve of the compensation mapping appears as a mirror-image of the natural MZM

response curve." *Id.* at 55–56 (citing Ex. 1003 ¶ 261). Reproduced below is Dr. Blumenthal's graph of compensator mapping and the natural MZM sinusoidal responsive curve.



Dr. Blumenthal's graph depicting a natural, sinusoidal MZM response curve, as well as input and output values of a non-linear compensation mapping curve. *Id.* at 56 (citing Ex. 1003 ¶ 261).

According to Petitioner, the graph "shows the natural MZM response curve (in blue) using the upper horizontal axis and the right vertical axis." *Id.* (citing Ex. 1003 ¶ 261).

Petitioner also presents a chart, reproduced below, including a "'first subset' of input values 60 to 63, and arranging those look-up table entries as 'decreasing digital inputs,' show[ing] that the absolute value difference between successive output values decreases ('deltas … decrease')." *Id.* at 57 (citing Ex. 1003 ¶ 262) (emphasis omitted).

Linearizer input	Linearizer output	Delta
63	255	21
62	234	8
61	226	7
60	219	

Petitioner's chart depicting decreasing delta values between output values mapped with successively decreasing input values. *Id*.

Petitioner explains that "between successive values 63, 62, 61, and 60, the deltas decrease from 21 to 8 to 7." *Id.* Petitioner contends that "[t]his result follows naturally from the observation that the nonlinear compensation must counteract the nonlinear response of the MZM, which is sinusoidal." *Id.* According to Petitioner, "[t]o counteract the MZM's sinusoidal response, it would have been obvious for a corresponding nonlinear compensation lookup table to have output values whose successive differences decrease ('deltas… decrease')." *Id.* (emphasis omitted).

> *[13.9] "wherein, for a second subset of successively decreasing digital inputs in the set of 2^N digital inputs specified in the digital-to-digital mapping, deltas between numerical values of digital outputs in the set of digital outputs corresponding to the successively decreasing digital inputs in the second subset increase."*

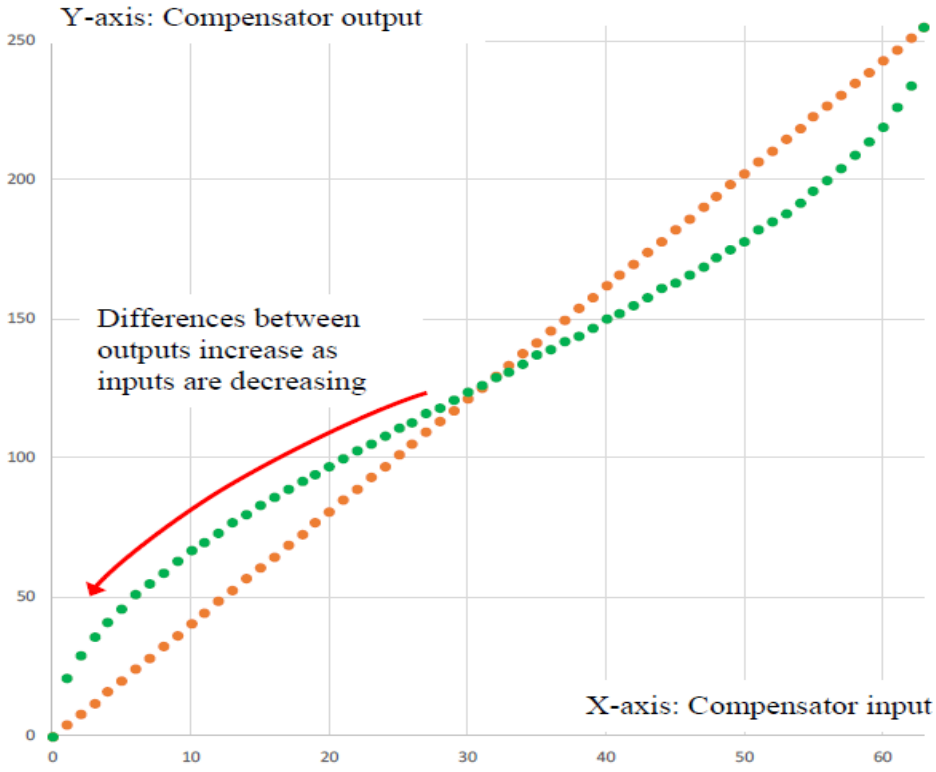
Petitioner contends that "[t]he obvious linearizer mapping table in [13.7] shows subsets where the deltas of successively decreasing outputs

increase," and that, "the input values are successively decreasing from 3 to 0, the corresponding deltas increase from 7 to 8 to 21." Pet. 61.

Linearizer input	Linearizer output	Delta
3	36	7
2	29	8
1	21	21
0	0	

Petitioner's chart depicting increasing delta values between output values mapped with successively decreasing input values. *Id.*

Petitioner contends that "[t]his increasing delta feature is similarly visible in the response curve of the nonlinear compensation mapping." *Id.* (citing Ex. 1003 ¶ 269).



Dr. Blumenthal's graph depicting non-linear compensator input values that are mapped to output values. *Id.* at 62 (citing Ex. 1003 ¶ 269).

Petitioner relies on Wright to provide "an example of a 'known manner' for determining the values for a non-linear compensation look-up table." Pet. 79–80. According to Petitioner, "[a]s shown in [Wright's] Fig. 6A, one way for a predistortion circuit to counteract the nonlinear response curve of a device is for . . . [it] to have a response curve that is a mirror image of the device's nonlinear response curve [reflected] across the desired linear-response line." *Id.* at 78 (citing Ex. 1009, 13:9–37). Petitioner explains that "[t]his reflected-response curve feature follows from the way the desired response curve of the predistortion circuit can be derived by working backwards from the nonlinear device's response curve and the desired linear response." *Id.* at 78–79 (citing Ex. 1003 ¶¶ 78–83, 326).

b. Patent Owner's Response Arguments

Patent Owner argues that "*Taraschuk's* disclosures are directed to compensating 'for the combined non-linear effects of ***logic level mismatches through the D/A converter 12 and*** the sinusoidal response of the modulator 52.'" PO Resp. 33 (quoting Ex. 1006, 7:61–67). Patent Owner further argues that Petitioner omitted this disclosure from its Petition and that "[t]he omitted disclosure suggests a combined compensation that accounts for logic level mismatches in the D/A converter as well as the real response curve of the modulator, not the separate idealized sinusoidal graphs Dr. Blumenthal calculates." *Id.* at 33–34. Dr. Dallesasse testifies that "[t]here is no disclosure in *Taraschuk* about the possibility of compensating the 'sinusoidal response of the modulator' alone, as Dr. Blumenthal does in his calculations in his declaration." Ex. 2018 ¶ 49 (citing Ex. 1003 ¶¶ 250–256), 85, 86, 104, 105. According to Patent Owner, "[Petitioner] and Dr. Blumenthal [also] do not point to a single disclosure of *Taraschuk* that could suggest the calculations of idealized response curves or derivation of table

values that Dr. Blumenthal performs." PO Resp. 32 (citing Pet. 49–62, 65–70; Ex. 1003 ¶¶ 245–269, 305–314).

Patent Owner also asserts that "[w]hat *Taraschuk* actually describes as an input into its mapping computation is an analog sample detected and fed back from the modulator output—***not*** graphs drawn by and derived table values calculated by Dr. Blumenthal." PO Resp. 35 (citing Ex. 2018 ¶¶ 48, 85–86, 89). "*Taraschuk* actually teaches away from the approach, and its complicated derivation, that Cisco and Dr. Blumenthal claim that a person of skill would adopt." *Id.* (citing Ex. 2018 ¶¶ 49, 86–87).

c. Petitioner's Reply Arguments

Petitioner responds that

> Patent Owner faults Dr. Blumenthal's modeled sinusoidal response curve because it doesn't factor in the "logic level mismatches" described by Taraschuk. . . . But there was no reason to do so, and Patent Owner's argument is untethered from the claim language. The claims do not recite compensating for logic level mismatches. *Thus, whether logic level mismatches are compensated—or even present in the Roberts-Taraschuk [and Wright] combination—does not matter*.

Pet. Reply 14 (citing PO Resp. 33–35) (emphasis added).

Petitioner further responds that

> Patent Owner argues that Taraschuk "accounts for logic level mismatches in the D/A converter as well as the real response curve of the modulator, not the separate idealized sinusoidal graphs Dr. Blumenthal calculates." . . . But the proposed combination does not bodily incorporate Taraschuk's entire system (logic-level mismatch compensation included) into Roberts. Rather, the proposed combination is that a POSITA would have found it obvious for Roberts' DSP and non-linear compensator to use a look-up table (as described for Taraschuk's 6-bit to 8-bit linearizer) to perform the *mapping*.

> Patent Owner quotes Dr. Dallesasse asserting that Taraschuk does not suggest "compensating the 'sinusoidal response of the modulator' alone." . . . As the petition pointed out, however, Taraschuk does make that suggestion, describing a linearizer for "**compensating non-linearities of** the A/D converter (and/or **the optical modulator** 52)."

Id. at 14–15 (citing PO Resp. 33–34; Pet. 28–34; Ex. 2018 ¶ 49; Ex. 1006, 8:49–53; Ex. 1003 ¶ 117).

d. Analysis of the Parties' Arguments

We are persuaded Petitioner does not sufficiently rebut Patent Owner's contentions that Dr. Blumenthal's idealized sinusoidal compensation curves are not representative of Tarschuk's teachings. In our Institution Decision we stated that

> [i]t remains a factual issue to be developed during trial as to whether the idealized, natural sinusoidal response curves derived by Dr. Blumenthal are representative of "***the combined non-linear effects of logic level mismatches through the D/A converter 12 and*** the sinusoidal response of the modulator 52'" disclosed by Taraschuk. . . . We invite the parties to fully brief this issue during trial.

Inst. Dec. 34 (citing Prelim. Resp. 49 (citing Ex. 1006, 7:61–67)) (emphasis added).

Petitioner responded that "[a]s the petition pointed out, however, Taraschuk does make that suggestion, describing a linearizer for '**compensating non-linearities of** the A/D converter (and/or **the optical modulator** 52).'" Pet. Reply 15 (quoting Ex. 1006, 8:49–53; Pet. 28; Ex. 1003 ¶ 117). But this portion of Taraschuk is only cited in the section of the Petition that summarizes Taraschuk. Pet. 28 (Section X.B.2, "Summary of Taraschuk"). Petitioner does not cite column 8, lines 49–53 with respect to claim 13 or any of the elements recited therein. Instead, Petitioner cites

column 7, lines 61–67, which discloses that a "mapping can be defined between the M-bit input digital signal 46 and an N-bit signal 6 processed by the phase aligner 14 and vector summation block 16, which compensates for the combined non-linear effects of logic level mismatches through the D/A converter 12 and the sinusoidal response of the modulator 52." Pet. 48 (citing Ex. 1006, 7:61–67, 8:13–15 ("The combined response of the D/A converter and optical modulator is more nearly linear, and can more easily be corrected by an MxN mapping in the linearizer 44."); Ex. 1003 ¶¶ 243, 244). As such, we do not consider Petitioner's citation to column 8, lines 49–53 of Taraschuk with respect to limitations 13.8 and 13.9.

We agree with Patent Owner's argument that the portions of Taraschuk in column 7, lines 61–67 and column 8, lines 13–15 cited by Petitioner in its challenge to claim 13 teach "an end-to-end approach" "because that calculation involves predistortion of the input M-bit word by subtracting a digitized analog sample of the ultimate output," and as such, teach "[a]n approach that necessarily does one combined correction for all of the nonlinearities that occur in-between those ends—whether bit mismatches in the digital logic or non-linearities in the Mach-Zehnder modulator." PO Sur-reply 18 (citing PO Resp. 30–36; Ex. 2018 ¶¶ 48, 49, 85–87, 89, 103; Ex. 1006, 7:34–39, 7:61–67).

We further agree with Patent Owner's assertion that

> [Patent Owner] and Prof. Dallesasse are not suggesting that Dr. Blumenthal should model the logic-level mismatches. But rather pointing out that calculating an idealized sinusoidal response in isolation is not obvious (or flowing naturally) from a reference that can only deal with compensating the combined response of the modulator and digital logic mismatches together—via real-time pre-distortion fed back from the ultimate output and subtracted from the input.

Id. at 19 (citing Ex. 2018 ¶¶ 49, 85–87) (emphasis omitted). In support, Dr. Dallesasse testifies that

> Dr. Blumenthal starts with the premise that all that is required is deriving a complementary function to the sinusoidal response. . . . But this ignores that the disclosure of *Taraschuk* describes compensating "the sinusoidal response of the modulator" ***and*** "logic level mismatches through the D/A converter" ***together***. . . . Dr. Blumenthal's complementary sinusoidal correction curve won't do that. The combined non-linearity from the multiple sources likely won't simply be evenly sinusoidal. *Taraschuk* does not disclose, or in my opinion render obvious, any pre-calculation solution. (*Taraschuk* mentions a real-time analog feedback loop to pre-distort, which would not involve pre-calculation.) And it certainly does not suggest one that could deal with the combined and likely complex non-linearities described.

Ex. 2018 ¶ 85 (citing Ex. 1006, 7:61–67).

Even if we did consider Petitioner's citation to column 8, lines 49–53 in the section of the Petition summarizing Taraschuk, Patent Owner notes that, in its Reply, Petitioner "cites to an instance of 'and/or' in the Taraschuk specification" with respect to "compensating non-linearities of the A/D converter (and/or the optical modulator 52)," and Patent Owner persuasively argues that "that disclosure refers to Fig. 7, which has the same end-to-end predistortion calculation as Figs. 5 and 6, none of which are able to isolate and correct for modulator non-linearity effects alone." PO Sur-reply 19, n.2 (citing Pet. Reply 15; Ex. 1006, 8:29–30, 8:49–53, Fig. 7) (emphasis omitted).

As Petitioner fails to sufficiently support its position that Dr. Blumenthal's idealized sinusoidal curves are representative of Taraschuk's teachings, Petitioner does not sufficiently carry its burden to show that the combination of Roberts, Taraschuk, and Wright teaches or even suggests

either limitation 13.8 or limitation 13.9. This is because the idealized sinusoidal curves that form the basis of Dr. Blumenthal's analysis lack a sufficient showing of relevance to the teachings of Taraschuk cited by Petitioner.

Patent Owner persuades us that Petitioner does not point to any basis for a LUT having the recited deltas except for Dr. Blumenthal's analysis. Although Wright *generally* teaches compensating for mismatches, Dr. Blumenthal's analysis fills in limitations 13.8 and 13.9—Petitioner does not set forth a sufficiently supported reason for using the specific values recited in limitations 13.8 and 13.9. At best, Petitioner presents an "obvious to try rationale":

> In addition to the reasons mentioned above, a POSITA would have found it obvious to try a mapping scheme in which entries in the look-up table as taught by Taraschuk are selected such that successively decreasing inputs correspond to digital output entries with either decreasing, increasing, or similar deltas between their values. . . . Doing so would have involved choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success. In that regard, the deltas between values of the corresponding digital outputs can either increase, decrease, or stay the same. Accordingly, there are only three possible relationships between deltas of successive digital outputs. With so few possibilities, a POSITA would have found it obvious to try each of them.

Pet. 59 (citing Ex. 1003 ¶ 265). The analysis for 13.8 is incorporated by reference in 13.9. *See* Pet. 60. Although there are three possible relationships between *two*, consecutive deltas, there are many possible sequences of deltas—Petitioner does not sufficiently show a finite number of solutions in its challenge.

Moreover, Petitioner's Reply includes positions not supported by a Reply Declaration from Dr. Blumenthal and thus, constitute attorney argument that is not sufficiently supported by evidence. *See e.g.*, Pet. Reply 16 (Petitioner arguing "Roberts' design obviates the need for a separate, discrete DAC (*compare* Ex.1005, Fig. 2 *to* Fig. 4), so Patent Owner's arguments about logic level mismatches in a DAC are a red herring"); *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984) (lawyer arguments and conclusory statements which are unsupported by factual evidence are entitled to little probative value).

For the foregoing reasons, we determine that Petitioner does not establish, by a preponderance of the evidence, that the combination of Roberts, Taraschuk, and Wright teaches or suggests the combination of features recited in independent claim 13, and in particular, does not teach or suggest limitations 13.8 or 13.9.

5. Independent Claim 23

With respect to independent claim 23, Petitioner cites, in large part, its analysis for independent claim 13. Pet. 64–70 (citing-in-part Ex. 1003 ¶¶ 297–314). Patent Owner appears to address independent claims 13 and 23 together. *See e.g.*, PO Resp. 8–9. For these reasons, our analysis for independent claim 13 is substantially applicable to independent claim 23. Accordingly, we determine Petitioner does not establish, by a preponderance of the evidence, that the combination of Roberts, Taraschuk, and Wright teaches or suggests the combination of features recited in independent claim 23.

6. Dependent Claims 14 and 24–29

Petitioner's showing with respect to dependent claims 14 and 24–29 does not cure the deficiencies noted above with respect to independent

claims 13 and 23. As such, we determine that Petitioner does not establish, by a preponderance of the evidence, that the combination of Roberts, Taraschuk, and Wright teaches or suggests the combination of features recited in dependent claims 14 and 24–29.

Further, with regard to claim 27, which recites "for a given digital input in the set of 2^N digital inputs, the mapping to a corresponding digital output is determined based on a pattern for actuating drive voltages that alters the linearity of an optical response of the optical modulator," the parties substantially reiterate positions taken in IPR2022-00575. In that Decision, we determined that Petitioner did not carry its burden to show, by a preponderance of the evidence, that the combination of Taraschuk and Roberts teach substantially similar limitations of independent claims 1, 11, and 15 of the '872 patent. In particular, we found that

> Petitioner cannot ignore these teachings of Taraschuk and consider only the portions that support its challenge. *See* Pet. Reply 17 (citing Pet. 43–45; Ex. 1006, 7:56–60) ("Patent Owner's emphasis on Taraschuk's digital feedback loop is also misplaced because the Petition *simply relied on Taraschuk's linearizer 44* as a *discrete*, known device for performing non-linear compensation of a Mach-Zehnder modulator." (emphasis added)). Petitioner cannot set forth the teachings of Taraschuk in such a piecemeal fashion, and view these teachings in a vacuum. As Petitioner fails to sufficiently explain why the converter of Taraschuk relies on analog pre-distortion, or explain why analog pre-distortion is encompassed by the invention recited in independent claim 1, Petitioner does not sufficiently carry its burden.

Cisco Systems, Inc. v. Ramot at Tel Aviv University, IPR2022-00575, Paper 33 at 25–26 (PTAB September 29, 2023) (Final Written Decision). In that Decision, we determined that "Petitioner's Reply includes positions not supported by a Reply Declaration from Dr. Blumenthal" because "Petitioner

supports neither its contention that '[i]n the combination with Roberts, [Taraschuk's] linearizer 44 *could be used either with or without a feedback loop*,' nor its contention that '[a] *feedback loop is not necessary* because "the mapping implemented by the linearizer 44 may be calculated in advance"' with the testimony of Dr. Blumenthal or disclosures from Roberts, Taraschuk, or any other contemporaneous reference." *Id.* at 26. Thus, we determined that "Petitioner's arguments constitute attorney argument that is not sufficiently supported by evidence." *Id.* (citing Pet. Reply 17–18; *In re De Blauwe*, 736 F.2d 699, 705 (Fed. Cir. 1984)). We make the same determinations, in the present proceeding, with respect to claim 27.

E. Obviousness over Roberts and Taraschuk

Petitioner argues that claims 13, 14, and 23–29 would have been obvious in view of Roberts and Taraschuk. Pet. 25–77. For this ground of unpatentability, Petitioner does not include Wright in the combination of prior art references, instead relying on Wright as evidence of the background knowledge of the POSITA. Patent Owner disagrees. PO Resp. 25–36, 50–54. The omission of Wright does not cure the deficiencies of Petitioner's challenge as set forth above with respect to the combination of Roberts, Taraschuk, and Wright. *Supra* § III.D.4.d. Accordingly, we reach the same determination here, that Petitioner does not establish, by a preponderance of the evidence, that the combination of Roberts and Taraschuk teaches or suggests the combination of features recited in any of claims 13, 14, and 23–29.

F. Patent Owner's Motion to Exclude

Patent Owner timely objected to Petitioner's Reply evidence (Paper 25) and thereafter filed a Motion to Exclude Exhibits 1026–1033. Paper 33 ("Mot. Ex."). Petitioner opposed Patent Owner's Motion to Exclude (Paper

34, "PO Opp. Ex."), and Patent Owner replied to Petitioner's Opposition (Paper 35, "Pet. Reply Ex."). We dismiss Patent Owner's Motion to Exclude as moot.

G. Patent Owner's Objections to Demonstratives

Patent Owner objected to certain portions of Petitioner's demonstratives. Paper 36. As the parties' demonstratives are not evidence, we do not cite them or otherwise rely on them in this Decision. As such, we dismiss Patent Owner's objections to Petitioner's demonstratives as moot.

IV. CONCLUSION

In summary:

Claims Challenged	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
13, 14, 23–29	103(a)	Roberts, Taraschuk		13, 14, 23–29
13, 14, 23–29	103(a)	Roberts, Taraschuk, Wright		13, 14, 23–29
Overall Outcome				13, 14, 23–29

V. ORDER

For the reasons given, it is:

ORDERED that Petitioner has not established, by a preponderance of evidence, that any of claims 13, 14, and 23–29 of the '872 patent are unpatentable as obvious under 35 U.S.C. § 103;

FURTHER ORDERED that Patent Owner's Motion to Exclude is dismissed as moot;

FURTHER ORDERED that Patent Owner's objections to Petitioner's demonstratives are dismissed as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Paper 46
Entered: February 29, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-00576
Patent 11,133,872 B2

Before MONICA S. ULLAGADDI, CHRISTOPHER L. OGDEN, and JASON M. REPKO, *Administrative Patent Judges.*

Opinion for the Board filed by Administrative Patent Judge ULLAGADDI

Opinion concurring filed by Administrative Patent Judge OGDEN

ULLAGADDI, *Administrative Patent Judge*.

DECISION
Denying Petitioner's Request on Rehearing
of the Final Written Decision
37 C.F.R. § 42.71

I. BACKGROUND

Cisco Systems, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting *inter partes* review of claims 13, 14, and 23–29 ("the challenged claims") of U.S. Patent No. 11,133,872 B2 (Ex. 1001, "the '872 patent"), accompanied by the supporting Declaration of Dr. Daniel J. Blumenthal (Ex. 1003). Ramot at Tel Aviv University Ltd. ("Patent Owner") filed a Preliminary Response. Paper 8. In our Institution Decision, we instituted an *inter partes* review of each of the challenged claims on the grounds set forth in the Petition. Paper 10.

Patent Owner filed a Response (Paper 18, "Patent Owner's Response" or "PO Resp.") accompanied by the supporting Declaration of Dr. John Dallesasse (Ex. 2018), Petitioner filed a Reply to Patent Owner's Response (Paper 24, "Petitioner's Reply" or "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 31). On July 5, 2023, we held an oral hearing. A transcript of the hearing is of record. Paper 39. We issued a Final Written Decision. Paper 41 ("FWD").

Petitioner requests Rehearing of our Final Written Decision. Paper 42 ("Req. Reh'g"). Patent Owner's filed an Opposition. Paper 44. For the reasons set forth below, Petitioner's Rehearing Request is denied.

II. LEGAL STANDARDS

A party requesting rehearing bears the burden of showing that a decision should be modified. 37 C.F.R. § 42.71(d). The party must specifically identify all matters it believes the Board misapprehended or overlooked, and the place where each matter was addressed previously in a motion, an opposition, or a reply. *Id.* "A party may request rehearing on a decision by the Board on whether to institute a trial" and "[w]hen rehearing

a decision on petition, a panel will review the decision for an abuse of discretion." *Id.* § 42.71(c). A request for rehearing, therefore, is not an opportunity merely to disagree with the Board's assessment of the arguments or weighing of the evidence, or to present new arguments or evidence. *See, e.g.*, *Presidio Components, Inc. v. AVX Corporation,* IPR2015-01332, Paper 21 at 4 (PTAB Feb. 21, 2016) ("Patent Owner's arguments in this regard amount to a mere disagreement with our analysis or conclusion. But mere disagreement with our analysis or conclusion is not a sufficient basis for rehearing. It is not an abuse of discretion to provide analysis or conclusion with which Patent Owner disagrees.").

III. REHEARING ARGUMENTS

First, Petitioner argues that its proposed "idealized sinusoidal curves are not intended to represent Taraschuk's teachings—they are intended to represent Roberts' sinusoidal modulator" and thus, we "overlooked the Petition's position that the 'deltas' limitations are 'merely an obvious aspect of compensating for the nonlinear response curve of **Roberts' Mach-Zehnder modulator**.'" Req. Reh'g 3 (citing Pet. 55). Petitioner argues that "the Board overlooks Petitioner's reply argument that 'the proposed combination does not bodily incorporate Taraschuk's entire system (logic-level mismatch compensation included) into Roberts.'" *Id.* at 5 (citing Pet. Reply 15). According to Petitioner, "[a]s explained in reply, 'Roberts' design obviates the need for a separate, discrete DAC (compare Ex. 1005, Fig. 2 to Fig. 4), so Patent Owner's arguments about logic level mismatches in a DAC are a red herring.'" *Id.* at 5–6 (citing Pet. Reply 16).

Petitioner argues that we "overlooked Petitioner's reply argument that 'the proposed combination is that a POSITA would have found it obvious

for **Roberts' DSP and non-linear compensator** to use a look-up table (as described for Taraschuk's 6-bit to 8-bit linearizer) to perform the *mapping*." *Id.* at 6 (citing Pet. 29–34; Pet. Reply 15). Petitioner further contends that

> [t]he Petition then explains that: "A POSITA would have been motivated to apply Taraschuk's **mapping techniques** to Roberts' non-linear compensator to compensate for non-linear effects of the modulator." Taraschuk's mapping technique is "designed in a known manner (e.g., using a random access memory look-up table) **to map an M-bit digital signal 46 into an N-bit parallel digital signal**."

Req. Reh'g 7 (citing Ex. 1006, 6:61–65; Pet. 22, 31). According to Petitioner,

> the addition of Taraschuk merely provides the implementation detail of having more output bits than input bits, which may be achieved through a lookup table. The actual proposed combination—overlooked by the Board—thus "does not bodily incorporate Taraschuk's entire system (logic-level mismatch compensation included) into Roberts."

Id. at 8 (citing Pet. Reply 15); *see* Pet. 9, 51; Ex. 1005, 1:56; Ex. 1003 ¶255.

Petitioner contends, in its Reply, that

> the proposed combination does not bodily incorporate Taraschuk's entire system (logic-level mismatch compensation included) into Roberts. Rather, the proposed combination is that a POSITA would have found it obvious for Roberts' DSP and nonlinear compensator to use a look-up table (as described for Taraschuk's 6-bit to 8-bit linearizer) to perform the mapping.

Id. at 10 (citing Pet. 29–34; Pet. Reply 15). Thus, Petitioner contends that "as argued in reply, '[t]here was no need for Dr. Blumenthal to model the unclaimed concept of compensating for logic-level mismatches.'" *Id.* (citing Pet. Reply 14).

Second, Petitioner argues that by "misapprehending the proposed combination, the Board focused on the unclaimed concepts of how the

lookup table values are populated" and that "[t]he Petition does not incorporate Taraschuk's feedback loop because the feedback loop represents the unclaimed concept of how the lookup table values are populated." *Id.* at 11. Petitioner further argues "[t]he Board's decision thus overlooks that using the lookup table (to perform non-linear compensation) is distinct from populating the lookup-table values." *Id.* Petitioner contends that

> Taraschuk's feedback loop is not what performs compensation of the modulator. Rather, Taraschuk's feedback loop is merely the mechanism by which the linearizer lookup table values are populated. But again, the claims do not recite the mechanism by which the values of the lookup table ("digital-to-digital mapping") are populated. Instead, and as argued in reply, the claims recite what the digital-to-digital mapping produces.
>
> Because the proposed combination does not incorporate Taraschuk's feedback loop, or any other unclaimed mechanism for populating the lookup table values, the appropriate inquiry is not whether the exemplary lookup table values presented by Dr. Blumenthal are representative of Taraschuk's teachings.

Id. at 11–12 (citing Pet. Reply 8).

Petitioner further contends that "[t]he Board further relied on Patent Owner's argument that 'Taraschuk mentions a real-time analog feedback loop to pre-distort, which would not involve pre-calculation,'" but that such reliance is in error because "this position also overlooks that pre-calculation of the lookup table values is not a claimed step." *Id.* at 13 (citing Final Dec. 29).

Third, Petitioner contends that

> [t]he Board stated that "[a]lthough there are three possible relationships between two, consecutive deltas, there are many possible sequences of deltas." But the claims do not require any specific sequence of deltas. Rather, the claims merely require that one set of deltas increase, one set of deltas decrease, and one set of deltas stay the same. It would have thus been obvious that

> for any set of consecutive deltas derived from Roberts' mapping, the relationship between them would either increase, decrease, or be equal.

Req. Reh'g 17 (citing Final Dec. 30; Pet. 59). According to Petitioner, it "does not argue that the act of calculating the idealized curve 'follows naturally' from the references," but rather, that "[t]he existence of the claimed 'deltas' characteristics that results "naturally from non-linear compensation of a sinusoidal modulator response." *Id.* at 16–17 (citing Pet. Reply 14).

IV. ANALYSIS

With regard to Petitioner's *first* set of arguments, the record does not clearly and sufficiently support Petitioner's position. Portions of the Petition suggest that Petitioner intended to rely on "Roberts' DSP having a non-linear compensator" to which "Taraschuk's linearizer mapping technique" is applied. Pet. 33 (citing Ex. 1003 ¶ 114); *see also e.g.*, *id.* at 39 n.6 (annotating Roberts' "Fig. 4 to include both the actual *modulator 4 and DSP 34*" and offering "an alternative interpretation in which the 'optical modulator' is Roberts' *modulator 4 only*" (emphasis added)), 50, 55. Other portions of the Petition suggest that Petitioner intended to rely on Taraschuk's modulator 52:

> Taraschuk teaches that "a mapping can be defined between the M-bit input digital signal 46 and an N-bit signal . . . which compensates for the combined non-linear effects of . . . *the sinusoidal response of the modulator 52*" such that the response of the optical modulator is "more nearly linear."

Id. at 48 (citing Ex. 1006, 7:61–67, 8:13–15; Ex. 1003 ¶¶ 243–44), 73. Still other portions of the Petition reference the "process of modeling the sinusoidal response curve for *an* MZM and calculating a non-linear compensation function to counteract the sinusoidal response curve" and that

"Dr. Blumenthal's analysis produces . . . [a] mapping table based on *a generic* sinusoidal response curve and Taraschuk's example of a 6-bit to 8-bit linearizer." Pet. 51 (citing Ex. 1003 ¶¶ 249–256).

Further muddying the waters, Petitioner disputes Dr. Dallesasse's position that "Taraschuk does not suggest 'compensating the 'sinusoidal response of the modulator' alone'" (Pet. Reply 15 (citing PO Resp. 34)) and asserts that "[a]s the petition pointed out, . . . Taraschuk does make that suggestion, describing a linearizer for 'compensating non-linearities of the A/D converter (and/*or the optical modulator 52*)'" (*id.* (citing Ex. 1006, 8:49–53; Pet. 28; Ex. 1003 ¶ 117) (emphasis added)). *But see* Pet. Reply 16 (citing Ex. 2020, 115:19–21) ("Regardless, Roberts' design obviates the need for a separate, discrete DAC (compare Ex. 1005, Fig. 2 to Fig. 4), so Patent Owner's arguments about logic level mismatches in a DAC are a red herring. To the extent that there would be logic level mismatches at Roberts' modulator (which performs both digital-to-analog and electrical-to-optical conversions), those mismatches would also be correctable with Taraschuk's linearizer." (footnote omitted)).

Even assuming, *arguendo*, the trial record made sufficiently clear that Petitioner had intended to rely on Roberts' "DSP having a non-linear compensator," modulator 4 and DSP 34, or modulatory 4 only (*see* Pet. 33, 39 n.6), Petitioner's proposed combination is piecemeal. With regard to Petitioner's *second* set of arguments, in its Rehearing Request, Petitioner argues that "[t]he Petition does not incorporate Taraschuk's feedback loop because the feedback loop represents the unclaimed concept of how the lookup table values are populated." Req. Reh'g 11. Even if the concept of populating the lookup-table values is not explicitly recited in the claims, Petitioner's proposed combination constitutes piecemeal analysis if it

ignores Roberts' feedback loop and Taraschuk's feedback loop in favor of an empty table populated only by Dr. Blumenthal's analysis. *See id.*; *cf. id.* at 12 ("Because the proposed combination does not incorporate Taraschuk's feedback loop, or any other unclaimed mechanism for populating the lookup table values, the appropriate inquiry is not whether the exemplary lookup table values presented by Dr. Blumenthal are representative of Taraschuk's teachings.").

Despite Petitioner's argument that "the claims do not recite the mechanism by which the values of the lookup table ('digital-to-digital mapping') are populated," and that instead, "the claims recite what the digital-to-digital mapping produces," (Req. Reh'g 11 (citing Pet. Reply 8)), the prosecution history indicates that the method by which compensation occurs is indeed relevant. During prosecution, Patent Owner argued:

> Roberts does not disclose a "digital-to-digital mapping," where, "for a given plurality of N digital input data bits, the mapping to the corresponding M digital output data bits is determined based on a pattern for actuating drive voltages that alters the linearity of an optical response of the modulator," as recited in amended claim 1. *Instead*, the linear compensation in Roberts is performed pursuant to a compensation function c(t) when the $V_x(n)$ multi-bit sample streams are generated. *Importantly*, this linear compensation in Roberts occurs *before* the mapping of $V_x(n)$ to $S_x(n)$. As a result, the mapping between $V_x(n)$ to $S_x(n)$ in Roberts, such as the mapping shown in Table 1 of Roberts, is not a part of the linear compensation operation performed in Roberts.

Ex. 1002, 172 (emphasis added). We interpret the quoted passage to exclude analog pre-distortion because we interpret the argument distinguishing Robert's compensation as happening "before the mapping" to refer to pre-distortion techniques—in particular, those accomplished by analog compensation function, c(t). *Id.* Both the '872 patent and Patent Owner's

arguments during prosecution support Dr. Dallesasse's testimony and Patent Owner's position that the scope of claim 1 does not encompass linear compensation methods effected by analog pre-distortion.

Petitioner does not point us in the direction of any case law, or factual evidence that indicates why we disregard these statements by Patent Owner, or why they do not constitute prosecution history estoppel. Thus, we disagree that "overlook[ing] that using the lookup table (to perform non-linear compensation) is distinct from populating the lookup-table values" is the relevant inquiry. Req. Reh'g 11. For this same reason, we find unpersuasive Petitioner's contention that "Taraschuk's feedback loop is not what performs compensation of the modulator," and that "Taraschuk's feedback loop is merely the mechanism by which the linearizer lookup table values are populated." *Id.* (citing Pet. Reply 8).

Assuming, *arguendo*, that Petitioner's "proposed combination does not incorporate Taraschuk's feedback loop, or any other unclaimed mechanism for populating the lookup table values," including Roberts' compensation function, it is not clear then why "the exemplary lookup table values presented by Dr. Blumenthal are representative of" Roberts' or Taraschuk's teachings. *Id.* at 12. This is yet another indication that Petitioner's intended proposed combination is a piecemeal combination predicated on hindsight.

With regard to Petitioner's *third* set of arguments, Petitioner does not sufficiently show that the sinusoidal response curve would look like the one Dr. Blumenthal proposes. Dr. Blumenthal asserts, without specifically or credibly explaining why, that a person of ordinary skill in the art would have selected a region of the sinusoidal response curve that includes an inflection point such that deltas both decrease and increase over some portion of the curve being linearized. *See* Ex. 1003 ¶ 52 (opining that "in the close vicinity

of the center of the positive or negative inflection regions, otherwise known as the Quadrature point, the modulator is almost linear," but without explaining why a person of ordinary skill in the art would have included regions on both sides of an inflection point). If a person of ordinary skill would have selected a region of the sinusoidal response curve on only one side of an inflection point, the evidence does not suggest that such a mapping would satisfy both limitations 13.8 and 13.9. Petitioner's obvious-to-try rationale is insufficient to show that a person of ordinary skill would have used a digital-to-digital-mapping in which there are regions in which the deltas are both decreasing and increasing. We reiterate that "[a]lthough there are three possible relationships between two, consecutive deltas, there are many possible sequences of deltas—Petitioner does not sufficiently show a finite number of solutions in its challenge." FWD 30.

V. CONCLUSION

For the foregoing reasons, we are not persuaded that we misapprehended or overlooked any matter in the Final Written Decision.

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner's Request for Rehearing is *denied*.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

RAMOT AT TEL AVIV UNIVERSITY, LTD.,
Patent Owner.

IPR2022-00576
Patent 11,133,872 B2

OGDEN, *Administrative Patent Judge*, concurring.

I agree with the majority's analysis and determinations regarding Petitioner's third set of arguments on rehearing, and I would deny Petitioner's Request for Rehearing on that basis alone.

In particular, I agree that the Board did not abuse its discretion in determining that Petitioner failed to show that a person of ordinary skill in the art would have selected a region of the sinusoidal response curve that includes an inflection point such that deltas both decrease and increase over some portion of the curve being linearized. I also agree that the Board did not abuse its discretion in determining that Petitioner's obvious-to-try rationale was unpersuasive.

Therefore, I concur in the denial of Petitioner's Request for Rehearing.

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