UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]

Petitioners,

v.

NETLIST, INC.,

Patent Owner.

_____

Case No. IPR2022-01428
Patent No. 8,787,060

_____

PATENT OWNER NETLIST, INC.'S NOTICE OF APPEAL

[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC, filed a motion and joinder and a petition in IPR2023-00882 and have been joined as petitioners in this proceeding.

Pursuant to 35 U.S.C. §§ 141, 142, and 319, and in accordance with 37 C.F.R. §§ 90.2-90.3, Patent Owner Netlist, Inc. ("Netlist") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board ("Board") entered on April 1, 2024 in IPR2022-01428 (Paper No. 48) ("Final Written Decision"), attached as Exhibit A; the Order denying Director Review of the Final Written Decision dated June 17, 2024 (Paper 52) ("Decision on Director Review Request"), attached as Exhibit B; and from all underlying findings, determinations, rulings, opinions, orders, and decisions regarding the *inter partes* review (Case IPR2022-01428) of U.S. Patent No. 8,787,060 (the "'060 Patent").

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Netlist states that the issues on appeal include, but are not limited to: the Board's determination that Claims 1 through 34 of the '060 Patent have been shown by a preponderance of the evidence to be unpatentable; the Board's construction of the challenged claims and application of its construction of the claims to the facts of record; the Board's procedural rulings, including its rulings regarding the adequate and timely preservation of certain of the parties' arguments and denial of submission of supplemental evidence that came into being after the sur-reply; the adequacy of the Board's consideration of the expert testimony, prior art, and other evidence in the record, including, but not limited to, evidence and testimony from related district court proceedings between Petitioner

and Patent Owner; the Board's factual findings, conclusions of law, or other determinations supporting or related to those issues (such as motivation to combine or reasonable expectation of success); the Board's compliance with the Administrative Procedure Act, including whether the Final Written Decision, denial of Director Review and the denial of Netlist's request for submitting supplemental evidence are arbitrary, capricious, an abuse of discretion, not in accordance with law, or in excess of the Board's jurisdiction, and any procedural irregularities associated with the review proceeding; as well as all other issues decided adversely to Netlist in any orders, decisions, rulings, and opinions.

This Notice of Appeal is being e-filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit, along with payment of the required docketing fees. In addition, a copy of this Notice of Appeal is being filed simultaneously with the Patent Trial and Appeal Board and filed by e-mail to the Director of the United States Patent and Trademark Office at efileSO@uspto.gov.

Dated: August 19, 2024

Respectfully submitted,

/Hong Zhong/

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, the undersigned certifies that on August 19, 2024, a copy of the foregoing **PATENT OWNER'S NOTICE OF APPEAL** was served by electronic mail, as agreed to by the parties, upon the following:

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I also certify that in addition to being filed electronically with the Board, a copy of this Notice of Appeal was filed on August 19, 2024, for delivery to the Director of the United States Patent and Trademark Office at the following e-mail address: efileSO@uspto.gov.

I further certify that a copy of the foregoing Notice of Appeal is being filed via CM/ECF on August 19, 2024, with the United States Court of Appeals for the Federal Circuit.

/Susan M. Langworthy/
Susan M. Langworthy

EXHIBIT A

Trials@uspto.gov
571-272-7822

Paper 48
Entered: April 1, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-01428
Patent 8,787,060 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and SHEILA F. McSHANE, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00882 and have been joined as petitioners to this proceeding.

I. INTRODUCTION

In this *inter partes* review, Samsung Electronics Co., Ltd. ("Samsung"), Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") challenge the patentability of claims 1–34 of U.S. Patent No. 8,787,060 B2 ("the '060 patent," Ex. 1001), which is assigned to Netlist, Inc. ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–34 of the '060 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

Samsung filed a Petition (Paper 1, "Pet.") challenging claims 1–34 of the '060 patent on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–6, 8–14, 16–19, 29–34	103(a)[2]	Kim,[3] Rajan[4]
1–14, 16–19, 29–34	103(a)	Kim, Rajan, Riho[5]

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Petitioner applies the pre-AIA version of § 103 based on an effective filing date before March 16, 2013. Pet. 3–4.
[3] US 2011/0103156 A1, published May 5, 2011 (Ex. 1014).
[4] US 8,041,881 B2, issued Oct. 18, 2011 (Ex. 1015).
[5] US 2011/0026293 A1, published Feb. 3, 2011 (Ex. 1016).

Claims Challenged	35 U.S.C. §	References/Basis
1–6, 8–34	103(a)	Kim, Rajan, Wyman[6]
1–14, 16–19, 29–34	103(a)	Riho, Rajan
1–34	103(a)	Riho, Rajan, Riho2[7]

Pet. 3. Patent Owner filed a Preliminary Response. Paper 6. With Board authorization (Ex. 3001), Samsung filed a preliminary reply (Paper 9) to the Preliminary Response, and Patent Owner filed a preliminary sur-reply (Paper 10). Trial was instituted on the asserted grounds of unpatentability. Paper 13 ("Inst. Dec.") at 28.

During the trial, Patent Owner filed a Response (Paper 20, "PO Resp."), and Samsung filed a Reply (Paper 24, "Pet. Reply"). After Samsung's Reply, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC were joined as petitioners to this proceeding based on a petition and a motion for joinder in IPR2023-00882. Paper 25. After this joinder, Patent Owner filed a Sur-reply (Paper 28, "PO Sur-reply").

Petitioner filed a motion to exclude certain evidence. Paper 34. Patent Owner opposed the motion (Paper 35), and Petitioner filed a reply in support of the motion (Paper 36).

An oral hearing was held on January 11, 2024, a transcript of which appears in the record. Paper 46 ("Tr.").

Petitioner relies on testimony from Andrew Wolfe, Ph.D. Ex. 1003. Patent Owner relies on testimony from Michael C. Brogioli, Ph.D. Ex. 2023. The parties have entered in the record transcripts of the

[6] US 7,969,192 B2, issued June 28, 2011 (Ex. 1017).
[7] US 2010/0195364 A1, published Aug. 5, 2010 (Ex. 1018).

depositions of these declarants. Exs. 2025 (Wolfe Deposition), 1052 (Brogioli Deposition).

B. Real Parties in Interest

The identified real parties in interest on the petitioner side are the following: Samsung, Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC. Pet. 1; IPR2023-00882, Paper 2 at 1.

Patent Owner identifies itself as the real party in interest. Paper 3 at 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters. Pet. 1; Paper 3 at 1; IPR2023-00882, Paper 2 at 1. We are issuing concurrently a final decision in IPR2022-01427 involving related U.S. Patent No. 9,318,160 B2 ("the '160 patent").

D. The '060 Patent and Illustrative Claim

The '060 patent relates to computer memory devices and, more specifically, to reducing the load of drivers in memory. Ex. 1001, 1:18–21. As background, the '060 patent describes an existing memory package with reference to Figure 1A, reproduced at right, which shows memory package 100 with control die 130 and three array dies 110. Ex. 1001, 1:30–44. Control die 130 has driver 134, which drives data signals from control die 130 to each array die via interconnect 142, and driver 140, which drives command and address

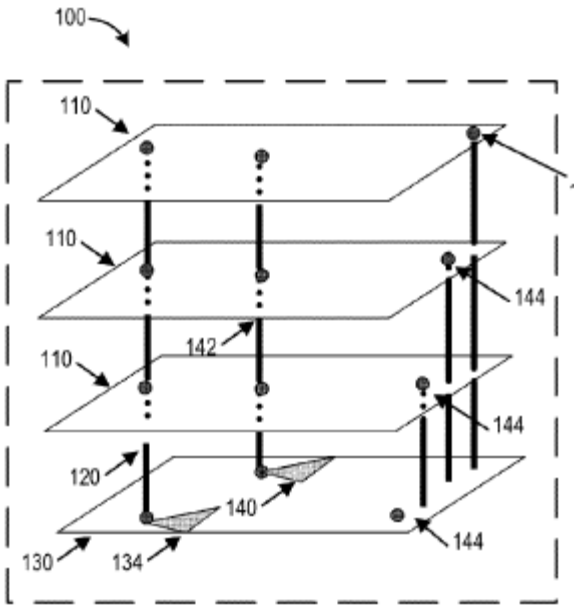


FIG. 1A

signals to each array die. Ex. 1001, 1:35–42. The '060 patent explains that "a load exists on each of the drivers 134, 140 . . . by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies." Ex. 1001, 2:8–11. The '060 patent discloses that, "to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver" and that "a larger driver not only consumes more space on the control die, but also consumes more power." Ex. 1001, 2:11–15.

The '060 patent states that driver size and power consumption can be reduced "by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die interconnect." Ex. 1001, 4:22–26. The '060 patent illustrates an exemplary configuration in Figure 2, reproduced at right, which shows memory package 200 with control die 230 and four array dies 210a–210d. Ex. 1001, 5:12–13. Control die 230 is connected to array dies 210a and 210b by die interconnect 220a, as shown by the darkened circles. Ex. 1001, 5:23–6:1. Die interconnect 220b connects control die 230 to array dies 210c and 210d, as shown by the darkened circles, but die interconnect

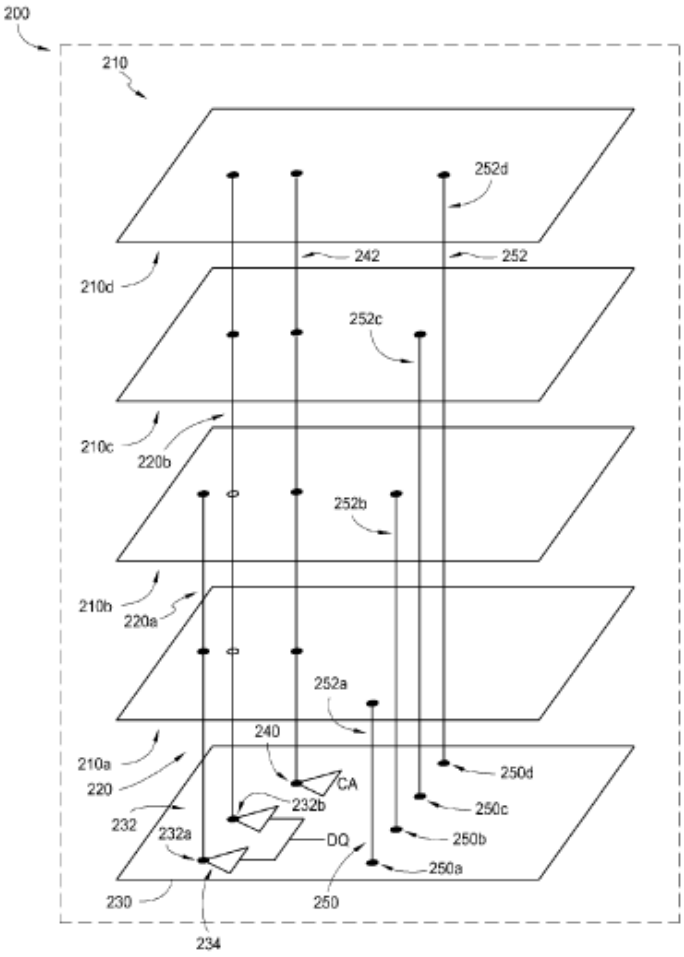


FIG. 2

220b is not electrically connected to array dies 210a and 210b, as shown by the unfilled circles. Ex. 1001, 6:9–23. The '060 patent also states that "[e]xamples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins." Ex. 1001, 5:51–53.

Claim 1 is illustrative and is reproduced below with Petitioner's claim element identifiers in brackets.

1. [1.a] A memory package, comprising:

   [1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;

   [1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;

   [1.d.1] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

   [1.e.1] a control die comprising [1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [1.e.3] and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, [1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

II. ANALYSIS

A. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Citing the testimony of its declarant, Dr. Wolfe, Petitioner contends that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 5 (citing Ex. 1003 ¶ 60). Petitioner also asserts that "[a]dditional training can substitute for educational or research experience, and vice versa," and Petitioner identifies particular technology with which a person of ordinary skill in the art would have been familiar, including JEDEC (Joint Electron Devices Engineering Council) industry standards, DRAM (dynamic random access memory) and SDRAM

(synchronous DRAM) memory modules, and "the structure and operation of circuitry used in stacked memory devices." Pet. 5 (citing Ex. 1003 ¶ 60).

Patent Owner states that, "[f]or purposes of this proceeding, Patent Owner applies the education and work-experience level specified on Petition, page 5." PO Resp. 6. Patent Owner then contends that "Petitioner does not allege that a [person of ordinary skill in the art] would have been familiar with designs and operations of non-DRAM devices or non-JEDEC specifications." PO Resp. 6. Patent Owner contends, therefore, that "under Petitioner's unpatentability theories" involving non-DRAM devices, persons of ordinary skill in the art "would be engaged in the project of making changes to memory devices that they have no experience with." PO Resp. 6 (citing Ex. 2023 ¶ 30).

We do not agree with Patent Owner's assertions regarding non-DRAM devices. The obviousness inquiry under 35 U.S.C. § 103(a) requires us to determine

> if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

As Patent Owner confirmed during oral argument, the term "array dies" in the claims encompasses non-DRAMs. Tr. 53:4–7. Because the subject matter pertains to configurations involving non-DRAM devices, the "person having ordinary skill in the art," by definition under the statute, would have had knowledge of non-DRAM devices. To the extent Petitioner's proposed skill level, on which the parties agree, does not make that clear, we do.

Thus, we accept the uncontested assessment offered by Petitioner with the exception of the qualifier "at least," which introduces vagueness as to the

amount of experience. We also determine that a person of ordinary skill in the art would have been familiar with designs and operations of non-DRAM devices for the reasons discussed above.

C. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b).

1. Array Die

The challenged claims recite the term "array dies." In related litigation, a district court construed this term based on the following argument made by the applicant during prosecution of the '060 patent regarding U.S. Patent Application Publication No. 2008/0025137 A1 (Ex. 1011 ("Rajan137")): "Rajan[137] does not disclose 'a plurality of stacked array dies.' Rajan[137] merely stacks DRAM circuits 206A–D, which are different from array dies." Ex. 2004, 31–32 (quoting Ex. 1002 ('060 patent prosecution history), 465 (January 13, 2014 Amendment at 10)). The district court found that Patent Owner "did not explain the structural difference between array dies and DRAM circuits, or even how they might be stacked differently" but, nonetheless, found that Patent Owner "*structurally* distinguished 'stacked DRAM circuits' from 'stacked array dies' to obtain the patent." Ex. 2004, 32. Based on this prosecution history, the district court adopted the defendants' proposed construction that "array die" means "array die that is different from a DRAM circuit." Ex. 2004, 32. Samsung is a defendant in that litigation.

Patent Owner argues that it "agreed to be bound by this construction and proceeded with the jury trial on that construction." PO Resp. 17 (citing

Exs. 2010, 2011). Yet, during the trial in this proceeding, Patent Owner qualifies the district court's construction to suggest that the term "array dies" means dies that are different from a particular kind of DRAM die. *See, e.g.*, PO Resp. 44 ("[T]he Petition contains no analysis on how or why Kim's memory chips are different from Rajan137's DRAM circuits."); *see also* Inst. Dec. 10–11 (addressing similar pre-institution arguments); Tr. 58:11–15 (Patent Owner's counsel asserting that Rajan137 "describes, for instance, monolithic memory circuits may take the form of, and then it lists an example. And it lists DRAM as an example of a monolithic memory circuit. So, we take DRAM circuit to be a monolithic memory circuit that holds state while powered."). The district court's construction, which Patent Owner asserts it adopted, does not contain any such qualification.

In our analysis below, we apply the district court's construction, and we find that the combination of Kim and Rajan teaches array dies that are not DRAMs and, therefore, are "different from a DRAM circuit." Therefore, we need not address any further qualifications of the district court's construction or construe the term "DRAM circuit" to determine what Patent Owner actually disclaimed, if anything. *See Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("[P]rosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution."); *see also Genuine Enabling Tech. LLC v. Nintendo Co.*, 29 F.4th 1365, 1374 (Fed. Cir. 2022) ("If the challenged statements are ambiguous or amenable to multiple reasonable interpretations, prosecution disclaimer is not established."). Based on our findings as to non-DRAM

dies, we also need not determine whether the term "array die" should be construed to also encompass DRAM circuits.

2. Chip Select

Claims 6, 11–14, 16–19, and 29–34 recite "chip select signals" or "chip select conduits." Patent Owner argues that the district court construed the terms "chip select signals" and "chip select conduits" to "exclude[] situations in which a chip select signal could enable multiple array dies at once" and contends that we should adopt this construction. PO Resp. 18–19 (citing Ex. 2004, 33–34). For the reasons explained below in section II.D, we determine that Petitioner has demonstrated unpatentability under the district court's construction, and, therefore, we need not further address this claim construction to render a final decision on patentability.

3. Group of Array Dies

Petitioner argues that the phrase "a first group of array dies," which is recited in the independent claims, can be just one die. Pet. Reply 7–8; *see also* Pet. 37 (arguing that multiple chips would have been obvious "[i]nsofar as one might argue that 'first group of array dies' requires multiple slave chips coupled to" one through-silicon via (TSV)).[8] Patent Owner disagrees and asserts that the first group must have plural dies. PO Resp. 20. We need not resolve this dispute because, as explained below in § II.D.2.d, we find persuasive Petitioner's contentions that the combination of Kim and Rajan teaches a first group that has multiple array dies.

[8] We omit the emphasis added by Petitioner for reference names and claim language when quoting Petitioner's arguments.

4. Driver Size

Various claims recite the term "driver size." Neither party argues for an express construction of this term, but Patent Owner notes that a district court in related litigation construed "driver size" as "driver physical size." PO Sur-reply 23; *see* Ex. 1066 (district court claim construction order), 13, 43. As explained below in § II.F, we find that the combination of Kim, Rajan, and Wyman teaches the subject matter under this construction, and we need not address the construction of this term further.

5. Remaining Terms

We determine that no other terms or phrases require express construction. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

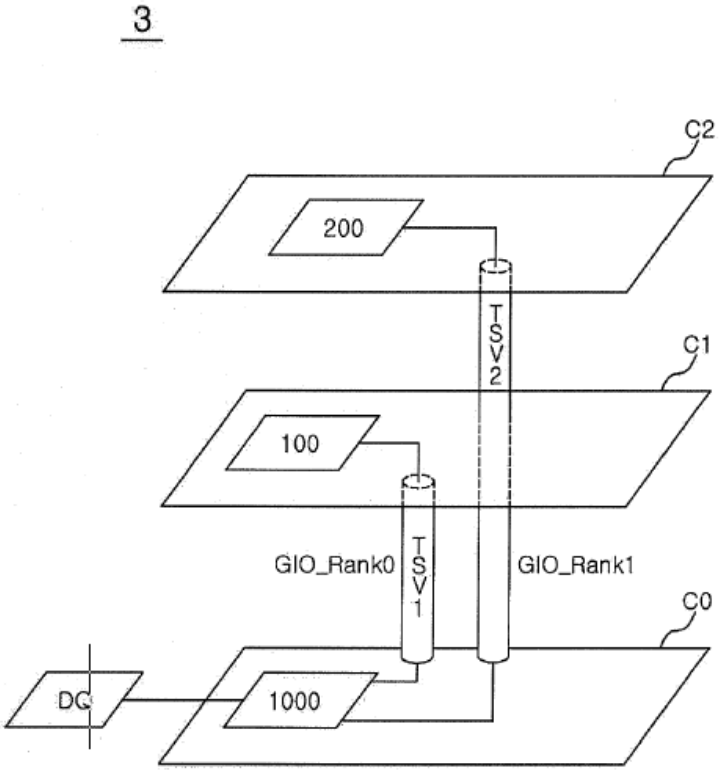
D. Obviousness over Kim and Rajan (Claims 1–6, 8–14, 16–19, 29–34)

Petitioner asserts that claims 1–6, 8–14, 16–19, and 29–34 are unpatentable as obvious over the combined teachings of Kim and Rajan. Pet. 3, 21–81. Patent Owner opposes. PO Resp. 20–51; PO Sur-reply 1–20.

1. Overview of the Prior Art

Kim discloses a semiconductor memory apparatus including stacked chips, as depicted in Figure 5 below.

FIG.5



Kim's Figure 5 above shows a memory including a plurality of stacked chips, including main chip C0 and first and second slave chips C1 and C2, connected by through-silicon vias (TSVs). Ex. 1014 ¶¶ 47–48.

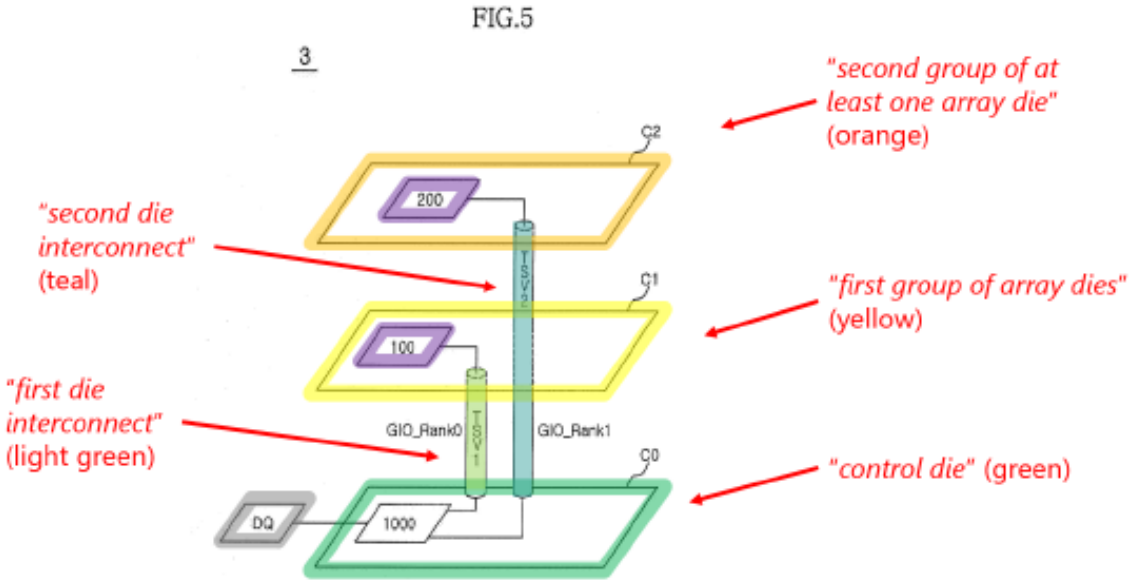
Rajan discloses using an interface circuit to emulate characteristics of particular memory even though the physical memory may not have those characteristics, which allows the "use of low cost memory chips in manufacturing high capacity memory modules." Ex. 1015, 1:51–54, 3:24–43. Rajan explains that the interface circuit may comply with JEDEC standards. Ex. 1015, 4:20–24.

We discuss additional pertinent details of the references below.

2. Claim 1

a) Overview of Petitioner's contentions for claim 1

To illustrate its contentions based on Kim, Petitioner provides the following annotated version of Kim's Figure 5:



Pet. 27. In the annotated figure above, Petitioner maps depicted components to elements of claim 1 as follows: chip C1 (yellow) as "first group of array dies"; chip C2 (orange) as "second ground of at least one array die"; chip C0 (green) as "control die"; TSV1 (light green) from C0 to C1 as "first die interconnect"; TSV2 (teal) from C0 to C2 as "second die interconnect." Pet. 27.

Petitioner argues that a person of ordinary skill in the art would have been motivated to make Kim's memory package compatible with JEDEC standards based on Rajan's teachings. Pet. 24–27. Petitioner also argues that a person of ordinary skill in the art would have been motivated to have multiple memory chips share a TSV because this was a known option and "would not require creating new TSVs (which would add space and

circuitry) and would allow emulating the JEDEC standard required by external devices." Pet. 28–29.

b) Preamble (1.a)

Petitioner argues that Kim's Figure 5 depicts a "memory package," as recited in the preamble. Pet. 30 (citing Ex. 1014 ¶¶ 46–47; Ex. 1003 ¶¶ 184–188). Patent Owner does not dispute this contention. We agree with Petitioner, and we find, that Kim's disclosure of semiconductor memory apparatus 3 in Figure 5 teaches a "memory package." In view of this finding, we need not decide whether the preamble is limiting.

c) Input/output terminals (1.b)

For claim 1's "plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices" (1.b), Petitioner argues that Kim's Figure 5 shows input/output data terminals as "DQ," that Kim's Figure 2 shows control terminals as CS0 and CS1, and that Kim's memory package would have control and address terminals to accept control and address signals in a JEDEC-compliant implementation. Pet. 31–34. Patent Owner does not dispute that the combination of Kim and Rajan teaches control, address, and data terminals, but Patent Owner does dispute the JEDEC aspect of Petitioner's combination. We agree with Petitioner, and we find, that Kim teaches a memory package having data, address, and control terminals, and we further address the parties' dispute about JEDEC below.

d) Stacked array dies (1.c) and die interconnects (1.d.1, 1.d.2)

Claim 1 recites "a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports" (1.c). Claim 1 further recites that the memory

package has "at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die," (1.d.1) and "the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies" (1.d.2).

As noted above in reference to Petitioner's annotated version of Kim's Figure 5, Petitioner identifies Kim's chip C1 as "a first group of array dies" and Kim's chip C2 as "a second group of at least one array die." Pet. 34–35 (citing Ex. 1014 ¶¶ 26, 48, Fig. 5; Ex. 1003 ¶¶ 211–219). Petitioner argues that having multiple dies in the first group all sharing the same die interconnect would have been obvious. Pet. 37–39 (citing Ex. 1014 ¶¶ 48, 50; Ex. 1024, 9:14–18, Fig. 5; Ex. 1015, Fig. 4; Ex. 1003 ¶¶ 219–227).[9] Petitioner argues that the annotated version of Rajan's Figure 4 below shows "multiple stacked memory chips connected to the same data bus." Pet. 38–39.

[9] Petitioner also argues that "a first group of array dies" can be just one die. Pet. Reply 7–8; *see also* Pet. 37. We do not rely on this argument and, therefore, need not resolve the parties' dispute regarding whether this phrase encompasses a single die.

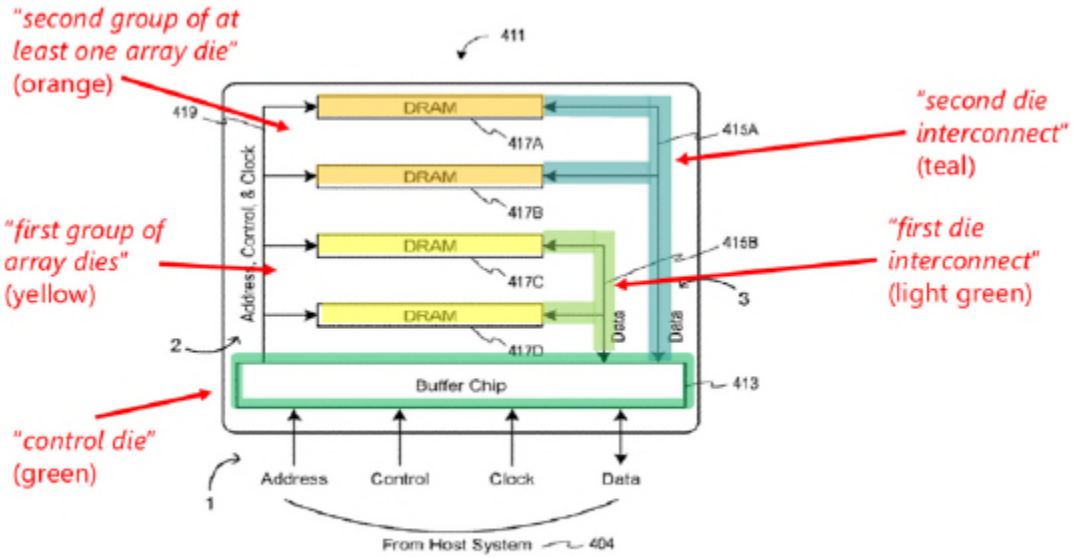


FIG. 4

Rajan's Figure 4 "shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses." Ex. 1015, 2:6–7. In the annotated figure above, Petitioner maps depicted components to elements of claim 1 as follows: DRAMs 417C and 417D (yellow) as "first group of array dies"; DRAMs 417A and 417B (orange) as "second ground of at least one array die"; buffer chip 413 (green) as "control die"; data bus (light green) from buffer chip 413 to DRAMs 417C and 417D as "first die interconnect"; and data bus from buffer chip 413 to DRAMs 417A and 417B as "second die interconnect." Pet. 42.

Petitioner argues that Kim and Rajan are analogous art. Pet. 24 (citing Ex. 1003 ¶¶ 154–155). Patent Owner does not dispute that Kim and Rajan are analogous art to the '060 patent. *See* PO Resp. We agree with Petitioner that Kim and Rajan are analogous art because they are both in the same field of endeavor as the '060 patent—memory packages and in particular those involving stacked memory. Ex. 1001, 1:18–19 ("The present disclosure relates to memory devices and memory modules."), claim 1 ("memory

package" with "stacked array dies"); Ex. 1014 ¶ 3 ("Various embodiments of the present disclosure generally relate to a semiconductor memory apparatus . . . ."), Fig. 5 (stacked memory chips); Ex. 1015, 1:14–16 ("This invention relates generally to digital memory such as used in computers[], and more specifically to organization and design of memory modules such as DIMMs [(dual in-line memory modules)]."), Figs. 2–6 (stacked memories).

Petitioner argues that a person of ordinary skill in the art "would be motivated to create a package with an interface that complied with the well-known JEDEC standards, as taught by Rajan," such that Kim's memory package would be compatible with JEDEC. Pet. 24–26 (citing Ex. 1014 ¶ 38, Fig. 5; Ex. 1015, 3:52–54, 4:20–24, 5:36–43, 8:8–11, Figs. 4, 18; Ex. 1003 ¶¶ 151–157; Ex. 1019, 12, Fig. 3).

Petitioner also argues that, based on Kim's disclosure of using "any number of" chips (Ex. 1014 ¶ 48), a person of ordinary skill in the art "would have been motivated to look at Rajan for the details about adding more memory chips in the stack." Pet. 26 (citing Ex. 1014 ¶¶ 48, 50; Ex. 1003 ¶¶ 158–160). Petitioner argues that a person of ordinary skill in the art "would have understood that there were a finite number of known ways to connect additional dies, including having a subset of dies sharing a through-silicon via (TSV)," and that "[s]haring a TSV among two or more dies was a known option, as confirmed by other references at the time." Pet. 28 (citing Ex. 1003 ¶¶ 161–163; Ex. 1015, 5:36–43, Figs. 2–6; Ex. 1025, Fig. 5). Petitioner also argues that a person of ordinary skill in the art "would have been motivated to connect additional memory dies to Kim's TSV1 and TSV2 because it would not require creating new TSVs (which

would add space and circuitry) and would allow emulating the JEDEC standard required by external devices." Pet. 28–29 (citing Ex. 1003 ¶ 164; Ex. 1015, 3:27–30, 3:52–61). Petitioner further argues that "it was common at the time to have multiple memory dies sharing a single data bus" and "to use a 'fork-in-the-road' arrangement with two data buses for two ranks of memory devices . . . with the option of adding two additional ranks of memory devices (resulting in four ranks) to the existing data busses," such that two dies share a bus. Pet. 29 (citing Ex. 1003 ¶¶ 165–166; Ex. 1026, Figs. 12, 13).

As to claim 1's "electrical communication" recitations (1.d.1 and 1.d.2), Petitioner argues that Kim's Figure 5 shows die interconnect (TSV1) connected from chip C0 to chip C1 and not extending to chip C2 and die interconnect (TSV2) connected from chip C0 to chip C2 and passing through chip C1 without being connected. Pet. 39–40 (citing Ex. 1014, code (57), ¶¶ 45, 49, Fig. 5; Ex. 1003 ¶¶ 230–239). And, as discussed above, in Petitioner's proposed combination, multiple dies would share a TSV (Pet. 28–29) such that each group would be in electrical communication with the TSVs shared by that group and not other TSVs.

Below, we address Patent Owner's arguments pertinent to recitations 1.c, 1.d.1, and 1.d.2.

(1) Array dies

As noted above in § II.C.1, a district court construed "array die" to mean "array die that is different from a DRAM circuit." Ex. 2004, 31–32. Patent Owner argues that "the Petition contains no analysis on how or why Kim's memory chips are different from Rajan137's DRAM circuits." PO Resp. 44. Patent Owner's argument, therefore, reflects an attempt to limit

the district court's construction to exclude only certain types of DRAM circuits, similar to arguments Patent Owner made before institution. *See* Inst. Dec. 11 ("Patent Owner appears to argue that the district court's construction is that the claimed array dies are different from Rajan137's DRAM circuits 206A–D, not all DRAM circuits.").

As noted at institution, Kim does not even mention DRAM and thus is not limited to DRAM, and Rajan states that "any type of memory whatsoever" may be used in its disclosure and lists non-DRAM memories. Inst. Dec. 23 (quoting Ex. 1015, 15:3–9). Therefore, we find that the combination of Kim and Rajan teaches "array dies" under the district court's construction and under Patent Owner's interpretation of that construction.

Patent Owner further argues that,

> if, in Petitioner's combination, the stacked dies are non-DRAM dies, neither the Petition nor the declaration explains why a [person of ordinary skill in the art] would be motivated to have the package emulate a DRAM interface or how the resulting structure would work given Petitioner's theory that the interface circuit should provide a JEDEC-compliant interface to the host, citing to SDRAM standards.

PO Resp. 45 (citing Pet. 31–33). According to Patent Owner, "Petitioner has not presented any evidence that with non-DRAM circuits such as NANDs or SRAMs [(static RAM)], a [person of ordinary skill in the art] would have or could have emulated the memory package as JEDEC-compliant DRAM devices." PO Resp. 46 (citing Pet. 8–11, 24–33; Ex. 2023 ¶¶ 173–177); *see also* PO Resp. 47–48 ("Petitioner has not shown that a [person of ordinary skill in the art] would have been motivated to use non-DRAM dies in combination with an interface circuit that emulates a JEDEC-compliant interface to the host.").

We disagree with Patent Owner's arguments because the evidence in support of Petitioner's position is the express disclosure of Rajan. As noted above, Petitioner argues that a person of ordinary skill in the art "would be motivated to create a package with an *interface* that complied with the well-known JEDEC standards, as taught by Rajan." Pet. 24 (emphasis added). Rajan discloses an "interface circuit [that] may take the form of or incorporate, or be incorporated into, a register, an AMB [(advanced memory buffer)], a buffer, or the like, and may comply with Joint Electron Device Engineering Council (JEDEC) standards, and may have forwarding, storing, and/or buffering capabilities." Ex. 1015, 4:20–24. Rajan explains that "the interface circuit presents to the system device an interface to emulated memory devices which differ in some aspect from the physical memory circuits which are actually present." Ex. 1015, 3:24–27. With reference to Figure 1, Rajan discloses that the "physical memory circuits may be any type of memory circuits." Ex. 1015, 2:59–60. Rajan further discloses that, "[a]lthough the embodiments described here show the stack consisting of multiple DRAM circuits, a stack may refer to any collection of memory circuits (e.g. DRAM circuits, flash memory circuits, or combinations of memory circuit technologies, etc.)." Ex. 1015. 4:51–55. Rajan still further discloses that the "physical memory circuits employed in practicing this invention may be any type of memory whatsoever, such as: DRAM, DDR DRAM, DDR2 DRAM, DDR3 DRAM, SDRAM, QDR DRAM, DRDRAM, FPM DRAM, VDRAM, EDO DRAM, BEDO DRAM, MDRAM, SGRAM, MRAM, IRAM, NAND flash, NOR flash, PSRAM, wetware memory, etc." Ex. 1015, 15:3–9. Thus, Rajan expressly discloses using non-DRAM dies as the memory circuits.

Patent Owner argues that "Rajan never suggests that its interface die would be emulating a different type of memory circuits from the backend memory." PO Sur-reply 18 (citing Ex. 1015, 15:3–9). We disagree with this argument. As noted above, Rajan's "interface circuit presents to the system device an interface to emulated memory devices which differ in some aspect from the physical memory circuits which are actually present" (Ex. 1015, 3:24–27), and we see nothing in Rajan that limits its teachings as Patent Owner's argument suggests. Furthermore, Rajan discloses that the

> memory subsystem includes a buffer chip 202 which presents the host system with emulated interface to emulated memory, and a plurality of physical memory circuits which, in the example shown, are DRAM chips 206A-D. In one embodiment, the DRAM chips are stacked, and the buffer chip is placed electrically between them and the host system. Although the embodiments described here show the stack consisting of multiple DRAM circuits, a stack may refer to any collection of memory circuits (e.g. DRAM circuits, flash memory circuits, or *combinations of memory circuit technologies*, etc.).

Ex. 1015, 4:45–55 (emphasis added). The fact that the memory stack may include "combinations of memory circuit technologies," such as DRAM and flash, shows that the interface would emulate a memory different from at least one of the memory technologies in the combination when it presents as one type of memory to the host. Rajan also discloses that "the memory circuits may be symmetrical, meaning each has the same capacity, *type*, speed, etc., while in other embodiments they may be asymmetrical." Ex. 1015, 2:62–67 (emphasis added). Thus, Rajan discloses that symmetrical circuits are of the same type, suggesting that asymmetrical circuits can be of different types behind the interface.

Patent Owner also asserts in a parenthetical that Rajan's disclosure at column 15, lines 3–9 "has no link to 4:20-24 which is part of the description for Fig. 1, related to 'DRAM circuits.'" PO Sur-reply 18. We disagree with this assertion. Rajan at column 4, lines 20–24 discloses that the interface circuit may comply with JEDEC, and this is the "interface circuit" of the disclosed invention. *See* Ex. 1015, 1:65–67 ("FIG. 1 shows a system coupled to multiple memory circuits and an interface circuit according to one embodiment of this invention."). Thus, Rajan's disclosure that the "physical memory circuits employed in practicing *this invention* may be any type of memory whatsoever," including non-DRAMs, (Ex. 1015, 15:3–9 (emphasis added)) is linked to the interface circuit of the invention, which is described throughout Rajan and is described as being JEDEC-compliant in column 4, lines 20–24.

For all of the reasons discussed above, we find that Rajan teaches using non-DRAM memories in a JEDEC-compliant memory package and, therefore, that Rajan provides an express motivation to "to use non-DRAM dies in combination with an interface circuit that emulates a JEDEC-compliant interface to the host." *See* PO Resp. 47–48.

We also disagree with Patent Owner's argument that "Petitioner has not presented any evidence that with non-DRAM circuits such as NANDs or SRAMs, a [person of ordinary skill in the art] . . . *could have* emulated the memory package as JEDEC-compliant DRAM devices." *See* PO Resp. 46 (emphasis added) (citing Pet. 8–11, 24–33; Ex. 2023 ¶¶ 173–177). We disagree because the express disclosure of Rajan, discussed above, is evidence that a person of ordinary skill in the art could have used non-DRAM memories in a JEDEC-compliant DRAM package. Petitioner

cites Rajan's Figure 18 (Pet. 24–25), which shows an embodiment of an interface circuit, and Rajan's accompanying disclosures provide more details as to how the interface circuit functions. Ex. 1015, 14:6–62.

Furthermore, we have considered the cited testimony from Dr. Brogioli, which focuses on how NAND flash and SRAM both differ from DRAM. Ex. 2023 ¶¶ 173–177. When considered in view of the disclosure of Rajan, the listed differences do not indicate or suggest difficulties beyond the skill of an ordinarily skilled artisan to implementing JEDEC-compliant interfaces with non-DRAM memories. For example, Dr. Brogioli testifies that NAND "signaling, electrical and physical interface are drastically different than that of DRAM memory devices, or DRAM memory modules that are JEDEC or JEDEC adjacent." Ex. 2023 ¶ 175. But Rajan discloses that memory characteristics emulated by the interface circuit "may be electrical in nature, physical in nature, logical in nature, pertaining to a protocol, etc." Ex. 1015, 3:36–38. As to signaling in particular, Rajan discloses that "[t]he interface circuit may emulate the number of signals, type of signals, duration of signal assertion, and so forth" and "may combine multiple signals to emulate another signal." Ex. 1015, 3:48–51. Dr. Brogioli also testifies about "vastly different timing" between NAND and DRAM (Ex. 2023 ¶ 175), but Rajan discloses that "[a]n example of an emulated protocol characteristic might be a timing" (Ex. 1015, 3:42–43) and that the interface circuit's "emulation logic may, in various embodiments, alter a *timing*, value, latency, etc. of any of the address, control, clock, and/or data signals it sends to or receives from the system and/or the physical memory" (Ex. 1015, 14:55–59 (emphasis added)). Therefore, Dr. Brogioli's testimony fails to account for Rajan's disclosure. Dr. Brogioli's

testimony as to the "different signaling mechanism" that SRAM uses (Ex. 2023 ¶ 177) is similarly unpersuasive.

Furthermore, Dr. Brogioli's testimony addressing NAND flash and SRAM differences fails to appreciate that Rajan is not so limited and lists other non-DRAM memories that can be used, including NOR flash. *See* Ex. 1015, 15:3–9.

For the foregoing reasons, we find that the combination of Kim and Rajan teaches "array dies."

(2) Electrical communication

Patent Owner argues that Petitioner has not shown that the combination of Kim and Rajan teaches a "first die interconnect in electrical communication with" multiple array dies. PO Resp. 20–44.

Patent Owner argues that Kim discloses that "each TSV is in communication with only a single chip." PO Resp. 20 (citing Ex. 1014, Fig. 5; Ex. 2023 ¶ 84). Although Kim's Figure 5 depicts TSV1 in communication with chip C1 and TSV2 in communication with chip C2, Kim discloses that "any number of . . . chips may be used" (Ex. 1014 ¶ 48), as Petitioner points out. *See* Pet. 26 (citing Ex. 1003 ¶¶ 158–160; Ex. 1014 ¶¶ 48, 50). Petitioner argues that this disclosure would have motivated a person of ordinary skill in the art "to look at Rajan for the details about adding more memory chips in the stack (resulting, e.g., in four chips . . . in two groups . . .)." Pet. 26. We agree with Petitioner, and we find, that Kim's disclosure suggests having more than the two chips depicted in Figure 5. *See* Ex. 1014 ¶¶ 48 ("Although only one main chip and two slave chips are shown, it is to be understood that any number of main and slave chips may be used."), 50 ("While the semiconductor memory apparatuses

having two ranks are explained with reference to FIGS. 2 and 5, a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus which are divided into three or more ranks."); *see also* Ex. 1003 ¶ 159 ("A Skilled Artisan would have understood from this disclosure that Kim's invention can include more slave chips (and more ranks) and that some of those additional slave chips proposed by Kim can be in the same group as chips C1 or C2 and connected to TSV1 or TSV2, respectively.").

> Petitioner contends that a person of ordinary skill in the art
>
> would have been motivated to implement a shared data bus for multiple memory chips as taught by Rajan (e.g., 415A and 415B, above) using, e.g., Kim's TSV interconnects . . ., in part because a [person of ordinary skill in the art] would have understood that there were a finite number of known ways to connect additional dies, including having a subset of dies sharing a through-silicon via (TSV).

Pet. 28 (citing Ex. 1003 ¶¶ 161–163; Ex. 1015, 5:36–43, Figs. 2–6). Thus, Petitioner's contention is that, given Kim's express disclosure of having more than two memory chips, a person of ordinary skill would have looked to Rajan for details about adding more memory chips. Petitioner argues that Rajan teaches "a shared data bus for multiple memory chips" as depicted in Rajan's Figure 4 (Pet. 28), and Patent Owner agrees. *See* PO Resp. 21 ("In Rajan, Figure 4, Rajan's DRAM circuits 417A and 417B share one data bus and DRAM circuits 417C and 417D share another data bus.").

Patent Owner does not dispute Petitioner's contention (Pet. 28) that there are a finite number of known ways to connect additional dies, one of which being to have dies share a TSV. *See* PO Resp. In support of its contention that "[s]haring a TSV among two or more dies was a known

option," as confirmed by other references, such as Foster, Petitioner provides the annotated figure below.

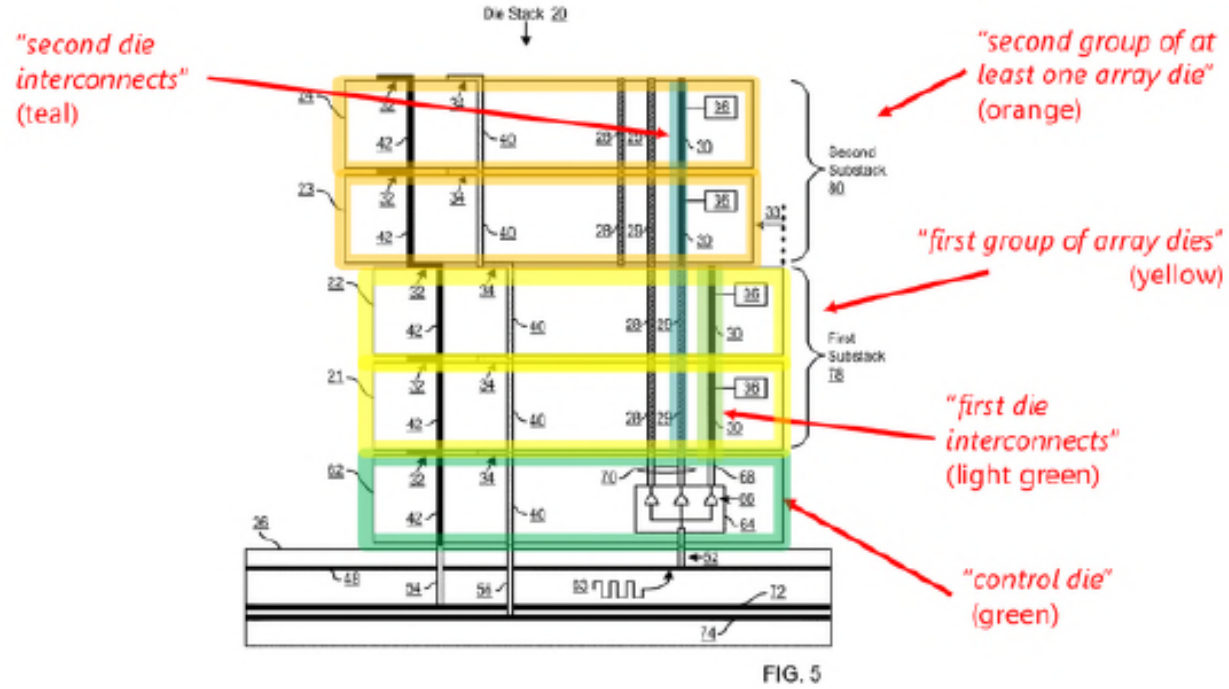


FIG. 5

Pet. 28 (citing Ex. 1025 ("Foster"),[10] Fig. 5). Foster's Figure 5 shows a cross-sectional view of die stack 20 including first substack 78 of dies 21 and 22 and second substack 80 of dies 23 and 24. Ex. 1025, 7:28–45. Petitioner identifies first substack 78 as a "first group of array dies" in yellow and second substack 80 as a "second group of at least one array die" in orange. Pet. 28. In Figure 5, TSVs 30 (identified by Petitioner in light green) connect to the first substack but do not extend to the second substack, and pass-through vias (PTVs) 29 (identified by Petitioner in teal) go through the first stack and connect to TSVs in the second substack. Ex. 1025, 7:45–54. Foster explains that PTVs are "conductive pathways through each die with no connections to any circuitry on the die" and that TSVs are

[10] US 8,258,619 B2, filed Nov. 12, 2009, issued Sept. 4, 2012.

"conductive pathways through the dies that also connect to electronic circuitry (36) on the die." Ex. 1025, 2:53–56.

Patent Owner and Dr. Brogioli do not disagree with Petitioner's assertion that Foster shows that "[s]haring a TSV among two or more dies was a known option." *See* Pet. 28. Rather, they address different issues. Patent Owner argues that Petitioner cites Foster "for die grouping." PO Resp. 21 n.3. And Dr. Brogioli testifies that "Foster does not specify the relationship of the dies forming the substack that shares a TSV or PTV" or suggest a certain die grouping. Ex. 2023 ¶ 164. Regardless of whether Foster teaches a certain die grouping, we agree with Petitioner that Foster shows that "[s]haring a TSV among two or more dies was a known option." *See* Pet. 28.

Petitioner's contention, as noted above, is that a person of ordinary skill in the art "would have been motivated to implement a shared data bus for multiple memory chips as taught by Rajan . . . using, e.g., Kim's TSV interconnects." Pet. 28. Rajan's Figure 4 is shown below.

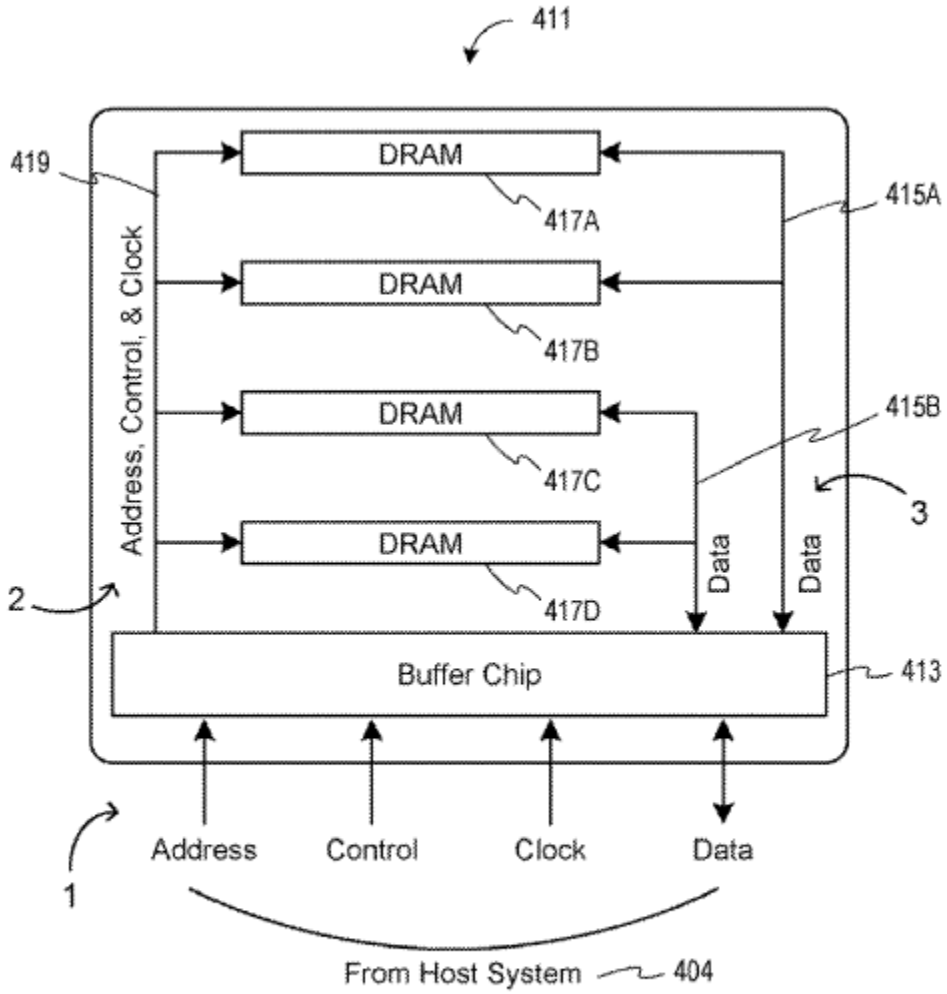


FIG. 4

Rajan's Figure 4 above "shows a buffered stack of DRAM circuits having one address, control, and clock bus and two data busses." Ex. 1015, 2:6–7; *see also* Ex. 1015, 4:51–55 ("Although the embodiments described here show the stack consisting of multiple DRAM circuits, a stack may refer to any collection of memory circuits (e.g. DRAM circuits, flash memory circuits, or combinations of memory circuit technologies, etc.)."). As shown in Figure 4, memory chips 417A and 417B share data bus 415A, and memory chips 417C and 417D share data bus 415B. Ex. 1015, 5:39–42.

Dr. Brogioli testifies that "Rajan uses wire bonds for connecting its DRAM circuits to the data busses, and wire bonds ordinarily cannot be shared in the way that TSVs are shared." Ex. 2023 ¶ 143 (citing Ex. 1011 ¶ 50). In support of this statement, Dr. Brogioli does not cite the Rajan reference on which Petitioner's challenge is based; rather, he cites Rajan137, which states that "data signals may be wired as one common bus, several busses or as an individual bus to each DRAM circuit." Ex. 1011 ¶ 50, *quoted in* Ex. 2023 ¶ 143. Rajan, however, does not include this disclosure and does not state that its dies are connected with wire bonds. Thus, we do not credit Dr. Brogioli's testimony that Rajan uses wire bonds.

Dr. Brogioli also testifies that

> [t]he '060 patent discloses that an example of a die interconnect is a wire bond. But that wire bond is different from a wire bond dangling from the side of a DRAM circuit such as those in Rajan. Instead, the type of wire bonds referenced by the '060 patent are wires internal to a die, acting, for example, like a redistribution line.

Ex. 2023 ¶ 39 n.1 (citing "*e.g.*, the red and blue wires in DDX4-48" (Ex. 2030)[11]). Even if Rajan's Figure 4 shows wire bonds, an opinion that we do not credit as explained above, Dr. Brogioli does not explain why a wire bond in Rajan would be different from the wire bonds that can be die interconnects in the '060 patent. *See* Ex. 1001, 5:51–53 ("Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins."). In addition, it is not clear what "the red and blue wires in DDX4-48" (Ex. 2023 ¶ 39 n.1) show because the cited page is about "Accused HBM Products" and does not mention wire

[11] Dr. Brogioli appears to be referring to Ex. 2030. *See* Ex. 2023 ¶ 57 (citing "EX2030, DDX4-53").

bonds. *See* Ex. 2030, DDX4-48. Thus, this testimony is not helpful in explaining any alleged differences in wire bonds. *See* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."). Furthermore, we do not agree with Dr. Brogioli's testimony that wire bond die interconnects in the '060 patent "are wires internal to a die" (Ex. 2023 ¶ 39 n.1) because wires that are only internal to one die would not interconnect with another die, and, thus, would not be a "die interconnect."

In view of the foregoing, we find that Rajan does not disclose the particular structure in which the shared data busses in Figure 4 are implemented. In other words, Rajan's disclosure is agnostic as to the particular interconnect technology by which the memories that share data busses are connected to the buffer chip.

Dr. Brogioli also testifies that a "data bus can be shared without sharing interconnects, especially in Rajan," "because Rajan uses wire bonds for connecting its DRAM circuits to the data busses." Ex. 2023 ¶ 143 (citing Ex. 1011 ¶ 50). As discussed above, we do not credit Dr. Brogioli's opinion that Rajan uses wire bonds because it is based on a different reference. Furthermore, the fact that a data bus can be shared without sharing interconnects is irrelevant because Petitioner's proposed combination is to share interconnects (Kim's TSVs). *See* Pet. 28. Rajan's Figure 4 discloses a stack of memory circuits, as discussed above (*see* Ex. 1015, 2:6–7, 4:51–55), and Kim discloses using TSVs in stacks of memory chips, as also discussed above (*see* Ex. 1014 ¶¶ 48, 50, Fig. 5). Thus, Petitioner's combination is a straightforward one – "implement a shared data bus for multiple memory

chips as taught by Rajan . . . using, e.g., Kim's TSV interconnects." Pet. 28 (discussed above).

At oral argument, Patent Owner's counsel argued that the "TSV is the individual data wire going down to the bus that's shared." Tr. 65:12–13. According to Patent Owner's counsel,

> Rajan talks about [two chips] sharing a data bus. So, I don't see how, from Rajan, you would get the idea of a shared TSV when Rajan speaks solely about sharing data buses. And the data bus, under JEDEC standard, involves individual data wires coming from each of the chips.

Tr. 65:26–66:4. By this argument, Patent Owner's counsel appears to be suggesting that, even if TSVs are used, they would just connect each chip to a shared data bus. But this is not the proposed combination, as stated above, which is to implement a shared bus per Rajan using Kim's TSVs. *See* Pet. 28. Implementing a bus using TSVs is consistent with the evidence of record. *See* Ex. 1025, 1:39–42 ("A more recent approach for wafer stacking is to connect the signals together with vias, effectively sending a bus of signal lines vertically through a stack of dies."), 2:56–64 ("[A]ggregations of PTVs and TSVs will often be used to effect connection of bus signals from a substrate up through the die stack to circuitry somewhere in the die stack.").

Based on the foregoing, we find persuasive Petitioner's contention that a person of ordinary skill in the art

> would have been motivated to implement a shared data bus for multiple memory chips as taught by Rajan (e.g., 415A and 415B, above) using, e.g., Kim's TSV interconnects . . ., in part because a [person of ordinary skill in the art] would have understood that there were a finite number of known ways to connect additional dies, including having a subset of dies sharing a through-silicon via (TSV).

See Pet. 28. Furthermore, we find persuasive Petitioner's reasoning that a person of ordinary skill in the art "would have been motivated to connect additional memory dies to Kim's TSV1 and TSV2 because it would not require creating new TSVs (which would add space and circuitry)." Pet. 28–29 (citing Ex. 1003 ¶ 164). As discussed above, Kim suggests having more than two dies, Rajan discloses how to share a data bus among multiples dies, and the evidence of record shows that TSVs were used to implement data busses. Ex. 1014 ¶¶ 48, 50; Ex. 1025, 1:39–42, 2:56–64. We find that using the existing TSVs of Kim would be beneficial to avoid having to create new ones, "which would require space and additional circuitry." Ex. 1003 ¶ 164.

Having found persuasive the above contentions, we turn to the issue of whether the proposed combination would have been within the ability of a person of ordinary skill in the art. *See KSR*, 550 U.S. at 421 (noting that "a person of ordinary skill has good reason to pursue the known options *within his or her technical grasp*" (emphasis added)); *see also id.* at 417 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.").

Patent Owner argues that the asserted combination could result in four possible configurations and that each configuration either would be inoperable or would not meet the claims. PO Resp. 22 (citing Ex. 2023 ¶ 86). Patent Owner asserts that the

> four possibilities are: (1) four chips belong to two ranks and two chips from the same rank share a common TSV; (2) four chips belong to two ranks and a chip from one rank shares a TSV with a chip from another rank; (3) four chips belong to four ranks and

> each of the four ranks has its own TSV; and (4) four chips belong to four ranks and every two ranks share a TSV.

PO Resp. 22 (citing Ex. 2023 ¶ 86).

We need not address the first three configurations because, for the reasons explained below, we find Petitioner's combination persuasive in the fourth configuration. Patent Owner argues that a person of ordinary skill in the art would not combine the teachings of Kim and Rajan in the fourth configuration because it would result in unavoidable data collisions. PO Resp. 32–44. Patent Owner asserts that, "[a]s Dr. Brogioli testified, handling data collisions involves 'a lot of complexities' that [are] 'beyond the scope of a person of skill.'" PO Sur-reply 8 (citing Ex. 1052, 283:17–284:12). Patent Owner argues, therefore, that "the requirement that at least one die interconnect be in connection with a group of array die*s* (plural) would result in inoperable apparatuses for Kim's intended purposes." PO Resp. 43 (citing Ex. 2023 ¶¶ 149–150); *see* Ex. 2023 ¶ 150 ("A person of ordinary skill in the art would not have had a reason or a reasonable expectation of success to modify Kim so that multiple dies share the same TSV signaling path.").

Petitioner argues that techniques for avoiding collisions on shared data lines were well-known to persons of ordinary skill in the art, citing as one example Rajan's teachings of timing solutions to avoid collisions. Pet. Reply 2–7 (citing, *inter alia*, Ex. 1015, 8:59–12:13, Figs. 9–15). For the reasons explained below, we find persuasive Petitioner's contentions that persons of ordinary skill in the art knew how to deal with collisions.

The specification of the '060 patent mentions collisions only once:

> Some implementations of the control dies 822 include a plurality of command/address buffers (not shown). These

> buffers may comprise latches. In certain embodiments, the buffers are configured to hold command/address signals to control the timing of command/address signals. In some cases, controlling the timing of the command/address signals may reduce or slow signal degradation. In some implementations, the control dies 822 include a plurality of data buffers, which may control the timing of data signals to reduce or slow signal degradation. Further, the control dies 822 may include a data path control circuit (not shown) that is configured to control command/address time slots and data bus time slots. Controlling the command/address time slots and the data bus time slots enables the control dies 822 to *reduce or prevent signal collisions* caused by multiple memory packages 820 sharing the data path control lines 816 and the data bus 818. In some implementations, the data path control circuit may be separate from the control die 822.

Ex. 1001, 21:39–56 (emphasis added). The fact that the '060 patent mentions *reducing or* preventing signal collisions suggests that there is no prohibition on signal collisions. This is in contrast with Dr. Brogioli's more limited view that if there are any data collisions the resulting structure would be inoperable. Ex. 2023 ¶ 150. Moreover, the challenged claims do not recite that data collisions must be avoided, and "[t]he reasonable expectation of success requirement refers to the likelihood of success in combining references *to meet the limitations of the claimed invention*." *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (emphasis added). Thus, Dr. Brogioli's testimony about the lack of "a reasonable expectation of success" (Ex. 2023 ¶ 150) is not commensurate in scope with the claims. Furthermore, the above-quoted passage from the '060 patent does not provide any particular details on how to control timing to reduce or prevent collisions, suggesting that this was within the knowledge and skill of a person of ordinary skill in the art, as Petitioner

asserts. *See* Pet. Reply 2–7. Thus, "the ['060] patent itself does not disclose the level of detail that [Patent Owner] would have us require of the prior art." *See Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1570 (Fed. Cir. 1997).

At oral argument, Patent Owner's counsel argued that the '060 patent "avoids the collisions" by "dramatically remov[ing] the latency on the TSVs," which "dramatically increases the speed at which the load and reads can be cleared." Tr. 40:4–11. According to Patent Owner's counsel, the '060 patent's collision solution is "a physical solution to a timing problem, not a timing solution to a physical problem." Tr. 39:15–40:11 (citing '160 patent at 8:1–21, which corresponds to 7:63–8:18 in the '060 patent). The cited disclosure is below.

> For certain embodiments, the load of each data conduit is less than the maximum load as described above. Thus, in some cases, the load of the data conduit 232a is less than the maximum load and the load of the data conduit 232b is less than the maximum load. Further, in many implementations, the combined load of the data conduit 232a and the data conduit 232b is less than the maximum load of a single data conduit. In other words, it is possible to design the data conduit 232a and the data conduit 232b to reduce the overall load compared to a single data conduit that is in electrical communication with a die interconnect that is in electrical communication with at least one data port of each of the array dies 210. By reducing the overall load compared to the single data conduit, it is possible in many cases to reduce power consumption. Further, it is possible in many cases to maintain signal quality (e.g. maintain signal amplitude, maintain low signal distortion, etc.) while reducing power consumption. Advantageously, in a number of embodiments, by using multiple data conduits instead of a single data conduit, the speed of the memory package 200 can be increased. In some cases, this speed increase can include a

> reduced latency in accessing array dies 210 and/or operating the memory package 200 at a higher clock frequency.

Ex. 1001, 7:63–8:18. This passage says nothing about avoiding collisions. As discussed above, the '060 patent discloses that "[c]ontrolling the command/address time slots and the data bus time slots enables the control dies 822 to reduce or prevent signal collisions." Ex. 1001, 21:51–54. Thus, the '060 patent suggests that there is a timing solution to address collisions, contrary to Patent Owner's counsel's argument. *See* Tr. 39:15–40:11.

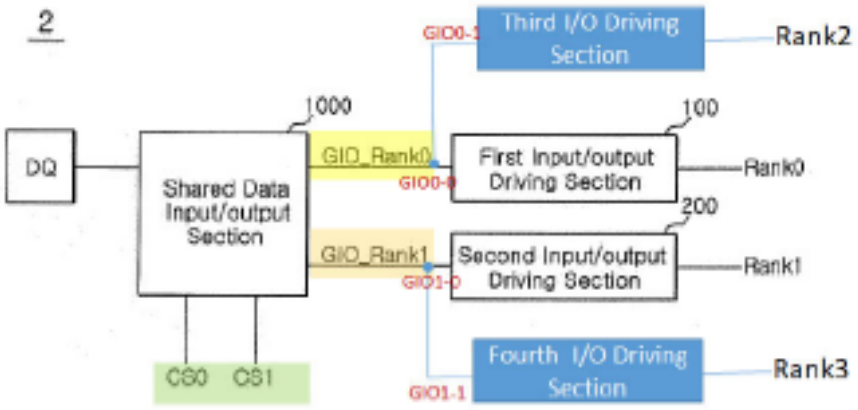
Petitioner asserts that Rajan "provides much more detail than the 060 Patent (EX1001, 21:51–:56) with respect to timing solutions for avoiding collisions." Pet. Reply 6 (citing Ex. 1015, 8:59–12:13, Figs. 9–15). We agree because, as discussed above, the '060 patent simply mentions controlling timing to reduce or prevent collisions but does not provide any particular details on how to do this. Ex. 1001, 21:51–54. Rajan, however, actually explains how to avoid collisions through the timing of various operations. *See, e.g.*, Ex. 1015, 11:12–12:13, Figs. 14, 15. For example, Rajan discloses that "FIGS. 14 and 15 are a timing diagram 1400 and a timing diagram 1500 illustrating methods of avoiding such collisions." Ex. 1015, 11:12–14; *see also* Ex. 1052, 200:15–19 (Dr. Brogioli testified as follows: "It looks like Figure 14 says it's a timing diagram illustrating methods of avoiding such collisions. These look like command collisions of things like activate commands, read and write commands.").

Patent Owner argues that Rajan does not teach how to avoid collisions for operations that "involved cross-rank read-after-write operations and certainly not for Kim's memory systems" and that "[d]elaying write commands will just further delay the write data, and does not solve Kim's data collision problem." PO Sur-reply 8–9 (citing Ex. 1014 ¶ 42, Fig. 4A).

Rajan's disclosure is more robust than simply delaying write operations. For example, Rajan discloses that the buffer chip can delay activate operations by one to three clock cycles and that "[t]he actual delay selected may depend on the presence or absence of other DRAM operations that may conflict with the activate operation, and may optionally change from one activate operation to another. In other words, the delay may be dynamic." Ex. 1015, 11:40–47.

In support of its arguments regarding the fourth configuration, in which four chips belong to four ranks and every two ranks share a TSV, Patent Owner refers to Dr. Brogioli's modification of Kim's Figure 2 below.

FIG.2



PO Resp. 33; Ex. 2023 ¶ 120. Kim's Figure 2 illustrates a memory configuration including shared data input/output (I/O) section 1000 connected via first and second global I/O lines GIO_Rank0 and GIO_Rank1 to first and second I/O driving sections 100 and 200, which are connected, respectively, to Rank0 and Rank1. Ex. 1014 ¶¶ 25–26. The modified figure above includes a third I/O driving section connected between GIO_Rank0 and Rank 2 and a fourth I/O driving section connected between GIO_Rank1 and Rank 3. Ex. 2023 ¶ 120. Dr. Brogioli testifies that this illustrates

Dr. Wolfe's proposal that "Kim could be modified by having four ranks sharing two data busses, for instance, in a rank multiplication scenario." Ex. 2023 ¶¶ 119–120. At deposition, Dr. Brogioli confirmed that he "assume[d] that Kim's circuits would operate the same way as in Kim's original Figure 2." Ex. 1052, 320:5–11.

Dr. Brogioli's assumption of no change in operation with the addition of two ranks fails to account for the combined teachings of Kim and Rajan and the knowledge and skill of a person of ordinary skill in the art. As the Federal Circuit instructs,

> *KSR* does not require that a combination only unite old elements without changing their respective functions. Instead, *KSR* teaches that "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." And it explains that the ordinary artisan recognizes "that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle."

ClassCo, Inc. v. Apple, Inc., 838 F.3d 1214, 1219 (Fed. Cir. 2016) (citations omitted; alteration in original). The Federal Circuit further cautioned in *ClassCo* that the "rationale of *KSR* does not support [the] theory that a person of ordinary skill can only perform combinations of a puzzle element A with a perfectly fitting puzzle element B." *Id.* Here, Dr. Brogioli alleges that the modified figure reflects "a rank multiplication scenario" (Ex. 2023 ¶ 119), but when asked about the fact that there are four ranks but only two chip select signals shown in the modified figure, Dr. Brogioli testified that "Dr. Wolfe didn't articulate anything about additional chip select signals that would relate to what this figure is visualizing." Ex. 1052, 320:12–24. Dr. Wolfe, however, testifies that Rajan teaches "emulation techniques, including rank multiplication techniques" (Ex. 1003 ¶ 165), and that Rajan

teaches rank multiplication by generating chip select signals for each chip in the stack. Ex. 1003 ¶¶ 141, 287 (quoting Ex. 1015, 6:34–38). In particular, Rajan discloses that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." Ex. 1015, 6:34–38. Thus, Dr. Brogioli's modified version of Kim's Figure 2 does not reflect "a rank multiplication scenario" (Ex. 2023 ¶ 119) in view of the teachings of Rajan.

Patent Owner also argues that "the Petition does not present any evidence that memory systems other than JEDEC-compliant SDRAMs would use chip-selection signals to select chips in the stack or process chip-selection signals on a device level (such that there would be a need to send CS signals to the device)." PO Resp. 49 (citing Ex. 2023 ¶¶ 169–171, 193; Ex. 1015, 6:34–38). Dr. Brogioli identifies NAND and SRAM datasheets that he says do not show "pins for chip-select signals." Ex. 2023 ¶¶ 169–170 (citing Ex. 2043, 8; Ex. 2044, 5–6). But at deposition, Dr. Brogioli acknowledged that these devices use chip enable signals. Ex. 1052, 236:23–239:3 (discussing Ex. 2043), 239:10–241:6 (discussing Ex. 2044). We agree with Petitioner that the chip enable signals are used "to select the chip that performs the read/write operation." *See* Pet. Reply 15; Ex. 2043, 16 ("CE# is used to enable the device."); Ex. 2044, 5 (pin for "Chip enable input"). The use of chip enable signals is consistent with the district court construction, which Patent Owner urges "should be applied by the Board," that "'excludes situations in which a chip select signal could *enable* multiple array dies at once.'" *See* PO Resp. 18–19 (quoting Ex. 2004, 33–34 (emphasis added)).

Patent Owner asserts that "[t]here is also no evidence that the concept of 'rank'/'rank multiplication' . . . would apply to non-DRAM memory systems." PO Resp. 49 n.8 (quoting Ex. 1022, 413 ("[T]he word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.")). We disagree for the reasons discussed above in section II.D.2.d.1, which explains that Kim does not even mention DRAM and thus is not limited to DRAM and that Rajan states that "any type of memory whatsoever" may be used in its disclosure and lists non-DRAM memories. Ex. 1015, 15:3–9.[12] Thus, we find that the combined teachings of Kim and Rajan teach ranks and rank multiplication with non-DRAM array dies.

(3) Summary of findings for 1.c, 1.d.1, 1.d.2

For the reasons discussed above, we find that the combination of Kim and Rajan teaches the subject matter of limitations 1.c, 1.d.1, and 1.d.2 and that a person of ordinary skill in the art would have combined the teachings of Kim and Rajan in the manner asserted with a reasonable expectation of success.

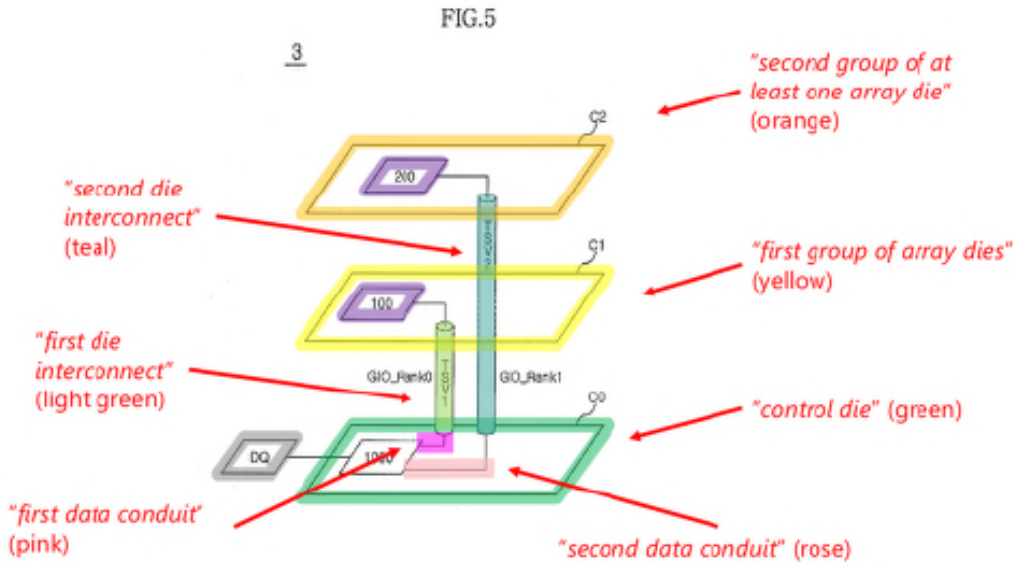
e) Control die (1.e.1), data conduits (1.e.2, 1.e.3), and control circuit (1.e.4)

Claim 1 recites a "control die" (1.e.1) comprising "at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals" (1.e.2) and "at least a second data conduit

[12] We further note that Patent Owner's argument is conclusory and appears only in a footnote. *Cf. CommScope Techs. LLC v. Dali Wireless Inc.*, 10 F.4th 1289, 1296 (Fed. Cir. 2021) ("[A]n argument that is only made in a footnote of an appellant's brief is forfeited.").

between the second die interconnect and the first terminal, the first terminal being a data terminal" (1.e.3).

Petitioner argues that Kim's main chip C0 is a control die and that Kim's Figure 5 (annotated version below) shows first and second data conduits between the TSVs and the data terminals DQ. Pet. 41–45.



Pet. 41. In the annotated figure above, Petitioner identifies the line from TSV1 to shared data I/O section 1000 as "first data conduit" in pink and identifies the line from TSV2 to shared data I/O section 1000 as "second data conduit" in rose. Pet. 42–46. As shown and as Petitioner asserts, the conduits are between the interconnects (TSVs) and the data terminal (DQ). *See* Pet. 42–45.

Claim 1 also recites "the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals" (1.e.4). Petitioner argues that Kim teaches a control circuit in rank selecting unit 1100 that controls the states of the conduits to the TSVs to be active or not active based on signals received

from an external device. Pet. 46–47 (citing Ex. 1014 ¶¶ 32, 35–36, 38, Fig. 3; Ex. 1003 ¶¶ 265–272; Ex. 1019, 6–14, 18, 33; Ex. 1023, 9, Fig. 16; Ex. 1022, 318–20, 332–35).

Patent Owner does not dispute Petitioner's contentions that the combination of Kim and Rajan teaches limitations 1.e.1–1.e.4. Based on Petitioner's persuasive contentions and evidence, summarized above, we find that the combination of Kim and Rajan teaches limitations 1.e.1–1.e.4.

f) Objective evidence of non-obviousness

We must consider any evidence of objective indicia of non-obviousness before reaching our conclusion on obviousness. *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016). This is one of the factual considerations underlying an obviousness determination. *Graham*, 383 U.S. at 17.

Patent Owner argues that the "history of commercial 3DS [(3D-Stacked)] and HBM [(high bandwidth memory)] in particular is objective evidence that the patented design is not obvious." PO Resp. 1. Patent Owner, however, does not make any arguments to establish the nexus required for consideration of secondary considerations. *See ClassCo*, 838 F.3d at 1220 ("For objective evidence of secondary considerations to be accorded substantial weight, its proponent must establish a nexus between the evidence and the merits of the claimed invention." (quotations and citation omitted)); *see also* Tr. 42:9–25 (Patent Owner confirming that it did not present an argument for secondary considerations).

Thus, the record does not contain any supportable arguments for objective indicia of non-obviousness.

g) Conclusion for Claim 1

We have considered the full trial record, and, for the reasons discussed above and based on Petitioner's contentions and evidence, we conclude that the subject matter of claim 1 would have been obvious to a person of ordinary skill in the art based on the combined teachings of Kim and Rajan.

3. Dependent Claim 6

Claim 6 depends from claim 1 and recites "wherein the control die further comprises chip-select conduits, the memory package further comprising: third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies."

Petitioner argues that it would have been obvious to include chip-select conduits and interconnects to conduct the chip-select signals, relying on Rajan's disclosure of using separate chip select signals for each chip. Pet. 57–62 (citing Ex. 1015, 3:27–30, 6:30–7:67; Ex. 1014 ¶¶ 28–30, 32, 49, Figs. 2, 5; Ex. 1019, 12–13, Fig. 2; Ex. 1022, 319, Ex. 1023, 2–4, 9; Ex. 1016 ¶ 38; Ex. 1003 ¶¶ 315–334).

Patent Owner argues that "the Petition does not present any evidence that memory systems other than JEDEC-compliant SDRAMs would use chip-selection signals to select chips in the stack or process chip-selection signals on a device level (such that there would be a need to send CS signals to the device)." PO Resp. 49 (citing Ex. 2023 ¶¶ 169–171, 193; Ex. 1015, 6:34–38). Patent Owner also asserts that "[t]here is also no evidence that the concept of 'rank'/'rank multiplication' . . . would apply to non-DRAM memory systems." PO Resp. 49 n.8 (quoting Ex. 1022, 413 ("[T]he word *rank* is now used to denote a set of DRAM devices that operate in lockstep

to respond to a given command in a memory system.")). We address these arguments above in § II.D.2.d.2 and disagree with them for the reasons explained above.

Patent Owner also argues that "TSVs that penetrate through multiple chips were difficult and expensive to form at the time of the invention" and that "one failed TSV would cause the entire die stack to be discarded." PO Resp. 50 (citing Ex. 2023 ¶¶ 195–196; Ex. 2007; Ex. 2046). Patent Owner includes a parenthetical regarding "a JEDEC presentation that indicated commercially viable speed bin yield would not be viable until 2016." PO Resp. 50 (citing Ex. 2046). According to Patent Owner, a person of ordinary skill in the art "would not have incurred the cost or the risk to build TSVs that are not needed for the memory chips' operation." PO Resp. 50 (citing Ex. 2023 ¶¶ 196–197). The evidence of record shows that a known configuration was to have multiple dies sharing TSVs, as discussed above in § II.D.2.d.2. *See* Ex. 1025 (Foster); *see also* Ex. 2023 ¶ 164 (Dr. Brogioli testifying with respect to Foster about "the dies forming the substack that shares a TSV"). The record evidence shows that using TSVs was within the skill of a person of ordinary skill in the art. *See* Exs. 1014 (Kim), 1025 (Foster). We find that this evidence shows that the use of TSVs was an obvious option for a person of ordinary skill in the art, notwithstanding Patent Owner's commercial viability arguments. *See Uber Technologies, Inc. v. X One, Inc.*, 957 F.3d 1334, 1340 (Fed. Cir. 2020) ("Because a person of ordinary skill 'has good reasons to pursue the known options within his or her technical grasp,' § 103 bars the patentability of such obvious variations." (quoting *KSR*, 550 U.S. at 421)); *cf. CFMT, Inc. v. Yieldup Int'l Corp.*, 349 F.3d 1333, 1338 (Fed. Cir. 2003) ("Title 35 does not require that a patent

disclosure enable one of ordinary skill in the art to make and use a perfected, commercially viable embodiment absent a claim limitation to that effect.").

We find Petitioner's contentions for claim 6 persuasive. Rajan discloses the following:

> If the buffer chip is emulating a memory device which has a larger capacity than each of the physical DRAM chips in the stack, the buffer chip may receive from the host system's memory controller more address bits than are required to address any given one of the DRAM chips. In this instance, the extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack.

Ex. 1015, 6:30–38. Thus, in Petitioner's combination, each chip receives a chip select signal, which supports Petitioner's position that conduits and interconnects conduct those signals to the chips. *See* Pet. 57–62.

Based on Petitioner's persuasive contentions and evidence, summarized above, and for the reasons discussed above, we conclude that claim 6 is unpatentable as obvious over the combined teachings of Kim and Rajan.

4. Claims 2–5, 8–14, 16–19, and 29–34

Below we address Petitioner's contentions for claims 2–6, 8–14, 16–19, and 29–34, which we find persuasive. Patent Owner does not raise arguments for these claims in addition to those already addressed above.

Claim 2 depends from claim 1 and recites "wherein the control signals include data path control signals for controlling the first and second data conduits." Petitioner argues that chip select and read/write command signals would be used per JEDEC to control the direction of data transfer. Pet. 47–49 (citing Ex. 1014 ¶¶ 31–38, Fig. 3; Ex. 1003 ¶¶ 273–280).

Claim 3 depends from claim 1 and recites "wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals." As with claim 2, Petitioner cites chip select and read/write signals as controlling the direction of data transfer. Pet. 49–51 (citing Ex. 1014 ¶ 38, Fig. 3; Ex. 1015, 3:27–30, 6:30–7:67, Fig. 18; Ex. 1003 ¶ 287).

Claim 4 depends from claim 3 and recites "wherein the control signals include command/address signals and wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies." Petitioner argues that the combination of Kim and Rajan teaches that command (write and read) and address signals are received at the memory module and that address signals are sent to the dies to identify where to store or retrieve data. Pet. 51–56 (citing Ex. 1014 ¶ 29–30, 32, 38, Ex. 1015, 14:11–18, 14:55–60, Figs. 4, 18; Ex. 1019, 6–14, 18, 33; Ex. 1022, 318–20, 332–35; Ex. 1023, 9, Fig. 6; Ex. 1003 ¶¶ 291–307).

Claim 5 depends from claim 1 and recites "wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via." As discussed for claim 1, Petitioner relies on Kim's TSVs as the die interconnects. Pet. 56–57 (citing Ex. 1014 ¶¶ 46–49, Fig. 5; Ex. 1003 ¶¶ 308–313).

Claim 8 recites,

> The memory package of claim 1, wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals, wherein the control die is configurable to operate in any one of a first mode and a second mode, and wherein: in the first mode, the control die receives the data path control signals from the one or more external devices; and in the second mode, the control die generates the data path

control signals from at least some of the control/address signals received from the one or more external devices.

Petitioner asserts that the combination of Kim and Rajan teaches data path control signals for the reasons given for claims 2 and 3. Pet. 62–63 (citing Ex. 1014, Fig. 3; Ex. 1003 ¶¶ 352–356). Petitioner argues that the combination of Kim and Rajan teaches a control die that is configurable to operate in two modes, one in which the number of ranks seen by the host system equals the actual number of ranks and the other in which there is rank multiplication. Pet. 62–66 (citing Ex. 1014, Fig. 3, Ex. 1015, code (57), 7:4–67, 14:51–62, Fig. 18; Ex. 1003 ¶¶ 352–376).

Claim 9 depends from claim 1 and recites "wherein the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address." Petitioner argues that the combination of Kim and Rajan teaches that the control die has conduits for the command/address signals discussed for claim 4 and that those signals include a memory cell address. Pet. 66–67 (citing Ex. 1015, 6;46–49, Fig. 18 (box labeled "Physical Storage Memory Cells")).

Claim 10 depends from claim 1 and recites "wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies." Petitioner argues that, in the combination of Kim and Rajan, conduits would provide power to the chips to operate and that a corresponding ground signal would be required to close the circuit. Pet. 67–69 (citing Ex. 1014 ¶¶ 26, Fig. 5; Ex. 1019, 14; Ex. 1016 ¶ 36, Fig. 2; Ex. 1003 ¶¶ 388–396).

Independent claim 11 is directed to a "memory package" and recites limitations substantially similar to subject matter recited in claims 1 and 6. *See* Pet. 69–70 (mapping similar claim limitations). Petitioner argues that the combination of Kim and Rajan teaches the additional subject matter of "driv[ing] a data signal to an array die selected by at least one of the chip-select signals" by sending data through Kim's write selecting unit 1110 to a selected array die. Pet. 70–71 (citing Ex. 1014 ¶¶ 35, 40, Fig. 3; Ex. 1003 ¶¶ 429–432).

Claim 12 depends from claim 11 and recites "wherein the chip select conduits pass through the control die." Petitioner argues that it would have been obvious for chip select signals that are received at the bottom of the memory package to pass through the control die to the array dies above the control die. Pet. 71 (citing Ex. 1015, 6:34–38, Fig. 4; Ex. 1014 ¶¶ 28, 32, Fig. 5; Ex. 1019, 6–11; Ex. 1021, 1–2; Ex. 1022, 374, 476; Ex. 1003 ¶¶ 437–443).

Claim 13 depends from claim 11 and recites "wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies." Petitioner argues that it would have been obvious to use drivers to produce enough current to transmit the chip select signals. Pet. 73 (citing Ex. 1014 ¶ 32; Ex. 1030, 135–36; Ex. 1038, 68; Ex. 1017, 1:14–20; Ex. 1003 ¶ 447).

Claims 14 and 16–19 recite subject matter that is substantially similar to subject matter recited in claims 1–5 and 8, and Petitioner refers to its contentions for similarly-recited subject matter in claims 1–5 and 8. Pet. 74.

Independent claim 29 is directed to a "memory module operable via a memory control hub" comprising "a register device configured to receive

command/address signals from the memory control hub and to generate control signals" and "a plurality of DRAM packages." Claim 29 recites that each DRAM package comprises subject matter that is substantially similar to limitations recited in claims 1, 4, 6, and 11.

Petitioner refers to its contentions for similar subject matter recited in other claims and argues that the combination of Kim and Rajan teaches the additional subject matter of claim 29. Pet. 74–78. In particular, Petitioner argues that the combination teaches a JEDEC memory module that has a register device (Rajan's register 804). Pet. 74–77 (citing Ex. 1015, 1:28–32, 3:5–7, 4:20–24, 8:52–58, 15:3–12, Fig. 8; Ex. 1014 ¶ 50; Ex. 1022, 43–44, 316–20, 418–19, Fig. 7.2; Ex. 1037, 1:34–37, Fig. 1; Ex. 1003 ¶¶ 591–604, 642–649). As discussed above with respect to claim 1, we find that Rajan teaches using non-DRAM memories in a JEDEC-compliant memory package. We also find that the combination of Kim and Rajan teaches "a plurality of DRAM packages" and "a register device configured to receive command/address signals from the memory control hub and to generate control signals" because Rajan discloses "high capacity DIMM 800 using a plurality of buffered stacks of DRAM circuits 802 and a register device 804," which "performs the addressing and control of the buffered stacks." Ex. 1015, 8:52–56; *see* Pet. 76–77 (discussing this disclosure and Fig. 8 of Rajan). We find Petitioner's contentions persuasive for the remaining subject matter of claim 29 for the reasons discussed for similar limitations in claims 1, 4, 6, and 11.

Claim 30 depends from claim 29 and recites "wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select

signals." Petitioner relies on Rajan's disclosure of using separate chip select signals for each chip to show rank multiplication. Pet. 78 (citing Ex. 1015, 3:27–30, 6:30–7:67, 8:56–58; Ex. 1003 ¶¶ 642–649); *see also* Pet. 8–11 (explaining rank multiplication as known in the art).

Claim 31 depends from claim 29 and recites "wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit." Petitioner refers to its contentions for similar subject matter in claims 1 and 2. Pet. 79.

Claim 32 depends from claim 29 and recites "wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal." Petitioner refers to its contentions for similar subject matter in claim 16. Pet. 79.

Claim 33 depends from claim 29 and recites "wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals." Petitioner argues that Rajan teaches delaying signals by two clock cycles and that a person of ordinary skill in the art would have implemented such a delay in Kim to emulate JEDEC. Pet. 79–80 (citing Ex. 1015, 9:46–10:27, Fig. 11; Ex. 1019, 23–24; Ex. 1003 ¶¶ 669–676).

Claim 34 depends from claim 29 and recites "wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit."

Petitioner refers to its contentions for similar subject matter in claims 1 and 3. Pet. 80–81.

As noted above, Patent Owner does not raise additional arguments for these claims. We have reviewed Petitioner's arguments and evidence, and we find them persuasive. Therefore, having considered the full record developed during the trial, we conclude that claims 2–5, 8–14, 16–19, and 29–34 are unpatentable as obvious over the combined teachings of Kim and Rajan.

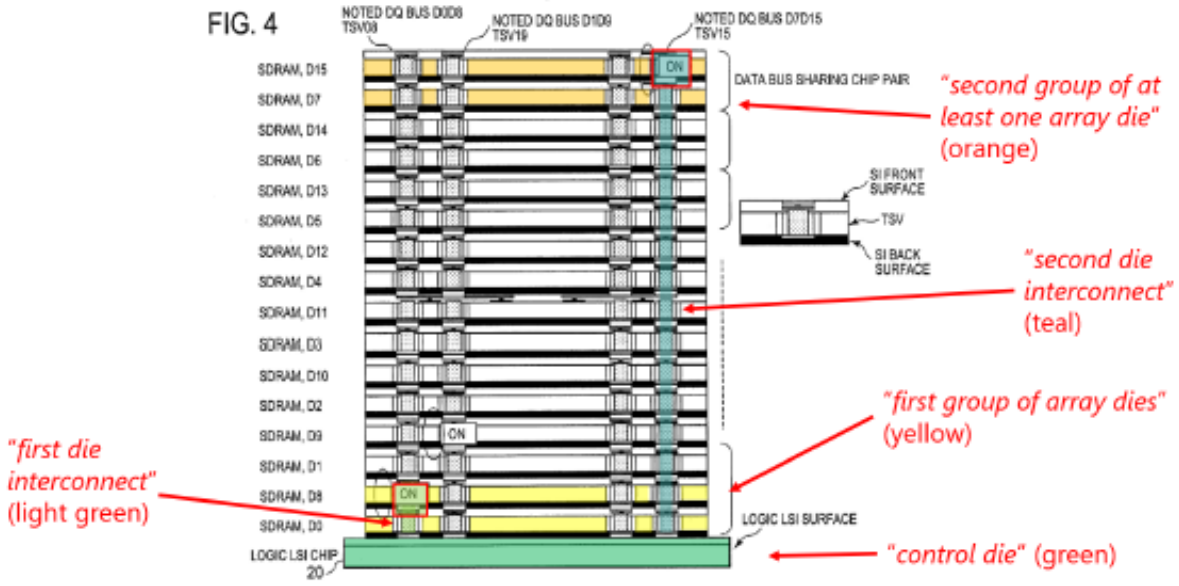
E. Obviousness over Kim, Rajan, and Riho (Claims 1–14, 16–19, 29–34)

In this ground, Petitioner substantively addresses only claim 7 and relies on its contentions based on Kim and Rajan for the remaining claims. Pet. 81–83.

Claim 7 recites,

> The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.

Petitioner provides the annotated version of Riho's Figure 4 below.



Pet. 82. Riho's Figure 4 shows a stack of memory chips in two groups, D0–D7 and D8–D15, and stacked above logic chip 20 from bottom to top in the following order: D0, D8, D1, D9, D2, D10, D3, D11, D4, D12, D5, D13, D6, D14, D7, and D15. Ex. 1016 ¶ 62. In the annotated version of Figure 4 above, Petitioner identifies TSV08 as the "first die interconnect" in light green and TSV15 as the "second die interconnect" in teal. Pet. 82. Petitioner argues that pair D0/D8 is coupled to TSV08 and that pair D7/D15 is coupled to TSV15 and that such pairing can reduce the load. Pet. 82–83 (citing Ex. 1016 ¶¶ 13, 62, 103, 132, Fig. 4; Ex. 1014 ¶¶ 48, 50, 53–54; Ex. 1003 ¶¶ 172–173, 336–350). Petitioner argues that a person of ordinary skill in the art "would have been motivated with a reasonable expectation of success (when adding chips to Kim) to use Riho's technique described above to further reduce the load (allowing for higher-frequency operations) and to compensate for phase variations, as taught by Riho, without the need to create additional TSVs." Pet. 82 (citing Ex. 1014 ¶¶ 48, 50; Ex. 1016 ¶¶ 119–120; Ex. 1003 ¶¶ 172–173).

Patent Owner raises several arguments in response. PO Resp. 51–54; PO Sur-reply 20–22. Patent Owner argues that analogousness is not a sufficient reason to combine the references. PO Resp. 51 (citing Pet. 81). The cited contention is not Petitioner's reason to combine (included in discussion above) but is simply an assertion that Rajan and Riho are analogous art, which is a required showing to prove obviousness. *See Netflix, Inc., v. DIVX, LLC*, 80 F.4th 1352, 1358 (Fed. Cir. 2023) ("[F]or an obviousness determination, a reference may only qualify as prior art that a person of ordinary skill in the art would look to if it is 'analogous to the claimed invention.'" (quoting *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004))). As explained above in § II.D, we find that Kim and Rajan are analogous art to the '060 patent. Patent Owner does not dispute that Riho is analogous art to the '060 patent. *See* PO Resp. We agree with Petitioner that Riho is analogous art because it is in the same field of endeavor as the '060 patent—memory packages and in particular those involving stacked memory. Ex. 1001, 1:20–21 ("The present disclosure relates to memory devices and memory modules."), claim 1 ("memory package" with "stacked array dies"); Ex. 1016 ¶ 2 ("This invention relates to a semiconductor device incorporating DRAM or other chips and, in particular, relates to a semiconductor device formed by stacking a plurality of chips.").

Patent Owner also argues that "unlike Kim where different ranks of memories cannot share a same TSVs, in Riho, pairs of dies from two different ranks are connected to the same TSV," a "material difference" that Petitioner ignores according to Patent Owner. PO Resp. 51–52 (citing Ex. 1014 ¶¶ 42–45, Fig. 5; Ex. 1016 ¶¶ 28–29, 62; Ex. 2023 ¶ 202). We disagree with this argument because the combination of Kim and Rajan

teaches different ranks sharing a TSV, as discussed for claim 1. *See* § II.D.2 above.

According to Patent Owner, "[t]he '060 patent teaches that because loads of TSVs could be significant, the number of array dies in a group might need to be adjusted to account for the TSV load, in order to achieve load balancing on different data conduits." PO Resp. 53 (citing Ex. 1001, 14:3–11, Table 1). Patent Owner argues that "Riho does not do that under Petitioner's own theory" and, therefore, that "[c]ombining Riho and Kim would also not result in the claimed inventions." PO Resp. 53 (citing Ex. 2023 ¶¶ 205–209).

Patent Owner's arguments are not commensurate in scope with claim 7, which does not recite load balancing. Rather, claim 7 recites that the number of array dies in the first and second groups "are selected in consideration of a load of the first die interconnect and a load of the second die interconnect *so as to reduce* a difference between a first load on the first data conduit and a second load on the second data conduit" (emphasis added). Thus, the prior art need not teach a balanced load to render obvious the claimed subject matter. Indeed, the '060 patent discloses that in some embodiments, "the load of each conduit 332 and/or driver 334 may differ" and that "[t]his difference in the load of the conduits 332 and/or drivers 334 may be a design decision." Ex. 1001, 14:14–17.

Patent Owner contends that Petitioner "simply announces that two chips per group would satisfy 7[a], without explaining why this resulted from 'consideration of' the TSV loads." PO Resp. 53 (citing Pet. 82–83). We disagree. Claim 7 is directed to a memory package that is claimed in part by the process by which numbers of dies are selected, specifically that

the numbers of dies "are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit."[13] Claim 7, however, does not recite that load is the only consideration, nor does it recite the starting point from which "to reduce a difference between" loads. Riho discloses the following:

> [W]hen the controlled chips are divided into a plurality of groups and the penetrating through substrate vias are commonly used by the controlled chips of the respective groups, it is possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used.

Ex. 1016 ¶ 13; *see* Pet. 83 (citing this disclosure). This disclosure makes clear that chip grouping is based on TSV load considerations.

Petitioner argues that Riho's disclosure of minimizing "skew between data signals DQ and data strobe signals DQS/B" (Ex. 1016 ¶ 50) teaches the subject matter reciting "so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit." Pet. 83 (citing Ex. 1016 ¶¶ 50, 53–54; Ex. 1003 ¶¶ 336–343). Patent Owner counters that, "in Riho, the skew between DQ and DQS/B is minimized by making the corresponding TSVs 'substantially equal in length to each other.'" PO Resp. 52 (quoting Ex. 1016 ¶ 50; citing Ex. 1016 ¶ 53; Ex. 2023

[13] Neither party asserts that this is a product-by-process claim. *Kamstrup A/S v. Axioma Metering UAB*, 43 F.4th 1374, 1381 (Fed. Cir. 2022) ("A product by process claim is one in which a product is claimed, at least in part, by the 'process by which it is made.'" (quoting *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985)). Because we conclude that the subject matter of claim 7 would have been obvious, we do not address whether this is a product-by-process claim element that does not impart patentable weight to the claim. *See id.* at 1382.

¶ 203). But as Petitioner points out, Riho discloses using an equal number of dies in each group as part of its structure of using equal length TSVs. *See* Pet. Reply 17. We agree with Petitioner, and we find, that Riho's die grouping teaches that numbers of dies are selected for groups based on load considerations, even if other considerations are used or are even more prominent. *See* Ex. 1016 ¶¶ 13 (disclosing that dividing chips into a plurality of groups and sharing TSVs makes it "possible to reduce the load of the interconnections as compared with the case where the penetrating through substrate vias are not commonly used"), 103 ("[B]y employing the structure in which the stacked SDRAM chips are divided into the groups (chip selection groups) and the through-silicon vias (TSVs) are each shared by the groups, it is possible to reduce by half the load of each SDRAM chip as compared with the case where the SDRAM chips are not divided into the groups.").

Patent Owner also argues that Petitioner never asserted that, in the proposed combination, the TSVs of Kim, which are not of equal length, would be made equal length according to the teachings of Riho. PO Sur-reply 20–21. We disagree because Petitioner asserts that a person of ordinary skill in the art "would have been motivated with a reasonable expectation of success (when adding chips to Kim) to use Riho's technique described above," referring to Riho's Figure 4 showing pairs of chips connected to equal length TSVs. Pet. 82 (citing Ex. 1016 ¶¶ 62, 103, Fig. 4; Ex. 1014 ¶¶ 48, 50; Ex. 1003 ¶¶ 172–173). But even if the proposed combination uses Kim's unequal length TSVs, Riho still provides a teaching of considering load when grouping dies, as discussed above. As the Supreme Court stated in *KSR*, "[w]hat matters is the objective reach of the

claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR*, 550 U.S. at 419. Here, claim 7 does not recite any particular amount of reduction of load difference nor the starting point from which to determine whether there is a reduction. We find that Riho's teachings show that a person of ordinary skill in the art would consider TSV load when grouping dies "so as to reduce a difference" between loads on conduits. Whether or not there actually is a reduction in the difference in loads from a particular starting point is not a question we must resolve as it is not required by claim 7.

Having considered the full record developed during the trial, we conclude that claim 7 is unpatentable as obvious over the combined teachings of Kim, Rajan, and Riho for the reasons discussed above and given by Petitioner. We also conclude that claims 1–6, 8–14, 16–19, and 29–34 are unpatentable as obvious for the reasons given above in § II.D.

F. Obviousness over Kim, Rajan, and Wyman (Claims 1–6, 8–34)

In this ground, Petitioner substantively addresses the additional subject matter pertaining to drivers recited in claims 15 and 20–28 and relies on its contentions based on Kim and Rajan for the remaining claims. Pet. 84–91.

Claim 15 recites,

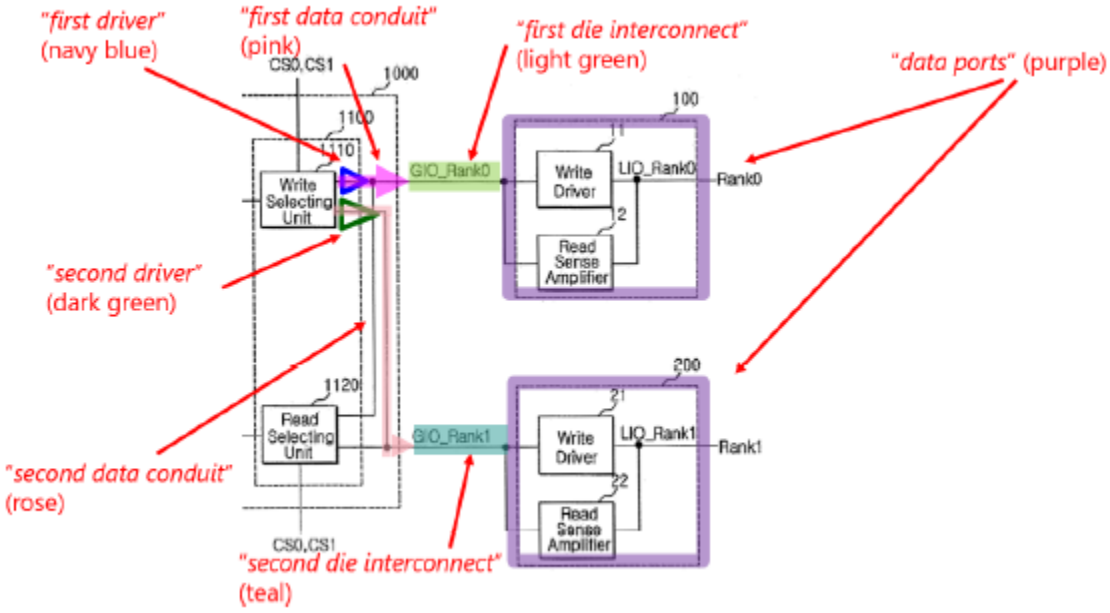
> The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

Petitioner argues that it would have been obvious for the data conduits to have drivers of different strengths for the TSVs of different lengths in Kim based on Wyman's teachings of using different amounts of drive that are adequate for different path lengths. Pet. 84–89 (citing Ex. 1017, 1:22–24, 1:45–48, 6:15–50, 6:57–60, 7:13–18, Fig. 8; Ex. 1014 ¶¶ 3, 46, Figs. 3, 5; Ex. 1030, 135–38; Ex. 1003 ¶¶ 174–181, 456–464). Petitioner contends that

> Kim's TSV1 and TSV2 are each coupled to circuitry in some, but not all, of the slave chips in the stack, requiring less driver strength than if *all* the slave chips were connected, and Wyman teaches to choose a driver size that will "adequately drive" the signal but is still less than the "total drive," which would be "overkill" and inefficient.

Pet. 88–89 (citing Ex. 1003 ¶¶ 465–471; Ex. 1017, 1:45–47, 6:57–60); *see* Ex. 1017, 6:57–60 (disclosing that "a designer could assess the amount of drive needed . . . to adequately supply the signal to the devices (902, 904, 906) as needed while using less than the total drive a drive circuit of the prior art might supply").

Below is Petitioner's annotated version of a portion of Kim's Figure 3.



Pet. 86, 88. The portion of Kim's Figure 3 above shows rank selecting unit 1100 as part of shared data I/O section 1000 including write selecting unit 1110 and read selecting unit 1120. Ex. 1014 ¶¶ 34–35. Petitioner modifies the figure above to include a navy blue triangle representing a "smaller driver" between write selecting unit 1110 GIO_Rank0 (first die interconnect) and a larger dark green triangle representing a "larger driver" between write selecting unit 1110 and GIO_Rank1 (second die interconnect). Pet. 85–88.

Patent Owner presents two main arguments in response to Petitioner's reliance on Wyman: (1) that Wyman teaches using a single driver such that a person of ordinary skill in the art would not have used different drivers as recited in the claim; and (2) that Wyman and Kim do not suggest that TSVs of different lengths in Kim would warrant using different amounts of drive. PO Resp. 54–55.

We disagree with Patent Owner's second argument because it ignores the express disclosure of Wyman. Figure 8 of Wyman is below.

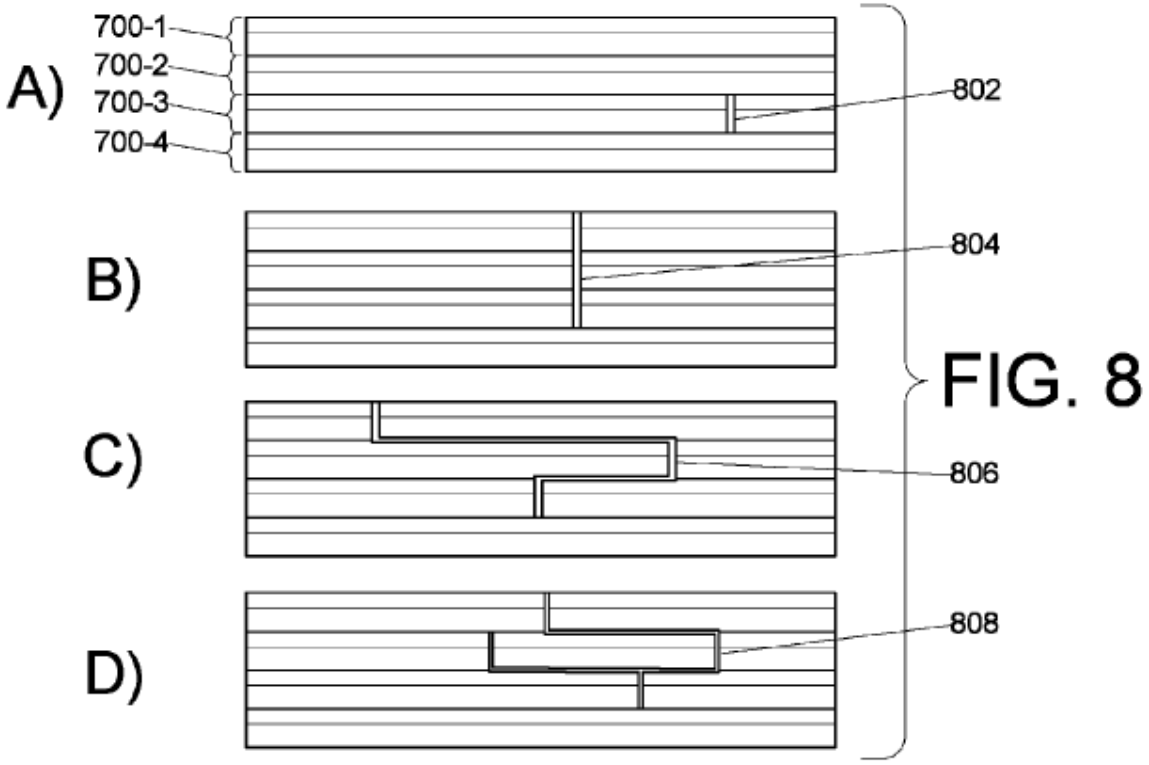


FIG. 8

Wyman's Figure 8 above shows "different through-chip via connections" for stacked chips 700-4 (the "mother chip") and 700-1, 700-2, and 700-3 (the "daughter chips"). Ex. 1017, 2:21–23, 6:9–14. Figure 8A shows through-chip via connection 802 from mother chip 700-4 to the closest daughter chip labeled 700-3, and Figure 8B shows through-chip via connection 804 from mother chip 700-4 to the farthest daughter chip labeled 700-1. Ex. 1017, 6:15–23. Wyman discloses that "[t]he increased resistance, capacitance and impedance of such a connection (804) might require additional drive than that referred to in connection with FIG. 8A" and that the drive used for connection 802 "would be inadequate." Ex. 1017, 6:24–28. Based on this disclosure of Wyman, we agree with Petitioner that "Wyman discloses that shorter paths (e.g., 802 . . .) have less

load and thus require less drive, while longer paths (e.g., 804 . . .) have more load and thus require a larger drive." *See* Pet. 84.

We also have considered the following testimony from Dr. Brogioli:

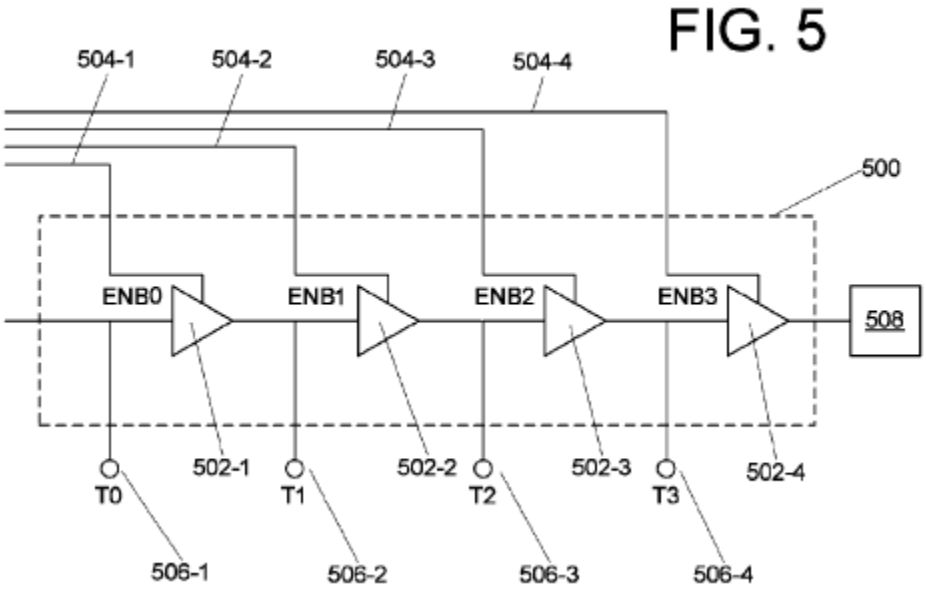
> Third, Wyman and Kim do not suggest that the two TSVs with different lengths would result in sufficiently different load to even warrant using different taps in a Wyman-style driver. For instance, load contribution from TSV "may be negligible compared to load contribution from the array dies." *See* EX1001, 4:36-38. In such situations, same driver strengths can be used and a driver circuitry like that shown in Wyman, Figure 2 will suffice.

Ex. 2023 ¶ 216. The quoted passage from the '060 patent states in full: "*In some embodiments*, the load contribution from a die interconnect may be negligible compared to the load contribution from the array dies." Ex. 1001, 4:36–38 (emphasis added). Dr. Brogioli may be correct that, "[i]n such situations, same driver strengths can be used." Ex. 2023 ¶ 216. Wyman, however, expressly discloses a different situation in which the signal drive for a shorter connection "would be inadequate" for a "longer through-chip via connection" due to "increased resistance, capacitance and impedance of" the longer connection. Ex. 1017, 6:21–30. Wyman also discloses that output drive can "meet the requirements of a particular output load." Ex. 1017, 7:13–18.

Based on the foregoing, we find that Wyman teaches using different amounts of signal drive for different lengths of TSVs and that, in the proposed combination in which different sets of chips are connected to different length TSVs, each drive amount would be less than the total amount needed to drive a signal to all chips.

We next turn to Patent Owner's argument that Wyman teaches using a single driver. More particularly, Patent Owner argues that Wyman teaches a

single driver circuit with different taps at which different drive levels can be selected. PO Resp. 54–55 (citing Ex. 1017, 1:36–37, 2:66–3:1, 6:15–50; Ex. 2023 ¶ 211). Patent Owner's contentions refer to a configuration such as the one below in Figure 5 of Wyman.



Wyman's Figure 5 above shows current drive portion 500 including driver circuits 502-1, 502-2, 502-3, and 502-4, each of which, via respective enabling leads 504-1, 504-2, 504-3, and 504-4, can be enabled, disabled, or placed in a tri state where minimal power is drawn. Ex. 1017, 3:37–41, 4:66–5:11. Wyman explains that "a designer may now utilize and tap-off at five locations (506-1 [T0], 506-2 [T1], 506-3 [T2], 506–4 [T3], 508) depending on the drive requirements for a specific element or device." Ex. 1017, 5:11–14.

According to Patent Owner, "Wyman's driver circuitry, once fabricated, would be regarded as a single driver of a given size regardless of the number of driver components used." PO Resp. 55 (citing Ex. 2024, 141:18–145:14, 145:24–146:7, 149:24–150:8; Ex. 2023 ¶ 215). Patent Owner argues, therefore, that a person of ordinary skill in the art would not

have used different drivers but, instead, would have used a single driver with selectable drive levels. PO Resp. 55 (citing Ex. 1017, 6:44–50; Ex. 2023 ¶¶ 213–214).

Patent Owner's proposed combination of using a single driver may be an acceptable option and may be even a better option than having separate drivers. The proposed combination, however, need not be the best option. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("Our caselaw is clear. It's not necessary to show that a combination is 'the *best* option, only that it be a *suitable* option.'" (quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014))). Petitioner proposes using separate drivers in its annotation of Kim's Figure 3, which is reproduced above in this section. *See* Pet. 85–86 (asserting that a person of ordinary skill in the art would have been motivated to use "a smaller driver (navy blue) for the shorter TSV1 (light green) and a larger driver (dark green) for the longer TSV2 (teal)"). Dr. Wolfe testifies that "you can provide a separate copy of [Wyman's] circuit 500 for each thing that needs to be driven after you analyze the current requirements." Ex. 2025, 129:2–7, *cited in* Pet. Reply 18–19. As noted above, Wyman teaches using different amounts of signal drive for different lengths of TSVs. We see no patentable distinction between whether the different amounts of drive come from one set of transistors that can be tapped for different drive strengths or from two different sets of transistors. *See In re Harza*, 274 F.2d 669, 671 (CCPA 1960) ("It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced . . . .").

According to Patent Owner, Petitioner's proposal to use different driver circuits for different TSVs "relies on nothing more than appeal to

common sense, which is improper under *Arendi*." PO Sur-reply 23–24 (citing *Arendi SARL v. Apple Inc.*, 832 F.3d 1355 (Fed. Cir. 2016)). We disagree that Petitioner's position relies on nothing more than common sense because Wyman teaches using different amounts of signal drive for different TSVs, as discussed above. That physically separate drivers could be used to produce different amounts of drive in different paths is an unremarkable observation. *See KSR*, 550 U.S. at 421 ("Rigid preventative rules that deny factfinders recourse to common sense . . . are neither necessary under our case law nor consistent with it.").

Patent Owner and Dr. Brogioli also rely on testimony from Dr. Harold Stone, a technical expert for the Micron entities in district court litigation. *See* Ex. 2024, 141:18–145:14, 145:24–146:7, 149:24–150:8, *cited in* PO Resp. 55 and Ex. 2023 ¶ 215. In this line of questioning, Dr. Stone confirmed that his testimony was based on a hypothetical in which you could "turn on all ten transistors," and he explained that "[i]f you can turn on all ten, the driver size is related to the load that you can drive. And if you're going to drive ten transistors, you have to have enough area to dissipate the power they generate." Ex. 2024, 147:3–11. This testimony, therefore, does not concern the situation in which different and separate drivers drive separate loads, as in Petitioner's proposed combination discussed above.

Furthermore, although Wyman discloses that different taps can be provided to provide different drive levels, Wyman also discloses an alternative configuration in which taps are not used, as Petitioner correctly points out. *See* Pet. Reply 19 (citing Ex. 1017, 5:34–44). More particularly, Wyman discloses that its "approach could be used with a conventional drive circuit made up of multiple stages by using a via approach." Ex. 1017,

5:35–44. In this configuration, Wyman discloses forming an "electrically conductive connection to an intermediate point between stages where the current drive is adequate, as needed, and to disable any remaining downstream stage(s) by using a via to break one or more connections and leaving the via unfilled or filling the via with an insulator." Ex. 1017, 5:35–44. Thus, Wyman expressly discloses that a suitable option involves disabling unneeded transistors and not using taps to provide selectable drive levels. *See Intel*, 21 F.4th at 800. Furthermore, we find that Wyman's disclosure of providing different drive strengths with different numbers of transistors would result in drivers of different physical size, consistent with the disclosure of the '060 patent that "[t]he size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver." Ex. 1001, 17:43–45; *see* Pet. Reply 19 (discussing this disclosure); *see also* Ex. 2024, 147:7–9 (Dr. Stone's testimony that "the driver size is related to the load that you can drive").

Based on the foregoing, we find that Wyman teaches using different amounts of signal drive for different lengths of TSVs and that a person of ordinary skill would have recognized that different, physically separate drivers can be used to provide those different amounts of signal drive. We also find that a person of ordinary skill in the art would have combined Wyman's teachings with Kim and Rajan "to meet the requirements of a particular output load" and to avoid using more drive power than necessary for each path. Ex. 1017, 7:13–18; *see also* Ex. 1017, 1:22–24 ("In instances where chips are stacked, creating shorter runs, utilizing the full capacity of a driver would be both wasteful and inefficient since far less power is required."); Ex. 1003 ¶ 179 ("A Skilled Artisan would have understood, and

been motivated, to turn to analogous art, like Wyman teaching about efficiently driving signals between stacked devices, in order to implement the stacked devices of Kim."). We also find that this combination teaches providing sufficient drive "without significant signal degradation," as recited in claim 15, because Wyman discloses meeting the requirements of the load. Ex. 1017, 7:13–18; Ex. 1003 ¶¶ 469–471).

Having considered the full record developed during the trial, we conclude that claim 15 is unpatentable as obvious over the combined teachings of Kim, Rajan, and Wyman for the reasons discussed above and given by Petitioner.

Independent claim 20 is directed to a "method for optimizing load in a memory package" and recites structure and method steps that correspond to limitations discussed for claims 1, 4, 6, 11, and 15, and Petitioner refers to its contentions for similarly-recited subject matter in those claims. Pet. 89–90. For claims 21–28, which depend directly or indirectly from claim 20, Petitioner refers to its contentions for similarly-recited subject matter in claims 3–5, 11, 12, 15, and 16. Pet. 90–91. Patent Owner does not raise arguments in addition to those already addressed above.

We have reviewed Petitioner's arguments and evidence, and we find them persuasive for the reasons discussed above for claims 1–6, 11, 12, 15, and 16. Therefore, having considered the full record developed during the trial, we conclude that claims 20–28 are unpatentable as obvious over the combined teachings of Kim, Rajan, and Wyman.

We also conclude that claims 1–6, 8–14, 16–19, and 29–34 are unpatentable as obvious for the reasons given above in § II.D.

G. Patent Owner's Procedural Arguments

Patent Owner makes various procedural arguments with which we disagree as discussed below.

1. Alleged Improper Incorporation by Reference

Patent Owner asserts that, "[t]hroughout the Petition, Petitioner tries to evade the word limit by including no substantive analysis in the Petition itself, but attempting to incorporate paragraphs and paragraphs of its expert's declaration." PO Resp. 19. As example, Patent Owner notes that "Petitioner devotes two paragraphs in Ground 1" for limitations 1.d.1. and 1.d.2 but cites eleven paragraphs of its expert declaration. PO Resp. 19. Patent Owner asserts that "[t]his is improper, and such arguments should be deemed as absent from the Petition itself." PO Resp. 19.

We disagree with Patent Owner that there is "no substantive analysis" for certain limitations, and we refer to our findings above as to the Petition's analysis. Furthermore, there is no prohibition on expert declarations that provide more discussion of claim limitations than a petition. Indeed, our Rules provide that "[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight." 37 C.F.R. § 42.65(a). Thus, an expert declaration should provide the necessary factual bases underlying the declarant's opinion, and the expert is not limited to only what a petitioner asserts in a petition.

2. Alleged Improper New Arguments

Patent Owner argues that having each die in the stack in a separate rank with its own chip select signal is a "new argument" that we should not consider. PO Sur-reply 19. At oral argument, Patent Owner's counsel stated, "I heard so many times, I couldn't count, oh, our combination is a

chip select for each die. So, in Riho, that would be 16 chip selects, and in Kim plus Rajan, that would be a chip select for each separate chip. That is nowhere in their petition." Tr. 36:25–37:2.

We disagree with Patent Owner because the Petition cites Rajan's disclosure of providing a separate chip select signal for each chip in the stack for claim 6. *See* Pet. 61 (citing Ex. 1015, 6:34–38). Thus, Patent Owner's contention that this is "nowhere in their petition" is incorrect. Petitioner's reliance on this disclosure for claim 1 in the Reply was an appropriate response to Patent Owner's arguments about collisions. *See Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 706 (Fed. Cir. 2020) ("[A]ny ambiguity as to whether Apple raised a new argument on reply is eliminated when we consider whether Apple's reply arguments are responsive to arguments raised in Andrea's Patent Owner Response.").

Patent Owner is also incorrect in asserting that having each die in the stack in a separate rank is a new argument. The Petition states the following:

> [W]hen implementing "rank multiplication" (discussed above, pp.8-11), it was common to use a "fork-in-the-road" arrangement with two data buses for two ranks of memory devices (shown below left, yellow and orange), with the option of adding two additional ranks of memory devices (*resulting in four ranks*) to the existing data busses (shown below right, two yellow, two orange), meaning two memory dies (e.g., two orange) would share a given data bus.

Pet. 29 (emphasis added; citing Ex. 1003 ¶ 165; Ex. 1026, Figs. 12–13). This passage refers to annotated versions of Figures 12 and 13 of U.S. Patent Application Publication No. 2006/0277355 A1 (Ex. 1026 ("Ellsberry")). Thus, the Petition expressly proposes four separate ranks in the combination. *See also* Pet. 8 (discussing rank multiplication and citing Ex. 1015, 6:30–

7:67 (Rajan's disclosure of using separate chip select signals for each chip)). Indeed, Patent Owner's declarant Dr. Brogioli testifies that, "in Ellsberry, the 4 ranks are in four separate physical ranks." Ex. 2023 ¶ 111. Petitioner, therefore, put Patent Owner on notice of its contention of using separate ranks. The passage quoted above also expressly states that "it was common to use a 'fork-in-the-road' arrangement." Pet. 29. Thus, we also disagree with Patent Owner's assertions that "fork in the road" is not in the Petition. *See, e.g.*, Tr. 37:4–7 ("The concept of a fork in the road is the magical elixir that makes clear that Rajan has a shared data interconnect, data terminal, and that the prior art references would share that data terminal. That is nowhere in the petition or the declaration."); 70:16–17 ("Where does the fork in the road . . . appear in their petition? It does not.").

Patent Owner also asserts that Petitioner's arguments about known solutions to collisions are "new arguments that should be disregarded." PO Sur-reply 2–3; *see also* PO Sur-reply 16–17 (asserting that Petitioner's "suggest[ion] that Kim's timing for read and write operations would change in the Kim-Rajan combination . . . is a new theory"). We disagree. Patent Owner asserts in its Response that having dies share a TSV would result in collisions. PO Resp. 32–44. In this case, Petitioner's arguments that there were known solutions to data collision issues are directly responsive to Patent Owner's collision arguments. *See Apple*, 949 F.3d at 706; *see also Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1385 (Fed. Cir. 2023) (finding proper a "reply argument discussing cost and time savings [that] has a nexus to [a] prior argument and is responsive").

Furthermore, Petitioner's discussion of the skilled artisan's knowledge of collision avoidance solutions is proper because it "it is used 'to document

the knowledge that skilled artisans would bring to bear in reading the prior art identified as producing obviousness.'" *Anacor Pharms., Inc v. Iancu*, 889 F.3d 1372, 1380–81 (Fed. Cir. 2018) (quoting *Genzyme Therapeutic Prods. Ltd. P'ship v. Biomarin Pharm. Inc.*, 825 F.3d 1360, 1369 (Fed. Cir. 2016)).

We also find Petitioner's reliance on *Lockwood* to be appropriate in pointing out that the prior art contains more detail on avoiding collisions than the '060 patent, which is directly responsive to Patent Owner's criticisms of the asserted combination. *See* Pet. Reply 12 (citing *Lockwood*, 107 F.3d at 1570); *but see* Tr. 39:3–9 (Patent Owner's counsel's assertion that "[t]his Lockwood argument, an argument just like essentially every argument that was made by Samsung in this oral argument was an argument in reply. And the reason why it was put in reply is so their expert can't have been tested on it, because if he would have been tested upon it, he would have told the truth, which is that there's a basic physics behind the speed at which a given memory die can clear a load or clear a read.").

Patent Owner also asserts that Petitioner's argument that a person of ordinary skill in the art "could use different driver circuits for different TSVs" rather than using "a single driver" is "a new argument." PO Sur-reply 23. Petitioner's reliance on different drivers of different sizes is not a new theory because the Petition expressly asserts this and illustrates it, as discussed above in § II.D.2.e. In particular, Petitioner asserts that a person of ordinary skill in the art "would have been motivated to implement Wyman's teachings in Kim to improve power efficiency by using a smaller driver (navy blue) for the shorter TSV1 (light green) and a larger driver (dark green) for the longer TSV2 (teal), as shown below," referring to an

annotated version of a portion of Kim's Figure 3. Pet. 85–86 (illustrating separate drivers). Patent Owner acknowledges as much by arguing that a person of ordinary skill in the art "would not have even used different drivers to drive TSV1 and TSV2 *as asserted*." PO Resp. 55 (emphasis added; citing Pet. 85). Thus, our Decision relies on the Petition's express assertions of separate drivers.

Patent Owner further asserts that reliance on non-DRAM devices such as NAND flash and SRAM is improper and "a complete violation of due process" because "the petition makes no discussion of NAND Flash and no discussion of SRAM as being a basis for the combination." Tr. 55:12–17. We disagree. Before institution, we authorized Petitioner to file a preliminary reply addressing the district court's construction of "array dies," and we authorized Patent Owner to file a preliminary sur-reply. Ex. 3001. In the preliminary reply, Petitioner cited disclosure in Rajan that allows for "any type of memory whatsoever" to be used, including NAND flash and SRAM. Paper 9 at 3 (quoting Ex. 1015, 15:3–9). The Petition also cites this disclosure. *See* Pet. 75 (citing Ex. 1015, 15:3–12). The Decision on Institution discussed this disclosure in view of Patent Owner's argument that array dies must be different from Rajan137's DRAM circuits. Inst. Dec. 23–24. Thus, Patent Owner was provided with notice and an opportunity to be heard. *See Apple Inc. v. Corephotonics, Ltd.*, 81 F.4th 1353, 1361 (Fed. Cir. 2023) (stating that the Board's "decisions must be reached only after the parties have been provided fair notice and an opportunity to be heard").

H. Remaining Grounds

Because we determine that all challenged claims are unpatentable as discussed above, we need not separately assess the remaining grounds of

unpatentability based on the combinations of Riho and Rajan and Riho, Rajan, and Riho2. 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d)."); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (nonprecedential) ("We agree that the Board need not address issues that are not necessary to the resolution of the proceeding.").

III. PETITIONER'S MOTION TO EXCLUDE

Petitioner filed a Motion to Exclude Exhibits 2024, 2026, 2027, and 2029–2031. Paper 34. Because we do not rely on this evidence in a manner adverse to Petitioner, we dismiss the Motion to Exclude as moot.

IV. CONCLUSION[14]

For the reasons discussed above, we determine that Petitioner has proven, by a preponderance of the evidence, that claims 1–34 of the '060 patent are unpatentable, as summarized in the following table:

[14] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–6, 8–14, 16–19, 29–34	103(a)	Kim, Rajan	1–6, 8–14, 16–19, 29–34	
1–14, 16–19, 29–34	103(a)	Kim, Rajan, Riho	1–14, 16–19, 29–34	
1–6, 8–34	103(a)	Kim, Rajan, Wyman	1–6, 8–34	
1–14, 16–19, 29–34	103(a)	Riho, Rajan[15]		
1–34	103(a)	Riho, Rajan, Riho2		
Overall Outcome			1–34	

V. ORDER

Accordingly, it is

ORDERED that claims 1–34 of the '060 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude (Paper 34) is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

[15] As explained above, because we determine that the challenged claims are unpatentable based on the combinations with Kim and Rajan, we decline to address the remaining grounds.

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EXHIBIT B

Trials@uspto.gov
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Paper 52
Date: June 17, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE OFFICE OF THE DEPUTY UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DEPUTY DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-01427 (Patent 9,318,160 B2)
IPR2022-01428 (Patent 8,787,060 B2)

Before DERRICK BRENT,[2] *Deputy Under Secretary of Commerce for Intellectual Property and Deputy Director of the United States Patent and Trademark Office*.

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed petitions in IPR2023-00882 and IPR2023-00883 and were joined as parties to these proceedings. *See* IPR2022-01427, Paper 25; IPR2022-01428, Paper 25.

[2] Katherine K. Vidal, Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office, took no part in this decision. The Director's authority is delegated to Derrick Brent, Deputy Under Secretary of Commerce for Intellectual Property and Deputy Director of the United States Patent and Trademark Office, by operation of

ORDER

The Office received a request for Director Review of the Final Written Decision in each of the above-captioned cases. *See* IPR2022-01427, Paper 50; Ex. 3100; IPR2022-01428, Paper 50; Ex. 3100. Director Vidal is recused from this matter, and the request was referred to me.

Upon consideration of the request, it is:

ORDERED that the requests for Director Review are denied; and

FURTHER ORDERED that the Patent Trial and Appeal Board's Final Written Decision in these cases is the final decision of the agency.

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the Director's Memorandum § II. c. *See* Director's Memorandum, Procedures for Recusal to Avoid Conflicts of Interest and Delegations of Authority (Apr. 20, 2022) (Recusal Procedure Memo), available at www.uspto.gov/sites/default/files/documents/Director-Memorandum-on-Recusal-Procedures.pdf.

IPR2022-01427 (Patent 9,318,160 B2)
IPR2022-01428 (Patent 8,787,060 B2)

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