UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2014-00970
U.S. Patent 8,001,434 B1

NETLIST INC.'S NOTICE OF APPEAL
TO THE U.S. COURT OF APPEALS FOR THE FEDERAL CIRCUIT

Via PRPS
Patent Trial and Appeal Board

Via Hand Carry
Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

Via CM/ECF
United State Court of Appeals for the Federal Circuit

Pursuant to 35 U.S.C. §§ 141, 142, and 319, 37 C.F.R. §§ 90.2, 90.3, and 104.2, and Rule 4(a) of the Federal Rules of Appellate Procedure, Patent Owner Netlist, Inc. hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision (Paper 32) entered by the Patent Trial and Appeal Board on December 14, 2015. In particular, Patent Owner identifies the following issues on appeal:

- The Board's judgment that Claims 1, 14, 15, 19–25, and 27–34 of U.S. Patent No. 8,001,434 B1 are unpatentable;
- The Board's claim constructions; and
- Any Board finding, determination, judgment, or order supporting or related to the Final Written Decision and decided adversely to Patent Owner.

Patent Owner is concurrently filing true and correct copies of this Notice of Appeal, along with the required fees, with the United States Court of Appeals for the Federal Circuit, and with the USPTO Patent Trial and Appeal Board.

Respectfully submitted,

Dated: June 29, 2016

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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PRPS, a true and correct copy of the above-captioned **NETLIST, INC.'S NOTICE OF APPEAL** is being filed by hand with the Director on June 29, 2016, at the following address:

Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

The undersigned also herby certifies that a true and correct copy of the above-captioned **NETLIST INC.'S NOTICE OF APPEAL** and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on June 29, 2016.

Dated: June 29, 2016

/*Thomas J. Wimbiscus*/
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CERTIFICATE OF SERVICE

The undersigned hereby certified that the foregoing **NETLIST INC.'S NOTICE OF APPEAL** was served electronically via e-mail on June 29, 2016 in its entirety on the following:

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Paper 32
Entered: December 14, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00970
Patent 8,001,434 B1

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and PETER P. CHEN, *Administrative Patent Judges.*

GAUDETTE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Sandisk Corporation ("Petitioner") filed a Petition (Paper 1, "Pet.") on June 18, 2014, requesting institution of an *inter partes* review of claims 1–35 (the "challenged claims") of U.S. Patent No. 8,001,434 B1 (Ex. 1001, "the '434 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp."). Based on these submissions, an *inter partes* review of claims 1, 2, 5–15, and 17–35 was instituted on December 16, 2014, pursuant to 35 U.S.C. § 314. Paper 12 ("Dec. on Inst." or "Institution Decision").

After institution, Patent Owner filed a Response (Paper 16, "PO Resp."), and Petitioner filed a Reply to the Patent Owner Response (Paper 23, "Reply").

Patent Owner also filed a Motion for Observation Regarding Cross-Examination of Dr. Donald Alpert. Paper 26 ("PO Mot."). Petitioner filed a Response to the Motion (Paper 30, "Pet. Resp."). Oral argument was held on July 27, 2015. A transcript of the oral hearing ("Tr.") has been entered into the record. *See* Paper 31.

The Board has jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision, issued pursuant to 35 U.S. C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1, 14, 15, 19–25, 27–34 of the '434 patent are unpatentable. Petitioner has not met its burden to show that claims 2, 5, 6, 7–13, 17, 18, 26, and 35 are unpatentable.

A. Related Proceedings

Petitioner also requested, and we instituted, an *inter partes* review of U.S. Patent No. 8,359,501 ("the '501 patent"), which claims priority as a

continuation of the '434 patent: *Sandisk Corp. v. Netlist, Inc.*, Case IPR2014-00971 (PTAB December 16, 2014). Oral argument in IPR2014-00971 was consolidated with the oral argument in the present *inter partes* review. A final decision in IPR2014-00971 is issued concurrently with this final decision.

Patent Owner informs us that the '434 patent is the subject of an infringement action filed by Patent Owner: *Netlist, Inc. v. Smart Modular Technologies, Inc.*, No. 4:13-cv-05889-YGR (N.D. Cal. Dec. 19, 2013). Paper 9, 2. SMART Modular Technologies, Inc., a named defendant, filed two petitions for *inter partes* review of the '434 patent on August 23, 2014: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Cases IPR2014-01372 and IPR2014-01373 (PTAB). *Id.* at 3. On August 23, 2014, SMART Modular Technologies, Inc. also filed two petitions for *inter partes* review of the related '501 patent: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Cases IPR2014-01374 and IPR2014-01375 (PTAB). *Id.* On March 10, 2015, we instituted *inter partes* reviews in IPR2014-01372 and IPR2014-01374. IPR2014-01372, Paper 13; IPR2014-01374, Paper 12. Oral arguments for IPR2014-01372 and IPR2014-01374 were consolidated, and held on November 17, 2015.

B. The '434 Patent (Ex. 1001)

The '434 patent relates to self-testing electronic memory modules. Ex. 1001, 1:23–24. A block diagram of an exemplary self-testing memory module is shown in Figure 3 of the '434 patent, reproduced below. *See id.* at 9:23–25.

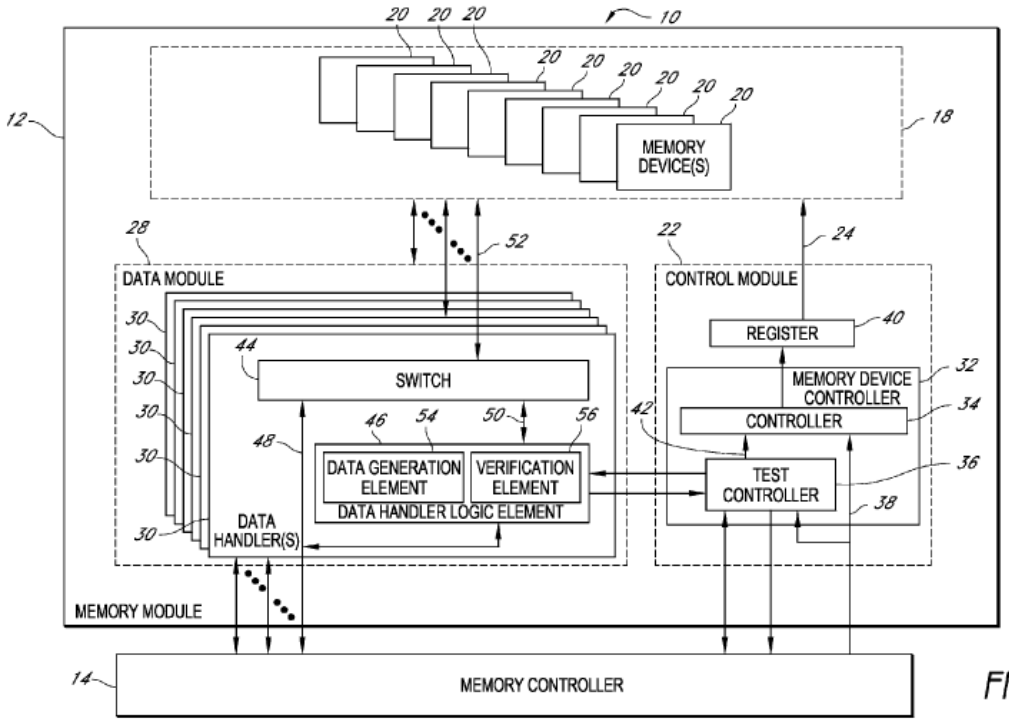


FIG. 3

As illustrated in Figure 3, above, "memory module 10 includes a printed circuit board 12 configured to be operatively coupled to a memory controller 14 of a computer system 16." *Id.* at 5:1–3. Memory module 10 includes a plurality of memory devices 18, each memory device 20 of the plurality of memory devices 18 comprising data, address, and control ports. *Id.* at 5:3–7. "[M]emory module 10 comprises a control module 22 [and] . . . a data module 28." *Id.* at 5:7–10.

"[C]ontrol module 22 can be configured to generate address and control signals 24 for testing the plurality of memory devices 18." *Id.* at 9:25–27. In the embodiment shown in Figure 3, control module 22 includes control mixer element 32 for controlling the address and control signals for the self-testing function. *Id.* at 9:31–33. Control mixer element 32 includes memory device controller 34 (e.g., a DRAM controller) and test controller 36. *Id.* at 9:29–31. "[T]est controller 36 controls the generation of the

address and control signal sequences to be used during the self-testing operation of the memory module 10 and also communicates with the data module 28." *Id.* at 9:53–56. "[M]emory device controller 34 receives signals 38 (e.g., address and control signals) from the system memory controller 14 and signals 42 (e.g., address and controls signals) from the test controller 36." *Id.* at 9:37–40.

Data module 28 comprises a plurality of data handlers 30 that "may be operatively coupled to (e.g., logically and/or electrically coupled to) the corresponding plurality of data ports" of memory devices 18. *Id.* at 5:10–11, 16–18. In the embodiment illustrated in Figure 3, each of data handlers 30 includes data handler logic element 46, comprising data generation element 54 and verification element 56. *Id.* at 10:27–30. "[D]ata generation element 54 may be configured to generate data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports" of memory devices 18. *Id.* at 10:31–33. "The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." *Id.* at 10:33–37.

C. Illustrative Claim

Of the challenged claims, claims 1, 20, and 29 are independent. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A self-testing memory module, comprising:
>
> a printed circuit board configured to be operatively coupled to a memory controller of a computer system;
>
> a plurality of memory devices on the printed circuit board, each memory device of the plurality of memory devices comprising data, address, and control ports; and

a circuit comprising:

a control module configured to generate address and control signals for testing the memory devices; and

a data module comprising a plurality of data handlers, each data handler operable independently from each of the other data handlers of the plurality of data handlers and operatively coupled to a corresponding plurality of the data ports of one or more of the memory devices and configured to generate data for writing to the corresponding plurality of data ports, wherein the circuit is configured to test the memory devices using the address and control signals generated by the control module and the data generated by the plurality of data handlers.

D. The Prior Art

The pending grounds of unpatentability in this *inter partes* review are based on the following prior art:

Reference	**Publication**	**Exhibit**	**Date**
Averbuj	U.S. Patent Application Publication No. 2005/0257109 A1	1003	Nov. 17, 2005
Huang	*An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers*, Fourteenth International Conference on VLSI Design 379–384 (2001), IEEE	1004	2001
JEDEC Standard	JEDEC Standard, Fully Buffered DIMM (FBDIMM): DFx Design for Validation and Test, JESD82–28	1006	Feb. 2008

E. The Instituted Grounds of Unpatentability

We instituted the instant *inter partes* review of claims 1, 2, 5–15, and 17–35 on the following grounds:

Claims	**Basis**	**Reference(s)**
1, 14, 15, 17–25, 27, and 29–35	§ 102(b)	Averbuj
28	§ 103(a)	Averbuj
1, 2, 5, 6, 14, 15, 19, and 29	§ 103(a)	Huang
7–12, 17, 18, 20–25, 27, 28, and 30–35	§ 103(a)	Huang and Averbuj
13 and 26	§ 103(a)	Huang, Averbuj, and JEDEC Standard

F. Expert Testimony

Petitioner relies on the testimony of Dr. Donald Alpert in support of its patentability challenges. Dr. Alpert executed a first declaration (Ex. 1007) in support of the Petition and a second declaration (Ex. 1009) in support of Petitioner's Reply. Dr. Alpert was cross-examined on the subject matter of his first and second declarations, and transcripts of the testimony were filed as Exhibits 2013 and 2021, respectively.

Dr. Alpert testified that he "received an Electrical Engineering Ph.D. degree in 1984 from Stanford University." Ex. 1007 ¶ 6. Dr. Alpert testified that he taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities (*id.*), and that he worked in the computer industry, i.e., designing microprocessors and components for Burroughs Corporation, Zilog, National Semiconductor, and Intel, at various

times between 1976 and 1997 (*id.* ¶ 7). Dr. Alpert testified that his "own training and experience exceeds that of ordinary skill in the art." *Id.* ¶ 21.

Patent Owner relies on the testimony of Dr. Carl Sechen. Dr. Sechen executed a declaration (Ex. 2012) in support of Patent Owner's Response. Dr. Sechen was cross-examined on the subject matter of his declaration, and a transcript of the testimony was filed as Exhibit 1010.

Dr. Sechen testified that he "was awarded a Ph.D. in electrical engineering from the University of California at Berkeley in 1986" (Ex. 2012 ¶ 6), and has been a Professor of Electrical Engineering for more than 28 years (*id.* ¶ 3). Dr. Sechen testified that during this time period, his research has focused on design and computer-aided design of digital integrated circuits, including the design of DRAM, and that he has taught numerous students how to design DRAM memories. *Id.* Dr. Sechen testified that he has "also been involved in numerous research projects on VLSI design and memory design[, and has] taught numerous graduate researchers how to design digital integrated circuits, including memories." *Id.* ¶ 5. Dr. Sechen testified, and Petitioner does not dispute, that he is "at least a person of ordinary skill" in the art of memory module design. *Id.* ¶¶ 34–35.

To testify as an expert under Federal Rule of Evidence (FRE) 702, a person need not be a person of ordinary skill in the art, but rather "qualified in the pertinent art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co., Inc.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge,

skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 Fed. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). There is no dispute that Dr. Alpert and Dr. Sechen are qualified to testify as experts under FRE 702.

II. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is relevant to claim construction and determinations of anticipation and obviousness. *See Graham v. John Deere Co*., 383 U.S. 1, 17–18 (1966) (explaining that obviousness is a question of law based on underlying factual findings including the level of ordinary skill in the pertinent art); *Yorkey v. Diab*, 605 F.3d 1297, 1300 (Fed. Cir. 2010) (explaining that a determination of anticipation involves, interpreting the claim language and then comparing the construed claim to a prior art reference); *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259–60 (Fed. Cir. 2010) ("[C]laim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.").

Petitioner's expert, Dr. Alpert, and Patent Owner's expert, Dr. Sechen, disagree as to the level of ordinary skill in the art. Dr. Alpert testified that "a person of ordinary skill in the art for the '434 patent would have a bachelor's degree or the equivalent training or experience in electrical engineering and at least one year of experience relating to memory systems and BIST." Ex. 1007 ¶ 20. Dr. Sechen testified that

one of ordinary skill in the art at the time of filing the

> application(s) for the '434 Patent, who would be working on the design of memory devices and memory modules, would have at least a Bachelor of Science degree in electrical engineering or computer engineering, and at least five years of industry experience designing memory devices and memory modules. Alternatively, one of ordinary skill in the art would have an M.S. degree in electrical engineering or computer engineering, and at least three years of industry experience designing memory devices and memory modules. Moreover, one of ordinary skill in the art would have a Ph.D. degree in electrical engineering or computer engineering, and have at least one year of industry experience designing memory devices and memory modules.

Ex. 2012 ¶ 33.

The difference in the opinions of the two experts is that Dr. Sechen believes a person of ordinary skill in the art would have an additional four years of experience, education, or a combination of the two, beyond that proposed by Dr. Alpert. *See* Ex. 1009 ¶ 7. According to Dr. Alpert, the difference in the proposed levels of ordinary skill in the art is not material to any dispute over claim construction or patentability in this *inter partes* review. *Id.*

We accord greater weight to Dr. Alpert's opinion as to the level of ordinary skill in the art because he has experience in both teaching students and working with engineers in the industry, while Dr. Sechen's experience is primarily in teaching. *Compare* Ex. 1007 ¶¶ 7, 21 *with* Ex. 2012 ¶¶ 3, 5. Moreover, based on our review of the '434 patent and the types of problems and solutions described in the '434 patent and cited prior art, we agree with Dr. Alpert's opinion on the level of ordinary skill. Accordingly, we find that a person of ordinary skill in the art at the time of the '434 patent would have a Bachelor's degree in electrical engineering, computer engineering, or in a

related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST.

III. CLAIM CONSTRUCTION

In its Petition, Petitioner requested that "each claim be construed in accordance with its plain and ordinary meaning under the required broadest reasonable interpretation" standard. Pet. 6–7. In its Preliminary Response, Patent Owner offered specific constructions for the claim terms: "memory module," "self-testing memory module," and "generate." Prelim. Resp. 22–27. For purposes of our Institution Decision, we interpreted the claim term "self-testing memory module" as a memory module that can be tested with internal and/or external test equipment. *See* Dec. on Inst. 7–8. We also interpreted the claim term "generate" as meaning "produce" or "cause." *See id.* at 8–10.

In its Response, Patent Owner disagrees with the Board's interpretations of "self-testing memory module" and "generate," (*see* PO Resp. 8, 17) and further asserts that express constructions of the claim language "operable independently" and "configured to generate" are "necessary in view of the arguments made by Petitioner" (*id.* at 7). Patent Owner proposes constructions for all four claim terms/phrases. *See generally id.* at 7–29. In its Reply, Petitioner argues Patent Owner's proposed constructions are overly narrow. Reply 1. Petitioner contends the claim terms/phrases in dispute are common words, whose plain and ordinary meanings are well-known (*id.*), such that no construction is necessary (*id.* at 3, 6, 7, 11). Petitioner also provides proposed constructions of the claim terms/phrases in dispute. *See generally* Reply 1–12.

Patent Owner's and Petitioner's proposed constructions for the disputed claim language are listed in the table below.

Claim Term/Phrase	**Patent Owner's Proposed Construction**	**Petitioner's Proposed Construction**
Self-testing memory module	a memory module configured to test itself (PO Resp. 9), i.e., a memory module that can be tested with only internal, or both internal and external test equipment (Tr. 39:23–24, 40:1–2)	memory modules that can be tested with internal and/or external test equipment (Reply 3)
Operable independently	each data handler is able to be used independently from the other data handlers (PO Resp. 11)	operation of a data handler is not influenced or controlled by another data handler (Reply 6–7)
Generate	produce (PO Resp. 29)	produce or cause production of (Reply 11 n.3)
Configured to generate	programmed to produce (PO Resp. 17–18)	designed to, adapted to, or arranged to produce or cause (Reply 7)

In an *inter partes* review, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definitions for claim terms must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir.

1994). "[E]xtrinsic evidence may be used only to assist in the proper understanding of the disputed limitation; it may not be used to vary, contradict, expand, or limit the claim language from how it is defined, even by implication, in the specification or file history." *Tempo Lighting, Inc. v. Tivoli*, LLC, 742 F.3d 973, 977–78 (Fed. Cir. 2014) (internal quotations and citations omitted). Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999). A court may revisit and alter its construction of claim terms as the record in a case develops. *See Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd*, 599 F.3d 1308, 1322 (Fed. Cir. 2010).

Applying the foregoing principles of law, we review our constructions of the claim terms "self-testing memory module" and "generate,"[1] and also determine that the claim terms "configured to" and "operable independently" require construction.

A. Self-testing Memory Module

The term "self-testing memory module" appears in the preamble of each of independent claims 1, 20, and 29, and also in the body of claim 29. For purposes of our Institution Decision, we interpreted this term as a memory module that can be tested with internal and/or external test equipment. *See* Dec. on Inst. 7–8. Petitioner agrees with this construction of "self-testing memory module." Reply 3.

Patent Owner contends our preliminary construction is overly broad, because it encompasses "memory modules that can be tested with only

[1] Our interpretation of the term "generate" also applies to other verb tenses used in the claims, i.e., "generating" and "generated."

external test equipment (*i.e.*, with no internal equipment)." PO. Resp. 8–9. During oral argument, Patent Owner clarified that it did not object to a construction of self-testing memory module as encompassing memory modules that can be tested with only internal, or both internal and external test equipment. Tr. 39:23–24.

Accordingly, we alter our prior construction, and interpret "self-testing memory module" as encompassing, at a minimum, memory modules that can be tested with only internal, or both internal and external test equipment. We decline to determine whether or not the broadest reasonable construction of "self-testing memory module" also encompasses modules that can be tested with only external test equipment, as such determination is unnecessary to our decision.

B. Operable Independently

Independent claims 1 and 29 recite: "a data module comprising a plurality of data handlers, each data handler operable independently from each of the other data handlers of the plurality of data handlers." Ex. 1001, 16:42–45, 19:1–4. Claim 27 depends from independent claim 20 and recites "[a data module comprising] at least two data handlers and each of the data handlers is operable independently from each of the other data handlers." *Id.* at 18:10, 49–51.

Patent Owner contends that "within the context of the claims, 'operable' is properly construed as 'able to be used,'" and that the above-quoted language from claims 1, 27, and 29 means that each data handler is "able to be used to independently test a portion of one or more memory devices." PO Resp. 9–10; *see also id.* at 12 ("The word 'able' [in 'operable'] leaves open the possibility that [a data handler] might NOT be

used for testing while other testing (via other data handlers) may be proceeding for a given testing period."); Tr. 43:1–6 ("'Operating independently' necessarily means that the use or operation of a data handler is not dependent on the use or operation of another data handler for testing. For example, to be 'independently operable' means that one data handler can be used – i.e., operated – in one mode while another data handler is operated or used in another mode."). Petitioner contends "'*operable independently*' merely means that each data handler can operate without influence or control by any of the other data handlers." Reply 5 (citing Ex. 1009 ¶ 22 ("This would encompass data handlers that receive common control signals from one controller, as long as the data handlers are not in communication with each other.")).

In their papers, both Patent Owner (PO Resp. 9–10) and Petitioner (Reply 5) rely on column 8, lines 1–11 of the '434 patent in support of their proposed constructions:[2]

> Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28. *For example, each data handler 30 is configured to write to and/or read from the corresponding plurality of data ports of one or more of the memory devices 20 without being in communication [with] any of the other data handlers 30 or other data ports of the memory devices 20.* As such, each data handler 30 can be used to generally independently test a portion of the memory space of the memory module 10. For example, each data handler 30 may be used to independently test one memory device 20 of the memory module 10.

Ex. 1001, 8:1–11 (emphasis added). Petitioner quotes lines 1–11 in their

[2] Both parties also rely on the testimony of their experts and dictionary definitions. *See generally* PO Resp. 9–12; Reply 3–7.

entirety. Reply 5. Patent Owner omits the italicized language from its quotation (PO Resp. 9–10), contending, at oral argument, that this language is immaterial to construction of the claim term "operable independently," because it "relates to reading and writing to the data ports[, not] . . . to data generation, which is the claimed operation of the data handler." Tr. 43:16–18.

"We apply a 'presumption that the same terms appearing in different portions of the claims should be given the same meaning unless it is clear from the specification and prosecution history that the terms have different meanings at different portions of the claims.'" *PODS, Inc. v. Porta Stor, Inc.*, 484 F.3d 1359, 1366 (Fed. Cir. 2007) (quoting *Fin Control Sys. Pty., Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001)). Independent apparatus claim 1 recites "a data module comprising *a plurality of data handlers*, each data handler" (1) "*operatively coupled* to a corresponding plurality of the data ports of one or more of the memory devices," (2) "*configured to generate* data for writing to the corresponding plurality of data ports," and (3) "*operable independently* from each of the other data handlers of the plurality of data handlers," Ex. 1001, 16:42–48 (emphasis added). Claim 1 further recites "wherein the circuit is configured to test the memory devices using the address and control signals generated by the control module and the data generated by the *plurality* of data handlers." *Id.* at 16:49–52. Similarly, independent method claim 29 recites "a data module comprising *a plurality of data handlers*" (*id.* at 19:1 (emphasis added)), requires that each data handler is *operable independently* and *operatively coupled* in the same manner recited in claim 1 (*compare id.* at 19:2–5 *with id.* at 16:43–46 (emphasis added)), and recites a step of "*generating*, by each

of the data handlers, *data* for writing to the corresponding plurality of data ports; and using . . . the generated data to test the memory devices" (*id.* at 19:8–11 (emphasis added)).

Independent apparatus claim 20 differs from claims 1 and 29 in that it requires that the data module comprise "*at least one* data handler" (*id.* at 18:10), rather than a *plurality* of data handlers. Similar to claims 1 and 29, claim 20 requires that the at least one data handler is (1) "*operatively coupled* to a corresponding plurality of the data ports of one or more of the memory devices," and (2) "*configured to generate* cyclic data for writing to the corresponding plurality of data ports." Claim 20 also requires a circuit "configured to test the memo[ry] devices using the address and control signals generated by the control module and the cyclic data generated by the at least one data handler." *Id.* at 18:15–18.

Claim 27 depends from claim 20 and recites: "wherein there are at least two data handlers and *each of the data handlers is operable independently* from each of the other data handlers." *Id.* at 18:48–51 (emphasis added). Claim 27 does not recite that the second data handler is part of the data module recited in claim 20. Therefore, unlike the first data handler of claim 20 and each of the plurality of data handlers of claims 1 and 29, the second data handler of claim 27 is not required to be *operatively coupled* to a corresponding plurality of the data ports of one or more of the memory devices (claims 1, 20, and 29) and *configured to generate* (claims 1 and 20) or *generating* (claim 29) data for writing to the corresponding plurality of data ports. In other words, the term "operable independently," as used in claim 27, is separate and distinct from data generation and testing.

We presume the term "operable independently" has the same meaning

in claims 1 and 29 that it has in claim 27, i.e., that "operable independently" as used in claims 1 and 29 is separate and distinct from data generation and testing, unless its usage in the context of the '434 patent specification indicates otherwise. *See Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1396–97 (Fed. Cir. 2008) (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) ("[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.")).

In addition to the '434 patent disclosure relied upon by the parties in support of their respective constructions of "operable independently" (*see* Ex. 1001, 8:1–11), the '434 patent includes the following description of the data handlers in connection with Figure 1:

> *Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28 and* is operatively coupled to a corresponding plurality of the data ports of one or more of the plurality of memory devices 18. For example, each of the data handlers 30 may be operatively coupled to (e.g., logically and/or electrically coupled to) the corresponding plurality of data ports. Each data handler 30 *is further configured to generate data for writing to the corresponding plurality of data ports*.

Id. at 5:11–20.

In the above quotation, each data handler is described as "operable independently," and having the "further" feature of being "configured to generate data." Use of the term "further" supports Petitioner's contention that the data generation function of the data handlers is an additional feature that is separate from the feature of independent operability. *Cf.* Tr. 86:24–87:2.

The ’434 patent discloses that a prior art problem associated with the implementation of memory module self-test logic is lack of flexibility, e.g., to changes in the data width of the memory module. *See* Ex. 1001, 4:36–55. The ’434 patent indicates that accommodating changes in data width, etc., may be less complicated in the inventive self-testing memory module. *See id.* at 8:22–26. The ’434 patent explains that:

> [b]ecause each of the data handlers 30 is operable independently of each of the other data handlers 30, the data handlers 30 are generally modular. . . . For example, where a new memory device 20 or set of memory devices 20 is added to the memory module 10, the change may be generally accommodated by adding a corresponding data handler 30. The change may be accommodated without having to implement a major reorganization of the memory module 10 or the self-testing logic of the memory module 10, for example.

Id. at 8:19–32.

The above disclosure uses the term “operable independently” to describe the data handlers as being discrete and functioning without being physically or logically connected to each other.

Based on our review of the ’434 patent, the specification and claim 27 both use the term “operable independently” in the same manner, i.e., to describe a feature of the data handler that is distinct from its data generation feature. We agree with Petitioner, therefore, that when interpreted in the context of the ’434 patent in its entirety, the claim term “operable independently” “merely means that each data handler can operate without influence or control by any of the other data handlers.” Reply 5. The ’434 patent specification uses the term “operable independently” in accordance with its plain and ordinary meaning, and we find no basis for applying the narrower construction advanced by Patent Owner to any of the challenged

claims.

Accordingly, we interpret "operable independently" as "operable without influence or control by another." *See Cuozzo*, 793 F.3d at 1278–79.

C. Configured to, and Generate

Each of independent claims 1, 20, and 29 recites "a control module *configured to generate* address and control signals for testing the memory devices" Ex. 1001, 16:40–41, 18:8–9, 18:66–67 (emphasis added). Claims 1 and 20 also recite that each data handler is "configured to generate" data for writing to data ports of one or more memory devices. *Id.* at 16:43–48, 18:10–13. Method claim 29 includes a step of "*generating*, by each of the data handlers, data for writing to . . . data ports" of the memory devices. *Id.* at 18:62–64, 19:8–9 (emphasis added).

1. Configured to

Prior to institution, neither party requested, nor did we deem necessary, construction of the term "configured to." In its Response, Patent Owner now requests that we construe the term "configured to" in the context of the claim phrase "configured to generate" (*see* claims 1, 20, and 29). *See* PO Resp. 12. As correctly observed by Petitioner, however, the term "configured to" is not used exclusively in conjunction with the term "generate" in the claims, but is also used with the claim terms "test," "write," "read," "calculate," "store," "verify," "be operatively coupled," and "selectively input." *See* Reply 7. The term "configured to" is also used in the '434 patent specification in conjunction with the terms "provide" (Ex. 1001, 6:4, 30–31), "operatively couple" (*id.* at 7:22), "read" (*id.* at 11:5–6), "receive" (*id.* at 11:7–8), "check" (*id.* at 11:10), "perform" (*id.* at 11:16–17), "report" (*id.* at 12:22), and "input" (*id.* at 14:2, 5). Presumptively,

"configured to" should carry the same meaning, and "configured to generate," "configured to test," "configured to write," etc. should have parallel meanings, differing only insofar as "test," "write," "generate," etc., differ. *See Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1337 (Fed. Cir. 2008) ("'[B]inary code' and 'trinary code' should have parallel meanings, differing only insofar as 'binary' and 'trinary' differ in their relationships to the numbers 2 and 3.").

Patent Owner does not offer an interpretation of the term "configured to" outside the context of the phrase "configured to generate" (*see* PO Resp. 12–17), but contends "'configured to generate' means 'programmed to generate' and to enable the subsequent execution of a self-testing function (*e.g.*, data generation, writing and verification)" (*id.* at 15; *see also id.* at 13 ("'Programmed' is therefore synonymous with 'configured.'")).

Petitioner contends the claim term "configured to" should be construed consistently, whether used in conjunction with "generate" or with another function recited in the claims, and should be given its plain and ordinary meaning of "designed to, adapted to, or arranged to [perform the recited function]." Reply 7–8. In addition to relying on the testimony of its expert, Dr. Alpert, Petitioner cites two dictionary definitions in support of its proposed interpretation. Reply 7–8 (citing Ex. 1011, 186; Ex. 1012, 428).

Dr. Alpert, testified that, in the '434 patent, "'program' is one example of 'configure,' but not the only example." Ex. 1009 ¶ 23. Dr. Alpert further testified "the '434 patent discloses that *configuring* can be accomplished in a wide variety of ways . . . , including those that do not require programming, for example using predefined values." *See id.* ¶ 26 (quoting Ex. 1001, 6:14–17 ("The address sequences and/or the data patterns

of certain embodiments may be programmable either through the I^2C interface or they may be defaulted to pre-defined values."); *id.* at 10:63–67 ("[R]andom or pseudorandom data may be generated and written to the corresponding plurality of data ports. For example, a linear feedback shift register (LFSR) may be used in some embodiments. In addition, the data patterns may be programmable."); *see also* Ex. 2021, 135:12–136:2 (wherein Dr. Alpert testified that a linear feedback shift register would not need to be programmed to generate data, but could be arranged or designed to generate data). In his second declaration, Dr. Alpert also testified that:

> The '434 patent uses "configured" to describe hardwired arrangements of components that cannot be programmed for their configuration. Additionally, the '434 patent discloses various components included in the control module, which do not all require programming: . . . . The configuration of the circuit board's coupling to the memory controller can be fixed, as shown by system bus 50 and I^2C bus 15 in Figs. 1-3. . . . [Referring to the] configured to verify . . . limitation . . . . [in] claim 8[,] [t]he configuration of the verification circuitry can be fixed without any memory structure for storing a copy of the generated data, as disclosed at 11:16-30. . . . [And,] control module 22 [can] include[] discrete logic [or] one or more application-specific integrated circuit (ASICs) . . . [b]oth . . . could be programmable or nonprogrammable as would have been understood by a person of ordinary skill.

Ex. 1009 ¶ 27 (emphasis omitted); *see also* Ex. 2021, 132:5–9 (explaining, with respect to the claim 8 limitation "wherein the verification element is configured to verify that the data read . . . corresponds to the data generated . . . without storing a copy of the data generated by the data handler" (Ex. 1001, 17:11–16): "[I]f in fact there's no copy stored, then this configuration would be hard wired. There would be no sense in which it would be programmed to meet this limitation.").

Patent Owner's expert, Dr. Sechen, testified that "the most conventional use of *configuration* refers to hardware programming" (Ex. 1010, 68:25–69:2 (emphasis added)), but that it could refer to software programming as well. *Id.* at 55:17–18. In his declaration, Dr. Sechen did not testify as to the meaning of "configured to" in conjunction with any term other than "generate." *See* Ex. 2012 ¶¶ 63–80. In response to questioning during cross-examination, however, Dr. Sechen testified that "configured to," as used in the context of the phrase "a printed circuit board configured to be operatively coupled to a memory controller of a computer system" (Ex. 1001, claims 1, 20, and 29), "might mean designed [to]" because the printed circuit board has to be configured "such that it fits into the slot on the motherboard and is able to communicate successfully with the memory controller." Ex. 1010, 84:14–19. The '434 patent discloses that components of control module 22 and data module 28 may include discrete logic and application specific integrated circuits (ASICs) (*see* Ex. 1001, 9:58–60, 12:30–34), which, on cross-examination, Dr. Sechen conceded can be designed to operate without the need for hardware programming.. Ex. 1010, 58:9–61:22.

Based on our analysis of the '434 patent claims and specification, and relying on the testimony of Drs. Alpert and Sechen regarding the technology,[3] we find the '434 patent uses the term "configured to" to

[3] "Although the patent file may often be sufficient to permit the judge to interpret the technical aspects of the patent properly, consultation of extrinsic evidence is particularly appropriate to ensure that his or her understanding of the technical aspects of the patent is not entirely at variance with the understanding of one skilled in the art." *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1309 (Fed. Cir. 1999).

describe components that can be programmed by a controller to perform a function, as well as components that can be hard-wired to perform a function and do not require programming. *See, e.g.*, Ex. 1001, 7:21–27 ("PCB 12 may include at least one connector (not shown) configured to operatively couple the memory module 10 to the memory controller 14 of the computer system 16. . . . For example, the memory module is electrically coupled, logically coupled, or both, with the memory controller 14"); *id.* at 8:47–50 ("[T]he data handlers 30 may be operatively coupled (e.g., electrically and/or logically coupled or connected) to the eight data ports 21 of one of the corresponding memory devices 20"). We do not agree with Patent Owner, therefore, that the broadest reasonable interpretation of "configured to" is "programmable to." *Cf.* Ex. 1010, 84:14–19 (wherein Dr. Sechen testified that "configured to" in the context of the phrase "configured to be operatively coupled" (claims 1, 20, and 29) "might mean designed [to]"); *id.* at 89:3–5 ("'Designed' implies a certain hardwiredness, that that's what it does, and 'configured' implies that maybe it only does that some of the time."). Rather, we agree with Petitioner that one of ordinary skill in the art would interpret the claim term "configured to" in accordance with its plain and ordinary meaning, and would understand that this term encompasses components both programmable and hard-wired to perform the functions described in the '434 patent. Accordingly, we interpret the term "configured to" as "designed, adapted, or arranged to."

2. Generate

In addition to reciting "a control module configured to generate address and control signals for testing" and a data handler "configured to generate data for writing" (claim 1; *see* claim 20), claims 1 and 20 require a

"circuit [] configured to test the memory devices using the address and control *signals generated by* the control module and the *data generated by* the plurality of data handlers" (claim 1 (emphasis added); *see* claim 20). Similarly, claim 29, in addition to reciting steps of "generating, by the control module, address and control signals for testing the memory devices" and "generating, by each of the data handlers, data for writing to the corresponding plurality of data ports," requires *using* these *generated signals and data* to test the memory devices (claim 29).

For purposes of our Institution Decision, we interpreted the claim term "generate" as meaning "produce" or "cause." *See* Dec. on Inst. 8–10. Our interpretation was based on findings that the plain and ordinary meaning of "generate," as evidenced by Merriam-Webster's Collegiate Dictionary, is "produce" or "be the cause of" (*id.* at 9–10 (citing Ex. 2002, 484)), and that interpreting "generate" to mean "cause" was not inconsistent with the '434 patent specification, which broadly states that data can be generated by the data handlers in a variety of ways (*see id.* at 9 (citing Ex. 1001, 10:49–59)).

Petitioner contends the Board should maintain its construction of "generate" as "produce" or "cause," because this construction "reflects the plain and ordinary meaning." Reply 11–12. Petitioner maintains one of ordinary skill in the art "would appreciate that when substituted in the claims, the Board's construction is 'produce or cause production of [data/address and control signals].'" *Id.* at 11 n.3 (citing Ex. 1009 ¶ 36). During cross-examination, Dr. Alpert explained the difference between producing and causing to produce" as follows: "[P]roducing would actually be either creating or providing, in this case, some data and causing to produce would be having one device be the cause of or invoking another

device to produce the data." Ex. 2013, 43:5–11. Dr. Alpert testified that one of ordinary skill in the art would understand the description of the data handler being logically coupled to the memory devices at column 5, lines 15–18 of the '434 patent as implying intermediary logical devices between the data handler and the memory device ports. *See id.* at 39:1–16. In other words, one of ordinary skill in the art would understand that the "physical system element" that produces the data used for testing in claim 1 "can be the data handler or it can be another device that the data handler causes to produce the data." *Id.* at 32:4–6. During cross examination, Dr. Alpert identified "a buffer or a multiplex[e]r" as examples of devices that could "exist between the data handler and the memory device" to produce the data used for testing. *Id.* at 36:13–16. Dr. Alpert explained that a

> buffer can take an input, information input and it can either produce a signal that contains that information or the complements of that information, or there could be several buffers that have potential to be in a third state, so-called tri-state buffers, such that the buffers can be used to select information that may be presented, that would be data that would be produced that would then be presented down to other circuits.

Id. at 36:24–37:8.

Patent Owner contends "'generate' is properly construed [only] as 'produce.'" PO Resp. 29 (citing Ex. 2012 ¶¶ 84–108); *see also id.* at 19 (citing Ex. 2012 ¶ 86 ("In the context of integrated circuit and printed circuit board design, *generate* or *produce* (which are synonyms in this context) are terms of art.")). Patent Owner argues that interpreting "generate" as "cause," or as "cause to produce," as suggested by Petitioner, would render other claim language superfluous. *See id.* at 22–29. Specifically, Patent

Owner contends that interpreting "generate" as "cause to produce" renders meaningless the structural limitation of a "circuit [] configured to test the memory devices using the address and control signals generated by the control module and the data generated by the plurality of data handlers" (claim 1; *see* claim 20) and the method step of "using the address and control signals and the generated data to test the memory devices" (claim 29), because the circuit can only use, or be configured to use, data and signals that are actually produced. *See id.* at 26–29; *see also id.* at 23 ("[T]he situation posited by the Board does not reflect that the data written by the data handler was 'generated by the data handler' . . . [and] improperly eliminates the requirement that 'the circuit is configured to test the memory devices using [] the data generated by the plurality of data handlers." (quoting (Ex. 1001, claim 1))).

"Proper claim construction . . . demands interpretation of the entire claim in context, not a single element in isolation." *Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999); *see also ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("While certain terms may be at the center of the claim construction debate, the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms."). "[W]here there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meaning." *Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 2003).

The '434 patent claims and specification uses the term "generate" in conjunction with the memory module, control module, data module, and

components thereof. The '434 patent uses the term "generate" as a specific example of "produce," the term "produce" appearing only once in the '434 patent:

> In some embodiments, the control module 22 and the data module 28 *produce* memory addresses, control and/or data signals according to the JEDEC standard memory protocol. In some embodiments, *for example*, the control module 22 and the data module 28 *generate* the memory interface signals with proper edge relationships based on the JEDEC standard.

Ex. 1001, 6:6–12 (emphasis added).

The '434 patent specification uses both the term "provide" and the term "generate" in describing the operation of data module 28:

> [D]uring testing, the control module 22 generates address and control signals 24 associated with memory locations to be tested and the *data module 28 generates corresponding test data patterns and provides them* to the appropriate memory devices 20. For example, the data module 28 may receive a write command from the control module 22 and provide data to be written to certain locations in the memory devices 20 during a write operation.

Id. at 5:43–50 (emphasis added). The term "provide" is also used separately from, but in a similar manner to, the term "generate" to describe embodiments of control module 22 and data module 28 used for testing memory devices 18. *Compare id.* at 5:67–6:6 ("The data module 28 and/or the control module 22 of certain embodiments are configured to test the plurality of memory devices 18 at the normal operating speed of the memory devices 20. For example, the data module 28 and/or the control module 22 are *configured to provide* memory signals (e.g., data, address and control signals) according the operating specification of the memory devices 20" (emphasis added)) *with id.* at 9:25–27 ("The control module 22 can be

configured to generate address and control signals 24 for testing the plurality of memory devices 18." (emphasis added)) *and id.* at 10:27–33 ("Each of the data handlers 30 of certain embodiments further includes a data handler logic element 46. The data handler logic element 46 of certain embodiments comprises a data generation element 54 and a verification element 56. The data generation element 54 may be *configured to generate* data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports." (emphasis added)).

In addition to using the term "provide" to describe embodiments of control module 22 and data module 28, the '434 patent specification uses this term to describe the operation of switch 44: "The switch 44 may provide a bi-directional data multiplexer function" and is "configured to selectively input" data signals 48 from system memory controller 14 or data signals 50 from data handler logic element 46. *Id.* at 10:6–11. The '434 patent specification discloses that switch 44 may positioned between data module 28 and memory devices 18 (*see id.* at 10:23–26), i.e., one of the hypothetical arrangements described by Dr. Alpert in which a data handler would cause an intermediary device (e.g., a multiplexer) to produce data. The '434 patent specification does not use the term generate (or produce), however, to describe the configuration or operation of switch 44.

The above-noted usages of the terms "provide" and "generate" to describe different embodiments of control module 22 and data module 28, and to describe different functions of the data handlers, do not support Dr. Alpert's opinion that the term "generate" is properly interpreted as

encompassing the selection function of a multiplexer.[4] Use of the term "generate" to describe an embodiment in which the control module and data module "produce" memory addresses, control and/or data signals, however, does support Dr. Sechen's opinion that "generate" and "produce" are synonymous.

The '434 patent specification also describes an embodiment in which switch 44 is included in each of data handlers 30 (*id.* at 10:3–4), as well as an embodiment in which the function of selective inputting of data signals to memory devices 18 is not limited explicitly to a switch (*see, e.g.*, *id.* at 5:63–66 ("[E]ach of the data handlers 30 write[s] the data generated by the data handler 30 to the corresponding plurality of data ports by selectively inputting data signals to the data ports of the plurality of memory devices 18.")). These embodiments are recited in claims 14 and 15. *See id.* at 17:39–43 ("each of the plurality of data handlers [is] *further configured to write* data to the memory devices *by selectively inputting* to the corresponding plurality of data ports either data signals from the system memory controller or data signals from the data handler." (emphasis

[4] Dr. Alpert's testimony, though consistent with Averbuj's use of the term "generate" (*see* Ex. 1003 ¶ 56 ("[D]ata generation unit 44 generates the transformed data signal 49 (BIST _DATA_ T) to fill the memory module 12 with the data dictated from the sequencer 8 without modification.")), cannot be relied on to construe this claim term in a manner that varies from the implicit definition in the '434 patent. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584–85 (Fed. Cir. 1996) ([P]rior art can often help to demonstrate how a disputed term is used by those skilled in the art. . . . [H]owever, reliance on such evidence is unnecessary, and indeed improper, when the disputed terms can be understood from a careful reading of the public record. Nor may it be used to vary claim terms from how they are defined, even implicitly, in the specification or file history." (internal citation omitted)).

added)); *id.* at 17:44–47 ("The self-testing memory module of claim 14, wherein each of the plurality of data handlers comprises *a switch which performs the selective inputting* to the corresponding plurality of data ports." (emphasis added)).

In the absence of evidence to the contrary, there is a presumption that different claim terms have different meanings. *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000); *see also SEB S.A. v. Montgomery Ward & Co., Inc.*, 594 F.3d 1360, 1369 (Fed. Cir. 2010) (noting there is a presumption that meanings of claim terms do not overlap); *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

The claim 1 recitation of "each data handler . . . configured to generate data for writing" and dependent claim 14 recitation of "each of the plurality of data handlers *further* configured to write data," as well as the above disclosure in the '434 patent specification, create a presumption that "generate" has a different meaning than "write" and/or "selectively input." *See also* claim 1 ("a control module configured to generate address and control signals") and dependent claim 17 ("the control module *further* configured to selectively input . . . either the address and control signals from the memory controller or the address and control signals from the control module" (emphasis added)). In other words, the '434 patent specification and claims do not support an interpretation of generating data as encompassing the function of selecting between data received from two or more different components, and/or writing or inputting the same data received from one component to another component, because such

interpretation would result in an overlap in the meaning of "generate" and "write" and/or "selectively input."

Having considered the ordinary meaning of the term "generate" in the context of both the claims and the '434 patent as a whole, we agree with Patent Owner that the broadest reasonable interpretation of the claim term "generate" is "produce," and that "generate" does not mean "cause" or "cause to produce." We interpret the claim language "address and control signals *generated* by the control module and the data *generated* by the plurality of data handlers" (claim 1), and the corresponding limitations in claims 20 and 29, as encompassing signals and data that originated in these modules, including by transformation or modification of information and/or data received from another component. *See e.g.* Ex. 1001, 10:33–37 ("The data signals and/or patterns of data signals may be *based on* information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." (emphasis added)); *id.* at 10:57–59 ("The data may be generated *based [on]* previously written data (e.g., inverting each of the bits of a previously written data word)" (emphasis added)). We do not interpret this language as encompassing signals and data received by the data and control modules from another component, and merely provided, propagated, sent, or input to memory devices, without transformation or modification by the data and control modules. *Compare, e.g.*, Ex. 1001, 9:51–53 ("In one embodiment, the memory device controller 34 *generates* the address and control signals for memory device (e.g., DRAM device) operations." (emphasis added)) *with id.* at 9:36–49 ("In one embodiment, the memory device controller 34 *receives* signals 38 (e.g., address and control signals) from the system memory controller 14 and

signals 42 (e.g., address and controls signals) . . . . [M]emory device controller 34 *may send* either the signals 38 from the system memory controller 14 or, alternatively, the signals 42 from the test controller 36, to the register 40." (emphasis added)).

Thus, in summary, we construe "operated independently/operating independently," "generate," and "configured to" as follows:

Claim Term/Phrase	**Interpretation**
Self-testing memory module	memory modules that can be tested, at a minimum with only internal, or both internal and external test equipment
Operable independently	operable without influence or control by another
Generate	produce
Configured to	designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]

IV. ANALYSIS

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged or combined in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

> A single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. Thus, a prior art reference without express reference to a claim limitation may nonetheless anticipate by inherency. "Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claims limitations, it anticipates."

Perricone v. Medicis Pharm. Corp., 432 F.3d 1368, 1375–76 (Fed. Cir. 2005) (citations omitted). "In general, a limitation or the entire invention is inherent and in the public domain if it is the 'natural result flowing from' the explicit disclosure of the prior art." *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003).

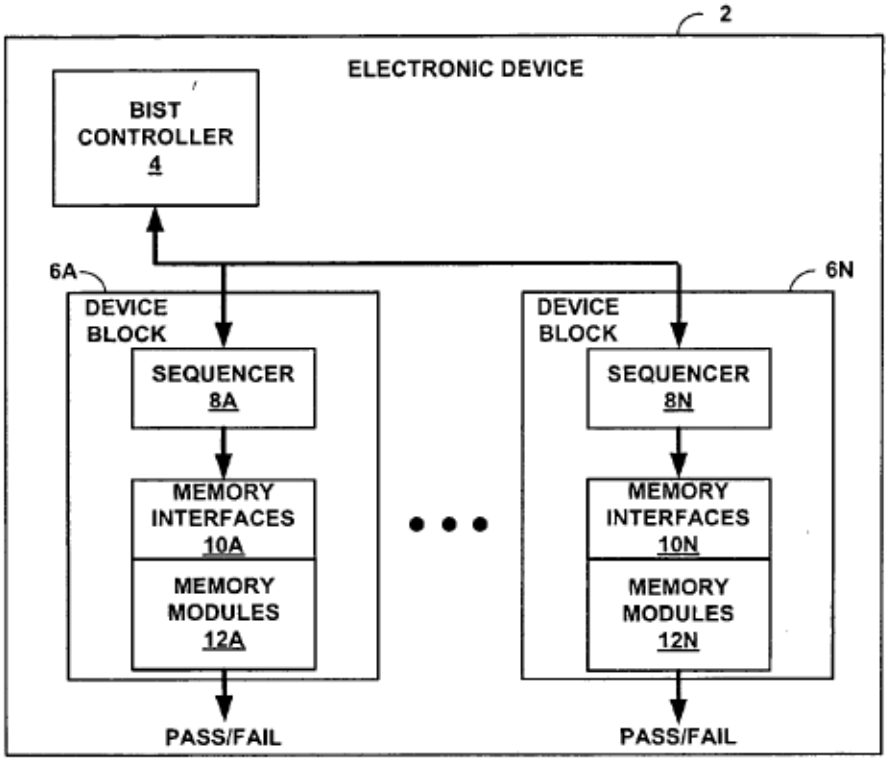
A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham*, 383 U.S. at 17–18. An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

A. Alleged unpatentability of claims 1, 14, 15, 17–25, 27, and 29–35 under §102(b) and alleged unpatentability of claim 28 under §103(a) based on Averbuj

1. Averbuj (Ex. 1003)

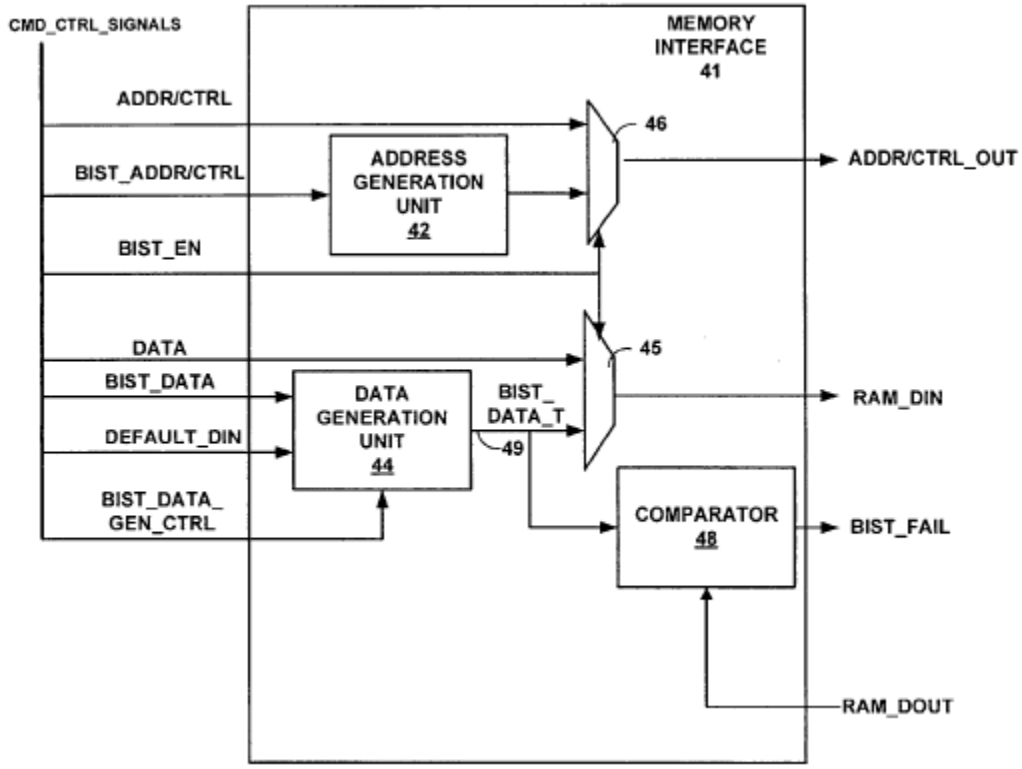
Averbuj describes a hierarchical built-in self-test (BIST) architecture wherein a BIST controller provides centralized, high level control of the testing of one or more memory modules. Ex. 1003 ¶¶ 7–8. Figure 1 of Averbuj is reproduced below.



Averbuj Figure 1, above, "is a block diagram illustrating an example electronic device 2 . . . includ[ing] a built-in self-test (BIST) controller 4 that provides centralized, high-level control over testing of device blocks 6A through 6N (collectively 'device blocks 6')." *Id.* ¶ 28. "Each of device blocks 6 includes a sequencer 8, and a set of one or more memory interfaces 10 and one or more respective memory modules 12." *Id.* BIST controller 4 provides and communicates test algorithms as a set of commands to

sequencers 8 for application to device blocks 6. *Id.* ¶ 29. Sequencers 8, in turn, issue command control signals (CMD_CTRL_SIGNALS) to receiving memory interfaces 10. *Id.* ¶ 43.

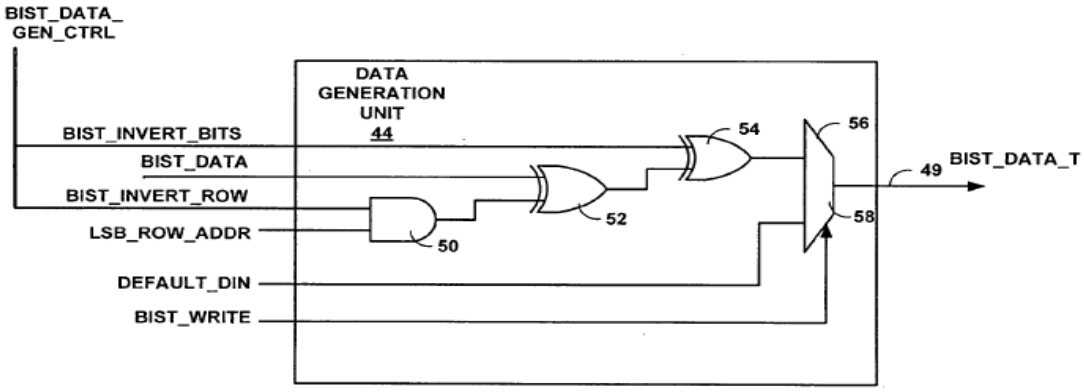
Exemplary memory interface 41 is shown in Figure 6, below. *Id.* ¶ 23.



As shown in the Figure 6 embodiment, above, memory interface 41 includes a layer of multiplexers 45, 46. *Id.* ¶ 48. "[U]nder normal operating conditions, BIST enable (BIST_EN) is de-asserted, causing multiplexers 45, 46 to select the address/control signals (ADDR/CTRL) and data signals (DATA), e.g., as provided by a programmable processor." *Id.* "When electronic device 2 is operating in BIST mode, however, the BIST enable signal causes multiplexers 45, 46 to select the BIST address/control signals (BIST_ADDR/CTRL) and the test data provided by a respective higher-level sequencer [, e.g., sequencer 8A]." *Id.*

"[M]emory interface 41 processes the sequential memory operations issued by [] higher-level sequencer [8A], and transforms the data and addresses provided by the sequencer as needed based on the particular physical characteristics of the memory module" (*id.* ¶ 54) using address generation unit 42 and data generation unit 44 (*id.* ¶¶ 49, 51). "For example, sequencer 8 may request a checkerboard bit pattern that requires columns of data within the memory module to alternate between ones and zeros. Different memory modules 12, however, may be arranged with different row and column configurations." *Id.* ¶ 50. In this case, address generation unit 42 transforms the address provided by sequencer 8 to correspond to the physical configuration of the specified memory module before the address is applied to that memory module. *See id.* ¶¶ 51–52.

An example embodiment of data generation unit 44 is illustrated in Figure 7, reproduced below.



As shown in Figure 7, above, "data generation unit 44 receives a BIST_DATA signal, a default data signal (DEFAULT_DIN) provided by the sequencer 8[, and] . . . a number of control signals in the form of BIST_INVERT_BITS, BIST_INVERT_ROWS, LSB_ROW_ADDR, and BIST_WRITE." *Id.* ¶ 55.

> [S]equencer 8 asserts and deasserts the invert bits signal (BIST_INVERT_ BITS), the invert rows signal (BIST_INVERT_ROWS), and the invert columns signal (not shown) to specify data patterns, such as solid, checkerboard, horizontal and vertical striped data patterns. If neither the invert bits nor the invert rows signals are asserted, then the BIST_DATA signal passes through XOR gates 52, 54 without modification. As a result, data generation unit 44 generates the transformed data signal 49, (BIST _DATA_ T) to fill the memory module 12 with the data dictated from the sequencer 8 without modification.

Id. ¶ 56. By contrast, when the BIST_INVERT_BITS signal is asserted, data generation unit 44 automatically inverts the values dictated by the sequencer. *Id.* ¶ 57.

2. Analysis

Petitioner contends each of Averbuj's device blocks 6 is "a 'self-testing memory module,' as recited in the preambles of claims 1 and 20, that perform 'a method of self-testing a memory module,' as recited in the preamble of claim 29." Pet. 8. Petitioner contends Averbuj's sequencer 8, memory interfaces 10, 41, and memory modules 12 correspond, respectively, to the claimed "control module," "data handlers," and memory devices. *See id.* at 16–18. Patent Owner argues: (1) Averbuj's memory interfaces (the alleged data handlers) are not configured to generate data, as recited in claims 1 and 20; (2) Averbuj's sequencer 8 (the alleged control module) does not generate the address and control signals used for testing the memory modules 12 (the alleged memory devices) as recited in claims 1, 20, and 29; (3) Averbuj's memory interfaces 10, 41 (the alleged data handlers) are not operable independently, as recited in claims 1, 20, and 29; and (4) Averbuj's sequencer (the alleged control module) is not configured

to selectively input address and control signals to the memory devices, as recited in claims 17, 19, and 35. *See* PO Resp. 30–37. Patent Owner does not dispute directly Petitioner's contentions with respect to the additional limitations recited in dependent claims 14, 15, 21–25, 28, and 30–34. *See id.* at 37–38. Patent Owner contends, however, that dependent claims 14, 15, 17–19, 21–25, 27, and 30–35 are not anticipated by Averbuj, and claim 28 is not obvious in view of Averbuj, because Petitioner has failed to show Averbuj discloses the limitations in independent claims 1, 20, and 29. *Id.*

a. "control module configured to generate address and control signals for testing the memory devices" (claims 1, 20, and 29)

Patent Owner argues Averbuj does not disclose a circuit configured to test the memory devices using the address and control signals generated by the control module as required by claims 1 and 20, or a method of testing using the address and control signals generated by the control module as recited in claim 29. PO Resp. 33–34. Patent Owner argues, more specifically, that in Averbuj, the address and control signals used to test the memory devices are produced by memory interfaces 10 (the alleged data handlers), not by sequencer 8 (the alleged control module). *See id.* at 33.

Petitioner references Averbuj paragraphs 37, 43, 48–53, 59–61, and 77–78 in support of its contention that Averbuj discloses a control module (sequencer 8) configured to generate address and control signals (CMD_CTRL_SIGNALS) used for testing memory devices (memory modules 12). Pet. 10, 16, 18. Petitioner contends "[t]he actual addressing information is produced by the [s]equencer, and the address generation unit 42 merely applies the received addressing information to a given physical memory configuration (*i.e.*, row/column configuration)." Reply 15; *see also*

Tr. 20:15–18 ("Averbuj teaches us a sequencer generates addresses, provides them to the memory interface, which may pass them through or may translate them. . . . It generates address and control signals.").

Averbuj discloses that "BIST controller 4 provides and communicates test algorithms to sequencers 8 for application to device blocks 6" (Ex. 1003 ¶ 29), and "[s]equencers 8 interpret" and "control the application of the test algorithms" to the memory modules (*id.* ¶ 30). *See also id.* ¶ 46 ("Sequencers 8 receive the generic BIST commands in accordance with the command protocol, and control the application of the commands by generating and issuing sequences of one or more memory operations for application to a set of respective memory modules 12."). For example, in the exemplary embodiment illustrated in Figure 5, command parser 30 of sequencer 8A processes a command received from BIST controller 4, and extracts one or more parameters from the command. *Id.* ¶¶ 41–42. Command parser 30 passes the extracted parameters to command controller 34, which then issues a sequence of one or more operations to each memory interface 10. *Id.* ¶¶ 42–43.

> In particular, . . . command controller[] 34 sequentially drives the appropriate command control signals (CMD_CTRL_SIGNALS) to carry out each operation of the sequence. The command control signals may include signals to provide a memory address and data to the receiving memory interfaces 10 and to direct the receiving memory interfaces to invert bits, perform read or write operations, invert rows, and the like.

Id. ¶ 43. "Memory interfaces 10 handle specific interface requirements for each of memory modules 12. For example, each of memory interfaces 10 may be designed in accordance with the particular signal interface

requirements and physical characteristics of the respective one of memory modules 12." *Id.* ¶ 31.

Averbuj further explains, in connection with the embodiment illustrated in Figure 6, that memory interface 41 "*transforms* the data and addresses provided by the sequencer *as needed* based on the particular physical characteristics of the memory module" (*id.* ¶ 54 (emphasis added)) using address generation unit 42 and data generation unit 44 (*id.* ¶¶ 49, 51). For example, if sequencer 8 asserts an invert rows signal and/or invert columns signal to specify a data pattern, data generation unit 44 inverts values dictated by the sequencer to generate transformed data signal 49 (BIST_DATA_T). *Id.* ¶ 57. If, however, none of the invert signals are asserted, then the BIST_DATA signal passes through XOR gates 52, 54 of data generation unit 44 without modification, and the BIST_DATA_T signal sent to memory module 12 is "the data dictated from the sequencer 8 *without modification*." *Id.* ¶ 56 (emphasis added). Likewise, "in some BIST tests," sequencer 8 may direct memory interface 41 to write BIST data in a row or column first fashion. *Id.* ¶ 51. In such case, address generation unit 42 must transform the address provided by sequencer 8 to conform to the particular row and column configuration of the memory module. *See id.* ¶¶ 51–52. "For example, a 256 bit memory module 12 may be organized as 128 rows and 2 columns, 32 rows by 8 columns, 16 rows by 16 columns, and the like." *Id.* ¶ 50.

Based on the above description in Averbuj, we agree with Patent Owner that Averbuj describes memory interfaces (the alleged data handlers) that are configured to produce address and control signals, and that Averbuj describes producing address and control signals in certain circumstances,

e.g., when Averbuj's sequencer (the alleged control module) specifies writing data in a particular pattern that requires transformation to conform to a particular configuration of a memory module. *See* PO Resp. 33. We also agree with Petitioner, however, that Averbuj's memory interfaces are further configured to apply to the memory modules the same address and control signals received from, and produced by, the sequencers for testing (*see* Reply 15), e.g., when the sequencer sends signals that can be applied, without modification or transformation (*see* Ex. 1003 ¶ 56), directly to a memory module irrespective of its physical configuration. Thus, Petitioner has shown, by a preponderance of the evidence, that Averbuj's sequencer meets the limitation of "a control module configured to generate address and control signals for testing the memory devices" as recited in challenged independent claims 1, 20, and 29 of the '434 patent.

b. "data handler . . . configured to generate" "data" (claim 1) or "cyclic data" (claim 20) for testing the memory devices

Petitioner relies on paragraphs 43, 48, and 49 of Averbuj in support of its contention that Averbuj's memory interfaces are data handlers that are configured to generate data for testing via data generation unit 44, described as "generat[ing] the exact data (RAM_DIN) applied to the memory inputs" of a memory module during testing. Pet. 12–13 (quoting Ex. 1003 ¶ 49).

Patent Owner argues Petitioner has not shown that Averbuj's memory interfaces 10 (the alleged data handlers) are configured to generate data for writing to the data ports of memory modules 12 (the alleged memory devices), because "Petitioner has not shown that the data generation unit 44 in Averbuj is capable of being programmed." PO Resp. 31 ("Averbuj's control signals for data generation (BIST_DATA_GEN_CTRL) are not

programmed – they are used to actively generate BIST_DATA_T. Without constant communication over the BIST_DATA_GEN_CTRL lines, BIST_DATA_T is not generated."). Patent Owner's argument is based on its interpretation of "configured to" as "programmed to." *Id.* at 30.

In Section III.C.1, we determined the broadest reasonable interpretation of "configured to," as used in the '434 patent claims, is "designed, adapted, or arranged to," and that one of ordinary skill in the art would understand that programmability is only one way that a component might be designed, adapted, or arranged to perform a function. In other words, lack of programmability is not determinative of whether data generation unit 44 is "configured to generate" data. We are persuaded Petitioner has shown, by a preponderance of the evidence, that Averbuj's data generation unit 44 is capable of generating data, including cyclic data, for testing memory modules 12 and, therefore, is necessarily designed, adapted, or arranged to generate data in the manner recited in challenged claims 1 and 20.

c. each data handler "operable independently" from each of the other data handlers (claims 1, 27, and 29)

Petitioner contends Averbuj describes each memory interface 10A–C (the alleged data handlers) of Figure 6 as receiving control and address data from sequencer 8 and using this information to generate address and test data that is specific to its particular memory module. Pet. 13. Petitioner argues each memory interface is operable independently from the other memory interfaces, because it "processes the sequential memory operations issued by the higher-level sequencer, and transforms the data and addresses provided by the sequencer as needed based on the particular physical characteristics of the memory module." *Id.* (citing Ex. 1003 ¶ 54). In other

words, each memory interface operates without being influenced or controlled by another memory interface because "[a] given memory interface (*i.e.*, data handler) does not communicate with any of the other memory interfaces, or with any of the memory ports used by the other memory interfaces." Reply 13 (citing Ex. 1003 ¶ 39).

Patent Owner argues Averbuj's memory interfaces (the alleged data handlers) are not operable independently, because they "are controlled by the same command control signals generated by the invoked command controller via a shared control line. Thus, the alleged plurality of data handlers, as shown in Averbuj Fig. 4, cannot be controlled independently." PO Resp. 35. In Section III.B., however, we determined the broadest reasonable interpretation of "operable independently," as used in the challenged claims, is "operable without influence or control by another."

We find Petitioner has shown, by a preponderance of the evidence that Averbuj's memory interfaces (the alleged data handlers) are capable of operating without influence or control by another data handler, for the reasons explained above and in the Petition. Patent Owner's argument is based on an overly narrow interpretation of "operable independently" as meaning that "each of the data handlers is *able to be used to independently test* a portion of one or more memory devices" (*id.* at 34), and, therefore, does not persuade us that Petitioner failed to meet its burden of proof.

d. dependent claims 14, 15, 17–19, 21–25, 27, 28, and 30–35

Claim 17 depends from claim 1 and recites: "the control module further configured to selectively input to the address and control ports of the memory devices either the address and control signals from the memory controller or the address and control signals from the control module." Ex.

1001, 17:50–54. Claim 18 depends from claim 17 and recites: "wherein the control module further comprises a DRAM controller which performs the selective inputting of the address and control" signals to the memory devices. *Id.* at 17:55–58. Claims 19 and 35 depend from claims 1 and 29, respectively, and recite: "the control module selectively inputs to the address and control ports of the memory devices the address and control signals from the control module." Petitioner contends Averbuj's multiplexer 46 meets these limitations. Pet. 19–21.

Patent Owner argues Averbuj's sequencer 8 (the alleged control module) does not selectively input the BIST_ADDR/CTRL signal to memory modules 12 (the alleged memory devices). PO Resp. 36. Rather, sequencer 8 inputs the BIST_ADDR/CTRL signal to address generation unit 42, which is part of memory interface 41 (the alleged data handler), and thereafter to multiplexer 46, i.e., the alleged device that selectively inputs the address and control signals to memory modules 12. *Id.* at 37.

Averbuj describes sequencer 8 (the alleged control module) as providing a BIST enable signal that causes multiplexer 46 of memory interface 41 (the alleged data handler) to select the BIST address/control signals provided by the sequencer. *See* Ex. 1003 ¶ 48. Averbuj states that "[i]n this manner, the sequencer controls multiplexers 45, 46 of memory interface 41 to selectively isolate the respective memory module, thereby allowing BIST algorithms to be applied to that memory module." *Id.*

We agree with Patent Owner that Petitioner has not explained adequately how Averbuj's sequencer 8 (the alleged control module) is "configured to" (i.e., designed, adapted, or arranged to) "selectively input" (claim 17) or how sequencer 8 "selectively inputs" (claims 19 and 35)

address and control signals to memory modules 12. Petitioner has not addressed Patent Owner's argument that the device that selectively inputs address and control signals to memory modules 12 is memory interface 41 (the alleged data handler), not sequencer 8 (the alleged control module). *See* Reply 17 (stating that "address and control signals, which are generated by the sequencer, are input to the address and control ports of the memory, respectively," but failing to explain how Averbuj's sequencer is configured to perform this function).

Patent Owner also contends Petitioner has not met its burden to show unpatentability of dependent claims 14, 15, 17–19, 21–25, 27, and 30–35, because Petitioner has failed to show independent claims 1, 20, and 29, from which these claims depend, are anticipated by Averbuj. PO Resp. 37–38. Patent Owner contends Petitioner has not met its burden to show unpatentability of dependent claim 28 because Petitioner has failed to show Averbuj teaches or suggests the limitations of claim 20, from which this claim depends. *Id.* at 38. We determined above that claims 1, 20, and 29 are anticipated by Averbuj. With respect to claims 14, 15, 21–25, 27, and 30–34, we have reviewed the Petition and evidence cited therein, and determine Petitioner has met its burden to show these dependent claims are anticipated by Averbuj. *See* Pet. 21–24. We also have reviewed the Petition and evidence cited therein in support of Petitioner's challenge as to claim 28, and determine Petitioner has also met its burden to show claim 28 is obvious in view of Averbuj. *See id.* at 29.

3. Conclusion

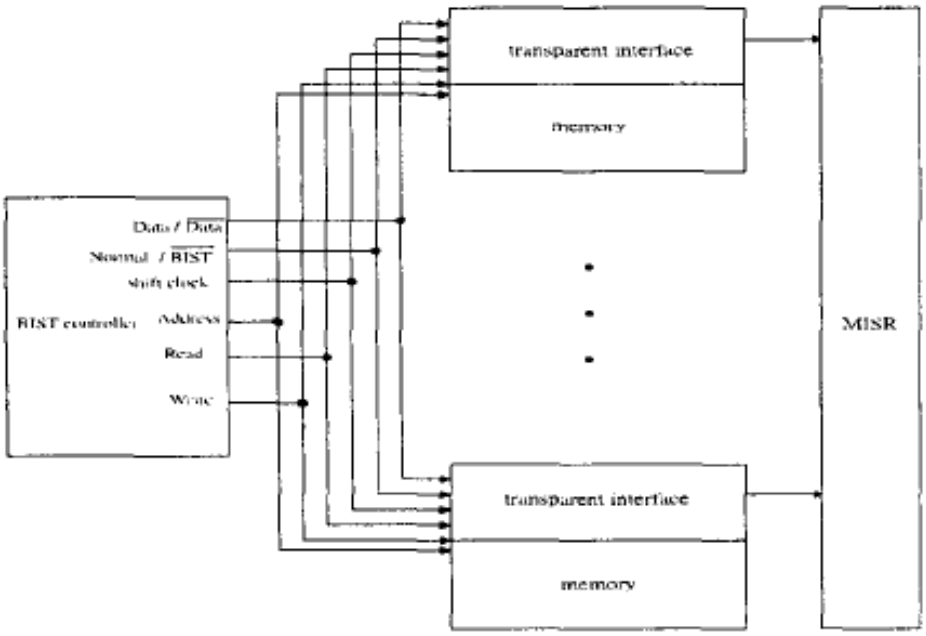
Petitioner has met its burden to show, by a preponderance of the evidence, that claims 1, 14, 15, 20–25, 27, and 29–34 are unpatentable under

35 U.S.C. §102(b) based on Averbuj and claim 28 is unpatentable under 35 U.S.C. §103(a) based on Averbuj. Patent Owner has persuaded us that Petitioner failed to meet its burden to establish unpatentability of claims 17–19 and 35 under 35 U.S.C. §102(b) based on Averbuj.

B. Alleged unpatentability of claims 1, 2, 5, 6, 14, 15, 19, and 29 under § 103(a) based on Huang and alleged unpatentabilityof claims 7–12, 17, 18, 20–25, 27, 28, and 30–35 under § 103(a) based on Huang and Averbuj

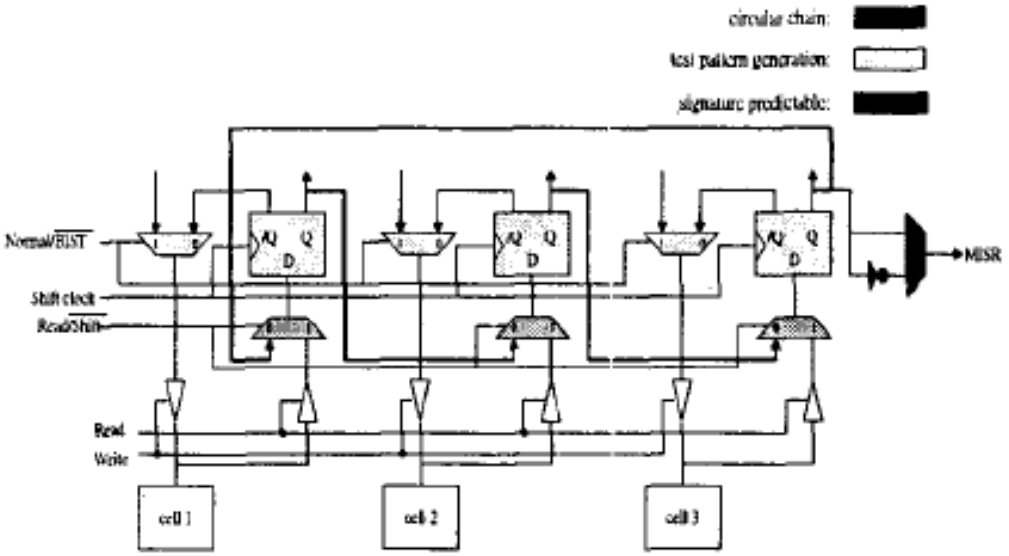
1. Huang (Ex. 1004)

Huang describes a transparent built-in self-test (TBIST) interface that is designed to perform testing of multiple embedded memory arrays in the normal mode. Ex. 1004, Abstract. Figure 2 of Huang is reproduced below:



As shown in Figure 2, above, Huang's transparent BIST system scheme includes a BIST controller, transparent test interface, memory arrays and a global multiple input shift register (MISR). *Id.* at 381, Fig. 2. As

illustrated in Figure 2, the BIST controller generates Address, and control (Normal/BIST, shift clock, Read, and Write) signals. *Id.* "[A]ll memory modules and interface circuits receive the same test control signals from the transparent BIST controller." *Id.* at 381, col. 2. Figure 1 of Huang is reproduced below:



Huang's Figure 1, above, illustrates the test interface. The test interface "implement[s] the functions of test pattern generation and test response evaluation." *Id.* at 384, col. 2. According to Huang, "the test interface generate[s] test patterns *locally* to avoid test data routing from test controller to each memory array." *Id.* at 381, col. 1. "[T]est patterns are generated by alternatively selecting Q or /Q as an input to each memory cell . . . , so the transition of Q→ /Q and /Q→Q will be exercised in each memory cell. Thus, based on the memory content left by normal operations, new test patterns are generated by complementing each memory word several times." *Id.*

2. Analysis – limitations allegedly disclosed or suggested by Huang

Independent claims 1, 20, and 29 recite a "self-testing memory module" comprising: (1) a control module; (2) a data module comprising at least one data handler; and (3) a plurality of memory devices. Petitioner contends Huang's BIST controller, test interfaces, and memory arrays teach or suggest, respectively, the aforementioned three components of claims 1, 20, and 29. Pet. 41–42 (citing Ex. 1007 ¶¶ 200–201, 207–208, and 209–210).

a. a printed circuit board configured to be operatively coupled to a memory controller of a computer system (claims 1, 20, and 29)

In addition to the above-listed three components, independent claims 1, 20, and 29 recite "a printed circuit board configured to be operatively coupled to a memory controller of a computer system." Ex. 1001, 16:34–35, 18:2–3, 59–60. Petitioner contends one of ordinary skill in the art would have found the use of a printed circuit board to assemble multiple integrated circuits and/or other components together with Huang's techniques for BIST to be an obvious, trivial implementation detail. *See* Pet. 39. Patent Owner does not directly refute Petitioner's contention, but argues "Petitioner does not cite to Huang to disclose or suggest []a printed circuit board." PO Resp. 40.

Dr. Alpert testified that "DIMM circuit boards are a standard form factor for memory modules" (Ex. 1007 ¶ 199), "us[ing] physically separate integrated circuit packages mounted on different portions of a printed circuit board . . . is established industry practice" (*id.* ¶ 229). Dr. Alpert further testified that a person of ordinary skill in the art "would have recognized that

Huang's teachings can be applied to systems with one or more components. . . . [S]uch a person would have understood that a printed circuit board would be obvious to use to assemble multiple integrated circuits and/or other components together with Huang's techniques for BIST." Ex. 1009 ¶ 71; *cf.* Ex. 1010, 21:6–14 (wherein Dr. Sechen acknowledged, on cross examination, that the concept of using BIST techniques on a printed circuit board has been in existence for about 25 years). Dr. Alpert also testified that "the number of ways to assemble multiple components is limited, and the techniques other than PCBs, such as package-on-package or multiple-chip modules with ceramic substrate, are highly specialized and relatively expensive." Ex. 1009 ¶ 70.

Patent Owner has not provided evidence that directly contradicts Dr. Alpert's testimony, or otherwise shown that Dr. Alpert's opinion is erroneous or unreasonable. Accordingly, we credit Dr. Alpert's opinion that one of ordinary skill in the art would have found the use of Huang's BIST techniques with a printed circuit board to be an easily predictable and achievable variation. "If a person of ordinary skill, before the time of invention and without knowledge of that invention, would have found the invention merely an easily predictable and achievable variation or combination of the prior art, then the invention likely would have been obvious." *Rolls-Royce, PLC v. United Technologies Corp.*, 603 F.3d 1325, 1338 (Fed. Cir. 2010).

b. "control module configured to generate address and control signals for testing the memory devices" (claims 1, 20, and 29)

Petitioner contends Huang Figure 2 "illustrates the generation of address signals by the BIST controller and reception of those signals by the

memory devices." Reply 20; *see* Pet. 41–43. Petitioner asserts that Huang Figure 2 also illustrates the generation of "read" and "write," i.e., control signals, by the BIST controller, and Huang Figure 1 illustrates that these control signals are received by the memory devices. *Id.*; *see* Pet. 41–43.

Patent Owner argues Huang's BIST controller is not "configured to generate address and control signals for testing the memory devices" (claims 1, 20, and 29), because it is not programmed to produce these signals. *See* PO Resp. 39–40, 51. Patent Owner's argument is based on an interpretation of "configured to generate" as "programmed to produce."

In Section III.C.1, we determined the broadest reasonable interpretation of "configured to," as used in the '434 patent claims, is "designed, adapted, or arranged to," and that one of ordinary skill in the art would understand that programmability is only one way that a component might be designed, adapted, or arranged to perform a function.

We find that Petitioner has shown, by a preponderance of the evidence, that Huang's BIST controller teaches or suggests the capability of generating address and control signals for testing the memory devices and, therefore, is necessarily designed, adapted, or arranged to generate address and control signals in the manner recited in challenged claims 1, 20, and 29.

c. each data handler "operable independently" from each of the other data handlers (claims 1, 27, and 29)

Patent Owner argues Huang's transparent interfaces (the alleged data handlers) are not "operable independently," because "Huang's transparent interfaces . . . are only used when Huang's BIST controller sends every . . . [transparent interface] the exact same commands" (PO Resp. 46), i.e., the transparent interfaces' "operations are intricately coordinated with each other" (*id.* at 49). Patent Owner's argument is based on an interpretation of

"operable independently" as requiring that each data handler is able to be used to independently test a portion of the memory space. *See, e.g.*, PO Resp. 47. In Section III.B, however, we determined the broadest reasonable interpretation of "operable independently" is "operable without influence or control by another."

Petitioner argues that "[w]hen the proper construction of 'operable independently' is applied, it is apparent that each of Huang's transparent memory interfaces (*i.e.*, data handlers) meets this claim limitation, since they each correspond to an associated memory device, and locally generate test data for the associated memory device." Reply 21 (citing Pet. 38). Petitioner's argument is persuasive, and Patent Owner has not explained sufficiently why each of Huang's transparent memory interfaces is not operable without influence or control by another transparent interface. *See generally*, PO Resp. 41–49; *see also* Reply 21 (citing Ex. 1010, 249:6–11 (wherein Dr. Sechen, when questioned about the operation of the transparent memory interfaces A and B (corresponding to the claimed data handlers), illustrated in Figure 4 of Huang, acknowledged that "when transparent memory interface A is applying a test pattern to memory module A," it does not "affect how transparent memory interface B is applying its test pattern to memory module B")). Therefore, Patent Owner has not refuted Petitioner's prima facie showing that Huang teaches or suggests that its transparent memory interfaces are "operable independently" as recited in challenged claims 1, 27, and 29.

d. "data handler . . . configured to generate data" (claim 1) for testing the memory devices

Independent claim 1 requires that "each data handler" is "configured to generate data for writing to the corresponding plurality of data ports" of

the memory devices. Ex. 1001, 16:43–48. Petitioner contends Huang's transparent interfaces (the alleged data handlers) are described as generating test patterns locally, and, therefore, it logically follows that they are "designed, arranged or adapted to perform the function of data generation." Reply 19; *see* Pet. 42.

Patent Owner argues Huang's transparent interfaces are not "configured to generate data" (claim 1) because they do not receive a signal that can be used for programming. PO Resp. 38. Patent Owner's argument is based on an overly narrow interpretation of "configured to generate" as "programmed to produce."

We find that Petitioner has shown, by a preponderance of the evidence, that Huang's transparent interfaces are capable of generating data for writing to the memory devices and, therefore, are necessarily designed, adapted, or arranged to generate data in the manner recited in challenged claim 1.

e. dependent claims 2, 5, 6, 14, 15, and 19

Claim 2 depends from claim 1 and recites: "wherein the plurality of data handlers comprise at least two physically separate components mounted on the printed circuit board." Ex. 1001, 16:53–55. Claims 5 and 6 depend from claim 2. Patent Owner contends Petitioner has not identified a teaching or suggestion of these limitations in Huang. *Id.* at 49–50. Patent Owner also contends Petitioner has not met its burden to show dependent claims 2, 5, 6, 14, 15, and 19 are unpatentable over Huang, because Petitioner has failed to show independent claim 1, from which these claims depend, would have been obvious in view of Huang. PO Resp. 50.

In its Reply, Petitioner directs us to page 39 of the Petition wherein it

argues, with respect to the independent claims, that implementation of a plurality of memory devices on the printed circuit board in Huang would have been a trivial detail. Reply 22. Petitioner further argues "the implementation of Huang's transparent memory interfaces on the PCB as either a single component or as multiple components is merely a design choice for a [person of ordinary skill in the art]." *Id.* at 22–23. In support of this latter statement, Petitioner cites the second Alpert declaration. Upon review of the Petition, however, we agree with Patent Owner (*see* PO Resp. 49) that Petitioner relied exclusively on Tsern for a disclosure or suggestion of this limitation (*see* Pet. 44). *Compare* Ex. 1007 ¶ 219 ("The combination of Huang and Tsern discloses each element of claim 2.") *and* ¶ 221 (testifying "[t]o the extent that this additional claim element may not be disclosed by Huang alone, it is obvious in view of Tsern," but failing to explain how the claim 2 limitations are disclosed or suggested by Huang) *with* Ex. 1009 ¶ 71 ("A person of ordinary skill in the art would have understood that an embedded computer system can be implemented as a single integrated circuit or as multiple integrated circuits ("chips") and other components.").

Rule 42.22(a)(2) provides that a petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent." 37 C.F.R. § 42.22(a)(2). Rule 42.23(b) provides that "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response." 37 C.F.R. § 42.23(b). Practice relating to replies is addressed in the Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012):

> While replies can help crystalize issues for decision, a reply that raises a new issue or belatedly presents evidence will not be considered and may be returned. The Board will not attempt to sort proper from improper portions of the reply. Examples of indications that a new issue has been raised in a reply include new evidence necessary to make out a *prima facie* case for the patentability or unpatentability of an original or proposed substitute claim, and new evidence that could have been presented in a prior filing.

"Whether a reply contains arguments or evidence that are outside the scope of a proper reply under 37 C.F.R. § 42.23(b) is left to our determination." *Vibrant Media Inc. v. General Electric Co.*, Case IPR2013-00170, slip op. at 31 (PTAB June 26, 2014) (Paper 56).

In our judgment, Petitioner's arguments and evidence in the Reply are outside the scope of a proper reply because they do more than merely address Patent Owner's argument that the Petition does not identify a disclosure or suggestion of the claim 2 limitations in Huang; rather, they attempt to provide a new theory for modifying Huang that was not set forth clearly in the Petition. Consideration by the Board of these arguments in the Reply and evidence presented in Dr. Alpert's second declaration in support thereof would be unfair to Patent Owner. We have, however, reviewed and considered the arguments in the Petition and evidence therein, and are in agreement with Patent Owner that Petitioner has not provided adequate explanation or evidence to support its contention that Huang discloses or suggests the limitations recited in claim 2. Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claim 2 and its dependent claims 5 and 6 would have been unpatentable over Huang.

With respect to claims 14, 15, and 19, we have reviewed the Petition and evidence cited therein, and determine Petitioner has met its burden to

show these claims are unpatentable as obvious in view of Huang. *See* Pet. 47–50.

3. Analysis – limitations allegedly disclosed or suggested by Huang in view of Averbuj

Independent claim 20 differs from claim 1 in that it requires "at least one data handler" "configured to generate *cyclic* data for writing to the corresponding plurality of data ports" of the memory devices. Ex. 1001, 18:10–14 (emphasis added). Claim 21 depends from claim 20 and recites:

> wherein the at least one data handler is further configured to read data from the corresponding plurality of data ports and further comprises a verification element for checking for failures in the operation of the memory devices by verifying that data read from the corresponding plurality of data ports corresponds to the data generated by the data handler for writing to the corresponding plurality of data ports.

Ex. 1001, 18:19–26. Claim 7 depends indirectly from independently claim 1 and includes a similar limitation. *Id.* at 17:5–10. Claim 30, which depends from independent claim 29, recites a step of "checking for failures in the operation of the memory devices by each of the plurality of data handlers by verifying that data read from the corresponding plurality of data ports corresponds to the generated data for writing to the corresponding plurality of data ports." *Id.* at 19:15–19.

With respect to claim 20, Petitioner contends Huang discloses data handlers (i.e., the test interfaces) that are capable of generating test patterns, and Averbuj discloses a data handler (i.e., data generation unit (44)) that "may be instructed to generate different types of test patterns, including a checkerboard pattern (*i.e.*, cyclic data)." Pet. 50–51 (citing Ex. 1003 ¶ 49). Petitioner contends that employing cyclic test patterns, as taught by Averbuj,

in Huang's system would have been an obvious implementation of a known technique commonly employed in BIST systems. *Id.* at 51 (citing Ex. 1007 ¶¶ 281–282).

With respect to claims 7, 21, and 30, Petitioner contends Averbuj's comparator 48 corresponds to the claimed verification element. *See* Pet. 51–52 (citing Ex. 1003 ¶ 53; Figs. 6, 10). Petitioner contends one of ordinary skill in the art "would have been motivated to combine the self-testing memory modules disclosed in Huang . . . with these teachings of Averbuj because (among other reasons) adding this functionality within the memory interface furthers Huang's desire to perform test data operations locally to avoid excess data routing." Pet. 52 (citing Ex. 1007 ¶¶ 283–284, 309–310, and 323–324).

Patent Owner contends Petitioner has not shown how Huang and Averbuj could be combined in the manner claimed. PO Resp. 52, 57. Patent Owner relies on the declaration testimony of Dr. Sechen to establish Huang and Averbuj are incapable of being combined. *Id.* at 54–55 (citing Ex. 2012 ¶¶ 235–241); *id.* at 57 (citing Ex. 2012 ¶¶ 244–248).

Dr. Sechen testified that he had "not found in either Dr. Alpert's or Petitioner's materials, any assertion as to how a [person of ordinary skill in the art] would even attempt to modify the Huang circuit to allow Averbuj's sequencer," and "[e]ven if it were assumed that [the ordinary artisan] would have attempted to combine Huang and Averbuj, the combination would not have worked for its intended purpose." Ex. 2012 ¶ 240. Dr. Sechen testified that "[t]he *cyclic data* generation in Averbuj is controlled by the sequencer, . . . [which] instructs the data generation unit 44 to generate different types of test patterns, including a checkerboard pattern (i.e., the alleged *cyclic*

data)." *Id.* ¶ 237. Dr. Sechen further testified that "one of ordinary skill in the art would understand that Huang's data generation is tied to the memory contents, and specific data patterns cannot be selected by Averbuj's sequencer. . . . Huang is unable to be instructed to generate different types of test patterns." *Id.* ¶¶ 238–239. Dr. Sechen also testified as to why he believed Averbuj's verification element could not be added to Huang. *See id.* ¶¶ 244–247.

In its Reply, Petitioner contends Patent Owner has "fail[ed] to consider the references as a whole," and has "mistakenly argue[d] that applying specific components of Averbuj with the system of Huang would render the resulting system unfit for its intended purpose." Reply 23. Petitioner explains that according to its proposed combination, Huang's Normal/BIST signal would be used to switch between the data outputs of Huang's testing scheme and Averbuj's testing scheme. *Id.* at 24. Petitioner relies on testimony in Dr. Alpert's second declaration in support of its arguments. *See id.* (citing Ex. 1009 ¶¶ 76–81).

Dr. Alpert testified that "Dr. Sechen's analysis fails to recognize the motivation for combining Huang and Averbuj because he erroneously conflates various types of testing that are used for different purposes at different times." Ex. 1009 ¶ 76. Dr. Alpert goes on to provide detailed opinion testimony on the understanding of the ordinary artisan with respect to the teachings of Huang and Averbuj, and a detailed explanation of how Huang's system could be modified to include Averbuj's testing system and the motivation of the ordinary artisan to make such combination. *See id.* ¶¶ 77–80. According to Dr. Alpert, "[a] person of ordinary skill in the art would have seen the combination of Averbuj and Huang as choosing from a

finite number of identified, predictable solutions, with a reasonable expectation of success." *Id.* ¶ 80.

At oral argument, Patent Owner confirmed its understanding of Petitioner's challenge, as set forth in the Petition, as "starting with Huang and bringing in one element from Averbuj." Tr. 59:24–25. Patent Owner argued that "Petitioner's reply changes the combination to comprise Averbuj's entire system, not just the cyclic test generation portion." *Id.* at 59:21–23. Patent Owner argued that the Petition includes only conclusory statements of a motivation to combine and fails to explain how Averbuj and Huang are combinable. *See id.* at 60:7–15. Patent Owner also argued Dr. Alpert's second declaration and deposition present new opinions as to how Averbuj and Huang could be combined. *Id.* at 53:3–5.

Petitioner contended the challenge, as set forth in the Petition, and Dr. Alpert's first declaration in support thereof, were sufficient because combining Averbuj and Huang was trivial. *See id.* at 26:15–17. Petitioner contended Dr. Alpert did not express new opinions in his second declaration and deposition, but was merely responding to Dr. Sechen's testimony. *Id.* at 81:17–19; *see also*, *id.* at 82:20–83:3 (wherein Petitioner argued: "[I]n their response, Patent Owner took the position that . . . it was physically incapable to combine Averbuj and Huang. We're entitled to respond to that and show that, in fact, they're not correct, and we did it by saying, listen, we pointed to the multiplexers in the petition, it's super, it's simple to use those multiplexers to combine. . . . [I]t is not incapable. A person of skill in the art could have done that.").

As discussed in Section IV.B.2.e., a petition must include "[a] full statement of the reasons for the relief requested, including a detailed

explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent" (37 C.F.R. § 42.22(a)(2)), and "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response" (37 C.F.R. § 42.23(b)).

We agree with Patent Owner that the Reply does more than merely respond to or rebut arguments made in Patent Owner's Response; rather, it sets forth a theory that was not presented clearly in the Petition. Patent Owner's position is supported by the fact that Dr. Sechen, whose skill level is at least (and appears to exceed) that of the ordinary artisan, apparently was unable to envision how Huang and Averbuj could be combined. Further, Dr. Alpert's second declaration includes, at a minimum, opinions as to the understanding of the ordinary artisan with respect to the teachings of Huang and Averbuj that were not presented in his first declaration.

In our judgment, consideration by the Board of the above-noted arguments in the Reply and evidence presented in Dr. Alpert's second declaration in support thereof would be improper under 37 CFR § 42.23 and unfair to Patent Owner. We have, however, reviewed and considered the arguments in the Petition and evidence therein, and are in agreement with Patent Owner that Petitioner has not provided adequate explanation or evidence to support its contention that one of ordinary skill in the art would have had a reasonable expectation of success in combining Huang and Averbuj. Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 7–12, 17, 18, 20–25, 27, 28, and 30–35 would have been unpatentable over Huang and Averbuj.

4. Conclusion

Petitioner has met its burden to show, by a preponderance of the

evidence, that claims 1, 14, 15, 19, and 29 are unpatentable under 35 U.S.C. §103(a) based on Huang. Patent Owner has persuaded us that Petitioner failed to meet its burden to establish unpatentability of claims 2, 5, and 6 under 35 U.S.C. §103(a) based on Huang and claims 7–12, 17, 18, 20–25, 27, 28, and 30–35 under 35 U.S.C. §103(a) based on Huang and Averbuj.

C. Alleged unpatentability of claims 13 and 26 under 35 U.S.C. § 103(a) based on Huang, Averbuj, and JEDEC Standard

Claims 13 and 26 depend, respectively, from claims 7 and 21. Petitioner relies on JEDEC Standard (Ex. 1006) as evidence that at the time of the invention claimed in the '434 patent, it was known in the art to record failing data and corresponding addresses for BIST failures as recited in claims 13 and 26 (Pet. 33–34, 57–58 (citing Ex. 1006 § 8.2.4.5)), and contends it would have been obvious to have recorded failing data and corresponding addresses in Averbuj's and Huang's BIST systems to enable a failure analysis and determination of error locations (*id.* at 34, 58). Petitioner's challenge does not present further arguments or evidence to cure the deficiencies in its challenge with respect to claims 7 and 21. *See* Section IV.B.3, above.

Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 13 and 26 would have been unpatentable under 35 U.S.C. §103(a) based on Huang, Averbuj, and JEDEC standard.

V. CONCLUSION

Petitioner has met its burden to show, by a preponderance of the evidence, unpatentability of: claims 1, 14, 15, 20–25, 27, and 29–34 under 35 U.S.C. §102(b) based on Averbuj; claim 28 under 35 U.S.C. §103(a)

based on Averbuj; and claims 1, 14, 15, 19, and 29 under 35 U.S.C. §103(a) based on Huang.

Petitioner has failed to meet its burden to establish unpatentability of: claims 17–19 and 35 under 35 U.S.C. §102(b) based on Averbuj; claims 2, 5, 6, under 35 U.S.C. §103(a) based on Huang; claims 7–12, 17, 18, 20–25, 27, 28, and 30–35 under 35 U.S.C. §103(a) based on Huang and Averbuj; and claims 13 and 26 under 35 U.S.C. §103(a) based on Huang, Averbuj, and JEDEC Standard.

VI. ORDER

For the reasons given, it is

ORDERED that claims 1, 14, 15, 19–25, and 27–34 are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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