UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2014-00971
U.S. Patent 8,359,501 B1

NETLIST INC.'S NOTICE OF APPEAL
TO THE U.S. COURT OF APPEALS FOR THE FEDERAL CIRCUIT

Via PRPS
Patent Trial and Appeal Board

Via Hand Carry
Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

Via CM/ECF
United State Court of Appeals for the Federal Circuit

Pursuant to 35 U.S.C. §§ 141, 142, and 319, 37 C.F.R. §§ 90.2, 90.3, and 104.2, and Rule 4(a) of the Federal Rules of Appellate Procedure, Patent Owner Netlist, Inc. hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision, dated December 14, 2015 (Paper 34) and the Final Written Decision (Paper 37) entered by the Patent Trial and Appeal Board on April 27, 2016. In particular, Patent Owner identifies the following issues on appeal:

- The Board's judgment that Claims 1–3, and 5–20 of U.S. Patent No. 8,359,501 B1 are unpatentable;
- The Board's claim construction; and
- Any Board finding, determination, judgment, or order supporting or related to the Final Written Decisions and decided adversely to Patent Owner.

Patent Owner is concurrently filing true and correct copies of this Notice of Appeal, along with the required fees, with the United States Court of Appeals for the Federal Circuit, and with the USPTO Patent Trial and Appeal Board.

Respectfully submitted,

Dated: June 29, 2016

/*Thomas J. Wimbiscus*/
Thomas J. Wimbiscus
Registration No. 36,059

MCANDREWS HELD & MALLOY
500 West Madison, 34th Floor
Chicago, IL 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100

CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PRPS, a true and correct copy of the above-captioned **NETLIST INC.'S NOTICE OF APPEAL** is being filed by hand with the Director on June 29, 2016, at the following address:

Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

The undersigned also herby certifies that a true and correct copy of the above-captioned **NETLIST INC.'S NOTICE OF APPEAL** and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on June 29, 2016.

Dated: June 29, 2016

/*Thomas J. Wimbiscus*/
Thomas J. Wimbiscus
(Registration No. 36,059)
Counsel for Patent Owner
Netlist Inc.

CERTIFICATE OF SERVICE

The undersigned hereby certified that the foregoing **NETLIST INC.'S NOTICE OF APPEAL** was served electronically via e-mail on June 29, 2016 in its entirety on the following:

Lori A. Gordon
Robert E. Sokohl
STERNE, KESSLER,
GOLDSTEIN & FOX P.L.L.C
1100 New York Avenue, N.W.
Washington, D.C. 20005
Lgordon-PTAB@skgf.com
Rsokohl-PTAB@skgf.com

Respectfully submitted,

Dated: June 29, 2016

/*Thomas J. Wimbiscus*/
Thomas J. Wimbiscus
Registration No. 36,059

MCANDREWS HELD & MALLOY
500 West Madison, 34th Floor
Chicago, IL 60661
Telephone: (312) 775-8000
Facsimile: (312) 775-8100

Trials@uspto.gov
571-272-7822

Paper 34
Entered: December 14, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00971
Patent 8,359,501 B1

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Sandisk Corporation ("Petitioner") filed a Petition (Paper 1, "Pet.") on June 18, 2014, requesting institution of an *inter partes* review of claims 1–20 (the "challenged claims") of U.S. Patent No. 8,359,501 B1 (Ex. 1001, "the '501 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp."). Based on these submissions, an *inter partes* review of claims 1–20 was instituted on December 16, 2014, pursuant to 35 U.S.C. § 314. Paper 12 ("Dec. on Inst." or "Institution Decision").

After institution, Patent Owner filed a Response (Paper 19, Corrected Patent Owner Response, "PO Resp."), and Petitioner filed a Reply to the Patent Owner Response (Paper 25, "Reply").

Patent Owner also filed a Motion for Observation Regarding Cross-Examination of Dr. Donald Alpert. Paper 28 ("PO Mot."). Petitioner filed a Response to the Motion (Paper 32, "Pet. Resp."). Oral argument was held on July 27, 2015. A transcript of the oral hearing ("Tr.") has been entered into the record. *See* Paper 33.

The Board has jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision, issued pursuant to 35 U.S. C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–3, 5–8, and 11–20 of the '501 patent are unpatentable. Petitioner has not met its burden to show that claims 4, 9, and 10 are unpatentable.

A. Related Proceedings

Petitioner also requested, and we instituted, an *inter partes* review of U.S. Patent No. 8,001,434 ("the '434 patent"). The '501 patent claims priority as a continuation of the '434 patent: *Sandisk Corp. v. Netlist, Inc.*,

Case IPR2014-00970 (PTAB December 16, 2014). Oral argument in IPR2014-00970 was consolidated with the oral argument in the present *inter partes* review. A final decision in IPR2014-00970 is issued concurrently with this final decision.

Patent Owner informs us that the ’501 patent is the subject of an infringement action filed by Patent Owner: *Netlist, Inc. v. Smart Modular Technologies, Inc.*, No. 4:13-cv-05889-YGR (N.D. Cal. Dec. 19, 2013). Paper 9, 2. SMART Modular Technologies, Inc., a named defendant, filed two petitions for *inter partes* review of the ’501 patent on August 23, 2014: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Cases IPR2014-01374 and IPR2014-01375 (PTAB). *Id.* at 3. On August 23, 2014, SMART Modular Technologies, Inc. also filed two petitions for *inter partes* review of the related ’434 patent: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Cases IPR2014-01372 and IPR2014-01373 (PTAB). *Id.* On March 10, 2015, we instituted *inter partes* reviews in IPR2014-01372 and IPR2014-01374. IPR2014-01372, Paper 13; IPR2014-01374, Paper 12. Oral arguments for IPR2014-01372 and IPR2014-01374 were consolidated, and held on November 17, 2015.

B. The ’501 patent (Ex. 1001)

The ’501 patent relates to self-testing electronic memory modules. Ex. 1001, 1:27–28. A block diagram of an exemplary self-testing memory module is shown in Figure 3 of the ’501 patent, reproduced below. *See id.* at 9:25–26.

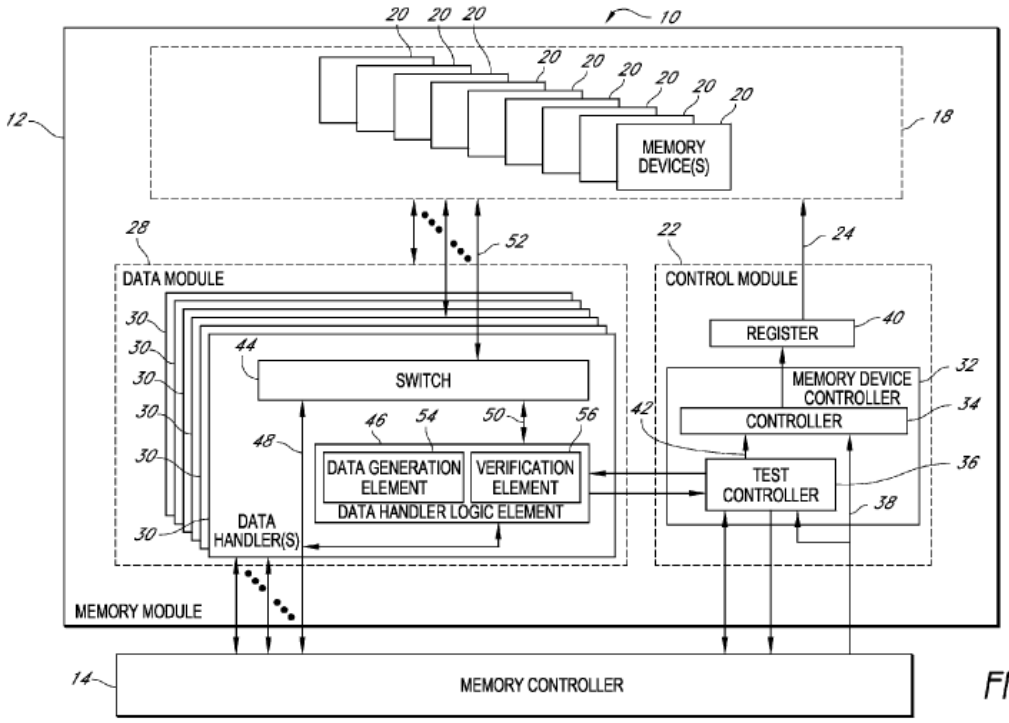

FIG. 3

As illustrated in Figure 3, above, "memory module 10 includes a printed circuit board 12 configured to be operatively coupled to a memory controller 14 of a computer system 16." *Id.* at 5:6–8. Memory module 10 includes a plurality of memory devices 18, each memory device 20 of the plurality of memory devices 18 comprising data, address, and control ports. *Id.* at 5:8–12. "[M]emory module 10 comprises a control module 22 [and] . . . a data module 28." *Id.* at 5:12–15.

"[C]ontrol module 22 can be configured to generate address and control signals 24 for testing the plurality of memory devices 18." *Id.* at 9:29–31. In the embodiment shown in Figure 3, control module 22 includes control mixer element 32 for controlling the address and control signals for the self-testing function. *Id.* at 9:35–37. Control mixer element 32 includes memory device controller 34 (e.g., a DRAM controller) and test controller 36. *Id.* at 9:33–35. "[T]est controller 36 controls the generation of the

address and control signal sequences to be used during the self-testing operation of the memory module 10 and also communicates with the data module 28." *Id.* at 9:53–56. "[M]emory device controller 34 receives signals 38 (e.g., address and control signals) from the system memory controller 14 and signals 42 (e.g., address and controls signals) from the test controller 36." *Id.* at 9:41–44.

Data module 28 comprises a plurality of data handlers 30 that "may be operatively coupled to (e.g., logically and/or electrically coupled to) the corresponding plurality of data ports" of memory devices 18. *Id.* at 5:14–16, 21–23. In the embodiment illustrated in Figure 3, each of data handlers 30 includes data handler logic element 46, comprising data generation element 54 and verification element 56. *Id.* at 10:31–34. "[D]ata generation element 54 may be configured to generate data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports" of memory devices 18. *Id.* at 10:35–37. "The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." *Id.* at 10:37–41.

C. Illustrative Claims

Independent claims 1 and 16 are illustrative of the claimed subject matter:

> 1. A memory system configured to be operatively coupled to a memory controller of a computer system, the memory system comprising:
>
> a plurality of memory chips;
>
> a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured

to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips;

a control circuit configured to generate address and control signals, wherein the memory system is configured to test the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the one or more data handlers.

16. A method of operating a memory system configured to be operatively coupled to a memory controller of a computer system, the memory system having a plurality of memory chips, the method comprising:

operating a plurality of data handlers independently from one another to generate and transmit data to one or more memory locations of one or more memory chips of the plurality of memory chips;

operating a control circuit to generate address and control signals; and

testing the one or more memory locations of the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the plurality of data handlers.

D. The Prior Art

The instituted grounds of unpatentability in this *inter partes* review are based on the following prior art:

Reference	**Publication**	**Exhibit**	**Date**
Averbuj	U.S. Patent Application Publication No. 2005/0257109 A1	1003	Nov. 17, 2005
Huang	*An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers*, Fourteenth International Conference on VLSI Design 379–384 (2001), IEEE	1004	2001

Reference	Publication	Exhibit	Date
JEDEC Standard	JEDEC Standard, Fully Buffered DIMM (FBDIMM): DFx Design for Validation and Test, JESD82–28	1006	Feb. 2008

E. The Instituted Grounds of Unpatentability

We instituted the instant *inter partes* review of claims 1–20 on the following grounds:

Claims	Basis	Reference(s)
1–3, 5–8, and 11–20	§ 102(b)	Averbuj
1–5 and 14–16	§ 103(a)	Huang
6–8, 11, and 17–20	§ 103(a)	Huang and Averbuj
9 and 10	§ 103(a)	Huang and JEDEC Standard

F. Expert Testimony

Petitioner relies on the testimony of Dr. Donald Alpert in support of its patentability challenges. Dr. Alpert executed a first declaration (Ex. 1007) in support of the Petition and a second declaration (Ex. 1009) in support of Petitioner's Reply. Dr. Alpert was cross-examined on the subject matter of his first and second declarations, and transcripts of the testimony were filed as Exhibits 2013 and 2021, respectively.

Dr. Alpert testified that he "received an Electrical Engineering Ph.D. degree in 1984 from Stanford University." Ex. 1007 ¶ 6. Dr. Alpert testified that he taught classes in computer architecture at Stanford, Tel

Aviv, and Arizona State Universities (*id.*), and that he worked in the computer industry, i.e., designing microprocessors and components for Burroughs Corporation, Zilog, National Semiconductor, and Intel, at various times between 1976 and 1997 (*id.* ¶ 7). Dr. Alpert testified that his "own training and experience exceeds that of ordinary skill in the art." *Id.* ¶ 21.

Patent Owner relies on the testimony of Dr. Carl Sechen. Dr. Sechen executed a declaration (Ex. 2012) in support of Patent Owner's Response. Dr. Sechen was cross-examined on the subject matter of his declaration, and a transcript of the testimony was filed as Exhibit 1010.

Dr. Sechen testified that he "was awarded a Ph.D. in electrical engineering from the University of California at Berkeley in 1986" (Ex. 2012 ¶ 6), and has been a Professor of Electrical Engineering for more than 28 years (*id.* ¶ 3). Dr. Sechen testified that during this time period, his research has focused on design and computer-aided design of digital integrated circuits, including the design of DRAM, and that he has taught numerous students how to design DRAM memories. *Id.* Dr. Sechen testified that he has "also been involved in numerous research projects on VLSI design and memory design[, and has] . . . taught numerous graduate researchers how to design digital integrated circuits, including memories." *Id.* ¶ 5. Dr. Sechen testified that he is "at least a person of ordinary skill" in the art of memory module design. *Id.* ¶¶ 33–34.

To testify as an expert under Federal Rule of Evidence (FRE) 702, a person need not be a person of ordinary skill in the art, but rather "qualified in the pertinent art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co., Inc.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's

ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 Fed. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). There is no dispute that Dr. Alpert and Dr. Sechen are qualified to testify as experts under FRE 702.

II. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is relevant to claim construction and determinations of anticipation and obviousness. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966) (explaining that obviousness is a question of law based on underlying factual findings including the level of ordinary skill in the pertinent art); *Yorkey v. Diab*, 605 F.3d 1297, 1300 (Fed. Cir. 2010) (explaining that a determination of anticipation involves, interpreting the claim language and then comparing the construed claim to a prior art reference); *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259–60 (Fed. Cir. 2010) ("[C]laim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.").

Petitioner's expert, Dr. Alpert, and Patent Owner's expert, Dr. Sechen, disagree as to the level of ordinary skill in the art. Dr. Alpert testified that "a person of ordinary skill in the art for the '501 patent would have a bachelor's degree or the equivalent training or experience in electrical engineering and at least one year of experience relating to memory systems and BIST." Ex. 1007 ¶ 20. Dr. Sechen testified that

> one of ordinary skill in the art at the time of filing the application(s) for the '501 patent, who would be working on the design of memory devices and memory modules, would have at least a Bachelor of Science degree in electrical engineering or computer engineering, and at least five years of industry experience designing memory devices and memory modules. Alternatively, one of ordinary skill in the art would have an M.S. degree in electrical engineering or computer engineering, and at least three years of industry experience designing memory devices and memory modules. Moreover, one of ordinary skill in the art would have a Ph.D. degree in electrical engineering or computer engineering, and have at least one year of industry experience designing memory devices and memory modules.

Ex. 2012 ¶ 33.

The difference in the opinions of the two experts is that Dr. Sechen believes a person of ordinary skill in the art would have an additional four years of experience, education, or a combination of the two, beyond that proposed by Dr. Alpert. *See* Ex. 1009 ¶ 7. According to Dr. Alpert, the difference in the proposed levels of ordinary skill in the art is not material to any dispute over claim construction or patentability in this *inter partes* review. *Id.*

We accord greater weight to Dr. Alpert's opinion as to the level of ordinary skill in the art because he has experience in both teaching students and working with engineers in the industry, while Dr. Sechen's experience is primarily in teaching. *Compare* Ex. 1007 ¶¶ 7, 21, *with* Ex. 2012 ¶¶ 3, 5. Moreover, based on our review of the '501 patent and the types of problems and solutions described in the '501 patent and cited prior art, we agree with Dr. Alpert's opinion on the level of ordinary skill. Accordingly, we find that a person of ordinary skill in the art at the time of the '501 patent would have

a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST.

III. CLAIM CONSTRUCTION

In its Petition, Petitioner requested that "each claim be construed in accordance with its plain and ordinary meaning under the required broadest reasonable interpretation" standard. Pet. 6–7. In its Preliminary Response, Patent Owner offered a specific construction for the claim term "generate." Prelim. Resp. 24–26. For purposes of our Institution Decision, we interpreted the claim term "generate" as meaning "produce" or "cause." Dec. on Inst. 9.

In its Response, Patent Owner disagrees with the Board's interpretation of "generate" (*see* PO Resp. 19), and further asserts that express construction of the claim language "configured to generate" (claim 1) is "necessary in view of the arguments made by Petitioner" (PO Resp. 14). Patent Owner also proposes a construction for "operated independently" (claim 1)/"operating . . . independently" (claim 16). PO Resp. 32.

In its Reply, Petitioner asserts that "'configured to,' 'operated independently,' and 'generate' are common words whose plain and ordinary meanings are well-known, even to a lay person" and, therefore, "the terms should be given their plain and ordinary meaning." Reply 1. Petitioner contends Patent Owner's proposed constructions "import[] limitations from the specification into the claims, which is impermissible." *Id.* Petitioner also provides proposed constructions of the claim terms/phrases in dispute.

See generally Reply 2–9.

Patent Owner's and Petitioner's proposed constructions for the disputed claim language are listed in the table below.

Claim Term/Phrase	**Patent Owner's Proposed Construction**	**Petitioner's Proposed Construction**
Operated independently/ Operating . . . independently	a plurality of data handlers configured to be *used to independently test*/*using* a plurality of data handlers *to independently test* (PO Resp. 32)	the operation of a data handler is not influenced or controlled by another data handler (Reply 4)
Generate	produce (PO Resp. 31)	produce or cause production of (Reply 8 n.2)
Configured to generate	programmed to produce (PO Resp. 20)	designed to, arranged to, or adapted to perform the function of producing or causing (Reply 7)

In an *inter partes* review, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definitions for claim terms must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). "[E]xtrinsic evidence may be used only to assist in the proper understanding of the disputed limitation; it may not be used to vary, contradict, expand, or limit the claim language from how it is defined, even

by implication, in the specification or file history." *Tempo Lighting, Inc. v. Tivoli*, LLC, 742 F.3d 973, 977–78 (Fed. Cir. 2014) (internal quotations and citations omitted). Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999). A court may revisit and alter its construction of claim terms as the record in a case develops. *See Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd*, 599 F.3d 1308, 1322 (Fed. Cir. 2010).

Applying the foregoing principles of law, we review our construction of the claim term "generate,"[1] and also determine that the claim terms "configured to" and "operated independently"/"operating . . . independently" require construction.

A. Operated Independently/Operating . . . Independently

Independent claim 1 recites: "a plurality of data handlers configured to be operated independently from one other." Ex. 1001, 16:42–43. Independent claim 16 recites "operating a plurality of data handlers independently from one another" *Id.* at 18:15–16.

In its Response, Patent Owner asserts that the above recitations in claims 1 and 16 mean that the data handlers are used to *independently test* a portion of one or more memory chips. PO Resp. 32. During the oral hearing, Patent Owner argued that "'[o]perating independently' necessarily means that the use or operation of a data handler is not dependent on the use or operation of another data handler for testing. For example, to be 'independently operable' means that one data handler can be used – i.e.,

[1] Our interpretation of the term "generate" also applies to other verb tenses used in the claims, i.e., "generating" and "generated."

operated – in one mode while another data handler is operated or used in another mode." Tr. 43:1–6. Petitioner contends "'*operable independently*' merely means that each data handler can operate without influence or control by any of the other data handlers." Reply 3 (citing Ex. 1009 ¶ 15 ("This would encompass data handlers that receive common control signals from one controller, as long as the data handlers are not in communication with each other.")).

In their papers, both Patent Owner (PO Resp. 32) and Petitioner (Reply 3) rely on column 8, lines 5–15 of the '501 patent in support of their proposed constructions:[2]

> Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28. *For example, each data handler 30 is configured to write to and/or read from the corresponding plurality of data ports of one or more of the memory devices 20 without being in communication [with] any of the other data handlers 30 or other data ports of the memory devices 20.* As such, each data handler 30 can be used to generally independently test a portion of the memory space of the memory module 10. For example, each data handler 30 may be used to independently test one memory device 20 of the memory module 10.

Ex. 1001, 8:5–15 (emphasis added). Petitioner quotes lines 1–11 in their entirety. Reply 3. Patent Owner omits the italicized language from its quotation. PO Resp. 32; *cf.* Tr. 43:16–18 (arguing that this language is immaterial to construction of the claim term "operable independently," because it "relates to reading and writing to the data ports[, not] . . . to data generation, which is the claimed operation of the data handler") .

[2] Both parties also rely on the testimony of their experts and Petitioner relies on a dictionary definition. *See generally* PO Resp. 32; Reply 2–4.

We begin our interpretation of the disputed terms with the language of the claims. *See Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1299 (Fed. Cir. 2015).

Independent claim 1 recites: "a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips." Ex. 1001, 16:42–46. Claim 1 also recites "wherein the memory system is configured to test the one or more memory chips . . . using the data generated by the one or more data handlers. *Id.* at 16:48–51. Claim 1 thus requires that each of the plurality of data handlers is configured to be operated independently, but that only some of the data handlers (i.e., "one or more") are further configured to generate data used for testing. Patent Owner's proposed interpretation of "configured to be operated independently" (claim 1) as "configured to be used independently" (PO Resp. 32) narrows the meaning of this claim 1 phrase to encompass only the subset of data handlers that are also "configured to generate data" (claim 1). Patent Owner's proposed interpretation of "configured to be operated independently" (claim 1) is, therefore, inconsistent with the use of this phrase in the context of claim 1 in its entirety.

Independent claim 16 recites "operating a plurality of data handlers independently from one another to generate and transmit data to one or more memory locations of one or more memory chips of the plurality of memory chips" and "testing the one or more memory locations of the one or more memory chips . . . using the data generated by the plurality of data handlers." *Id.* at 18:15–18, 21–24. We apply a presumption that "operating . . .

independently" in claim 16 has the same meaning as "operated independently" in claim 1. *See PODS, Inc. v. Porta Stor, Inc.*, 484 F.3d 1359, 1366 (Fed. Cir. 2007) ("We apply a 'presumption that the same terms appearing in different portions of the claims should be given the same meaning unless it is clear from the specification and prosecution history that the terms have different meanings at different portions of the claims.'" (quoting *Fin Control Sys. Pty., Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001))). In other words, unless usage of "operating . . . independently" in the context of the '501 patent specification indicates otherwise, we presume one of ordinary skill in the art would not interpret the claim 16 phrase "operating a plurality of data handlers independently from one another" as limited to "*using* a plurality of data handlers *to independently test* a portion of one or more memory chips" (PO Resp. 32).

The term "operating" does not appear in the '501 patent specification. The phrase "configured to be operated" appears only once in the '501 patent specification as follows: "In certain embodiments, the memory module 10 is configured to be operated in a test mode." *See* Ex. 1001, 5:64–65. In our interpretation of the similar '434 patent claim term "operable independently" in our Final Decision in IPR2014-00970, we considered the disclosure in the related '434 patent corresponding to the following '501 patent disclosure:

> *Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28 and* is operatively coupled to a corresponding plurality of the data ports of one or more of the plurality of memory devices 18. For example, each of the data handlers 30 may be operatively coupled to (e.g., logically and/or electrically coupled to) the corresponding plurality of data ports. Each data handler 30 *is further configured to generate data for writing to the corresponding plurality of data ports*.

Ex. 1001, 5:16–23.

> Because each of the data handlers 30 is operable independently of each of the other data handlers 30, the data handlers 30 are generally modular. As such, modifications in the configuration of the memory module 10 (e.g., changes in the bit-width of the memory bus, changes in the number of memory devices 20, etc.) may be less complicated to accommodate than in other types of self-testing memory modules 10. For example, where a new memory device 20 or set of memory devices 20 is added to the memory module 10, the change may be generally accommodated by adding a corresponding data handler 30. The change may be accommodated without having to implement a major reorganization of the memory module 10 or the self-testing logic of the memory module 10, for example.

Id. at 8:22–35. In our Final Decision in IPR2014-00970, we found that the above description of each data handler as "operable independently" and having the "further" feature of being "configured to generate data" (*see id.* at 5:16–23) supported Petitioner's contention that the data generation function of the data handlers is an additional feature that is separate from the feature of independent operability. We found that based on the description quoted in column 8, lines 22–35, above, coupled with the discussion of the prior art problem of lack of flexibility in memory module self-test logic to accommodate changes to data width (*see id.* at 4:41–60, 8:24–29), one of ordinary skill in the art would understand the term "operable independently" to describe the data handlers as being discrete and functioning without being physically or logically connected to each other. In the present case, we find similarly that the above-quoted language from the '501 patent specification is consistent with the plain meaning of the language in claim 1, i.e., that each of the plurality of data handlers is configured to be operated independently, but only some of the data handlers (i.e., "one or more") are further

configured to generate data used for testing. We agree with Petitioner, therefore, that when interpreted in the context of the '501 patent in its entirety, the claim term "operated independently" "merely means that each data handler can operate without influence or control by any of the other data handlers." Reply 3. We find no basis in the '501 patent specification for applying a different construction to the claim 16 language "operating . . . independently." Accordingly, we interpret "operated independently"/"operating . . . independently" in accordance with its plain and ordinary meaning: "the operation of a data handler is not influenced or controlled by another data handler" (Reply 4).

B. Configured to, and Generate

Independent claim 1 recites "a plurality of data handlers . . . *configured to generate* data for writing to a corresponding one or more memory chips" and "a control circuit *configured to generate* address and control signals." Ex. 1001, 16:42–48. Independent claim 16 recites "operating a plurality of data handlers independently from one another to *generate* and transmit data" and "operating a control circuit to *generate* address and control signals." *Id.* at 18:15–16, 19–20 (emphasis added).

1. Configured to

Prior to institution, neither party requested, nor did we deem necessary, construction of the term "configured to." In its Response, Patent Owner now requests that we construe the term "configured to" in the context of the claim phrase "configured to generate" (claim 1). *See* PO Resp. 14. As correctly observed by Petitioner, however, the term "configured to" is not used exclusively in conjunction with the term "generate" in claim 1, but is also used with the claim terms "test," "receive," "write," "calculate,"

"store," "verify," "be operatively coupled," "be operated independently" and "selectively input." *See* Reply 4. The term "configured to" is also used in the '501 patent specification in conjunction with the terms "provide" (Ex. 1001, 6:6, 33), "operatively couple" (*id.* at 7:26), "read" (*id.* at 9–10), "receive" (*id.* at 11:11–12), "check" (*id.* at 11:14), "perform" (*id.* at 11:20–21), "report" (*id.* at 12:25), and "input" (*id.* at 14:5, 8). Presumptively, "configured to" should carry the same meaning, and "configured to generate," "configured to test," "configured to write," etc. should have parallel meanings, differing only insofar as "test," "write," "generate," etc., differ. *See Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1337 (Fed. Cir. 2008) ("'[B]inary code' and 'trinary code' should have parallel meanings, differing only insofar as 'binary' and 'trinary' differ in their relationships to the numbers 2 and 3.").

Patent Owner does not offer an interpretation of the term "configured to" outside the context of the phrase "configured to generate" (*see* PO Resp. 14–19), but contends "'configured to generate' means 'programmed to generate' and enables the subsequent execution of a self-testing function (*e.g.*, data generation, writing and verification)" (*id.* at 18; *see also id.* at 15 ("'Programmed' is therefore synonymous with 'configured.'")).

Petitioner contends the claim term "configured to" should be construed consistently, whether used in conjunction with "generate" or with another function recited in the claims, and should be given its plain and ordinary meaning of "designed to, adapted to, or arranged to." Reply 4. In addition to relying on the testimony of its expert, Dr. Alpert, Petitioner cites two dictionary definitions in support of its proposed interpretation. Reply 5 (citing Ex. 1011, 186; Ex. 1012, 428).

Dr. Alpert, testified that, in the '501 patent, "'program' is one example of 'configure,' but not the only example." Ex. 1009 ¶ 16. Dr. Alpert further testified "the '501 patent discloses that *configuring* can be accomplished in a wide variety of ways . . . , including those that do not require programming, for example using predefined values." *See id.* ¶ 19 (quoting Ex. 1001, 6:19–22 ("The address sequences and/or the data patterns of certain embodiments may be programmable either through the I^2C interface or they may be defaulted to pre-defined values."); Ex. 1001, 10:67–11:4 ("[R]andom or pseudorandom data may be generated and written to the corresponding plurality of data ports. For example, a linear feedback shift register (LFSR) may be used in some embodiments. In addition, the data patterns may be programmable."); *see also id.* at ¶ 20 ("The configuration of the data handlers can be fixed, hardwired." (citing Ex. 1001, Figure 2, 8:5–19, 36–55)); Ex. 2021, 135:12–136:2 (wherein Dr. Alpert testified that a linear feedback shift register would not need to be programmed to generate data, but could be arranged or designed to generate data). In his second declaration, Dr. Alpert also testified that:

> The '501 patent uses "configured" to describe hardwired arrangements of components that cannot be programmed for their configuration. Additionally, the '501 patent discloses various components included in the control module, which do not all require programming: . . . . The configuration of the verification circuitry can be fixed without any memory structure for storing a copy of the generated data, as disclosed at 11:28–31. . . . [And,] control module 22 [can] include[] discrete logic [or] one or more application-specific integrated circuit (ASICs) . . . [b]oth . . . could be programmable or nonprogrammable as would have been understood by a person of ordinary skill.

Ex. 1009 ¶ 20 (emphasis omitted).

Patent Owner's expert, Dr. Sechen, testified that "the most

conventional use of *configuration* refers to hardware programming" (Ex. 1010, 68:25–69:2 (emphasis added)), but that it could refer to software programming as well. *Id.* at 55:17–18. In his declaration, Dr. Sechen did not testify as to the meaning of "configured to" in conjunction with any term other than "generate." *See* Ex. 2012 ¶¶ 46–67. In response to questioning during cross-examination, however, Dr. Sechen testified that "configured to," as used in the context of the phrase "a printed circuit board configured to be operatively coupled to a memory controller of a computer system" (Ex. 1001, 2:25–27), "might mean designed [to]" because the printed circuit board has to be configured "such that it fits into the slot on the motherboard and is able to communicate successfully with the memory controller." Ex. 1010, 84:14–19. The '501 patent discloses that components of control module 22 and data module 28 may include discrete logic and application specific integrated circuits (ASICs) (*see* Ex. 1001, 9:62–64, 12:33–37), which, on cross-examination, Dr. Sechen conceded can be designed to operate without the need for hardware programming. Ex. 1010, 58:9–61:22.

Based on our analysis of the '501 patent claims and specification, and relying on the testimony of Drs. Alpert and Sechen regarding the technology,[3] we find the '501 patent uses the term "configured to" to describe components that can be programmed by a controller to perform a function, as well as components that can be hard-wired to perform a function

[3] "Although the patent file may often be sufficient to permit the judge to interpret the technical aspects of the patent properly, consultation of extrinsic evidence is particularly appropriate to ensure that his or her understanding of the technical aspects of the patent is not entirely at variance with the understanding of one skilled in the art." *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1309 (Fed. Cir. 1999).

and do not require programming. *See, e.g.*, Ex. 1001, 7:25–31 ("PCB 12 may include at least one connector (not shown) configured to operatively couple the memory module 10 to the memory controller 14 of the computer system 16. . . . For example, the memory module is electrically coupled, logically coupled, or both, with the memory controller 14"); *id.* at 8:50–53 ("[T]he data handlers 30 may be operatively coupled (e.g., electrically and/or logically coupled or connected) to the eight data ports 21 of one of the corresponding memory devices 20"). We do not agree with Patent Owner, therefore, that the broadest reasonable interpretation of "configured to" is "programmable to." *Cf.* Ex. 1010, 89:3–5 ("'Designed' implies a certain hardwiredness, that that's what it does, and 'configured' implies that maybe it only does that some of the time."). Rather, we agree with Petitioner that one of ordinary skill in the art would interpret the claim term "configured to" in accordance with its plain and ordinary meaning, and would understand that this term encompasses components both programmable and hard-wired to perform the functions described in the '501 patent. Accordingly, we interpret the term "configured to" as "designed, adapted, or arranged to."

2. Generate

In addition to reciting "a plurality of data handlers . . . configured to generate data" and "a control circuit configured to generate address and control signals," claim 1 recites: "wherein the memory system is configured to test the one or more memory chips using the address and control signals *generated by* the control circuit and using the data *generated by* the one or more data handlers" (Ex. 1001, 16:48–51 (emphasis added)). Similarly, in addition to reciting "operating a plurality of data handlers independently

from one another to *generate* and transmit data" and "operating a control circuit to *generate* address and control signals," claim 16 recites a step of : "testing the one or more memory locations of the one or more memory chips using the address and control signals *generated by* the control circuit and using the data *generated by* the plurality of data handlers" (*id.* at 18:21–24 (emphasis added)).

For purposes of our Institution Decision, we interpreted the claim term "generate" as meaning "produce" or "cause." *See* Dec. on Inst. 8–9. Our interpretation was based on findings that the plain and ordinary meaning of "generate," as evidenced by Merriam-Webster's Collegiate Dictionary, is "produce" or "be the cause of" (*id.* at 9 (citing Ex. 2002, 484)), and that interpreting "generate" to mean "cause" was not inconsistent with the '501 patent specification, which broadly states that data can be generated by the data handlers in a variety of ways (*see id.* at 8–9 (citing Ex. 1001, 10:53–54)).

Petitioner contends the Board should maintain its construction of "generate" as "produce" or "cause," because this construction "reflects the plain and ordinary meaning." Reply 8–9. Petitioner maintains one of ordinary skill in the art "would appreciate that when substituted in the claims, the Board's construction is 'produce or cause production of [data/address and control signals].'" *Id.* at 8 n.2 (citing Ex. 1009 ¶ 29). During cross-examination, Dr. Alpert explained the difference between producing and causing to produce" as follows: "[P]roducing would actually be either creating or providing, in this case, some data and causing to produce would be having one device be the cause of or invoking another device to produce the data." Ex. 2013, 43:5–11. Dr. Alpert testified that one

of ordinary skill in the art would understand the description of the data handler being logically coupled to the memory devices at column 5, lines 20–23 of the '501 patent as implying intermediary logical devices between the data handler and the memory device ports. *See id.* at 39:1–16. In other words, one of ordinary skill in the art would understand that the "physical system element" that produces the data used for testing in claim 1 "can be the data handler or it can be another device that the data handler causes to produce the data." *Id.* at 32:4–6. During cross examination, Dr. Alpert identified "a buffer or a multiplex[e]r" as examples of devices that could "exist between the data handler and the memory device" to produce the data used for testing. *Id.* at 36:13–16. Dr. Alpert explained that a

> buffer can take an input, information input and it can either produce a signal that contains that information or the complements of that information, or there could be several buffers that have potential to be in a third state, so-called tri-state buffers, such that the buffers can be used to select information that may be presented, that would be data that would be produced that would then be presented down to other circuits.

Id. at 36:24–37:8.

Patent Owner contends "'generate' is properly construed [only] as 'produce.'" PO Resp. 31 (citing Ex. 2012 ¶¶ 68–96); *see also id.* at 20 (quoting Ex. 2012 ¶ 70 ("In the context of integrated circuit and printed circuit board design, *generate* or *produce* (which are synonyms in this context) are terms of art.")). Patent Owner argues that interpreting "generate" as "cause," or as "cause to produce," as suggested by Petitioner, would render other claim language superfluous. *See id.* at 24–31. Specifically, Patent Owner contends that interpreting "generate" as "cause to

produce" renders meaningless the claim limitations "the memory system is configured to test" (claim 1) and "testing" (claim 16) the memory chips "using the address and control signals generated by the control circuit and using the data generated by the . . . data handlers" (claim 1 and 16). *See id.* at 29–31; *see also id.* at 25 ("[T]he situation posited by the Board does not reflect that the data written by the data handler was 'generated by the data handler'" and eliminates the claim requirements that data generated by the data handlers is used for testing.

"[W]here there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meaning." *Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 2003). The '501 patent claims and specification use the term "generate" in conjunction with the memory module, control circuit/module, data module, and components thereof. The '501 patent further uses the term "generate" as a specific example of "produce," with the term "produce" appearing only once in the '501 patent:

> In some embodiments, the control module 22 and the data module 28 *produce* memory addresses, control and/or data signals according to the JEDEC standard memory protocol. In some embodiments, *for example*, the control module 22 and the data module 28 *generate* the memory interface signals with proper edge relationships based on the JEDEC standard.

Ex. 1001, 6:11–17 (emphasis added).

The '501 patent specification uses both the term "provide" and the term "generate" in describing the operation of data module 28:

> [D]uring testing, the control module 22 generates address and control signals 24 associated with memory locations to be tested and the *data module 28 generates corresponding test data patterns and provides them* to the appropriate memory

> devices 20. For example, the data module 28 may receive a write command from the control module 22 and provide data to be written to certain locations in the memory devices 20 during a write operation.

Id. at 5:48–55 (emphasis added). The term "provide" is also used separately from, but in a similar manner to, the term "generate" to describe embodiments of control module 22 and data module 28 used for testing memory devices 18. *Compare id.* at 6:5–11 ("The data module 28 and/or the control module 22 of certain embodiments are configured to test the plurality of memory devices 18 at the normal operating speed of the memory devices 20. For example, the data module 28 and/or the control module 22 are *configured to provide* memory signals (e.g., data, address and control signals) according the operating specification of the memory devices 20" (emphasis added)) *with id.* at 9:29–31 ("The control module 22 can be *configured to generate* address and control signals 24 for testing the plurality of memory devices 18." (emphasis added)) *and id.* at 10:31–37 ("Each of the data handlers 30 of certain embodiments further includes a data handler logic element 46. The data handler logic element 46 of certain embodiments comprises a data generation element 54 and a verification element 56. The data generation element 54 may be *configured to generate* data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports." (emphasis added)).

In addition to using the term "provide" to describe embodiments of control module 22 and data module 28, the '501 patent specification uses this term to describe the operation of switch 44: "The switch 44 may *provide* a bi-directional data multiplexer function" and is "configured to selectively input" data signals 48 from system memory controller 14 or data

signals 50 from data handler logic element 46. *Id.* at 10:10–15 (emphasis added). The '501 patent specification discloses that switch 44 may positioned between data module 28 and memory devices 18 (*see id.* at 10:28–30), i.e., one of the hypothetical arrangements described by Dr. Alpert in which a data handler would cause an intermediary device (e.g., a multiplexer) to produce data. The '501 patent specification does not use the term generate (or produce), however, to describe the configuration or operation of switch 44. The '501 patent specification also describes an embodiment in which switch 44 is included in each of data handlers 30 (*id.* at 10:7–8), as well as an embodiment in which the function of selective inputting of data signals to memory devices 18 is not limited explicitly to a switch (*see, e.g., id.* at 6:1–4 ("[E]ach of the data handlers 30 write[s] the data generated by the data handler 30 to the corresponding plurality of data ports by selectively inputting data signals to the data ports of the plurality of memory devices 18.")).

The above-noted usages of the terms "provide" and "generate" to describe different embodiments of control module 22 and data module 28, and to describe different functions of the data handlers, do not support Dr. Alpert's opinion that the term "generate" is properly interpreted as encompassing the selection function of a multiplexer.[4] Use of the term

[4] Dr. Alpert's testimony, though consistent with Averbuj's use of the term "generate" (*see* Ex. 1003 ¶ 56 ("[D]ata generation unit 44 generates the transformed data signal 49 (BIST_DATA_T) to fill the memory module 12 with the data dictated from the sequencer 8 without modification.")), cannot be relied on to construe this claim term in a manner that varies from the implicit definition in the '501 patent. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584–85 (Fed. Cir. 1996) ([P]rior art can often help to demonstrate how a disputed term is used by those skilled in the art. . . .

"generate" to describe an embodiment in which the control module and data handlers "produce" memory addresses, control and/or data signals, however, does support Dr. Sechen's opinion that "generate" and "produce" are synonymous.

In the absence of evidence to the contrary, there is a presumption that different claim terms have different meanings. *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000); *see also SEB S.A. v. Montgomery Ward & Co., Inc.*, 594 F.3d 1360, 1369 (Fed. Cir. 2010) (noting there is a presumption that meanings of claim terms do not overlap); *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

The claim 1 recitation of "data handlers . . . configured to generate data for writing" and dependent claim 14 recitation of "the one or more circuits [sic, data handlers] . . . *further configured* to write data to the one or more memory chips by selectively inputting," as well as the above disclosure in the '501 patent specification, create a presumption that "generate" has a different meaning than "write" and/or "selectively input." *See also* claim 1 ("a control circuit configured to generate address and control signals") and dependent claim 15 ("the control circuit is *further configured* to selectively input to the address and control ports of the one or more memory chips either the address and control signals from the memory

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[H]owever, reliance on such evidence is unnecessary, and indeed improper, when the disputed terms can be understood from a careful reading of the public record. Nor may it be used to vary claim terms from how they are defined, even implicitly, in the specification or file history." (internal citation omitted)).

controller of the computer system or the address and control signals from the control circuit." (emphasis added)). Likewise, the recitations of "operating a plurality of data handlers . . . to generate and transmit data" in independent claim 1, and "data transmitted to the one or more . . . memory chips" in dependent claims 17 and 20, create a presumption that "generate" has a different meaning than "transmit." In other words, the '501 patent specification and claims do not support an interpretation of "data generated" by a component as encompassing data selected, written, input, or transmitted by a first component to a second component, because such interpretation would result in an overlap in the meaning of "generate" and "write" and/or "selectively input" and/or "transmit."

Having considered the ordinary meaning of the term "generate" in the context of both the claims and the '501 patent as a whole, we agree with Patent Owner that the broadest reasonable interpretation of the claim term "generate" is "produce," and that "generate" does not mean "cause" or "cause to produce." We interpret the claim language "address and control signals *generated* by the control circuit" and "data *generated* by the . . . data handlers" (claims 1 and 16), as encompassing signals and data that originated in the control circuit and data handlers, including by transformation or modification of information and/or data received from another component. *See e.g.* Ex. 1001, 10:37–41 ("The data signals and/or patterns of data signals may be *based on* information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." (emphasis added)); *id.* at 10:61–63 ("The data may be generated *based [on]* previously written data (e.g., inverting each of the bits of a previously written data word)" (emphasis added)). We do not

interpret this language as encompassing signals and data received by the control circuit and data handlers from another component, and merely provided, propagated, sent, or input to memory devices, without transformation or modification by the control circuit and data handlers. *Compare, e.g.*, Ex. 1001, 9:54–57 ("In one embodiment, the memory device controller 34 *generates* the address and control signals for memory device (e.g., DRAM device) operations." (emphasis added)), *with id.* at 9:40–53 ("In one embodiment, the memory device controller 34 *receives* signals 38 (e.g., address and control signals) from the system memory controller 14 and signals 42 (e.g., address and controls signals) . . . [M]emory device controller 34 *may send* either the signals 38 from the system memory controller 14 or, alternatively, the signals 42 from the test controller 36, to the register 40." (emphasis added)).

Thus, in summary, we construe "operated independently/operating independently," "generate," and "configured to" as follows:

Claim Term/Phrase	**Interpretation**
Operated independently/ Operating . . . independently	Operated, or operating, without influence or control by another
Generate	produce
Configured to	designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]

IV. ANALYSIS

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance

of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged or combined in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

> A single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. Thus, a prior art reference without express reference to a claim limitation may nonetheless anticipate by inherency. "Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claims limitations, it anticipates."

Perricone v. Medicis Pharm. Corp., 432 F.3d 1368, 1375–76 (Fed. Cir. 2005) (citations omitted). "In general, a limitation or the entire invention is inherent and in the public domain if it is the 'natural result flowing from' the explicit disclosure of the prior art." *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3)

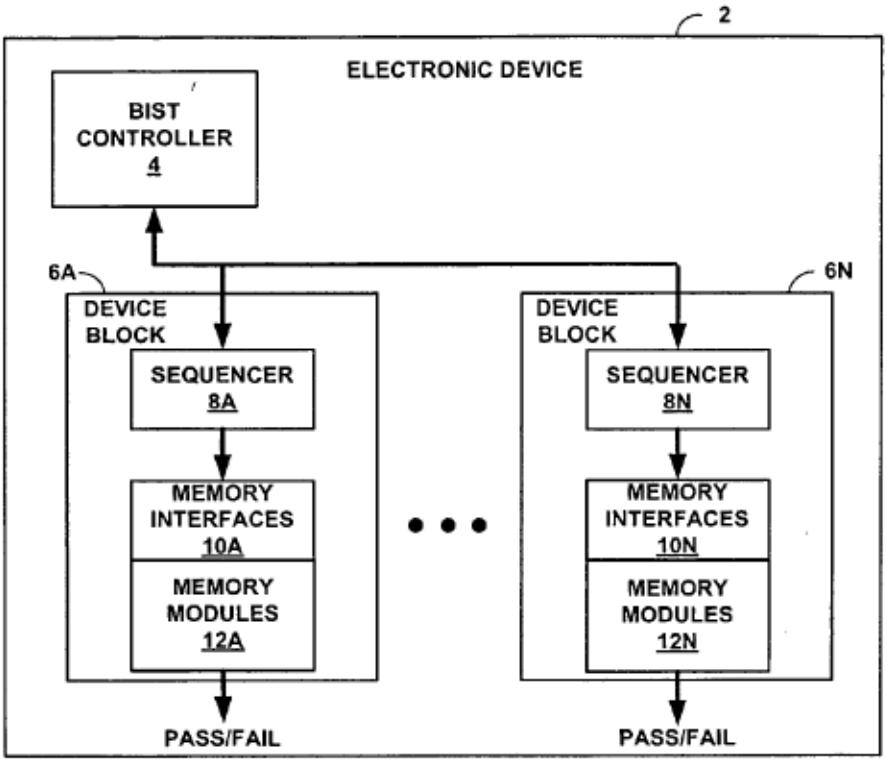
the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham*, 383 U.S. at 17–18. An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

A. Alleged unpatentability of claims 1–3, 5–8, and 11–20 under §102(b) based on Averbuj

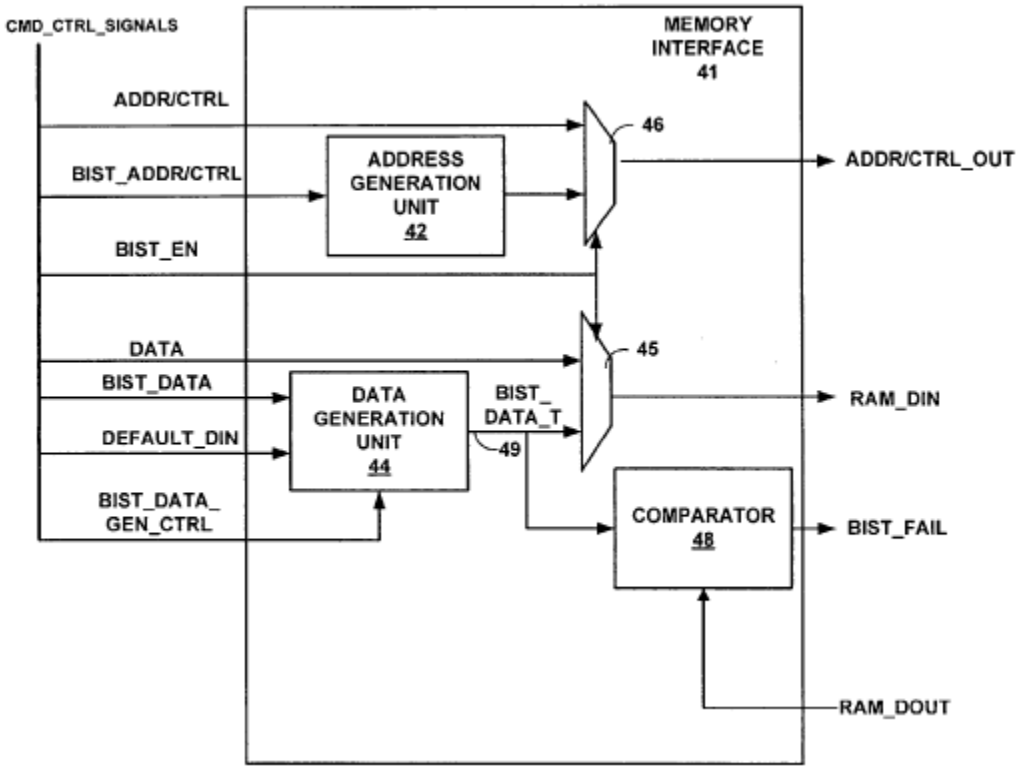
1. Averbuj (Ex. 1003)

Averbuj describes a hierarchical built-in self-test (BIST) architecture wherein a BIST controller provides centralized, high level control of the testing of one or more memory modules. Ex. 1003 ¶¶ 7–8. Figure 1 of Averbuj is reproduced below.



Averbuj Figure 1, above, "is a block diagram illustrating an example electronic device 2 . . . includ[ing] a built-in self-test (BIST) controller 4 that provides centralized, high-level control over testing of device blocks 6A through 6N (collectively 'device blocks 6')." *Id.* ¶ 28. "Each of device blocks 6 includes a sequencer 8, and a set of one or more memory interfaces 10 and one or more respective memory modules 12." *Id.* BIST controller 4 provides and communicates test algorithms as a set of commands to sequencers 8 for application to device blocks 6. *Id.* ¶ 29. Sequencers 8, in turn, issue command control signals (CMD_CTRL_SIGNALS) to receiving memory interfaces 10. *Id.* ¶ 43.

Exemplary memory interface 41 is shown in Figure 6, below. *Id.* ¶ 23.

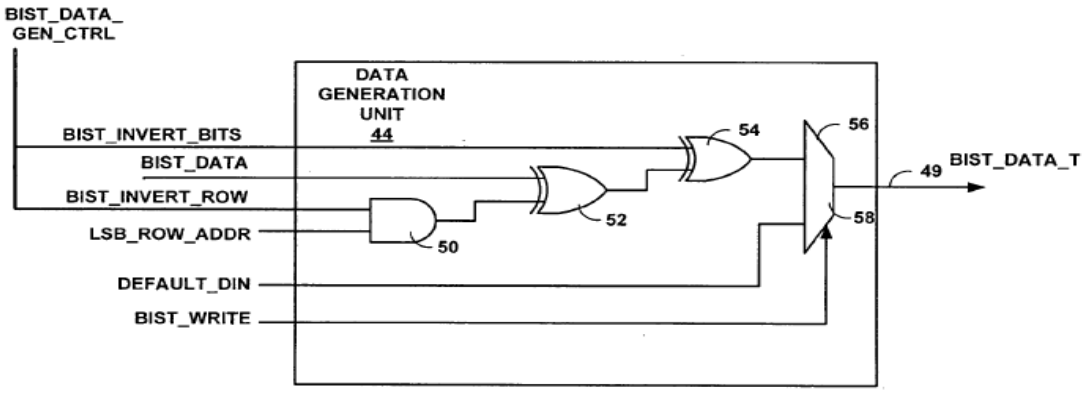


As shown in the Figure 6 embodiment, above, memory interface 41 includes a layer of multiplexers 45, 46. *Id.* ¶ 48. "[U]nder normal operating conditions, BIST enable (BIST_EN) is de-asserted, causing multiplexers 45, 46 to select the address/control signals (ADDR/CTRL) and data signals (DATA), e.g., as provided by a programmable processor." *Id.* "When electronic device 2 is operating in BIST mode, however, the BIST enable signal causes multiplexers 45, 46 to select the BIST address/control signals (BIST_ADDR/CTRL) and the test data provided by a respective higher-level sequencer [, e.g., sequencer 8A]." *Id.*

"[M]emory interface 41 processes the sequential memory operations issued by [] higher-level sequencer [8A], and transforms the data and addresses provided by the sequencer as needed based on the particular physical characteristics of the memory module" (*id.* ¶ 54) using address generation unit 42 and data generation unit 44 (*id.* ¶¶ 49, 51). "For example,

sequencer 8 may request a checkerboard bit pattern that requires columns of data within the memory module to alternate between ones and zeros. Different memory modules 12, however, may be arranged with different row and column configurations." *Id.* ¶ 50. In this case, address generation unit 42 transforms the address provided by sequencer 8 to correspond to the physical configuration of the specified memory module before the address is applied to that memory module. *See id.* ¶¶ 51–52.

An example embodiment of data generation unit 44 is illustrated in Figure 7, reproduced below.



As shown in Figure 7, above, "data generation unit 44 receives a BIST_DATA signal, a default data signal (DEFAULT_DIN) provided by the sequencer 8[, and] . . . a number of control signals in the form of BIST_INVERT_BITS, BIST_INVERT_ROWS, LSB_ROW_ADDR, and BIST_WRITE." *Id.* ¶ 55.

> [S]equencer 8 asserts and deasserts the invert bits signal (BIST_INVERT_ BITS), the invert rows signal (BIST_INVERT_ROWS), and the invert columns signal (not shown) to specify data patterns, such as solid, checkerboard, horizontal and vertical striped data patterns. If neither the invert bits nor the invert rows signals are asserted, then the BIST_DATA signal passes through XOR gates 52, 54 without

> modification. As a result, data generation unit 44 generates the transformed data signal 49, (BIST _DATA_ T) to fill the memory module 12 with the data dictated from the sequencer 8 without modification.

Id. ¶ 56. By contrast, when the BIST_INVERT_BITS signal is asserted, data generation unit 44 automatically inverts the values dictated by the sequencer. *Id.* ¶ 57.

2. Analysis

Petitioner contends the claim 1 limitations (and corresponding claim 16 limitations) of "a control circuit configured generate address and control signals," "data handlers [] configured to generate data," and a "memory system [] configured to test [] one or memory chips" using these generated signals and data are met by Averbuj's sequencers 8 and memory interfaces 10 that generate address/control signals and data, respectively, for testing memory modules 12. Pet. 12. Patent Owner argues: (1) Averbuj's memory interfaces (the alleged data handlers) are not "configured to generate data," as recited in claim 1; (2) Averbuj's sequencer 8 (the alleged control circuit) is not "configured to generate" (claim 1), and does not "generate" (claim 16) the address and control signals used for testing the memory modules 12 (the alleged memory chips); (3) Averbuj's memory interfaces 10 (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot be "operating . . . independently" (claim 16); and (4) Averbuj's sequencer (the alleged control circuit) is not "configured to selectively input" address and control signals to the memory chips, as recited in dependent claim 15. *See* PO Resp. 32–41. With the exception of the above-noted limitation in dependent claim 15, Patent Owner does not dispute directly Petitioner's contentions with respect to the additional limitations

recited in dependent claims 2, 3, 5–8, 11–15, and 17–34, but contends these claims are not anticipated by Averbuj because Petitioner has failed to show Averbuj anticipates independent claims 1 and 16. *See id.* at 41.

a. "one or more data handlers . . . configured to generate data" (claim 1) for testing memory chips

Petitioner relies on paragraphs 43, 48, and 49 of Averbuj in support of its contention that Averbuj's memory interfaces are data handlers that are configured to generate data for testing via data generation unit 44, described as "generat[ing] the exact data (RAM_DIN) applied to the memory inputs" of a memory module during testing. Pet. 15–16 (quoting Ex. 1003 ¶ 49).

Patent Owner argues Petitioner has not shown that Averbuj's memory interfaces 10 (the alleged data handlers) are "configured to generate data" (claim 1) for testing memory modules 12 (the alleged memory chips), because "Petitioner has not shown that the data generation unit 44 in Averbuj is capable of being programmed." PO Resp. 34 ("Averbuj's control signals for data generation (BIST_DATA_GEN_CTRL) are not programmed – they are used to actively generate BIST_DATA_T. Without constant communication over the BIST_DATA_GEN_CTRL lines, BIST_DATA_T is not generated."). Patent Owner's argument is based on its interpretation of "configured to" as "programmed to." *Id.* at 33.

In Section III.B.1, we determined the broadest reasonable interpretation of "configured to," as used in the '501 patent claims, is "designed, adapted, or arranged to," and that one of ordinary skill in the art would understand that programmability is only one way that a component might be designed, adapted, or arranged to perform a function. In other words, lack of programmability is not determinative of whether data generation unit 44 is "configured to generate" data. We are persuaded

Petitioner has shown, by a preponderance of the evidence, that Averbuj's data generation unit 44 is capable of generating data for testing memory modules 12 and, therefore, is necessarily designed, adapted, or arranged to generate data in the manner recited in challenged claim 1.

b. "a control circuit configured to generate address and control signals"(claim 1)/"operating a control circuit to generate address and control signals" (claim 16) for testing memory chips

Patent Owner argues Averbuj's sequencer 8 (the alleged control circuit) does not generate (i.e., produce) the address and control signals used to test memory modules 12 (the alleged memory chips) and, therefore, does not describe "a control circuit configured to generate address and control signals" or "operating a control circuit to generate address and control signals" (claim 16) for testing memory chips as recited in the challenged claim. PO Resp. 35. Patent Owner argues, more specifically, that in Averbuj, the address and control signals used to test memory modules 12 are produced by memory interfaces 10 (the alleged data handlers), not by sequencer 8 (the alleged control circuit). *See id.*

Petitioner references Averbuj paragraphs 37, 43, 48–53, 59–61, and 77–78 in support of its contention that Averbuj discloses a control circuit (sequencer 8) configured to generate address and control signals (CMD_CTRL_SIGNALS) used for testing memory chips (memory modules 12). Pet. 16–17. Petitioner contends "[t]he actual addressing information is produced by the [s]equencer, and the address generation unit 42 merely applies the received addressing information to a given physical memory configuration (*i.e.*, row/column configuration)." Reply 12–13; *see also* Tr. 20:15–18 ("Averbuj teaches us a sequencer generates addresses, provides

them to the memory interface, which may pass them through or may translate them. . . . It generates address and control signals.").

Averbuj discloses that "BIST controller 4 provides and communicates test algorithms to sequencers 8 for application to device blocks 6" (Ex. 1003 ¶ 29), and "[s]equencers 8 interpret" and "control the application of the test algorithms" to the memory modules (*id.* ¶ 30). *See also id.* ¶ 46 ("Sequencers 8 receive the generic BIST commands in accordance with the command protocol, and control the application of the commands by generating and issuing sequences of one or more memory operations for application to a set of respective memory modules 12."). For example, in the exemplary embodiment illustrated in Figure 5, command parser 30 of sequencer 8A processes a command received from BIST controller 4, and extracts one or more parameters from the command. *Id.* ¶¶ 41–42. Command parser 30 passes the extracted parameters to command controller 34, which then issues a sequence of one or more operations to each memory interface 10. *Id.* ¶¶ 42–43.

> In particular, . . . command controller[] 34 sequentially drives the appropriate command control signals (CMD_CTRL_SIGNALS) to carry out each operation of the sequence. The command control signals may include signals to provide a memory address and data to the receiving memory interfaces 10 and to direct the receiving memory interfaces to invert bits, perform read or write operations, invert rows, and the like.

Id. ¶ 43. "Memory interfaces 10 handle specific interface requirements for each of memory modules 12. For example, each of memory interfaces 10 may be designed in accordance with the particular signal interface requirements and physical characteristics of the respective one of memory modules 12." *Id.* ¶ 31.

Averbuj further explains, in connection with the embodiment illustrated in Figure 6, that memory interface 41 "*transforms* the data and addresses provided by the sequencer *as needed* based on the particular physical characteristics of the memory module" (*id.* ¶ 54 (emphasis added)) using address generation unit 42 and data generation unit 44 (*id.* ¶¶ 49, 51). For example, if sequencer 8 asserts an invert rows signal and/or invert columns signal to specify a data pattern, data generation unit 44 inverts values dictated by the sequencer to generate transformed data signal 49 (BIST_DATA_T). *Id.* ¶ 57. If, however, none of the invert signals are asserted, then the BIST_DATA signal passes through XOR gates 52, 54 of data generation unit 44 without modification, and the BIST_DATA_T signal sent to memory module 12 is "the data dictated from the sequencer 8 *without modification*." *Id.* ¶ 56 (emphasis added). Likewise, "in some BIST tests," sequencer 8 may direct memory interface 41 to write BIST data in a row or column first fashion. *Id.* ¶ 51. In such case, address generation unit 42 must transform the address provided by sequencer 8 to conform to the particular row and column configuration of the memory module. *See id.* ¶¶ 51–52. "For example, a 256 bit memory module 12 may be organized as 128 rows and 2 columns, 32 rows by 8 columns, 16 rows by 16 columns, and the like." *Id.* ¶ 50.

Based on the above description in Averbuj, we agree with Patent Owner that Averbuj describes memory interfaces (the alleged data handlers) that are configured to produce address and control signals, and that Averbuj describes producing address and control signals in certain circumstances, e.g., when Averbuj's sequencer (the alleged control circuit) specifies writing data in a particular pattern that requires transformation to conform to a

particular configuration of a memory module. *See* PO Resp. 35. We also agree with Petitioner, however, that Averbuj's memory interfaces are further configured to apply to the memory modules the same address and control signals received from, and produced by, the sequencers for testing (*see* Reply 12–13), e.g., when the sequencer sends signals that can be applied, without modification or transformation (*see* Ex. 1003 ¶ 56), directly to a memory module irrespective of its physical configuration. Thus, Petitioner has shown, by a preponderance of the evidence, that Averbuj's sequencer meets the claim 1 limitation of "a control circuit configured to generate address and control signals" for testing memory chips, and that Averbuj describes "operating a control circuit [(i.e., a sequencer)] to generate address and control signals" used in testing memory chips as recited in claim 16 of the '501 patent.

c. "a plurality of data handlers configured to be operated independently from one [an]other" (claim 1)/ "operating a plurality of data handlers independently from one another" (claim 16)

Petitioner contends Averbuj describes each memory interface 10A–C (the alleged data handlers) of Figure 6 as receiving control and address data from sequencer 8 and using this information to generate address and test data that is specific to its particular memory module 12. Pet. 11. Petitioner argues each memory interface operates independently from the other memory interfaces, because it "processes the sequential memory operations issued by the higher-level sequencer, and transforms the data and addresses provided by the sequencer as needed based on the particular physical characteristics of the memory module." *Id.* (citing Ex. 1003 ¶ 54). In other words, each memory interface operates without being influenced or

controlled by another memory interface because "[a] given memory interface (*i.e.*, data handler) does not communicate with any of the other memory interfaces, or with any of the memory ports used by the other memory interfaces." Reply 13 (citing Ex. 1003 ¶ 39).

Patent Owner argues Averbuj's memory interfaces (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot "operat[e] . . . independently" (claim 16) as recited in the challenged claims because they "are controlled by the same command control signals generated by the invoked command controller via a shared control line. Thus, as shown in Averbuj Fig. 4, the alleged plurality of data handlers cannot be controlled independently." PO Resp. 38. In Section III.A., however, we determined the broadest reasonable interpretation of "operated independently" and "operating . . . independently" as recited in claim 1 and claim 16, respectively, is "operated, or operating, without influence or control by another."

We find Petitioner has shown, by a preponderance of the evidence that Averbuj's memory interfaces (the alleged data handlers) are "configured to be operated" (claim 1) and can perform the function of "operating" (claim 16) without influence or control by another data handler for the reasons stated in the Petition and above. Patent Owner's argument is based on an overly narrow interpretation of "operated independently"/"operating . . . independently" as meaning that the data handlers are configured to be used, or are used "*to independently test* a portion of one or more memory chips" (*id.* at 38), and, therefore, does not persuade us that Petitioner failed to meet its burden of proof.

d. dependent claims 2, 3, 5–8, 11–15, and 17–20

Claim 15 depends from claim 1 and recites: "wherein the control circuit is further configured to selectively input to the address and control ports of the one or more memory chips either the address and control signals from the memory controller of the computer system or the address and control signals from the control circuit." Ex. 1001, 18:5–10. Petitioner contends Averbuj's multiplexer 46 meets these limitations. Pet. 24–25.

Patent Owner argues Averbuj's sequencer 8 (the alleged control circuit) does not selectively input the BIST_ADDR/CTRL signal to memory modules 12 (the alleged memory chips). PO Resp. 40. Rather, sequencer 8 inputs the BIST_ADDR/CTRL signal to address generation unit 42, which is part of memory interface 41 (the alleged data handler), and thereafter to multiplexer 46, i.e., the alleged device that selectively inputs the address and control signals to memory modules 12. *Id.*

Averbuj describes sequencer 8 (the alleged control circuit) as providing a BIST enable signal that causes multiplexer 46 of memory interface 41 (the alleged data handler) to select the BIST address/control signals provided by the sequencer. *See* Ex. 1003 ¶ 48. Averbuj states that "[i]n this manner, the sequencer controls multiplexers 45, 46 of memory interface 41 to selectively isolate the respective memory module, thereby allowing BIST algorithms to be applied to that memory module." *Id.*

We agree with Patent Owner that Petitioner has not explained adequately how Averbuj's sequencer 8 (the alleged control circuit) is "configured to" (i.e., designed, adapted, or arranged to) "selectively input . . . address and control signals" (claim 15) to memory modules 12. Petitioner has not addressed Patent Owner's argument that the device that

selectively inputs address and control signals to memory modules 12 is memory interface 41 (the alleged data handler), not sequencer 8 (the alleged control circuit). *See* Reply 14–15 (arguing "the Sequencer of Averbuj generates the address and control signals since it causes address generation unit 42 to produce the address and control signals received by the memory . . . Alternatively, the sequencer would also be understood to produce the address and control signals received by the memory," but failing to explain how Averbuj's sequencer is "configured to selectively input" (claim 15)).

Patent Owner also contends Petitioner has not met its burden to show dependent claims 2, 3, 5–8, 11–15, and 17–20 are anticipated by Averbuj, because Petitioner has failed to show independent claims 1 and 16, from which these claims depend, are anticipated. PO Resp. 41. We determined above that claims 1 and 16 are anticipated by Averbuj. With respect to claims 2, 3, 5–8, 11–14, and 17–20, we have reviewed the Petition and evidence cited therein, and determine Petitioner has met its burden to show these dependent claims are anticipated by Averbuj. *See* Pet. 17–24.

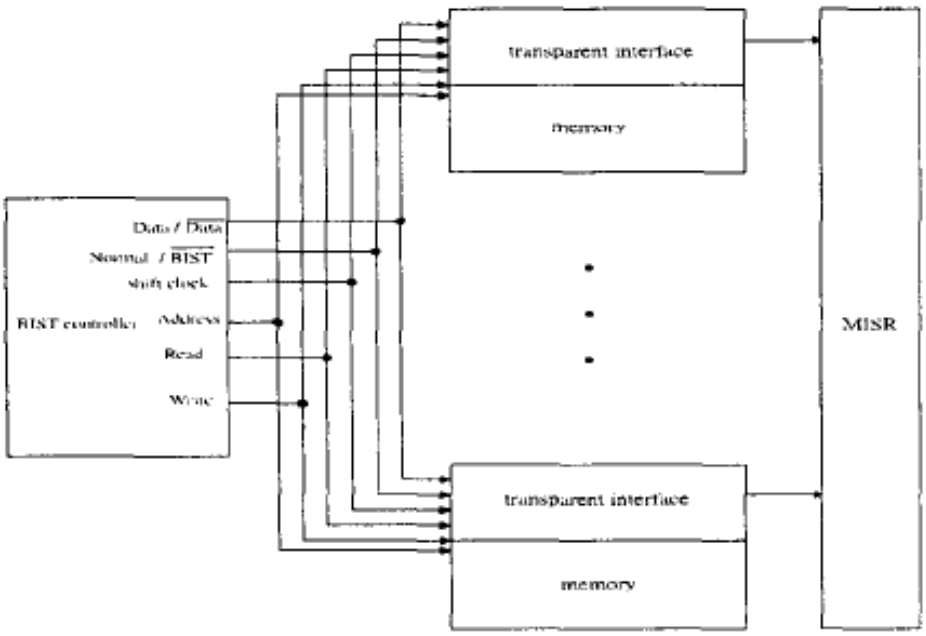
3. Conclusion

Petitioner has met its burden to show, by a preponderance of the evidence, that claims 1–3, 5–8, 11–14, and 16–20 are unpatentable under 35 U.S.C. §102(b) based on Averbuj. Patent Owner has persuaded us that Petitioner failed to meet its burden to establish unpatentability of claim 15 under 35 U.S.C. §102(b) based on Averbuj.

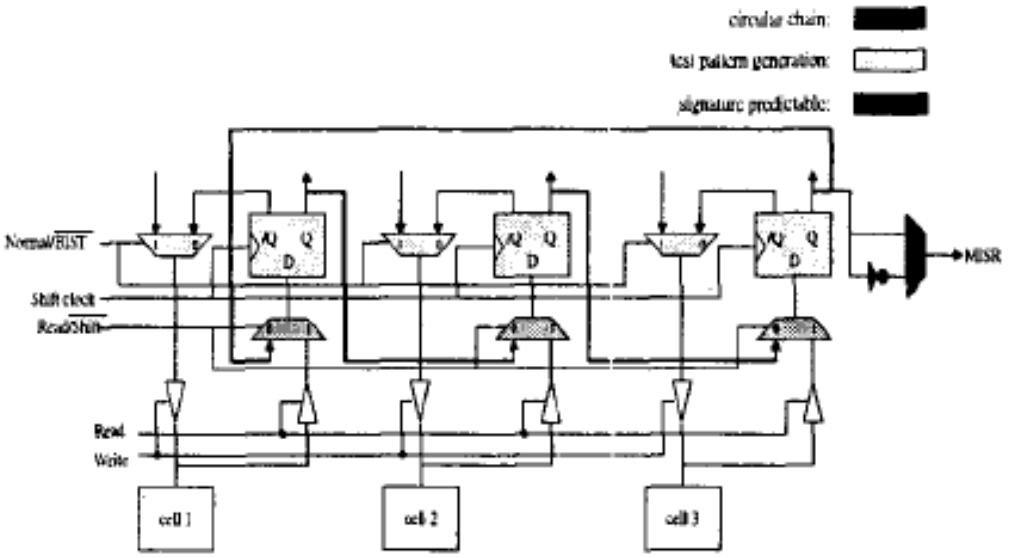
B. Alleged unpatentability of claims 1–5 and 14–16 under § 103(a) based on Huang

1. Huang (Ex. 1004)

Huang describes a transparent built-in self-test (TBIST) interface that is designed to perform testing of multiple embedded memory arrays in the normal mode. Ex. 1004, Abstract. Figure 2 of Huang is reproduced below:



As shown in Figure 2, above, Huang's transparent BIST system scheme includes a BIST controller, transparent test interface, memory arrays and a global multiple input shift register (MISR). *Id.* at 381, Fig. 2. As illustrated in Figure 2, the BIST controller generates Address, and control (Normal/BIST, shift clock, Read, and Write) signals. *Id.* "[A]ll memory modules and interface circuits receive the same test control signals from the transparent BIST controller." *Id.* at 381, col. 2. Figure 1 of Huang is reproduced below:



Huang's Figure 1, above, illustrates the test interface. The test interface "implement[s] the functions of test pattern generation and test response evaluation." *Id.* at 384, col. 2. According to Huang, "the test interface generate[s] test patterns *locally* to avoid test data routing from test controller to each memory array." *Id.* at 381, col. 1. "[T]est patterns are generated by alternatively selecting Q or /Q as an input to each memory cell . . . , so the transition of Q→ /Q and /Q→Q will be exercised in each memory cell. Thus, based on the memory content left by normal operations, new test patterns are generated by complementing each memory word several times." *Id.*

2. Analysis

Petitioner contends Huang's BIST controller, test interfaces, and memory arrays teach or suggest a control circuit, data handlers and memory chips as recited in independent claims 1 and 16. Pet. 36–38. Patent Owner argues: (1) Huang's test interfaces (the alleged data handlers) are not "configured to generate data," and Huang's BIST controller (the alleged

control circuit) is not "configured to generate address and control signals," as recited in claim 1; (2) Huang's test interfaces (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot be "operating . . . independently" (claim 16); and (3) Huang teaches away from "physically separate integrated circuit packages" as recited in dependent claim 4. PO Resp. 41–54. With the exception of the above-noted limitation in dependent claim 4, Patent Owner does not dispute directly Petitioner's contentions with respect to the additional limitations recited in dependent claims 2–5, 14, and 15, but contends these claims are not unpatentable over Huang because Petitioner has failed to show independent claim 1, from which these claims depend, would have been obvious in view of Huang. *See id.* at 54.

a. "control circuit configured to generate address and control signals" and "one or more data handlers . . . configured to generate data" (claim 1)

Petitioner contends Huang Figure 2 "illustrates the generation of address signals by the BIST controller and reception of those signals by the memory devices." Reply 17; *see* Pet. 38–39. Petitioner asserts that Huang Figure 2 also illustrates the generation of "read" and "write," i.e., control signals, by the BIST controller (the alleged control circuit), and Huang Figure 1 illustrates that these control signals are received by the memory arrays (the alleged memory chips). *Id.*; *see* Pet. 38–39. Petitioner contends Huang's transparent interfaces (the alleged data handlers) are described as generating test patterns locally, and, therefore, it logically follows that they are "designed, arranged or adapted to perform the function of data generation." Reply 16; *see* Pet. 37–38.

Patent Owner argues Huang's BIST controller and Huang's transparent interfaces and are not "configured to generate address and control signals" and "data," respectively, as recited in claim 1, because they do not receive signals that can be used for programming. PO Resp. 41–43. Patent Owner's argument is based on an overly narrow interpretation of "configured to generate" as "programmed to generate." *See id.* at 42–43. In Section III.B.1, we determined the broadest reasonable interpretation of "configured to," as used in the '501 patent claims, is "designed, adapted, or arranged to," and that one of ordinary skill in the art would understand that programmability is only one way that a component might be designed, adapted, or arranged to perform a function.

We find that Petitioner has shown, by a preponderance of the evidence, that Huang's BIST controller and transparent interfaces teach or suggest the capability of generating address/control signals and data, respectively, for testing the memory arrays, and, therefore, are designed, adapted, or arranged to generate address/control signals and data in the manner recited in challenged claim 1.

b. "a plurality of data handlers configured to be operated independently from one [an]other" (claim 1)/"operating a plurality of data handlers independently from one another" (claim 16)

Patent Owner argues Huang's transparent interfaces (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot "operat[e] . . . independently" (claim 16) as recited in the challenged claims because the transparent interfaces "are (i) specified to receive the exact control signals, and (ii) designed to continuously shift the latched content and output multiple bit streams to the MISR in parallel, and thus are

not able to be used *independently* from each of the other data handlers of the plurality of data handlers in order to *independently* test a portion of one or more memory chips." PO Resp. 43. Patent Owner's arguments are based on an interpretation of "operable independently" as requiring that each data handler is able to be used to independently test a portion of the memory space. *See generally* PO Resp. 43–52. In Section III.A., however, we determined the broadest reasonable interpretation of "operable independently" is "capable of being put into use without influence or control by another."

Petitioner argues that "[w]hen the proper construction of 'operated independently' is applied, it is apparent that each of Huang's transparent memory interfaces (*i.e.*, data handlers) meets this claim limitation, since they each correspond to an associated memory device, and locally generate test data for the associated memory device." Reply 18–19 (citing Pet. 35). Petitioner's argument is persuasive, and Patent Owner has not explained sufficiently why each of Huang's transparent memory interfaces is not capable of being put into use without influence or control by another transparent interface. *See generally*, PO Resp. 43–52; *see also* Reply 19 (citing Ex. 1010, 249:6–11 (wherein Dr. Sechen, when questioned about the operation of the transparent memory interfaces A and B (corresponding to the claimed data handlers), illustrated in Figure 4 of Huang, acknowledged that "when transparent memory interface A is applying a test pattern to memory module A," it does not "affect how transparent memory interface B is applying its test pattern to memory module B")). Therefore, Patent Owner has not refuted Petitioner's prima facie showing that Huang teaches or suggests that its transparent memory interfaces are "configured to be

operated independently" (claim 1) and can "operat[e] . . . independently" (claim 16) as recited in the challenged claims.

c. dependent claims 2–5, 14 and 15

Claim 4 depends from claim 1 and recites: "wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers." Ex. 1001, 16:61–65.

Patent Owner argues Petitioner's challenge as to claim 4 is based on the combination of Huang and Tsern, and that Petitioner has not explained how Huang, alone, discloses or suggests two physically separate integrated circuit packages as claimed. PO Resp. 53. Patent Owner further relies on the following statement in Huang in support of its contention that Huang teaches away from a design in which individual data handlers are in separate integrated circuit packages: "Due to the improvement of VLSI technology, most systems can be condensed into a chip." *Id.* at 53–54 (quoting Ex. 1004, 379).

We agree with Patent Owner that in its Petition, Petitioner does not identify clearly a teaching or suggestion in Huang, alone, of two physically separate integrated circuit packages. *See* Pet. 42 ("[A] POSITA would be motivated to combine Huang and Tsern . . . to supplement the teachings of Huang relating to the desire to have test interfaces generate test patterns locally with Tsern's teachings of efficient ways to incorporate a self-testing memory system within multiple integrated circuits on a printed circuit board."). Petitioner does not argue, until its Reply, that it would have been nothing more than a routine design choice to use physically separate

integrated circuit packages for individual transparent interfaces (the alleged data handlers). In support of its Reply, Petitioner relies exclusively on the second Alpert declaration, wherein Dr. Alpert explains, for the first time, that modification of Huang to achieve the limitations recited in claim 4 would have been within the knowledge and level of skill of the ordinary artisan. *Compare* Ex. 1007 ¶ 156 (testifying "[t]o the extent that this additional claim element may not be disclosed by Huang alone, it is disclosed by Tsern," but failing to explain how the claim 4 limitations are disclosed or suggested by Huang), *with* Ex. 1009 ¶ 64 ("A person of ordinary skill in the art would have understood that an embedded computer system can be implemented as a single integrated circuit or as multiple integrated circuits ("chips") and other components.").

Rule 42.22(a)(2) provides that a petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent." 37 C.F.R. § 42.22(a)(2). Rule 42.23(b) provides that "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response." 37 C.F.R. § 42.23(b). Practice relating to replies is addressed in the Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012):

> While replies can help crystalize issues for decision, a reply that raises a new issue or belatedly presents evidence will not be considered and may be returned. The Board will not attempt to sort proper from improper portions of the reply. Examples of indications that a new issue has been raised in a reply include new evidence necessary to make out a *prima facie* case for the patentability or unpatentability of an original or proposed substitute claim, and new evidence that could have been presented in a prior filing.

"Whether a reply contains arguments or evidence that are outside the scope of a proper reply under 37 C.F.R. § 42.23(b) is left to our determination." *Vibrant Media Inc. v. General Electric Co.*, Case IPR2013-00170, slip op. at 31 (PTAB June 26, 2014) (Paper 56).

In our judgment, Petitioner's arguments and evidence in the Reply are outside the scope of a proper reply because they do more than merely address Patent Owner's argument that Huang teaches away; rather, they attempt to provide a new theory for modifying Huang that was not set forth clearly in the Petition. Consideration by the Board of these arguments in the Reply and evidence presented in Dr. Alpert's second declaration in support thereof would be unfair to Patent Owner. We have, however, reviewed and considered the arguments in the Petition and evidence therein, and are in agreement with Patent Owner that Petitioner has not provided adequate explanation or evidence to support its contention that Huang discloses or suggests the limitations recited in claim 4. Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claim 4 would have been unpatentable over Huang.

Patent Owner also contends Petitioner has not met its burden to show unpatentability of dependent claims 2–5, 14, and 15, because Petitioner has failed to show Huang discloses or suggests all of the limitations of independent claim 1, from which these claims depend. PO Resp. 54. With respect to claims 2, 3, 5, 14, and 15, we have reviewed the Petition and evidence cited therein, and determine Petitioner has met its burden to show these claims are unpatentable as obvious in view of Huang. *See* Pet. 39–41, 43–45.

3. Conclusion

Petitioner has met its burden to show that claims 1–3, 5, and 14–16 are unpatentable under 35 U.S.C. §103(a) based on Huang. Patent Owner has persuaded us that Petitioner failed to meet its burden to establish unpatentability of claim 4 under 35 U.S.C. §103(a) based on Huang.

C. Alleged unpatentability of claims 6–8, 11, and 17–20 under § 103(a) based on Huang and Averbuj

Claim 6 depends indirectly from claim 1 and claim 17 depends directly from claim 16. Claims 6 and 17 and recite: "verifying that data received from the one or more memory locations of the one or more memory chips corresponds to the data" written/transmitted "to the one or more memory locations of the one or more memory chips." Ex. 1001, 17:7–11, 18:29–32. Claims 7 and 8, and claims 18–20 include these limitations by virtue of their dependencies from claims 6 and 17, respectively. Claim 11 depends directly from claim 1 and recites that the data generated by the one or more data handlers comprises "*cyclic* data." *Id.* at 17:33–35. Claim 20 includes a similar limitation. *Id.* at 18:43–45.

With respect to claims 6 and 17, Petitioner contends Averbuj's comparator 48 corresponds to the claimed verification element. *See* Pet. 46 (citing Ex. 1003 ¶ 53; Figs. 6, 10). Petitioner contends one of ordinary skill in the art "would have been motivated to combine the self-testing memory modules disclosed in Huang . . . with the teachings of Averbuj because (among other reasons) adding this additional functionality within the memory interface furthers Huang's desire to perform test data operations locally to avoid excess data routing." Pet. 46 (citing Ex. 1007 ¶¶ 177, 181).

With respect to claims 11 and 20, Petitioner contends Averbuj discloses a data handler (i.e., data generation unit (44)) that "may be

instructed to generate different types of test patterns, including a checkerboard pattern (*i.e.*, cyclic data)." Pet. 49 (citing Ex. 1003 ¶ 49). Petitioner contends one of ordinary skill in the art "would have been motivated to combine the self-testing memory modules disclosed in Huang . . . with Averbuj's disclosure of cyclic test patterns because this is a well-known technique commonly employed in BIST systems. *Id.* at 49 (citing Ex. 1007 ¶¶ 190).

Patent Owner contends Petitioner has not shown how Huang and Averbuj could be combined in the manner claimed. PO Resp. 54. Patent Owner relies on the declaration testimony of Dr. Sechen to establish Huang and Averbuj are incapable of being combined. *Id.* at 55–59 (citing Ex. 2012 ¶¶ 213, 216–217, 219–220, 223, 225–226).

Dr. Sechen testified that "the prior art elements of Averbuj (*i.e.*, cyclic data generation and data verification) that Petitioner cites are incapable of being combined with Huang" (Ex. 2012 ¶ 213) and "[e]ven if it were assumed that [the ordinary artisan] would have attempted to combine Huang and Averbuj, the combination would not have worked for its intended purpose" (*id.* ¶ 220). Dr. Sechen testified that "[t]he *cyclic data* generation in Averbuj is controlled by the sequencer, . . . [which] instructs the data generation unit 44 to generate different types of test patterns, including a checkerboard pattern (i.e., the alleged *cyclic data*)." *Id.* ¶¶ 217–218. Dr. Sechen further testified that "Huang's data generation is tied to the memory contents, and specific data patterns cannot be selected by Averbuj's sequencer;" "Huang's system cannot be instructed to generate different types of test patterns." *Id.* ¶ 219. Dr. Sechen also testified as to why he believed

Averbuj's verification element could not be added to Huang. *See id.* ¶¶ 221–227.

In its Reply, Petitioner contends Patent Owner has "fail[ed] to consider the references as a whole," and has "mistakenly argue[d] that applying specific components of Averbuj with the system of Huang would render the resulting system unfit for its intended purpose." Reply 20–21. Petitioner explains that according to its proposed combination, Huang's Normal/BIST signal would be used to switch between the data outputs of Huang's testing scheme and Averbuj's testing scheme. *Id.* at 21. Petitioner relies on testimony in Dr. Alpert's second declaration in support of its arguments. *See id.* at21–22 (citing Ex. 1009 ¶¶ 68–73).

Dr. Alpert testified that "Dr. Sechen's analysis fails to recognize the motivation for combining Huang and Averbuj because he erroneously conflates various types of testing that are used for different purposes at different times." Ex. 1009 ¶ 68. Dr. Alpert goes on to provide detailed opinion testimony on the understanding of the ordinary artisan with respect to the teachings of Huang and Averbuj, and a detailed explanation of how Huang's system could be modified to include Averbuj's testing system and the motivation of the ordinary artisan to make such combination. *See id.* ¶¶ 69–72. According to Dr. Alpert, "[a] person of ordinary skill in the art would have seen the combination of Averbuj and Huang as choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success." *Id.* ¶ 72.

At oral argument, Patent Owner confirmed its understanding of Petitioner's challenge, as set forth in the Petition, as "starting with Huang and bringing in one element from Averbuj." Tr. 59:24–25. Patent Owner

argued that "Petitioner's reply changes the combination to comprise Averbuj's entire system, not just the cyclic test generation portion." *Id.* at 59:21–23. Patent Owner argued that the Petition includes only conclusory statements of a motivation to combine and fails to explain how Averbuj and Huang are combinable. *See id.* at 60:7–15. Patent Owner also argued Dr. Alpert's second declaration and deposition present new opinions as to how Averbuj and Huang could be combined. *Id.* at 53:3–5. Petitioner contended the challenge, as set forth in the Petition, and Dr. Alpert's first declaration in support thereof, were sufficient because combining Averbuj and Huang was trivial. *See id.* at 26:15–17.

Petitioner contended Dr. Alpert did not express new opinions in his second declaration and deposition, but was merely responding to Dr. Sechen's testimony. *Id.* at 81:17–19; *see also*, *id.* at 82:20–83:3 (wherein Petitioner argued: "[I]n their response, Patent Owner took the position that . . . it was physically incapable to combine Averbuj and Huang. We're entitled to respond to that and show that, in fact, they're not correct, and we did it by saying, listen, we pointed to the multiplexers in the petition, it's super, it's simple to use those multiplexers to combine. . . . [I]t is not incapable. A person of skill in the art could have done that.").

As discussed in Section IV.B.2.c., a petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent" (37 C.F.R. § 42.22(a)(2)), and "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response" (37 C.F.R. § 42.23(b)).

We agree with Patent Owner that the Reply does more than merely respond to or rebut arguments made in Patent Owner's Response; rather, it sets forth a theory that was not presented clearly in the Petition. Patent Owner's position is supported by the fact that Dr. Sechen, whose skill level is at least (and appears to exceed) that of the ordinary artisan, apparently was unable to envision how Huang and Averbuj could be combined. Further, Dr. Alpert's second declaration includes, at a minimum, opinions as to the understanding of the ordinary artisan with respect to the teachings of Huang and Averbuj that were not presented in his first declaration.

In our judgment, consideration by the Board of the above-noted arguments in the Reply and evidence presented in Dr. Alpert's second declaration in support thereof would be improper under 37 C.F.R. § 42.23, and unfair to Patent Owner. We have, however, reviewed and considered the arguments in the Petition and evidence therein, and are in agreement with Patent Owner that Petitioner has not provided adequate explanation or evidence to support its contention that one of ordinary skill in the art would have had a reasonable expectation of success in combining Huang and Averbuj. Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 6–8, 11, and 17–20 would have been unpatentable over Huang and Averbuj.

D. Alleged unpatentability of claims 9 and 10 under 35 U.S.C. § 103(a) based on Huang, Averbuj, and JEDEC Standard

Claims 9 and 10 depend from claim 5. Petitioner relies on JEDEC Standard (Ex. 1006) as evidence that at the time of the invention claimed in the '501 patent, it was known in the art to record failing data and corresponding addresses for BIST failures as recited in claims 9 and 10 (Pet. 30, 51 (citing Ex. 1006 § 8.2.4.5)), and contends it would have been obvious

to have recorded failing data and corresponding addresses in Averbuj's and Huang's BIST systems to enable a failure analysis and determination of error locations (*id.* at 31, 51–52). Petitioner's challenge does not present further arguments or evidence to cure the deficiencies in its challenge with respect to claim 5. *See* Section IV.B.2., above.

Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 9 and 10 are unpatentable under 35 U.S.C. §103(a) based on Huang, Averbuj, and JEDEC standard.

V. CONCLUSION

Petitioner has met its burden to show, by a preponderance of the evidence, unpatentability of: claims 1–3, 5–8, 11–14, and 16–20 under 35 U.S.C. §102(b) based on Averbuj; and claims 1–3, 5, and 14–16 under 35 U.S.C. §103(a) based on Huang.

Petitioner has failed to meet its burden to establish unpatentability of: claim 15 under 35 U.S.C. §102(b) based on Averbuj; claim 4 under 35 U.S.C. §103(a) based on Huang; claims 6–8, 11, and 17–20 under 35 U.S.C. §103(a) based on based on Huang and Averbuj; and claims 9 and 10 under 35 U.S.C. §103(a) based on Huang, Averbuj, and JEDEC Standard.

VI. ORDER

For the reasons given, it is

ORDERED that claims 1–3, 5–8, and 11–20 are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Lori A. Gordon
lgordon-PTAB@skgf.com

Robert E. Sokohl
rsokohl-PTAB@skgf.com

PATENT OWNER:

Thomas J. Wimbiscus
twimbisucs@mcandrews-ip.com

Scott P. McBride
smcbride@mcandrews-ip.com

Gregory C. Schodde
gschodde@mcandrews-ip.com
Ronald H. Spuhler
rspuhler@mcandrews-ip.com

Wayne H. Bradley
wbradley@mcandrews-ip.com

Trials@uspto.gov
571-272-7822

Paper 37
Entered: April 27, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00971
Patent 8,359,501 B1

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges.*

GAUDETTE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

Sandisk Corporation ("Petitioner") filed a Petition (Paper 1, "Pet.") on June 18, 2014, requesting institution of an *inter partes* review of claims 1–20 (the "challenged claims") of U.S. Patent No. 8,359,501 B1 (Ex. 1001, "the '501 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp."). Based on these submissions, an *inter partes* review of claims 1–20 was instituted on December 16, 2014, pursuant to 35 U.S.C. § 314. Paper 12 ("Dec. on Inst." or "Institution Decision").

After institution, Patent Owner filed a Response (Paper 19, Corrected Patent Owner Response, "PO Resp."), and Petitioner filed a Reply to the Patent Owner Response (Paper 25, "Reply").

Patent Owner also filed a Motion for Observation Regarding Cross-Examination of Dr. Donald Alpert. Paper 28 ("PO Mot."). Petitioner filed a Response to the Motion (Paper 32, "Pet. Resp."). Oral argument was held on July 27, 2015. A transcript of the oral hearing ("Tr.") has been entered into the record. *See* Paper 33.

The Board has jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision, issued pursuant to 35 U.S. C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–3, 5–20 of the '501 patent are unpatentable. Petitioner has not met its burden to show that claim 4 is unpatentable.

A. Related Proceedings

Petitioner also requested, and we instituted, an *inter partes* review of U.S. Patent No. 8,001,434 ("the '434 patent"). The '501 patent claims priority as a continuation of the '434 patent: *Sandisk Corp. v. Netlist, Inc.*,

Case IPR2014-00970 (PTAB December 16, 2014). Oral argument in IPR2014-00970 was consolidated with the oral argument in the present *inter partes* review. A final decision in IPR2014-00970 is issued concurrently with this final decision.

Patent Owner informs us that the '501 patent is the subject of an infringement action filed by Patent Owner: *Netlist, Inc. v. Smart Modular Technologies, Inc.*, No. 4:13-cv-05889-YGR (N.D. Cal. Dec. 19, 2013). Paper 9, 2. SMART Modular Technologies, Inc., a named defendant, filed two petitions for *inter partes* review of the '501 patent on August 23, 2014: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Cases IPR2014-01374 and IPR2014-01375 (PTAB). *Id.* at 3. On August 23, 2014, SMART Modular Technologies, Inc. also filed two petitions for *inter partes* review of the related '434 patent: *Smart Modular Technologies Inc. v. Netlist, Inc.*, Cases IPR2014-01372 and IPR2014-01373 (PTAB). *Id.* On March 10, 2015, we instituted *inter partes* reviews in IPR2014-01372 and IPR2014-01374. IPR2014-01372, Paper 13; IPR2014-01374, Paper 12. Oral arguments for IPR2014-01372 and IPR2014-01374 were consolidated, and held on November 17, 2015.

B. The '501 patent (Ex. 1001)

The '501 patent relates to self-testing electronic memory modules. Ex. 1001, 1:27–28. A block diagram of an exemplary self-testing memory module is shown in Figure 3 of the '501 patent, reproduced below. *See id.* at 9:25–26.

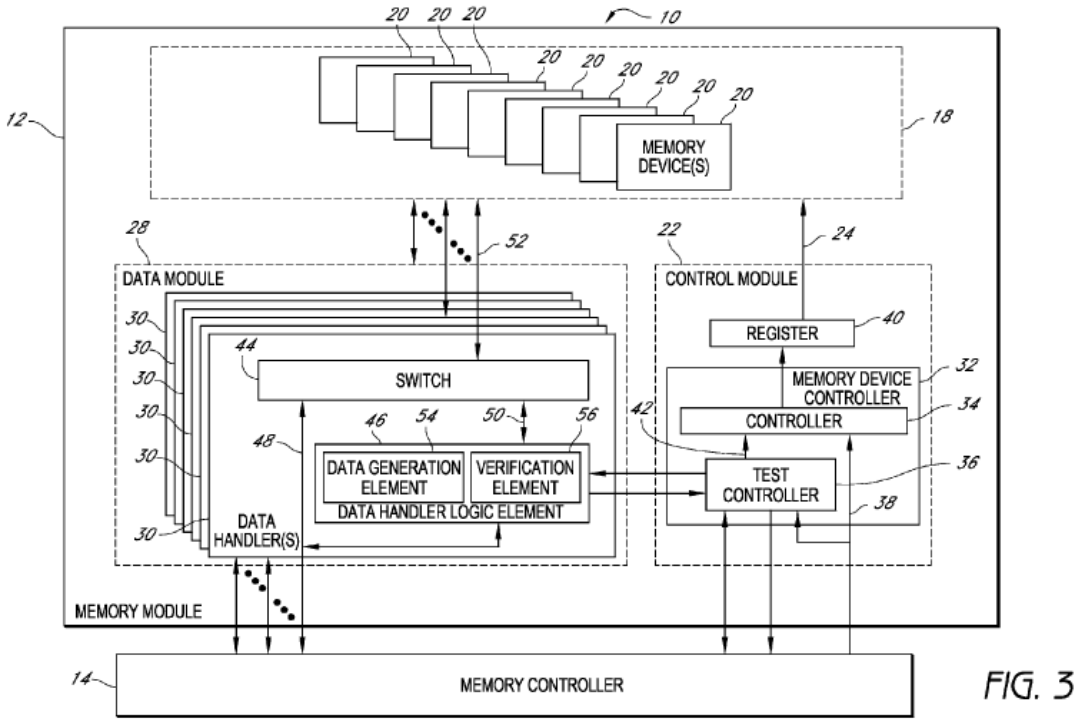


FIG. 3

As illustrated in Figure 3, above, "memory module 10 includes a printed circuit board 12 configured to be operatively coupled to a memory controller 14 of a computer system 16." *Id.* at 5:6–8. Memory module 10 includes a plurality of memory devices 18, each memory device 20 of the plurality of memory devices 18 comprising data, address, and control ports. *Id.* at 5:8–12. "[M]emory module 10 comprises a control module 22 [and] . . . a data module 28." *Id.* at 5:12–15.

"[C]ontrol module 22 can be configured to generate address and control signals 24 for testing the plurality of memory devices 18." *Id.* at 9:29–31. In the embodiment shown in Figure 3, control module 22 includes control mixer element 32 for controlling the address and control signals for the self-testing function. *Id.* at 9:35–37. Control mixer element 32 includes memory device controller 34 (e.g., a DRAM controller) and test controller 36. *Id.* at 9:33–35. "[T]est controller 36 controls the generation of the

address and control signal sequences to be used during the self-testing operation of the memory module 10 and also communicates with the data module 28." *Id.* at 9:53–56. "[M]emory device controller 34 receives signals 38 (e.g., address and control signals) from the system memory controller 14 and signals 42 (e.g., address and controls signals) from the test controller 36." *Id.* at 9:41–44.

Data module 28 comprises a plurality of data handlers 30 that "may be operatively coupled to (e.g., logically and/or electrically coupled to) the corresponding plurality of data ports" of memory devices 18. *Id.* at 5:14–16, 21–23. In the embodiment illustrated in Figure 3, each of data handlers 30 includes data handler logic element 46, comprising data generation element 54 and verification element 56. *Id.* at 10:31–34. "[D]ata generation element 54 may be configured to generate data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports" of memory devices 18. *Id.* at 10:35–37. "The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." *Id.* at 10:37–41.

C. Illustrative Claims

Independent claims 1 and 16 are illustrative of the claimed subject matter:

> 1. A memory system configured to be operatively coupled to a memory controller of a computer system, the memory system comprising:
>
> a plurality of memory chips;
>
> a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured

to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips;

a control circuit configured to generate address and control signals, wherein the memory system is configured to test the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the one or more data handlers.

16. A method of operating a memory system configured to be operatively coupled to a memory controller of a computer system, the memory system having a plurality of memory chips, the method comprising:

operating a plurality of data handlers independently from one another to generate and transmit data to one or more memory locations of one or more memory chips of the plurality of memory chips;

operating a control circuit to generate address and control signals; and

testing the one or more memory locations of the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the plurality of data handlers.

D. The Prior Art

The instituted grounds of unpatentability in this *inter partes* review are based on the following prior art:

Reference	**Publication**	**Exhibit**	**Date**
Averbuj	U.S. Patent Application Publication No. 2005/0257109 A1	1003	Nov. 17, 2005
Huang	*An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers*, Fourteenth International Conference on VLSI Design 379–384 (2001), IEEE	1004	2001

Reference	Publication	Exhibit	Date
JEDEC Standard	JEDEC Standard, Fully Buffered DIMM (FBDIMM): DFx Design for Validation and Test, JESD82–28	1006	Feb. 2008

E. The Instituted Grounds of Unpatentability

We instituted the instant *inter partes* review of claims 1–20 on the following grounds:

Claims	Basis	Reference(s)
1–3, 5–8, and 11–20	§ 102(b)	Averbuj
1–5 and 14–16	§ 103(a)	Huang
6–8, 11, and 17–20	§ 103(a)	Huang and Averbuj
9 and 10	§ 103(a)	Huang and JEDEC Standard
9 and 10	§ 103(a)	Averbuj and JEDEC Standard

F. Expert Testimony

Petitioner relies on the testimony of Dr. Donald Alpert in support of its patentability challenges. Dr. Alpert executed a first declaration (Ex. 1007) in support of the Petition and a second declaration (Ex. 1009) in support of Petitioner's Reply. Dr. Alpert was cross-examined on the subject matter of his first and second declarations, and transcripts of the testimony were filed as Exhibits 2013 and 2021, respectively.

Dr. Alpert testified that he "received an Electrical Engineering Ph.D. degree in 1984 from Stanford University." Ex. 1007 ¶ 6. Dr. Alpert testified that he taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities (*id.*), and that he worked in the computer industry, i.e., designing microprocessors and components for Burroughs Corporation, Zilog, National Semiconductor, and Intel, at various times between 1976 and 1997 (*id.* ¶ 7). Dr. Alpert testified that his "own training and experience exceeds that of ordinary skill in the art." *Id.* ¶ 21.

Patent Owner relies on the testimony of Dr. Carl Sechen. Dr. Sechen executed a declaration (Ex. 2012) in support of Patent Owner's Response. Dr. Sechen was cross-examined on the subject matter of his declaration, and a transcript of the testimony was filed as Exhibit 1010.

Dr. Sechen testified that he "was awarded a Ph.D. in electrical engineering from the University of California at Berkeley in 1986" (Ex. 2012 ¶ 6), and has been a Professor of Electrical Engineering for more than 28 years (*id.* ¶ 3). Dr. Sechen testified that during this time period, his research has focused on design and computer-aided design of digital integrated circuits, including the design of DRAM, and that he has taught numerous students how to design DRAM memories. *Id.* Dr. Sechen testified that he has "also been involved in numerous research projects on VLSI design and memory design[, and has] . . . taught numerous graduate researchers how to design digital integrated circuits, including memories." *Id.* ¶ 5. Dr. Sechen testified that he is "at least a person of ordinary skill" in the art of memory module design. *Id.* ¶¶ 33–34.

To testify as an expert under Federal Rule of Evidence (FRE) 702, a person need not be a person of ordinary skill in the art, but rather "qualified

in the pertinent art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co., Inc.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 Fed. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). There is no dispute that Dr. Alpert and Dr. Sechen are qualified to testify as experts under FRE 702.

II. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is relevant to claim construction and determinations of anticipation and obviousness. *See Graham v. John Deere Co*., 383 U.S. 1, 17–18 (1966) (explaining that obviousness is a question of law based on underlying factual findings including the level of ordinary skill in the pertinent art); *Yorkey v. Diab*, 605 F.3d 1297, 1300 (Fed. Cir. 2010) (explaining that a determination of anticipation involves, interpreting the claim language and then comparing the construed claim to a prior art reference); *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1259–60 (Fed. Cir. 2010) ("[C]laim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.").

Petitioner's expert, Dr. Alpert, and Patent Owner's expert, Dr. Sechen, disagree as to the level of ordinary skill in the art. Dr. Alpert testified that "a person of ordinary skill in the art for the '501 patent would

have a bachelor's degree or the equivalent training or experience in electrical engineering and at least one year of experience relating to memory systems and BIST." Ex. 1007 ¶ 20. Dr. Sechen testified that

> one of ordinary skill in the art at the time of filing the application(s) for the '501 patent, who would be working on the design of memory devices and memory modules, would have at least a Bachelor of Science degree in electrical engineering or computer engineering, and at least five years of industry experience designing memory devices and memory modules. Alternatively, one of ordinary skill in the art would have an M.S. degree in electrical engineering or computer engineering, and at least three years of industry experience designing memory devices and memory modules. Moreover, one of ordinary skill in the art would have a Ph.D. degree in electrical engineering or computer engineering, and have at least one year of industry experience designing memory devices and memory modules.

Ex. 2012 ¶ 33.

The difference in the opinions of the two experts is that Dr. Sechen believes a person of ordinary skill in the art would have an additional four years of experience, education, or a combination of the two, beyond that proposed by Dr. Alpert. *See* Ex. 1009 ¶ 7. According to Dr. Alpert, the difference in the proposed levels of ordinary skill in the art is not material to any dispute over claim construction or patentability in this *inter partes* review. *Id.*

We accord greater weight to Dr. Alpert's opinion as to the level of ordinary skill in the art because he has experience in both teaching students and working with engineers in the industry, while Dr. Sechen's experience is primarily in teaching. *Compare* Ex. 1007 ¶¶ 7, 21, *with* Ex. 2012 ¶¶ 3, 5. Moreover, based on our review of the '501 patent and the types of problems

and solutions described in the '501 patent and cited prior art, we agree with Dr. Alpert's opinion on the level of ordinary skill. Accordingly, we find that a person of ordinary skill in the art at the time of the '501 patent would have a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST.

III. CLAIM CONSTRUCTION

In its Petition, Petitioner requested that "each claim be construed in accordance with its plain and ordinary meaning under the required broadest reasonable interpretation" standard. Pet. 6–7. In its Preliminary Response, Patent Owner offered a specific construction for the claim term "generate." Prelim. Resp. 24–26. For purposes of our Institution Decision, we interpreted the claim term "generate" as meaning "produce" or "cause." Dec. on Inst. 9.

In its Response, Patent Owner disagrees with the Board's interpretation of "generate" (*see* PO Resp. 19), and further asserts that express construction of the claim language "configured to generate" (claim 1) is "necessary in view of the arguments made by Petitioner" (PO Resp. 14). Patent Owner also proposes a construction for "operated independently" (claim 1)/"operating . . . independently" (claim 16). PO Resp. 32.

In its Reply, Petitioner asserts that "'configured to,' 'operated independently,' and 'generate' are common words whose plain and ordinary meanings are well-known, even to a lay person" and, therefore, "the terms should be given their plain and ordinary meaning." Reply 1. Petitioner

contends Patent Owner's proposed constructions "import[] limitations from the specification into the claims, which is impermissible." *Id.* Petitioner also provides proposed constructions of the claim terms/phrases in dispute. *See generally* Reply 2–9.

Patent Owner's and Petitioner's proposed constructions for the disputed claim language are listed in the table below.

Claim Term/Phrase	**Patent Owner's Proposed Construction**	**Petitioner's Proposed Construction**
Operated independently/ Operating . . . independently	a plurality of data handlers configured to be *used to independently test*/*using* a plurality of data handlers *to independently test* (PO Resp. 32)	the operation of a data handler is not influenced or controlled by another data handler (Reply 4)
Generate	produce (PO Resp. 31)	produce or cause production of (Reply 8 n.2)
Configured to generate	programmed to produce (PO Resp. 20)	designed to, arranged to, or adapted to perform the function of producing or causing (Reply 7)

In an *inter partes* review, the Board interprets claim terms in an unexpired patent according to the broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definitions for claim terms must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir.

1994). "[E]xtrinsic evidence may be used only to assist in the proper understanding of the disputed limitation; it may not be used to vary, contradict, expand, or limit the claim language from how it is defined, even by implication, in the specification or file history." *Tempo Lighting, Inc. v. Tivoli*, LLC, 742 F.3d 973, 977–78 (Fed. Cir. 2014) (internal quotations and citations omitted). Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999). A court may revisit and alter its construction of claim terms as the record in a case develops. *See Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd*, 599 F.3d 1308, 1322 (Fed. Cir. 2010).

Applying the foregoing principles of law, we review our construction of the claim term "generate,"[1] and also determine that the claim terms "configured to" and "operated independently"/"operating . . . independently" require construction.

A. Operated Independently/Operating . . . Independently

Independent claim 1 recites: "a plurality of data handlers configured to be operated independently from one other." Ex. 1001, 16:42–43. Independent claim 16 recites "operating a plurality of data handlers independently from one another" *Id.* at 18:15–16.

In its Response, Patent Owner asserts that the above recitations in claims 1 and 16 mean that the data handlers are used to *independently test* a portion of one or more memory chips. PO Resp. 32. During the oral hearing, Patent Owner argued that "'[o]perating independently' necessarily

[1] Our interpretation of the term "generate" also applies to other verb tenses used in the claims, i.e., "generating" and "generated."

means that the use or operation of a data handler is not dependent on the use or operation of another data handler for testing. For example, to be 'independently operable' means that one data handler can be used – i.e., operated – in one mode while another data handler is operated or used in another mode." Tr. 43:1–6. Petitioner contends "'*operable independently*' merely means that each data handler can operate without influence or control by any of the other data handlers." Reply 3 (citing Ex. 1009 ¶ 15 ("This would encompass data handlers that receive common control signals from one controller, as long as the data handlers are not in communication with each other.")).

In their papers, both Patent Owner (PO Resp. 32) and Petitioner (Reply 3) rely on column 8, lines 5–15 of the '501 patent in support of their proposed constructions:[2]

> Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28. *For example, each data handler 30 is configured to write to and/or read from the corresponding plurality of data ports of one or more of the memory devices 20 without being in communication [with] any of the other data handlers 30 or other data ports of the memory devices 20.* As such, each data handler 30 can be used to generally independently test a portion of the memory space of the memory module 10. For example, each data handler 30 may be used to independently test one memory device 20 of the memory module 10.

Ex. 1001, 8:5–15 (emphasis added). Petitioner quotes lines 1–11 in their entirety. Reply 3. Patent Owner omits the italicized language from its quotation. PO Resp. 32; *cf.* Tr. 43:16–18 (arguing that this language is

[2] Both parties also rely on the testimony of their experts and Petitioner relies on a dictionary definition. *See generally* PO Resp. 32; Reply 2–4.

immaterial to construction of the claim term "operable independently," because it "relates to reading and writing to the data ports[, not] . . . to data generation, which is the claimed operation of the data handler") .

We begin our interpretation of the disputed terms with the language of the claims. *See Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1299 (Fed. Cir. 2015).

Independent claim 1 recites: "a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips." Ex. 1001, 16:42–46. Claim 1 also recites "wherein the memory system is configured to test the one or more memory chips . . . using the data generated by the one or more data handlers. *Id.* at 16:48–51. Claim 1 thus requires that each of the plurality of data handlers is configured to be operated independently, but that only some of the data handlers (i.e., "one or more") are further configured to generate data used for testing. Patent Owner's proposed interpretation of "configured to be operated independently" (claim 1) as "configured to be used independently" (PO Resp. 32) narrows the meaning of this claim 1 phrase to encompass only the subset of data handlers that are also "configured to generate data" (claim 1). Patent Owner's proposed interpretation of "configured to be operated independently" (claim 1) is, therefore, inconsistent with the use of this phrase in the context of claim 1 in its entirety.

Independent claim 16 recites "operating a plurality of data handlers independently from one another to generate and transmit data to one or more memory locations of one or more memory chips of the plurality of memory

chips" and "testing the one or more memory locations of the one or more memory chips . . . using the data generated by the plurality of data handlers." *Id.* at 18:15–18, 21–24. We apply a presumption that "operating . . . independently" in claim 16 has the same meaning as "operated independently" in claim 1. *See PODS, Inc. v. Porta Stor, Inc.*, 484 F.3d 1359, 1366 (Fed. Cir. 2007) ("We apply a 'presumption that the same terms appearing in different portions of the claims should be given the same meaning unless it is clear from the specification and prosecution history that the terms have different meanings at different portions of the claims.'" (quoting *Fin Control Sys. Pty., Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001))). In other words, unless usage of "operating . . . independently" in the context of the '501 patent specification indicates otherwise, we presume one of ordinary skill in the art would not interpret the claim 16 phrase "operating a plurality of data handlers independently from one another" as limited to "*using* a plurality of data handlers *to independently test* a portion of one or more memory chips" (PO Resp. 32).

The term "operating" does not appear in the '501 patent specification. The phrase "configured to be operated" appears only once in the '501 patent specification as follows: "In certain embodiments, the memory module 10 is configured to be operated in a test mode." *See* Ex. 1001, 5:64–65. In our interpretation of the similar '434 patent claim term "operable independently" in our Final Decision in IPR2014-00970, we considered the disclosure in the related '434 patent corresponding to the following '501 patent disclosure:

> *Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28 and* is operatively coupled to a corresponding plurality of the data ports of one or more of the plurality of

> memory devices 18. For example, each of the data handlers 30 may be operatively coupled to (e.g., logically and/or electrically coupled to) the corresponding plurality of data ports. Each data handler 30 *is further configured to generate data for writing to the corresponding plurality of data ports*.

Ex. 1001, 5:16–23.

> Because each of the data handlers 30 is operable independently of each of the other data handlers 30, the data handlers 30 are generally modular. As such, modifications in the configuration of the memory module 10 (e.g., changes in the bit-width of the memory bus, changes in the number of memory devices 20, etc.) may be less complicated to accommodate than in other types of self-testing memory modules 10. For example, where a new memory device 20 or set of memory devices 20 is added to the memory module 10, the change may be generally accommodated by adding a corresponding data handler 30. The change may be accommodated without having to implement a major reorganization of the memory module 10 or the self-testing logic of the memory module 10, for example.

Id. at 8:22–35. In our Final Decision in IPR2014-00970, we found that the above description of each data handler as "operable independently" and having the "further" feature of being "configured to generate data" (*see id.* at 5:16–23) supported Petitioner's contention that the data generation function of the data handlers is an additional feature that is separate from the feature of independent operability. We found that based on the description quoted in column 8, lines 22–35, above, coupled with the discussion of the prior art problem of lack of flexibility in memory module self-test logic to accommodate changes to data width (*see id.* at 4:41–60, 8:24–29), one of ordinary skill in the art would understand the term "operable independently" to describe the data handlers as being discrete and functioning without being physically or logically connected to each other. In the present case, we find

similarly that the above-quoted language from the '501 patent specification is consistent with the plain meaning of the language in claim 1, i.e., that each of the plurality of data handlers is configured to be operated independently, but only some of the data handlers (i.e., "one or more") are further configured to generate data used for testing. We agree with Petitioner, therefore, that when interpreted in the context of the '501 patent in its entirety, the claim term "operated independently" "merely means that each data handler can operate without influence or control by any of the other data handlers." Reply 3. We find no basis in the '501 patent specification for applying a different construction to the claim 16 language "operating . . . independently." Accordingly, we interpret "operated independently"/"operating . . . independently" in accordance with its plain and ordinary meaning: "the operation of a data handler is not influenced or controlled by another data handler" (Reply 4).

B. Configured to, and Generate

Independent claim 1 recites "a plurality of data handlers . . . *configured to generate* data for writing to a corresponding one or more memory chips" and "a control circuit *configured to generate* address and control signals." Ex. 1001, 16:42–48. Independent claim 16 recites "operating a plurality of data handlers independently from one another to *generate* and transmit data" and "operating a control circuit to *generate* address and control signals." *Id.* at 18:15–16, 19–20 (emphasis added).

1. Configured to

Prior to institution, neither party requested, nor did we deem necessary, construction of the term "configured to." In its Response, Patent Owner now requests that we construe the term "configured to" in the context

of the claim phrase "configured to generate" (claim 1). *See* PO Resp. 14. As correctly observed by Petitioner, however, the term "configured to" is not used exclusively in conjunction with the term "generate" in claim 1, but is also used with the claim terms "test," "receive," "write," "calculate," "store," "verify," "be operatively coupled," "be operated independently" and "selectively input." *See* Reply 4. The term "configured to" is also used in the '501 patent specification in conjunction with the terms "provide" (Ex. 1001, 6:6, 33), "operatively couple" (*id.* at 7:26), "read" (*id.* at 9–10), "receive" (*id.* at 11:11–12), "check" (*id.* at 11:14), "perform" (*id.* at 11:20–21), "report" (*id.* at 12:25), and "input" (*id.* at 14:5, 8). Presumptively, "configured to" should carry the same meaning, and "configured to generate," "configured to test," "configured to write," etc. should have parallel meanings, differing only insofar as "test," "write," "generate," etc., differ. *See Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1337 (Fed. Cir. 2008) ("'[B]inary code' and 'trinary code' should have parallel meanings, differing only insofar as 'binary' and 'trinary' differ in their relationships to the numbers 2 and 3.").

Patent Owner does not offer an interpretation of the term "configured to" outside the context of the phrase "configured to generate" (*see* PO Resp. 14–19), but contends "'configured to generate' means 'programmed to generate' and enables the subsequent execution of a self-testing function (*e.g.,* data generation, writing and verification)" (*id.* at 18; *see also id.* at 15 ("'Programmed' is therefore synonymous with 'configured.'")).

Petitioner contends the claim term "configured to" should be construed consistently, whether used in conjunction with "generate" or with another function recited in the claims, and should be given its plain and

ordinary meaning of "designed to, adapted to, or arranged to." Reply 4. In addition to relying on the testimony of its expert, Dr. Alpert, Petitioner cites two dictionary definitions in support of its proposed interpretation. Reply 5 (citing Ex. 1011, 186; Ex. 1012, 428).

Dr. Alpert, testified that, in the '501 patent, "'program' is one example of 'configure,' but not the only example." Ex. 1009 ¶ 16. Dr. Alpert further testified "the '501 patent discloses that *configuring* can be accomplished in a wide variety of ways . . . , including those that do not require programming, for example using predefined values." *See id.* ¶ 19 (quoting Ex. 1001, 6:19–22 ("The address sequences and/or the data patterns of certain embodiments may be programmable either through the I^2C interface or they may be defaulted to pre-defined values."); Ex. 1001, 10:67–11:4 ("[R]andom or pseudorandom data may be generated and written to the corresponding plurality of data ports. For example, a linear feedback shift register (LFSR) may be used in some embodiments. In addition, the data patterns may be programmable."); *see also id.* at ¶ 20 ("The configuration of the data handlers can be fixed, hardwired." (citing Ex. 1001, Figure 2, 8:5–19, 36–55)); Ex. 2021, 135:12–136:2 (wherein Dr. Alpert testified that a linear feedback shift register would not need to be programmed to generate data, but could be arranged or designed to generate data). In his second declaration, Dr. Alpert also testified that:

> The '501 patent uses "configured" to describe hardwired arrangements of components that cannot be programmed for their configuration. Additionally, the '501 patent discloses various components included in the control module, which do not all require programming: . . . . The configuration of the verification circuitry can be fixed without any memory structure for storing a copy of the generated data, as disclosed at 11:28–

> 31. . . . [And,] control module 22 [can] include[] discrete logic [or] one or more application-specific integrated circuit (ASICs) . . . [b]oth . . . could be programmable or nonprogrammable as would have been understood by a person of ordinary skill.

Ex. 1009 ¶ 20 (emphasis omitted).

Patent Owner's expert, Dr. Sechen, testified that "the most conventional use of *configuration* refers to hardware programming" (Ex. 1010, 68:25–69:2 (emphasis added)), but that it could refer to software programming as well. *Id.* at 55:17–18. In his declaration, Dr. Sechen did not testify as to the meaning of "configured to" in conjunction with any term other than "generate." *See* Ex. 2012 ¶¶ 46–67. In response to questioning during cross-examination, however, Dr. Sechen testified that "configured to," as used in the context of the phrase "a printed circuit board configured to be operatively coupled to a memory controller of a computer system" (Ex. 1001, 2:25–27), "might mean designed [to]" because the printed circuit board has to be configured "such that it fits into the slot on the motherboard and is able to communicate successfully with the memory controller." Ex. 1010, 84:14–19. The '501 patent discloses that components of control module 22 and data module 28 may include discrete logic and application specific integrated circuits (ASICs) (*see* Ex. 1001, 9:62–64, 12:33–37), which, on cross-examination, Dr. Sechen conceded can be designed to operate without the need for hardware programming. Ex. 1010, 58:9–61:22.

Based on our analysis of the '501 patent claims and specification, and relying on the testimony of Drs. Alpert and Sechen regarding the technology,[3] we find the '501 patent uses the term "configured to" to

[3] "Although the patent file may often be sufficient to permit the judge to interpret the technical aspects of the patent properly, consultation of

describe components that can be programmed by a controller to perform a function, as well as components that can be hard-wired to perform a function and do not require programming. *See, e.g.*, Ex. 1001, 7:25–31 ("PCB 12 may include at least one connector (not shown) configured to operatively couple the memory module 10 to the memory controller 14 of the computer system 16. . . . For example, the memory module is electrically coupled, logically coupled, or both, with the memory controller 14"); *id.* at 8:50–53 ("[T]he data handlers 30 may be operatively coupled (e.g., electrically and/or logically coupled or connected) to the eight data ports 21 of one of the corresponding memory devices 20"). We do not agree with Patent Owner, therefore, that the broadest reasonable interpretation of "configured to" is "programmable to." *Cf.* Ex. 1010, 89:3–5 ("'Designed' implies a certain hardwiredness, that that's what it does, and 'configured' implies that maybe it only does that some of the time."). Rather, we agree with Petitioner that one of ordinary skill in the art would interpret the claim term "configured to" in accordance with its plain and ordinary meaning, and would understand that this term encompasses components both programmable and hard-wired to perform the functions described in the '501 patent. Accordingly, we interpret the term "configured to" as "designed, adapted, or arranged to."

2. Generate

In addition to reciting "a plurality of data handlers . . . configured to

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extrinsic evidence is particularly appropriate to ensure that his or her understanding of the technical aspects of the patent is not entirely at variance with the understanding of one skilled in the art." *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1309 (Fed. Cir. 1999).

generate data" and "a control circuit configured to generate address and control signals," claim 1 recites: "wherein the memory system is configured to test the one or more memory chips using the address and control signals *generated by* the control circuit and using the data *generated by* the one or more data handlers" (Ex. 1001, 16:48–51 (emphasis added)). Similarly, in addition to reciting "operating a plurality of data handlers independently from one another to *generate* and transmit data" and "operating a control circuit to *generate* address and control signals," claim 16 recites a step of : "testing the one or more memory locations of the one or more memory chips using the address and control signals *generated by* the control circuit and using the data *generated by* the plurality of data handlers" (*id.* at 18:21–24 (emphasis added)).

For purposes of our Institution Decision, we interpreted the claim term "generate" as meaning "produce" or "cause." *See* Dec. on Inst. 8–9. Our interpretation was based on findings that the plain and ordinary meaning of "generate," as evidenced by Merriam-Webster's Collegiate Dictionary, is "produce" or "be the cause of" (*id.* at 9 (citing Ex. 2002, 484)), and that interpreting "generate" to mean "cause" was not inconsistent with the '501 patent specification, which broadly states that data can be generated by the data handlers in a variety of ways (*see id.* at 8–9 (citing Ex. 1001, 10:53–54)).

Petitioner contends the Board should maintain its construction of "generate" as "produce" or "cause," because this construction "reflects the plain and ordinary meaning." Reply 8–9. Petitioner maintains one of ordinary skill in the art "would appreciate that when substituted in the claims, the Board's construction is 'produce or cause production of

[data/address and control signals].'" *Id.* at 8 n.2 (citing Ex. 1009 ¶ 29). During cross-examination, Dr. Alpert explained the difference between producing and causing to produce" as follows: "[P]roducing would actually be either creating or providing, in this case, some data and causing to produce would be having one device be the cause of or invoking another device to produce the data." Ex. 2013, 43:5–11. Dr. Alpert testified that one of ordinary skill in the art would understand the description of the data handler being logically coupled to the memory devices at column 5, lines 20–23 of the '501 patent as implying intermediary logical devices between the data handler and the memory device ports. *See id.* at 39:1–16. In other words, one of ordinary skill in the art would understand that the "physical system element" that produces the data used for testing in claim 1 "can be the data handler or it can be another device that the data handler causes to produce the data." *Id.* at 32:4–6. During cross examination, Dr. Alpert identified "a buffer or a multiplex[e]r" as examples of devices that could "exist between the data handler and the memory device" to produce the data used for testing. *Id.* at 36:13–16. Dr. Alpert explained that a

> buffer can take an input, information input and it can either produce a signal that contains that information or the complements of that information, or there could be several buffers that have potential to be in a third state, so-called tri-state buffers, such that the buffers can be used to select information that may be presented, that would be data that would be produced that would then be presented down to other circuits.

Id. at 36:24–37:8.

Patent Owner contends "'generate' is properly construed [only] as 'produce.'" PO Resp. 31 (citing Ex. 2012 ¶¶ 68–96); *see also id.* at 20

(quoting Ex. 2012 ¶ 70 ("In the context of integrated circuit and printed circuit board design, *generate* or *produce* (which are synonyms in this context) are terms of art.")). Patent Owner argues that interpreting "generate" as "cause," or as "cause to produce," as suggested by Petitioner, would render other claim language superfluous. *See id.* at 24–31. Specifically, Patent Owner contends that interpreting "generate" as "cause to produce" renders meaningless the claim limitations "the memory system is configured to test" (claim 1) and "testing" (claim 16) the memory chips "using the address and control signals generated by the control circuit and using the data generated by the . . . data handlers" (claim 1 and 16). *See id.* at 29–31; *see also id.* at 25 ("[T]he situation posited by the Board does not reflect that the data written by the data handler was 'generated by the data handler'" and eliminates the claim requirements that data generated by the data handlers is used for testing.

"[W]here there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meaning." *Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 2003). The '501 patent claims and specification use the term "generate" in conjunction with the memory module, control circuit/module, data module, and components thereof. The '501 patent further uses the term "generate" as a specific example of "produce," with the term "produce" appearing only once in the '501 patent:

> In some embodiments, the control module 22 and the data module 28 *produce* memory addresses, control and/or data signals according to the JEDEC standard memory protocol. In some embodiments, *for example*, the control module 22 and the data module 28 *generate* the memory interface signals with proper edge relationships based on the JEDEC standard.

Ex. 1001, 6:11–17 (emphasis added).

The '501 patent specification uses both the term "provide" and the term "generate" in describing the operation of data module 28:

> [D]uring testing, the control module 22 generates address and control signals 24 associated with memory locations to be tested and the *data module 28 generates corresponding test data patterns and provides them* to the appropriate memory devices 20. For example, the data module 28 may receive a write command from the control module 22 and provide data to be written to certain locations in the memory devices 20 during a write operation.

Id. at 5:48–55 (emphasis added). The term "provide" is also used separately from, but in a similar manner to, the term "generate" to describe embodiments of control module 22 and data module 28 used for testing memory devices 18. *Compare id.* at 6:5–11 ("The data module 28 and/or the control module 22 of certain embodiments are configured to test the plurality of memory devices 18 at the normal operating speed of the memory devices 20. For example, the data module 28 and/or the control module 22 are *configured to provide* memory signals (e.g., data, address and control signals) according the operating specification of the memory devices 20" (emphasis added)) *with id.* at 9:29–31 ("The control module 22 can be *configured to generate* address and control signals 24 for testing the plurality of memory devices 18." (emphasis added)) *and id.* at 10:31–37 ("Each of the data handlers 30 of certain embodiments further includes a data handler logic element 46. The data handler logic element 46 of certain embodiments comprises a data generation element 54 and a verification element 56. The data generation element 54 may be *configured to generate* data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports." (emphasis added)).

In addition to using the term "provide" to describe embodiments of control module 22 and data module 28, the '501 patent specification uses this term to describe the operation of switch 44: "The switch 44 may *provide* a bi-directional data multiplexer function" and is "configured to selectively input" data signals 48 from system memory controller 14 or data signals 50 from data handler logic element 46. *Id.* at 10:10–15 (emphasis added). The '501 patent specification discloses that switch 44 may positioned between data module 28 and memory devices 18 (*see id.* at 10:28–30), i.e., one of the hypothetical arrangements described by Dr. Alpert in which a data handler would cause an intermediary device (e.g., a multiplexer) to produce data. The '501 patent specification does not use the term generate (or produce), however, to describe the configuration or operation of switch 44. The '501 patent specification also describes an embodiment in which switch 44 is included in each of data handlers 30 (*id.* at 10:7–8), as well as an embodiment in which the function of selective inputting of data signals to memory devices 18 is not limited explicitly to a switch (*see, e.g.*, *id.* at 6:1–4 ("[E]ach of the data handlers 30 write[s] the data generated by the data handler 30 to the corresponding plurality of data ports by selectively inputting data signals to the data ports of the plurality of memory devices 18.")).

The above-noted usages of the terms "provide" and "generate" to describe different embodiments of control module 22 and data module 28, and to describe different functions of the data handlers, do not support Dr. Alpert's opinion that the term "generate" is properly interpreted as

encompassing the selection function of a multiplexer.[4] Use of the term "generate" to describe an embodiment in which the control module and data handlers "produce" memory addresses, control and/or data signals, however, does support Dr. Sechen's opinion that "generate" and "produce" are synonymous.

In the absence of evidence to the contrary, there is a presumption that different claim terms have different meanings. *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000); *see also SEB S.A. v. Montgomery Ward & Co., Inc.*, 594 F.3d 1360, 1369 (Fed. Cir. 2010) (noting there is a presumption that meanings of claim terms do not overlap); *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

The claim 1 recitation of "data handlers . . . configured to generate data for writing" and dependent claim 14 recitation of "the one or more circuits [sic, data handlers] . . . *further configured* to write data to the one or

[4] Dr. Alpert's testimony, though consistent with Averbuj's use of the term "generate" (*see* Ex. 1003 ¶ 56 ("[D]ata generation unit 44 generates the transformed data signal 49 (BIST_DATA_T) to fill the memory module 12 with the data dictated from the sequencer 8 without modification.")), cannot be relied on to construe this claim term in a manner that varies from the implicit definition in the '501 patent. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584–85 (Fed. Cir. 1996) ([P]rior art can often help to demonstrate how a disputed term is used by those skilled in the art. . . . [H]owever, reliance on such evidence is unnecessary, and indeed improper, when the disputed terms can be understood from a careful reading of the public record. Nor may it be used to vary claim terms from how they are defined, even implicitly, in the specification or file history." (internal citation omitted)).

more memory chips by selectively inputting," as well as the above disclosure in the '501 patent specification, create a presumption that "generate" has a different meaning than "write" and/or "selectively input." *See also* claim 1 ("a control circuit configured to generate address and control signals") and dependent claim 15 ("the control circuit is *further configured* to selectively input to the address and control ports of the one or more memory chips either the address and control signals from the memory controller of the computer system or the address and control signals from the control circuit." (emphasis added)). Likewise, the recitations of "operating a plurality of data handlers . . . to generate and transmit data" in independent claim 1, and "data transmitted to the one or more . . . memory chips" in dependent claims 17 and 20, create a presumption that "generate" has a different meaning than "transmit." In other words, the '501 patent specification and claims do not support an interpretation of "data generated" by a component as encompassing data selected, written, input, or transmitted by a first component to a second component, because such interpretation would result in an overlap in the meaning of "generate" and "write" and/or "selectively input" and/or "transmit."

Having considered the ordinary meaning of the term "generate" in the context of both the claims and the '501 patent as a whole, we agree with Patent Owner that the broadest reasonable interpretation of the claim term "generate" is "produce," and that "generate" does not mean "cause" or "cause to produce." We interpret the claim language "address and control signals *generated* by the control circuit" and "data *generated* by the . . . data handlers" (claims 1 and 16), as encompassing signals and data that originated in the control circuit and data handlers, including by

transformation or modification of information and/or data received from another component. *See e.g.* Ex. 1001, 10:37–41 ("The data signals and/or patterns of data signals may be *based on* information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." (emphasis added)); *id.* at 10:61–63 ("The data may be generated *based [on]* previously written data (e.g., inverting each of the bits of a previously written data word)" (emphasis added)). We do not interpret this language as encompassing signals and data received by the control circuit and data handlers from another component, and merely provided, propagated, sent, or input to memory devices, without transformation or modification by the control circuit and data handlers. *Compare, e.g.*, Ex. 1001, 9:54–57 ("In one embodiment, the memory device controller 34 *generates* the address and control signals for memory device (e.g., DRAM device) operations." (emphasis added)), *with id.* at 9:40–53 ("In one embodiment, the memory device controller 34 *receives* signals 38 (e.g., address and control signals) from the system memory controller 14 and signals 42 (e.g., address and controls signals) . . . [M]emory device controller 34 *may send* either the signals 38 from the system memory controller 14 or, alternatively, the signals 42 from the test controller 36, to the register 40." (emphasis added)).

Thus, in summary, we construe "operated independently/operating independently," "generate," and "configured to" as follows:

Claim Term/Phrase	**Interpretation**
Operated independently/ Operating . . . independently	Operated, or operating, without influence or control by another

Claim Term/Phrase	Interpretation
Generate	produce
Configured to	designed to, adapted to, or arranged to [e.g., perform a function or be capable of performing a function]

IV. ANALYSIS

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged or combined in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

> A single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. Thus, a prior art reference without express reference to a claim limitation may nonetheless anticipate by inherency. "Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claims limitations, it anticipates."

Perricone v. Medicis Pharm. Corp., 432 F.3d 1368, 1375–76 (Fed. Cir. 2005) (citations omitted). "In general, a limitation or the entire invention is inherent and in the public domain if it is the 'natural result flowing from' the explicit disclosure of the prior art." *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham*, 383 U.S. at 17–18. An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

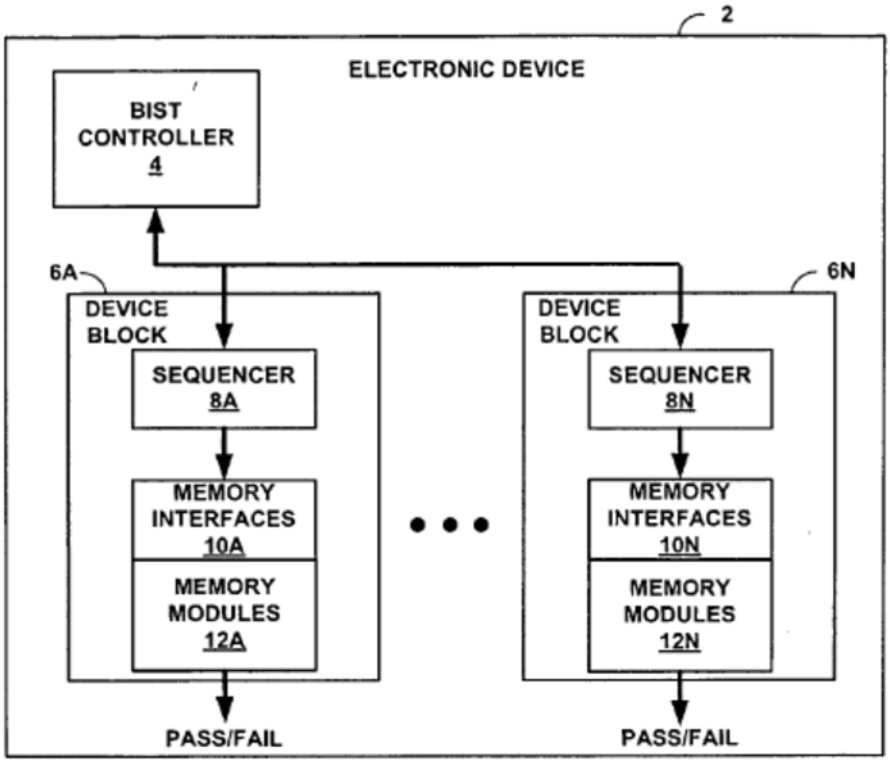
We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

A. Alleged unpatentability of claims 1–3, 5–8, and 11–20 under §102(b) based on Averbuj

1. Averbuj (Ex. 1003)

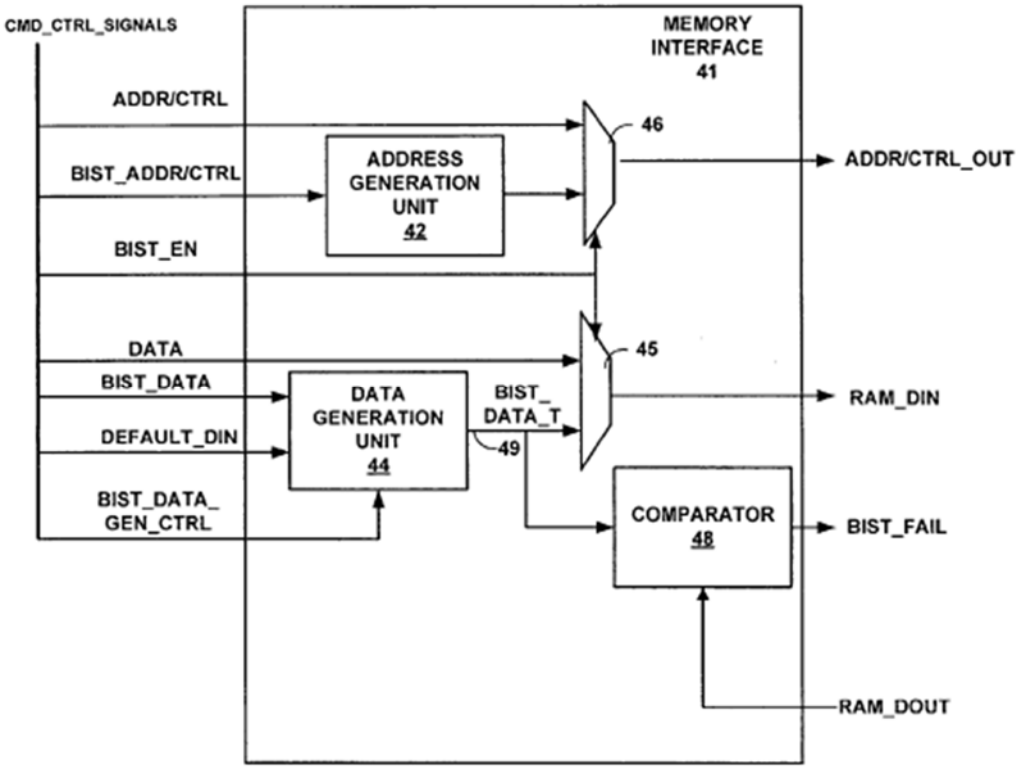
Averbuj describes a hierarchical built-in self-test (BIST) architecture wherein a BIST controller provides centralized, high level control of the

testing of one or more memory modules. Ex. 1003 ¶¶ 7–8. Figure 1 of Averbuj is reproduced below.



Averbuj Figure 1, above, "is a block diagram illustrating an example electronic device 2 . . . includ[ing] a built-in self-test (BIST) controller 4 that provides centralized, high-level control over testing of device blocks 6A through 6N (collectively 'device blocks 6')." *Id.* ¶ 28. "Each of device blocks 6 includes a sequencer 8, and a set of one or more memory interfaces 10 and one or more respective memory modules 12." *Id.* BIST controller 4 provides and communicates test algorithms as a set of commands to sequencers 8 for application to device blocks 6. *Id.* ¶ 29. Sequencers 8, in turn, issue command control signals (CMD_CTRL_SIGNALS) to receiving memory interfaces 10. *Id.* ¶ 43.

Exemplary memory interface 41 is shown in Figure 6, below. *Id.* ¶ 23.

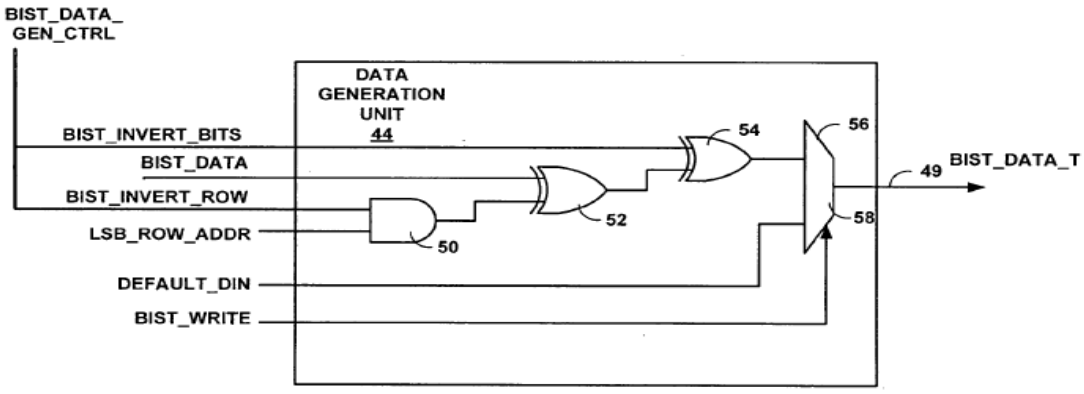


As shown in the Figure 6 embodiment, above, memory interface 41 includes a layer of multiplexers 45, 46. *Id.* ¶ 48. "[U]nder normal operating conditions, BIST enable (BIST_EN) is de-asserted, causing multiplexers 45, 46 to select the address/control signals (ADDR/CTRL) and data signals (DATA), e.g., as provided by a programmable processor." *Id.* "When electronic device 2 is operating in BIST mode, however, the BIST enable signal causes multiplexers 45, 46 to select the BIST address/control signals (BIST_ADDR/CTRL) and the test data provided by a respective higher-level sequencer [, e.g., sequencer 8A]." *Id.*

"[M]emory interface 41 processes the sequential memory operations issued by [] higher-level sequencer [8A], and transforms the data and addresses provided by the sequencer as needed based on the particular physical characteristics of the memory module" (*id.* ¶ 54) using address generation unit 42 and data generation unit 44 (*id.* ¶¶ 49, 51). "For example,

sequencer 8 may request a checkerboard bit pattern that requires columns of data within the memory module to alternate between ones and zeros. Different memory modules 12, however, may be arranged with different row and column configurations." *Id.* ¶ 50. In this case, address generation unit 42 transforms the address provided by sequencer 8 to correspond to the physical configuration of the specified memory module before the address is applied to that memory module. *See id.* ¶¶ 51–52.

An example embodiment of data generation unit 44 is illustrated in Figure 7, reproduced below.



As shown in Figure 7, above, "data generation unit 44 receives a BIST_DATA signal, a default data signal (DEFAULT_DIN) provided by the sequencer 8[, and] . . . a number of control signals in the form of BIST_INVERT_BITS, BIST_INVERT_ROWS, LSB_ROW_ADDR, and BIST_WRITE." *Id.* ¶ 55.

> [S]equencer 8 asserts and deasserts the invert bits signal (BIST_INVERT_ BITS), the invert rows signal (BIST_INVERT_ROWS), and the invert columns signal (not shown) to specify data patterns, such as solid, checkerboard, horizontal and vertical striped data patterns. If neither the invert bits nor the invert rows signals are asserted, then the BIST_DATA signal passes through XOR gates 52, 54 without

> modification. As a result, data generation unit 44 generates the transformed data signal 49, (BIST _DATA_ T) to fill the memory module 12 with the data dictated from the sequencer 8 without modification.

Id. ¶ 56. By contrast, when the BIST_INVERT_BITS signal is asserted, data generation unit 44 automatically inverts the values dictated by the sequencer. *Id.* ¶ 57.

2. Analysis

Petitioner contends the claim 1 limitations (and corresponding claim 16 limitations) of "a control circuit configured generate address and control signals," "data handlers [] configured to generate data," and a "memory system [] configured to test [] one or memory chips" using these generated signals and data are met by Averbuj's sequencers 8 and memory interfaces 10 that generate address/control signals and data, respectively, for testing memory modules 12. Pet. 12. Patent Owner argues: (1) Averbuj's memory interfaces (the alleged data handlers) are not "configured to generate data," as recited in claim 1; (2) Averbuj's sequencer 8 (the alleged control circuit) is not "configured to generate" (claim 1), and does not "generate" (claim 16) the address and control signals used for testing the memory modules 12 (the alleged memory chips); (3) Averbuj's memory interfaces 10 (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot be "operating . . . independently" (claim 16); and (4) Averbuj's sequencer (the alleged control circuit) is not "configured to selectively input" address and control signals to the memory chips, as recited in dependent claim 15. *See* PO Resp. 32–41. With the exception of the above-noted limitation in dependent claim 15, Patent Owner does not dispute directly Petitioner's contentions with respect to the additional limitations

recited in dependent claims 2, 3, 5–8, 11–15, and 17–34, but contends these claims are not anticipated by Averbuj because Petitioner has failed to show Averbuj anticipates independent claims 1 and 16. *See id.* at 41.

a. "one or more data handlers . . . configured to generate data" (claim 1) for testing memory chips

Petitioner relies on paragraphs 43, 48, and 49 of Averbuj in support of its contention that Averbuj's memory interfaces are data handlers that are configured to generate data for testing via data generation unit 44, described as "generat[ing] the exact data (RAM_DIN) applied to the memory inputs" of a memory module during testing. Pet. 15–16 (quoting Ex. 1003 ¶ 49).

Patent Owner argues Petitioner has not shown that Averbuj's memory interfaces 10 (the alleged data handlers) are "configured to generate data" (claim 1) for testing memory modules 12 (the alleged memory chips), because "Petitioner has not shown that the data generation unit 44 in Averbuj is capable of being programmed." PO Resp. 34 ("Averbuj's control signals for data generation (BIST_DATA_GEN_CTRL) are not programmed – they are used to actively generate BIST_DATA_T. Without constant communication over the BIST_DATA_GEN_CTRL lines, BIST_DATA_T is not generated."). Patent Owner's argument is based on its interpretation of "configured to" as "programmed to." *Id.* at 33.

In Section III.B.1, we determined the broadest reasonable interpretation of "configured to," as used in the '501 patent claims, is "designed, adapted, or arranged to," and that one of ordinary skill in the art would understand that programmability is only one way that a component might be designed, adapted, or arranged to perform a function. In other words, lack of programmability is not determinative of whether data generation unit 44 is "configured to generate" data. We are persuaded

Petitioner has shown, by a preponderance of the evidence, that Averbuj's data generation unit 44 is capable of generating data for testing memory modules 12 and, therefore, is necessarily designed, adapted, or arranged to generate data in the manner recited in challenged claim 1.

b. "a control circuit configured to generate address and control signals"(claim 1)/"operating a control circuit to generate address and control signals" (claim 16) for testing memory chips

Patent Owner argues Averbuj's sequencer 8 (the alleged control circuit) does not generate (i.e., produce) the address and control signals used to test memory modules 12 (the alleged memory chips) and, therefore, does not describe "a control circuit configured to generate address and control signals" or "operating a control circuit to generate address and control signals" (claim 16) for testing memory chips as recited in the challenged claim. PO Resp. 35. Patent Owner argues, more specifically, that in Averbuj, the address and control signals used to test memory modules 12 are produced by memory interfaces 10 (the alleged data handlers), not by sequencer 8 (the alleged control circuit). *See id.*

Petitioner references Averbuj paragraphs 37, 43, 48–53, 59–61, and 77–78 in support of its contention that Averbuj discloses a control circuit (sequencer 8) configured to generate address and control signals (CMD_CTRL_SIGNALS) used for testing memory chips (memory modules 12). Pet. 16–17. Petitioner contends "[t]he actual addressing information is produced by the [s]equencer, and the address generation unit 42 merely applies the received addressing information to a given physical memory configuration (*i.e.*, row/column configuration)." Reply 12–13; *see also* Tr. 20:15–18 ("Averbuj teaches us a sequencer generates addresses, provides

them to the memory interface, which may pass them through or may translate them. . . . It generates address and control signals.").

Averbuj discloses that "BIST controller 4 provides and communicates test algorithms to sequencers 8 for application to device blocks 6" (Ex. 1003 ¶ 29), and "[s]equencers 8 interpret" and "control the application of the test algorithms" to the memory modules (*id.* ¶ 30). *See also id.* ¶ 46 ("Sequencers 8 receive the generic BIST commands in accordance with the command protocol, and control the application of the commands by generating and issuing sequences of one or more memory operations for application to a set of respective memory modules 12."). For example, in the exemplary embodiment illustrated in Figure 5, command parser 30 of sequencer 8A processes a command received from BIST controller 4, and extracts one or more parameters from the command. *Id.* ¶¶ 41–42. Command parser 30 passes the extracted parameters to command controller 34, which then issues a sequence of one or more operations to each memory interface 10. *Id.* ¶¶ 42–43.

> In particular, . . . command controller[] 34 sequentially drives the appropriate command control signals (CMD_CTRL_SIGNALS) to carry out each operation of the sequence. The command control signals may include signals to provide a memory address and data to the receiving memory interfaces 10 and to direct the receiving memory interfaces to invert bits, perform read or write operations, invert rows, and the like.

Id. ¶ 43. "Memory interfaces 10 handle specific interface requirements for each of memory modules 12. For example, each of memory interfaces 10 may be designed in accordance with the particular signal interface requirements and physical characteristics of the respective one of memory modules 12." *Id.* ¶ 31.

Averbuj further explains, in connection with the embodiment illustrated in Figure 6, that memory interface 41 "*transforms* the data and addresses provided by the sequencer *as needed* based on the particular physical characteristics of the memory module" (*id.* ¶ 54 (emphasis added)) using address generation unit 42 and data generation unit 44 (*id.* ¶¶ 49, 51). For example, if sequencer 8 asserts an invert rows signal and/or invert columns signal to specify a data pattern, data generation unit 44 inverts values dictated by the sequencer to generate transformed data signal 49 (BIST_DATA_T). *Id.* ¶ 57. If, however, none of the invert signals are asserted, then the BIST_DATA signal passes through XOR gates 52, 54 of data generation unit 44 without modification, and the BIST_DATA_T signal sent to memory module 12 is "the data dictated from the sequencer 8 *without modification*." *Id.* ¶ 56 (emphasis added). Likewise, "in some BIST tests," sequencer 8 may direct memory interface 41 to write BIST data in a row or column first fashion. *Id.* ¶ 51. In such case, address generation unit 42 must transform the address provided by sequencer 8 to conform to the particular row and column configuration of the memory module. *See id.* ¶¶ 51–52. "For example, a 256 bit memory module 12 may be organized as 128 rows and 2 columns, 32 rows by 8 columns, 16 rows by 16 columns, and the like." *Id.* ¶ 50.

Based on the above description in Averbuj, we agree with Patent Owner that Averbuj describes memory interfaces (the alleged data handlers) that are configured to produce address and control signals, and that Averbuj describes producing address and control signals in certain circumstances, e.g., when Averbuj's sequencer (the alleged control circuit) specifies writing data in a particular pattern that requires transformation to conform to a

particular configuration of a memory module. *See* PO Resp. 35. We also agree with Petitioner, however, that Averbuj's memory interfaces are further configured to apply to the memory modules the same address and control signals received from, and produced by, the sequencers for testing (*see* Reply 12–13), e.g., when the sequencer sends signals that can be applied, without modification or transformation (*see* Ex. 1003 ¶ 56), directly to a memory module irrespective of its physical configuration. Thus, Petitioner has shown, by a preponderance of the evidence, that Averbuj's sequencer meets the claim 1 limitation of "a control circuit configured to generate address and control signals" for testing memory chips, and that Averbuj describes "operating a control circuit [(i.e., a sequencer)] to generate address and control signals" used in testing memory chips as recited in claim 16 of the '501 patent.

c. "a plurality of data handlers configured to be operated independently from one [an]other" (claim 1)/ "operating a plurality of data handlers independently from one another" (claim 16)

Petitioner contends Averbuj describes each memory interface 10A–C (the alleged data handlers) of Figure 6 as receiving control and address data from sequencer 8 and using this information to generate address and test data that is specific to its particular memory module 12. Pet. 11. Petitioner argues each memory interface operates independently from the other memory interfaces, because it "processes the sequential memory operations issued by the higher-level sequencer, and transforms the data and addresses provided by the sequencer as needed based on the particular physical characteristics of the memory module." *Id.* (citing Ex. 1003 ¶ 54). In other words, each memory interface operates without being influenced or

controlled by another memory interface because "[a] given memory interface (*i.e.*, data handler) does not communicate with any of the other memory interfaces, or with any of the memory ports used by the other memory interfaces." Reply 13 (citing Ex. 1003 ¶ 39).

Patent Owner argues Averbuj's memory interfaces (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot "operat[e] . . . independently" (claim 16) as recited in the challenged claims because they "are controlled by the same command control signals generated by the invoked command controller via a shared control line. Thus, as shown in Averbuj Fig. 4, the alleged plurality of data handlers cannot be controlled independently." PO Resp. 38. In Section III.A., however, we determined the broadest reasonable interpretation of "operated independently" and "operating . . . independently" as recited in claim 1 and claim 16, respectively, is "operated, or operating, without influence or control by another."

We find Petitioner has shown, by a preponderance of the evidence that Averbuj's memory interfaces (the alleged data handlers) are "configured to be operated" (claim 1) and can perform the function of "operating" (claim 16) without influence or control by another data handler for the reasons stated in the Petition and above. Patent Owner's argument is based on an overly narrow interpretation of "operated independently"/"operating . . . independently" as meaning that the data handlers are configured to be used, or are used "*to independently test* a portion of one or more memory chips" (*id.* at 38), and, therefore, does not persuade us that Petitioner failed to meet its burden of proof.

d. dependent claims 2, 3, 5–8, 11–15, and 17–20

Claim 15 depends from claim 1 and recites: "wherein the control circuit is further configured to selectively input to the address and control ports of the one or more memory chips either the address and control signals from the memory controller of the computer system or the address and control signals from the control circuit." Ex. 1001, 18:5–10. Petitioner contends Averbuj's multiplexer 46 meets these limitations. Pet. 24–25.

Patent Owner argues Averbuj's sequencer 8 (the alleged control circuit) does not selectively input the BIST_ADDR/CTRL signal to memory modules 12 (the alleged memory chips). PO Resp. 40. Rather, sequencer 8 inputs the BIST_ADDR/CTRL signal to address generation unit 42, which is part of memory interface 41 (the alleged data handler), and thereafter to multiplexer 46, i.e., the alleged device that selectively inputs the address and control signals to memory modules 12. *Id.*

Averbuj describes sequencer 8 (the alleged control circuit) as providing a BIST enable signal that causes multiplexer 46 of memory interface 41 (the alleged data handler) to select the BIST address/control signals provided by the sequencer. *See* Ex. 1003 ¶ 48. Averbuj states that "[i]n this manner, the sequencer controls multiplexers 45, 46 of memory interface 41 to selectively isolate the respective memory module, thereby allowing BIST algorithms to be applied to that memory module." *Id.*

We agree with Patent Owner that Petitioner has not explained adequately how Averbuj's sequencer 8 (the alleged control circuit) is "configured to" (i.e., designed, adapted, or arranged to) "selectively input . . . address and control signals" (claim 15) to memory modules 12. Petitioner has not addressed Patent Owner's argument that the device that

selectively inputs address and control signals to memory modules 12 is memory interface 41 (the alleged data handler), not sequencer 8 (the alleged control circuit). *See* Reply 14–15 (arguing "the Sequencer of Averbuj generates the address and control signals since it causes address generation unit 42 to produce the address and control signals received by the memory . . . Alternatively, the sequencer would also be understood to produce the address and control signals received by the memory," but failing to explain how Averbuj's sequencer is "configured to selectively input" (claim 15)).

Patent Owner also contends Petitioner has not met its burden to show dependent claims 2, 3, 5–8, 11–15, and 17–20 are anticipated by Averbuj, because Petitioner has failed to show independent claims 1 and 16, from which these claims depend, are anticipated. PO Resp. 41. We determined above that claims 1 and 16 are anticipated by Averbuj. With respect to claims 2, 3, 5–8, 11–14, and 17–20, we have reviewed the Petition and evidence cited therein, and determine Petitioner has met its burden to show these dependent claims are anticipated by Averbuj. *See* Pet. 17–24.

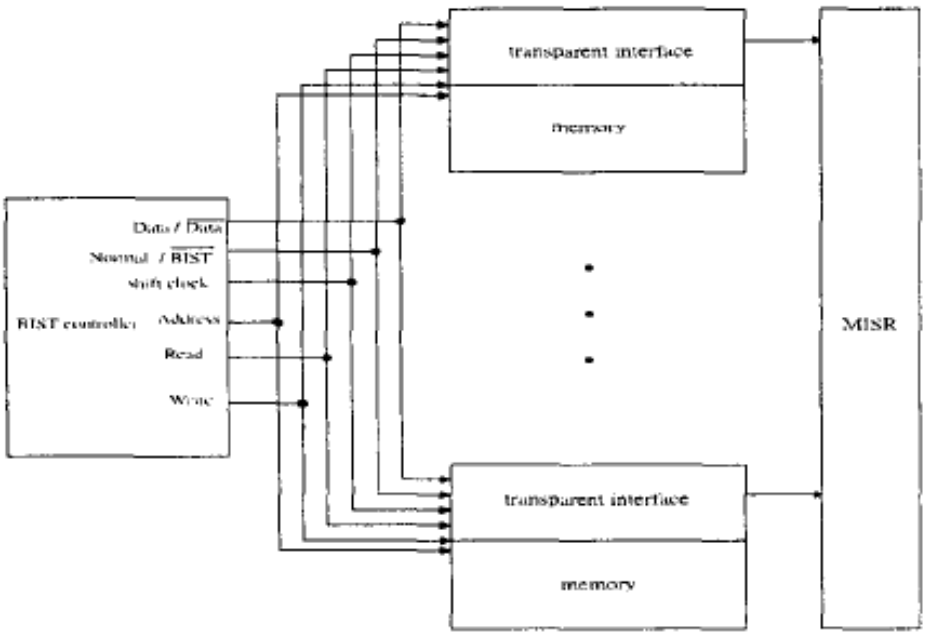
3. Conclusion

Petitioner has met its burden to show, by a preponderance of the evidence, that claims 1–3, 5–8, 11–14, and 16–20 are unpatentable under 35 U.S.C. §102(b) based on Averbuj. Patent Owner has persuaded us that Petitioner failed to meet its burden to establish unpatentability of claim 15 under 35 U.S.C. §102(b) based on Averbuj.

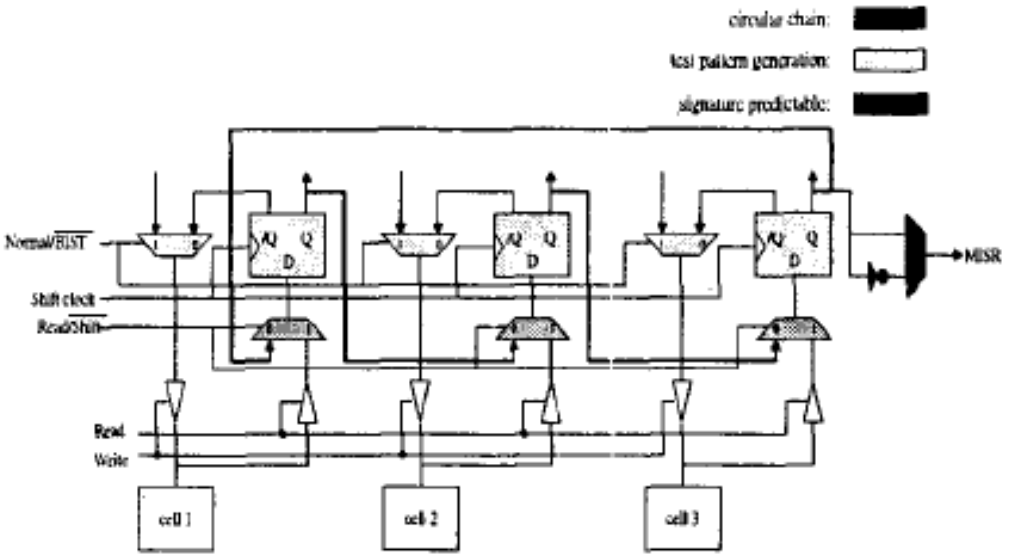
B. Alleged unpatentability of claims 1–5 and 14–16 under § 103(a) based on Huang

1. Huang (Ex. 1004)

Huang describes a transparent built-in self-test (TBIST) interface that is designed to perform testing of multiple embedded memory arrays in the normal mode. Ex. 1004, Abstract. Figure 2 of Huang is reproduced below:



As shown in Figure 2, above, Huang's transparent BIST system scheme includes a BIST controller, transparent test interface, memory arrays and a global multiple input shift register (MISR). *Id.* at 381, Fig. 2. As illustrated in Figure 2, the BIST controller generates Address, and control (Normal/BIST, shift clock, Read, and Write) signals. *Id.* "[A]ll memory modules and interface circuits receive the same test control signals from the transparent BIST controller." *Id.* at 381, col. 2. Figure 1 of Huang is reproduced below:



Huang's Figure 1, above, illustrates the test interface. The test interface "implement[s] the functions of test pattern generation and test response evaluation." *Id.* at 384, col. 2. According to Huang, "the test interface generate[s] test patterns *locally* to avoid test data routing from test controller to each memory array." *Id.* at 381, col. 1. "[T]est patterns are generated by alternatively selecting Q or /Q as an input to each memory cell . . . , so the transition of Q→ /Q and /Q→Q will be exercised in each memory cell. Thus, based on the memory content left by normal operations, new test patterns are generated by complementing each memory word several times." *Id.*

2. Analysis

Petitioner contends Huang's BIST controller, test interfaces, and memory arrays teach or suggest a control circuit, data handlers and memory chips as recited in independent claims 1 and 16. Pet. 36–38. Patent Owner argues: (1) Huang's test interfaces (the alleged data handlers) are not "configured to generate data," and Huang's BIST controller (the alleged

control circuit) is not "configured to generate address and control signals," as recited in claim 1; (2) Huang's test interfaces (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot be "operating . . . independently" (claim 16); and (3) Huang teaches away from "physically separate integrated circuit packages" as recited in dependent claim 4. PO Resp. 41–54. With the exception of the above-noted limitation in dependent claim 4, Patent Owner does not dispute directly Petitioner's contentions with respect to the additional limitations recited in dependent claims 2–5, 14, and 15, but contends these claims are not unpatentable over Huang because Petitioner has failed to show independent claim 1, from which these claims depend, would have been obvious in view of Huang. *See id.* at 54.

a. "control circuit configured to generate address and control signals" and "one or more data handlers . . . configured to generate data" (claim 1)

Petitioner contends Huang Figure 2 "illustrates the generation of address signals by the BIST controller and reception of those signals by the memory devices." Reply 17; *see* Pet. 38–39. Petitioner asserts that Huang Figure 2 also illustrates the generation of "read" and "write," i.e., control signals, by the BIST controller (the alleged control circuit), and Huang Figure 1 illustrates that these control signals are received by the memory arrays (the alleged memory chips). *Id.*; *see* Pet. 38–39. Petitioner contends Huang's transparent interfaces (the alleged data handlers) are described as generating test patterns locally, and, therefore, it logically follows that they are "designed, arranged or adapted to perform the function of data generation." Reply 16; *see* Pet. 37–38.

Patent Owner argues Huang's BIST controller and Huang's transparent interfaces and are not "configured to generate address and control signals" and "data," respectively, as recited in claim 1, because they do not receive signals that can be used for programming. PO Resp. 41–43. Patent Owner's argument is based on an overly narrow interpretation of "configured to generate" as "programmed to generate." *See id.* at 42–43. In Section III.B.1, we determined the broadest reasonable interpretation of "configured to," as used in the '501 patent claims, is "designed, adapted, or arranged to," and that one of ordinary skill in the art would understand that programmability is only one way that a component might be designed, adapted, or arranged to perform a function.

We find that Petitioner has shown, by a preponderance of the evidence, that Huang's BIST controller and transparent interfaces teach or suggest the capability of generating address/control signals and data, respectively, for testing the memory arrays, and, therefore, are designed, adapted, or arranged to generate address/control signals and data in the manner recited in challenged claim 1.

b. "a plurality of data handlers configured to be operated independently from one [an]other" (claim 1)/"operating a plurality of data handlers independently from one another" (claim 16)

Patent Owner argues Huang's transparent interfaces (the alleged data handlers) are not "configured to be operated independently" (claim 1) and cannot "operat[e] . . . independently" (claim 16) as recited in the challenged claims because the transparent interfaces "are (i) specified to receive the exact control signals, and (ii) designed to continuously shift the latched content and output multiple bit streams to the MISR in parallel, and thus are

not able to be used *independently* from each of the other data handlers of the plurality of data handlers in order to *independently* test a portion of one or more memory chips." PO Resp. 43. Patent Owner's arguments are based on an interpretation of "operable independently" as requiring that each data handler is able to be used to independently test a portion of the memory space. *See generally* PO Resp. 43–52. In Section III.A., however, we determined the broadest reasonable interpretation of "operable independently" is "capable of being put into use without influence or control by another."

Petitioner argues that "[w]hen the proper construction of 'operated independently' is applied, it is apparent that each of Huang's transparent memory interfaces (*i.e.*, data handlers) meets this claim limitation, since they each correspond to an associated memory device, and locally generate test data for the associated memory device." Reply 18–19 (citing Pet. 35). Petitioner's argument is persuasive, and Patent Owner has not explained sufficiently why each of Huang's transparent memory interfaces is not capable of being put into use without influence or control by another transparent interface. *See generally*, PO Resp. 43–52; *see also* Reply 19 (citing Ex. 1010, 249:6–11 (wherein Dr. Sechen, when questioned about the operation of the transparent memory interfaces A and B (corresponding to the claimed data handlers), illustrated in Figure 4 of Huang, acknowledged that "when transparent memory interface A is applying a test pattern to memory module A," it does not "affect how transparent memory interface B is applying its test pattern to memory module B")). Therefore, Patent Owner has not refuted Petitioner's prima facie showing that Huang teaches or suggests that its transparent memory interfaces are "configured to be

operated independently" (claim 1) and can "operat[e] . . . independently" (claim 16) as recited in the challenged claims.

c. dependent claims 2–5, 14 and 15

Claim 4 depends from claim 1 and recites: "wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers." Ex. 1001, 16:61–65.

Patent Owner argues Petitioner's challenge as to claim 4 is based on the combination of Huang and Tsern, and that Petitioner has not explained how Huang, alone, discloses or suggests two physically separate integrated circuit packages as claimed. PO Resp. 53. Patent Owner further relies on the following statement in Huang in support of its contention that Huang teaches away from a design in which individual data handlers are in separate integrated circuit packages: "Due to the improvement of VLSI technology, most systems can be condensed into a chip." *Id.* at 53–54 (quoting Ex. 1004, 379).

We agree with Patent Owner that in its Petition, Petitioner does not identify clearly a teaching or suggestion in Huang, alone, of two physically separate integrated circuit packages. *See* Pet. 42 ("[A] POSITA would be motivated to combine Huang and Tsern . . . to supplement the teachings of Huang relating to the desire to have test interfaces generate test patterns locally with Tsern's teachings of efficient ways to incorporate a self-testing memory system within multiple integrated circuits on a printed circuit board."). Petitioner does not argue, until its Reply, that it would have been nothing more than a routine design choice to use physically separate

integrated circuit packages for individual transparent interfaces (the alleged data handlers). In support of its Reply, Petitioner relies exclusively on the second Alpert declaration, wherein Dr. Alpert explains, for the first time, that modification of Huang to achieve the limitations recited in claim 4 would have been within the knowledge and level of skill of the ordinary artisan. *Compare* Ex. 1007 ¶ 156 (testifying "[t]o the extent that this additional claim element may not be disclosed by Huang alone, it is disclosed by Tsern," but failing to explain how the claim 4 limitations are disclosed or suggested by Huang), *with* Ex. 1009 ¶ 64 ("A person of ordinary skill in the art would have understood that an embedded computer system can be implemented as a single integrated circuit or as multiple integrated circuits ("chips") and other components.").

Rule 42.22(a)(2) provides that a petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent." 37 C.F.R. § 42.22(a)(2). Rule 42.23(b) provides that "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response." 37 C.F.R. § 42.23(b). Practice relating to replies is addressed in the Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012):

> While replies can help crystalize issues for decision, a reply that raises a new issue or belatedly presents evidence will not be considered and may be returned. The Board will not attempt to sort proper from improper portions of the reply. Examples of indications that a new issue has been raised in a reply include new evidence necessary to make out a *prima facie* case for the patentability or unpatentability of an original or proposed substitute claim, and new evidence that could have been presented in a prior filing.

"Whether a reply contains arguments or evidence that are outside the scope of a proper reply under 37 C.F.R. § 42.23(b) is left to our determination." *Vibrant Media Inc. v. General Electric Co.*, Case IPR2013-00170, slip op. at 31 (PTAB June 26, 2014) (Paper 56).

In our judgment, Petitioner's arguments and evidence in the Reply are outside the scope of a proper reply because they do more than merely address Patent Owner's argument that Huang teaches away; rather, they attempt to provide a new theory for modifying Huang that was not set forth clearly in the Petition. Consideration by the Board of these arguments in the Reply and evidence presented in Dr. Alpert's second declaration in support thereof would be unfair to Patent Owner. We have, however, reviewed and considered the arguments in the Petition and evidence therein, and are in agreement with Patent Owner that Petitioner has not provided adequate explanation or evidence to support its contention that Huang discloses or suggests the limitations recited in claim 4. Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claim 4 would have been unpatentable over Huang.

Patent Owner also contends Petitioner has not met its burden to show unpatentability of dependent claims 2–5, 14, and 15, because Petitioner has failed to show Huang discloses or suggests all of the limitations of independent claim 1, from which these claims depend. PO Resp. 54. With respect to claims 2, 3, 5, 14, and 15, we have reviewed the Petition and evidence cited therein, and determine Petitioner has met its burden to show these claims are unpatentable as obvious in view of Huang. *See* Pet. 39–41, 43–45.

3. Conclusion

Petitioner has met its burden to show that claims 1–3, 5, and 14–16 are unpatentable under 35 U.S.C. §103(a) based on Huang. Patent Owner has persuaded us that Petitioner failed to meet its burden to establish unpatentability of claim 4 under 35 U.S.C. §103(a) based on Huang.

C. Alleged unpatentability of claims 6–8, 11, and 17–20 under § 103(a) based on Huang and Averbuj

Claim 6 depends indirectly from claim 1 and claim 17 depends directly from claim 16. Claims 6 and 17 and recite: "verifying that data received from the one or more memory locations of the one or more memory chips corresponds to the data" written/transmitted "to the one or more memory locations of the one or more memory chips." Ex. 1001, 17:7–11, 18:29–32. Claims 7 and 8, and claims 18–20 include these limitations by virtue of their dependencies from claims 6 and 17, respectively. Claim 11 depends directly from claim 1 and recites that the data generated by the one or more data handlers comprises "*cyclic* data." *Id.* at 17:33–35. Claim 20 includes a similar limitation. *Id.* at 18:43–45.

With respect to claims 6 and 17, Petitioner contends Averbuj's comparator 48 corresponds to the claimed verification element. *See* Pet. 46 (citing Ex. 1003 ¶ 53; Figs. 6, 10). Petitioner contends one of ordinary skill in the art "would have been motivated to combine the self-testing memory modules disclosed in Huang . . . with the teachings of Averbuj because (among other reasons) adding this additional functionality within the memory interface furthers Huang's desire to perform test data operations locally to avoid excess data routing." Pet. 46 (citing Ex. 1007 ¶¶ 177, 181).

With respect to claims 11 and 20, Petitioner contends Averbuj discloses a data handler (i.e., data generation unit (44)) that "may be

instructed to generate different types of test patterns, including a checkerboard pattern (*i.e.*, cyclic data)." Pet. 49 (citing Ex. 1003 ¶ 49). Petitioner contends one of ordinary skill in the art "would have been motivated to combine the self-testing memory modules disclosed in Huang . . . with Averbuj's disclosure of cyclic test patterns because this is a well-known technique commonly employed in BIST systems. *Id.* at 49 (citing Ex. 1007 ¶¶ 190).

Patent Owner contends Petitioner has not shown how Huang and Averbuj could be combined in the manner claimed. PO Resp. 54. Patent Owner relies on the declaration testimony of Dr. Sechen to establish Huang and Averbuj are incapable of being combined. *Id.* at 55–59 (citing Ex. 2012 ¶¶ 213, 216–217, 219–220, 223, 225–226).

Dr. Sechen testified that "the prior art elements of Averbuj (*i.e.,* cyclic data generation and data verification) that Petitioner cites are incapable of being combined with Huang" (Ex. 2012 ¶ 213) and "[e]ven if it were assumed that [the ordinary artisan] would have attempted to combine Huang and Averbuj, the combination would not have worked for its intended purpose" (*id.* ¶ 220). Dr. Sechen testified that "[t]he *cyclic data* generation in Averbuj is controlled by the sequencer, . . . [which] instructs the data generation unit 44 to generate different types of test patterns, including a checkerboard pattern (i.e., the alleged *cyclic data*)." *Id.* ¶¶ 217–218. Dr. Sechen further testified that "Huang's data generation is tied to the memory contents, and specific data patterns cannot be selected by Averbuj's sequencer;" "Huang's system cannot be instructed to generate different types of test patterns." *Id.* ¶ 219. Dr. Sechen also testified as to why he believed

Averbuj's verification element could not be added to Huang. *See id.* ¶¶ 221–227.

In its Reply, Petitioner contends Patent Owner has "fail[ed] to consider the references as a whole," and has "mistakenly argue[d] that applying specific components of Averbuj with the system of Huang would render the resulting system unfit for its intended purpose." Reply 20–21. Petitioner explains that according to its proposed combination, Huang's Normal/BIST signal would be used to switch between the data outputs of Huang's testing scheme and Averbuj's testing scheme. *Id.* at 21. Petitioner relies on testimony in Dr. Alpert's second declaration in support of its arguments. *See id.* at21–22 (citing Ex. 1009 ¶¶ 68–73).

Dr. Alpert testified that "Dr. Sechen's analysis fails to recognize the motivation for combining Huang and Averbuj because he erroneously conflates various types of testing that are used for different purposes at different times." Ex. 1009 ¶ 68. Dr. Alpert goes on to provide detailed opinion testimony on the understanding of the ordinary artisan with respect to the teachings of Huang and Averbuj, and a detailed explanation of how Huang's system could be modified to include Averbuj's testing system and the motivation of the ordinary artisan to make such combination. *See id.* ¶¶ 69–72. According to Dr. Alpert, "[a] person of ordinary skill in the art would have seen the combination of Averbuj and Huang as choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success." *Id.* ¶ 72.

At oral argument, Patent Owner confirmed its understanding of Petitioner's challenge, as set forth in the Petition, as "starting with Huang and bringing in one element from Averbuj." Tr. 59:24–25. Patent Owner

argued that "Petitioner's reply changes the combination to comprise Averbuj's entire system, not just the cyclic test generation portion." *Id.* at 59:21–23. Patent Owner argued that the Petition includes only conclusory statements of a motivation to combine and fails to explain how Averbuj and Huang are combinable. *See id.* at 60:7–15. Patent Owner also argued Dr. Alpert's second declaration and deposition present new opinions as to how Averbuj and Huang could be combined. *Id.* at 53:3–5. Petitioner contended the challenge, as set forth in the Petition, and Dr. Alpert's first declaration in support thereof, were sufficient because combining Averbuj and Huang was trivial. *See id.* at 26:15–17.

Petitioner contended Dr. Alpert did not express new opinions in his second declaration and deposition, but was merely responding to Dr. Sechen's testimony. *Id.* at 81:17–19; *see also*, *id.* at 82:20–83:3 (wherein Petitioner argued: "[I]n their response, Patent Owner took the position that . . . it was physically incapable to combine Averbuj and Huang. We're entitled to respond to that and show that, in fact, they're not correct, and we did it by saying, listen, we pointed to the multiplexers in the petition, it's super, it's simple to use those multiplexers to combine. . . . [I]t is not incapable. A person of skill in the art could have done that.").

As discussed in Section IV.B.2.c., a petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent" (37 C.F.R. § 42.22(a)(2)), and "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response" (37 C.F.R. § 42.23(b)).

We agree with Patent Owner that the Reply does more than merely respond to or rebut arguments made in Patent Owner's Response; rather, it sets forth a theory that was not presented clearly in the Petition. Patent Owner's position is supported by the fact that Dr. Sechen, whose skill level is at least (and appears to exceed) that of the ordinary artisan, apparently was unable to envision how Huang and Averbuj could be combined. Further, Dr. Alpert's second declaration includes, at a minimum, opinions as to the understanding of the ordinary artisan with respect to the teachings of Huang and Averbuj that were not presented in his first declaration.

In our judgment, consideration by the Board of the above-noted arguments in the Reply and evidence presented in Dr. Alpert's second declaration in support thereof would be improper under 37 C.F.R. § 42.23, and unfair to Patent Owner. We have, however, reviewed and considered the arguments in the Petition and evidence therein, and are in agreement with Patent Owner that Petitioner has not provided adequate explanation or evidence to support its contention that one of ordinary skill in the art would have had a reasonable expectation of success in combining Huang and Averbuj. Accordingly, Petitioner has not met its burden to show, by a preponderance of the evidence, that claims 6–8, 11, and 17–20 would have been unpatentable over Huang and Averbuj.

D. Alleged unpatentability of claims 9 and 10 under 35 U.S.C. § 103(a) based on (1) Huang and JEDEC Standard, and (2) Averbuj and JEDEC Standard

JEDEC Standard "covers Design for Test, Design for Manufacturing and Design for Validation ('DFx') requirements and implementation guidelines for Fully Buffered DIMM technology." Ex. 1006, 1. In its Petition, Petitioner relies on JEDEC Standard for a teaching that "failing

data and [the] corresponding address should be recorded in an error register." Pet. 30, 51 (citing Ex. 1006 § 8.2.4.5). Petitioner argues it would have been obvious to combine the teachings of JEDEC Standard with the BIST architectures disclosed in Averbuj and Huang "for many reasons, including the well known benefit of recording memory errors in a BIST system to enable a failure analysis and determine where the errors are located." *Id.* at 31, 52. Petitioner relies on Dr. Alpert's first Declaration to support its contention that it would have been obvious to modify the respective memory systems of Averbuj and Huang to store addresses and data as taught by JEDEC Standard. Pet. 30–31, 51–52 (citing Ex. 1007 ¶¶ 123–127, 206–209). Dr. Alpert cites column 3, lines 46–49 of the '501 patent in support of his testimony that "the '501 patent acknowledges the relevancy of the JEDEC standard to self-testing memory modules." Ex. 1007 ¶ 124; *see* Ex. 1001, 3:46–49 ("Certain embodiments described herein present a self-testing memory module that includes a control module and a data module which can generate memory addresses and data according to the JEDEC standard memory protocol.").

In its Response, Patent Owner argues that claims 9 and 10 require a system configured to record "failures," but in the system described in JEDEC Standard, testing stops after only one failure is recorded. Resp. 59–60. Patent Owner further argues claims 9 and 10 require an internal tester, but the tester in JEDEC Standard is external to the memory system being tested. *Id.* at 60. In support of these arguments, Patent Owner relies on the declaration testimony of its witness, Dr. Sechen (Exhibit 2012). *Id.* at 59–60 (citing Ex. 2012 ¶¶ 229–32).

Petitioner, in its Reply, argues "[t]he claims are not limited to recording failures during a single test. Instead, the cla[i]ms only require that the data and addresses associated with the failures be stored." Reply 22. Petitioner directs us to the section of JEDEC Standard relied on its Petition, noting there is a subsection on "Multiple Failures" and a description of "a procedure to generate 'a complete data log of all failures' including the address and data associated with the failure." *Id.* (citing Ex. 1006 § 8.2.4.5). In response to Patent Owner's argument that the system in JEDEC Standard uses an external tester, Petitioner, relies on testimony in Dr. Alpert's second Declaration (Ex. 1009). *See* Reply 22–23. Petitioner argues Dr. Sechen's testimony is based on disclosure in JEDEC Standard relating to transparent mode testing (Ex. 1006 § 8.1), which differs from Memory BIST, described in the section of JEDEC Standard cited in the Petition (*id.* at § 8.2). *See id.*; Ex. 1009 ¶ 79 (asserting that the sections of JEDEC Standard relied on by Dr. Sechen, e.g., sections 5.1 and 5.5, relate to transparent mode). Dr. Alpert explains that "Transparent Mode is used during FB-DIMM manufacturing to detect defects in the memory devices, interface, and board assembly using data patterns supplied by an external tester. Memory BIST is used for testing a FB-DIMM in a system at power-on initialization without using test equipment external to the system." Ex. 1009 ¶ 78. During the oral hearing, Patent Owner did not dispute these assertions. *See generally*, Paper 33 (transcript of the oral hearing).

We find that Dr. Sechen's testimony related to JEDEC Standard's description of testing in transparent mode and does not address adequately JEDEC Standard's discussion of Memory BIST, i.e., the section of JEDEC Standard relied on by Petitioner in support of its patentability challenges as

to claims 9 and 10. We also agree with Petitioner that Patent Owner's arguments are not commensurate in scope with claims 9 and 10. We find Petitioner's contentions with respect to the teachings of JEDEC Standard and motivation for modifying the respective systems of Averbuj and Huang are supported by JEDEC Standard, and conclude Petitioner has met its burden to show, by a preponderance of the evidence that claims 9 and 10 are unpatentable over (1) Averbuj and JEDEC Standard, and (2) Huang and JEDEC Standard.

V. CONCLUSION

Petitioner has met its burden to show, by a preponderance of the evidence, unpatentability of: (1) claims 1–3, 5–8, 11–14, and 16–20 under 35 U.S.C. §102(b) based on Averbuj; (2) claims 1–3, 5, and 14–16 under 35 U.S.C. §103(a) based on Huang; (3) claims 9 and 10 under 35 U.S.C. § 103(a) based on Averbuj and JEDEC Standard; and (4) claims 9 and 10 under 35 U.S.C. § 103(a) based on Huang and JEDEC Standard.

Petitioner has failed to meet its burden to establish unpatentability of: (1) claim 15 under 35 U.S.C. §102(b) based on Averbuj; (2) claim 4 under 35 U.S.C. §103(a) based on Huang; and (3) claims 6–8, 11, and 17–20 under 35 U.S.C. §103(a) based on Huang and Averbuj.

VI. ORDER

For the reasons given, it is

ORDERED that claims 1–3 and 5–20 are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Lori A. Gordon
Robert E. Sokohl
STERNE, KESSLER, GOLDSTEIN & FOX
lgordon-PTAB@skgf.com
rsokohl-PTAB@skgf.com

David Cochran
Joseph Sauer
Matthew Johnson
JONES DAY
dcochran@jonesday.com
jmsauer@jonesday.com
mwjohnson@jonesday.com

PATENT OWNER:

Thomas J. Wimbiscus
Scott P. McBride
Gregory C. Schodde
Ronald H. Spuhler
Wayne H. Bradley
McANDREWS, HELD & MALLOY, LTD.
twimbiscus@mcandrews-ip.com
smcbride@mcandrews-ip.com
gschodde@mcandrews-ip.com
rspuhler@mcandrews-ip.com
wbradley@mcandrews-ip.com