UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX INC.
Petitioners

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner

Case IPR2016-00393
Patent 7,193,239

PETITIONERS' NOTICE OF APPEAL

Pursuant to 37 C.F.R § 90.2(a) and 35 U.S.C. § 142, Petitioners Samsung Electronics Co., Ltd., Micron Technology, Inc., and SK hynix Inc. ("Petitioners") hereby respectfully give Notice that they appeal the Patent Trial and Appeal Board's ("Board") Final Written Decision, dated June 23, 2017 (Paper 62), concluding that claims 10-12, 18-20, 60-63, 67, 70-73, and 77 of U.S. Patent No. 7,193,239 have not been shown to be unpatentable to the United States Court of Appeals for the Federal Circuit, and from all underlying orders, decisions, rulings, and opinions that are adverse to Petitioners, including, without limitation, those within the Decision on Institution of *Inter Partes* Review, entered June 30, 2016 (Paper 11).

For the limited purpose of providing the Director with the information requested in 37 C.F.R § 90.2(a)(3)(ii), issues on Petitioners' appeal may include, but are not limited to, the construction of the "substantially flexible" terms, including the Board's construction of these terms; the Board's interpretation of its construction and application of its construction to the prior art; the Board's determination of patentability of claims 10-12, 18-20, 60-63, 67, 70-73, and 77 of U.S. Patent No. 7,193,239 under 35 U.S.C § 103, which is factually incorrect, not supported by law or substantial evidence, was not the result of a logical and rational process, and is incorrect as a matter of law; any findings supporting that determination, including findings regarding motivation to combine and a

reasonable expectation of success; the Board's failure to consider evidence of record fully and properly; the Board's legal errors in undertaking its obviousness analysis; the Board's findings that conflict with the evidence of record and are not supported by substantial evidence; any finding or determination supporting or related to those issues; and any other issues decided adversely to Petitioners in any orders, decisions, rulings and opinions.

Simultaneous with this submission, a copy of the Notice of Appeal is being filed electronically with the Patent Trial and Appeal Board. In addition, a copy of this Notice of Appeal, along with the required docketing fees, are being filed electronically with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Respectfully submitted,

Date: August 24, 2017

/Naveen Modi/

Naveen Modi (Reg. No. 46,224)
Paul Hastings LLP
875 15th St. N.W.
Washington, D.C., 20005
Tel.: 202.551.1700
Fax: 202.551.1705
PH-Samsung-ELM-IPR@paulhastings.com

Attorney for Petitioners

CERTIFICATE OF SERVICE

In accordance with 37 CFR § 90.2(a)(1) and § 104.2, I hereby certify that on August 24, 2017, in addition to being filed electronically through the Board's E2E System, the original version of the foregoing Petitioners' Notice of Appeal was filed by hand on the Director of the United States Patent and Trademark Office, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
Madison Building East, 10B20
600 Dulany Street
Alexandria, VA 22314-5793

CERTIFICATE OF SERVICE

I hereby certify that on August 24, 2017, a true and correct copy of the foregoing Petitioners' Notice of Appeal, along with a copy of the Final Written Decision, was filed electronically with the Clerk's Office of the United States Court of Appeals for the Federal Circuit, at the following address:

United States Court of Appeals for the Federal Circuit
717 Madison Place, N.W., Suite 401
Washington, DC 20005

CERTIFICATE OF SERVICE

Pursuant to 37 CFR § 42.6(e)(1), the undersigned certifies that on August 24, 2017, a complete and entire copy of the Petitioners' Notice of Appeal was provided via email, to the Patent Owner by serving the email correspondence addresses of record as follows:

William A. Meunier
Michael T. Renaud
Mintz, Levin, Cohn, Ferris,
Glovsky and Popeo, P.C.
One Financial Center
Boston, MA 02111

James Carmichael
Carmichael IP, PLLC
8000 Towers Crescent Drive, 13th Floor
Tysons Corner, VA 22182

Email: WAMeunier@mintz.com
Email: mtrenaud@mintz.com
Email: mcnewman@mintz.com
Email: ELM_3DS_IPRs@mintz.com
Email: jim@carmichaelip.com

/Naveen Modi/
Naveen Modi

Trials@uspto.gov
Tel: 571.272.7822

Paper 62
Entered: June 23, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD,
MICRON TECHNOLOGY, INC., and
SK HYNIX, INC.
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00393
Patent 7,193,239 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L. IPPOLITO, *Administrative Patent Judges.*

PERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a); 37 C.F.R. § 42.73

I. INTRODUCTION

A. Procedural History

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition on December 28, 2015, requesting an *inter partes* review of claims 1, 10–13, 18–20, 46, 47, 60–63, 67, 70–73, and 77 of U.S. Patent No. 7,193,239 B2 (Ex. 1001, "the '239 patent" or "the challenged patent"). (Paper 4, "Pet."). Subsequently, Patent Owner filed a Preliminary Response to the Petition on April 19, 2016 (Paper 8).

Based on these submissions, we instituted an *inter partes* review of claims 10−12, 18−20, 60−63, 67, 70−73, and 77 of the '239 patent on the following grounds:

Reference[s]	Basis	Claims Challenged
Bertin '754,[1] Poole,[2] and Leedy '695[3]	§ 103(a)	10−12 and 18−20
Bertin '754, Poole, Bertin '333,[4] and Leedy '695	§ 103(a)	60−63, 67, 70−73, and 77

Paper 11 ("Dec.").

In our Decision to Institute, we did not agree with Patent Owner that the Petitions were barred under 35 U.S.C. § 315(b) because, according to

[1] US Patent No. 5,202,754, issued April 13, 1993 (Ex. 1004, "Bertin '754").
[2] US Patent No. 5,162,251, issued November 10, 1992 (Ex. 1005, "Poole").
[3] US Patent No. 5,354,695, issued October 11, 1994 (Ex. 1006, "Leedy '695").
[4] US Patent No. 5,502,333, issued March 26, 1996 (Ex. 1010, "Bertin '333").

Patent Owner, the Office lacked authority to treat certain days, on which the Office experienced an emergency situation such that many of its online and information technology systems were shut down, as federal holidays. Dec. 4–5. Patent Owner has not raised this issue subsequent to institution in any of the three proceedings.

After institution, Patent Owner filed its Patent Owner Response on October 14, 2016 (Paper 48, "PO Resp.") and Petitioner filed a Reply (Paper 56, "Pet. Reply,").

This *inter partes* review pertains to one member of the "Elm 3DS family" of patents that share a common core of written description but have different claims (continuations and divisional applications of a common parent). Some of the patents being considered in *inter partes* reviews of patents in the Elm 3DS family have expired and others have not (*e.g.* the '617 patent). On April 5, 2017, we held a consolidated hearing in which we heard argument on fourteen *inter partes* reviews (including this one and all having the same panel of Administrative Patent Judges) of Elm 3DS family patents. Although there are differences among these related *inter partes* reviews (different claims and different combinations of prior art references, different reasons to combine, and different arguments regarding reasonable expectation of success) there is a significant overlap of evidentiary records among the reviews. Each decision regarding an Elm 3DS family patent is based on its own evidentiary record. A transcript of the oral hearing is included in the record of each proceeding, including this one. Paper 63 ("Tr."). This Decision relies in part on analysis set forth in the combined Final Written Decision in IPR2016-00386, IPR2016-00387, and IPR2016-00388, particularly with regard to claim construction. In addition, we

analyze, where appropriate, different prior art combinations including reasons to combine and reasonable expectation of success.

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. For the reasons discussed herein, Petitioner has not demonstrated by a preponderance of the evidence that claims 10−12, 18−20, 60−63, 67, 70−73, and 77 of the '239 patent are unpatentable. This Decision is issued concurrently with a Final Written Decision in IPR2016-00388, which also challenges the patentability of claims 10−12, 18−20, 60−63, 67, 70−73, and 77 of the '239 patent.

B. Related Proceedings

As required by 37 C.F.R. § 42.8(b)(2), each party identified various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; *see also* Paper 6 (Patent Owner's Mandatory Notices).

Petitioner indicates that the challenged patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

The challenged patent and related family member patents (collectively "Elm 3DS patents" or "Elm 3DS family") are the subject of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00389 (US Patent No. 8,035,233); IPR2016-00390 (US Patent No. 8,629,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00393

(US Patent 7,193,239) (this case); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00691 (US Patent No. 7,474,004); IPR2016-00703 (US Patent No. 8,791,581) (not instituted); IPR2016-00706 (US Patent No. 8,791,581) (not instituted); IPR2016-00786 (US Patent No. 8,933,570); IPR2016-00708 (US Patent No. 8,907,499); and IPR2016-00770 (US Patent No. 8,907,499).

C. The '239 Patent ("the Challenged Patent")

The '239 patent and the other patents of the Elm 3DS family have in common written description of a "three-dimensional structure (3DS)" for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1*a* is reproduced below.

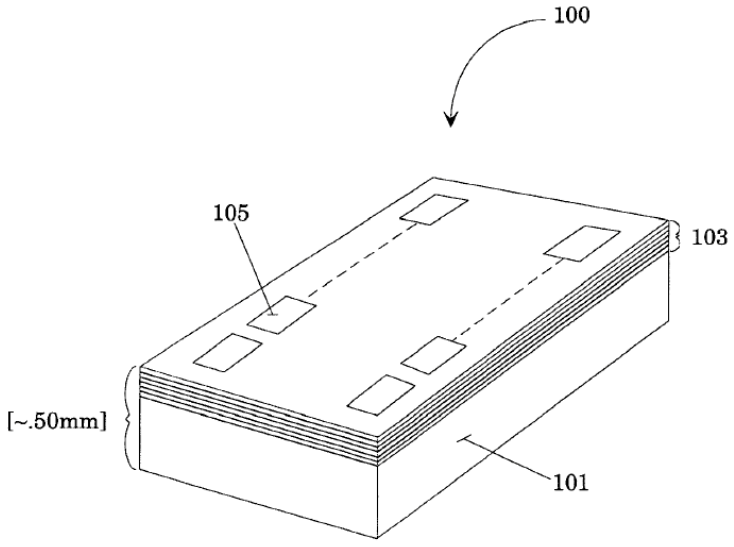


Figure 1*a* is a pictorial view of a 3DS DRAM IC manufactured with Method A or Method B and demonstrating the same physical appearance of I/O bond pads as a conventional IC die. Ex. 1001, 3:47−50.

Figure 1*a* shows 3DS memory device 100 having a stack of integrated circuit layers with a "fine-grain inter-layer vertical interconnect" between all circuit layers. *Id.* at 4:10–13. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:30–32. The written description states that "each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness." *Id.* at 4:35–38. The "thinned (substantially flexible) substrate circuit layers are made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." *Id.* at 8:66–9:4.

Figure 1*b* is reproduced below.

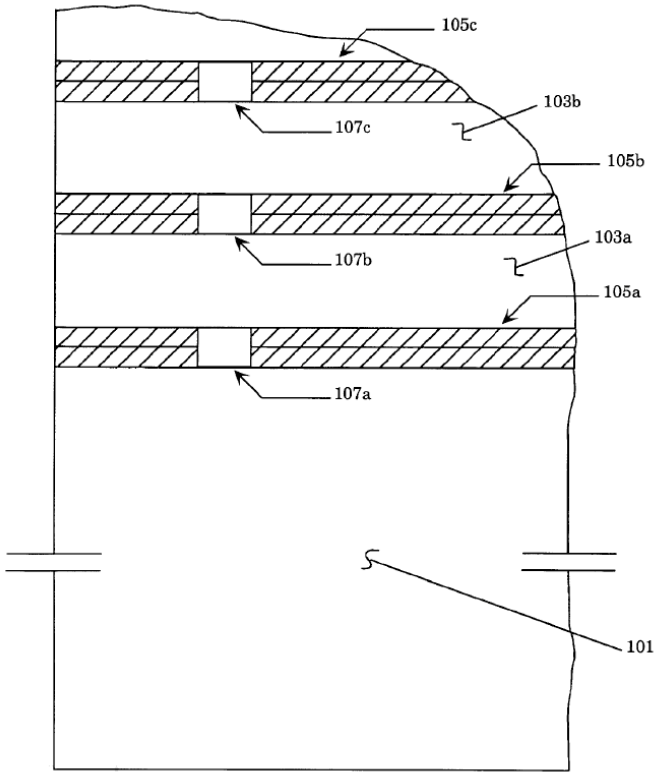


Figure l*b* is a cross-sectional view of a 3DS memory IC showing the metal bonding interconnect between several thinned circuit layers. Ex. 1001, 3:50−52

Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* Fig. 1*b*. The ’239 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4:24–29. Additionally, the ’239 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:28–29.

Further, the ’239 patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through

a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 µm." *Id.* at 4:13–19. The fine-grained inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:19–20.

D. Illustrative Claim

Independent claim 60 of the challenged patent is illustrative of the claimed subject matter:

> 60. An integrated circuit structure comprising:
>
> a plurality of semiconductor dice, each die having an integrated circuit formed thereon, said dice being stacked in layers, wherein at least one of the plurality of dice is *substantially flexible*, and wherein at least one of the plurality of dice has at least one of polycrystalline active circuitry formed thereon, reconfiguration circuitry formed thereon, and passive circuitry formed thereon; and
>
> between adjacent dice, a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice. Emphasis added.

II. ANALYSIS

A. Principles of Claim Construction

For claims of an expired patent, the Board's claim construction analysis is similar to that of a district court. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012); *see, e.g.*, Paper 24 (determining a district court-type claim construction approach following *Phillips* is to be applied during IPR2016-IPR00386, IPR2016-00387, IPR2016-00388, and this proceeding, among others). In this context, claim terms "are generally given their

ordinary and customary meaning" as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (*en banc*). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence, such as expert testimony and dictionary definitions, can be helpful but is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips*, 415 F.3d at 1317. Also, extrinsic evidence is to be considered within the context of the intrinsic evidence. *Id.* A claim term may be construed contrary to its ordinary and customary meaning only "under two circumstances: '(1) when a patentee sets out a definition and acts as [its] own lexicographer, or (2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.'" *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012) (quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *Hill-Rom Svcs, Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014).

In each proceeding addressing an expired patent, we construe the challenged claims according to these principles.

B. Principles of Law Concerning Demonstrating Unpatentability

To prevail in challenging Patent Owner's claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are

unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Petitioner asserts that certain claims of the challenged patents are unpatentable under 35 U.S.C. § 103(a) as obvious over various combinations of references. A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Consideration of the *Graham* factors "helps inform

the ultimate obviousness determination." *Apple v. Samsung Elecs. Co.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016) (en banc).

C. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, 35 U.S.C. § 103 requires us to resolve the level of ordinary skill in the pertinent art at the time of the invention. *Graham,* 383 U.S. at 17. "The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors that may be considered in determining the level of ordinary skill in the art include, but are not limited to, the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *GPAC,* 57 F.3d at 1579. In a given case, one or more factors may predominate. *Id.* Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC v. MGA Entm't, Inc*., 637 F.3d 1314, 1323 (Fed. Cir. 2011) ("A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.").

Petitioner, with support (Ex. 1002) of its declarant Paul D. Franzon, Ph.D., contends that one of ordinary skill in the art at the time of the inventions of the challenge patents "would have had at least a B.S. degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing."

Pet. 5 (citing Ex. 1002 ¶¶ 52–53). According to Dr. Franzon, his testimony as to the level of ordinary skill is based on considering "the types of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field." Ex. 1002 ¶ 53. Patent Owner did not propose expressly a particular level of ordinary skill. *See, e.g.*, *generally* PO Resp. At the oral hearing, however, Petitioner indicated that there did not seem to be any dispute as to the correct level of ordinary skill. Tr. 112:11–14 ("I don't think there was any dispute about whether [Dr. Franzon's proposed level of ordinary skill] was the correct level of skill, although Patent Owner can correct me.").

Having reviewed the prior art asserted in these proceedings (*see*, *e.g.*, Exs. 1004–07, 1009, 2160), we determine that the level of ordinary skill proposed by Petitioner's declarant is consistent with the challenged patent and the referenced prior art, and we adopt Petitioner's proposed definition of the level of ordinary skill in the art for the purposes of the analysis below.

D. Construction of "Substantially Flexible"[5]

For reasons stated in our combined final written decision for IPR2016-00386, IPR2016-00387, and IPR2016-00388, we construe "substantially flexible," in the context of the related patents, as "largely

[5] The term "substantially flexible" is at issue in thirteen of the Elm 3DS *inter partes* reviews: IPR2016-00386 ('672 patent), IPR2016-00387 ('778 patent), IPR2016-00388 ('239 patent), IPR2016-00390 ('542 patent), IPR2016-00391 ('862 patent), IPR2016-00393 ('239 patent), IPR2016-00394 ('617 patent), IPR2016-00395 ('732 patent), IPR2016-00687 ('119 patent), IPR2016-00691 ('004 patent), IPR2016-00708 ('499 patent), IPR2016-00770 ('499 patent), and IPR2016-00786 ('570 patent).

able to bend without breaking." The '239 patent, at issue here, has expired. Paper 19 (Patent Owner indicating the '239 patent would expire on April 4, 2017, which has now passed).

In the challenged claims of the '239 patent, the term "substantially flexible" is used as a modifier of "substrate" (claim 1, from which claim 10 depends, claim 13) and "die" or "dice" (e.g. claims 60 and 70). Each of the challenged claims recites either a "substantially flexible" substrate or die. Thus, Petitioner must establish that the substrate or die of the prior art combinations on which claim challenges are made must provide a substrate or die that is largely able to bend without breaking.

E. Disclosures of Prior Art References

1. Bertin '754

Bertin '754 describes an improvement to a known multichip package shown in its "prior art" Figure 1, reproduced below.

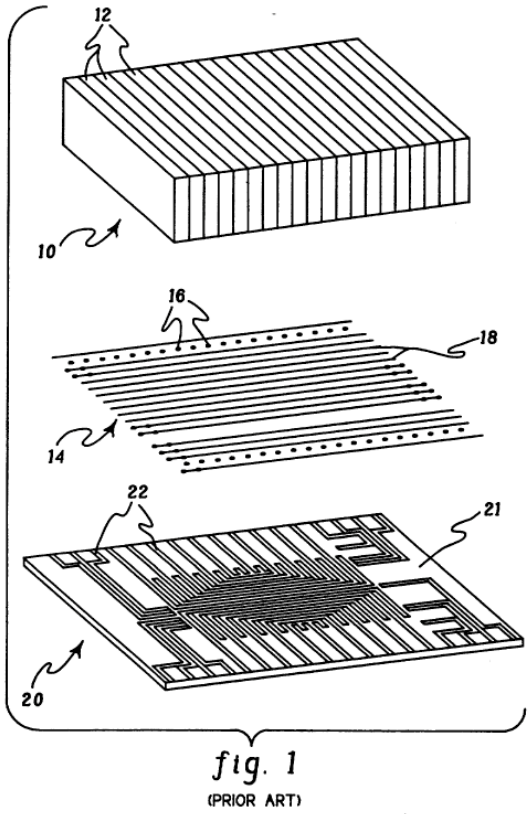
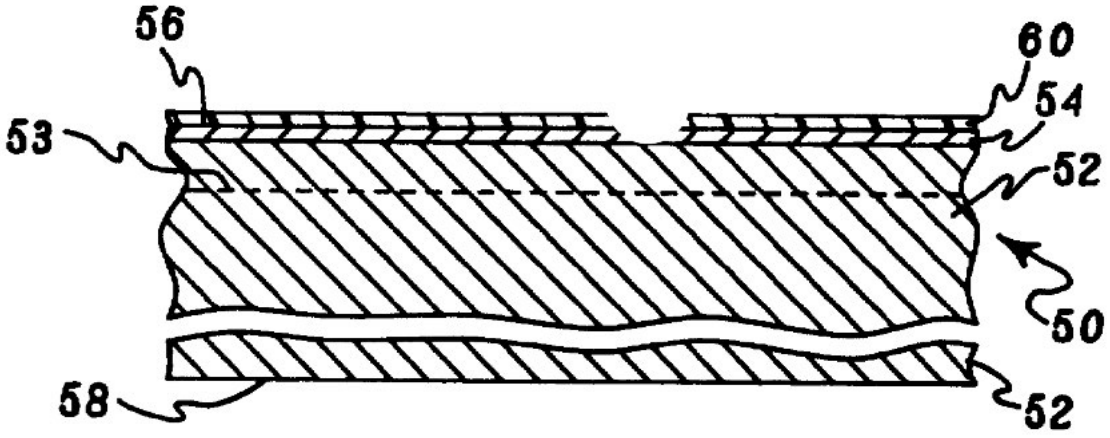


fig. 1
(PRIOR ART)

Figure 1 is an exploded perspective view of a basic prior art multichip package. Ex. 1004, 2:43–44.

Bertin '754 describes "[a] fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips." Ex. 1004, Abstract. Bertin '754 describes a method for fabricating the multichip package by means of a plurality of metallized trenches in the semiconductor chips. Ex. 1004, 1:10–15. Figure 3a is reproduced below.



> Referring first to FIG. 3a, processing begins with a semiconductor device 50 (preferably comprising a wafer) having a substrate 52 and an active layer 54, which is typically positioned at least partially therein. (Layer 54 may be totally or partially defused into substrate 52 and/or partially or totally built up from substrate 52 using *conventional semiconductor processing techniques* known to those skilled in the art.) (emphasis added)

Ex. 1004, 3:50–57. Layer 54 is adjacent to a first, upper planar surface 56 of device 50. *Id.* at 3:57–58. A second, lower planar surface 58 of stacked chip 50 is positioned substantially parallel to first planar surface 56. *Id.* at 3:59–60. Stacked chip 50 includes a semiconductor "substrate 52" (*Id.* at 3:50–4:3), which is thinned to 20 μm or less (*Id.* at 3:25–46, 5:10–22). Bertin '754 further teaches that "dielectric layer 60, for example, SiO_2, is grown over active layer 54 of device 50." *Id.* at 3:60–62, Fig. 3a. Bertin '754 describes vertical electrical interconnections (e.g., metallized trenches) that pass completely through substrates 52. Ex. 1004, Abstract, 1:62–2:12, 4:11–52, Figs. 3c, 3b, 3e, and 3g.

2. Poole

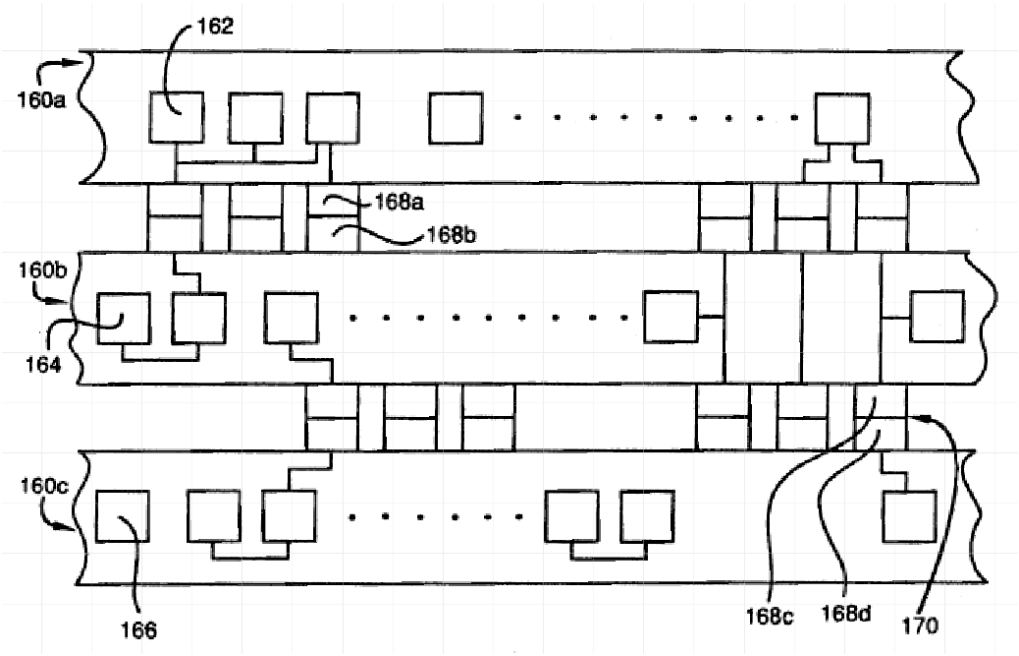
Poole describes techniques for making thinned charge-coupled devices, which are thinned to allow illumination of the backside of the device to improve quantum efficiency and UV spectral response. *Id.* at Abstract, 1:8–11. It describes a two-step method for thinning the backside of a silicon semiconductor substrate that includes integrated circuitry previously formed on the front side. Ex. 1005, Abstract, 1:7–18, and 3:12–6. First, "[t]he bulk silicon is thinned to 75 μm with a 700 micro-grit aluminum oxide abrasive" (*Id.* at 3:21–25; *see also id.* Abstract, 3:33–34, 5:60–6:35), and "is then thinned and polished to 10 μm using 80 nm grit colloidal silica" (*Id.* at 3:21–25; *see also id.* Abstract, 3:33–34, 6:37–46). The result is a surface "almost totally free of work damage." *Id.* at 5:64–65; *see also id.* at 3:44–46.

3. Leedy '695

The Leedy '695 patent, entitled "Membrane Dielectric Isolation (MDI) IC Fabrication," describes a method of fabricating integrated circuits from flexible membranes formed of very thin low stress dielectric materials. Ex. 1006, 1:38–41. Leedy '695 is incorporated by reference into the '239 patent (and the entire Elm 3DS family). Ex. 1001, 2:34–36. It describes fabricating integrated circuits from "flexible membranes" "formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers." *Id.* at Abstract. It describes forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 defines "low stress . . . relative to the silicon dioxide and silicon nitride deposition made

with the Novellus equipment as being less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension." *Id.* at 11:33–37. Leedy '695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing "structurally enhanced low stress dielectric circuit membranes." *Id.* at 11:51–65.

Referring to Figure 8, reproduced below, Leedy '695 discloses a three-dimensional circuit membrane. *Id.* at 4:43.



Leedy '695, Figure 8 shows a three-dimensional circuit membrane. Ex. 1006, 4:42.

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three-dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, and 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, and 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically

between 4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

4. Bertin '333

Bertin '333's Figure 1*a* is reproduced below.

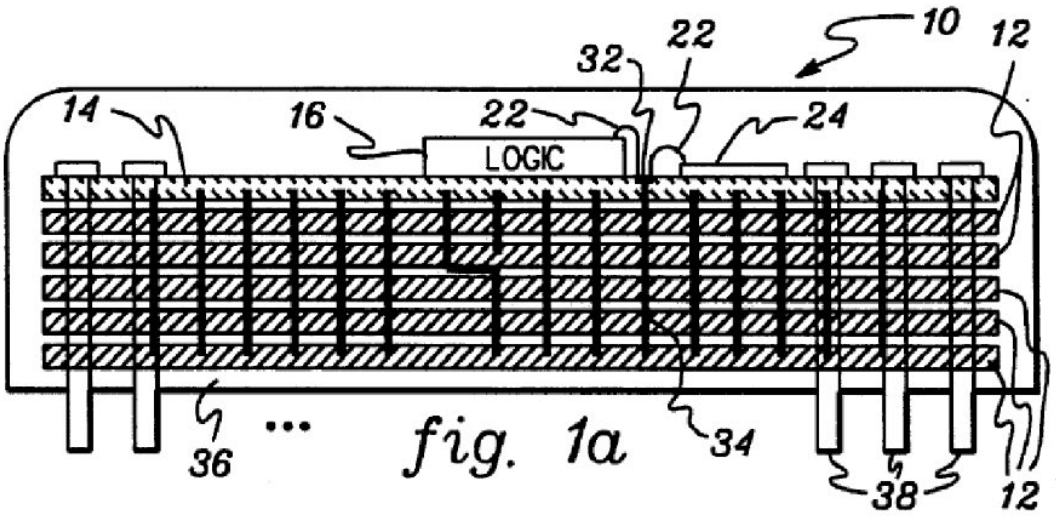


fig. 1a

Bertin '333 describes electronic semiconductor structures having an electrically programmable spare circuit incorporated with a multichip package 10 have lead frame pins 38. Individual failed memory cells in the semiconductor chips 12 of a stack can be functionally replaced by memory cells of the spare memory circuit subsequent to encapsulation and burn-in testing. Ex. 1010, Abstract and 5:37–55. Bertin '333's multichip stack includes a logic/SRAM chip "embedded within an endcap chip" and multiple memory chip layers. *Id.* 5:37–55, 7:59–8:18, 8:50–64, 11:4–42, Figs. 1a, 2, 4a, 5, 9, and 10; *see also* Ex. 1002 ¶¶ 104–107. The logic/SRAM chip includes a sparing circuit 180 that "receives each address signal and continuously compares these signals with the stored failed cell

addresses." *Id.* at 10:15–22; *see also id.* at 5:56–6:2, 8:19–35; and Ex. 1002 ¶ 107. "Metallized via holes" are used to electrically connect the logic/SRAM chip to the other semiconductor chip layers. *Id.* at 11:34–36, 5:56–61, and 8:8–10; *see also* Ex. 1002 ¶¶ 104–107.

F. Asserted Grounds of Obviousness based on Bertin '754, Poole, and Leedy '695

Petitioner contends that claims 10–12 (depending from claim 1) and 18–20 (depending from claim 13) are unpatentable under 35 U.S.C. § 103 as obvious over Bertin '754, Poole, and Leedy '695. Pet. 17–42. In support of its contentions, Petitioner provides citations to the references and to declaration testimony of Dr. Franzon (Ex. 1002). *Id.*

1. Petitioner's Contentions

Petitioner relies on Bertin '754 as describing most of the limitations of the challenged claims arguing, for example, that "Bertin teaches or suggests all but a few features recited in the Challenged Claims, as construed by Petitioner" and noting that silicon substrate 52, having exposed surface 58, is thinned by a conventional wet etching process. Pet. 21 (citing Ex. 1004 at 5:10–22, Fig. 3f).

Given Petitioner's proffered construction of "substantially flexible" (which we did not adopt), Petitioner argues that it would have been obvious to replace Bertin '754's wet etching process with Poole's two-step thinning process. Pet. 22 (citing Ex. 1002 ¶¶ 110–111, 116), 27. Poole's two-step thinning process includes a grinding (or lapping) step followed by a chemical mechanical polishing ("CMP"). *Id.* at 28.

Petitioner acknowledges that Bertin '754 does not explicitly disclose that the dielectric layer 60, interconnect insulator, or oxide/metallization layer 63 constitutes a "low stress" dielectric characterized by a low tensile stress. Pet. 35 (citing Ex. 1002 ¶ 112). However, Petitioner argues that it would have been obvious to one of ordinary skill to modify the fabrication processes of Bertin '754 to utilize the Leedy '695 low tensile stress dielectric (for example, to replace dielectric layer 60, interconnect insulators, and oxide/metallization layer 63). *Id.* (citing Ex. 1002 ¶¶ 98–102).

Petitioner argues a motivation to combine based on Bertin '754 and Leedy '695 both being directed to the improvement of integrated circuits and both recognizing the central role the fabrication process plays in facilitating this improvement. Pet. 35–36 (citing Ex. 1004 at 1:7–2:31; Ex. 1006 at 1:38–67, 3:56–4:13). Thus, according to Petitioner, one of ordinary skill would have been "encouraged" to look to the teachings in Leedy '695 to improve Bertin '754. Pet. 36.

Petitioner also argues express motivation in Leedy '695 to incorporate its low tensile stress dielectric material into other devices, explaining that "otherwise surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." Pet. 36 (citing Ex. 1006 at 5:63–6:5; Ex. 1002 ¶¶ 98–102).

According to Petitioner, it would have been obvious to one of ordinary skill in the art to "simply substitute" Leedy '695's low tensile stress dielectric material for the dielectrics disclosed in Bertin '754. Pet. 37.

2. Patent Owner Contentions

Patent Owner argues that Petitioner has not established that Bertin '754 has a substantially flexible substrate. PO Resp. 48. Given our preliminary construction of "substantially flexible" (see Section II, D)), Patent Owner argues that Poole's two-step grinding process would not have been used by one of ordinary skill in the Bertin '754 structure. PO Resp. 49.

Patent Owner argues that we should adopt its proposed construction of "substantially flexible" (which we have done) and that Petitioner has not established that Bertin '754 has a "substantially flexible" substrate and that it would not have been obvious to render Bertin '754's substrate "substantially flexible" by combining the teachings of Poole and Leedy '695. PO Resp. 50–57.

Patent Owner also argues that one of ordinary skill would not have substituted the Leedy '695 dielectric for the Bertin '754 dielectric. In support of its argument against dielectric substitution, Patent Owner presents a tutorial explaining the complexity of semiconductor fabrication, with numerous citations to the prior art references and declaration testimony of its expert, Alexander D. Glew, Ph.D. (Ex. 2166).

The tutorial stresses the detailed planning and decisions required to establish a fabrication process for a semiconductor integrated circuit. PO Resp. 3–30. It explains four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called "wafers." PO Resp. 6 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). The tutorial also explains

different techniques for producing and layering dielectrics (PO Resp. 16 – 30), including growing dielectrics using thermal oxidation (PO Resp. 18 – 19), depositing dielectrics (PO Resp. 19), and a comparison of thermal CVD (PO Resp. 20) with Plasma Enhanced CVD (PO Resp. 21); different kinds and uses of dielectrics (PO Resp. 22–29) including field oxide dielectrics, gate oxide dielectrics, pre-metal dielectrics, intermetal dielectrics, and passivation dielectrics.

3. "Substantially Flexible" Claim Requirement

Claims 10–12 each require a "substantially flexible substrate." Claims 18–20 require a "substantially flexible monolithic monocrystalline semiconductor substrate." Claims 60–63, 67, 70–73, and 77 each require a "substantially flexible die/dice." For reasons set forth below, based on our construction of "substantially flexible," Petitioner has not established that one of ordinary skill would have combined the teachings of Bertin '754, Poole, and Leedy '695 to meet the "substantially flexible" requirement of each of the challenged claims.

Petitioner argues that Bertin '754 discloses a semiconductor substrate that has been thinned to less than 50 μm and therefore discloses a substantially flexible semiconductor substrate as required by the claims. A preponderance of the evidence establishes, however, that, in the context of semiconductor fabrication, mere thinning is not the same as flexibility—being able to bend without breaking. We find that "thinning" does not equate to "flexibility" because it does not account for materials and the processing steps acting on those materials.

The Examiner, during the prosecution history of the now-abandoned '652 application, agreed that flexibility is not the equivalent of mere

thinning. Ex. 2168, 4 (The Examiner indicating that "Bertin also fails to specifically teach wherein at least one of the first and second circuit layers is substantially flexible."); PO Resp. 35 (Patent Owner indicating that the "Examiner agreed that flexibility is not the equivalent of mere thinning." (quoting Ex. 2168, 4)); Tr. 24:23–25:1 (Petitioner's counsel agreeing with Patent Owner's characterization that flexibility is not the equivalent of mere thinning).

Petitioner's expert, Dr. Franzon, testified that the flexibility of a semiconductor substrate depends on a number of factors, only one of which is the physical dimensions of the substrate—width and thickness. Ex. 1002 ¶ 71. Specifically, Dr. Franzon stated:

> In the context of semiconductor processing, the flexibility of a semiconductor substrate depends on a number of factors, including, for example, the type of semiconductor substrate (e.g., while silicon and gallium arsenide are both semiconductors, they have different elastic moduli), the crystal orientation of the material (e.g., {100} and {111} silicon wafers have different elastic moduli), and the physical dimensions of the substrate (e.g., width and thickness).

Ex. 1002 ¶ 71; *see also* Tr. 33:8–24 (Patent Owner's counsel at oral hearing discussing Dr. Franzon's testimony about the factors on which flexibility of a semiconductor substrate depends); Tr. 64:16–65:11 (Petitioner's counsel responding to Patent Owner's argument about Dr. Franzon's testimony regarding the various factors that would be considered to determine whether something is flexible).

Petitioner's counsel asserted at the oral hearing that the asserted art shows bendability in addition to thinning because the asserted "prior [art] mirrors the prior [preferred] embodiment." Tr. 175:21–176:2. Petitioner,

however, does not point to sufficient evidence to support its position that prior art mirrors the preferred embodiment in the challenged patent. *See generally* Tr. 175:13–180:16. For example, Petitioner contends that Dr. Franzon's testimony that the limitations are met by the prior art supports its position. Tr. 178:20–22 (Asking "is there any evidence of record that any of the combinations that you propose would be the same as the preferred embodiment"?); Tr. 180:8–10 (Petitioner's counsel responding that "[i]t's Dr. Franzon's testimony that those limitations are met by the prior art, and it's the prior art itself, lining up with the claims"). Dr. Franzon, however, testifies that he was given Petitioner's proposed construction of "a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed" and he "applied Petitioner's construction in [his] analysis." Ex. 1002 ¶ 72.

Petitioner's counsel at the oral hearing confirmed that Petitioner's Reply to Patent Owner's claim construction position is that "first and foremost their claim construction is improper because it is indefinite, so in drafting the reply, . . . we couldn't figure out how to apply their construction to the prior art, so the claim construction portion of the reply explains why their construction is incorrect." Tr. 176:7–12.

Patent Owner argues that Bertin '754 does not disclose or even suggest a substantially flexible substrate, die, or dice; and that Petitioner does not argue that it does. PO Resp. 48. Petitioner relies upon Bertin '754, as modified by Poole, as disclosing a substrate that has been thinned, regardless of whether the substrate or the resulting circuit is actually flexible. Per our construction of "substantially flexible," we do not equate "thinned" with "substantially flexible." Common sense also supports a

conclusion that thickness is not the only factor that determines whether a material is flexible. After all, a thicker piece of rubber is more flexible than a thinner potato chip. Without comparing and explaining particular materials, conditions and fabrication steps, relying upon thinness alone does not satisfy the claim requirement of "substantially flexible."

Petitioner's reliance on Poole does not overcome this deficiency. Petitioner suggests applying Poole's two-step thinning process to Bertin '754 to achieve the "predictable result of a thin substrate with a planar surface having minimal defects which is desired in Bertin '754 to facilitate the formation of reliable vertical interconnects and bonds between substrates." Pet. 23. Petitioner has not made a sufficient case for why one of ordinary skill would have applied Poole's process to the structures of Bertin '754. Further, Petitioner has not made the case for why doing so would have resulted in a substrate that satisfies the "substantially flexible" claim requirement.

We therefore determine that Petitioner has not demonstrated by a preponderance of the evidence that Bertin '754 utilizes a "substantially flexible" substrate or die/dice. Petitioner has not demonstrated by a preponderance of the evidence a reason to combine Bertin '754, Poole, and Leedy '695 and a reasonable expectation of success in establishing a "substantially flexible" substrate or die/dice, as required by the claims.

This reason alone is sufficient for us to conclude that Petitioner does not satisfy its burden to establish that claims 10–12 and 18–20 are unpatentable. However, as set forth below, there is an additional independent and separate reason for our decision regarding unpatentability of these claims.

4. Low Tensile Stress Dielectric Substitution

For reasons set forth below, we also conclude that the record does not support Petitioner's contention that one of ordinary skill would have utilized the Leedy '695 dielectric in Bertin '754. The Petition falls short in explaining why one of ordinary skill would have implemented the teachings of Leedy '695 in Bertin '754 and how that implementation would have been carried out.

When an obviousness determination relies on the combination of two or more references, as here, there must be some suggestion or motivation to combine the references and a reasonable expectation of success. *KSR Int'l v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). It is axiomatic that an asserted ground of obviousness must be supported by articulated reasoning with rational underpinning. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *see KSR*, 550 U.S. at 418 (quoting *In re Kahn*). Mere conclusory statements are not sufficient. *Kahn*, 441 F.3d at 988. Furthermore, "[c]are must be taken to avoid hindsight reconstruction by using 'the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.'" *Grain Processing Corp. v. Am. Maize-Prods. Co.*, 840 F.2d 902, 907 (Fed. Cir. 1988) (quoting *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1012 (Fed. Cir. 1983)).

We discuss the fabrication process steps of Bertin '754 and Leedy '695 in the context of determining whether the claimed product would have been obvious. *See Nike v. Adidas*, 812 F.3d 1326, 1336 (Fed. Cir. 2016) (analyzing three processes of producing a claimed product to determine obviousness of the product). Petitioner's combination relies on

Bertin ’754’s dielectric layer 60 that has interconnect insulators, which do not have the required tensile stress, in combination with the “disclosure of Leedy ’695.

Petitioner contends that “it would have been obvious to one of ordinary skill . . . to modify the processes and device in Bertin ’754 such that each of the dielectric layer 60, the interconnect insulators, or oxide/metallization layer 63 constitutes a dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, based on the disclosure of Leedy ’695.” Pet. 35 (citing Ex. 1002 ¶¶ 98–102).

Petitioner provides several purported reasons for combining the references. First, Petitioner contends that “[o]ne of ordinary skill would have looked to Leedy ’695 to improve the teachings of Bertin [’754]” because “both are directed to the improvement of [integrated circuits] and recognize the central role the fabrication process plays in facilitating this improvement” and “[b]oth disclosures seek to achieve high density [integrated circuits] (e.g., 3D [integrated circuits]).” Pet. 35–36 (citing Ex. 1004, 1:7–2:31; Ex. 1006, Abstract, 1:38–1:67, 2:9–2:14, 3:56–4:13, 45:49–45:49, 47:31–47:33). Petitioner cites Dr. Franzon’s conclusion for support. Pet. 36 (citing Ex. 1002 ¶¶ 100–102).

Second, Petitioner contends that “Leedy ’695 also provides express motivations for modifying Bertin ’754’s process and device to incorporate Leedy ’695’s low tensile stress dielectric material.” Pet. 36. Specifically, Petitioner contends:

> Leedy ’695 explains that low tensile stress is important because otherwise “surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free

> standing membrane." Ex. 1006 at 5:63–6:5; Ex. 1002 at ¶98. As discussed above, Leedy '695 describes processes for depositing silicon oxide or silicon nitride dielectric material, preferably having a tensile stress of 1 x 10^7 dynes/cm^2. Ex. 1006 at 11:33–37; Ex. 1002 at ¶99. Leedy '695 explains that the described low tensile stress dielectrics can advantageously be used to insulate circuit devices and interconnect metallization, while at the same time increasing structural integrity and durability. Ex. 1006 at Abstract, 1:53–62, 2:9–31, 2:66–3:3, 3:56–4:13, 30:36–42, 45:49–46:26, 46:52–47:33, Figs. 32a–32d. Leedy '695 also explains that such dielectrics advantageously have lower stress than thermally grown oxides, like those in Bertin. *Id.* at 6:30–33.

Pet. 36–37.

Third, Petitioner contends that "one of ordinary skill would have expected success combining the teaching of Bertin and Leedy '695" because PECVD was a commonly available Pet. 38.

Patent Owner opposes, relying on declaration testimony from Dr. Glew. Patent Owner contends one of ordinary skill in the art would not have been motivated to use the Leedy '695 dielectric but rather would understand that the Leedy '695 dielectric could not be used in the manner proposed by Petitioner. PO Resp. 3. More specifically, Patent Owner contends that Petitioner overlooks that "[d]ielectrics have different requirements, characteristics, and behaviors depending on how they are being used and how they are made, so that one cannot simply replace another." PO Resp. 2. Patent Owner further contends that Leedy '695's dielectric, because it is made by plasma-enhanced chemical vapor deposition (or PECVD), "cannot be deposited on silicon without damaging it, does not meet the required purity level [of Bertin '754's process] and cannot withstand high temperatures without changing its form." PO Resp. 3.

In its Reply, Petitioner contends, without support of expert testimony or citation to law, that "the lack of disclosure of 'tensile' dielectrics or how to make a [low tensile stress dielectric], aside from incorporating a § 102(b) reference, indicates that it was "trivial" to substitute Leedy '695's [low tensile stress dielectrics] in place of other dielectrics." Pet. Reply 2. We disagree with Petitioner—one does not necessarily follow from the other.

Similarly, we disagree with Petitioner's conclusory position that the technical obstacles to incorporating Leedy '695's dielectric into prior art integrated circuits (such as Bertin's) and not addressed by Leedy '695 are not "real or the challenged claims would not be enabled." Pet. Reply 2–3. Leedy '695 sets forth sixty-four pages of figures and more than forty-six columns of text to describe his membrane dielectric isolation integrated circuit fabrication techniques and does not also need to explain in detail specific ways to substitute its techniques for those in a conventional integrated circuit fabrication process. Petitioner's position is based on attorney argument. Accordingly, we determine Petitioner's conclusory assertions in its Reply are insufficient to overcome Patent Owner's well-reasoned and supported arguments.

Nor are we persuaded that the parties' dispute over front-end and back-end use of dielectrics needs to be decided to resolve the dispute over whether Petitioner's contentions regarding reason to combine and expected success are sufficient to support its conclusion of obviousness. *Compare* PO Resp. 22–29, *with* Pet. Reply 15. Even if we were to assume that the Leedy '695 dielectrics could be used in either front-end or back-end processes (as Petitioner contends), this does not explain, as Petitioner must, why one of ordinary skill in the art would have combined the references in the manner

proposed by Petitioner to arrive at the claimed invention and would have had a reasonable expectation of success in doing so. The mere capability of combining Leedy '695's plasma-enhanced chemical vapor deposition process to deposit low tensile stress dielectric material in place of Bertin '754's thermal oxidation process of growing dielectric material is not dispositive. Rather, Petitioner must also demonstrate by a preponderance of the evidence that one of ordinary skill in the art would have had a reason to do so. *See, e.g.*, *In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) ("In the context of the claimed rowing machine, however, the mere capability of pulling the handles is not the inquiry that the Board should have made; it should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed rowing machine.").

Petitioner argues why one of ordinary skill in the art would have been motivated to combine Bertin '754 with Leedy '695 to achieve the purported claimed invention. Patent Owner provides well-reasoned argument based on testimonial and prior art reference evidence identifying shortcomings in Petitioner's position. There is evidence from both sides regarding the presence or absence of a reason to combine Bertin '754 and Leedy '695 in the manner proposed by Petitioner to arrive at the claimed invention.

Petitioner has the burden to show, by a preponderance of the evidence, a reason why one of ordinary skill in the art would have combined the prior art references to arrive at the invention and why one of ordinary skill in the art would have had reasonable expectation of success of combining the references to meet the limitations of the claimed invention. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) ("The reasonable expectation of success requirement refers

to the likelihood of success in combining the references to meet the limitations of the claimed invention. . . . [O]ne must have a motivation to combine [the references] accompanied by a reasonable expectation of achieving what is claimed in the patent-at-issue."). 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [inter partes review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")).

Without question, fabrication of integrated circuits is complex technology. No less than four prior art text books, ranging from 600 pages to nearly 850 pages and describing the fabrication of integrated circuits, have been provided as background references, principally in support of the declaration testimony of Dr. Glew, Patent Owner's expert. These include Ex. 1040, Ex. 2146, Ex. 2158, Ex. 2162, and Ex. 2169.

We understand from Patent Owner's tutorial on semiconductor fabrication (*see* Patent Owner's Contentions, Section II.F.2, above) and from testimony of both side's Declarants and reference citations, that a typical fabrication of a semiconductor integrated circuit may include thousands of process steps. Ex. 2166 ¶ 30.

Both experts agree that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties. For example, Dr. Franzon testifies:

Q. Do the different methods result in different properties of the

dielectrics?

A. Yes.

Ex. 2164 (Dr. Franzon deposition transcript), 69:17–19; *see, e.g.*, Ex. 2166 (Dr. Glew's declaration) ¶ 139 (Identifying eighteen properties[6] of dielectrics; testifying that one of ordinary skill in the art would consider many of those factors when choosing a dielectric); *see also* PO Resp. 59–60 (discussing Dr. Franzon's and Dr. Glew's testimony). Notably, Dr. Franzon acknowledges dielectric properties that should be considered when selecting a dielectric: intrinsic stress, coefficient of thermal expansion, dielectric constant, deposition rate, etch rate, susceptibility to impurities, and propensity to cause pinholes. Ex. 2164 (Dr. Franzon deposition transcript), 59:25–60:2, 61:10–13, 79:25–80:3, 91:8–12. Dr. Franzon further testifies that intrinsic stress, in turn, depends on a number of factors, such as deposition rate, deposition temperature, pressure in the deposition chamber, incorporation of impurities during growth, grain structure from fabrication process defects. Ex. 2164, 63:1–7 (Dr. Franzon deposition transcript citing his report (Ex. 1022 ¶ 24)). Moreover, Dr. Franzon testifies that "[t]here is likely quite a long list of factors that go into choosing between them

[6] Dr. Glew identifies the following properties of dielectrics: dielectric constant, breakdown of field strength, leakage, surface conductance, moisture absorption or permeability to moisture, stress, adhesion to aluminum, adhesion to other dielectric layers, stability, etch rate, permeability to hydrogen, amount of incorporated electrical charge or dipoles, amount of impurities, quality of step coverage, thickness and uniformity of the film, ability to provide good doped uniformity across a wafer, defect density, and amount of residual constituents that "outgas" during later processing. Ex. 2166 ¶ 139.

[dielectrics], and an engineer would weigh those using his knowledge and skills." Ex. 2164, 78:23–79:1. Also, Dr. Franzon testifies:

> Q. In your opinion, in Table 7, which of those are the best dielectric for use in semiconductor technology? . . .
>
> THE WITNESS: There are many factors that would go into that choice, including stress and other factors.

Ex. 2164, 77:13–24. Dr. Franzon further testifies that the variety of factors that an engineer would consider "can be very context specific" and that "factors matter to different degrees, depending on the application, the materials, the other materials, the overall process flow, the overall process integration, the recipes, and so forth." Ex. 2164, 109:19–110:3. Furthermore, Dr. Franzon testifies that "[t]here is no single most important characteristic" of a dielectric in semiconductor technology. Ex. 2164, 65:15–20.

Yet, in marked contrast to Dr. Franzon's testimony concerning the variety of factors that an engineer would consider when selecting a dielectric for use in semiconductor fabrication and that there is no single most important characteristic of a dielectric in semiconductor technology, Petitioner contends that "[i]t would have been obvious to one of ordinary skill in the art to modify Bertin such that each of the dielectric layer 60 and the interconnect insulators constitutes a dielectric characterized by [a particular tensile stress] based on the disclosure of Leedy '695" (Pet. 17). Petitioner's contention seems to suggest that the characteristic of tensile stress is the most important characteristic of a dielectric to be considered, which is counter to its expert's testimony.

In addition, in contrast to Dr. Franzon's deposition testimony

concerning the variety of context-specific factors that an engineer would consider when selecting a dielectric, Dr. Franzon's declaration testimony does not provide an analysis of such factors. Rather, Dr. Franzon's testimony summarizes the disclosure of Leedy '695 and the known use and advantage of using plasma-enhanced chemical vapor deposition techniques. Ex. 1002 ¶¶ 91–102.

Furthermore, Dr. Franzon's testimony does not expressly support Petitioner's specific proposed substitution of Bertin '754's dielectric layers (such as layer 60). Pet. 17 (citing Ex. 1002 ¶¶ 91–102). Rather, Dr. Franzon's testimony is more general—"a person of ordinary skill in the art would have been motivated by these advantages [identified in Leedy '695 and an advantage of using plasma-enhanced chemical vapor deposition techniques] to implement the low-stress dielectric deposition techniques disclosed by Leedy '695 to the stacked integrated circuit structures disclosed in each of Bertin '754 (alone or in combination with Poole) and Yu." Ex. 1002 ¶ 100 (emphasis added).

In general, we weigh the testimony of Patent Owner's declarant, Dr. Glew, concerning the reasons why one of ordinary skill in the art would not have reason to combine the references in the manner proposed by Petitioner more heavily than Dr. Franzon's declaration testimony. Dr. Franzon's testimony, which is cited but not discussed by Petitioner, is that plasma-enhanced chemical vapor deposition was commonly available and was known to "advantageously provide" various benefits. Dr. Franzon's testimony cites the general advantages of low tensile stress dielectrics in fabricating integrated circuits and the benefits of using a plasma-enhanced chemical vapor deposition process (as Leedy '695 uses). *See* Ex. 1002

¶¶ 98, 99, 102; Pet. 17–20 (citing Ex. 1002 ¶¶ 91–102). Neither Dr. Franzon nor Petitioner adequately addresses how one of ordinary skill in the art would specifically use Leedy '695's fabrication process to make Bertin '754's integrated circuit having Leedy '695's low tensile stress dielectric as layer 60 and insulated interconnecting structures. Here, Petitioner proposes a combination of references that purports to show the claimed invention would have been obvious seemingly on the basis that low tensile stress dielectrics have advantages.

In contrast, Patent Owner relies on Dr. Glew's testimony, which is specific as to reasons why one of ordinary skill in the art would not have combined Leedy '695's fabrication process to make Bertin '754's integrated circuit having Leedy '695's low tensile stress dielectric as layer 60 and insulated interconnecting structures. Specifically, for example, Patent Owner relies on Dr. Glew's testimony that Bertin '754's "dielectric layer 60" was grown using thermal oxidation and could not be produced using plasma-enhanced chemical vapor deposition used by Leedy '695. PO Resp. 42–44. More specifically, Dr. Glew explains that, because Bertin '754's dielectric layer is grown as silicon dioxide (rather than deposited using a chemical vapor deposition process), one of ordinary skill in the art would understand that Bertin '754's dielectric layer 60 was produced "using thermal oxidation to grow exposed silicon components into silicon dioxide." PO Resp. 42–43 (citing Ex. 2166 ¶ 127 (Dr. Glew's testimony citing Ex. 1004, 3:60–62, Ex. 2158 (Zant text), 102–103), Ex. 1004, 3:60–62, Ex. 2158, 102–103). In addition, Dr. Glew testifies that "because Bertin describes the silicon dioxide dielectric layer 60 as being grown directly over active silicon components (such as a silicon source,

gate, or drain), one of ordinary skill also would understand that the dielectric layer 60 needs to be highly pure, which again would mean it was grown at high temperatures using thermal oxidation." PO Resp. 43 (citing Ex. 2166 at ¶128; Ex. 1004 at 3:60–4:3; Ex. 2158, 68–70; Ex. 2159, 54, 139). Dr. Glew further testifies that one of ordinary skill in the art would understand that Bertin '754's dielectric layer 60 could not be deposited using plasma-enhanced chemical vapor deposition described by Leedy '695 "because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining . . . steps[7] without changing its form." Ex. 2166 ¶ 130 (citing Ex. 2169, 29–30). Notably, Dr. Glew testifies that plasma-enhanced chemical vapor deposition (a known technique used by Leedy '695) cannot be used with Bertin '754's techniques because "positive ions present in the plasma can strike and damage the wafer and the exposed active components in and on its surface." Ex. 2166 ¶ 130 (citing Ex. 2159, 139).

Furthermore, Dr. Glew's testimony is supported by numerous citations to the prior art references and Exhibits to support his opinions. *See, e.g.*, Ex. 2158 (*see* ¶¶ 31–32), Ex. 2159 (*see* ¶ 70), Ex. 2146 ¶¶ 113–137.

We also note the absence of further declaration testimony by Dr. Franzon in support of Petitioner's Reply to Patent Owner's Response. Rather, Petitioner contests Petitioner's position, which is based on

[7] Petitioner and Patent Owner dispute what is meant by front-end and back-end processing steps. However, we are not persuaded that such a distinction is necessary or helpful to resolution of this issue.

Dr. Glew's well-reasoned and supported testimony, with attorney-argument consisting of conclusory statements with insufficiently explained citations to Leedy '695 and other references. Such untethered reference to conclusory attorney-argument are insufficient to establish that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner. *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements").

For example, Petitioner's attorneys contest Dr. Glew's testimony that, e.g., Leedy '695's PECVD method cannot be used in front end process steps. Pet. Reply 20. We recognize that expert testimony is not always necessary. *See, e.g.*, *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co*., 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) ("However, as we [have] noted . . . 'expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,' particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references." (internal citations omitted)) (alteration in original)). Because of the complexity of integrated circuit fabrication discussed above, however, attorney-argument purportedly addressing Dr. Glew's well-reasoned and supported testimony is not sufficient to convince us that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner.

It is Petitioner's burden to demonstrate by a preponderance of the evidence both a reason to combine and reasonable expectation of achieving

what is claimed. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) ("The reasonable expectation of success requirement refers to the likelihood of success in combining the references to meet the limitations of the claimed invention. . . . [O]ne must have a motivation to combine [the references] accompanied by a reasonable expectation of achieving what is claimed in the patent-at-issue."). It is well-settled that identifying a reason to combine references is not confined to a "rigid or mandatory formula[]." *KSR*, 550 U.S. at 419; *see In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016). We must be careful not to allow hindsight reconstruction of references to reach the claimed invention without adequate explanation as to how or why the references would be combined to produce the claimed invention. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) (quoting *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 n.3 ("We must still be careful not to allow hindsight reconstruction of the references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention.").

In the particular circumstances of this case, with its complex technology of integrated circuit fabrication and robust written description articulating general advantages of its membrane dielectric isolation process, we are not persuaded that Petitioner has met its burden to provide sufficient articulated reasoning with rational underpinning to support Petitioner's conclusion of obviousness.

First, we find Petitioner's combination to be incomplete—utilizing "the material" of Leedy '695 without providing sufficient detail as to the combined process to produce the claimed "material." In the complex

technology of semiconductor fabrication, merely asserting that the low tensile stress dielectric material of Leedy '695 would be utilized to form Bertin '754's dielectric material layer 60 and its insulated interconnectors of Bertin '754 is insufficient. Petitioner has not explained sufficiently how one of ordinary skill in the art would have had reasonable expectation of success of incorporating low tensile stress dielectric material of Leedy '695 into Bertin '754's integrated circuit, without adequately explaining the process changes of Bertin '754 required to do so. We recognize that it is axiomatic that bodily incorporation is not required. *See, e.g.*, *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) ("It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of the elements."). To be clear, we are not suggesting that Petitioner must explain how Leedy '695's entire membrane dielectric isolation process could be somehow meshed to be included with Bertin '754's integrated circuit fabrication process, duplicating the thermal oxidation growing of layer 60 with Leedy '695's plasma-enhanced chemical vapor deposition of its low tensile stress dielectric material. Rather, we find Petitioner's explanation to be incomplete because it does not adequately explain how Bertin '754's fabrication process would be changed to use Leedy '695's dielectric material, which is formed in an entirely different manner than Bertin '754's dielectric layer 60. This is necessary, at least, to support a conclusion that one of ordinary skill in the art would have had reasonable expectation of success of using Leedy '695's dielectric material in place of Bertin '754's layer 60 and interconnecting insulators.

Second, this is particularly true in view of the significant differences between the two process—growing versus chemical deposition. The

question is not only whether one of ordinary skill in the art *could* have done so but also whether one *would* have done so. *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention."). Thus, we find Petitioner's statement that "[i]t would also have been obvious to one of ordinary skill in the art to simply substitute Leedy '695's low tensile stress dielectric material for the dielectrics disclosed in Bertin" to be contrary to the record as a whole.

Furthermore, as noted above, Petitioner's expert does not opine on reasons one of ordinary skill in the art would have made Petitioner's particular combination—substituting Leedy '695's dielectric material for Bertin '754's dielectric layer 60 and interconnecting insulators.

Similarly, we find Petitioner's statement that "[a]s discussed in Leedy '695, such dielectrics can easily be used in place of other dielectrics, including thermal oxide insulators, like the interconnect insulators disclosed in Bertin, which Leedy '695 indicates have high stress" to be unsupported. Pet. 18 (citing Ex. 1006, 6:30–33, 8:59–64; Ex.1002 ¶¶ 99–102). Contrary to Petitioner's statement, the cited portion of Leedy '695 does not indicate that its dielectrics "can be easily used" in place of other dielectrics. Ex. 1006, 6:30–33 ("Thermally formed silicon dioxide forms as a strongly compressive file and most deposited dielectrics currently in use form typically with compressive surface stress."), 8:59–64 ("The thermal oxide isolation created by the LOCOS[8] method may change the net tensile surface

[8] "LOCOS (LOCal Oxidation of Silicon) isolation method." Ex. 1006, 8:

stress of the semiconductor (substrate) membrane layer. The deposition of low stress dielectric films on either side of the semiconductor layer prior to LOCOS processing will offset most compressive effects of the oxide formation."). Rather, the cited text in column 8 discusses how an "alternative technique" to part of Leedy '695's "Method #1" is to use the LOCOS isolation method, which also "could be applied as part of . . . Method #2)." Petitioner fails to explain adequately how the use of the LOCOS isolation method (discussed in column 8) "could be easily used," as Petitioner contends, to address the compressive stress of thermally formed silicon dioxide. The fact that Leedy '695 discloses that the use of a particular method could be used in its two methods does not, without more, suggest that Leedy '695's dielectrics "could be easily" used in place of other dielectrics.

Dr. Franzon's testimony (Ex. 1002 ¶¶ 99–102) is not particularly helpful. Even setting aside the fact that Petitioner cites but does not discuss its expert's testimony,[9] Dr. Franzon does not explain how the cited portions of Leedy '695 show "its dielectrics can be easily used." The fact that PECVD was a well-known process capable of providing TSV insulation (Ex. 1002 ¶ 99) does not in itself indicate that Leedy '695's alternative processes "could have been easily used" in place of Bertin '754's techniques. The fact that an alternative process could be used does not necessarily lead to a conclusion that the alternative process could have been easily used.

[9] 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference from one document to another).

For reasons stated above, and separate and distinct from the insufficiency of proof regarding "substantial flexibility" discussed in the section above, we determine that Petitioner has not established that one of ordinary skill would have utilized the Leedy '695 dielectric in Bertin '754, as proposed, thereby failing to meet the low stress dielectric limitation of claims 10–12 and 18–20.

G. Asserted Grounds of Obviousness Over Bertin '754, Poole, Bertin '333, and Leedy '695

Petitioner challenges claims 60–63, 67, 70–73, and 77 based on the combined teachings of Bertin '754, Poole, Bertin '333, and Leedy '695. Pet. 47. With regard to the "substantially flexible" and low stress dielectric limitations of these claims, Petitioner relies on the same combination discussed above with respect to claims 10–12 and 18–20. However, claims 60–63, 67, 70–73, and 77 use the term "die" or "dice" rather than "substrate(s)." For this reason, Petitioner adds the Bertin '333 reference to the combination. All of claims 60–63, 67, 70–73, and 77 require a "substantially flexible" die. Claims 61–63 and 71–73 also require a low stress dielectric.

With regard to the "die/dice" limitation, Petitioner argues, and we agree, that Bertin '333 explains how wafers are diced into individual circuit chips and how dies are incorporated into a multichip package. However, the addition of Bertin '333 to the combination does not overcome the lack of description of "substantially flexible" discussed above with respect to claims 10–12 and 18–20. Nor does it alter our view that one of ordinary skill would not have made the dielectric substitution as proposed by Petitioner.

With regard to claims 60–63, 67, 70–73, and 77, the inadequacies of proof regarding "substantially flexible" and dielectric substitution remain. Therefore, we are not persuaded that Petitioner has established by a preponderance of the evidence the unpatentability of claims 60–63, 67, 70–73, and 77.

III. SUMMARY OF CONCLUSIONS

We now summarize our determinations and conclusions.

"Substantially flexible" is construed to mean "largely able to bend without breaking." Petitioner has not sufficiently demonstrated that one of ordinary skill would have thinned the Bertin '754 substrate and that doing so, would have resulted in a "substantially flexible" substrate or die/dice.

Petitioner has not sufficiently demonstrated that Bertin '754 has a "substantially flexible" substrate or that one would have resulted from the proposed combination.

Petitioner has not sufficiently demonstrated that one of ordinary skill would have substituted the dielectric of Leedy '695, into Bertin '754.

We conclude, based on a preponderance of the evidence, that Petitioner has not established that claims 10–12, 18–20, 60–63, 67, 70–73, and 77 of the '239 patent are unpatentable.

IV. ORDER

For the reasons given, it is hereby:

ORDERED that claims 10–12, 18–20, 60–63, 67, 70–73, and 77 of the '239 patent have not been shown by a preponderance of the evidence to be unpatentable;

FURTHER ORDERED that this is a Final Written Decision under 35

U.S.C. § 318(a), and that parties to the proceeding seeking judicial review of the decision under 35 U.S.C. § 319 must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

John Kappos
Xin-Yi (Vincent) Zhou
Brian Cook
O'MELVENY & MYERS LLP
jkappos@omm.com
PTABMICRONELM@omm.com
PTABMICRONELM@omm.com

Naveen Modi
Allan Soobert
Phillip Citroen
PAUL HASTINGS LLP
PH Samsung ELM IPR@paulhastings.com
PH-Samsung-ELM-IPR@paulhastings.com
PH-Samsung-ELM-IPR@paulhastings.com

Jason Engel
Benjamin Weed
K&L GATES LLP
jason.engel.PTAB@klgates.com
Skhynix-Elm@klgates.com

FOR PATENT OWNER:

Cyrus A. Morton
Kelsey Thorkelson
ROBINS KAPLAN LLP
cmorton@robinskaplan.com
kthorkelson@robinskaplan.com

William A. Meunier
Michael T. Renaud
MINTZ, LEVIN, COHN, FERRIS, GLOVSKY AND POPEO, P.C.
wameunier@mintz.com
mtrenaud@mintz.com

James Carmichael
CARMICHAEL IP, PLLC
jim@carmichaelip.com