UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX INC.
Petitioners

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner

Case IPR2016-00786
Patent 8,933,570 B2

PETITIONERS' NOTICE OF APPEAL

Pursuant to 37 C.F.R § 90.2(a) and 35 U.S.C. § 142, Petitioners Samsung Electronics Co., Ltd., Micron Technology, Inc., and SK hynix Inc. ("Petitioners") hereby respectfully give Notice that they appeal the Patent Trial and Appeal Board's ("Board") Final Written Decision, dated August 28, 2017 (Paper 37), concluding that claims 58, 60, 61, and 67 of U.S. Patent No. 8,933,570 have not been shown to be unpatentable to the United States Court of Appeals for the Federal Circuit, and from all underlying orders, decisions, rulings, and opinions that are adverse to Petitioners, including, without limitation, those within the Decision on Institution of *Inter Partes* Review, entered October 4, 2016 (Paper 14).

For the limited purpose of providing the Director with the information requested in 37 C.F.R § 90.2(a)(3)(ii), issues on Petitioners' appeal may include, but are not limited to, the construction of the "substantially flexible" term(s); the Board's interpretation of its construction and application of its construction to the prior art; the Board's determination of patentability of claims 58, 60, 61, and 67 of U.S. Patent No. 8,933,570 under 35 U.S.C § 103, which is factually incorrect, not supported by law or substantial evidence, was not the result of a logical and rational process, and is incorrect as a matter of law; any findings supporting that determination, including findings regarding motivation to combine and a reasonable expectation of success; the Board's failure to consider evidence of

record fully and properly; the Board's legal errors in undertaking its obviousness analysis; the Board's findings that conflict with the evidence of record and are not supported by substantial evidence; any finding or determination supporting or related to those issues; and any other issues decided adversely to Petitioners in any orders, decisions, rulings and opinions.

Simultaneous with this submission, a copy of the Notice of Appeal is being filed electronically with the Patent Trial and Appeal Board. In addition, a copy of this Notice of Appeal, along with the required docketing fees, are being filed electronically with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Respectfully submitted,

Date: October 18, 2017

/Naveen Modi/

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CERTIFICATE OF SERVICE

In accordance with 37 CFR § 90.2(a)(1) and § 104.2, I hereby certify that on October 18, 2017, in addition to being filed electronically through the Board's E2E System, the original version of the foregoing Petitioners' Notice of Appeal was filed by express overnight mail on the Director of the United States Patent and Trademark Office, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
Madison Building East, 10B20
600 Dulany Street
Alexandria, VA 22314-5793

CERTIFICATE OF SERVICE

I hereby certify that on October 18, 2017, a true and correct copy of the foregoing Petitioners' Notice of Appeal, along with a copy of the Final Written Decision, was filed electronically with the Clerk's Office of the United States Court of Appeals for the Federal Circuit, at the following address:

United States Court of Appeals for the Federal Circuit
717 Madison Place, N.W., Suite 401
Washington, DC 20005

CERTIFICATE OF SERVICE

Pursuant to 37 CFR § 42.6(e)(1), the undersigned certifies that on October 18, 2017, a complete and entire copy of the Petitioners' Notice of Appeal was provided via email to the Patent Owner by serving the email correspondence addresses of record as follows:

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Paper 37
Entered: August 28, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and
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ELM 3DS INNOVATIONS, LLC,
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Case IPR2016-00786
Patent 8,933,570 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L. IPPOLITO, *Administrative Patent Judges*.

PERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Procedural History

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition on March 21, 2016, requesting an *inter partes* review of claims 58, 60, 61, and 67 of U.S. Patent No. 8,933,570 B2 (Ex. 1001, "the '570 patent" or "the challenged patent"). Paper 1, "Pet." Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition on July 5, 2016. Paper 11, "Prelim. Resp."

Based on these submissions and accompanying exhibits, we instituted an *inter partes* review of claims 58, 60, 61, and 67 of the '570 patent on the following grounds:

References	Basis	Claim(s) Challenged
Bertin '754[1], Poole[2], and Leedy '695[3]	§ 103	58, 60, 61, and 67
Hsu[4] and Leedy '695	§ 103	58, 60, 61, and 67
Bertin '754 and Poole	§ 103	58

Paper 14 ("Dec. on Inst.").

After institution, Patent Owner filed its Patent Owner Response on January 4, 2017 (Paper 30, "PO Resp.") and Petitioner filed a Reply (Paper

[1] U.S. Patent No. 5,202,754, issued April 13, 1993 (Ex. 1004, "Bertin '754").
[2] U.S. Patent No. 5,162,251, issued Nov. 10, 1992 (Ex. 1005, "Poole").
[3] U.S. Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, "Leedy '695").
[4] U.S. Patent No. 5,627,106, issued May 6, 1997 (Ex. 1008, "Hsu").

33, "Reply").

This *inter partes* review pertains to one member of the "Elm 3DS family" of patents that shares a common core of written description but have different claims (continuations and divisional applications of a common parent). Some of the patents being considered in *inter partes* reviews of patents in the Elm 3DS family have expired and others have not (*e.g.*, the '570 patent). On April 6, 2017, we held a consolidated hearing in which we heard arguments on fourteen *inter partes* reviews (including this one and all having the same panel of Administrative Patent Judges) of Elm 3DS family patents. Final written decisions have been issued in some of the proceedings. *See, e.g.*, IPR2016-00386–IPR2016-00391, IPR2016-00393–IPR2016-00395. Although there are differences among these related *inter partes* reviews (different claims and different combinations of prior art references, different reasons to combine, and different arguments regarding reasonable expectation of success), there is a significant overlap of evidentiary records among the reviews. Each *inter partes* review has been decided on its own evidentiary record. A transcript of the Oral Hearing is included in the record of each proceeding, including this one. Paper 36 ("Tr.").

This Decision relies in part on analysis set forth in the combined Final Written Decision in IPR2016-00386 (Paper 68), IPR2016-00387 (Paper 63), and IPR2016-00388 (Paper 60), particularly as to claim construction. In addition, we analyze, where appropriate, different prior art combinations including reasons to combine and reasonable expectation of success.

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the

challenged claims. For the reasons discussed herein, Petitioner has not demonstrated by a preponderance of the evidence that claims 58, 60, 61, and 67 of the '570 patent are unpatentable.

B. Related Proceedings

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; Paper 6 (Patent Owner's Mandatory Notices). Petitioner indicates that Patent Owner has asserted the challenged patent against Petitioner in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc*., No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc*., No. 1:14-cv-01432 (D. Del.). Pet. 1–2.

Petitioner also indicates that Patent Owner has asserted related U.S. Patent Nos. 7,193,239; 7,474,004; 7,504,732; 8,035,233; 8,410,617; 8,629,542; 8,653,672; 8,791,581; 8,796,862; 8,841,778; 8,907,499; and 8,928,119 in one or more of these actions. Pet. 2

Petitioner further indicates that it requested *inter partes* review of the following patents: 7,193,239 (IPR2016-00388 and IPR2016-00393); 7,504,732 (IPR2016-00395); 8,629,542 (IPR2016-00390); 8,035,233 (IPR2016-00389); 8,410,617 (IPR2016-00394); 8,653,672 (IPR2016-00386); 8,796,862 (IPR2016-00391); 8,841,778 (IPR2016-00387); 8,928,119 (IPR2016-00687); and 7,474,004 (IPR2016-00691). *Id.*

Petitioner also indicates that Micron Technology, Inc. and SK Hynix Inc. requested *inter partes* review of 8,791,581 (IPR2016-00703 and IPR2016-00706). *Id.* We did not institute those requested *inter partes*

reviews. We note that Samsung Electronics, Co., Ltd. filed a request for *inter partes* review of certain claims of U.S. Patent No. 8,791,581. *See* IPR2017-01305, Paper 2.

C. The '570 Patent (the Challenged Patent)

The '570 patent relates generally to a three-dimensional structure (3DS) for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

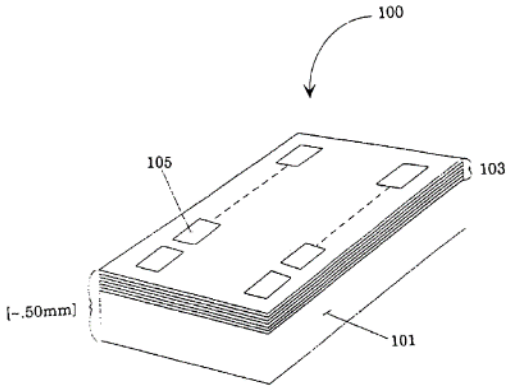

Figure 1a

Figure 1a shows three-dimensional memory device 100 having a stack of integrated circuit layers with vertical interconnects between all circuit layers. *Id.* at 3:10–14. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:30–32. The challenged patent describes that "each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness." *Id.* at 4:33–40. It further discloses that the

> thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication.

Id. at 8:56–61.

Figure 1b is reproduced below.

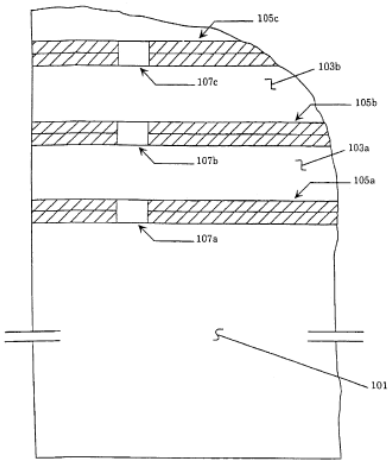

Figure 1b

Figure 1b shows a cross-section of a three-dimensional integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:51–53. Bond and interconnect layers 105a, 105b, 105c are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. Pattern 107a, 107b, and 107c, in the bond and interconnect layers 105a, 105b, and 105c, defines vertical interconnect contacts between the integrated circuit layers and electrically isolates these contacts from each other and the remaining bond material. *Id.* at 4:24–29. The pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:28–29.

In the challenged patent, the "term fine-grain inter-layer vertical interconnect [refers to] electrical conductors that pass through a circuit layer

with or without an intervening device element and have a pitch of nominally less than 100 µm . . . ." *Id.* at 4:13–16. These fine-grain inter-layer vertical interconnects bond together various circuit layers. *Id.* at 4:13–14.

D. The Challenged Claims

Claim 58, the only independent claim at issue, is reproduced below:

> 58. An apparatus comprising:
>
> a first integrated circuit layer having a thickness Th_1;
>
> a second integrated circuit layer in a stacked relationship with and adjacent to the first integrated circuit layer having a thickness Th_2; and
>
> a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits;
>
> wherein the vertical interconnect segments have lengths of Th_1+Th_2 or less; and
>
> wherein at least one of the first integrated circuit and the second integrated circuit is thin and *substantially flexible* and comprises a thinned, *substantially flexible* monocrystalline semiconductor substrate of one piece made from a semiconductor wafer thinned from a backside thereof by at least one of abrasion, etching and parting, and subsequently polished or smoothed to form a polished or smoothed surface.

Ex. 1001, 19:66–20:18 (emphasis added). Claims 60, 61, and 67 depend from and further limit claim 58 to require a dielectric material having a *tensile stress of less than 5 x 10^8 dynes/cm^2*.

II. ANALYSIS

A. Principles of Claim Construction

Members of the Elm 3DS family share a common core of written descriptions but have different claims (continuations and divisional applications of a common parent). Some of the patents being considered have expired and others have not.

The '570 patent has not yet expired. Thus, the broadest reasonable construction standard applies to the claims at issue. Accordingly, here, we interpret claims of an unexpired patent using the "broadest reasonable construction in light of the specification of the patent in which [the claims] appear[]." 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144 (2016) (concluding the broadest reasonable construction "regulation represent[s] a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office").

Under this standard, the Board may not "construe claims during IPR so broadly that its constructions are *unreasonable* under general claim construction principles. . . . '[T]he protocol of giving claims their broadest reasonable interpretation . . . does not include giving claims a legally incorrect interpretation.'" *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2016). "Rather, 'claims should always be read in light of the specification and teachings in the underlying patent'" and "[e]ven under the broadest reasonable interpretation, the Board's construction 'cannot be divorced from the specification and the record evidence.'" *Id.* (citations omitted).

B. Principles of Law Concerning Demonstrating Unpatentability

To prevail in challenging Patent Owner's claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc., v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "'with particularity . . . the evidence that supports the grounds for the challenge to each claim'")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC, v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Petitioner asserts that certain claims of the challenged patents are unpatentable under 35 U.S.C. § 103(a) as obvious over various combinations of references. A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co., v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and

(4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Consideration of the *Graham* factors helps "inform the ultimate obviousness determination." *Apple Inc., v. Samsung Elecs. Co., LTD.*, 839 F.3d 1034, 1048 (Fed. Cir. 2016) (en banc).

C. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, 35 U.S.C. § 103 requires us to resolve the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. "The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co., v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991). The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors that may be considered in determining the level of ordinary skill in the art include, but are not limited to, the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *GPAC*, 57 F.3d at 1579. In a given case, one or more factors may predominate. *Id.* Generally, it is easier to establish obviousness under a higher level of ordinary skill in the art. *Innovention Toys, LLC, v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011) ("A less sophisticated level of skill generally favors a determination of nonobviousness . . . while a higher level of skill favors the reverse.") (citation omitted).

Petitioner, with support of its declarant Paul D. Franzon, Ph.D., contends that one of ordinary skill in the art at the time of the inventions of the challenge patents "would have had at least a B.S. degree in electrical

engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing." Pet. 5 (citing Ex. 1002 ¶¶ 52–53). Dr. Franzon states that his testimony as to the level of ordinary skill is based on considering "the type of problems encountered in the art, prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field." Ex. 1002 ¶ 53. Patent Owner did not propose expressly a particular level of ordinary skill. *See, e.g.*, *generally* PO Resp. At the Oral Hearing, however, Petitioner indicated that there did not seem to be any dispute as to the correct level of ordinary skill. Tr. 112:11–14 ("I don't think there was any dispute about whether [Dr. Franzon's proposed level of ordinary skill] was the correct level of skill, although Patent Owner can correct me.").

Having reviewed the prior art asserted in these proceedings (*see, e.g.*, Exs. 1004–07, 1009, 2160), we determine that the level of ordinary skill proposed by Petitioner's declarant is consistent with the challenged patent and the referenced prior art, and we adopt Petitioner's proposed definition of the level of ordinary skill in the art for the purposes of the analysis below.

D. Construction of "Substantially Flexible"[5]

For reasons stated in our final written decision for IPR2016-00386, we construe "substantially flexible" in the context of the related patents to

[5] The term "substantially flexible" is at issue in thirteen of the Elm 3DS *inter partes* reviews: IPR2016-00386 ('672 patent), IPR2016-00387 ('778 patent), IPR2016-00388 ('239 patent), IPR2016-00390 ('542 patent), IPR2016-00391 ('862 patent), IPR2016-00393 ('239 patent), IPR2016-00394 ('617 patent), IPR2016-00395 ('732 patent), IPR2016-00687 ('119 patent), IPR2016-00691 ('004 patent), IPR2016-00708 ('499 patent),

as "largely able to bend without breaking." The '570 patent, at issue here, has not yet expired; thus, the applicable construction is broadest reasonable interpretation. At Oral Hearing, Petitioner's counsel asserted that the claim construction of "substantially flexible" would be the same under both claim construction standards. Tr. 12:2–4 (Petitioner's counsel indicating that the "we don't see there as being a difference, whether BRI or Phillips is applied."); *see generally* Tr. 11:21–13:16. Similarly, Patent Owner's counsel at Oral Hearing indicated that the same construction would apply under broadest reasonable construction standard or the standard under *Phillips*. Tr. 50:10–14 (Q: "[I]n terms of the different claim construction standards, I understood that your position is that the same construction would apply under BRI or in District Court for substantially flexible." A: "That's correct.").

In the context of the Elm 3DS family, we find that the broadest reasonable interpretation of "substantially flexible" is the same as our construction under the *Phillips* standard. Under the broadest reasonable construction standard, we presume a claim term carries its ordinary and customary meaning, which "'is the meaning that the term would have to a person of ordinary skill in the art in question'" at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). As discussed in detail in the Final Written Decisions in IPR2016–00386, IPR2016-00387, and IPR2016–00388, the ordinary and customary meaning of "substantially flexible" is "largely able to bend without breaking." Also as discussed extensively in those Final Written Decisions,

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IPR2016-00770 ('499 patent), and IPR2016-00786 ('570 patent).

the inventor did not give the term "substantially flexible" a particular meaning in the Specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Claim 58 includes the term "substantially flexible" as a modifier of "integrated circuit" and "monocrystalline semiconductor substrate." Thus, a "substantially flexible" integrated circuit requires an integrated circuit that is able to bend without breaking; and a "substantially flexible" monocrystalline semiconductor layer requires a monocrystalline semiconductor layer that is able to bend without breaking.

E. Summaries of the Prior Art Disclosures

Our understanding of the various prior art references relied upon by Petitioner is set forth in the following summaries.

1. Summary of Bertin '754 (Ex. 1004)

Bertin '754 is a United States patent that describes an improvement to a known multichip package as shown in its "prior art" Figure 1, reproduced below.

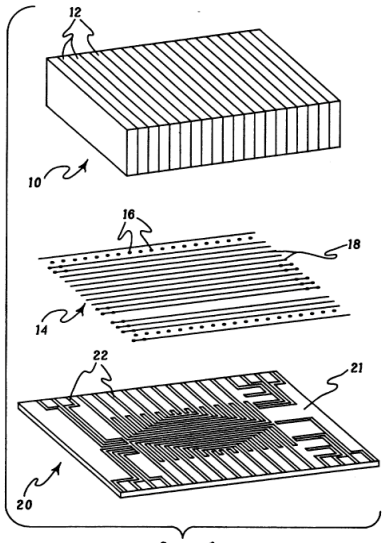


fig. 1
(PRIOR ART)

Bertin ’754’s Figure 1 is an exploded perspective view of a basic prior art multichip package. *Id.* at 2:43–44.

Bertin ’754 describes “[a] fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips.” *Id.* at Abstract. More specifically, Bertin ’754 relates to a method for fabricating a three-dimensional multichip package having a densely stacked array of semiconductor chips interconnected at least partially by means of a plurality of metallized trenches in the semiconductor chips. Ex. 1004, 1:10–15. Figure 3a is reproduced below.

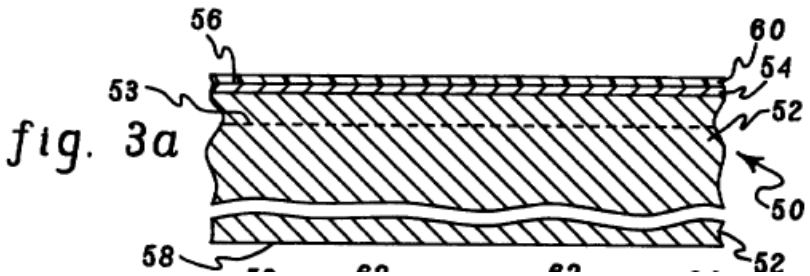


fig. 3a

Referring first to FIG. 3a, processing begins with a semiconductor device 50 (preferably comprising a wafer) having a substrate 52 and an active layer 54, which is typically positioned at least partially therein. *Id.* at 3:50–53. Layer 54 may be totally or partially defused into substrate 52 and/or partially or totally built up from substrate 52 using *conventional semiconductor processing techniques* known to those skilled in the art. *Id.* at 3:53–57. Layer 54 is adjacent to a first, upper planar surface 56 of device 50. *Id.* at 3:57–58. A second, lower planar surface 58 of stacked chip 50 is positioned substantially parallel to first planar surface 56. *Id.* at 3:59–60. Stacked chip 50 includes a semiconductor “substrate **52**” (*id.* at 3:50–4:3), which is thinned to 20 μm or less (*id.* at 3:25–46, 5:10–22). Bertin ’754 further teaches that “dielectric layer **60**, for example, SiO_2, is grown over

active layer **54** of device **50**." *Id.* at 3:60–62, Fig. 3a. Additionally, Bertin '754 teaches that the multichip package includes vertical electrical interconnections (e.g., metallized trenches) that pass completely through substrates 52. *Id.* at Abstract, 1:62–2:12, 4:11–52, Figs. 3c, 3b, 3e, 3g.

2. Summary of Poole (Ex. 1005)

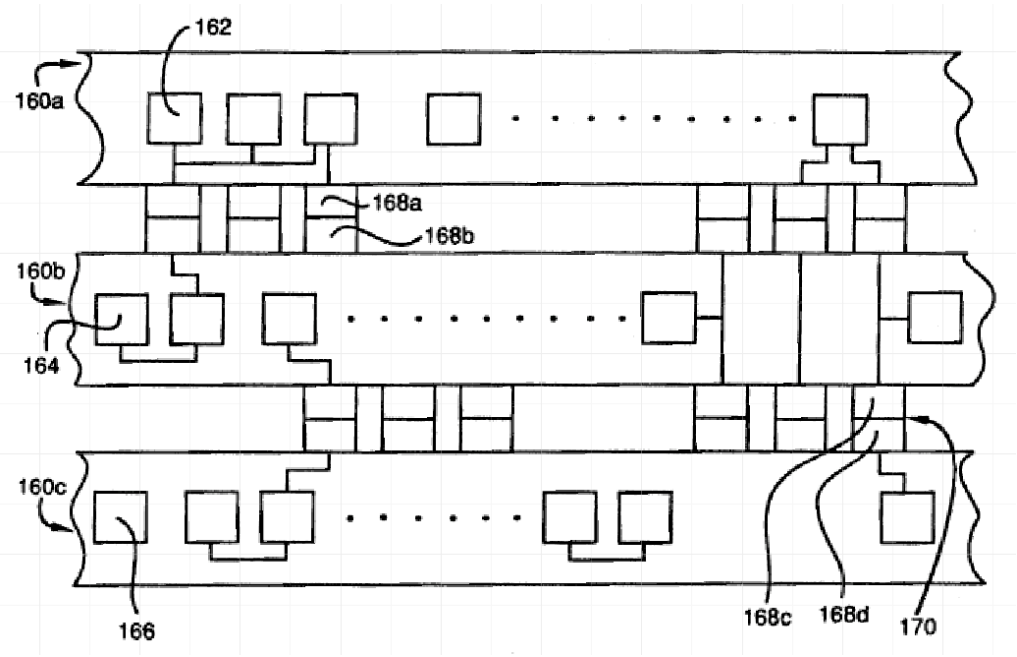
Poole is a United States patent that describes techniques for making thinned charge-coupled devices, which are thinned to allow illumination of the backside of the device to improve quantum efficiency and UV spectral response. *Id.* at Abstract, 1:8–11. Poole describes a two-step method for thinning the backside of a silicon semiconductor substrate that includes integrated circuitry previously formed on the front side. Ex. 1005, Abstract, 1:7–18, 3:12–6. First, "[t]he bulk silicon is thinned to 75 μm with a 700 micro-grit aluminum oxide abrasive" (*id.* at 3:21–25; *see also id.* at Abstract, 3:33–34, 5:60–6:35), and "is then thinned and polished to 10 μm using 80 nm grit colloidal silica" (*id.* at 3:21–25; *see also id.* at Abstract, 3:33–34, 6:37–46). The result is a surface "almost totally free of work damage." *Id.* at 5:64–65; *see also id.* at 3:44–46.

3. Summary of Leedy '695 (Ex. 1006)

Leedy '695 is a United States patent that describes fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In its Abstract, Leedy indicates that the disclosed integrated circuits are fabricated from flexible membranes "formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers." *Id.* at Abstract. Leedy describes forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated

circuit structure. *Id.* at 1:53–58. Leedy defines "[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension." *Id.* at 11:33–37. Additionally, Leedy discloses two chemical vapor deposition (CVD) process recipes for manufacturing "Structurally Enhanced Low Stress Dielectric Circuit Membranes." *Id.* at 11:51–65.

Referring to Figure 8, Leedy discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.



Leedy '695, Figure 8 shows a three dimensional circuit membrane. Ex. 1006, 4:42.

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160*a*, 160*b*, 160*c* including SDs 162, 164, 166 is by compression bonding of circuit membrane surface

electrodes 168*a*, 168*b*, 168*c*, 168*d* (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168*c*, 168*d* (typically between 4 μm and 25 μm in diameter) on the surface of two circuit membranes 160*b*, 160*c* and using a mechanical or gas pressure source to press bond pads 168*c*, 168*d* together. *Id.* at 16:43–49.

4. Summary of Hsu (Ex. 1008)

Hsu describes a "method of connecting three-dimensional integrated circuit chips using trench technology." Ex. 1008, Abstract, 1:8–11. Hsu's fabrication process, depicted in Figures 2–8, starts with etching deep trenches 16 on silicon substrate 10, which Hsu indicates can be composed of monocrystalline silicon. *Id.* at 2:50–61. Hsu's integrated circuits consist of "one master chip and some subordinate chips." *Id.* at 1:20–21. According to Hsu, the master chip and subordinate chip each consist of a semiconductor substrate, preferably composed of monocrystalline silicon. *Id.* at 2:51–54, 3:42–45. These chips can be "stacked by interconnection through [a] pad window [. . .] during integrated circuit processing." *Id.* at 1:28–31. Hsu further describes that the "bottom surface of the [subordinate] substrate is ground and polished so that only a thin portion of the substrate remains." *Id.* at 3:21–23.

F. Challenge Based on Bertin '754, Poole, and Leedy '695

Having considered the parties' arguments and weighed the parties' evidence cited therein, and for the reasons set forth below, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 58, 60, 61, and 67 are unpatentable under 35 U.S.C. § 103 over Bertin '754, Poole, and Leedy '695.

1. Petitioner's Contentions

A common theme in all of Petitioner's challenges is that it would have been obvious to one of ordinary skill to substitute one or more dielectrics of a stacked-IC base reference (e.g., Bertin '754, Hsu) with a different dielectric (Leedy '695's low tensile stress dielectric). For this particular challenge, Petitioner argues that Bertin '754 teaches or suggests "all but a few" of the features recited in claims 58, 60, 61, and 67, including "stacked chips" each having a "'dielectric layer,'" for example SiO_2, and through-silicon metal interconnects insulated by oxidized sidewalls. Pet. 22 (citing Ex. 1004, 3:60–62, 4:30–33).

Petitioner admits that Bertin '754 does not explicitly disclose that the dielectric layer or the interconnect insulator constitutes a "'low stress'" dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, as recited in the challenged claims. Pet. 22 (citing Ex. 1002 ¶ 124 (element 58e)). Petitioner argues that it would have been obvious to one of ordinary skill to modify the processes and device in Bertin '754 such that each of the dielectric layers and the interconnect insulators constitutes a dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, based on the disclosure of Leedy '695. Pet. 22–23 (citing Ex. 1002 ¶¶ 103–113).

According to Petitioner, the motivation for one of ordinary skill to combine these teachings is in part because Bertin '754 and Leedy '695 are both directed to the improvement of integrated circuits and recognize the central role the fabrication process plays in facilitating this improvement. Pet. 23 (citing Ex. 1004 at 1:7–2:31; Ex. 1006 at 1:38–67, 3:56–4:13).

Petitioner argues that Leedy '695 provides "express motivations" for modifying Bertin '754's processes and device to incorporate Leedy '695's

low tensile stress dielectric material because Leedy '695 explains that low tensile stress is important because otherwise "'surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane.'" Pet. 23 (citing Ex. 1006, 5:63–6:5; Ex. 1002 ¶ 109).

Petitioner also points to the Leedy '695 use of a plasma-enhanced chemical vapor deposition ("PECVD") to deposit low tensile stress dielectrics. Pet. 24 (citing Ex. 1006, 11:28–63). Petitioner argues that one of ordinary skill would incorporate Poole's two-step thinning process into Bertin '754 to achieve a predictable result of a thin substrate with a planar surface having minimal defects. Pet. 27 (citing Ex. 1005, 6:68–7:2). Petitioner provides an element-by-element "read" of the challenged claims on Bertin '754, Poole, and Leedy '695 at Petition pages 28–45.

2. Patent Owner's Contentions

Patent Owner argues with respect to all challenges that "substantially flexible" cannot be read out of the claims. PO Resp. 1. In particular, Petitioner's arguments that the prior art teach a "thinned" substrate do not establish that the substrate and resulting circuit are in fact "substantially flexible." Patent Owner notes that, for example, a potato chip can be thin but still be rigid and break rather than flex. *Id.*

Patent Owner also argues with respect to all challenges that "**dielectrics are not fungible**." PO Resp. 2. In support of its argument against dielectric substitution, Patent Owner presents a tutorial explaining the complexity of semiconductor fabrication, with numerous citations to the

prior art references and declaration testimony of its expert, Alexander D. Glew, Ph.D. (Ex. 2166). PO Resp. 3–31.

The tutorial stresses the detailed planning and decisions required to establish a fabrication process for a semiconductor integrated circuit. It explains four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called "'wafers.'" PO Resp. 6 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). The tutorial explains different techniques for producing and layering dielectrics (PO Resp. 16–30), including growing dielectrics using thermal oxidation (PO Resp. 18–19), depositing dielectrics (PO Resp. 19) and a comparison of thermal CVD (PO Resp. 20) with Plasma Enhanced CVD (PO Resp. 21); different kinds and uses of dielectrics (PO Resp. 22–29) including field oxide dielectrics, gate oxide dielectrics, pre-metal dielectrics, intermetal dielectrics, and passivation dielectrics.

Patent Owner argues, with respect to both challenges that rely on Leedy '695, that Leedy '695 describes an approach to IC fabrication that relies upon a free-standing, flexible membrane, as opposed to a traditional rigid semiconductor substrate and that one of ordinary skill would not have adapted any of the primary references to utilize the Leedy '695 dielectric. PO Resp. 37–42.

With regard to Bertin '754 in particular, Patent Owner argues that Bertin '754's "'dielectric layer 60,'" its "'trench sidewalls,'" and its "'oxidation/connecting metallization layer 63'" could not be produced and

layered using plasma enhanced CVD. PO Resp. 43–46. Further, Patent Owner argues, Bertin '754's "dielectric layer 60" is removed from the chip during processing and is not part of its final integrated circuit. PO Resp. 46–47 (citing Ex. 2166 ¶ 131).

Patent Owner also argues that one of ordinary skill would understand that Bertin '754's layers 60 and 63 are high-purity silicon dioxide grown over active circuit components via thermal oxidation at high temperatures during the front-end-of-line phase of fabrication. PO Resp. 64 (citing Ex. 2166 ¶ 143). Because of the requirements and positions of these dielectrics, one of ordinary skill would not replace layer 60 or 63 with the Leedy '695 low-tensile stress PECVD dielectric. PECVD cannot be used during front end of line to produce and deposit a high-purity silicon dioxide dielectric over actgive circuit components because the resulting dielectric would not 1) be sufficiently pure; 2) have the ability to adhere sufficiently to the wafer; and 3) be able to maintain its properties when subjected to high temperatures in the remaining FEOL steps without changing its form. PO Resp. 64–65.

3. "Substantially Flexible" Claim Requirement

All claims at issue require that Petitioner establish that the prior art describes an integrated circuit that is "substantially flexible." *See* independent claim 58. The evidentiary record in this review, particularly with respect to Bertin '754, Poole, and Leedy '695 is substantially the same as that presented in IPR2016-00386, IPR2016-00387 and IPR2016-00388. We adopt and incorporate the combined Final Written Decision in those cases. *See* IPR2016-00386, Paper 68. For the same reasons set forth in that decision, we conclude that Bertin '754, Poole, and Leedy '695 do not meet the claim requirement of "substantially flexible." *See* IPR2016-00386,

Paper 68, pp. 41–46. Claims 58, 60, 61, and 67 present the same issue with respect to "substantially flexible" as did the claims under consideration in IPR2016-00386.

Given our construction of "substantially flexible," the evidentiary record directed to establishing "thin" and "polished" does not establish flexibility.

Petitioner argues here, as in IPR2016-00386, that Bertin '754 discloses a semiconductor substrate that has been thinned to less than 50 μm and so discloses a substantially flexible semiconductor substrate as required by the claims. A preponderance of the evidence establishes, however, that, in the context of semiconductor substrates, mere thinning is not the same as flexibility—being able to bend without breaking. We find that "thinning" does not equate to "flexibility" because thinning does not account for materials and the processing steps acting on those materials.

Petitioner has the burden "to show with particularity why the patent it challenges is unpatentable." *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3)). Accordingly, we are not persuaded that Petitioner has demonstrated by a preponderance of the evidence that the prior art embodiments mirror the preferred embodiment in the challenged patent and, therefore, the prior art shows bendability. Furthermore, Petitioner's counsel at the Oral Hearing confirmed that Petitioner's Reply to Patent Owner's claim construction position is that "first and foremost their claim construction is improper because it's indefinite, so in drafting the reply, . . . we tried and couldn't figure out how to apply their construction to the prior art, so the claim construction portion of the reply explains why their construction is incorrect." Tr. 176:7–12.

As in IPR2016-00386, Petitioner also relies on Poole's teaching of a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed. Pet. 26. Petitioner relies on Poole's two-step grinding process in which "'[t]he bulk silicon is thinned to 75 μm . . . and is then thinned and polished to 10 μm.'" Pet. 26–28. Thus, Petitioner relies on thinness to produce a substantially flexible semiconductor substrate. As discussed previously, without explaining particular materials, conditions, and other context, relying upon thinness alone does not establish that Poole's substrate satisfies the claim requirement of "substantially flexible." Thus, Petitioner has not sufficiently explained why Poole's thinning and polishing would have satisfied the "substantially flexible" claim requirement.

For these reasons, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the combination of Bertin '754's substrate of less than 50 μm and Poole's polishing would have conveyed to one of ordinary skill in the art the "substantially flexible" integrated circuit required by the challenged claims. Insufficient proof of "substantially flexible" alone is sufficient for us to conclude that Petitioner does not satisfy its burden to establish that claims 58, 60, 61, and 67 are unpatentable. There is, however, an additional independent and separate reason as set forth below for our conclusion that Petitioner does not satisfy this burden with respect to claims 60, 61, and 67.

4. Low Tensile Stress Dielectric Substitution

Claim 58 does not require Petitioner to establish low tensile stress dielectric substitution. However, claims 60, 61, and 67 do.

In this review, Petitioner relies upon one of ordinary skill making the

same dielectric substitution as relied upon in IPR2016-00386 with regard to Bertin '754, Poole, and Leedy '695. For the same reasons as stated in our Final Written Description in IPR2016-00386, we conclude the evidentiary record of this review, which is substantially the same as that of IPR2016-00386, that Petitioner has not established by a preponderance of the evidence, that one of ordinary skill would have made the required dielectric substitution. *See* IPR2016-00386, Paper 68, pp. 46–77.

As in the '386 review, at the heart of this issue is whether Petitioner has demonstrated by a preponderance of the evidence a reason why one of ordinary skill in the art would have substituted the dielectric material of Leedy '695 and would have had a reasonable expectation of success of doing so. This substitution would require substituting at least some portions of Leedy '695's fabrication techniques in which integrated circuit elements are formed on a low tensile stress dielectric membrane for some of the conventional fabrication process steps of Bertin '754.

As we concluded, based on the substantially same evidentiary record in the '386 review, we determine that Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have a reason to combine the references in the manner proposed by Petitioner to arrive at the claimed invention and would have had a reasonable expectation of success.

As in the '386 review, our conclusions are based in part on the complexity of integrated circuit fabrication and Petitioner's evidence not sufficiently establishing how one of ordinary skill would have taken into account the numerous process steps and parameter considerations, considering that selecting a dielectric material involves choosing particular

fabrication techniques that are part of an overall fabrication process for a particular integrated circuit.

5. Conclusion

For this separate and independent reason, we conclude that the preponderance of evidence does not support a finding of unpatentability of claims 60, 61, and 67 based on Bertin '754, Poole, and Leedy '695.

G. Challenges Based on Hsu and Leedy '695

Having considered the parties' arguments and weighed the parties' evidence cited therein, and for the reasons set forth below, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 58, 60, 61, and 67 are unpatentable under 35 U.S.C. § 103 over Hsu and Leedy '695.

1. Petitioner's Contentions

Petitioner contends that Hsu explicitly discloses all but a few of the features recited in claims 58, 60, 61, and 67, including stacked chips each having a silicon dioxide film. Pet. 45. Petitioner admits that Hsu does not explicitly disclose that the dielectric layer constitutes a "'low stress'" dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, as recited in the challenged claims. *Id.*

However, Petitioner argues that it would have been obvious to one of ordinary skill to modify the processes and device in Hsu such that the dielectric layer constitutes a dielectric with a tensile stress of about 5×10^8 dynes/cm^2 or less, based on the disclosure of Leedy '695. Pet. 45 (citing Ex. 1002 ¶¶ 103–113).

Petitioner argues, as a motivation to combine, that Hsu and Leedy '695 are both directed to the improvement of integrated circuits and

recognize the central role the fabrication process plays in facilitating this improvement. Pet. 46 (citing Ex. 1008, 1:7–10, 1:19–33; Ex. 1006 at 1:38–67, 3:56–4:13). Further, both disclosures suggest the need to improve the manufacture of "'high density integrated circuits'" including 3D integrated circuits. *Id.* (citing Ex.1008, 1:7–10, 1:19–33; Ex. 1006, Abstract, 2:9–14, 45:49–59, 47:31–33).

Petitioner points to the same "express motivations" for combination in in Leedy '695 as pointed to in arguing the Bertin '754 combination, above. Pet. 46–49. Petitioner provides a detailed "read" of the challenged claims on Hsu and Leedy '695 at pages 49–57 of the Petition.

2. Patent Owner's Contentions

In addition to its general arguments regarding "substantial flexibility" and "dielectric substitution," Patent Owner argues that one of ordinary skill would not have used the Leedy '695 dielectric in place of Hsu's silicon dioxide layer 18. Pet. 45–59; PO Resp. 65–67. This is because Hsu's silicon dioxide film 18 could not be replaced with a dielectric deposited using a plasma-enchanced CVD such as described in Leedy '695. PO Resp. 66.

3. "Substantially Flexible" Claim Requirement

All of the claims at issue require at least one layer or circuit to have "substantial flexibility."

We are not persuaded by Petitioner's argument that the "substantially flexible" limitations of claims 58, 60, 61, and 67 are met by Hsu or Leedy '695 individually or in combination.

Independent claim 58 requires at least one of the first integrated circuit and the second integrated circuit to be thin and substantially flexible.

We regard "thin" and "substantially flexible" as separate and distinct requirements. Petitioner's arguments regarding substantial flexibility are all based on its proposed narrow construction of a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed. *See, e.g.*, Pet. 13.

As noted in our claim construction section, above and as referenced in our Final Written Decision in IPR2016-00386, a preponderance of the evidence establishes that, in the context of semiconductor substrates, mere thinning is not the same as flexibility—being able to bend without breaking.

Although Petitioner presents arguments attempting to demonstrate thinning, there are no arguments that this thinning necessarily results in flexibility. Thus, we determine that Petitioner has not met its burden to demonstrate the required "substantial flexibility."

The Examiner, during prosecution of the abandoned '652 application, stated that flexibility is not the equivalent of mere thinning. Ex. 2168, 4. Petitioner's expert, Dr. Franzon, testified that the flexibility of a semiconductor substrate depends on many factors, only one of which is the physical dimensions of the substrate—width and thickness. Ex. 1002 ¶ 71. Specifically, Dr. Franzon stated:

> In the context of semiconductor processing, the flexibility of a semiconductor substrate depends on a number of factors, including, for example, the type of semiconductor substrate (e.g., while silicon and gallium arsenide are both semiconductors, they have different elastic moduli), the crystal orientation of the material (e.g., {100} and {111} silicon wafers have different elastic moduli), and the physical dimensions of the substrate (e.g., width and thickness).

Ex. 1002 ¶ 70, *see also* Tr. 33:8–24 (Patent Owner's counsel at Oral Hearing discussing Dr. Franzon's testimony about the factors on which flexibility of

a semiconductor substrate depends); Tr. 64:16–65:11 (Petitioner's counsel responding to Patent Owner's argument about Dr. Franzon's testimony regarding the various factors that would be considered to determine whether something is flexible).

Petitioner's counsel asserted at the Oral Hearing that the prior art shows bendability in addition to thinning because the asserted "prior [art] mirrors the prior [preferred] embodiment." Tr. 175:21–176:2. Petitioner, however, does not point to sufficient evidence to support its position that prior art mirrors the preferred embodiment in the challenged patent. *See generally* Tr. 175:13–180:16. For example, Petitioner contends that Dr. Franzon's testimony that the limitations are met by the prior art supports its position. Tr. 178:20–22 (Asking "is there any evidence of record that any of the combinations that you propose would be the same as the preferred embodiment"?); Tr. 180:8–10 (Petitioner's counsel responding that "[i]t's Dr. Franzon's testimony that those limitations are met by the prior art, and it's the prior art itself, lining up with the claims,"). Dr. Franzon, however, testifies that he was given Petitioner's proposed construction of "a semiconductor [layer] that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed" and he "applied Petitioner's construction in [his] analysis." Ex. 1002 ¶ 75. That construction was not adopted as our final claim construction.

As stated above in our claim construction discussion of "substantially flexible," we do not equate "thinned" with "substantially flexible." Common sense also supports a conclusion that thickness is not the only factor that determines whether a material is flexible. After all, a thicker piece of rubber is more flexible than a thinner potato chip. Without

comparing and considering materials, conditions and fabrication steps, relying upon thinness alone does not satisfy the claim requirement of "substantially flexible."

This reason alone sufficiently supports our conclusion as to claims 58, 60, 61 and 67. However, we also conclude, as set forth below that for a second, independent reason, Petitioner has not established that claims 60, 61, and 67 are unpatentable. Petitioner has not sufficiently established that one of ordinary skill would have substituted the dielectric material of Leedy '695 for the various layers proposed for substitution in Hsu. Therefore we do not credit Leedy '695 as providing any potential "substantial flexibility" to Hsu.

4. Low Tensile Stress Dielectric Substitution

Claims 60 and 61 require "at least one of a silicon dioxide dielectric material and an oxide of silicon dielectric material and has a tensile stress of less than 5×10^8 dynes/cm^2." Claim 67 requires a substrate that is insulated "by a low-stress silicon-based dielectric material with a tensile stress of less than 5×10^8 dynes/cm^2." Claim 58 has no such limitation.

As a reason one of ordinary skill in the art would have combined Hsu and Leedy '695, Petitioner presents the general argument that "*Hsu* and *Leedy '695* are both directed to the improvement of integrated circuits and recognize the central role the fabrication process plays in facilitating this improvement." Pet. 46 (citing Ex. 1008 at 1:7–10, 1:19–33; Ex. 1006 at 1:38–67, 3:56–4:13).

Dr. Franzon's testimony aligns with this argument. Ex. 1002 ¶ 114. However, in the complicated technology field of integrated circuit fabrication, Dr. Franzon's testimony in paragraph 114 is too general in asserting the reason of "they are in the same technology field of three-

dimensional integration and address similar challenges relating to the stacking of integrated circuit devices" without discussing particular challenges must be addressed in making the combination. Ex. 1002 ¶ 113. Although Dr. Franzon lists a string of citations, he does not explain or otherwise reference those citations. We find Petitioner's contention here to be insufficient.

Petitioner relies on purported express motivations of Leedy '695 (tensile strength is important for membrane structural integrity in Leedy '695). Pet. 46. Here, too, Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for Hsu's layer 18. Moreover, as discussed in detail previously, Petitioner characterizes Leedy '695's teaching to be about low tensile stress dielectrics. The citations by Petitioner, discuss advantages of its low tensile stress dielectric flexible membrane or its membrane dielectric isolation fabrication techniques. The probative value of Petitioner's argument is diminished because Petitioner credits Leedy '695's low tensile stress dielectric material with the benefits disclosed by Leedy '695 for its membrane dielectric isolation process for fabricating integrated circuits.

We also find Petitioner's contention (Pet. 47) that plasma-enhanced chemical vapor deposition was well-known, commonly available, and has recognized advantages does not sufficiently support Petitioner's conclusion in view of the complexities of integrated circuit fabrication, as discussed previously.

In view of these complexities, Petitioner's reasoning that dielectrics can easily be substituted in place of others is not persuasive. Pet 48 (citing Ex. 1006 at 6:30–33, 8:59–64; Ex. 1002 ¶¶ 110–120).

Although Petitioner cites to Dr. Franzon's declaration for support, Dr. Franzon's declaration testimony is unavailing. The cited portion of Dr. Franzon's testimony (Ex. 1002 ¶¶ 113–14) does not discuss Hsu's use of PECVD, the implications of Hsu's disclosure on one of ordinary skill in the art's awareness of using use of silicon dioxide dielectric layers, or a purported motivation to look to other references as Petitioner contends. As discussed previously, in this complex technology area of integrated circuit fabrication, expert testimony is critical. *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) ("However, as we [have] noted . . . 'expert testimony regarding matters beyond the comprehension of laypersons is sometimes essential,' particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references." (internal citations omitted)) (alteration in original)). Thus, we find Petitioner's contention to have minimal probative value.

In addition, Petitioner's reasoning that the similarity of the references "constitutes a motivation to look to other references" seems inadequate on its face. Even if true, that statement does not provide a reason would pick out these particular references and combine them to arrive at the claimed invention. *Cf. Personal Web Techs., LLC, v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (concluding "that reasoning seems to say no more than

that a skilled artisan, once presented with the two references, would have understood that they *could* be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention (citing *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.")).

Similarly, in view of the complex technology involved in integrated circuit fabrication and, particularly and the agreement of both experts that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties (as discussed previously), we determine that Petitioner's contentions and Dr. Franzon's broad conclusions (Pet. 49; Ex. 1002 ¶¶ 111, 113–14) that one of ordinary skill in the art would have reasonable expectation of success to be insufficient to meet its burden, which requires a preponderance of evidence. For example, as discussed previously, we find Petitioner's contention that Leedy '695 thus discloses that its dielectrics can be easily used in place of other dielectrics to be insufficiently supported by the evidence of record.

Accordingly, having considered the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers, we determine that Petitioner has not met its burden to demonstrate by a preponderance of the evidence that a person of ordinary skill in the art would have reason to combine the asserted references to arrive at the claimed invention or that a person of ordinary skill would have

had a reasonable expectation of success in making the combination proposed by Petitioner.

5. Conclusion

For the above separate and independent reasons, we conclude that the preponderance of evidence does not support a finding of unpatentability of claims 60, 61, and 67 based on Hsu and Leedy '695.

H. Challenge Based on Bertin '754 and Poole (Claim 58 Only)

Petitioner's challenge to claim 58 based on Bertin '754 and Poole alone was included by Petitioner to deal with a potential alternative claim construction of "substantially flexible." Pet. 58–59. This challenge to claim 58 was made in the event the Board adopted a construction of "substantially flexible" that required only "'an integrated circuit having a semiconductor substrate that has been thinned to a thickness of 150 μm or less,'" which would make reliance on Leedy '695 unnecessary. Pet. 59.

We did not adopt this construction and therefore this challenge has become moot.

III. SUMMARY OF CONCLUSIONS

We now summarize our determinations and conclusions.

"Substantially flexible" is construed to mean "largely able to bend without breaking."

Petitioner has not demonstrated sufficiently that any of the references, singly or taken in combinations as proposed would meet the "substantially flexible" requirement of the claims.

Petitioner has not demonstrated sufficiently that one of ordinary skill would have substituted the dielectric of Leedy '695 into Bertin '754 or Hsu.

We conclude, based on a preponderance of the evidence, that Petitioner has not established that claims 58, 60, 61, and 67 of the '570 patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 58, 60, 61, and 67 of U.S. Patent No. 8,933,570 have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to the proceedings seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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