UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner

v.

TQ DELTA LLC,
Patent Owner

Case IPR2016-01466
Patent No. 8,611,404

PETITIONER'S NOTICE OF APPEAL

via E2E
Patent Trial and Appeal Board

via Hand Delivery
Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

via CM/ECF
United States Court of Appeals for the Federal Circuit

Pursuant to 35 U.S.C. §§ 141-44 and 319, and 37 C.F.R. § 90.2-90.3, notice is hereby given that Petitioner Cisco Systems, Inc. ("Petitioner") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered February 7, 2018 (Paper 34) in IPR2016-01466, and all prior and interlocutory rulings related thereto or subsumed therein.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Cisco Systems, Inc.'s issues on appeal include at least:

(i) the Board erred in failing to find claims 6, 10, 11, 15, 16, and 20 of U.S. Patent No. 8,611,404 unpatentable;

(ii) the Board erred in failing to find claims 6, 10, 11, 15, 16, and 20 obvious over the combination of Bowie, Yamano, and ANSI T1.413;

(iii) the Board erred in construing the term "synchronization signal" to mean "a signal allowing synchronization between the clock of the transmitter of the signal and the clock of the receiver of the signal"; and

(iv) any findings or determinations supporting or related to the aforementioned issues as well as all other issues decided adversely to Cisco Systems, Inc. in any orders, decisions, rulings, phone conference decisions, and/or opinions.

Pursuant to 37 C.F.R. § 90.3, this Notice of Appeal is timely filed within 63 days of the Final Written Decision dated February 7, 2018.

Simultaneously with this submission, Cisco Systems, Inc. is filing a true and correct copy of this Notice of Appeal with the Director of the United States Patent and Trademark Office and a true and correct copy of the same, along with the required docketing fee, with the Clerk of the United States Court of Appeals for the Federal Circuit as set forth in the accompanying Certificate of Filing.

Respectfully submitted,

Dated: April 10, 2018

/David L. McCombs/
David L. McCombs
Reg. No. 32,271

CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PTAB E2E, a true and correct copy of the above-captioned PETITIONER'S NOTICE OF APPEAL is being filed by hand with the Director on April 10, 2018, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

The undersigned also hereby certifies that a true and correct copy of the above-captioned PETITIONER'S NOTICE OF APPEAL and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on April 10, 2018.

Respectfully submitted,

Dated: April 10, 2018

/David L. McCombs/
David L. McCombs
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PETITIONER'S NOTICE OF APPEAL was served electronically via e-mail on April 10, 2018, in its entirety on the following counsel for Patent Owner:

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Paper No. 34
Entered: February 7, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

TQ DELTA, LLC,
Patent Owner.

Case IPR2016-01466
Patent 8,611,404 B2

Before SALLY C. MEDLEY, TREVOR M. JEFFERSON, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Cisco Systems, Inc. ("Petitioner") challenges claims 6, 10, 11, 15, 16, and 20 ("the challenged claims") of U.S. Patent No. 8,611,404 B2 (Ex. 1001, "the '404 patent"), owned by TQ Delta, LLC ("Patent Owner"). We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has not shown by a preponderance of the evidence that the challenged claims are unpatentable. Patent Owner's Motion to Exclude is *dismissed*.

A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 6, 10, 11, 15, 16, and 20 of the '404 patent. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 6. On February 9, 2017, we instituted *inter partes* review of claims 6, 10, 11, 15, 16, and 20 of the '404 patent as unpatentable under 35 U.S.C. § 103(a)[1] over Bowie,[2] Yamano,[3] and ANSI T1.413.[4] Paper 7 ("Inst. Dec."), 26.

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[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the '404 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

[2] U.S. Patent No. 5,956,323; issued Sept. 21, 1999 (Ex. 1005) ("Bowie").

[3] U.S. Patent No. 6,075,814; issued June 13, 2000 (Ex. 1006) ("Yamano").

[4] *Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface*, AMERICAN NATIONAL STANDARDS INSTITUTION (ANSI) T1.413-1995 STANDARD (Ex. 1007) ("ANSI T1.413").

Thereafter, Patent Owner filed a Patent Owner Response (Paper 11, "PO Resp."), to which Petitioner filed a Reply (Paper 14, "Reply"). Pursuant to an Order (Paper 21), Patent Owner filed a listing of alleged statements and evidence in connection with Petitioner's Reply it deemed to be beyond the proper scope of a reply. Paper 22. Petitioner filed a response to Patent Owner's listing. Paper 27.

We held a hearing on November 8, 2017, and a transcript of the hearing is included in the record. Paper 33 ("Tr.").

B. Related Proceedings

The parties indicate that the '404 patent is the subject of several district court cases. Pet. 1; Paper 3, 2–3.

C. The '404 patent (Ex. 1001)

The '404 patent discloses a method and apparatus for establishing a power management sleep state in a multicarrier system. Ex. 1001, 1:31–33. The '404 patent discloses an asynchronous digital subscriber loop (ADSL) system having a first transceiver located at the site of a customer's premises ("CPE transceiver") and a second transceiver located at the local central telephone office ("CO transceiver"). *Id*. at 3:62–67. The transceivers include a transmitter section for transmitting data over a digital subscriber line and a receiver section for receiving data from the line. *Id*. at 4:14–17. The transceivers further include a clock, controller, frame counter, and a state memory. *Id*. at 4:58–5:15. Typically, data is communicated in the form of a sequence of data frames, sixty-eight frames for ADSL, followed by a synchronization frame. *Id*. The sixty-nine frames comprise a "superframe." *Id*.

The power down operation of the CPE transceiver begins on receipt of a power-down indication. *Id*. at 6:27–30. The CPE transceiver responds to the power down indication by transmitting to the CO transceiver an "Intend to Enter Sleep Mode" notification. *Id*. at 6:39–42. The CO transceiver responds by transmitting an "Acknowledge Sleep Mode" notification to the CPE transceiver, and the CPE transceiver transmits an "Entering Sleep Mode" notification to the CO transceiver. *Id*. at 6:52–65. The CO transceiver detects the notification and transmits its own "Entering Sleep Mode" notification. *Id*. at 6:65–67. The CO transceiver stores its state in its own state memory corresponding to the state memory of the CPE transceiver. *Id*. at 6:67–7:2. "The CO transceiver continues to advance the frame count and the superframe count during the period of power-down in order to ensure synchrony with the remote CPE transceiver when communications are resumed." *Id*. at 7:9–12. The CO transceiver further continues to monitor the subscriber line for an "Exiting Sleep Mode" notification, and the CPE transceiver transmits this signal when it receives an "Awaken" indication. *Id*. at 7:57–64. In response to the "Awaken" signal, CPE transceiver retrieves its stored state from state memory and restores full power to its circuitry. *Id*. at 7:64–66. CO Transmitter detects "Exit Sleep Mode" notification and restores its state and power. *Id*. at 8:1–4.

D. Illustrative Claim

Petitioner challenges claims 6, 10, 11, 15, 16, and 20 of the '404 patent. Pet. 22–58. Claims 6, 11, and 16 are independent claims. Claim 6 is illustrative of the claims at issue and is reproduced below:

6. An apparatus comprising a transceiver operable to:

receive, in a full power mode, a plurality of superframes,

> wherein the superframe comprises a plurality of data frames followed by a synchronization frame;
>
> receive, in the full power mode, a synchronization signal; transmit a message to enter into a low power mode;
>
> store, in a low power mode, at least one parameter associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter;
>
> receive, in the low power mode, a synchronization signal; and
>
> exit from the low power and restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

Ex. 1001, 10:29–43.

II. ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

1. "store/storing, in a/the low power mode"

In our Decision on Institution, we construed "store/storing in a/the low power mode" to mean "maintaining in memory while in a reduced power consumption mode." Inst. Dec. 6–7. Neither party addressed this

construction in subsequent briefing. Based on the record developed during this proceeding, we continue to apply this construction.

2. "synchronization signal"

Each independent claim recites a "synchronization signal." In our Decision on Institution, we construed this term to mean "a signal allowing frame synchronization between the transmitter of the signal and the receiver of the signal." Inst. Dec. 5–6.

Patent Owner argues that our construction is not consistent with the ordinary meaning of the claim language, and proposes to construe this term to mean "a signal used to maintain a timing relationship between transceivers by correcting errors or differences between a timing reference of the transmitter of the signal and a timing reference of the receiver of the signal." PO Resp. 17–18. Patent Owner agrees with Petitioner's reliance on the timing reference signal disclosed in the '404 patent (*id.* at 19–20 ("The parties agree that the timing reference signal that is transmitted by the CO is an embodiment of the claimed synchronization signal")), but argues that the timing reference signal provides for timing synchronization between two transceivers—i.e., to synchronize their respective clocks—not for frame synchronization—i.e., to detect the boundaries of the transmitted superframe (*id.* at 18). According to Patent Owner, Petitioner's reliance on lines 50 to 52 of column 5 of the '404 patent is misplaced because that passage describes synchronizing the timing of the transceivers' respective frame counters—i.e., timing synchronization—not detecting superframe boundaries—i.e., frame synchronization. *Id.* at 19. Patent Owner also argues that the recited "synchronization signal" cannot encompass frame synchronization because the claims separately recite a "synchronization

frame," which provides frame synchronization. *Id.* at 18. Finally, Patent Owner argues that its proposed construction is correct because a "synchronization signal" is used to maintain timing synchronization by correcting or compensating for errors or differences between the timing references of the transmitter of the signal and the receiver of the signal. *Id.* at 20–21.

Petitioner, in its Reply, argues that "synchronization signal" should encompass *both* frame synchronization *and* timing synchronization. Pet. Reply 5–6. Petitioner argues that the construction proposed in Patent Owner's Response is not the broadest reasonable interpretation because "it was proposed specifically in response to the analysis in Dr. Kiaei's declaration" and because "it relies on a dictionary definition of a different term and fails to refer to anything in the specification." *Id.* at 7.

Having considered the arguments and evidence, we agree with Patent Owner that our construction in the Decision to Institute is overly broad to the extent it encompasses a synchronization frame. Column 5, lines 50 to 52 of the '404 patent, on which we relied and which we reproduce below for context, describes "normal (non-sleep mode) operation":

> During normal (non-sleep mode) operation, a phase-lock loop (PLL) 62 receives from the FFT 56 a timing reference signal 62a (see FIG. 1A) via a line 62b. The timing reference signal 62a is transmitted from the transmitter with which the receiver 16 communicates (e.g., the CO transmitter). This signal is advantageously a pure tone of fixed frequency and phase which is synchronized with the Master Clock in the transmitter; its frequency defines the frame rate of the transceivers. Other forms of timing signal may, of course, be used, but use of a pure tone has the advantage of simplicity and reliability even when portions of the transceiver are powered down in accordance with the invention. The PLL 62 locks itself to this signal and drives

> clock 30 in synchronism with the Master Clock in the driving transmitter. *This also synchronizes frame counter 34 of the CPE transceiver to the corresponding frame counter of the CO transceiver.* Control of the receiver section is provided by the controller 32.

Ex. 1001, 5:37–53 (emphasis added to 5:50–52). We agree with Patent Owner that the italicized "this" refers to what is disclosed in the preceding sentence—i.e., driving clock 30 in synchronism with the Master Clock in the driving transmitter. PO Resp. 19. The synchronism of clock 30 with the Master Clock in the driving transmitter is what "synchronizes frame counter 34 of the CPE transceiver to the corresponding frame counter of the CO transceiver." Ex. 1001, 5:50–52.

We also agree with Patent Owner that a "synchronization signal" should not be construed to encompass a synchronization frame because the claims separately recite a "synchronization frame." Claim 6, for example, recites:

> receive, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of data frames followed by a *synchronization frame*;
>
> receive, in the full power mode, *a synchronization signal*;

Ex. 1001, 10:30–33 (emphases added). If we were to construe "synchronization signal" to encompass a synchronization frame, the step of "receive, in the full power mode, a synchronization signal" would be duplicative because a synchronization frame would have been received, in full power mode, when "receiv[ing], in full power mode, a plurality of superframes." *Id.* "A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so." *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Circ. 2005).

Notwithstanding our agreement with Patent Owner that "synchronization signal" should not encompass a synchronization frame, we are not persuaded that Patent Owner's proposed construction is correct because it also is overly broad. Whereas our preliminary construction required "allowing frame synchronization between the transmitter of the signal and the receiver of the signal," Patent Owner's proposed construction replaces that with the more general "used to maintain a timing relationship between transceivers." PO Resp. 17. Patent Owner does not attempt to find support in the '404 patent for "timing relationship," relying instead upon the testimony of its declarant. Id. at 17–18 (citing Ex. 2005 ¶ 81). Moreover, "timing relationship" is arguably broad enough to encompass the timing of superframe boundaries and, therefore, encompass the very frame synchronization that Patent Owner tries to distinguish. Patent Owner proposes to limit the way in which the timing relationship is maintained to "by correcting errors or differences between a timing reference of the transmitter of the signal and a timing reference of the receiver of the signal," (*id.*), but Patent Owner again relies not upon the Specification for that language, but upon a dictionary definition. Because portions of Patent Owner's proposed construction lack support in the Specification and would encompass the very synchronization frame that we are persuaded should be excluded, we determine that Patent Owner's proposed construction also is overly broad.

Because both parties agree that timing reference signal 62a corresponds to the recited "synchronization signal" and because the only purpose disclosed for timing reference signal 62a is being used by PLL 62 to "drive[] clock 30 in synchronism with the Master Clock in the driving

transmitter," we determine that "synchronization signal" means "a signal allowing synchronization between the clock of the transmitter of the signal and the clock of the receiver of the signal."

3. "parameter associated with the full power mode operation"

Patent Owner proposes construing this term to mean "parameter associated with the transmission and/or reception of data during normal operation." PO Resp. 21. The '404 patent describes storing a list of parameters comprising the "state" of transceiver. Ex. 1001, 6:67–7:9. Patent Owner argues that this list "includes only communication protocol-specific parameters that are used for the transmission and/or reception of data – it does not include loop characteristics." PO Resp. 22.

Petitioner counters that the term should have its ordinary and customary meaning. Pet. Reply 8. Petitioner also argues that the rest of the limitation—reciting "a fine gain parameter and a bit allocation parameter"—provide sufficient meaning. *Id.*

Having considered the arguments and evidence, we are not persuaded that this term requires an express construction. Patent Owner's proposed construction merely replaces "full power mode operation" with "transmission and/or reception of data during normal operation." The parties, however, do not dispute the meaning of "full power mode operation." As a result, an express construction of this term is not necessary in order to resolve the parties' dispute.

B. Level of Ordinary Skill in the Art

Petitioner contends that a hypothetical person of ordinary skill in the art, with respect to and at the time of the'404 patent, "would have (i) a

Master's degree in Electrical and/or Computer Engineering, or equivalent training, and (ii) approximately five years of experience working in digital telecommunications." Pet. 13.

Patent Owner contends that such a person would have had "a bachelor's degree in electrical engineering (or a similar technical degree or equivalent work experience) and at least 3 years of experience working with such multicarrier communication systems." PO Resp. 17.

We determine that no express finding on a specific corresponding level of technical education and experience is necessary. Here, the level of ordinary skill in the art is reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Obviousness over Bowie, Yamano, and ANSI T1.413

Petitioner contends that claims 6, 10, 11, 15, 16, and 20 of the '404 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowie, Yamano, and ANSI T1.413. Pet. 13–61.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness

(i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Bowie Overview

Bowie discloses a power conservation system for transmission systems in which data is modulated over a communications loop from a central office location to a customer premise. Ex. 1005, 1:4–8. Bowie discloses that to provision ADSL service, ADSL units are located at each end of a wire loop, a first ADSL unit at the customer premises (CPE) and a second ADSL unit at the telephone company central office (COT). *Id.* at 3:51–58. Data is arranged in a structure known as a "frame" prior to transmission. *Id.* at 3:66–67.

ADSL units enter a low power mode to reduce power requirements. *Id.* at 5:6–8. CPE unit initiates low power mode by sending a "shut-down" signal to the COT unit. *Id.* at 5:8–10. Both the CPE unit and COT unit may store loop characteristics that enable rapid resumption of user data transmission when units return to full power mode. *Id.* at 5:17–25. Each unit then enters low power mode by shutting off the now unnecessary sections of the signal processing, transmitting, and receiving circuitry. *Id.* at 5:26–28. After shutdown, the loop is in an inactive state. *Id.* at 5:28–29.

The units return to full power mode after the CPE unit transmits to the COT unit a resume signal. *Id.* at 5:48–59. The stored loop characteristics are used to restore the loop parameters. *Id.* at 5:60–66.

3. Yamano Overview

Yamano discloses a method for the reduction of the required amount of signal processing in a modulator and demodulator transferring packet-

based data. Ex. 1006, 1:9–13. Yamano discloses an embodiment where a transmitter circuit transmits a predetermined non-idle state signal to indicate that packet data is about to be transmitted prior to the transmission of packet data. *Id.* at 13:56–59. If the non-idle state signal is not transmitted, the transmitter does not transmit any signals on the communication channel, and, therefore, the transmitter does not transmit any idle information. *Id.* at 13:59–63. Upon detection of the predetermined non-idle state signal, the receiver enters full processing mode and performs full demodulation of the incoming signal. *Id.* at 14:25–29. After the packet data has been received, the receiver detects the absence of the predetermined non-idle state signal and the receiver enters a reduced processing mode by disabling several components of the receiver. *Id.* at 14:29–42.

4. ANSI T1.413 Overview

ANSI T1.413 discloses electrical characteristics of Asymmetric Digital Subscriber Line (ADSL) signals appearing at a network interface. Ex. 1007, Abstract. ADSL allows for the provision of Plain Old Telephone Service (POTS) and a variety of digital channels. *Id.* at 1. Digital channels consist of full duplex low-speed channels and simplex high-speed channels in the direction from the network to the customer premises, and low-speed channels in the opposite direction. *Id.*

5. Analysis

Petitioner contends that a combination of Bowie, Yamano, and ANSI T1.413 would have rendered obvious claims 6, 10, 11, 15, 16, and 20 of the '404 patent. Pet. 13–61. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are not persuaded that the

record establishes Petitioner's contentions for claims 6, 10, 11, 15, 16, and 20.

Each independent claim recites a "synchronization signal." Claim 6 recites "receive, in the full power mode, a synchronization signal." Claim 11 recites "transmitting, in the full power mode, a synchronization signal." Claim 16 recites "receiving, in the full power mode, a synchronization signal."

For these limitations, the Petition relies upon ANSI T1.413's teachings of a synchronization frame within a superframe:

> [ANSI] T1.413 teaches that a synchronization symbol is included in one of the frames transmitted and received by the ADSL units. Ex. 1003 at p.46. As shown in figure 5 of ANSI T1.413, a synchronization symbol is included as the last frame of a superframe.
>
> . . .
>
> ANSI T1.413 teaches that the synchronization symbol is used to maintain timing by correcting timing errors in the communication between DSL transceivers. Ex. 1007 at p. 64 ("correction of such timing errors is made possible by the use of the synchronization symbol defined in 6.9.3."). "The synchronization symbol permits recovery of the frame boundary after micro-interruptions that might otherwise force retraining." Ex. 1007 at p. 64. The synchronization symbol is "inserted after every 68 data symbols" and includes no user or bit-level data. Ex. 1007 at 42; 64.

Pet. 35–36; *see also id.* at 51 (corresponding limitation of independent claim 11), 59 (corresponding limitation of independent claim 16).

Patent Owner argues that the synchronization frame of ANSI T1.413 does not teach a "synchronization signal." PO Resp. 37–38.

In the Reply, Petitioner contends that a person of ordinary skill in the art "would understand that a synchronization symbol in the ANSI specification is a type of synchronization signal because it is used to maintain timing synchronization with a remote transceiver." Pet. Reply 15 (citing Ex. 1003, 46–49; Ex. 1007, 62).

We agree with Patent Owner. The contentions in the Petition and Reply are based upon Petitioner's proposed construction of "synchronization signal" as encompassing a synchronization frame—i.e., "allowing for frame synchronization." *See, e.g.*, Pet. 11–12, 35–36. We have not adopted that construction, however, for the reasons discussed above. Because our construction of "synchronization signal" excludes a synchronization frame, we are not persuaded that the argument and evidence in the Petition and Reply shows that the combination of Bowie, Yamano, and ANSI T1.413 teaches transmitting/receiving, in full power mode, a "synchronization signal."

As a result, Petitioner has not shown, by a preponderance of the evidence, that claims 6, 10, 11, 15, 16, and 20 would have been obvious over Bowie, Yamano, and ANSI T1.413.

D. Patent Owner's Motion to Exclude

Patent Owner filed a Motion to Exclude (Paper 25, "Motion"). Petitioner filed an Opposition to Patent Owner's Motion (Paper 31, "Opp."), and Patent Owner filed a Reply in support of its Motion (Paper 32). As movant, Patent Owner has the burden of proof to establish that it is entitled to the requested relief. *See* 37 C.F.R. § 42.20(c).

We decline to assess the merits of Patent Owner's Motion to Exclude. Even without excluding the identified evidence, we have concluded that

Petitioner has not demonstrated, by a preponderance of the evidence, that the challenged claims are unpatentable. Accordingly, Patent Owner's Motion to Exclude is *dismissed* as moot.

III. CONCLUSION

Petitioner has not demonstrated, by a preponderance of the evidence, that claims 6, 10, 11, 15, 16, and 20 of the '404 patent are unpatentable under 35 U.S.C. § 103(a) over Bowie, Yamano, and ANSI T1.413.

IV. ORDER

Accordingly, it is

ORDERED that claims 6, 10, 11, 15, 16, and 20 of the '404 patent are not held *unpatentable*;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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