UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DIABLO TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00883
Patent 8,081,536 B1

NETLIST, INC.'S NOTICE OF APPEAL

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via E2E
Patent Trial and Appeal Board

via Hand Carry
Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

via CM/ECF
United States Court of Appeals for the Federal Circuit

INTRODUCTION

Netlist, Inc.'s appeal stems from the Patent Trial and Appeal Board's Decision On Remand entered on March 29, 2018 (Paper 36) (the "Remand Decision") in the above-captioned *inter partes* review of United States Patent No. 8,081,536 B1 ("the '536 patent"). This notice is timely filed within 63 days of the Board's Remand Decision. 37 C.F.R. § 90.3.

NETLIST, INC.'S APPEAL

Please take notice that under 35 U.S.C. §§ 141(c), 142, 319; 37 C.F.R. §§ 90.2(a), 90.3; and Federal Rules of Appellate Procedure/Federal Circuit Rule 15, Patent Owner Netlist, Inc. hereby appeals to the United States Court of Appeals for the Federal Circuit from the Remand Decision and all underlying decisions and orders in this action on which that decision is based.

NETLIST, INC.'S ISSUES ON APPEAL

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Netlist, Inc.'s issues on appeal include at least: (i) the Board's finding that claims 1, 16-17, 24, and 30-31 of the '536 patent have been shown to be unpatentable as obvious over combinations of U.S. Patent Publications No. 2001/0008006 A1 by Klein and No. 2006/0117152 A1 by Amidi and U.S. Patent No. 6,446,184 B2 to Dell; (ii) the Board's claim constructions; and (iii) any findings or determinations supporting or related to the aforementioned issues as well as other issues decided adversely to Netlist, Inc. in

any order, decisions, rulings, or opinions.

Simultaneously with this submission, Netlist, Inc. is filing a true and correct copy of this Notice of Appeal with the Director of the United States Patent and Trademark Office and a true and correct copy (or copies) of the same, along with the required filing fee, with the Clerk of the United States Court of Appeals for the Federal Circuit as set forth in the accompanying Certificate of Filing.

Dated: May 30, 2018

Respectfully submitted,

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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through E2E, a true and correct copy of the above-captioned NETLIST, INC.'S NOTICE OF APPEAL is being filed by hand with the Director on May 30, 2018, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

The undersigned also hereby certifies that a true and correct copy of the above-captioned NETLIST, INC.'S NOTICE OF APPEAL and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on May 30, 2018.

Dated: May 30, 2018

Respectfully submitted,

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CERTIFICATION OF SERVICE

The undersigned hereby certifies that the foregoing NETLIST, INC.'S NOTICE OF APPEAL was served electronically via e-mail on May 30, 2018, by agreement of the parties, in its entirety on the following:

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Paper 36
Entered: March 29, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DIABLO TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00883
Patent 8,081,536 B1

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

DECISION ON REMAND
35 U.S.C. § 144 and 37 C.F.R. § 42.5(a)

I. INTRODUCTION

This Decision addresses the order of the United States Court of Appeals for the Federal Circuit in *Netlist, Inc. v. Diablo Technologies, Inc.*, 701 F. App'x 1001 (Fed. Cir. 2017) ("*Netlist*"), vacating our opinion with respect to U.S. Patent 8,081,536 B1 (Ex. 1001 ("the '536 patent")), and remanding for further proceedings. Having analyzed the entirety of the record anew in light of the court's directive in *Netlist*, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 of the '536 patent are unpatentable.

A. Procedural History

Diablo Technologies, Inc. ("Petitioner") filed a Petition (Paper 4, Corrected Petition ("Pet.")) requesting *inter partes* review of claims 1, 16, 17, 24, 30, and 31 of the '536 patent. On the same day, Diablo also filed petitions requesting *inter partes* review of U.S. Patent 7,881,150 B2 ("the '150 patent) in *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-00882 ("IPR882") and *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-01011 ("IPR1011"). The '536 patent is a continuation of the application that issued as the '150 patent. Ex. 1001, (63).

In its Petition, Petitioner did not assert that any claim terms required express construction. *See* Pet. 9–11. Netlist, Inc. ("Patent Owner"), however, filed a Preliminary Response to the Petition wherein it proposed a construction for the claim term "selectively isolate" or "selectively isolating," recited in challenged independent claims 1 and 24, respectively. Paper 8 ("Prelim. Resp."), 14–15.[1]

[1] For convenience, our discussion below refers to the term "selectively

In our Institution Decision, we agreed that express construction of the term "selectively isolating" was necessary, but determined Patent Owner had not proposed the broadest reasonable construction of this term. *See* Paper 11 ("Inst. Dec."), 8–9. Accordingly, we applied our own construction of "selectively isolating" in instituting an *inter partes* review of '536 patent claims 1, 16, 17, 24, 30, and 31. *See generally*, *id.* at 10–26.

Patent Owner subsequently filed a Patent Owner Response (Paper 25 ("PO Resp.")), and Petitioner filed a Reply (Paper 27). An oral hearing, consolidated with related cases IPR882 and IPR1011, was held on July 28, 2015. Paper 31 (Record of Oral Hearing).

On December 14, 2015, this Board issued a Final Written Decision in the present *inter partes* review, wherein we adopted our construction of "selectively isolating" from the Institution Decision. Paper 33 ("Final Decision" or "Final Dec."), 8 (noting neither party challenged this construction after institution). In the Final Decision, all challenged claims of the '536 patent were determined to be unpatentable as follows:

References	**Basis**	**Claims Challenged**	**Claims Held Unpatentable**
Klein[2] & Amidi[3]	§ 103	1, 16, 17, 24, 30, and 31	1, 16, 17, 24, 30, and 31
Klein, Amidi, & Dell[4]	§ 103	16, 17, 30, and 31	16, 17, 30, and 31

Final Dec. 37. We likewise applied our own constructions of the '150 patent

isolating." However, our findings and conclusions also apply to the term "selectively isolate."

[2]U.S. Patent Publication 2001/0008006 A1(Ex. 1006).

[3] U.S. Patent Publication 2006/0117152 A1 (Ex. 1008).

[4] U.S. Patent 6,446,184 B2 (Ex. 1009).

claim term "selectively isolating," and related term "selectively electrically coupling" in holding unpatentable all challenged claims of the '150 patent in both IPR882 and IPR1011. IPR882, Paper 33; IPR1011, Paper 34.

Patent Owner filed a Notice of Appeal to the United States Court of Appeals for the Federal Circuit requesting review of our unpatentability determinations. Paper 34. The Federal Circuit consolidated the appeal from our decision in the present *inter partes* review with Patent Owner's concurrently-filed appeals from our decisions in related cases IPR882 and IPR1011. *Netlist*, 701 F. App'x. at 1002.

On July 25, 2017, the Federal Circuit issued a decision determining that we erred in our construction of the '150 patent claim term "selectively electrically coupling." *Netlist*, 701 F. App'x at 1005. The court further determined that because the construction of "selectively isolating" applied in our analysis of the challenges to the '150 patent claims was based on an erroneous construction of "selectively electrically coupling," we likewise erred in the construction of "selectively isolating" applied in IPR882 and IPR1011. *Id.* (noting that "[t]he specification uses the terms 'coupling' and 'isolating' in a similar fashion"). The court observed that we had construed the term "selectively isolating" differently in the present *inter partes* review, but found the record was unclear as to which construction of "selectively isolating" we actually had applied in our analysis of the challenges to the '536 patent. *Id.* at 1005–06. The court directed us on remand to construe "selectively isolating" in view of its construction of "selectively electrically coupling," and to reconsider whether the references disclose circuits that are capable of selectively isolating based on our new construction. *See id.* at 1005.

The court's mandate issued on August 31, 2017. Neither party sought to provide additional briefing or requested that we take new evidence upon remand. Here, we determine that no new argument or evidence is necessary because the claim construction we apply on remand was proposed by Patent Owner (*compare* Prelim. Resp. 14–15, *with* Section II *infra*) and "the effect thereof has been fully briefed" (Patent Trial and Appeal Board Standard Operating Procedure ("SOP") 9[5] (Rev. 1), 8). *Cf. Netlist*, 701 F. App'x at 1005 ("Indeed, the parties below raised factual disputes about whether prior art circuits perform selective electrical coupling, even under Netlist's construction. . . . But because the Board based its conclusions of obviousness and anticipation on an erroneous construction, the Board must assess these factual issues on remand."). We address the errors identified by the Federal Circuit in view of the record as of December 14, 2015, the date of issuance of the Board's Final Decision. For the reasons that follow, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 of the '536 patent are unpatentable.

B. The '536 Patent

The '536 patent is described in the Final Decision. *See* Final Dec. 3–7. A summary description is provided below.

[5] SOP 9 addresses the procedure for handling all decisions on cases remanded from the Court of Appeals for the Federal Circuit to the Patent Trial and Appeal Board for further proceedings. SOP 9 currently is available at https://www.uspto.gov/sites/default/files/documents/sop_9_%20procedure_for_decisions_remanded_from_the_federal_circuit.pdf.

The ’536 patent relates to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:35–38. The memory module includes a plurality of memory devices (arranged in ranks), and a circuit electrically coupled to the memory devices. *Id.* at 5:28–32, Fig. 1. The circuit includes a logic element, such as a complex programmable-logic device (CPLD). *Id.* at 6:40–45. In response to a set of input address and command signals from a memory controller, the circuit generates a set of output address and command signals (*id.* at 16:37–44), whereby the circuit selectively isolates the loads of some of the memory devices from the computer system (*id.* at 7:17–19).

Figure 3A, reproduced below, is a schematic diagram of a circuit in accordance with certain embodiments of the invention. *Id.* at 4:14–18.

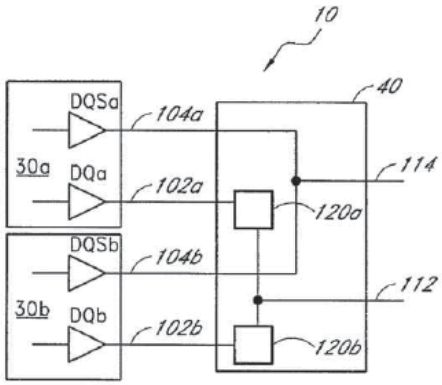


FIG. 3A

As shown in Figure 3A, the logic element of circuit 40 uses switches 120a, 120b to selectively isolate one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b from common data signal line 112. *Id.* at 4:15–17, 7:38–41. By selectively isolating the loads of unaccessed memory devices, the capacitive load on the memory controller can be substantially reduced. *Id.* at 7:27–31.

II. CLAIM CONSTRUCTION

"A claim in an unexpired patent that will not expire before a final written decision is issued shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). Pursuant to that standard, the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). "[W]here multiple patents 'derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents.'" *SightSound Tech., LLC v. Apple Inc.*, 809 F.3d 1307, 1316 (Fed. Cir. 2015) (quoting *NTP, Inc. v. Research in Motion, Ltd.*, 418 F.3d 1282, 1293 (Fed. Cir. 2005)).

In our Final Decision, we construed the terms "selectively isolating" and "circuit configured to be mounted on a memory module." *See* Final Dec. 8–11. The Federal Circuit agreed with our construction of "circuit configured to be mounted on a memory module," but determined we erred in our construction of "selectively isolating." *See Netlist*, 701 F. App'x at 1004–05. As instructed by the court, below we construe the term "selectively isolating" in view of the court's construction of the '150 patent claim term "selectively electrically coupling." *See id.* at 1005–06.

"Selectively isolating" is recited in challenged '536 patent claims 1 and 24 as follows:

> 1. A circuit configured to be mounted on a memory module configured to be operationally coupled to a computer system, the memory module having a first number of ranks, each rank of the first number of ranks comprising a plurality of double data-rate (DDR) memory circuits . . . , the circuit including at least one configuration in which the circuit is configured to . . . *selectively isolate* a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of [address and DDR chip-select] signals . . . .

Ex. 1001, 41:20–24, 27–29, 36–39 (emphasis added).

> 24. A method of operating a memory module configured to be operationally coupled to a computer system, the memory module having a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits . . . the method comprising . . . *selectively isolating* a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of [address and DDR chip-select] signals . . . .

Id. at 43:18–22, 25–26, 33–36 (emphasis added).

As noted above, Petitioner did not propose an explicit construction of "selectively isolating." *See* Pet. 9–11. In its Preliminary Response, Patent Owner proposed construing the term "selectively isolating" as "isolating in response to a selection." Prelim. Resp. 15. In support of this construction, Patent Owner cited column 7, line 32 through column 8, line 56 of the '536 patent (Prelim. Resp. 15) which discloses, with reference to Figures 3A, 3B, that by selectively isolating DQ data signal line 102a of memory device 30a from common DQ data signal line 112, which is coupled to the computer system, circuit 40 "selectively allows" (1) a DQ data signal to be transmitted from the memory controller of the computer system to DQ data signal line

102b of memory device 30b, and (2) a DQ data signal from DQ data signal line 102b of memory device 30b to be transmitted to the memory controller via common DQ data signal line 112 (*see* Ex. 1001, 7:32–48). The '536 patent explains that by selectively isolating DQ data signal line 102a and DQS data strobe signal line 104a of memory device 30a (i.e., the memory device that is not being accessed by the computer system) from the common data signal and data strobe signal lines 112, 114 to the memory controller, the load from memory device 30a is isolated from the memory controller, thereby reducing the capacitive load on the memory controller. *Id.* at 7:9–16, 27–31. The '536 patent describes DQ data signal line 102b (i.e., the data signal line to the memory device that is being accessed by the computer system), as "selectively electrically couple[d]" to common DQ signal line 112. *See id.* at 7:55–8:3.

In construing the '150 patent claim term "selectively electrically coupling," the Federal Circuit determined that this term "is directed to *how* the circuit performs th[e] function [of activating some memory devices and not others], which is by coupling or decoupling specific data signal lines." *Netlist*, 701 F. App'x at 1005. Noting that "the claims call out exactly which two data lines must be coupled," the court determined that our construction of "selectively electrically coupling" as "making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component," was unreasonable. *Id.* at 1004–05. The court explained that "the 'selection' is to couple or uncouple the first/second data signal line to the common signal line, not to select among multiple components." *Id.* at 1005.

The above cited disclosure in the '536 patent similarly is directed to how the circuit performs the function of reducing the load to the computer system, which is by isolating the load of specific memory devices from the memory controller, and to how the circuit performs the function of preventing data transmission between a specific memory device and the computer system, which is by isolating specific data signal lines from the common signal line.

In its arguments in support of patentability, Patent Owner asserts that the term "selectively isolating" requires electrical separation. *See* PO Resp. 47. Patent Owner's assertion is based on the declaration testimony of its expert, Dr. Carl Sechen, who testified that one of ordinary skill in the art would understand the description of load isolation at column 5, lines 39–44 of the '536 patent as meaning "'electrical separation' of an 'electrical load.'" Ex. 2002 (Declaration of Dr. Carl Sechen) ¶ 66; *see also* Ex. 1025 (Transcript of Dr. Carl Sechen's deposition), 133:6–14. Dr. Sechen further testified that in a system in which the chip select signal lines and the data bus lines are permanently hard-wired via an electrical conduit to the memory devices, load isolation is not possible without switches on these lines to enable electrical decoupling. *Id.* ¶ 78.

We are not persuaded that the broadest reasonable construction of "selectively isolating" requires electrical separation. Dr. Sechen's testimony is not supported by the relied-upon disclosure in the '536 patent, which reads as follows:

> As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, *the term "isolation" is a broad term which includes, without*

> *limitation, electrical separation* of one or more components from another component or from one another.

Ex. 1001, 5:39–44 (emphasis added). Nor do we find any other disclosure in the '536 patent that supports a broadest reasonable construction of the claim term "selectively isolating" as requiring electrical separation. To the contrary, use of the term "electrically" throughout the '536 patent to specify how the data signal lines are selectively coupled, suggests that the inventors did not intend to limit how the data signal lines are selectively isolated or the type of loads that are selectively isolated. *See, e.g.*, Ex. 1001, 9:17–21 ("In certain embodiments, the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (*e.g.*, *electrical load*, such as capacitive load, inductive load, or impedance load) to the computer system." (emphasis added)); *id.* at 10:13–15 ("In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading."). Because we are not persuaded that the claim term "selectively isolating" requires electrical separation, we also decline to construe this term as requiring a switch or other specific component that would enable electrical decoupling. *See Netlist*, 701 F. App'x at 1005 ("To be clear, we do not limit 'selectively electrically coupling' to a switch or other specific component. Nor do we hold that 'selectively electrically coupling' necessarily precludes a hard-wired connection.").

Accordingly, consistent with the Federal Circuit's determination that the broadest reasonable construction of "selectively electrically coupling" is "coupling in response to a selection," *id.* at 1004, we determine the broadest

reasonable construction of the claim term "selectively isolating" is "isolating in response to a selection."[6]

III. ANALYSIS

To prevail in its patentability challenges, a petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). In its decision, the Federal Circuit found that we applied an erroneous construction of "selectively isolating" in determining Petitioner had met its burden to prove unpatentability. *See Netlist*, 701 F. App'x at 1005. Following the court's directive in its construction of the '150 patent claim term "selectively electrically coupling," in this decision, we construe "selectively isolating" as "isolating in response to a selection." *See* Section II *supra*. As instructed by the court, we apply this construction in reconsidering whether Petitioner has met its burden to show that the combination of Klein and Amidi discloses "selectively isolating." *See id.* at 1005–06. The court did not identify any other error in our findings and, therefore, we do not revisit our determinations that: the combination of Klein and Amidi discloses or suggests all other limitations of challenged claims 1, 16, 17, 24, 30, and 31; the combination of Klein, Amidi and Dell, discloses or suggests all other limitations of challenged claims 16, 17, 30, and 31; and that one of ordinary skill in the art would have had a reason to combine these references and a reasonable expectation of success in so doing. *See generally*, Final Dec. 20–37.

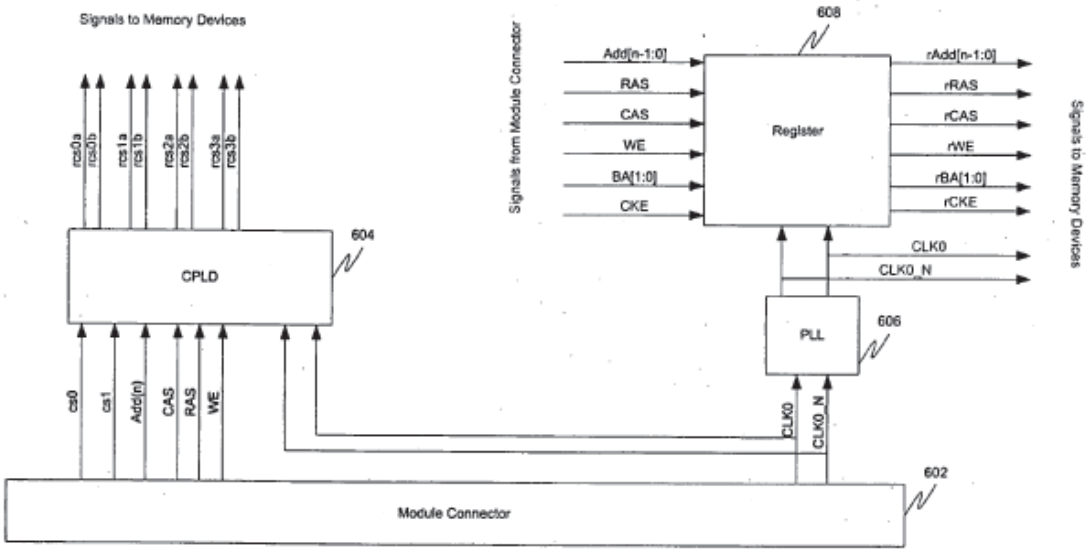
[6] We apply the same construction of this term in our decisions on remand in IPR882 and IPR1011.

A. The Prior Art

The prior art is described in the Final Decision. *See* Final Dec. 15–20. Below we provide summary descriptions.

1. Amidi (Ex. 1008)

Amidi discloses a transparent four rank memory module for use in a standard two rank sub-system. Ex. 1008, Title. As illustrated in Figure 6A, below, Amidi's memory module includes complex programmable logic device ("CPLD") 604, phase-lock loop ("PLL") 606, and register 608. *Id.* ¶¶ 28, 50.



Row Address Decoding
FIG.6A

Figure 6A is a block diagram schematically illustrating a row address decoding system for a transparent four rank memory module in accordance with an embodiment of Amidi's invention. *Id.* ¶ 21. Module connector 602 sends signals from a memory controller (not shown) to CPLD 604, PLL 606, and register 608. *Id.* ¶¶ 38, 50. The signals sent to CPLD 604 include chip select, row address, and column address signals. *Id.* ¶¶ 41, 50. CPLD 604

includes internal decoding circuitry for determining which rank from the four ranks of memory devices to activate based upon the address and command signals from the memory controller. *See id.* ¶¶ 41, 43, 57, 61. CPLD 604 generates and relays the command signals to activate a rank of memory devices. *Id.* ¶ 62.

2. Klein (Ex. 1006)

Klein discloses a method for reducing data bus capacitance "by decoupling unaccessed memory circuits from a data bus during data transfers to or from other memory circuits." Ex. 1009, Abstract. An embodiment of Klein's method is described in connection with Figure 6, reproduced below.

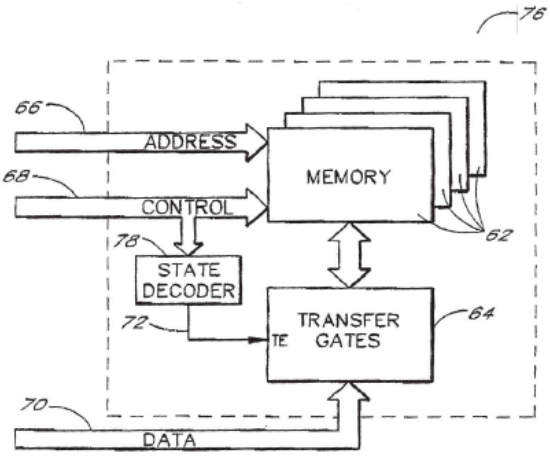


FIG. 6

Figure 6 is a block diagram illustrating memory module 76. *Id.* ¶¶ 16, 35. Memory module 76 includes memory elements 62, transfer gates 64, and electrical contacts for interfacing with address bus 66, control lines 68, and data bus 70. *Id.* ¶ 35. Memory module 76 further includes state decoder 78 for receiving one or more control signals from the host system. *Id.* "[S]tate decoder 78 decodes the signals on the control lines to determine whether or not a memory access to or from the module is being made, and

asserts the gate control signal 72 to open the transfer gates 64 when a memory access is being made." *Id.* Klein discloses that state decoder 78 may be an inverter which has chip select signal 82 as an input. *Id.* ¶ 36. Klein discloses that transfer gates 64 may be constructed as described in Figure 2 (*id.* ¶ 32), which shows a bus switch comprising one or more n-channel MOSFET transistors with commonly connected gates 15, an input portion and an output portion for connection to one or more lines of a bus (*id.* ¶ 25). The transistors are turned on by asserting the gates via an input transfer enable ("TE") signal line. *Id.* ¶ 26. "The switch . . . therefore decouples or isolates the bus segments when the transistors comprising the switch are in the off state, and couples or connects the bus segments when the transistors comprising the switch are in the on state." *Id.* Figure 3 of Klein is reproduced below.

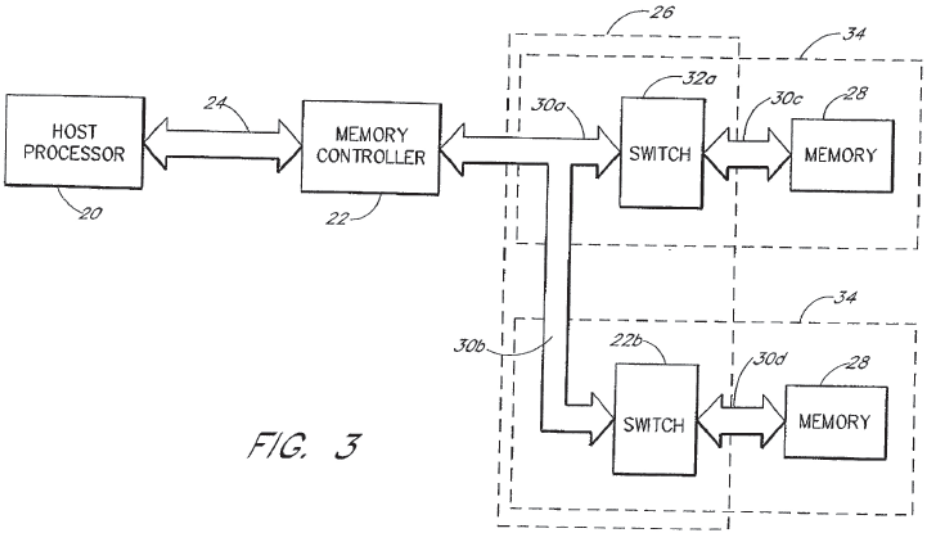


FIG. 3

Figure 3 is a block diagram of a computing system including host processor 20 that interfaces with memory controller 22 which, in turn, connects to circuitry 26 for interfacing with one or more memory elements 28 on memory module 34. *Id.* ¶¶ 13, 27–29. Circuitry 26 includes data bus

30*a–d* for transferring data between memory elements 28 and memory controller 22. *Id.*

> [T]he data bus between the memory controller 22 and memory elements 28 may comprise several branches 30*a*, 30*b*, one for each of the separate memory elements 28. Each branch may include a switch 32*a*, 32*b* that . . . may be used to selectively isolate portions or segments 30*c*, 30*d* of the data bus running from the memory controller to the memory circuitry 28.

Id. at 28.

> [B]y turning the switches 32a and 32b on or off, one or the other memory [device] 28 may be removed from the data bus. For example, when the host processor requires data in the memory [device] 28 connected to bus segment 30c, switch 32a may be switched on, while switch 32b may be switched off. Thus, the design of FIG. 3 may reduce the parasitic capacitance that the memory controller needs to charge and discharge during data transfers because a portion of the data bus and the stray capacitance of unaccessed memory circuits are removed.

Id.

B. Alleged Obviousness of claims 1, 16, 17, 24, 30 and 31 over Klein and Amidi, and of claims 16, 17, 30, and 31 over Klein, Amidi, and Dell

Independent claim 1 recites: "the circuit is configured to . . . *selectively isolate* a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of [address and DDR chip-select] signals . . . ." Ex. 1001, 41:27–29, 36–39 (emphasis added). Independent claim 24 recites: "the method comprising . . . *selectively isolating* a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of [address and DDR chip-select] signals . . . ." *Id.* at 43:25–26, 33–36 (emphasis added). Petitioner

relies on the declaration testimony of Srinivasan Jagannathan, Ph.D. in support of its contention that the combination of Amidi and Klein discloses these claim limitations. *See* Pet. 18; Ex. 1011 (Declaration of Dr. Srinivasan Jagannathan); Ex. 1026 (Supplemental Declaration of Dr. Srinivasan Jagannathan).

Petitioner contends Amidi discloses a memory module comprising four ranks of memory devices, and a circuit including a CPLD. Pet. 20, 23. Petitioner asserts that Amidi's CPLD receives chip select signals cs0, cs1 and address signal Add(n) from a memory controller, and in response, generates signals to activate a selected one of the four ranks of memory devices, while inactivating the other three ranks from the data bus. *Id.* at 20–21 (citing Ex. 1008 ¶¶ 34, 43, 52), 26 (citing Ex. 1008 ¶¶ 43, 44, 62). Petitioner contends "Klein discloses a switch and switch control circuitry ('a circuit') that are provided ('mounted') on a memory module." *Id.* at 18 (citing Ex. 1006 ¶ 32). With reference to Klein Figure 3, Petitioner asserts that

> Klein discloses that the switches ("the circuit") selectively couples data bus segment 30c of memory circuit 28 to the input data bus 30a, 30b, and decouples ("selectively isolates") data bus segment 30d of another memory circuit ("a load of the DDR memory circuits of at least one rank") from the input data bus 30a, 30b that is connected to the memory controller ("the computer system").

Id. at 22–23 (citing Ex. 1006 ¶ 28). Petitioner contends Klein discloses address signals and TE signals are used to select the memory devices for access by/connection to the memory controller. *See id.* at 23 (citing Ex. 1006, Fig. 9). Petitioner asserts that Klein discloses that by decoupling memory circuits that are not being accessed from a data bus during data

transfers to or from other memory devices, data bus capacitance is reduced. *Id.* at 22 (citing Ex. 1006, Abstract).

Petitioner contends "both Klein and Amidi describe coupling or isolating memory device loads," and "[a] POSITA would have been motivated to combine the bus switch taught by Klein and memory module of Amidi . . . for the benefit of isolating a memory device load from the computer system to reduce parasitic capacitance and increase the speed at which memory accesses can be performed." *Id.* at 26 (citing Ex. 1006 ¶¶ 5–10, Abstract; Ex. 1008 ¶¶ 38, 39; Ex. 1011[7] ¶¶ 99, 101).

Patent Owner contends the ordinary artisan "would understand that load isolation is directed specifically to the issue of electrical loading." PO Resp. 24. Patent Owner argues that the data lines of Amidi's four ranks are "hard-wired in permanent connection to the same 72-line data bus." *Id.* at 23 (citing Ex. 1008, Fig. 3, ¶¶ 34–35). Patent Owner contends that "[d]ue to the permanent electrical connections of Amidi's data bus, there would never be electrical separation and, thus, [the electrical loads of Amidi's memory devices] could never be subject to an act of selectively isolating." *Id.* Patent Owner relies on Dr. Sechen's testimony that the rank inactivation in Amidi's system would not result in load isolation as claimed because "there are . . . no switches to facilitate any type of decoupling or isolating" (Ex. 2002 ¶ 80) of "the chip select signal lines and data bus lines[, which] are permanently hard-wired via an electrical conduit to the memory devices" (*id.* ¶ 78). We decline to give weight to this testimony because it is based on an erroneous construction of "selectively isolating" as requiring electrical separation. As

[7] Petitioner erroneously cites to Ex. 1007.

discussed in Section II, above, we do not construe "selectively isolating" as requiring *electrical* separation or as requiring a switch or other specific component that would enable electrical decoupling. Likewise, the '536 patent does not support construing the claim term "load" as limited to electrical loads. *See* Section II *supra*.

We find Amidi discloses a circuit that, in response to a signal selecting a rank of memory devices, activates the selected rank thereby enabling it to read and write data to a system bus while de-activating non-selected ranks, thereby disabling those ranks from reading and writing data to the system bus. Ex. 1008 ¶¶ 43, 44, 62. We find Dr. Jagannathan applies the broadest reasonable constructions of "selectively isolating" (i.e., "isolating in response to a selection") and "load" (i.e., a broad term that is not limited to electrical load) in his analysis of Amidi, and we credit his testimony that one of ordinary skill in the art would have understood that *in response to the selection* of a rank of memory devices to drive or receive data signals, the data bus pins on the memory devices of the inactive ranks would be in a high impedance state such that the associated *data loads* of the inactive ranks *are* thereby *isolated* from the computer system. *See* Ex. 1011 ¶ 72; *id.* ¶ 39 ("A person of ordinary skill would understand that a high-impedance state on the DQ pins means that the chip is essentially not driving these pins."); Ex. 1026 ¶ 28 ("[W]hen the data is transmitted . . . , the data pins of the inactive ranks are in a high impedance state. This is a requirement of the JEDEC standards. (See JEDEC79C (Ex. 1015), pp. 7, 22, 31.)"[8]). Dr. Jagannathan's testimony is supported by the cited disclosure

[8] In our Final Decision, we found that "a person of ordinary skill in the art at

in JEDEC79C. *See* Ex. 1015, 7 ("[D]uring power-up . . . the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access)."), 22 ("Upon completion of a [READ] burst, assuming no other commands have been initiated, the DQs will go High-Z."), 31 ("Upon completion of a [WRITE] burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored."). Moreover, neither Patent Owner nor Dr. Sechen disputes that the data pins of the inactive ranks remain in a high-impedance state during a read or write transaction. *See, e.g.*, PO Resp. 22–28 (arguing Amidi does not disclose "selectively isolating"); Ex. 2002 ¶ 80 (wherein Dr. Sechen addresses the testimony in paragraph 72 of Dr. Jagannathan's declaration (Ex. 1007)). In other words, we are satisfied that Amidi discloses "selectively isolating" under our construction of this term as "isolating in response to a selection."

Even if we were to construe "selectively isolating" as requiring electrical separation, we are persuaded that combining the bus switch taught by Klein and the memory module of Amidi would have resulted in a circuit

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the time of the '536 patent would have . . . familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules." Final Dec. 13. Dr. Jagannathan's testified that "DRAM memory modules used in personal computer applications typically conform[] to [JEDEC] standards." Ex. 1011 ¶ 24. Dr. Sechen does not disagree with this testimony. *See, e.g.*, Ex. 2002 ¶ 18 ("[M]emory modules must be designed to properly interface with a memory controller and remain compliant with relevant JEDEC standards for proper operational performance and interoperability."). JEDEC79C provides a standard for DDR SDRAM memory devices. Ex. 1015, i.

"configured to . . . selectively isolate," and a method "comprising . . . selectively isolating," "a load of . . . DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of [address and DDR chip-select] signals" as recited in claims 1 and 24. In this regard, we note Dr. Sechen conceded that Klein's MOSFET switches (i.e., data bus switches) are capable of electrically decoupling a memory device from a data bus. *See* Ex. 1025, 49:16–50:18, 88:5–22; *see also* Ex. 1001, 9:3–5 ("Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches."), 10:32–33 (Example 1 circuit "comprising six FET switches for providing load isolation to DQ and DQS lines"). We credit Dr. Jagannathan's testimony that one of ordinary skill in the art would have "implemented the bus switch of Klein into the architecture of Amidi" (Ex. 1011 ¶ 101) to "provide[] the benefit of incorporating more functionality in a smaller space, thereby providing more space on the memory module for additional memory devices" (*id.* ¶ 99) and to "provide the benefits of load isolation of data buses and reduction in parasitic capacitance on the data buses" (*id.* ¶ 101). We further credit Dr. Jagannathan's testimony that modifying Amidi in this manner "would have been routine for one of ordinary skill in the art." *Id.*; *see also* Final Dec. 30 (crediting Dr. Jagannathan's testimony in finding motivation to combine and a reasonable expectation of success).

IV. CONCLUSION

Having reconsidered the parties' respective arguments and evidence cited in support thereof in light of our construction of "selectively isolating"

as "isolating in response to a selection," we are persuaded that combining the bus switch taught by Klein and the memory module of Amidi would have resulted in a circuit "configured to . . . selectively isolate," and a method "comprising . . . selectively isolating," "a load of . . . DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of [address and DDR chip-select] signals" as recited in claims 1 and 24. Accordingly, given the Federal Circuit's directive, because we find the asserted prior art discloses or suggests these limitations, we determine that '536 patent claims 1, 16, 17, 24, 30, and 31 are unpatentable.

V. ORDER

Accordingly, it is

ORDERED that claims 1, 16, 17, 24, 30, and 31 of U.S. Patent 8,081,536 B1 are unpatentable; and

FURTHER ORDERED that this is a final written decision under 35 U.S.C. § 318(a). Parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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