UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., AND
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioners,
v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00562
Patent No. 8,395,501

NETLIST INC.'S NOTICE OF APPEAL
TO THE U.S. COURT OF APPEALS FOR THE FEDERAL CIRCUIT

Via PRPS
Patent Trial and Appeal Board

Via Hand Carry
Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

Via CM/ECF
United State Court of Appeals for the Federal Circuit

Pursuant to 35 U.S.C. §§ 141, 142, and 319, 37 C.F.R. §§ 90.2, 90.3, and 104.2, and Rule 4(a) of the Federal Rules of Appellate Procedure, Patent Owner

Netlist, Inc. hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision (Paper 36) entered by the Patent Trial and Appeal Board on July 5, 2018. In particular, Patent Owner identifies the following issues on appeal:

- The Board's judgment that claim 4 of Patent No. 8,359,501 has been shown to be unpatentable as obvious;
- The Board's judgment that claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel pursuant to C.F.R. §42.72; and
- Any Board finding, determination, judgment, or order supporting or related to the Final Written Decision and decided adversely to Patent Owner.

Patent Owner is concurrently filing true and correct copies of this Notice of Appeal, along with the required fees, with the United States Court of Appeals for the Federal Circuit, and with the USPTO Patent Trial and Appeal Board.

Respectfully submitted,

Dated: September 6, 2018

/*Thomas J. Wimbiscus*/
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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through PRPS, a true and correct copy of the above-captioned **NETLIST, INC.'S NOTICE OF APPEAL** is being filed by hand with the Director on September 6, 2018, at the following address:

Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

The undersigned also herby certifies that a true and correct copy of the above-captioned **NETLIST INC.'S NOTICE OF APPEAL** and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on September 6, 2018.

Dated: September 6, 2018

/*Thomas J. Wimbiscus*/
Thomas J. Wimbiscus
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Netlist Inc.

CERTIFICATE OF SERVICE

The undersigned hereby certified that the foregoing **NETLIST INC.'S NOTICE OF APPEAL** was served electronically via e-mail on September 6, 2018 in its entirety on the following:

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Paper 36
Entered: July 5, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00562
Patent 8,359,501 B1

Before BRYAN F. MOORE, MATTHEW R. CLEMENTS, and SHEILA F. McSHANE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. 318(a)

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc., (collectively "Petitioner") filed a Petition (Paper 1, "Pet.") pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1 and 4 ("the challenged claims") of U.S. Patent No. 8,359,501 B1 ("the '501 Patent," Ex. 1001). The Petition is supported by the Declaration of Pinaki Mazumder, Ph.D. ("Mazumder Declaration," "Mazumder Dec.," Ex. 1003). Netlist, Inc. ("Patent Owner") filed a Preliminary Response ("Prelim. Resp.," Paper 6).

On July 7, 2017, we instituted an *inter partes* review of claims 1 and 4 of the '501 Patent, but did not institute on all grounds. Paper 7, 7, 29 ("Inst. Dec."). Patent Owner filed a Response. Paper 14 ("PO Resp."). Patent Owner Response is supported by the Declaration of R. Jacob Baker, Ph.D. ("Baker Declaration," "Baker Dec.," Ex. 2010). Petitioner filed a Reply. Paper 18 ("Reply").

On February 28, 2018, Petitioner and Patent Owner filed motions to exclude. Paper 21 ("Pet. Mot. to Excl."); Paper 23 ("PO Mot. to Excl."). Petitioner and Patent Owner filed responses to their respective motions to exclude. Paper 25 ("Pet. Mot. to Excl. Resp."); Paper 26 ("PO Mot. to Excl. Resp."). Petitioner and Patent Owner filed replies to those respective responses. Paper 29 ("Pet. Mot. to Excl. Reply"); Paper 30 ("PO Mot. to Excl. Reply"). Patent Owner also filed a Motion to Strike directed to portions of Petitioner's Reply, with Petitioner filing an Opposition. Paper 32 ("Mot. to Strike"); Paper 33 ("Opp. Mot. to Strike").

On March 13, 2018, we entered a *sua sponte* Order to Show Cause why the *inter partes* review should not be terminated as to claim 1 because it

has been finally adjudicated as unpatentable. Paper 24 ("Show Cause Order"). Petitioner and Patent Owner responded to the order. Paper 27 ("Pet. Show Cause Resp."); Paper 28 ("PO Show Cause Resp.").

An oral hearing was held on April 6, 2018. Paper 34 ("Tr.").

On April 24, 2018, the Supreme Court held that a decision on institution under 35 U.S.C. § 314 may not institute on less than all claims challenged in the petition. 138 S. Ct. 1348 (2018). We modified our Institution Decision to institute trial on all of the challenged claims and all of the grounds presented in the Petition. Paper 35 ("SAS Order"). We invited the parties to request briefing regarding the newly added grounds and no request was made. *Id.*

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claim 4 is unpatentable. Based on collateral estoppel, we also terminate the trial pursuant to 37 C.F.R. § 42.72 as to claim 1.

A. Related Proceedings

Petitioner recites a list of District Court proceedings related to this *inter partes* review. Pet. 2. This *inter partes* review challenges the same patent at issue in the decision entered in IPR2014-00971 (the '971 IPR). *See Sandisk Corp. v. Netlist, Inc.*, Case IPR2014-00971 (PTAB Dec. 16, 2014) (Paper 12). In the '971 IPR, as to the claims at issue here, claim 1 was held unpatentable as anticipated by Averbuj in a final written decision. *Sandisk Corp. v. Netlist, Inc.*, Case IPR2014-00971 (PTAB Apr. 27, 2016) (Paper 37). That decision was appealed to Federal Circuit, the decision was affirmed, and the mandate issued on December 21, 2017. *See* Exs. 1029,

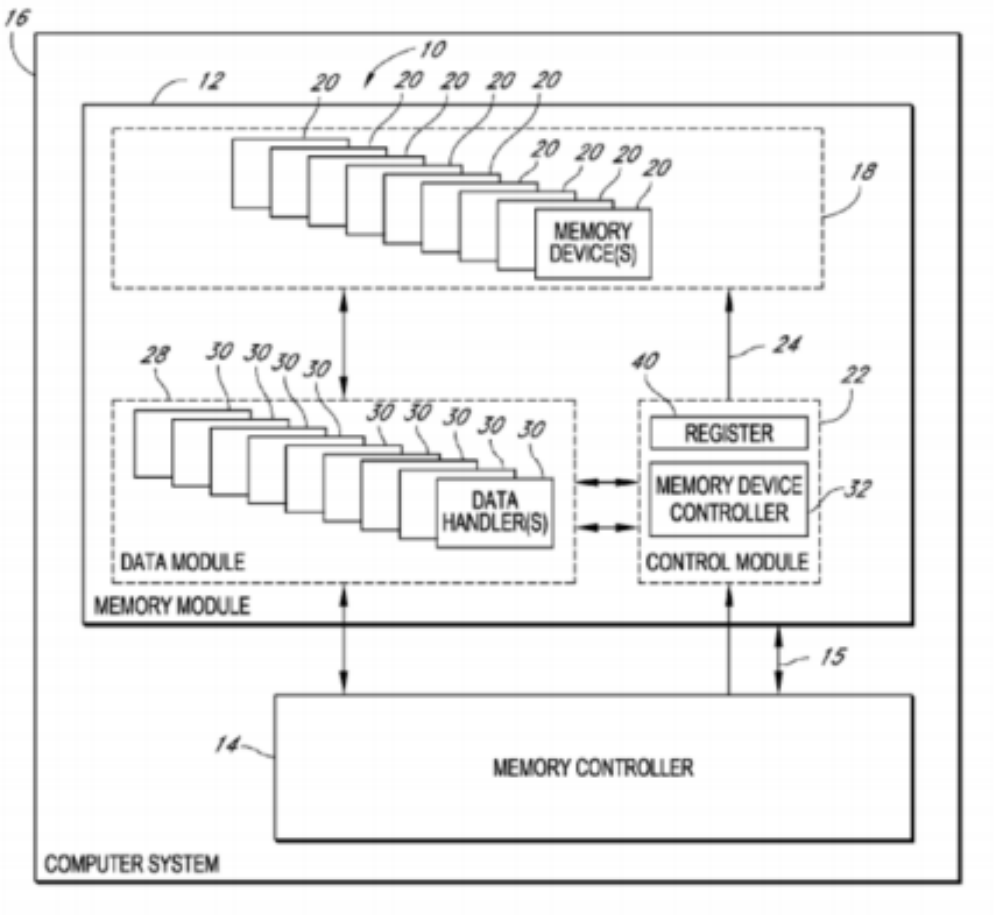
1034. In the '971 IPR, claims 1 and 4 were also challenged as obvious over Averbuj and Tsern, but that challenge was not instituted. *Sandisk*, IPR2014-00971 (Paper 12, 15–16, 23).

The '501 Patent was also challenged in IPR2014-01374 (the '1374 IPR). In the 1374 IPR, as to the claims at issue here, claims 1 and 4 were held not unpatentable as anticipated by Averbuj (under a different theory of anticipation than the '971 IPR) in a final written decision. *Smart Modular Techs. Inc. v. Netlist, Inc.*, Case IPR2014-01374 (PTAB March 6, 2016) (Paper 44). The decision in the '1374 IPR was not appealed to Federal Circuit.

The '501 Patent was also challenged in IPR2014-01375 (the '1375 IPR), in which institution was denied as to all challenges on the merits. *Smart Modular Techs. Inc. v. Netlist, Inc.*, Case IPR2014-01375 (PTAB Mar. 13, 2015) (Paper 12). Neither Averbuj nor Tsern was asserted in the '1375 IPR.

B. The '501 Patent

The '501 Patent relates to self-testing electronic memory modules. Ex. 1001, 1:28–29. A block diagram of an exemplary self-testing memory module is shown in Figure 1 of the '501 Patent, reproduced below.



As illustrated in Figure 1, above, "memory module 10 includes a printed circuit board 12 configured to be operatively coupled to a memory controller 14 of a computer system 16." *Id*. at 5:6–8. Memory module 10 includes a plurality of memory devices 18, e.g., ETT DRAM chips, each memory device 20 of the plurality of memory devices 18 comprising data, address, and control ports. *Id*. at 3:34–36, 5:10–12. Memory module 10 further includes data module 28 comprising a plurality of independently operable data handlers 30, and control module 22 that may include a dual input register for registering address and control signals coming from either self-testing logic or from memory controller 14 on the system board. *Id*. at 5:14–16, 42–46. "In various embodiments, the control module 22 includes .

. . one or more application-specific integrated circuit[s]." *Id*. at 9:62–64. "[D]ata module 28 and/or the control module 22 of certain embodiments are configured to test the plurality of memory devices 18 at the normal operating speed of the memory devices 20." *Id*. at 6:5–8. "For example, the data module 28 and/or the control module 22 are configured to provide memory signals (e.g., data, address and control signals) according [to] the operating specification of the memory devices 20." *Id*. at 6:8–11. "In some embodiments, during testing, the control module 22 generates address and control signals 24 associated with memory locations to be tested and the data module 28 generates corresponding test data patterns and provides them to the appropriate memory devices 20." *Id*. at 5:48–52. "For example, the data module 28 may receive a write command from the control module 22 and provide data to be written to certain locations in the memory devices 20 during a write operation." *Id*. at 5:52–55.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A memory system configured to be operatively coupled to a memory controller of a computer system, the memory system comprising:
>
> a plurality of memory chips;
>
> a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips;
>
> a control circuit configured to generate address and control signals, wherein the memory system is configured to test the one or more memory chips using the address and control signals

generated by the control circuit and using the data generated by the one or more data handlers.

Ex. 1001, 16:38–51.

D. Instituted Grounds of Unpatentability

We instituted trial on the following grounds (Inst. Dec. 29; SAS Order 2):

Reference[s]	Basis	Claims Challenged
Averbuj[1]	§ 102	1 and 4
Averbuj	§ 103	1 and 4
Averbuj and Tsern[2]	§ 103	4

II. ANALYSIS

A. Collateral Estoppel

The parties raised an issue arising from challenges to the subject patent in related *inter partes* review proceedings brought by a different petitioner, namely the '971 IPR. In the '971 IPR, the Board held that claim 1 is unpatentable over art that is the same as the art considered in this proceeding as against a different petitioner (Sandisk) than this proceeding. *Sandisk Corp. v. Netlist, Inc.*, Case IPR2014-00971 (PTAB Apr. 27, 2016) (Paper 37). The Federal Circuit affirmed that decision. *Netlist, Inc. v. SanDisk LLC*, 702 F. App'x 986 (Fed. Cir. 2017) (per curiam). Accordingly, claim 1, which is involved in this proceeding, has been held

[1] U.S. Patent Application Publication No. 2005/0257109 (Ex. 1005, "Averbuj")
[2] U.S. Patent Application Publication No. 2007/0070669 (Ex. 1006, "Tsern")

unpatentable. This raises the issue of whether we should terminate the proceeding as to claim 1 based on collateral estoppel.

"It is well established that collateral estoppel, also known as issue preclusion, applies in the administrative context." *MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1376 (Fed. Cir. 2018) (citations omitted); *Webpower, Inc.*, Case IPR2016-01239, slip. op. at 26–28 (PTAB Dec. 26, 2017) (Paper 21). A patentee is estopped from asserting the validity of a patent that has been declared invalid in a prior suit against a different defendant, unless patentee demonstrates that he did not have full and fair opportunity, procedurally, substantively, and evidentially, to litigate the validity of his patent in the prior suit. *MaxLinear, Inc.*, 880 F.3d at 1377 (citing *Blonder-Tongue Labs., Inc. v. Univ. of Illinois Found.*, 402 U.S. 313, 91 S. Ct. 1501, 28 L. Ed. 2d 788 (1971) (finding collateral estoppel applies to a patentee who had a full and fair opportunity to litigate the validity of a patent in a prior federal case.)) Thus, as to a different petitioner, when the prior decisions finding claims unpatentable have "subsequently been affirmed by [the Federal Circuit] those prior decisions, having been affirmed by [the Federal Circuit], are binding in this proceeding, as a matter of collateral estoppel." *Id.* at 1376.

In response to our Order to Show Cause why the proceeding should not be terminated as to claim 1, Patent Owner argued that "[t]his IPR should be terminated as to claim 1" to avoid wasting the resources of the Board. PO Show Cause Resp. 1. Petitioner argued "[c]ollateral estoppel only binds Patent Owner, not Petitioners, and Petitioners, in addition to advancing the same mapping of Averbuj to claim 1 as did SanDisk in IPR2014-0971, also present alternative mappings as well." Pet. Show Cause Br. 1. Petitioner

further argues "[g]iven that the Board may need to consider whether Petitioners' alternative mappings read on the limitations of claim 1 when addressing the patentability of claims 4, there may be little efficiency gained by terminating this IPR as to claim 1." *Id*. at 2. We recognize that Petitioner presents alternative mappings as to claim 1. Nevertheless, as explained below, we find that claims 4 is unpatentable under the mappings used in the '971 IPR. Thus, given that we find that collateral estoppel applies, judicial efficiency is advanced by declining to reassess the patentability of claim 1 under alternative mappings.

Patent Owner asserts that this *inter partes* review relies on obviousness based on the combination of Averbuj and Tsern rather than the ground under which claim 1 was found unpatentable in the '971 IPR, i.e. anticipation by Averbuj. Thus, according to Patent Owner, "Petitioners must also provide evidence of a reason why a POSITA would have modified/combined the limitations of claim 1 (as allegedly shown in Averbuj) with the limitations of dependent claims 4 (as allegedly shown in Tsern), to create the claimed inventions." PO Show Cause Br. 1. We agree that Petitioner must show a motivation to combine Tsern with Averbuj, but this does not mean that Petitioner must prove again that Averbuj meets the limitations of claim 1; it means only that Petitioner need show a rationale for combining Tsern with those aspects of Averbuj that the Board has already determined meet the limitations of claim 1.

Patent Owner asserts that "collateral estoppel does not apply to the application of the claim 1 limitations in assessing dependent claim 4." *Id.* at 2. Patent Owner further asserts "[a] party seeking to apply collateral estoppel based on a prior action must show that (1) the identical issue was

actually litigated; (2) the issue was actually decided in a final decision on the merits; (3) the issue was necessary to the final decision; and (4) the party being estopped was adequately represented in the prior action [i.e. "the *United Access* test"]." *Id.* at 2 (citing *United Access Techs., LLC v. CenturyTel Broadband Services LLC*, 778 F.3d 1327, 1331 (Fed. Cir. 2015)). We agree that this is the proper test to use to assess the applicability of collateral estoppel. Nevertheless, we note *United Access* applies collateral estoppel in a different context and suggests that issue preclusion can be applied in an obviousness challenge, even if the final decision on the original issue was considered under an anticipation challenge. In particular, in *United Access* it was noted that "[i]ssue preclusion [traditionally called "collateral estoppel"[3]] applies to issues litigated in prior disputes . . . [and, thus, i]t thus makes no difference that the earlier no-damages-due-to-competition ruling arose in a case under the Truth in Negotiation Act and that this dispute arises under the False Claims Act and the common law." *United Access*, 778 F.3d. at 726. The "issue" of whether Averbuj teaches the limitations of claim 1 is identical to the issue that was litigated in the '971 IPR which found that Averbuj anticipates the limitations of claim 1. The question becomes how does the fact that the limitations of claim 1 rely on an obviousness combination with Tsern effect the analysis. To that point, we recognize that "though anticipation is the epitome of obviousness, [they] are separate and distinct concepts." *Jones v. Hardy*, 727 F.2d 1524, 1529 (Fed.Cir.1984). It is that difference that is important here.

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[3] *Mother's Rest., Inc. v. Mama's Pizza, Inc.*, 723 F.2d 1566, 1569 (Fed. Cir. 1983)

The Federal Circuit has noted that obviousness is different because: more than one reference can be used in obviousness; secondary considerations must be analyzed in obviousness; inherency in anticipation is different than obviousness (*Cohesive Techs., Inc. v. Waters Corp.*, 543 F.3d 1351, 1364 (Fed. Cir. 2008)); and single reference obviousness requires a showing of motivation to modify a reference when a party argues that such a modification must be made to meet the limitations of a claim (*Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1346 (Fed. Cir. 2018). Here, however, Petitioner relies on Averbuj alone, not on the combination of Averbuj and Tsern (or any modification of Avebuj), to meet any limitation of claim 1, Petitioner (here and in the '971 IPR) did not rely on inherency to show any limitations of claim 1, and Patent Owner has not argued secondary considerations. *See generally*, Pet.; PO Resp.; Ex. 1028 ('971 IPR FWD).

Thus, the relevant legal issue, in this essentially single reference obviousness situation as to claim 1, is the same as in anticipation, i.e. does the reference teach the limitations of the claim. In fact, anticipation requires a higher level of teaching requiring that references teach limitations of a claim explicitly or inherently. Under obviousness, the reference need only render a limitation obvious to one of skill in the art at the time of the invention. Thus, the adage "anticipation is the epitome of obviousness." *Jones*, 727 F.2d at 1529. The Board is allowed to rely on findings regarding whether a reference anticipates a limitation in its obviousness analysis.[4] *See*

[4] In fact, the Board relied on this principle in the Decision to Institute. Dec. to Inst. 19 ("[W]e determine that claim 1 is anticipated by Averbuj.

Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc., 853 F.3d 1272, 1278 (Fed. Cir. 2017) (stating approvingly in a footnote that the "Board noted that Oselin rendered [the challenged claims] obvious by virtue of its anticipation of them.") (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Also, as to the remaining prongs of the *United Access* test, the issue of whether Averbuj teaches the limitations of claim 1 was actually decided in a final decision on the merits, the issue was necessary to the final decision because it went to the ultimate issue of patentability, and there is no allegation that Patent Owner was not adequately represented in the prior action. Thus, for the reasons above, claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel and the issue of whether the limitations of claim 1 are met by Averbuj by obviousness over Averbuj and Tsern also is established under the doctrine of collateral estoppel. Thus, we terminate this proceeding as to claim 1.

Our reviewing court has recently ordered the Board, on remand, to assess whether claims depending from a claim that has been finally adjudicated as unpatentable should not also be found unpatentable for the same reasons as the independent claim. *MaxLinear, Inc.*, 880 F.3d at 1377–1378. We apply this analysis to claim 4. Claim 4 has not been finally adjudicated as unpatentable in any previous case. Because the differences between the unadjudicated patent claim 4 and the adjudicated patent claim 1

Inasmuch as 'anticipation is the epitome of obviousness' (*In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002)), we determine that Petitioner has established a reasonable likelihood of prevailing in its assertion that claim 1 would have been obvious over Averbuj alone.").

materially alter the question of unpatentability, collateral estoppel does not apply. *C.f. In re Arunachalam*, 709 F. App'x 699, 702 (Fed. Cir. 2017) (unpublished) (finding collateral estoppel applies to an adjudicated claim that is not "materially different" than the adjudicated claims); *accord MaxLinear, Inc.*, 880 F.3d at 1377–1378. In this case, there are material differences between claim 4 and claim 1. For example, claim 4, recites "the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers." Separate ICs is not contemplated in claim 1. It is still true, however, as Petitioner asserts, "Patent Owner is precluded from relitigating here whether Averbuj discloses all the limitations of claim 1, as arranged in the claim, including for purposes of determining the patentability of claim 4." Pet. Show Cause Resp. 3. Thus, we do not terminate as to claim 4 under collateral estoppel.

B. Relevant Law

1. Obviousness Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and, (4) where in evidence, so-called secondary

considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results.[5] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966) ("the *Graham* factors").

2. Level of Skill Law

The level of ordinary skill in the art usually is evidenced by the references themselves. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). For an obviousness analysis, prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (quoting *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). Moreover, "it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). That is because an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *see also In re Translogic Tech., Inc.*, 504 F.3d at 1259.

3. Claim Interpretation Law

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under this standard, we

[5] Patent Owner does not put forth evidence it alleges tend to show secondary considerations of non-obviousness in its Response.

interpret claim terms using "the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

We presume that claim terms have their ordinary and customary meaning. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016) ("Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history."); *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning is the meaning that the term would have to a person of ordinary skill in the art in question." (internal citation and quotation marks omitted)). A patentee, however, may rebut this presumption by acting as his or her own lexicographer, providing a definition of the term in the specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Only those terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

C. Level of Skill Analysis

Petitioner asserts "[a] person of ordinary skill in the art at the time of the '501 Patent would have been someone with "a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least

one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and BIST" Pet. 6 (citing, *inter alia*, Ex. 1003 ¶ 51). Patent Owner asserts through its declarant:

> [A Person of ordinary skill in the art at the time of the invention would have been] working on the design of memory devices, would have at least a Bachelor of Science degree in Electrical and/or Computer Engineering, and at least five years of industry experience designing memory devices and controllers. Alternatively, one of ordinary skill in the art would have a Master of Science degree in Electrical and/or Computer Engineering, and at least three years of industry experience designing memory devices and controllers. Also alternatively, one of ordinary skill in the art would have a Doctorate degree in Electrical and/or Computer Engineering, and have at least one year of industry experience designing memory devices and controllers.
>
> I agree with Petitioner's expert that the memory industry requires a POSITA with industry experience.

Ex. 2010 ¶¶ 32–33.

Neither party has argued that the difference between the parties' articulated level of skill should change the analysis as to patentability. Therefore, we adopt Petitioner's articulation of the level of skill, above, and acknowledge that, commensurate with that articulation of the level of skill, the level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

D. Claim Construction Analysis

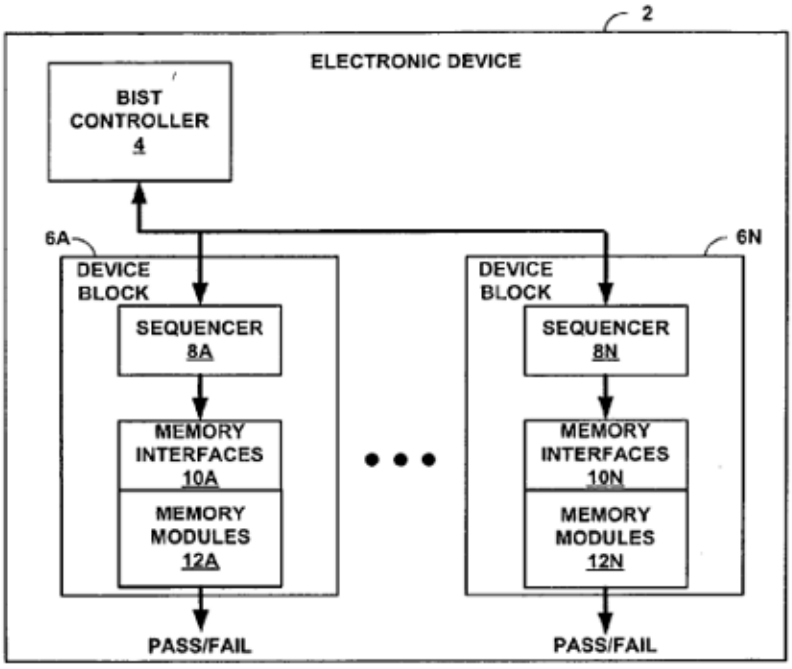
Claim 4 does not recite claim limitations whose constructions are in controversy. Patent Owner disputes only the construction for the term "memory module," recited in claim 1. PO Resp. 16–19. The "memory controller" is not argued as a reason that Averbuj or Tsern do not meet the limitations of claim 4. *Id.* at 52–56. Thus, we do not further construe any terms including memory controller in this Final Written Decision.

E. Claims 1 and 4 — Anticipation by Averbuj (Ex. 1005) (Ground 1)

Petitioner argues that claims 1 and 4 are unpatentable over Averbuj under 35 U.S.C. § 102. Pet. 19–31. We refer to this as "Ground 1."

1. Averbuj (Ex. 1005)

Averbuj describes a hierarchical built-in self-test (BIST) architecture wherein a BIST controller provides centralized, high level control of the testing of one or more memory modules. Ex. 1005 ¶¶ 7–8. Figure 1 of Averbuj is reproduced below.



Averbuj Figure 1, above, "is a block diagram illustrating an example electronic device 2 having a distributed, hierarchical built-in self-test (BIST) architecture." *Id.* ¶ 28. "[E]lectronic device 2 may be any device that incorporates memory modules, such as an embedded computing system, a computer, server, personal digital assistant (PDA), mobile computing device, mobile communication device, digital recording device, network appliance, mobile positioning device, and the like." *Id.* ¶ 32. Averbuj states that "electronic devices . . . are [normally] constructed from many integrated circuit chips and many supporting components mounted on a circuit board." *Id.* ¶ 5. "[E]lectronic device 2 includes a built-in self-test (BIST) controller 4 that provides centralized, high-level control over testing of device blocks 6A through 6N (collectively 'device blocks 6')." *Id.* ¶ 28. "Each of device blocks 6 includes a Sequencer 8, and a set of one or more memory interfaces 10 and one or more respective memory modules 12." *Id.* BIST controller 4 provides and communicates test algorithms as a set of commands to Sequencers 8 for application to device blocks 6. *Id.* ¶ 29.

Figure 5, below, illustrates an exemplary Sequencer 8A. *Id.* ¶ 22

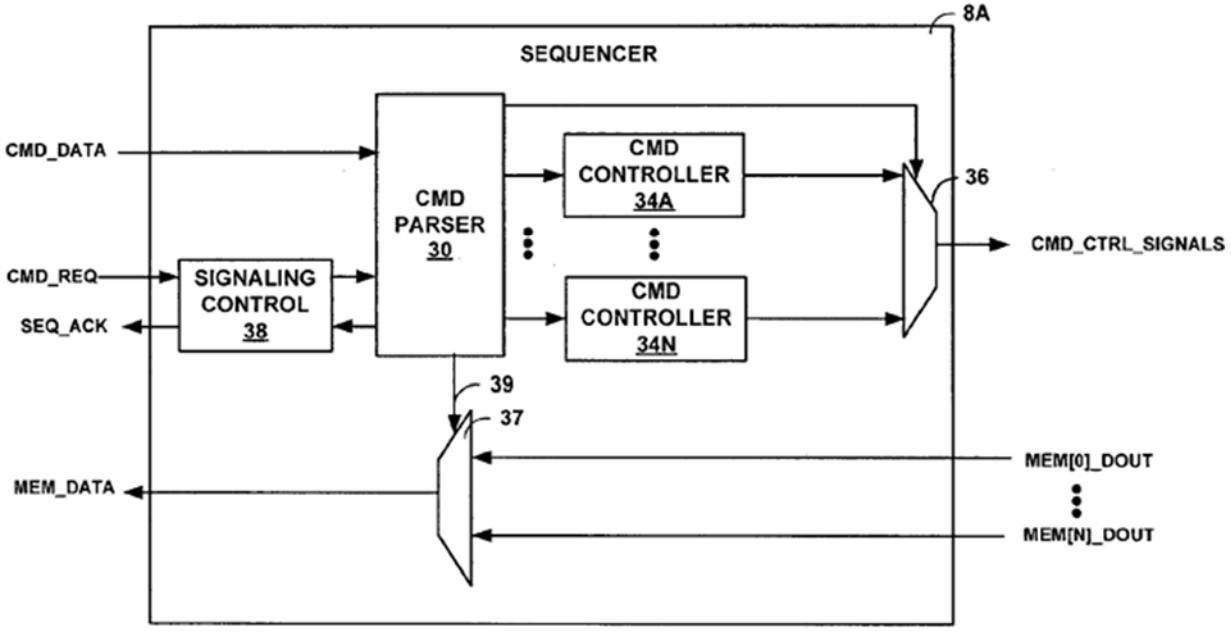


FIG. 5

As shown in Figure 5, above, exemplary Sequencer 8A includes command parser 30 and command controllers 34. *Id.* ¶¶ 41–42. Command parser 30 processes the commands from BIST controller 4 and invokes one of command controllers 34, which, in turn, issues command control signals, such as signals to provide a memory address and data, to receiving memory interfaces 10, 41. *Id.* ¶¶ 43, 51. An exemplary memory interface is shown in Figure 6, below. *Id.* ¶ 23.

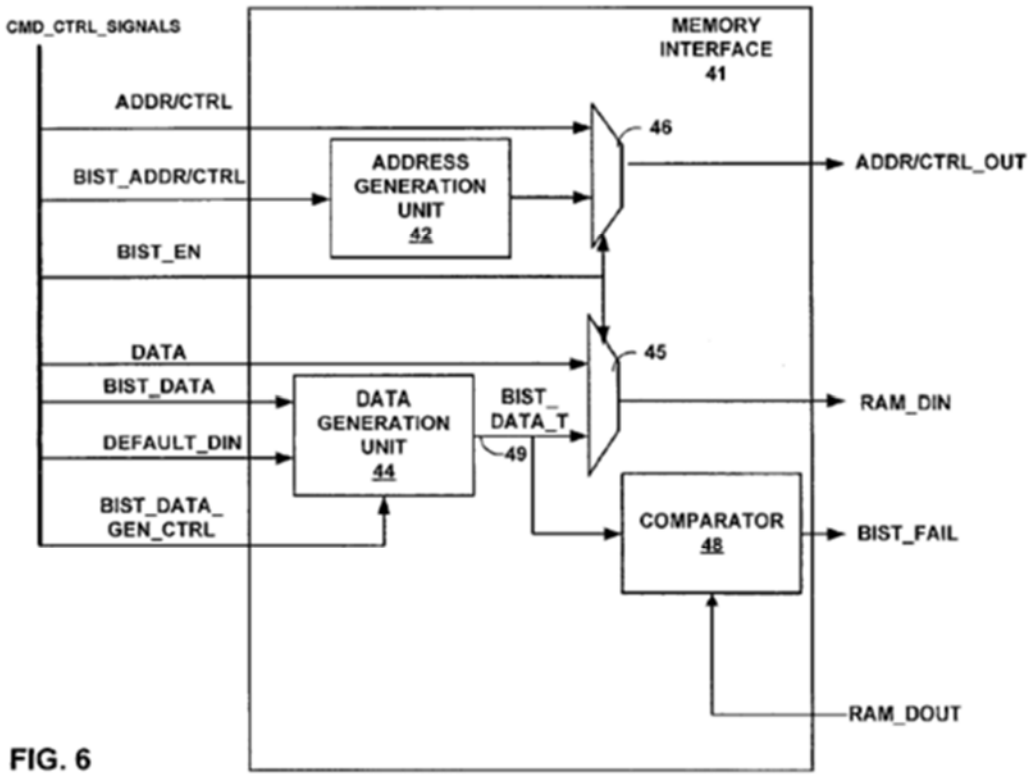


FIG. 6

As shown in the Figure 6 embodiment, above, memory interface 41 includes multiplexers 45, 46. *Id*. ¶ 48. "[U]nder normal operating conditions, BIST enable (BIST_EN) is de-asserted, causing multiplexers 45, 46 to select the address/control signals (ADDR/CTRL) and data signals (DATA), e.g., as provided by a programmable processor." *Id.* "When electronic device 2 is operating in BIST mode, however, the BIST enable signal causes multiplexers 45, 46 to select the BIST address/control signals (BIST_ADDR/CTRL) and the test data provided by a respective higher level Sequencer[, e.g., Sequencer 8A]." *Id*.

"[M]emory interface 41 processes the sequential memory operations issued by [] higher-level Sequencer [8A], and transforms the data and

addresses provided by the Sequencer as needed based on the particular physical characteristics of the memory module" (*id*. ¶ 54), using address generation unit 42 and data generation unit 44 (*id*. ¶¶ 49, 51). "[A]ddress generation unit 42 generates the address applied to [] memory module 12 based on the addressing requirements specified by Sequencer 8A and the physical configuration of the rows and columns of the memory module." *Id*. ¶ 51. "[D]ata generation unit 44 [] receives BIST _DATA signals and default data (DEFAULT_DIN) as provided by [] Sequencer 8[A], and generates transformed BIST data signals 49 (BIST_DATA_T) based on control signals (BIST_DATA_GEN_CTRL) provided by the Sequencer and the specific physical characteristics of the corresponding memory module." *Id*. ¶ 49. "[D]ata generation unit 44 generates the exact data (RAM_DIN) applied to the memory inputs during each operation of the algorithm." *Id*.

2. Analysis

a. Claim 1

Claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel. *See supra* Section II. A.

b. Claim 4

Claim 4 recites "[t]he memory system of claim 1, wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers." Petitioner asserts that

> Averbuj discloses that BIST units are "commonly incorporated into memory chips and other integrated circuits." Ex. 1005 at ¶ [0003]. Because the memory interfaces are part of a BIST unit, Averbuj also discloses the memory interface (10,

> 41) is commonly incorporated into (memory or other) chips, or "integrated circuits." Ex. 1012 at 98, 277; Ex. 1003 at ¶ 126. Averbuj further discloses that the device block (6) and the components contained therein, such as the sequencer (8) and the memory modules (12), are "distributed" and "located throughout an electronic device," i.e., physically separated. *See e.g.,* Ex. 1005 at ¶¶ [0013], [0015]; Ex. 1003 at ¶ 127. Since memory interfaces (10, 41) are also components of each device block (6), at a minimum, the different sets of memory interfaces (10, 41) belonging to different device blocks (6) must also be physically separated. Ex. 1003 at ¶ 127. Averbuj also discloses that the various integrated circuits or chips of an electronic device are "mounted on a circuit board," indicating that the integrated circuits and chips comprising the electronic device are packaged integrated circuits or chips. Ex. 1005 at ¶ [0005]; Ex. 1016 at 1:15-27; Ex. 1003 at ¶ 128. Therefore, Averbuj discloses that the memory interfaces (each containing a "data handler") of different device blocks (which comprise a "memory system") must be distributed across "at least two physically separate integrated circuit packages." Ex. 1003 at ¶ 129.

Pet. 30–31.

In other words, Petitioner asserts that because the sequencer can be distributed throughout an electronic device, the memory system comprises two separate chip packages. We disagree. Claim 4 requires that the memory module comprise "two physically separate integrated circuit packages." Petitioner has not shown sufficient support for its broad reading that the memory system as claimed would be distributed across the device as Petitioner suggests. Thus, Petitioner has not established a preponderance of the evidence as to anticipation of claim 4 by Averbuj.

F. Claims 1 and 4 — Obviousness over Averbuj (Ex. 1005) (Ground 2)

Petitioner argues that claims 1 and 4 are unpatentable over Averbuj under 35 U.S.C. § 103. Pet. 31–38. We refer to this as "Ground 2." As to

claim 1, Petitioner includes an obviousness ground in case we determine that Averbuj does not disclose a "memory system configured to be operatively coupled to a memory controller of a computer system" and "memory chip." *Id.* at 31–34. As explained above, claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel. As also explained above, we determine that claim 1 can also be considered obvious over Averbuj.

As to claim 4, we explained above that we are not persuaded that Petitioner has shown sufficiently that Averbuj anticipates that claim. In the Institution Decision, we found Petitioner failed to establish a reasonable likelihood of prevailing in its assertion that claim 4 would have been obvious over Averbuj. Inst. Dec. 19–22. Therefore, we discuss the obviousness challenge to dependent claim 4 below under the preponderance of the evidence standard.

Petitioner's argument regarding obviousness of claim 4 over Averbuj alone is based on Petitioner's declarant's testimony that it was known to house data handlers in physically separate integrated circuit packages. Pet. 34–38 (citing Ex. 1003 ¶¶ 143–161)[6]. Petitioner argues that to do so would "have been the use of a known technique for its known purpose and would

[6] Petitioner's arguments regarding obviousness of claim 4 over Averbuj alone are based in part on disclosures in Tsern. Pet. 34–35 (citing Ex. 1006 ¶¶ 29, 52–53, Fig. 9A). Petitioner's arguments based on the disclosure of Tsern rely on structures in Tsern to modify Averbuj rather than only Tsern's general teachings to one of ordinary skill in the art and, thus, those arguments are properly considered below in Petitioner's ground based upon the combination of Averbuj and Tsern. As such we do not consider them here.

have achieved only predictable results, such as the protection of integrated circuits by the packaging." Pet. 35. Petitioner asserts that memory modules at the time of the invention were composed of memory chips mounted on different portions of a memory board with BIST units in each memory chip. *Id.*

Given that memory chips mounted on different portions of a memory board with BIST units in each memory chip were known, according to Petitioner, Petitioner asserts that reducing redundancy would have been a motivation to modify Averbuj. Specifically, Petitioner asserts

> [a] skilled artisan that seeks to reduce the redundant BIST circuitry of conventional memory chips and BIST units would have been motivated to modify the conventional design in such a way as to avoid unnecessary modifications to the conventional design. Ex. 1003 ¶ 151. Specifically, a skilled artisan would have understood that the BIST controller and sequencer portions of conventional BIST units would need to be carved out from each memory chip and combined to reduce redundant circuitry. Ex. 1003 ¶ 151. However, a skilled artisan would also have understood and recognized that the memory interface portions need not be excised and implemented as a separate chip since doing so would not reduce much, if any, circuitry. Ex. 1003 ¶ 151. Hence, a skilled artisan would have been motivated to avoid unnecessary design changes by keeping the original design with respect to the memory interface portion—i.e., retain the memory interfaces (each of which includes a "*data handler*") within each memory chip that was separately packaged and mounted on a printed circuit board of a memory module ("*physically separate integrated circuit packages*."). Ex. 1003 ¶ 152.

Pet. 53–54.

Patent Owner's Preliminary Response[7] argued that "modifying Averbuj as the Petitioner proposes would eliminate the 'built-in' aspect of Averbuj's memory BIST (built-in self-test). The proposed modification would therefore be contrary to Averbuj's principle of operation." *Id*. at 46. Patent Owner's Preliminary Response arguments assume that Averbuj would not be modified based on the single chip structure of Averbuj. In this Final Written Decision, we do not need to, and do not rely on this argument. Here, as in the Decision to Institute (Inst. Dec. 25), we focus on the motivation given by Petitioner to modify Averbuj.

Patent Owner also argued, in its Preliminary Response, that "the skilled artisan that the Petition imagines is one who has Averbuj and uses hindsight to turn Averbuj into the '501 patent. According to the Petition, this particularly skilled artisan is looking to implement Averbuj's memory BIST circuitry as a memory module." Prelim. Resp. 46.

"There must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008) (internal quotations omitted) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). For example, in *ActiveVideo Networks, Inc. v. Verizon*, our reviewing court

[7] Patent Owner chose not to request additional briefing to address this ground and arguments in the Preliminary Response are generally waived (Paper 8, 2–3), however, we acknowledge these arguments due to the unusual circumstance created by the Supreme Court's decision in *SAS* and to explain the background in the context of Patent Owners' Motion to Strike.

held that the following expert testimony on the motivation to combine was deficient as a matter of law:

> [Y]ou wanted to build something better. You wanted a system that was more efficient, cheaper, or you wanted a system that had more features, makes it more attractive to your customers, because by combining these two things you could do something new that hadn't been able to do before.

Active Video Networks, Inc. v. Verizon Commc'ns, Inc., 694 F.3d 1312, 1328 (Fed. Cir. 2012). The court noted that because the expert "failed to explain how specific references could be combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims," the expert's testimony was conclusory and bore no relation to any specific combination of prior art elements. *Id.* at 1327. Although the declarant's testimony here goes further than in *Active Video*, it fills in gaps about how the combination would be made with only conclusory testimony that appears to be tainted with hindsight.

As to other of Petitioner's arguments supported by its declarant, we find those to employ hindsight to piece together the device as claimed. The expert provides a host of rationales for separating the components of Averbuj into separate ICs including structures of Tsern (Ex. 1003 ¶ 143) and other secondary references. We acknowledge that Tsern contains structures that suggest the claimed configuration of the data handlers, but in this ground Petitioner does not assert Tsern as a reference, rather simply as evidence of the knowledge of one of skill in the art. Pet. 34–38. Relying on knowledge in the art does not obviate the need to prove a reference is prior art as of the critical date and show a motivation to combine existing

components in the manner claimed free of hindsight motivation. This amounts to an argument that the individual elements of the claim were known and that combining them would have yielded the claimed invention, but Petitioner provides insufficient explanation why an ordinarily skilled artisan would have combined those elements in the claimed manner without the explicit reliance on the structures of Tsern. *See KSR*, 550 U.S. at 418 ("[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.); *Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) ("it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would have made the combination") (citation omitted).

For the above reasons, we find the evidence and argument presented on the ground based on Averbuj alone is insufficient to show by a preponderance of the evidence that claim 4 would have been obvious.

Petitioner has not shown sufficiently that Averbuj teaches or suggests the physically separate ICs limitation for the reasons discussed above. Thus, Petitioner has failed to establish, by a preponderance of the evidence, its assertion that claim 4 would have been obvious over Averbuj.

G. Claim 4 — Obviousness over Averbuj (Ex. 1005) and Tsern (Ex. 1006) (Ground 3)

Petitioner argues that claim 4 is unpatentable over Averbuj and Tsern under 35 U.S.C. § 103. Pet. 38–42. We refer to this as "Ground 3." Claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel. Upon consideration of the full record of evidence and arguments, we determine that Petitioner has shown by a preponderance of the evidence that claim 4 is unpatentable under 35 U.S.C. § 103(a) as obvious over Averbuj and Tsern.

1. Tsern

Figure 1 of Tsern is reproduced below.

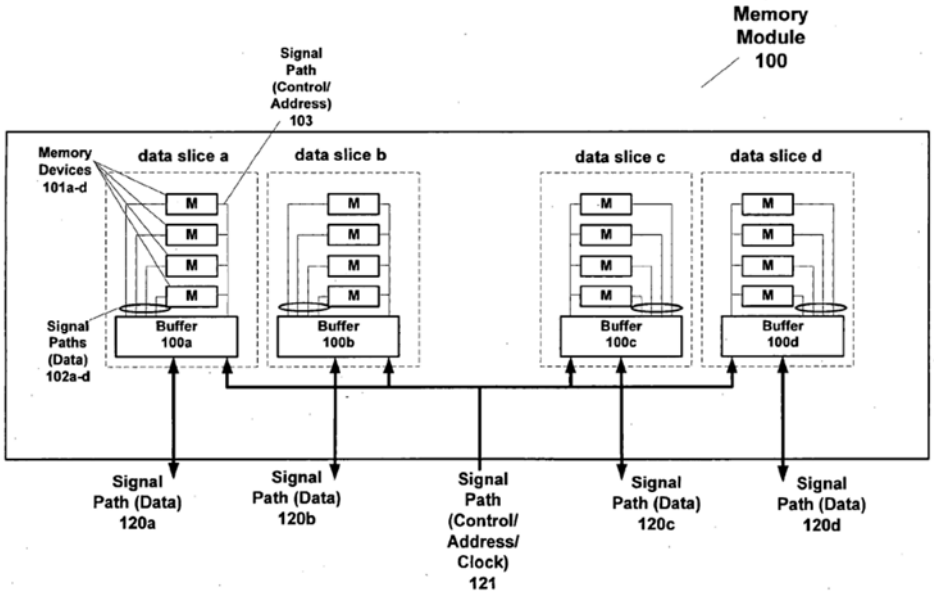


Fig. 1

Figure 1 of Tsern, above, illustrates an embodiment of a memory module with memory devices (101a–d) and corresponding buffer devices (100a–d). Figure 18 of Tsern is reproduced below.

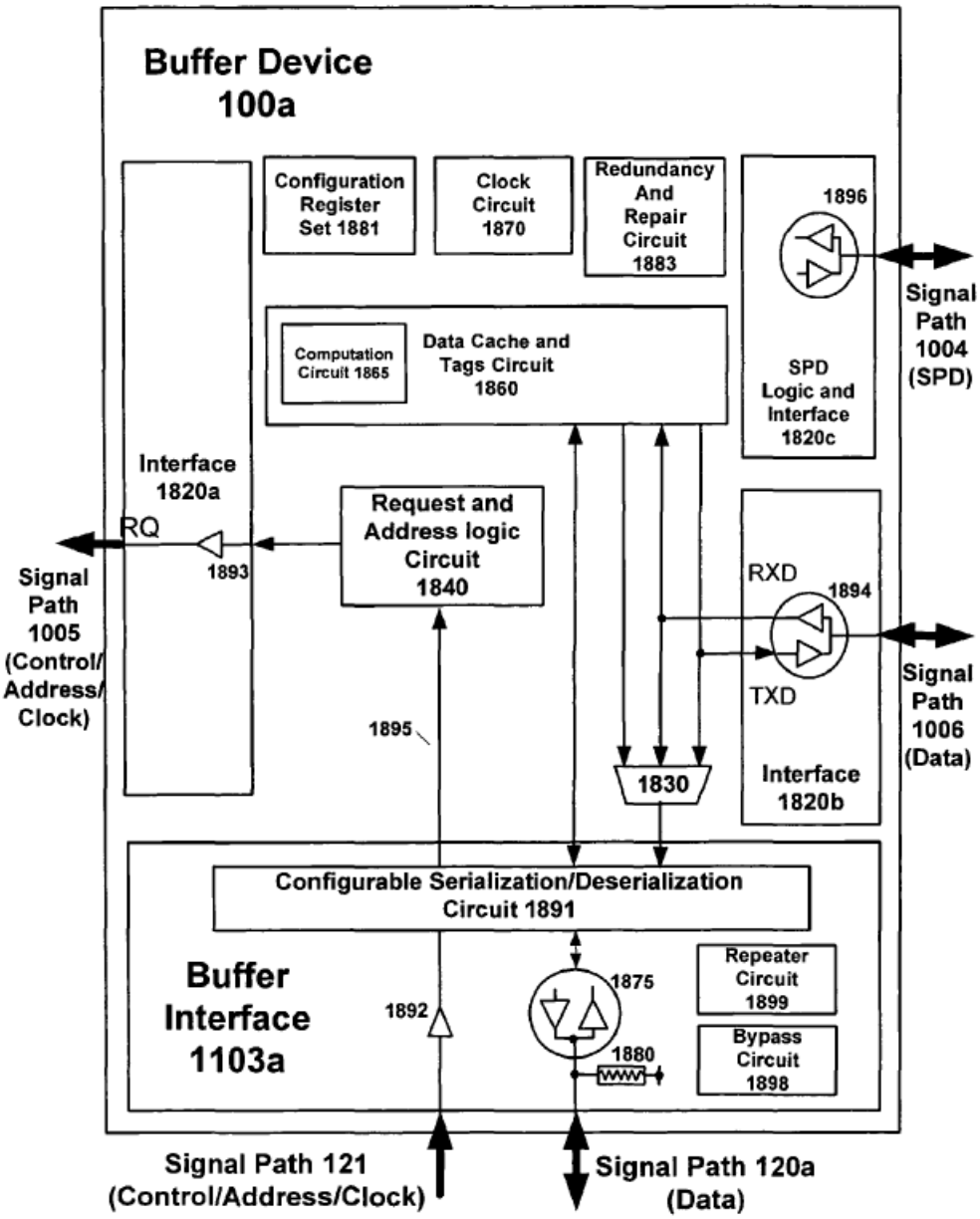


Fig. 18

As shown in Figure 18, above, Tsern discloses that, in one embodiment, each buffer device (100a) includes a redundancy and repair unit (1883), which tests and repairs the corresponding memory device(s). Ex. 1006, Fig. 18, ¶ 77. Each such buffer device (100a) includes data, address, and control interfaces (1820a and 1820b) that can be programmed

or configured to support memory modules with different number, size, width, and type of memory devices. *Id*. ¶ 99, Fig. 18.

Figure 1 of Tsern shows that each buffer device (100a–d) communicates address, control, and data signals with its corresponding memory device(s) (101a–d) without being in communication with any of the other buffer devices (100a–d) or other data ports of the other memory devices. Ex. 1006, Fig. 1.

2. Analysis

As discussed above, claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel, and we determined that claim 1 is also rendered obvious by Averbuj.

As to claim 4, we did not find that those claims are anticipated by, or would have been obvious over, Averbuj. Thus, below we discuss the combination of Averbuj and Tsern as it relates to claim 4.

Claim 4 recites that "[t]he memory system of claim 1, wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers." Petitioner relies on Figure 9 of Tsern, reproduced below.

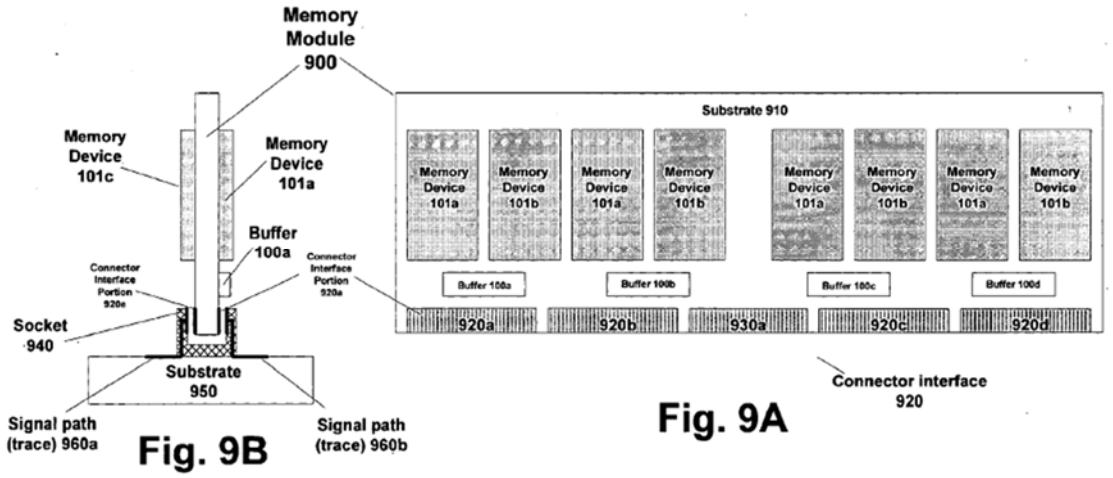


Fig. 9B

Fig. 9A

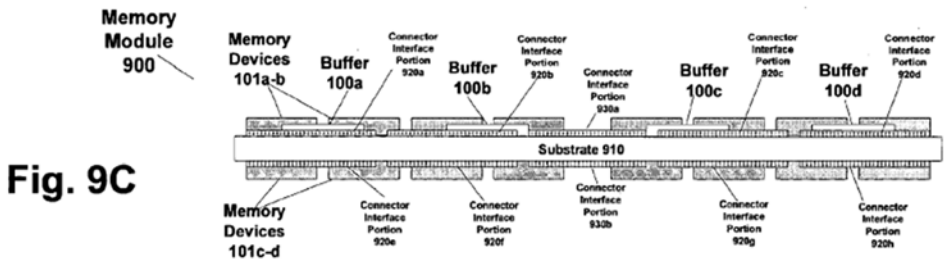


Fig. 9C

Figure 9 of Tsern, above, shows an implementation of a memory module in which each of the four buffer devices (100a–d) is implemented as a physically separate integrated circuit package and mounted on different portions of the printed circuit board that houses the memory module. Ex. 1006, Figs. 9A–C.

Based on Petitioner's arguments on specific prior art disclosures and supporting evidence, we are persuaded that Petitioner sets forth sufficient articulated reasoning with rational underpinning to support the legal conclusion that it would have been obvious to modify the teachings of Averbuj with Tsern's teachings to include physically separate integrated chip packages. Pet. 40–42. For example, Petitioner asserts:

It would have been obvious to include the "separate integrated circuit packages" configuration of Tsern, including the distribution of self-test circuitry, in the system of Averbuj for several reasons. First, to do so would have been merely the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement. Tsern demonstrates that, before the priority date of the '501 Patent, it was within the average skill of the art to include a plurality of data handler circuits in physically separate integrated circuit packages, on a printed circuit board and that such circuits would operate as expected. Ex. 1003 at ¶ 167.

A skilled artisan would have been further motivated to implement the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj, particularly for the memory interfaces of Averbuj, in order to reduce the busing area a centralized approach would require. See, e.g., Ex. 1017 at 3:45-53; Ex. 1003 at ¶ 168.

A skilled artisan also would also have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj so that the self-test circuitry could be conveniently placed in the same packaging as buffer circuitry used to access and isolate different portions of the memory array. By the priority date of the '501 Patent it was known that separate buffers, in separate packages, for different portions of the memory array could advantageously reduce the load experienced by the memory controllers and improve the memory timing. Ex. 1018 at 1:5-23, Fig. 3; Ex. 1019 at 1:32-2:3, Fig. 5. A skilled artisan would therefore have been motivated to place the sequencers and the memory interfaces of Averbuj within such buffer components in order to reduce the load on the memory controller and also improve memory timing. Ex. 1003 at ¶ 169.

A skilled artisan also would have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj so that failing sequencers and memory interface components could be easily replaced, by

> simply replacing a standard package on the printed circuit board, without the necessity to replace other self-test circuitry in other packages that was operating normally. Ex. 1003 at ¶ 170.
>
> A skilled artisan also would have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj in order to place each data handler at positions on the PCB close and perhaps closest to its associated memory. Doing so would (i) simplify the wiring plan on the circuit board (Ex. 1021 at 6); (ii) reduce EMI interference and improve signal integrity (Ex. 1010 at 23-24, 207); and (iii) limit the capacitive load on those lines and permit faster and more efficient data transmission (Ex. 1020 at 2:27–3:6). See above at § V.C.1; Ex. 1003 at ¶ 171.

Id.

We also find that these findings regarding claim 4 are consistent with the findings of the '971 IPR that Averbuj meets the limitations of claim 1 such that those limitations, as they apply to claim 4, are met by collateral estoppel in this *inter partes* review.

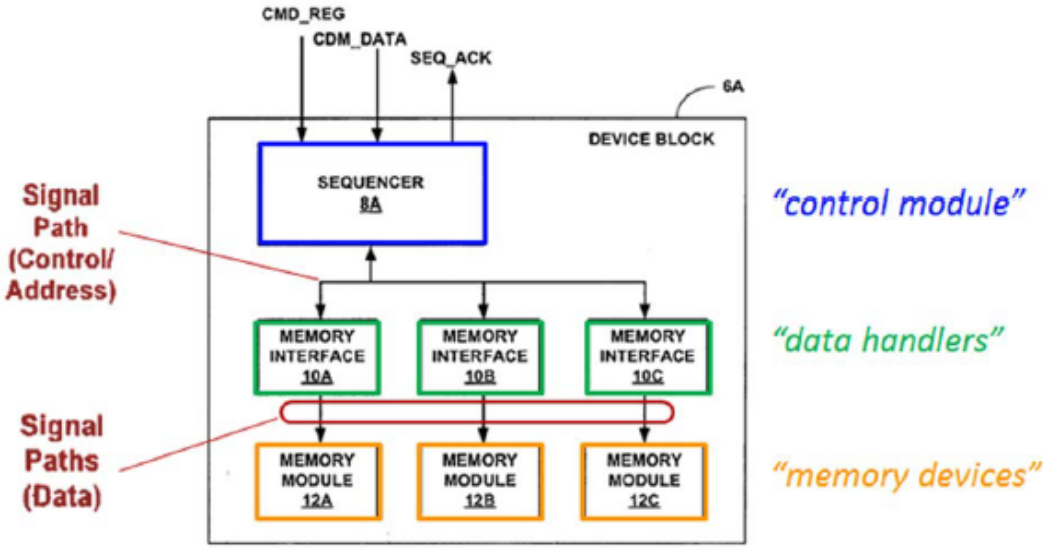
a. Patent Owner Response –Mapping of claim 1

Patent Owner's Response to the Petition was directed to an alternative mapping in which the address generation unit is mapped to the "control circuit." *See* generally PO Resp. Thus, the arguments in the Patent Owner Response are not relevant to any issue we seek to resolve in this Final Written Decision. This is because Patent Owner contends that Petitioner did not assert in the Petition that the limitations of claim 4 were met under the same mapping of Averbuj to claim 1 as was used in the '971 IPR. Mot. To Strike, 2–5.

To summarize the argument, the Petition presents three mappings that are directed to which component of Averbuj is mapped to the "control circuit" recited in claim 1. "Mapping 1," which is the same mapping used in

the '971 IPR, maps Averbuj's Sequencer to the "control circuit." Pet. 26–27. "Mapping 2," which was not at issue in the '971 IPR, maps the address generation unit to the "control circuit." Pet. 27–28. "Mapping 3," which was also not used in the '971 IPR, maps both the Sequencer and the address generation unit to the "control circuit." Pet. 28–29.

To illustrate Patent Owner's argument, we include below several annotated figures provided by Patent Owner. Below is Patent Owner's annotated version of Figure 4 of Averbuj alleged to represent Mapping 1. PO Show Cause Resp. 3.



Averbuj, Fig. 4

MAPPING 1

The annotated Figure 4, above, shows Mapping 1 of claim 1 limitations to Averbuj, the mapping used in the '971 IPR, in which the Sequencer alone is

the "control circuit."[8] PO Show Cause Resp. 3; Pet. 26–27 (Petitioner's contention that the sequencer alone meet the "control circuit" limitation).

Below are Patent Owner's edited and annotated versions of Figures 1 and 6 of Averbuj. PO Resp. 55.

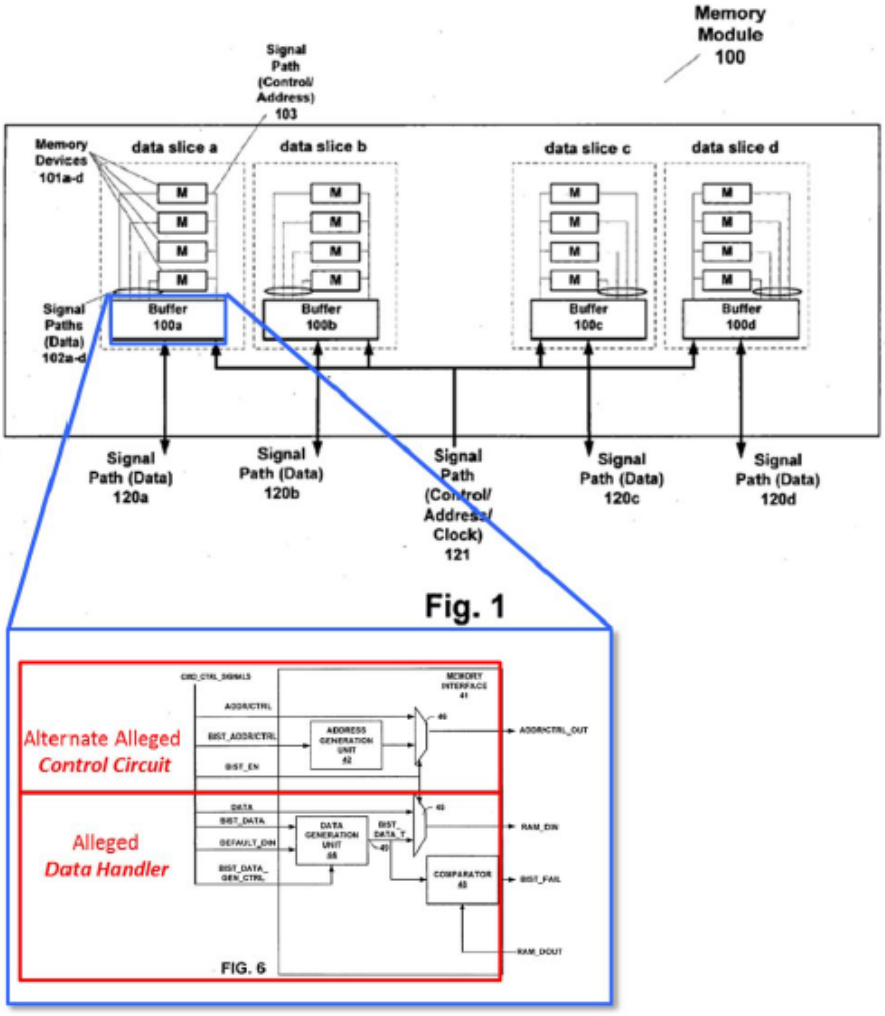


Fig. 1

MAPPING 2

[8] Unlike other Patent Owner annotated figures used in this Final Written Decision, this annotated figure does not show how each element would be placed on a separate IC as required by claim 4, however, in that case each element in the colored box would represent a different IC.

The annotated Figures 1 and 6, above, represents Mapping 2 in which the Address Generation Unit of Averbuj is mapped to the "control circuit."

Patent Owner does not include an annotated figure for Mapping 3, but it would be similar to Mapping 2, with the Sequencer included in the red box containing the Address Generation Unit. *See* Pet. 27–28.

As noted above, in Ground 3 discussing the combination of Averbuj and Tsern, the Petition states "A skilled artisan would have been further motivated to include the 'separate components' configuration of Tsern in the system of Averbuj, *particularly for the Memory Interfaces of Averbuj*, in order to reduce the busing area a centralized approach would require." Pet. 28–29 (emphasis added) (citations omitted). This statement does not mention where the "control circuit" is located or what component is mapped to the "control circuit." Petitioner asserts that claim 4 is directed to separating the "data handlers" from each other and is, at best, agnostic as to whether the "control circuit" is in the same IC as the data handlers. Tr. 12:14–19. We find these facts are sufficient to find that Petitioner did not limit its contentions regarding the combination of Averbuj and Tsern to Mapping 2 or Mapping 3.

Nevertheless, Patent Owner presents a further argument that claim 4 requires a one-to-many relationship between the "control circuit" and the "data handlers" such that Petitioner's theory under Ground 3 cannot meet the limitations of claim 1. We discuss that below.

b. Patent Owner Motion to Strike–One-to-Many

Patent Owner, in the Motion to Strike, asserts that because claim 1 recites that "wherein the memory system is configured to test the one or more memory chips using the address and control signals generated by the

control circuit and using the data generated by the one or more data handlers" there must be a one-to-many relationship between the "control circuit" and the "data handlers." Mot. to Strike 1–2. We disagree. The claim explicitly recites using signals from a "control circuit" and from a plurality of data handlers, but no explicit required connection between the plurality of "data handlers" and the "control circuit" is recited such that a one-to-many relationship is required. We also do not find any one-to-many relationship limitation was imported into the claims from the Specification by the Patentee. For that reason, as explained above, Petitioner has set forth a sufficient contention that the combination of Averbuj and Tsern would render obvious putting the "data handlers" in physically separate components.

Nevertheless, we will analyze this issue assuming that a one-to-many relationship is required such that having one "control circuit" in a chip with only one "data handler" would not meet the limitations of claim 1, which are incorporated into claim 4. This exercise may be slightly difficult to follow because it appears that Petitioner did not anticipate this one-to-many argument and simply focused on showing that the "data handlers" each could be put in separate components regardless of the mapping of the "control circuit." An additional difficulty is that this issue is separate and distinct from the mappings issue presented above.

i. Alleged Separate Component Theories

We begin by explaining Petitioner's theories regarding where the "control circuit" and "data handlers" are mapped in the grounds presented in the Petition. In the Petition, as to anticipation by Averbuj, Petitioner argued that

> Averbuj further discloses that the device block (6) and the components contained therein, such as the sequencer (8) and the memory modules (12), are 'distributed' and 'located throughout an electronic device,' i.e., physically separated. *See e.g.*, Ex. 1005 ¶¶ 13, 15; Ex. 1003 ¶ 127. Because memory interfaces (10, 41) are also components of each device block (6), at a minimum, the different sets of memory interfaces (10, 41) belonging to different device blocks (6) must also be physically separated. Ex. 1003 at ¶ 127

Pet. 30. Petitioner further argued that "Averbuj also discloses that the various integrated circuits or chips of an electronic device are 'mounted on a circuit board,' indicating that the integrated circuits and chips comprising the electronic device are packaged integrated circuits or chips." *Id.* Thus, Petitioner argued the memory interfaces 10A, 10B and 10C were physically separate. We disagreed that this contention, as presented in the Petition, met the reasonable likelihood standard for institution, stating "[c]laim 4 requires that the memory module be [] 'two physically separate integrated circuit packages.' Petitioner has not shown sufficient support for its broad reading that the memory system as claimed would be distributed across the device as Petitioner suggests." Inst. Dec. 19. Thus, we found that Averbuj did not show sufficiently that memory interfaces 10A, 10B, and 10C were physically separate ICs under Ground 1 as to anticipation by Averbuj.

As to Ground 2, Petitioner argues that separating components of the BIST architecture into physically separate ICs would have been "the use of a known technique for its known purpose and would have achieved only predictable results, such as the protection of integrated circuits by the packaging." Pet. 35. Petitioner asserts that memory modules at the time of the invention were composed of memory chips mounted on different portions of a memory board with BIST units in each memory chip. *Id.* at

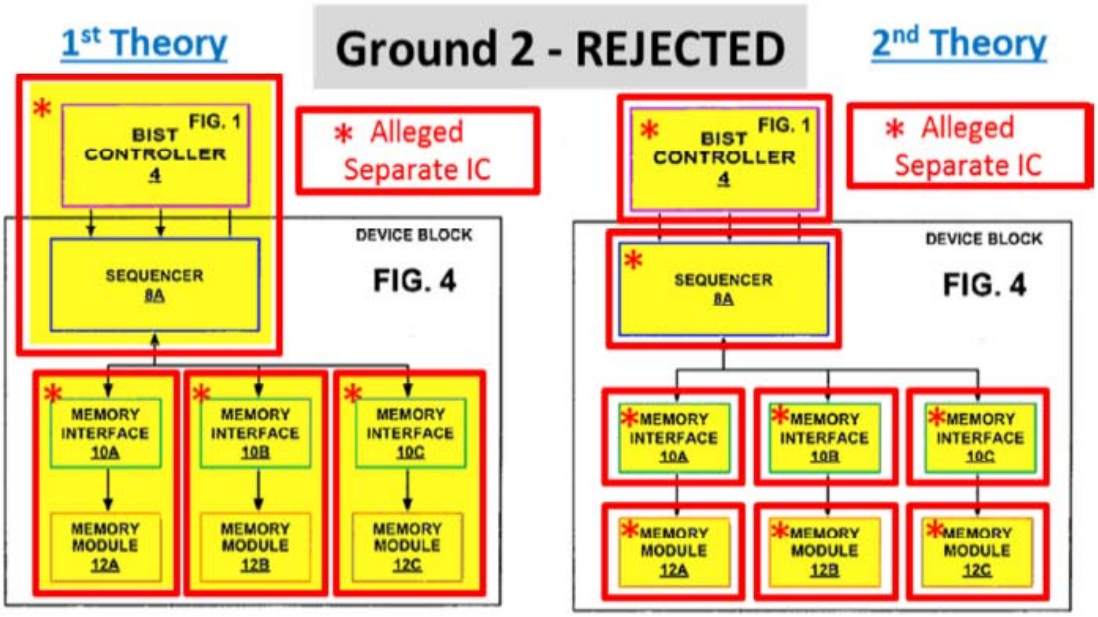
35–37. Given its assertion that memory chips mounted on different portions of a memory board with BIST units in each memory chip were known, Petitioner asserts that reducing redundancy is a motivation to modify Averbuj. *Id.*

> Specifically, Petitioner presents a first alternative asserting a skilled artisan would have understood that the BIST controller and sequencer portions of conventional BIST units would need to be removed from each memory chip and combined in order to reduce redundant circuitry . . . [but] a skilled artisan would also have understood and recognized that the memory interface portions need not be excised and implemented as a separate chip since doing so would not reduce much, if any, circuitry [thus remaining in a chip with the memory devices].

Pet. 36.

Later, also as to Ground 2, Petitioner presents a second alternative asserting "a skilled artisan, particularly a skilled artisan looking to implement Averbuj's BIST circuitry in a memory module that does not have a BIST circuitry, would have been motivated to incorporate each component of Averbuj's BIST circuitry—i.e., BIST controller, sequencers, and memory interfaces—into separate integrated circuit chips/packages" Pet. 37.

Reproduced below are Patent Owner's annotated versions of Figure 4 of Averbuj representing these two alternate theories as to Ground 2 which is obviousness based on Averbuj alone.

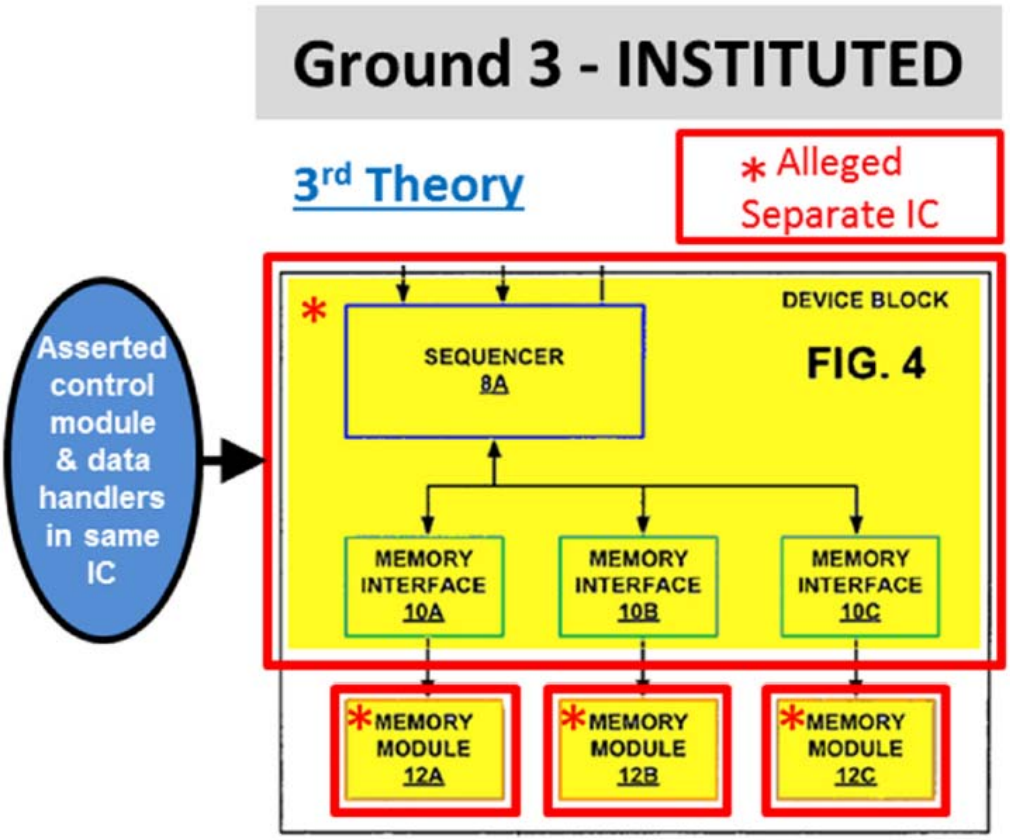


Patent Owner's annotated versions of Figure 4, above, accurately shows two alternate theories which are associated with Ground 2 based on obviousness over Averbuj alone. Mot. to Strike 3. These theories do not specify which component is the "control circuit." Pet. 35–37. In our Decision to Institute, we rejected these theories as relying on hindsight stating:

> As to Petitioner's arguments supported by its declarant, we agree with Patent Owner and find those to employ hindsight to piece together the device as claimed. Prelim. Resp. 46. The only evidence in the record of separating the data handlers and BIST controllers as claimed presented by Petitioner, other than the long complicated explanation of its declarant or the misplaced reliance on the structures of Tsern under this challenge, is in the '501 Patent itself.

Inst. Dec. 21. Thus, we found only that there was insufficient motivation shown, absent a combination with Tsern, to break up Averbuj's single chip architecture into an architecture in which the "data handlers" are in physically separate ICs.

Patent Owner represents what it considers Petitioner's Ground 3 theory in the annotated Figure 4 of Averbuj below. Mot. To Strike, 3.



As illustrated in the annotated Figure 4 of Averbuj, above, Patent Owner contends Petitioner is limited to a theory in which the Sequencer (the alleged "control circuit") and the memory interfaces (the alleged data handlers) are in the same IC. Mot. To Strike, 3.

ii. Patent Owner Asserts Petitioner's Ground 3 Theory does not include Sequencer Alone as the "Control Circuit"

With that background, Patent Owner's argument focuses on Ground 3 and the following statement in the Petition:

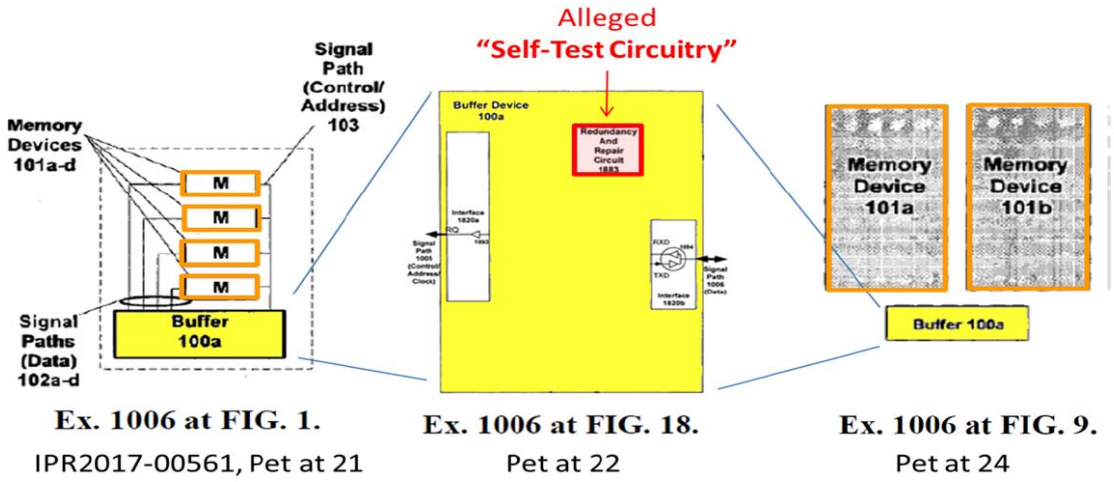
> A skilled artisan also would also have been motivated to include the "separate integrated circuit packages" configuration of Tsern in the system of Averbuj so that *the self-test circuitry could be*

> *conveniently placed in the same packaging as buffer circuitry* used to access and isolate different portions of the memory array. By the priority date of the '501 Patent it was known that separate buffers, in separate packages, for different portions of the memory array could advantageously reduce the load experienced by the memory controllers and improve the memory timing. Ex. 1018 at 1:5-23, Fig. 3; Ex. 1019 at 1:32-2:3, Fig. 5. A skilled artisan would therefore have been motivated to *place the sequencers and the memory interfaces of Averbuj within such buffer components* in order to reduce the load on the memory controller and also improve memory timing. Ex. 1003 ¶ 169.

Pet. 40–41 (emphasis added). Based on this statement, Patent Owner asserts Petitioner's theory under Ground 3 regarding the combination of Averbuj and Tsern is limited to a configuration in which the Sequencer and the memory interfaces are in the same chip such that the plurality of "data handlers" (memory interfaces) are not physically separate from the "control circuit." Mot. To Strike, 3–4. We note this paragraph does not mention the "control circuit" at all, but we will address that later. According to Patent Owner, this configuration would violate the so called "one-to-many" relationship required by claim 1. *Id.*

Petitioner responds that the statement that "the self-test circuitry could be conveniently placed in the same packaging as buffer circuitry" in the Petition was meant to express "that the components can be placed in the same type of packaging, not a single package." Mot. To Strike Resp. 5. We disagree. A reasonable reading of this statement is that a single buffer circuitry package would include "the self-test circuitry." Petitioner also responds that the statement "the Sequencers and the Memory Interfaces of Averbuj within such buffer components" in the Petition means "that each of the Sequencers (plural) and each of the Memory Interfaces can be placed in

a "buffer component" (i.e., "separate component"), not all in one." *Id.* We disagree. A reasonable reading of this sentence is that the Sequencers and Memory Interfaces would both be in the buffer component of Tsern. This is supported by Patent Owner's annotated figures, reproduced below, illustrating the Petition's summery of Tsern.



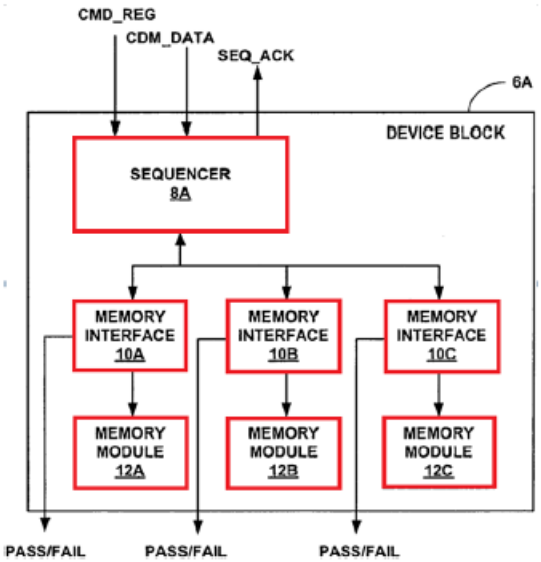
PO Show Cause Resp. 4. The annotated figures illustrate Patent Owner's assertion that the buffer that Petitioner refers to as the "separate component" contains the "self-test circuitry" which is contains the alleged "control circuit" (Sequencer) and the memory interface which is the alleged data handler. *Id.*

Nevertheless, Petitioner also responds that it had presented an argument that the "data handler" alone would be placed in separate chips. Resp. Mot. To Strike. 1–4. Petitioner ties a citation to the following statement from the Ground 2 Section of the Petition regarding obviousness over Averbuj alone to its argument regarding Averbuj in combination with Tsern. Reply 15 (citing Pet. at 34-35):

> It was known in the art to include circuit components of a memory system, including those components responsible for

> handling the transfer of data to and from a memory device, in physically separate integrated circuit packages, and to do so would have been well within the average skill in the art. See, e.g., Ex. 1006 at Fig. 9A; ¶¶ [0052-0053] (explaining that the depicted separate "buffer devices" are in one embodiment "housed in separate packages"); ¶ [0029] (noting that as used therein "an integrated circuit buffer device is also referred to as a buffer or buffer device."); Ex. 1003 at ¶ 143.

Pet. 34 (emphasis added). Petitioner's declarant states in the cited portion of his testimony that "the idea to implement the components of a memory module, such as the components responsible for handling the transfer of data to and from a memory device, in physically separate integrated circuit packages had already been proposed and adopted by the priority date of the '501 Patent." Ex. 1003 ¶ 143 (citing Ex. 1006, Fig. 9A, ¶¶ 52–53, 29). Reproduced below is an annotated version of Figure 4 of Averbuj from Petitioner's declarant's testimony. *Id.* ¶ 153.



Annotated Figure 4 above shows each memory interface in a separate IC. Ex. 1003 ¶ 153. This testimony is cited at page 37 of the Petition. Pet.

37. Thus, we find that Petitioner presented a contention that Averbuj, as modified in light of the structures of Tsern, teaches a Sequencer in a separate component from its associated memory interfaces. We acknowledge that petitioners routinely rely on earlier anticipation or single reference obviousness grounds to support and build up later combination grounds. *See Silicon Labs., Inc. v. Cresta Tech. Corp.*, Case IPR2015-00626, slip op. at 38 (PTAB Aug. 11, 2016) (Paper 65) ("Patent Owner characterizes the ground of unpatentability as if Petitioner relies only on Grumman for a 'signal processor' as claimed. Such is not the case. The ground of unpatentability against claim 24 must be understood in the context that it builds upon the ground against claim 1.").

Given that context, the Petition states later in the Ground 3 Section dealing with the combination of Averbuj and Tsern that

> Tsern further discloses that his buffer devices may be separate integrated circuit devices that can be housed in separate packages. Ex. 1006 at ¶ [0031] ("Likewise in an embodiment, an integrated circuit buffer device is distinguished from a buffer die in that a buffer die is a monolithic integrated circuit formed from semiconductor materials and performs at least one or more buffer functions described herein, whereas an integrated circuit buffer device is a buffer die having at least some form of packaging or interface that allows communication with the buffer die.") (emphasis added.); *see also id.* at ¶ [0053] ("In an embodiment, each memory device and buffer device are housed in separate packages."); ¶ [0043] ("packages used to house buffer devices 100a and 100d"); Ex. 1003 at ¶ 165.

Pet. 39. In the quoted portion above, the Petition cites the same section of Tsern, i.e. paragraph 53, as cited in support of Petitioner's contention that Averbuj alone rendered claim 2 obvious. The Petition also recites "[a] skilled artisan would have been further motivated to implement the 'separate

integrated circuit packages' configuration of Tsern in the system of Averbuj, particularly for the memory interfaces of Averbuj, in order to reduce the busing area a centralized approach would require.." *Id.* at 40 (citing Ex. 1017 at 3:45–53; Ex. 1003 ¶ 168.) Thus, as Petitioner points out in its response to the Motion to Strike, there are several statements in the Ground 3 portion of the Petition that can apply to Mapping 1, which was asserted in the '971 IPR, and which places the Sequencer itself (as the alleged "control circuit") in a separate IC from the "data handlers" thus satisfying the alleged one-to-many requirement of the claims. Mot. To Strike Resp., 2–5.

Patent Owner, in its Motion to Strike, argues that the contentions under this ground are either not sufficiently tied to Petitioner's theory under Ground 3 or that they were specifically rejected as hindsight in the Institution Decision. Mot. to Strike. 2–5. We note Petitioner cannot expect the Board to read through the entire record, searching for relevant evidence that might support Petitioner's arguments. *Cf., DeSilva v. DiLeonardi*, 181 F.3d 865, 866–67 (7th Cir. 1999)("[B]rief must make all arguments accessible to the judges, rather than ask them to play archaeologist with the record."). Nevertheless, the reference to Tsern and its structures under this ground is plainly relevant to Ground 3 based on Averbuj and Tsern. We decline to limit Petitioner's Ground 3 based on obviousness over Averbuj and Tsern to only the arguments made specifically in the section of the Petition labeled Ground 3.

We find that, based on all the parts of the Petition cited above, the Petition—without any *ex post facto* reconstruction by the Board—can be reasonably read to present two theories based on Averbuj and Tsern—one in which each portion of the device is in a separate component (or IC) and

possibly one in which the Sequencer and memory interfaces are together in the same component. *Cf. In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380–81 (Fed. Cir. 2016) (rejecting an argument that the Board properly "ma[de] an obviousness argument on behalf of [petitioner]" that "could have been included in a properly drafted petition," because "petitioner ... bears the burden of proof"). As noted above, we rely on collateral estoppel to show the limitations of claim 1. Thus, for the reasons above, Petitioner has shown sufficiently in the Petition its theory that each portion of the device, including the Sequencer and each memory interface, would be in separate components mounted on a printed circuit board, as recited by claim 4 even under Patent Owner's "one-to-many" construction of claims 1 and 4. Finally, as explained above, Petitioner has shown sufficient motivation to combine Averbuj and Tsern.

For the reasons above, we are persuaded by and adopt Petitioner's contentions as to the limitations of claim 4. Accordingly, upon review of the full record before us, we determine that Petitioner has demonstrated by a preponderance of the evidence that claim 4 is unpatentable over the combination of Averbuj and Tsern.

H. Patent Owner's Motion to Strike

Patent Owner moves to strike pages 13–16 of Petitioners' Reply and to exclude any argument based thereon, as violating Patent Owner's due process and procedural rights. Mot. to Strike 1. Pages 13–16 of Petitioner's Reply are directed to Ground 3 of the Petition which challenges claims 1 and 4 as rendered obvious by Averbuj and Tsern. In those pages, Petitioner argues that Patent Owner ignored Petitioner's alternative theory that the Sequencer alone is the "control circuit." Reply 13–16. As explained above

(Sections II. G. 2. b.), we do not find that Petitioner's Reply introduces a new theory. *See* Mot. to Strike Resp. 1–5. Thus, Patent Owner's Motion to Strike is denied.

I. Petitioner's Motion to Exclude

Petitioner moves to exclude Patent Owner's Exhibits 2005, 2006, 2012. Pet. Mot. to Excl. 1–2. Exhibits 2005 and 2012 relate to whether the BIST unit is in a single embedded chip and whether Averbuj's Sequencer is the "control circuit." This issue is moot because the limitations of claim 1 have been shown to be met by Averbuj by collateral estoppel. Thus, we deny the Petitioner's Motion to Exclude as to Exhibits 2005 and 2012.

Patent Owner does not oppose the motion to exclude Exhibit 2006. Pet. Mot. to Excl. Resp. 6. Thus, Petitioner's Motion to Exclude Exhibit 2006 is granted.

J. Patent Owner's Motion to Exclude

Patent Owner summarily moves to exclude paragraphs 1–45, 55–63, 71, 73, 80–82, 93, 99, 105, 114, 121, 125,131, 138, 142, 157, 162 and 166 of Exhibit 1003, along with the entirety of Exhibit 1022, because those paragraphs and that exhibit were submitted with, but were not cited in, the Petition. PO Mot. to Excl. 1.

Petitioner explains why each of the paragraph/exhibits are referred to indirectly; why they are relevant to a foreseeable issue even though they are not explicitly cited; and why Petitioner's reliance on these exhibits is not unfairly prejudicial to Patent Owner. PO Mot. to Excl. Reply 1–3. Patent Owner does not respond to those specific arguments except as to Exhibit 1022. PO Mot. to Excl. Resp. 2–3.

The paragraphs cited in Exhibit 1003 are general background of the expert and how he conducted his analysis and summaries of analysis that is cited in the Petition. Additionally, as above in relation to Petitioner's Motion to Exclude, many of the relevant paragraphs are moot due to the collateral estoppel issue.

The Board acts as both the gatekeeper of evidence and as the weigher of evidence. Rather than excluding evidence that is allegedly confusing, misleading, untimely, and/or irrelevant, we will simply not rely on it or give it little weight, as appropriate, in our analysis. Similar to a district court in a bench trial, the Board, sitting as a non-jury tribunal with administrative expertise, is well positioned to determine and assign appropriate weight to evidence presented, including giving it no weight. *See, e.g., Donnelly Garment Co. v. NLRB*, 123 F.2d 215, 224 (8th Cir. 1941) ("One who is capable of ruling accurately upon the admissibility of evidence is equally capable of sifting it accurately after it has been received ...."). Thus, in this *inter partes* review, the better course is to have a complete record of the evidence to facilitate public access as well as appellate review. Thus, as to the relevant paragraphs of Exhibit 1003, Patent Owner's Motion to Exclude is denied.

As to Exhibit 1022, this is a reference relied on by Dr. Mazumder to show the state of the art. PO Mot. to Excl. Reply 3. Patent Owner argues that this is an improper incorporation by reference. PO Mot. to Excl. Reply. 2–3 (citing 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference); *Oxford Nanopore Tech's Inc. v. University of Washington*, Case IPR2014-00512, slip op. (PTAB Sept. 14, 2014) (Paper 12); *Biodelivery Sciences Intern., Inc. v. Monosol RX, LLC*, Case IPR2015-00167, slip op.

(PTAB.May 20, 2015) (Paper 6); *Conopco, Inc. v. Procter & Gamble Co.*, Case IPR2013-00510, slip op. at 8 (PTAB Feb. 12, 2014) (Paper 9) ("We decline to consider information presented in a supporting declaration, but not discussed in a petition, because, among other reasons, doing so would encourage the use of declarations to circumvent the page limits that apply to petitions.")). 37 C.F.R. § 42.6(a)(3) prohibits incorporating arguments into the Petition by reference to other documents, and 37 C.F.R. § 42.104(b)(5) gives us discretion to "exclude or give no weight to . . . evidence" where the Petition "fail[s] to state its relevance." *See* 37 C.F.R. § 42.6(a)(3) ("Arguments must not be incorporated by reference from one document into another document."); 37 C.F.R. § 42.104(b)(5) ("The Board may exclude or give no weight to the evidence where a party has failed to state its relevance or to identify specific portions of the evidence that support the challenge."). Nevertheless, we are encouraged to consider all evidence of record that is probative of the background knowledge of a person of ordinary skill in the relevant technology. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362–63 (Fed. Cir. 2013). There is a balance between making sure the Petition is complete, as a stand-alone document, in stating everything necessary to meet the elements of establishing a preponderance of evidence of unpatentability, with the need for citation to, and reliance on, evidence to support each argument. Here, the balance tips in favor of Petitioner. The testimony regarding Exhibit 1022 is relevant to why Averbuj would be modified to the configuration in claim 4 in which the components are on separate ICs. This argument is fully explored in the Petition despite the lack of specific citation to Exhibit 1022. *See* Pet. 34–38 (citing, *inter alia*, Ex. 1003 ¶¶ 148–149 (citing Exhibit 1022)). We do not find that Dr. Mazumder's reference to this

Exhibit introduces argument that was not contained in the Petition or introduces material that was either excessive or material that the relevance of which is not explained. Thus, we deny Patent Owner's Motion to Exclude as to Exhibit 1022.

III. CONCLUSION

For the foregoing reasons, we determine claim 1 is anticipated by Averbuj under the doctrine of collateral estoppel. Thus, pursuant to 37 C.F.R. § 42.72, and the doctrine of collateral estoppel, this trial is terminated as to claim 1. Additionally, Petitioner has demonstrated, by a preponderance of the evidence, that claim 4 of the '501 Patent is unpatentable as obvious in view of Averbuj and Tsern.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claim 4 of the '501 Patent has been shown to be unpatentable;

FURTHER ORDERED, pursuant to 37 C.F.R. § 42.72 and the doctrine of collateral estoppel, that trial is terminated as to claim 1; and

FURTHER ORDERED Patent Owner's Motion to Strike is *denied;* Patent Owner's Motion to Exclude is *denied*; Petitioner's Motion to Exclude is *granted* as to Exhibit 2006 and *denied* as to Exhibit 2005 and 2012.

This is a final decision. Parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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