UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01413
Patent 6,069,507

PATENT OWNER'S NOTICE OF APPEAL

Director of the U.S. Patent and Trademark Office
c/o Office of the General Counsel
Madison Building East, 10B20
600 Dulany Street
Alexandria, VA 22314-5793

Pursuant to 35 U.S.C. §142 and 37 C.F.R. § 90.2(a), Patent Owner ProMOS Technologies, Inc. hereby provides notice of its appeal to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered on October 22, 2018 (Paper 33), and from all underlying orders, decisions, rulings and opinions provided therein.

Pursuant to 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal may include, but are not limited to:

1. Whether the Patent Trial and Appeal Board's claim construction was correct as to the term "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°";
2. Whether the Patent Trial and Appeal Board's claim construction was correct as to the term "selecting a switch position according to the determining step"; and
3. The Patent Trial and Appeal Board's determination of unpatentability of claims 10, 11, 13, and 15 of U.S. Patent No. 6,069,507 under 35 U.S.C. § 102.

Simultaneously with this submission, a copy of the Notice of Appeal is being filed with the Patent Trial and Appeal Board. In addition, the required copy of this Notice of Appeal, along with the docketing fee, are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Dated: December 26, 2018

Respectfully submitted,

By: */s/ Craig R. Kaufman*

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Certificate of Filing

I hereby certify that on December 26, 2018, pursuant to 37 C.F.R. § 90.2(a) a copy of Patent Owner's Notice of Appeal was filed with the Patent Trial and Appeal Board pursuant to the procedures provided in 37 C.F.R. § 42.6(b) by filing a copy using the PTAB E2E system.

I hereby certify that the required copies of Patent Owner's Notice of Appeal were filed with the required docketing fee on December 26, 2018 with the Clerk's Office of the United States Court of Appeals for the Federal Circuit.

CERTIFICATE OF SERVICE

I hereby certify that on December 26, 2018, a true and correct copy of the foregoing PATENT OWNER'S NOTICE OF APPEAL was served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

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Paper 33
Entered: October 22, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

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SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

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PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01413
Patent 6,069,507

Before JAMESON LEE, KEVIN F. TURNER, and JOHN A. HUDALLA, *Administrative Patent Judges.*

LEE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Petitioner[1] filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 10, 11, 13, and 15 of U.S. Patent No. 6,069,507 (Ex. 1001, "the '507 patent"). We instituted trial only as to claims 13 and 15 on the sole alleged ground of anticipation by Kim.[2] Pet. 3. Subsequent to the Supreme Court's decision in *SAS Institute v. Iancu*, 138 S. Ct. 1348 (2018), we instituted trial on the remaining claims and grounds presented in the Petition. Paper 16. Thus, included for trial are claims 10, 11, 13, and 15 on the sole alleged ground of anticipation by Kim.

Prior to our adding claims 10 and 11 to the trial, Patent Owner[3] filed a Patent Owner Response (Paper 11, "PO Resp.") addressing only claims 13 and 15.[4] Ordinarily, arguments in a Preliminary Response do not carry automatically over to the Patent Owner Response. However, after we added claims 10 and 11 to the trial, we allowed Patent Owner to rely on its Preliminary Response (Paper 6) insofar as it addressed claims 10 and 11, and Patent Owner waived the opportunity to supplement its Patent Owner Response to address claims 10 and 11. Paper 19. Petitioner filed a Reply addressing all challenged claims and grounds. Paper 22 ("Reply"). Patent Owner filed a Sur-Reply. Paper 25 ("SR").

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[1] Samsung Electronics Co., Ltd.

[2] U.S. Patent No. 5,875,219.

[3] ProMOS Technologies, Inc.

[4] Patent Owner also submitted the declaration of Mr. Bill Gervasi in support of the Patent Owner Response. Ex. 2002.

Oral argument was consolidated for IPR2017-01412 and IPR2017-01413, and held on June 21, 2018. A transcript of the consolidated oral argument has been entered as Paper 32.

We find that Petitioner has shown by a preponderance of the evidence that each of claims 10, 11, 13, and 15 is unpatentable.

B. Related Matters

Both Petitioner and Patent Owner have identified the following action as involving the '507 patent: *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd.*, No. 1:16-cv-00335-SLR (D. Del.). Pet. 1, Paper 5. Petitioner filed another petition for *inter partes* review of the '507 patent in IPR2017-01412. Petitioner further identifies these *inter partes* review proceedings between the parties that involve other patents: IPR2017-00032; IPR2017-00033; IPR2017-00035; IPR2017-00036; IPR2017-00037; IPR2017-00038; IPR2017-00039; and IPR2017-00040. Pet. 1–2. Patent Owner additionally identifies these *inter partes* review proceedings between the parties that involve other patents: IPR2017-01414, IPR2017-01415, IPR2017-01416, IPR2017-01417, IPR2017-01418, and IPR2017-01419. Paper 5.

C. The '507 Patent

The '507 patent relates to delay-locked loops (DLLs) and to reducing delay line length in DLLs. Ex. 1001, 1:7–9. The '507 patent notes that "[i]n order to achieve sufficient coverage of frequency ranges and guarantee desired resolution, DLLs generally require long delay lines." *Id.* at 1:14–18. Figure 1 is reproduced below:

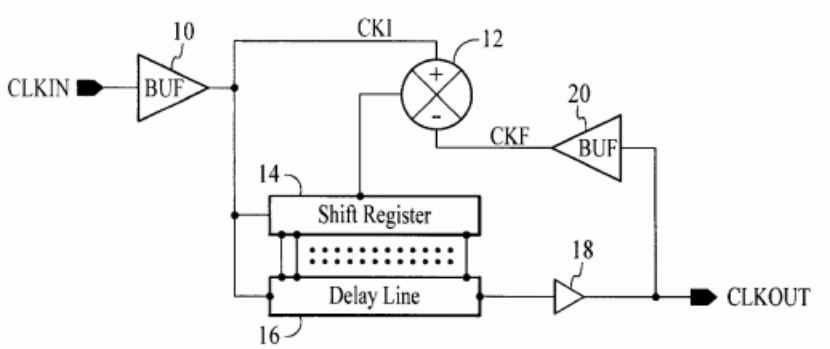

FIG. 1
(PRIOR ART)

Figure 1 illustrates a diagram of what the '507 patent regards as typical digital DLL according to the prior art. *Id.* at 2:24.

With respect to the prior art shown in Figure 1, input clock signal CLKIN is received at buffer 10 which provides a buffered clock signal CKI and which is coupled to phase detector 12, shift register 14, and delay line 16. *Id.* at 1:20–23. Delay line 16 is coupled to buffer 18 through which an output clock signal, CLKOUT, is produced. *Id.* at 1:23–25. The CLKOUT signal passes through buffer 20 to produce a feedback clock signal, CKF, to phase detector 12. *Id.* at 1:25–27. Phase detector 12 determines whether a phase difference exists between the buffered input signal CKI and feedback clock signal CKF. *Id.* at 1:27–29. The phase difference determines an appropriate shift in the buffered input clock signal via adjustment of shift register 14 to select sufficient delay via delay line 16. *Id.* at 1:29–32.

The '507 patent explains that there are several disadvantages with prior art type DDLs as clock speeds continue to increase. *Id.* at 1:34–36. To achieve high resolution and coverage of wide frequency ranges, the delay cells in delay line 16 and associated register cells in shift register 14 increase in number. *Id.* at 1:37–40. That expansion in length of the delay line leads

to larger silicon area requirements and higher power consumption, as well as longer lock-in time and larger frequency signal distortion. *Id.* at 1:43–47.

The '507 patent aims to overcome these disadvantages via the following disclosed method:

> [A] method for reducing delay line length in a digital delay locked loop (DLL) includes determining a phase difference between an input clock signal and a feedback clock signal, and maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°. The method also includes delaying the input clock signal to compensate for the phase difference, wherein a number of delay cells utilized is reduced by approximately one-half.

Id. at 2:3–11. In that regard, Figure 2 of the '507 patent is reproduced below:

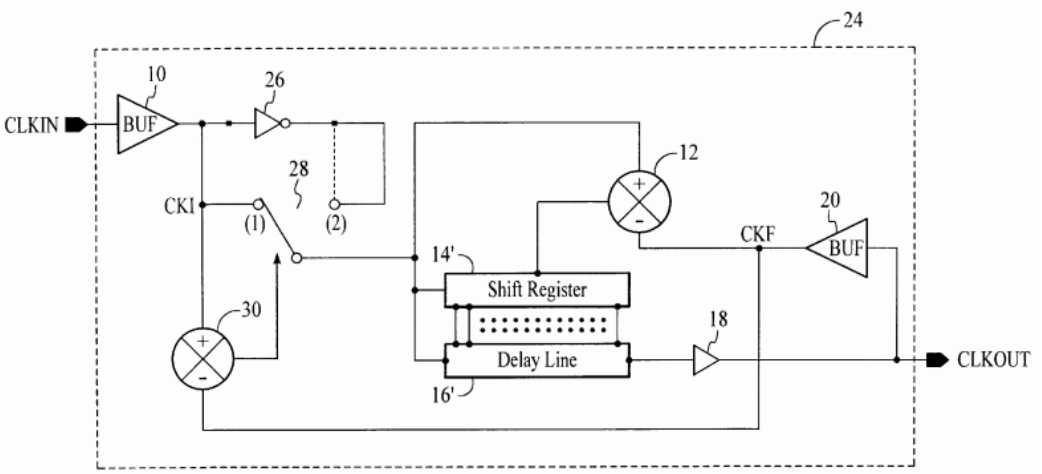

FIG. 2

Figure 2 illustrates a diagram of a DLL according to the '507 patent. *Id.* at 2:25–26. With respect to Figures 1 and 2, the '507 patent states that like components have been similarly numbered in the two figures. *Id.* at 2:49–51. As compared to the DLL of the prior art mentioned in the '507 patent, DLL 24 in Figure 2 of the '507 patent adds inverter 26, switch 28, and second phase detector 30. *Id.* at 2:55–57. According to the '507 patent, the length of delay line 16' and the corresponding number of cells in shift

register 14' are reduced as compared to the prior art DLL. *Id.* at 2:57–60.

Operation of DLL 24 in Figure 2 is described as follows:

> In operation, the second phase detector 30 preferably controls the course of the buffered input clock signal CKI by controlling the selection of the switch 28. When the second phase detector 30 determines that the feedback clock signal CKF from the DLL 24 is behind the buffered input clock CKI within a 180° phase difference, the second phase detector 30 controls the switch 28 to be at position (1). The inverter 26 is thus bypassed, and the operation of DLL 24 proceeds in a typical manner as described with reference to FIG. 1. With the second phase detector 30 determining that CKF was within 180° behind CKI, the delay line 16' is required to compensate for a less than 180° phase difference after the DLL 24 gets locked by the feedback through phase detector 12.
>
> When the second phase detector 30 determines that CKF is more than 180° behind CKI, the second phase detector 30 controls switch 28 to be at position (2). The inverted buffered clock signal is thus selected, so that the input clock signal CKI is reversed by 180°[.] Through the inversion, the phase difference needing to be compensated by the delay line 16' is made less than 180° and within the normal operation capabilities of the phase adjusting loop formed by phase detector 12, shift register 14', and delay line 16'.

Id. at 2:61 to 3:15. According to the '507 patent, DLL 24 as described above "requires approximately one-half the length that a typical DLL would require for comparable clock deskewing needs." *Id.* at 3:16–19.

Of all challenged claims, claims 10 and 13 are independent and are reproduced below:

> 10. A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:
>
> determining a phase difference between an input clock signal and a feedback clock signal;

maintaining the phase difference between the input clock signal and the feedback clock signal [within[5]] approximately 180°, including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°; and

delaying the input clock signal to compensate for the phase difference, wherein a number of delay cells utilized is reduced by approximately one-half.

13. A method for reducing delay line length in a digital delay lock look (DLL), the method comprising:

determining whether a feedback clock signal in the DLL follows within a 180° phase difference behind an input clock signal; and

selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal with[in[6]] 180°.

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[5] Based on an apparent error, the word "within" is missing from the maintaining clause as it appears in the published version of claim 10. During prosecution, Applicant amended the language of what became claim 10 to include, *inter alia*, the limitation "within approximately 180°." Ex. 1004, 58, 59. In the Notice of Allowance, the Examiner also acknowledged that the maintaining step recites "within approximately 180 degree[s]." *Id.* at 65. As indicated in our institution decision, we read claim 10 as including "within." Paper 7, 6 n.3. Neither party contested this reading in subsequent papers.

[6] The word "with" in the selecting clause evidently reflects a publishing error, and so we read it as the different word "within." During prosecution, the language of what became claim 13 recited the following limitation: "selecting a switch position according to the determining step," including "selecting a first switch position when the feedback clock signal follows behind the input clock signal *within* 180°." Ex. 1004, 27–28, 59 (emphasis added). The Examiner also used the word "within" when stating the reasons for allowing this claim. *Id.* at 65. As indicated in our institution decision,

Ex. 1001, 4:47–59; 4:66–5:7.

D. Evidence Relied Upon by Petitioner

Petitioner relies on the following references[7]:

Reference		Date	Exhibit
Kim	U.S. Pat. No. 5,875,219	Feb. 23, 1999, Filed January 2, 1997	Ex. 1009

Petitioner also relies on the Declaration of Jacob Baker, Ph.D., P.E. (Ex. 1002).

E. The Instituted Grounds

We instituted trial on the following ground of unpatentability. Paper 7, 26; Paper 16, 2.

Claim(s) Challenged	Basis	Reference
10, 11, 13, and 15	§ 102(e)	Kim

II. ANALYSIS

A. The Law on Anticipation

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). While the elements must be arranged in the same way as is recited in the claim, "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831,

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we read claim 13 as including "within. Paper 7, 6 n. 4. Neither party contested this reading in subsequent papers.

[7] The '507 patent was filed on May 22, 1998 and does not claim priority to any earlier application. Ex. 1001, [22].

832–33 (Fed. Cir. 1990)). Identity of terminology between the anticipatory prior art reference and the claim is not required. "A reference anticipates a claim if it discloses the claimed invention 'such that a skilled artisan could take its teachings in *combination with his own knowledge of the particular art and be in possession of the invention.*'" *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Also, "it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826 (CCPA 1968). As the Court of Appeals for the Federal Circuit recently explained, the dispositive question for anticipation is whether one skilled in the art would reasonably understand or infer from a prior art reference that every claim element is disclosed in that reference. *Eli Lilly v. Los Angeles Biomedical Research Inst.*, 849 F.3d 1073, 1074–1075 (Fed. Cir. 2017).

B. Level of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art at the time of the alleged invention of the '507 patent "would have had at least a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002, ¶¶ 18–19.)" Pet. 4 (footnote omitted). Patent Owner has not expressed what constitutes the level of ordinary skill in the art. We find Petitioner's proposal vague insofar as it includes the qualifier "at least" to describe the level of education and the amount of working experience. This qualifier results in ranges that are too broad to provide a meaningful indication of what knowledge and skills would have been possessed by one with ordinary

skill in the art. We adopt the level of skill in the art proposed by Petitioner, as we credit the testimony of Petitioner's declarant in that regard (Ex. 1002 ¶ 18), but eliminate the qualifier "at least" to eliminate vagueness.

C. Claim Construction

The Petition contends that the expiration date of the '507 patent is May 22, 2018. Pet. 10. Patent Owner does not dispute that expiration date. PO Resp. 5. Thus, the '507 patent has expired, and we construe the challenged claims according to rules applicable to expired patent claims.

We review expired patent claims according to the standard applied by the district courts. *See In re Rambus*, 694 F.3d 42, 46 (Fed. Cir. 2012). Specifically, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). Patent Owner agrees that the claim construction principles set forth in *Phillips* apply. PO Resp. 5. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). However, claim construction does not mean importing limitations into the claims in the name of construction, if the limitations are not otherwise there. As the Federal Circuit explained in *Phillips*,

> It is a "bedrock principle" of patent law that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Innova*, 381 F.3d at 1115; *see also Vitrionics*, 90 F.3d at 1582 ("we look to the words of the claims themselves . . . to define the scope of the patented invention"); *Markman*, 52 F.3d at 980 ("The written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of claims."). That principle has been recognized

> since at least 1836, when Congress first required that the specification include a potion in which the inventor "shall particularly specify and point out the part, improvement, or combination, which he claims as his own invention or discovery." Act of July 4, 1836, ch. 357, § 6, 5 Stat. 117, 119. In the following years, the Supreme Court made clear that the claims are "of primary importance, in the effort to ascertain precisely what it is that is patented." *Merrill v. Yeomans*, 94 U.S. 568, 570, 24 L.Ed. 235 (1876). Because the patentee is required to "define precisely what his invention is," the Court explained, it is "unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms." *White v. Dunbar*, 119 U.S. 47, 52, 7 S.Ct. 72, 30 L.Ed. 303 (1886); *see also Cont'l Paper Bag Co. v. E. Paper Bag Co.*, 210 U.S. 405, 419, 28 S.Ct. 748, 52 L.Ed. 1122 (1908) ("the claims measure the invention"); *McCarty v. Lehigh Valley R.R. Co.*, 160 U.S. 110, 116, 16 S.Ct. 240, 40 L.Ed. 358 (1895) ("if we once begin to include elements not mentioned in the claim, in order to limit such claim . . ., we should never know where to stop"); *Aro Mfg. Co. v. Convertible Top Replacement Co.*, 365 U.S. 336, 339, 81 S.Ct. 599, 5 L.Ed.2d 592 (1961) ("the claims made in the patent are the sole measure of the grant").

Phillips, 415 F.3d at 1312.

Claim terms generally are given their ordinary and customary meaning, as understood by one with ordinary skill in the art when read in the context of the specification and prosecution history. *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (citing *Phillips*, 415 F.3d at 1313). There are two exceptions to that rule: "1) when a patentee sets out a definition and acts as his own lexicographer," and "2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner*, 669 F.3d at 1365. Disavowal can be effectuated by language in the specification or the prosecution history. *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016). "In either case, the standard for disavowal is exacting, requiring

clear and unequivocal evidence that the claimed invention includes or does not include a particular feature." *Id.*

If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). "[T]he claims must 'not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.'" *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347 (Fed. Cir. 2015) (internal quotation omitted). Neither party contends that the Specification of the '507 patent specially defined any term or that the inventors of the '507 acted as their own lexicographer. We have no reason to determine otherwise.

If the words of the claim are clear, and absent the exceptions above, the claims should be interpreted as written and not rewritten in the name of claim construction. *SRAM Corp. v. AD-II Engineering Inc.*, 465 F.3d 1351, 1359 (Fed. Cir. 2006). In *SRAM Corp.*, the Federal Circuit stated:

> While SRAM strongly urges the court to interpret the claim to encompass the innovative precision indexing shifting feature it contends it has invented, *we are powerless to rewrite the claims and must construe the language of the claim at issue based on the words used*. *Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 951 (Fed. Cir. 1993). In this case, the words are clear and the claims cover no more than the recited method of taking up lost motion and effecting a shift.

SRAM Corp., 465 F.3d at 1359 (emphasis added); *see K-2 Corp. v. Solomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999) ("Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee.").

Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Wellman, Inc. v.*

Eastman Chem. Co., 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1.

"maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°"

Claim 10 includes a step of "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°." Ex. 1001, 4:51–53. In our institution decision, we construed this phrase to mean "ensuring that the feedback clock signal follows behind the input clock signal by less than approximately 180°." Paper 7, 12. We have reconsidered our initial construction in light of the entire trial record.

The "maintaining . . . [within] approximately 180°" recitation does not specify whether the input clock signal must be ahead of the feedback clock signal or the feedback clock signal must be ahead of the input clock signal. Without that restrictive recitation, either signal can be ahead of the other by within approximately 180°, and either signal can lag the other by within approximately 180°. That is how Petitioner has treated the limitation, i.e., that the within approximately 180° separation can be in either direction. Pet. 18–23, Reply 16.

That position is significant in this case, because there exist two different ways of looking at a phase lead or a phase lag. Petitioner's declarant, Dr. Baker, explains,

> A person of ordinary skill in the art would have understood that for two clock signals having the same frequency, and hence the same period, the phase difference between the two signals is always within approximately 180°. For example, if the feedback clock signal is lagging the input clock signal by 210°,

> that is the same as the feedback clock signal leading the input clock signal by 150°.

Ex. 1002 ¶ 62. From that perspective, for signals that have the same frequency and period, a particular phase lag is the same as a phase lead of an amount that is the 360° complement (difference from 360°) of the phase lag. Petitioner contends the limitation at issue is always satisfied by two clock signals having the same frequency and period in a system, because the 180° difference required by the limitation can be in either direction. Pet. 18–19 (citing Ex. 1002 ¶ 62).

Patent Owner does not dispute Petitioner's assertion that if the 180° difference required by the limitation can be in either direction, then the limitation always is satisfied by an input clock signal and a feedback clock signal that have the same frequency and period. Patent Owner, however, argues that a reading of the limitation covering a variation in either direction is inconsistent with the intrinsic record, i.e., the Specification and the prosecution history, and would, in effect, read the limitation out of the claim and render it meaningless. Prelim. Resp. 6. In essence, Patent Owner notes that a feedback clock signal is always either within 180° behind the input clock signal or within 180° ahead of the input clock signal, without exception. According to the Patent Owner, the limitation "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°" should be construed as meaning "ensuring that the feedback clock signal *follows behind* the input clock signal by less than 180°." *Id.* at 8 (emphasis added).

In the Decision on Institution, we determined that the above-noted arguments of Patent Owner were persuasive. Paper 7, 11. However, initial claim construction made at the time of institution of trial is not conclusive

and does not carry over necessarily to a Final Written Decision. Here, we must reassess the issue on the basis of the complete record developed during trial and also on a fresh review of the applicable binding case authority governing the law on claim interpretation. Based on the complete trial record, Patent Owner's arguments are not persuasive.

Subsequent to institution of trial, Petitioner submitted a Reply. Paper 22. It identifies and addresses numerous factors, all discussed below, that weigh in favor of Petitioner's claim construction, including (1) that we must respect the language of the claims in the absence of clear disavowal, Reply 15; (2) that the record does not support Patent Owner's contention that under Petitioner's broader construction, the limitation at issue is superfluous or meaningless, Reply 17–18; (3) that the prosecution history does not support an express disavowal by the patent applicant during pre-issuance examination, Reply 23–24; and (4) that the Specification of the '507 patent demonstrates the patent drafter knew how to describe the relationship between two clock signals in a manner that makes clear which clock signal leads or lags the other in phase, via express recitations with the words "behind" or "follows." Reply 19.

Patent Owner relies on general principles that urge in favor of "giving effect to all terms in the claim" and avoid rendering claim language "functionally meaningless." Prelim. Resp. 6. Those principles do not override the bedrock principle of patent law, explained in *Phillips*, that it is a claim that defines the covered invention and that it is "unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms." *Phillips*, 415 F.3d at 1312; s*ee McCarty*, 160 U.S. at 116 ("if we once begin to include elements not mentioned in the claim, in order to limit such claim . . ., we should never know where to

stop."). We must not, if the words of the claim are clear and if there is no disavowal, rewrite a claim in the name of claim construction. *SRAM Corp.*, 465 F.3d at 1359; *see also K-2 Corp.*, 191 F.3d at 1364. This is such a case. We must not rewrite the claims.

The words of the claim are clear in not specifying which signal leads or lags, and there is no express disavowal by Patent Owner, either in the Specification or in the prosecution history, as will be explained below. We must not rewrite the claim to add the requirement proposed by Patent Owner.

The Specification of the '507 patent describes,

> When the second phase detector 30 determines that CKF [feedback clock signal] is more than 180° behind CKI [input clock signal], the second phase detector 30 controls switch 28 to be at position (2). The inverted buffered clock signal is thus selected, so that the input clock signal CKI is reversed by 180°[.] Through the inversion, the phase difference needing to be compensated by the delay line 16' is made less than 180° and within the normal operation capabilities of the phase adjusting loop formed by phase detector 12, shift register 14', and delay line 16'.

Ex. 1001, 3:7–15.[8] The above-quoted description constitutes an affirmative disclosure of one embodiment, and not a disavowal of anything that is

[8] According to Petitioner, even this disclosed embodiment of the '507 patent does not ensure that the feedback clock signal follows behind the input clock signal by less than 180°, because in some instances, the switch continuously toggles between position (1) and position (2). Reply 19–23. We do not reach that issue because Petitioner would still prevail even if the sole embodiment disclosed in the Specification of the '507 patent ensures that the feedback clock signal follows behind the input clock signal by less than 180°.

different. Elsewhere in the Specification, there also is no clear language of disavowal.

Also, as noted by Petitioner (Reply 19–20), the Specification of the '507 patent demonstrates that Patent Owner knows how to describe the relationship between two clock signals in a manner that makes clear which clock signal leads or lags the other in phase, by using the word "behind" to indicate which signal lags the other. Ex. 1001, 2:63–66; 3:3–4; 3:8–9. Similarly, claim 13 recites "determining whether a feedback clock signal in the DLL *follows* within a 180° phase difference *behind* an input clock signal." *Id.* at 5:1–3 (emphasis added). By not rewriting the claim, we give effect to the words chosen by Patent Owner in drafting the claims. If they are so broad as to be functionally meaningless, they still are what the claim drafter has recited and Patent Owner could have sought correction during the pendency of the patent, e.g., seeking to reissue the patent claim.

With regard to the prosecution history, it is anything but clear even as presented by Patent Owner. Patent Owner's articulation is this:

> [T]he prosecution history makes clear that this limitation must be given meaning, and that it was important to the issuance of the patent over the art of record. During prosecution, claims that lacked this limitation were rejected as obvious over Butcher which, among other things, disclosed a system that included two clocks having the same frequency (and thus the same period). Ex. 1004 ('507 file history) at 45; Ex. 2001 (Butcher) at col. 4:9–16. Claim 11, which issued as claim 10, included the language being construed here, and was identified as allowable over the art of record. Ex. 1004 ('507 file history) at 65. Once the claim was amended to include the limitation "maintaining the phase difference between an input clock signal and a feedback clock signal [within] approximately 180 degree" it was allowed, and the Notice of Allowance stated: "As to claims 9, 11, and 15 [which issued as claims 8, 10 and 13], none of the prior art teaches the limitation "maintaining the phase difference between

> an input clock signal and a feedback clock signal within approximately 180 degree." *Id.*

Prelim. Resp. 7–8.

The above description by Patent Owner is internally inconsistent and self-contradictory. First, Patent Owner asserts that application claim 11, which issued as patent claim 10, already "included the language being construed here, and was identified as being allowable over the art of record." *Id.* at 7. Then, Patent Owner states "Once [application claim 11] was amended to include the limitation 'maintaining the phase difference between an input clock signal and a feedback clock signal [within] approximately 180 degree' it was allowed." *Id.* at 7–8. Patent Owner's suggestion that application claim 11 was amended to overcome a prior art rejection cannot be correct if it was allowable prior to the amendment. Instead, Petitioner's accounting of the prosecution history, partially reproduced below, is more accurate:

> Pending claim 11 already included the "maintaining" feature based on its dependency on claim 8 and had already been deemed to be allowable—while pending claim 8 was not. (Ex. 1004 at 26–27, 46.) Patentee never added the "maintaining" feature to claim 11. Instead, in responding to the Office Action, patentee simply rewrote claims 9 and 11 in independent form, incorporating the features of claim 8 from which they depended. (*Id.* at 58–59.)

Reply 24.[9] Also, as indicated by Petitioner, application claim 11 included additional limitations not present in claim 8 from which it depends. *Id.* at 23.

[9] In its Sur-Reply, Patent Owner asserts that the Examiner's Office Action stated that the Butcher reference discloses a method comprising all steps of claims 8–11 and 14 except for the step of "maintaining the phase difference between the input clock signal and the feedback clock signal within 180

Finally, Patent Owner points to this statement in the Examiner's Notice of Allowance: "As to claims 9, 11 and 15 [which issued as claims 8, 10 and 13], none of the prior art teaches the limitation 'maintaining the phase difference between an input clock signal and a feedback clock signal within approximately 180 degree[s].' *Id*." Ex. 1004, 65 (cited at Prelim. Resp. 8). However, the statement mentions nothing about whether one signal is behind or follows the other. Moreover, the statement was not made by the applicant for patent. Here, the applicant for patent remained silent with regard to the limitation at issue. With regard to Examiner's statements and responsive silence from applicants, the Federal Circuit has provided the following guidance:

> This court has recognized that an Examiner's Statement of Reasons for Allowance "will not necessarily limit a claim." *ACCO Brands, Inc. v. Micro Sec. Devices, Inc.*, 346 F.3d 1075, 1079 (Fed. Cir. 2003). Consequently, an applicant's silence regarding statements made by the examiner during prosecution, without more, cannot amount to a "clear and unmistakable disavowal" of claim scope. *See 3M Innovative Props.*, 350 F.3d at 1373–74 ("'Prosecution history . . . cannot be used to limit the scope of a claim unless the applicant took a position before the PTO.' *Schwing GmbH v. Putzmeister Aktiengesellschaft*, 305 F.3d 1318, 1324–25 (Fed. Cir. 2002) (emphasis added). An applicant's silence in response to an examiner's characterization of a claim does not reflect the applicant's clear and unmistakable acquiescence to that characterization if the claim is eventually allowed on grounds unrelated to the examiner's unrebutted characterization."). *After all, the applicant has disavowed nothing*.

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degrees." SR. 3. That assertion actually supports Petitioner's position that the maintaining feature already was present in claim 11 and was not added by amendment in response to the Examiner's Office Action.

Salazar v. Proctor & Gamble Co., 414 F.3d 1342, 1345 (Fed. Cir. 2005) (emphasis added).

Based on the foregoing, we see no disavowal by the applicant for patent in the prosecution history with regard to the subject matter of patent claim 10.

In any event, we find further that Patent Owner has not established that the limitation, if read plainly for what it states, i.e., allowing either the input clock signal or the feedback clock signal to lead or lag the other, is meaningless because the 180° phase difference would be met all the time by two signals whose frequencies are the same. Claim 10 does not require the input clock signal and the feedback clock signal to have the same frequency and period. Also, Patent Owner has not, as noted by Petitioner, argued "that a feedback clock signal and an input clock signal in a delay locked loop (DLL) always have the same frequency and period." Reply 17. In its Sur-Reply, Patent Owner points to cross-examination testimony of Dr. Baker indicating that a DLL is a circuit that synchronizes an input clock signal and an output clock signal, and that "synchronizes" means "the frequencies of the two clock signals would be the same." Paper 25, 3.

A Sur-Reply, however, is not an opportunity for Patent Owner to raise a new argument that should have been asserted earlier. Patent Owner has not, either in its Preliminary Response or its Patent Owner Response, asserted that in a DLL the input clock signal and the feedback clock signal necessarily would have the same frequency. Petitioner has not had a full opportunity to respond to this new argument. Accordingly, the new argument, raised for the first time in Patent Owner's Sur-Reply, will not be considered. *See* 37 C.F.R. § 42.23(b). On the record before us, we do not find that in a DLL the input clock signal and the feedback clock signal

always have the same frequency. But even if they did, we would not find merit in Patent Owner's proposed construction, as explained above.

For all of the foregoing reasons, we reject Patent Owner's proposed construction that the limitation "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°" requires the feedback signal to be behind the input clock signal. Rather, we conclude that this limitation imposes no directional requirement, so either signal can be ahead or behind the other by within approximately 180°."

2.

"selecting a switch position according to the determining step"

Claim 13 recites a step of "selecting a switch position according to the determining step." Ex. 1001, 5:4–5. We find, as Petitioner asserts (Reply 3), that the plain and ordinary meaning of this phrase is self-evident—a position of the switch is selected according to the determining step. The determining step, previously recited in claim 13, is this: "determining whether a feedback clock signal in the DLL follows within a 180° phase difference behind an input clock signal." *Id.* at 5:1–3. Claim 13 clearly recites only a general switch position based on the determination of whether the feedback clock signal follows the input clock signal by 180° or less, and does not require anything more about the generic switch position, e.g., what is on one end of the switch or what is on the other end of the switch, when the switch is placed in that selected position.

Patent Owner contends otherwise. According to Patent Owner, "selecting a switch position according to the determining step" should be construed to mean—*selecting a non-inverted input clock signal or an inverted input clock signal according to the determining step.* PO Resp. 5.

Patent Owner bases its contention on several theories, all of which are without merit, either individually or collectively, as discussed below.

First, Patent Owner refers to the disclosure in the Specification, which describes that according to the outcome of the determining step, i.e., whether the feedback clock signal follows the input clock signal by 180° or less, the switch selects either a non-inverted clock signal or an inverted clock signal for connection to the rest of the circuit. PO Resp. 2–4. According to Patent Owner, that is the "inventive concept" of the '507 patent, and its proposed construction "is consistent [with] the fundamental purpose of the invention provided in the '507 specification and file history. *Id.* at 4–5. Specifically, Patent Owner explains

> If the switch did not select either a standard or an inverted clock, then it would not have the effect of shifting the input clock by 180◦ when needed, and it would not have any relationship to the first "determining step" on which it relies. In other words, the first and second switch positions must select either a non-inverted or an inverted clock in order to provide any meaning to the claim term "according to the determining step."

Id. at 7.

We disagree that for "according to the determining step" to have any meaning, Patent Owner's proposed claim construction must be adopted. Rather, we find substantial meaning in "according to the determining step" without adding the non-inverted clock signal and the inverted clock signal as potential sources to the switch as proposed by Patent Owner. A different switch position is selected depending on the outcome of the determining step. We do not find that reading to be without meaning.

As for the "inventive concept" and "fundamental purpose" assertions of Patent Owner, they go about the claim interpretation process in a reverse manner, by starting with the patent disclosure first, and then ensuring,

notwithstanding what the claim language states, that more restrictive details are added to the claims under the name of claim interpretation. That is inappropriate. We must respect the language of the claims.

> It is a "bedrock principle" of patent law that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Innova*, 381 F.3d at 1115; *see also Vitrionics*, 90 F.3d at 1582 ("we look to the words of the claims themselves . . . to define the scope of the patented invention"); *Markman*, 52 F.3d at 980 ("The written description part of the specification itself does not delimit the right to exclude. That is the function and purpose of claims.").

Phillips, 415 F.3d at 1312. "We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that." *Thorner*, 669 F.3d at 1366–67. The Federal Circuit has explained,

> The Court's [trial tribunal] task is not to limit claim language to exclude particular devices because they do not serve a perceived "purpose" of the invention. Rather, the district court's function is to interpret claims according to their plain language unless the patentee has chosen to be his own lexicographer in the specification or has clearly disclaimed coverage during prosecution.

E-Pass Techs., Inc. v. 3COM Corp., 343 F.3d 1364, 1370 (Fed. Cir. 2003).

Nothing in the plain language of claims 13 or claim 15[10] imposes any restriction on what would be connected by the switch once a first or a second switch position is selected according to the results of the step of "determining whether a feedback clock signal in the DLL follows within a

[10] Claim 15 depends from claim 13 and recites "wherein selecting further comprises selecting a second switch position when the feedback clock signal does not follow the input clock signal within 180°. Ex. 1001, 6:1–4.

180° phase difference behind an input clock signal." Patent Owner incorrectly states

> The last element in claim 13 and claim 15 explicitly claim these two conditions – the switch selects a first position, which passes the non-inverted clock as the output, when the feedback clock signal follows within 180° behind the input clock signal. Likewise, when the output of the phase detector indicates the feedback clock follows by more than 180°, the switch is set to a second position, which passes the inverted clock as the output. Ex. 1001 ('507 patent) at claims 13, 15.

PO Resp. 6.

We decline to impose as a requirement the non-inverted input clock signal and inverted clock signal as signal sources for connection through the selected switch position, based on the outcome of the determining step, in the absence of clear and unmistakable disavowal of other types of connections effected through the switch.

Patent Owner identifies no express disavowal in the Specification, and we find none. Mere disclosure of one embodiment does not constitute disavowal of other embodiments, much less a clear and unmistakable disavowal. Furthermore, as Petitioner notes (Reply 5–6), independent claim 1 indicates that the inventors knew how to specify and indeed particularly specified the input clock signal and the inverted clock signal for connection by a switch in the context of claim 1. This fact urges against a finding of disavowal. Application of the doctrine of claim differentiation, which we recognize is not a hard and fast rule and is not itself determinative, leads to the same result.[11] The doctrine of claim differentiation is at its strongest

[11] Claim 14 depends from claim 13 and recites "wherein the first switch position selects the input clock signal for transfer through the DLL." Ex. 1001, 5:8–10. According to Patent Owner's proposed claim

where the limitation sought to be read into an independent claim already appears in a dependent claim. *Seachange Int'l., Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1368–69 (Fed. Cir. 2005). And, contrary to Patent Owner's arguments (PO Resp. 9), the facts here are unlike those in *Retractable Techs., Inc. v. Becton, Dickenson & Co.*, 653 F.3d 1296 (Fed. Cir. 2011). There, the specification contained what was sufficient for a finding of disavowal, and that superseded a contrary indication by application of the doctrine of claim differentiation. *Retractable Techs.*, 413 F.3d at 1305 ("In distinguishing prior art syringes comprised of multiple pieces, the specifications state that the prior art had failed to recognize a retractable syringe that 'can be molded as one piece outer body.'"). Our reading of the claim is not dependent on application of the doctrine of claim differentiation. We note simply that application of the doctrine reaches the same result.

Patent Owner argues that the prosecution history of the '507 patent supports its restrictive reading of the claims. PO Resp. 7. We disagree. Patent Owner has identified no express disavowal by the applicant for patent that would so limit the claims and we can find none.

"[T]he doctrine of prosecution history disclaimer only applies to unambiguous disavowals." *Grober v. Mako Products, Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012). At most, Patent Owner's arguments indicate that the specification is vague and ambiguous. It shows no clear disavowal of any kind by the patent applicant. Patent Owner states:

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construction, this feature already would have been required by claim 13 and need not be expressly recited in claim 14. Similarly, claim 16 depends form claim 15 and recites "wherein the second switch position selects an inverted input clock signal for transfer through the DLL." *Id.* at 6:5–7.

> During prosecution, the examiner allowed claim 13 based on the understanding that it required "maintaining the phase difference between an input clock signal and a feedback clock signal within approximately 180 degrees." Ex. 1004 ('507 file history) at 65. The phase difference is maintained by the switch's selection of the non-inverted or inverted clock – precisely ProMOS's construction.

PO Resp. 7. Patent Owner further states: "While other claims state explicitly 'maintaining' the phase difference, claim 13 claims this concept as: 'selecting a switch position according to the determining step.'" *Id.* at 8.

There is no statement in the prosecution history, either from the Examiner or from the patent applicant, that the limitation "maintaining the phase difference between an input clock signal and a feedback clock signal within approximately 180 degrees" is the same or equivalent in scope as "selecting a switch position according to the determining step." There also is no statement in the prosecution history, either from the Examiner or from the patent applicant, that the limitation "selecting a switch position according to the determining step" is the same or equivalent in scope as "selecting a non-inverted input clock signal or an inverted input clock signal according to the determining step." And, as Petitioner explains persuasively, there is no such equivalency. Reply 8. One does not necessarily mean the other, and vice versa.

In any event, the patent applicant made no representation of any kind that constitutes an express disavowal of any claim scope. As we discussed above, an applicant's silence regarding statements made by the examiner during prosecution, without more, cannot amount to a clear and unmistakable disavowal. *Salazar*, 414 F.3d at 1345.

Patent Owner further argues that the Examiner rejected several claims including what is now claim 13 but indicated that certain claims would be

allowable if they incorporated the concept of a "switch controlled by the second phase detector for switching between the non-inverting input clock signal and the inverting clock signal." PO Resp. 8. According to Patent Owner, the patent applicant then amended what issued as claim 13 to include the determining step and the clock selection step, and then the Examiner allowed the claim. *Id.* That is not an accurate accounting of the prosecution history.

As we discussed above, claim 13 includes no "clock" selection step, just the general step of "selecting a switch position according to the determining step" which refers to nothing about an input clock signal or an inverted clock signal being coupled by the switch through any selected switch position. Additionally, Petitioner correctly notes that application claim 15 was not amended by the patent applicant to add any limitation in response to the Examiner's suggestion of adding the concept of a "switch controlled by the second phase detector for switching between the non-inverting input clock signal and the inverting clock signal." Reply 9–10.

The step of "selecting a switch position according to the determining step" already was recited in application claim 15, which depended from claim 14, and the applicant merely rewrote application claim 15 in independent form to include the features of claim 14 except for the limitation "wherein fewer delay line cells are needed to compensate for phase difference in the DLL." Ex. 1004. 27–28, 59, 61 (cited at Pet. 10). Steps involving connecting a clock signal through the selected switch position were present in then pending application claims 16 and 18 but were not added to application claim 15 which issued as patent claim 13. *Id.* at 28.

We recognize that Patent Owner's declarant, Mr. Gervasi, has testified: "It is my opinion that [Patent Owner's] construction is consistent

with the '507 patent and how one of ordinary skill in the art would understand the term." Ex. 2002 ¶ 28. We do not credit that testimony, because Mr. Gervasi does not adequately explain why the plain claim language of "selecting a switch position according to the determining step" should be read restrictively to require a selection between non-inverted and inverted input cock signals. As discussed above, it is claims which define the scope of an invention, not the Specification.

For the foregoing reasons, we find no clear and unmistakable disavowal in either the Specification or the prosecution history, and we reject Patent Owner's proposed reading of "selecting a switch position according to the determining step" as requiring a selection between non-inverted and inverted input clock signals. Instead, no express construction is necessary and the plain and ordinary meaning of "selecting a switch position according to the determining step" applies.

D. Alleged Unpatentability of Claims 10, 11, 13, and 15 as Anticipated by Kim

1. Kim

Kim pertains to and discloses a digital phase delay locked loop (DLL). Ex. 1009, 2:46–47. Figure 3 of Kim is reproduced below:

FIG. 3

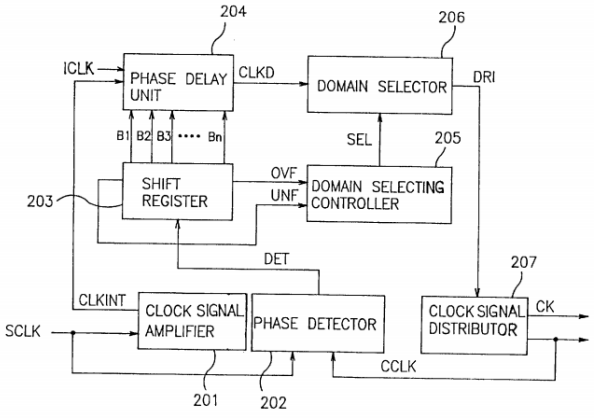


Figure 3 illustrates a schematic block diagram of a phase delay correction apparatus according to Kim. Ex. 1009, 3:3–4. With regard to Figure 3, Kim describes:

> FIG. 3 is a schematic block diagram of a phase delay correction apparatus according to the present invention, which includes a clock signal amplifier 201 for amplifying a system clock signal (SCLK), a phase detector 202 for outputting a comparing signal (DET) by comparing the phases of the system clock signal (SCLK) and a chip clock signal (CCLK), a shift register 203 for sequentially shifting data (0 or 1) in two directions in accordance with the comparing signal (DET) from the phase detector 202, a phase delay unit 204 for outputting a phase-adjusted clock signal (CKLD) by delaying the output of the clock signal amplifier 201 in accordance with the bit values of the shift register 203, a domain selecting controller 205 for outputting a domain selection controlling signal (SEL) by detecting an overflow signal (OVF) or an underflow signal (UNF) generated by the shift register 203, a domain selector 206 for outputting a driving signal (DRI) of an operation domain corresponding to the domain selection controlling signal (SEL) from the domain selecting controller 205, and a clock signal distributor 207 for distributing a clock signal (CK) and the chip clock signal (CCLK) in accordance with the driving signal (DRI) from the domain selector 206 and feeding back the clock signal (CK) and the chip clock signal (CCLK) to the phase detector 202.

Id. at 3:22–45. Phase detector 202 outputs a "1" to the shift register when it is determined that chip clock signal (CCLK) leads the system clock signal (SCLK), and outputs a "0" to the shift register when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase. *Id.* at 5:14–19.

When the comparing signal from the phase detector is a "1," a data bit "1" is shifted one bit to the right from the left side of the shift register as shown in Figure 3, and when the comparing signal from the phase detector is a "0," a data bit "0" is shifted one bit to the left from the right side of the shift register as shown in Figure 3. *Id.* at 3:46–55, 5:20–28. When all the

bits in the shift register are "0" and the comparing signal from the phase detector is a "0," then the shift register outputs an underflow (UNF) signal. *Id.* at 3:55–59. When all the bits in the shift register are "1" and the comparing signal from the phase detector is a "1," then the shift register outputs an overflow (OVF) signal. *Id.* at 3:60–64, 5:29–36.

Whenever an overflow or underflow signal is provided by the shift register to domain selecting controller 205, the domain selecting controller outputs a selection controlling signal (SEL) to domain selector 206, which then selects a corresponding one of two domains, 0° to 180° as one domain and 180° to 360° as another domain. *Id.* at 7:11–18, 7:32–36. Figure 6 of Kim is reproduced below:

FIG. 6

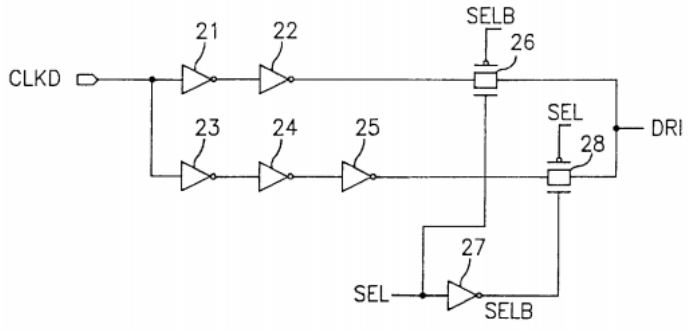


Figure 6 illustrates the schematic diagram of a domain selector shown in Figure 3. *Id.* at 3:9–10. When the domain selection controlling signal SEL is "1," the phase-adjusted clock signal from phase delay unit 204 is sequentially delayed through inverters 21 and 22, and when the domain selection controlling signal SEL is "0," the phase-adjusted clock signal from phase delay unit 204 is sequentially delayed through inverters 23, 24, and 25. *Id.* at 7:19–30. Thus, depending on the determined domain, 0° to 180° or

180° to 360°, the clock signal is inverted when provided as output driving signal DRI.

When the shift register outputs an overflow signal, the data bits in the shift register are reset to "0." *Id*. at 6:7–11. In contrast, when the shift register outputs an underflow signal, the data bits in the shift register are set to "1." *Id*. at 6:44–48. As described above, Kim discloses performing a standard phase shift in a first domain, and an inversion in the second domain. The same length shift register can be used to cover both domains. Kim states: "[T]he present invention has the effect that a phase shift apparatus having a more precise resolution can be embodied, by reducing the number of the elements comprising the delay units." *Id*. at 10:9–12.

2. Claim 10

Claim 10 recites: "A method for reducing delay line length in a digital delay locked loop (DLL)." Ex. 1001, 4:47–48. Kim discloses such a method. Kim discloses a digital delay locked loop. Ex. 1009, 2:46–63 (cited at Pet. 11). Regarding the reduction in delay line length, Kim states: "the present invention has the effect that a phase shift apparatus having a more precise resolution can be embodied, by reducing the number of the elements comprising the delay units." *Id*. at 10:9–12 (cited at Pet. 13). Reducing the number of elements in the delay units meets the "reducing delay line length" limitation.

Claim 10 further recites: "determining a phase difference between an input clock signal and a feedback clock signal." Ex. 1001, 4:49–50. Kim discloses this step. Kim's phase detector 202 receives SCLK and CCLK as inputs and makes a comparison of the two. Ex. 1009, 3:24–27 (cited at Pet. 15). Phase detector 202 outputs a "1" to the shift register when it is determined that CCLK leads SCLK, and outputs a "0" to the shift register

when CCLK trails SCLK. *Id.* at 5:14–19 (cited at Pet. 17). Dr. Baker testifies: "A person of ordinary skill in the art would have understood that if a clock 'lags' another clock in phase, it 'follows within a 180° phase difference behind the other clock.'" Ex. 1002 ¶ 92. Dr. Baker further explains that where CCLK leads the SCLK, that is the equivalent to the CCLK following the SCLK by more than 180°. *Id.* ¶ 95. The comparison phase detector 202 performs on the input clock signal and the feedback clock signal meets the recited step of "determining a phase difference between an input clock signal and a feedback clock signal," because the comparison result indicates categorically whether the CCLK leads or lags the SCLK, or whether the CCLK is within 180° behind the SCLK.

Claim 10 further recites: "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°, including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°.)" Ex. 1001, 4:51–55. Hereinafter, we refer to this limitation as "the maintaining step."

First, Petitioner argues that the phase difference between two clock signals having the same frequency, and hence the same period (e.g., Kim's system clock signal SCLK and chip clock signal CCLK), is always within approximately 180°. Pet. 19 (citing Ex. 1002 ¶ 62).

Second, Petitioner argues that because Kim's delay locked loop maintains the difference between the SCLK and CCLK to near zero degrees, which is "within approximately 180°," Kim discloses "maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°." Pet. 21–22.

Petitioner explains Kim's disclosure as follows,

> Thus, when the chip signal (CCLK) leads the system clock signal (SCLK), a "1" bit is shifted into the shift register 203 from the left, with the existing content of the data bit units each being shifted by one cell to the right, and when the chip clock signal (CCLK) trails the system clock signal (SCLK), a "0" bit is shifted into the shift register 203 from the right, with the existing contents of the data bit units each being shifted by one cell to the left. (Ex. 1002, ¶ 70.)
>
> Kim discloses that the "phase delay unit 204 is controlled by the bit values (B1, B2, . . . , B_n) outputted from the shift register 203." (Ex. 1009, 6:50–51.)

Pet. 25. The explanation is supported by the testimony of Dr. Baker.

Ex. 1002 ¶ 70. In more detail, Petitioner explains,

> Thus, when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase, DET is set to '1', which causes a '1' bit to be shifted into the shift register 203, which in turn increases the delay applied by the phase delay unit 204; and when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase, DET is set to '0', which causes a '0' bit to be shifted into [] shift register 203, which in turn decreases the delay applied by the phase delay unit 204. ([Ex. 1002], ¶ 72.)
>
> *Kim* discloses that the phase delay unit 204 applies delay to clock signal CLKINT, which is an amplified version of system clock signal SCLK. (Ex. 1009, 4:47–49, ("The delay units 24-1, 24-2, . . . 24-(n-1) each includes series inverters 16, 17 which sequentially delay the clock signal (CLKINT) from the clock signal amplifier 201"), FIG. 3; *see also id.*, 6:50–54; Ex. 1002, ¶ 73.) *Kim* further discloses that the chip clock signal CCLK is based on the phase-adjusted clock signal CLKD outputted by the phase delay unit 204. (Ex. 1009, 3:30–45, FIG. 3.) Therefore, a person of ordinary skill in the art would have understood that Kim's delay locked loop described with reference to figure 3 operates to maintain the system clock signal SCLK phase-aligned with the chip clock signal CCLK, i.e., with a goal of maintaining 0° of phase difference. (Ex. 1002 ¶ 73.) . . . . A person of ordinary skill in the art would have understood that

> once the delay locked loop of *Kim* has locked (i.e., achieved the best phase alignment between CCLK and SCLK that it can), it will alternate back and forth between detecting the chip clock signal (CCLK) slightly lagging the system clock signal (SCLK) at which point it will reduce the delay slightly, and then detecting the chip clock signal (CCLK) slightly leading the system clock signal (SCLK) at which point it will increase the delay slightly. (*Id.*) Once locked, the phase of the chip clock signal (CCLK) will move back and forth over the ideal point of alignment such that the chip clock signal (CCLK) jitters back and forth between lagging and leading the system clock signal (SCLK). (*Id.*)

Pet. 26–28. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶¶ 72–73. We credit Dr. Baker's testimony and give it substantial weight. Notwithstanding Patent Owner's arguments to the contrary, discussed below, we are persuaded by Petitioner's showings, summarized above, that Kim discloses "maintaining the phase difference between the input clock signal and the feedback clock signal within approximately 180°."

With regard to the recitation "including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line," the above explanations fully account for the adjustment of the input clock signal using a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°. Additionally, Petitioner makes reference to Kim's Figure 3, reproduced below,

FIG. 3

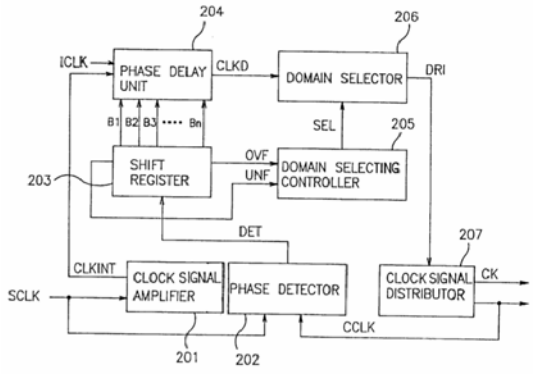


Figure 3 illustrates a schematic block diagram of a phase delay correction apparatus according to Kim. Ex. 1009, 3:3–4.

Further with regard to Kim's Figure 3, Petitioner explains,

> The delay locked loop shown in figure 3 of Kim operates to adjust the system clock signal (SCLK) ("input clock signal") when the determined phase difference is less than approximately 180°. As discussed above, the delay locked loop described in Kim in conjunction with figure 3 continuously adjusts the system clock signal (SCLK) ("input clock signal") to produce the chip clock signal (CCLK) ("feedback clock signal"). (Ex. 1002, ¶ 75, citing Ex. 1009, 9:61-63 ("Then the chip clock signal (CCLK) is fed back to the phase detector 202, and the operation is repeatedly performed.").)

Pet. 29. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶ 75. We credit Dr. Baker's testimony and give it substantial weight.

With regard to the requirement that the adjusting action or operation be done "when the determined phase difference is less than approximately 180°," Petitioner explains that because Kim is constantly adjusting the delay of the system clock signal (SCLK) to maintain a phase difference that is near zero degrees, Kim discloses that the adjusting occurs "when the determined phase difference is less than approximately 180°." Pet. 31–32. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶ 79. We credit Dr. Baker's testimony and give it substantial weight. Petitioner establishes that Kim discloses the recited timing condition.

Kim also teaches timing recited by "when the determined phase difference is less than approximately 180°" for an alternative reason. Dr. Baker testifies that a person of ordinary skill in the art would have understood that the system clock signal (input clock signal) and the chip

clock signal (feedback clock signal) of Kim have the same frequency and therefore the phase difference between them is always within approximately 180°. Ex. 1002 ¶ 64 (cited at Pet. 20–21); *see also id.* ¶¶ 62–63, 76. We credit Dr. Baker's testimony and give it substantial weight.

Patent Owner disputes Petitioner's contention that the maintaining step reads on Kim's jittering scheme. Prelim. Resp. 11. In particular, Patent Owner cites Petitioner's contention that, "[o]nce locked, the phase of the chip clock signal (CCLK) will move back and forth over the ideal point of alignment such that the chip clock signal (CCLK) jitters back and forth between lagging and leading the system clock signal (SCLK)." Pet. 28. Patent Owner contends that "[t]his kind of jitter . . . is not 'maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°' because Kim continuously moves the feedback signal out of that range." Prelim. Resp. 11. This argument is based on Patent Owner's proposed construction of "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°," whereby even a very small lead of the feedback clock signal over the input clock signal causes claim 10 not to be met, because the feedback clock signal must follow the input clock signal by less than 180°. *Id.* at 8.

We have, however, rejected Patent Owner's proposed claim construction. *See supra* § II.C.1. We do not read any requirement that the feedback clock signal must follow the input clock signal into the meaning of "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°," and agree with Petitioner that the recitation is met by either the feedback clock signal or the input clock signal being behind the other by less than approximately 180°.

Consequently, the jittering that occurs in Kim, as noted by Patent Owner, does not undermine or discredit Petitioner's analysis in any way. Based on our claim construction, Patent Owner's argument is without merit.

Claim 10 further recites "delaying the input clock signal to compensate for the phase difference." Ex. 1001, 4:57–58. As discussed above, Petitioner's analysis regarding the maintaining step already accounts for the step of "delaying the input clock signal to compensate for the phase difference" through the explanation of how Kim gets the phase difference between the input clock signal and the feedback clock signal down to near zero degrees. Petitioner further explains,

> *Kim* discloses that "the phase delay unit 204 is controlled in accordance with the bit values (B1, B2, . . . , B_n) outputted from the shift register" (Ex. 1009, 4:40–42; *see also id.*, 6:50–51), where those bit values are set based on the value of the comparing signal DET, which in turn is based on the determined phase difference. (*See supra*, Section IX.A.1(c); Ex. 1009, FIG. 3; Ex. 1002, ¶ 82.) Consequently, as discussed above with respect to limitation 10(c), when the chip clock signal (CCLK) leads the system clock signal (SCLK) in phase, the delay applied by the phase delay unit 204 is increased, and when the chip clock signal (CCLK) trails the system clock signal (SCLK) in phase, the delay applied by the phase delay unit 204 is decreased. (*See supra* Section IX.A.1(c); Ex. 1002, ¶ 82.) Thus, Kim discloses performing delaying the system clock signal (SCLK) ("delaying the input clock signal") where the delay is adjusted based on whether the chip clock signal (CCLK) leads or lags the system clock signal (SCLK) ("to compensate for the phase difference"). (Ex. 1002 ¶ 82.)

Pet. 34. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶ 64. We credit Dr. Baker's testimony and give it substantial weight. We find that Kim discloses the step of "delaying the input clock signal to compensate for the phase difference."

Finally, claim 10 recites "wherein a number of delay cells utilized is reduced by approximately one-half." Ex. 1001, 4:58–59. Petitioner's analysis, as discussed above, regarding the preamble of claim 10 already accounts for Kim's disclosure of reducing the delay line length. Petitioner further explains "Kim discloses that '**the number of the delaying elements of the present invention can be reduced to half**, since the phase shift is performed only in the first domain and the phase shift in the second domain is performed inverse to the phase shift in the first domain.' (Ex. 1009, 10:4–8 (emphasis added).)" Pet. 35. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶ 83. We credit Dr. Baker's testimony and give it substantial weight. We find that Kim discloses the feature of "wherein a number of delay cells utilized is reduced by approximately one-half."

We have considered the arguments and evidence presented by Petitioner and all of the opposing arguments and evidence presented by Patent Owner. Petitioner establishes that Kim describes all of the limitations in claim 10. For the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 10 is anticipated by Kim.

3. Claim 11

Claim 11 depends from claim 10 and further recites "wherein the phase detector comprises a phase difference detector with a first resolution." Ex. 1001, 4:60–61. Petitioner's analysis for claim 10, as discussed above, already identifies and explain the operation of Kim's phase detector 202 shown in Kim's Figure 3. Petitioner explains that because phase detector 202 determines whether the feedback clock signal leads or lags the

input clock signal, it is a "phase difference detector." Pet. 35. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶ 86.

Petitioner further explains why Kim's phase difference detector 202 has a first resolution:

> [A] person having ordinary skill in the art would have understood that *Kim's* phase detector 202 necessarily has [a first resolution], and that *Kim* inherently discloses [a first resolution]. (*Id.*, ¶ 87.) Such a person would have had that understanding because Kim discloses determining a phase difference as discussed above and because a determination of phase difference must be with respect to some resolution ("first resolution"). (*Id.*) Such a person would have understood that resolution refers to the capability to distinguish one phase from another (e.g., the phase of one input of phase detector 202 from the phase of another input of the phase detector), and that if the phase detector 202 did not have a resolution ("first resolution") then it would have been unable to perform its disclosed function. (*Id.*) In other words, in order for phase detector 202 and the delay locked loop of figure 3 of *Kim* to function properly, phase detector 202 must comprise a phase difference detector that inherently has a "first resolution." (*Id.*)

Pet. 36–37. The explanation is supported by the testimony of Dr. Baker. Ex. 1002 ¶ 87. We credit Dr. Baker's testimony and give it substantial weight. Patent Owner advances the same arguments it has argued with respect to independent claim 10, which we have rejected above. We find that Kim discloses the feature of "wherein the phase detector comprises a phase difference detector with a first resolution."

We agree with Petitioner's assertions and Dr. Baker's supporting testimony, discussed above, that Kim discloses all the limitations of claim 11. Based on the foregoing, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 11 is anticipated by Kim.

4. Claim 13

The preamble of claim 13 recites: "A method for reducing delay line length in a digital delay locked loop (DLL)." Ex. 1001, 4:66–67. We observe that the body of claim 13 does not recite any limitations related to reducing delay line length. Thus, we agree with Petitioner (Pet. 37) that the phrase "for reducing delay line length" merely constitutes an intended field of use for the claimed invention and does not give life, meaning, and vitality to the body of claim 13 to be limiting. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999). Nonetheless, the body of claim 13 recites a "DLL." So we determine that the reference to "DLL" in the preamble necessitates that the steps in the body of the claim must be performed in a delay locked loop. Kim meets this limitation, because Kim discloses a clock signal distribution scheme using a digital delay lock loop. Ex. 1009, 2:46–63 (cited at Pet. 11).

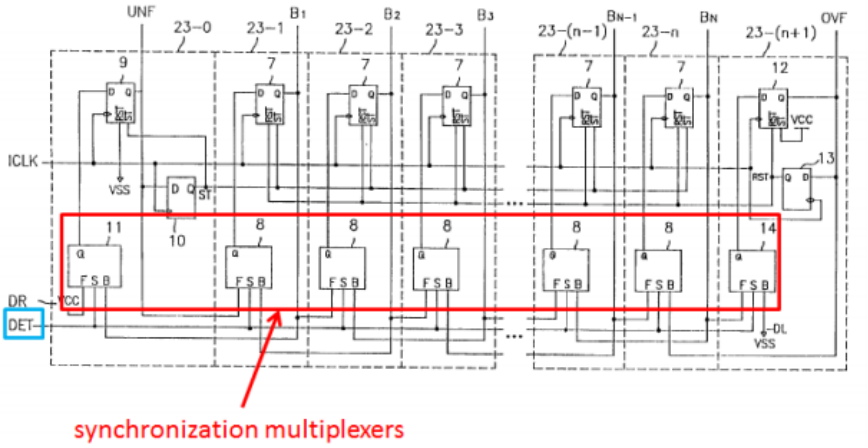
Claim 13 further recites: "determining whether a feedback clock signal in the DLL follows within a 180° phase difference behind an input clock signal." Ex. 1001, 5:1–3. As supported by the Declaration of Dr. Baker, Petitioner establishes that Kim's digital delay locked loop performs this step. Pet. 38–43 (citing Ex. 1002 ¶¶ 89–96). We need not reiterate every detail of the explanation, but make the following observations. With reference to Kim's Figure 3, the input clock signal recited in claim 13 of the '507 patent reads on the system clock signal (SCLK) in Kim, and the feedback clock signal recited in claim 13 of the '507 patent reads on the chip clock signal (CCLK) in Kim. Phase detector 202 receives SCLK and CCLK as inputs and makes a comparison of the two. Ex. 1009, 3:22–44. Phase detector 202 outputs a "1" to the shift

register when it is determined that CCLK leads SCLK, and outputs a "0" to the shift register when CCLK trails SCLK. *Id.* at 5:14–19.

Dr. Baker testifies: "A person of ordinary skill in the art would have understood that if a clock 'lags' another clock in phase, it 'follows within a 180° phase difference behind the other clock.'" Ex. 1002 ¶ 92. Dr. Baker further explains that where CCLK leads the SCLK, that is the equivalent to the CCLK following the SCLK by more than 180°. *Id.* ¶ 95. Dr. Baker's reasoning on this point is consistent with his testimony that one cycle of a periodic signal encompasses 360° in phase and that a lag of so many degrees is the same as a lead that is the difference between 360° and the lag amount. *Id.* ¶ 62. We credit Dr. Baker's testimony and give it substantial weight. We agree with Petitioner's assertion, supported by Dr. Baker's above-noted testimony, that Kim discloses the step of "determining whether a feedback clock signal in the DLL follows within a 180° phase difference behind an input clock signal."

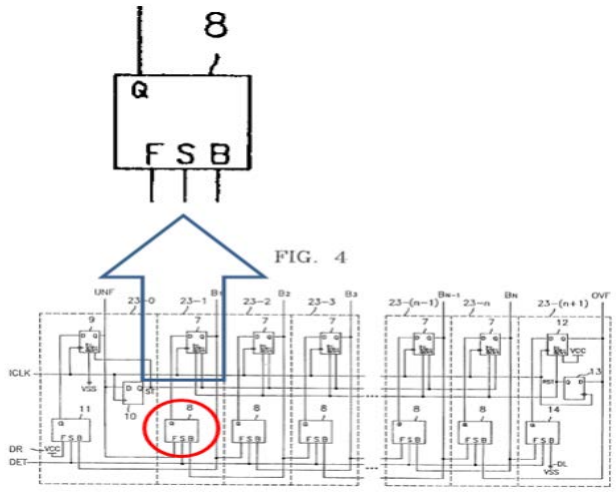
Claim 13 further recites: "selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal with[in] 180°." Ex. 1001, 5:4–7. As explained by Petitioner on pages 44–49 of the Petition, Kim's DLL also performs this step through the synchronization multiplexers within the shift register. Petitioner annotated Figure 4 of Kim to show, specifically, synchronization multiplexers 8, 11, and 14. The annotated Figure 4 on page 45 of the Petition is reproduced below:

FIG. 4



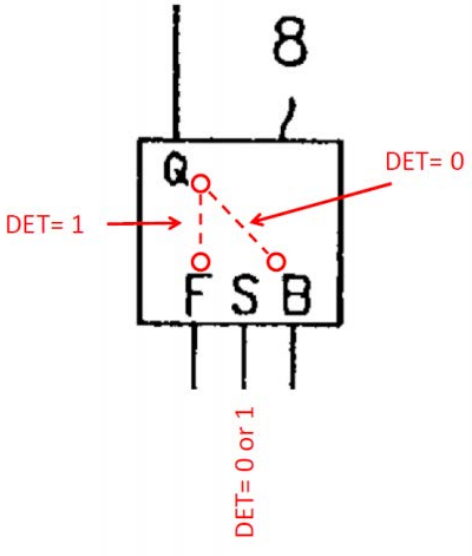
The above figure is a version of Figure 4 of Kim, which has been annotated by Petitioner to identify synchronization multiplexers 8, 11, and 14 within the shift register. Pet. 45. The DET signal is provided by phase detector 202 to the shift register for shifting data bits in the shift register either right or left in accordance with the "0" or "1" value of the DET signal. Ex. 1009, 3:27–29. As Dr. Baker explains, the DET signal is commonly provided to the "S" inputs of all synchronization multiplexers 8, 11, and 14. Ex. 1002 ¶ 98.

A further annotated version of Kim's Figure 4, as it appears on page 46 of the Petition, is reproduced below:



The reproduced figure is an annotated version of Kim's Figure 4, including an enlargement of a representative synchronization multiplexer 8. Petitioner explains: "As further disclosed by Kim, the synchronization multiplexer selects its output (Q) to be either the signal provided to the forward (F) input or the signal provided to the backward (B) input based on the selection (S) input." Pet. 47 (citing Ex. 1009, 5:39–43, 5:51–54, 6:21–25; Ex. 1002 ¶ 101). Dr. Baker explains how the functionality provided by each of Kim's multiplexers is that of a single-pole double throw switch:

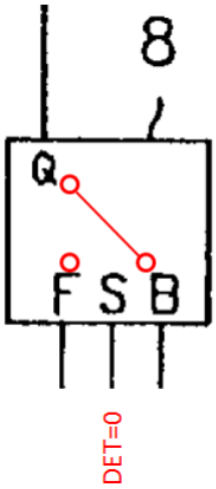
> A person of ordinary skill in the art would have understood that the synchronization multiplexers 8, 11, and 14 each choose one of two inputs (F or B) as the output (Q) based on the selection signal (S). (Ex. 1009 at 5:51–54, 6:21–25.) As such, those multiplexers in *Kim* provide the functionality of a single-pole double throw switch, with two possible states dependent on a control input. (See above at [Ex. 1002 ¶¶ 34–37].) As such, *Kim* discloses selecting a switch position "according to the determining step" (each synchronization multiplexer selects F (forward) or B (backward) based on S (selection)). The demonstrative below helps illustrate this understanding.



(Ex. 1009 at FIG. 4 (excerpted and annotated); *see also* above at [Ex. 1002 ¶¶ 34–37].).

Ex. 1002 ¶ 104. The illustration in Dr. Baker's explanation shows two possible connections, F to Q and B to Q, based on whether signal DET is a "0" or a "1."

Based on the foregoing, Petitioner notes the following and provides the annotated diagram below.

> Thus, *Kim* discloses selecting the switch position shown below, corresponding to connecting the input on B to the output Q ("selecting a first switch position"), when the chip clock signal (CCLK) lags the system clock signal (SCLK) and DET='0' ("when the feedback clock signal follows behind the input clock signal within 180°"). (*See supra* Section IX.A.3(b) [Pet. 38–43]; Ex. 1002 ¶ 105; *see also* Ex. 1002, ¶¶ 34–37 (discussing multiplexers).)
>
> 
>
>
> (Ex. 1002, ¶ 105, citing Ex. 1009, FIG. 4 (excerpted and annotated).)

Pet. 50–51. The annotated diagram shows a first switch position put in place in response to a DET signal value of "0" corresponding to when the feedback clock signal follows behind the input clock signal within 180°. The above reasoning is supported by the evidence cited by Petitioner, e.g., Ex. 1002 ¶ 1005. The switch position connecting B to Q is engaged when DET signal is "0," representing that the feedback clock signal follows behind the input clock signal within 180°. *Id.*

Patent Owner argues

> Kim does not teach "selecting a switch position according to the determining step." In the evidence presented with its petition, Samsung alleges that each of the synchronization multiplexers 8, 11, or 14 shown in Fig. 4 in Kim perform this claim element. Paper 1 (Petition) at 44–53; Ex. 1002 (Baker decl.) at 63–71. These synchronization multiplexers 8, 11, and 14 output only B1–BN signals and UNF and OVF signals, each of which are a binary value (0 or 1) and do not select a non-inverted or inverted input clock signal. Ex. 2002 (Gervasi decl.) at 38–41.

PO Resp. 13.

> [N]one of the synchronization multiplexers in Kim select a non-inverted input clock signal or an inverted clock signal. This is because each synchronization multiplexer simply controls one stage of a standard delay line, as opposed to the switch in the '507 patent which selects either a non-inverted or an inverted clock.

Id. at 14.

> The B1–BN outputs of each synchronization multiplexer indicate to the phase delay unit simply whether the corresponding delay unit should be active or not. Ex. 1009 (Kim) at col. 3:40–57, 6:50–7:6, 8:9–16, 9:17–23; Ex. 2002 (Gervasi decl.) at 34, 35, 41. The phase delay unit performs a corresponding adjustment to the delay applied to the clock. *Id.* This operation indisputably has nothing to do with selection of a non-inverted or inverted input clock signal. *Id.* at 36, 37.
>
> The underflow bit (UNF) and overflow (OVF) bit from two of the synchronization multiplexers also do not select a non-inverted or inverted clock.

Id. at 15. Patent Owner summarily states that "[t]he switches [identified by Petitioner in Kim] do not select a non-inverted or inverted clock, but merely increase or decrease delay by one stage." *Id.* at 14. Patent Owner asserts that "the alleged switch does not select any clock signal." *Id.*

All of Patent Owner's arguments, however, depend on its proposed construction of the claim phrase "selecting a switch position according to the determining step" as meaning "selecting a non-inverted input clock signal or an inverted input clock signal according to the determining step." We have rejected Patent Owner's proposed construction, as discussed above. *See supra* § II.C.2. The claim phrase simply means that a position of the switch is selected according to the determining step. Selection of a clock signal, whether inverted or non-inverted, is not required. Therefore, Patent Owner's arguments are unpersuasive.

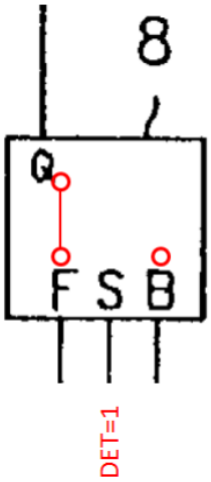
Accordingly, we are persuaded by Petitioner's showings, as summarized in our analysis above, that Kim discloses the step of "selecting a switch position according to the determining step, including selecting a first switch position when the feedback clock signal follows behind the input clock signal with[in] 180°."

We have considered the arguments and evidence presented by Petitioner and all of the opposing arguments and evidence presented by Patent Owner. Petitioner establishes that Kim describes all of the limitations of claim 13. For the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 13 is anticipated by Kim.

5. Claim 15

Claim 15 depends from claim 13 and adds: "wherein selecting further comprises selecting a second switch position when the feedback clock signal does not follow the input clock within 180°." Ex. 1001, 6:1–4. As explained above in the discussion of claim 13, Kim discloses that multiplexer 8 implements the functionality of a single-pole double-throw switch, with two possible states dependent on a single control input. Ex. 1002 ¶ 104 (cited at Pet. 49). A DET signal of "1" triggers the second switch position that

connects F to Q, as is shown below in an annotated diagram appearing on page 53 of the Petition:



The diagram shows a second switch position put in place in response to a DET signal value of "1" corresponding to when the feedback clock signal does not follow the input clock signal within 180°. Ex. 1002 ¶ 108 (cited at Pet. 53). At that switch position, the multiplexer output Q is connected to input F. *Id.* We credit the testimony in Paragraph 108 of Dr. Baker's declaration, as cited by Petitioner (Pet. 53).

Patent Owner puts forth the same arguments it makes for claim 13, i.e., that Kim does not disclose any switch position that selects a clock signal, either non-inverted clock signal or inverted clock signal. The arguments are based on Patent Owner's proposed claim construction, which we have rejected above. *See supra* § II.C.2. Petitioner establishes that Kim describes all of the limitations in claim 15. Based on the foregoing, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 15 is anticipated by Kim.

III. CONCLUSION

Petitioner has established by a preponderance of the evidence that each of claims 10, 11, 13, and 15 is anticipated by Kim under 35 U.S.C. § 102.

IV. ORDER

It is

ORDERED that each of claims 10, 11, 13, and 15 is *unpatentable*; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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