UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

EGENERA, INC.,
Patent Owner.

Case IPR2017-01340
Patent 6,971,044 B2

Before MELISSA A. HAAPALA, *Acting Vice Chief Administrative Patent Judge*, KRISTEN L. DROESCH and CHARLES J. BOUDREAU, *Administrative Patent Judges*.

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141, 142, and 319, and in accordance with 37 C.F.R. § 90.2-90.3, Patent Owner Egenera, Inc. ("Egenera") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered on October 29, 2018 (Paper 33) in IPR2017-1340 and from all orders, decisions, rulings, and opinions underlying or supporting the Final Written Decision. 35 U.S.C. § 141(c). A copy of the Final Written Decision is attached as Exhibit A.

For the limited purpose of providing the Director with the information requested in 37 C.F.R. § 90.2(a)(3)(ii), issues on appeal may include but are not limited to the Board's factual findings and conclusions of law, the Board's determinations of the unpatentability of claims and any finding or determination supporting or relating to such determinations of unpatentability including but not limited to claim construction issues, the applicable claim construction standard, obviousness issues, the scope of the alleged prior art, Board findings that conflict with the evidence of record and are not supported by substantial evidence, as well as all other issues decided adversely to Patent Owner in any orders, decisions, rulings and/or opinions, further including but not limited to: whether the Board erred by failing to consider and address Patent Owner's arguments regarding the scope and interpretation of the alleged prior art; whether the Board erred by failing to consider and address Patent Owner's evidence and arguments concerning earlier

conception, reduction to practice, and priority; whether the Board erred by failing to consider and address Patent Owner's evidence and arguments concerning motivation to combine and how alleged prior art would be combined; whether the Board erred by failing to properly consider expert and fact witness testimony, and whether the Board erred in failing to adequately support its findings concerning obviousness.

Patent Owner Egenera reserves the right to challenge any finding or determination supporting or relating to the issues listed above and to challenge any other issues decided adversely to Patent Owner by the Board in this proceeding.

Simultaneous with this submission, a copy of this Notice of Appeal is being filed with the Patent Trial and Appeal Board and the Clerk's Office for the United States Court of Appeals for the Federal Circuit, along with the required docketing fee for the United States Court of Appeals for the Federal Circuit.

Respectfully submitted,

Dated: December 28, 2018

by: / Christopher Bovenkamp /

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing Patent Owner's Notice of Appeal was filed electronically on this 28th day of December, 2018, with the Director of the United States Patent and Trademark Office, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
Madison Building East, 10B20
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Alexandria, VA 22314-5793

CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing Patent Owner's Notice of Appeal was filed electronically on this 28th day of December, 2018, with the Clerk's Office of the United States Court of Appeals for the Federal Circuit:

United States Court of Appeals for the Federal Circuit
717 Madison Place, N.W., Suite 401
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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing Patent Owner's Notice of Appeal has been served on Petitioner via electronic mail transmission addressed to the person(s) below:

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EXHIBIT A

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Paper 33
Entered: October 29, 2018

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HAAPALA, *Acting Vice Chief Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

Cisco Systems, Inc. ("Petitioner") filed a Petition pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–6 of U.S. Patent No. 6,971,044 B2 ("'044 patent"). Paper 1 ("Pet."). Egenera, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). Applying the standard set forth in 35 U.S.C. § 314(a), we granted Petitioner's request and instituted an *inter partes* review of all challenged claims. Paper 7 ("Dec.").

During the trial, Patent Owner timely filed a Response (Paper 18, "PO Resp."), to which Petitioner timely filed a Reply (Paper 25, "Reply"). An oral hearing was held on July 25, 2018, and a copy of the transcript was entered into the record. Paper 32 ("Tr.").

Additionally, Patent Owner filed a Motion to Exclude Evidence (Paper 29, "Mot. To Exclude"), to which Petitioner filed an Opposition (Paper 31,"Mot. Opp.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of the claims on which we instituted trial. Based on the record before us, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–6 of the '044 patent are unpatentable.

I. BACKGROUND

A. The '044 Patent (Ex. 1001)

The '044 patent describes processing systems having virtualized communication networks and storage for quick deployment and reconfiguration. Ex. 1001, 1:17–19. The platform provides a large pool of processors from which a subset may be selected and configured through software commands to form a virtualized network of computers that may be

deployed to serve a given set of applications or customer. *Id.* at 2:59–64. The virtualization may include virtualization of local area networks (LANs) or the virtualization of I/O storage. *Id.* at 2:67–3:2.

Figure 1 of the '044 patent is reproduced below:

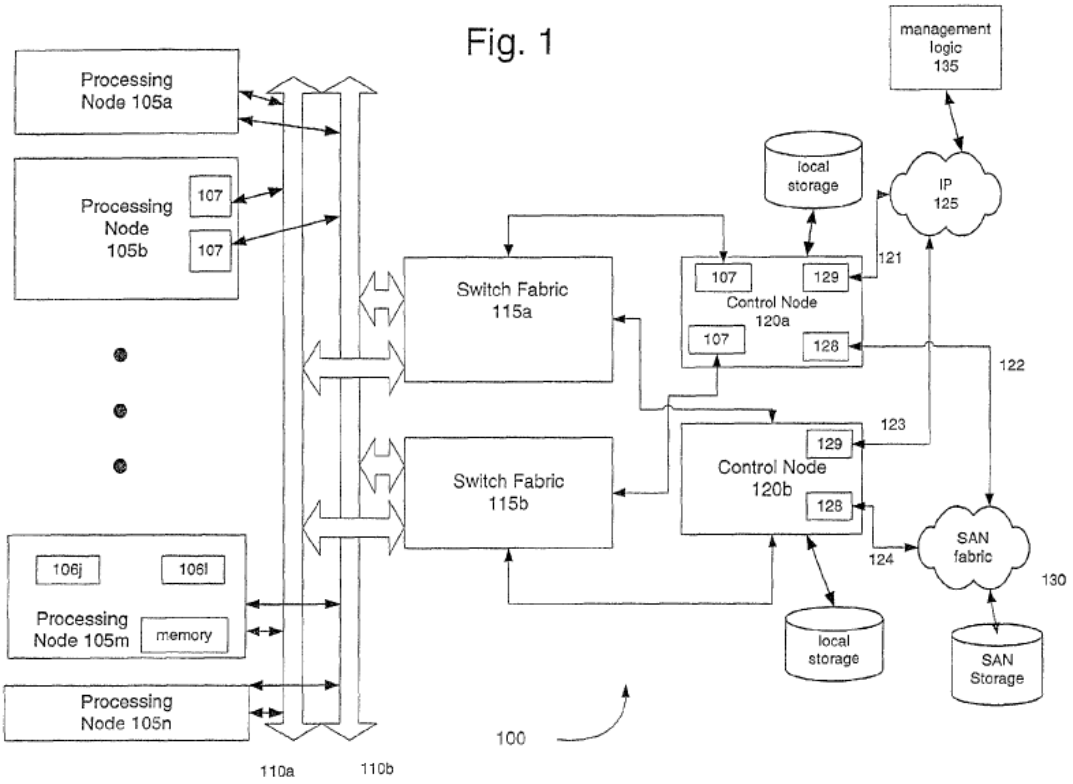

Figure 1 depicts hardware platform 100, which includes processing nodes 105a-105n connected to switch fabrics 115a, 115b via high-speed interconnects 110a, 110b. *Id.* at 3:10–12. Switch fabrics 115a, 115b are also connected to at least one control node 120a, 120b in communication with external Internet Protocol (IP) network 125 and storage area network (SAN) 130. *Id.* at 3:13–16. In some embodiments, processing nodes 105a–105n, control nodes 120a, 120b, and switch fabrics 115a, 115b are contained in a single chassis and interconnected via a fixed, pre-wired mesh of point-to-point (PtP) links. *Id.* at 3:20–24. Figure 1 depicts additional components not described.

Under software control, the platform supports multiple, simultaneous, and independent processing area networks (PANs), which are each configured to have a corresponding subset of processors that may communicate via a virtual local area network emulated over the PtP mesh. *Id.* at 3:65–4:3. An administrator defines the network topology of a PAN and specifies media access control (MAC) address assignments of the various nodes. *Id.* at 6:4–7. The MAC address is virtual, identifying a virtual interface, and is not tied to any specific physical node. *Id.* at 6:7–9. The virtual local area network provides communication among a set of computer processors, but excludes processors not in the defined set. *Id.* at 2:8–11. A virtual storage space is also defined and established with a defined correspondence to the address space of a storage network. *Id.* at 2:11–13.

The ’044 patent further describes that the control node, via software (without any physical re-cabling), may change the PAN configuration to allow a new processor to inherit the storage and networking personality of another. *See id.* at 23:3–7, 28:14–19. This may be done to swap a new processor into a PAN to replace a failing one. *Id.* at 29:19–21. In response to a failure by a computer processor, a computer processor is allocated to replace the failed processor, and the MAC address of the failed processor is assigned to the processor that replaces the failed processor. *Id.* at 2:13–17. The virtual storage space and defined correspondence to the address space of the storage network is also assigned to the processor that replaces the failed processor. *Id.* at 2:17–19. The virtual local area network is then reestablished to include the processor that replaced the failed processor and to exclude the failed processor. *Id.* at 2:19–22.

B. Illustrative Claim

Claims 1 and 4 are independent claims. Claim 1 is illustrative of the subject matter of the claims at issue:

> 1. A platform for computer processing, connectable to an external communication network and a storage network and comprising:
>
> a plurality of computer processors connected to an internal communication network;
>
> configuration logic to define and establish (a) a virtual local area communication network over the internal network, wherein each computer processor in the virtual local area communication network has a corresponding virtual MAC address and the virtual local area network provides communication among a set of computer processors but excludes the processors from the plurality not in the defined set, and (b) a virtual storage space with a defined correspondence to the address space of the storage network; and
>
> failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed processor, the failover logic including logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor, logic to assign the virtual storage space and defined correspondence of the failed processor to the processor that replaces the failed processor, and logic to reestablish the virtual local area network to include the processor that replaces the failed processor and to exclude the failed processor.

C. Instituted Grounds of Unpatentability

Petitioner relies on the following references:

1. U.S. Patent No. 6,779,016, issued Aug. 17, 2004 ("Aziz") (Ex. 1006).
2. U.S. Patent No. 6,856,591, issued Feb. 15, 2005 ("Ma") (Ex. 1007).

3. Thorsten von Eicken & Werner Vogels, *Evolution of the Virtual Interface Architecture*, 10 IEEE COMPUTER 61 (Nov. 1998) ("Von Eicken") (Ex. 1008).

We instituted trial under 35 U.S.C. § 103(a) based on the following combinations of references. Dec. 18.

References	Claims
Aziz and Ma	1, 3, 4, 6
Aziz, Ma, and Von Eicken	2, 5

In support of its contentions, Petitioner submitted a declaration by its witness, Prashant Shenoy, Ph.D. Ex. 1004. In response, Patent Owner submitted a declaration by its witness, H. Jonathan Chao, Ph.D. Ex. 2015. Both witnesses were cross-examined during the trial, and transcripts of their depositions are in the record. Ex. 2017 (Shenoy deposition); Ex. 1035 (Chao deposition).

D. Related Proceedings

Petitioner and Patent Owner identify the following related district court litigation: *Egenera, Inc. v. Cisco Systems, Inc.* (1-16-cv-11613, D. Mass). Pet. 6; Paper 4, 2. Petitioner also filed a petition for *inter partes* review of claims 1–8 of U.S. Patent No. 7,231,430 B2 (IPR2017-01341, Paper 2) (institution denied; Paper 10), which Patent Owner identifies as a related proceeding. Paper 4, 2.

II. ANALYSIS

A. Legal Principles

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of non-obviousness, i.e., secondary considerations such as commercial success, long felt but unsolved needs, and failure of others.[1] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The obviousness inquiry further requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")).

B. Level of Ordinary Skill in the Art

Petitioner asserts a person of ordinary skill in the art is someone knowledgeable and familiar with network computing and that such a person would have (i) a Bachelor's degree in Electrical and/or Computer Engineering, Computer Science, or equivalent training, and (ii) approximately two years of experience working in hardware and/or software design and development relating to network computing. Pet. 13–14. Petitioner asserts lack of work experience can be remedied by additional education, and vice versa. *Id.* at 14. Patent Owner does not provide a level

[1] The record does not include arguments or evidence regarding objective indicia of non-obviousness.

of skill in the art or otherwise contest the level of skill advocated by Petitioner. *See* PO Resp.

We accept the level of skill advocated by Petitioner as it is uncontested and consistent with the prior art of record.

C. Claim Construction

In an *inter partes* review, claims of an unexpired patent are interpreted using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b) (2016); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). Under that standard, "words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016).

1. "virtual local area communication network"

This term appears in independent claims 1 and 4. In our Institution Decision, we construed "virtual local area communication network" as "a local area network of computer processors that is at least in part simulated by software." Dec. 6–8. Petitioner does not object to our construction. Reply 6. Patent Owner states that although it sought a different construction pre-institution, it applies the Board's construction in its Response. PO Resp. 32.

However, Patent Owner seeks clarification as to what it means to "simulate" part of a "local area network" with "software." *Id.* at 33. Patent Owner asserts that in the context of the '044 patent, a person of ordinary skill in the art would understand there are two possible relevant types of virtualization or simulation: (1) using software to configure a network topology with interconnections of specified computers and network

equipment; and (2) using software to implement network equipment itself. *Id.* Patent Owner argues it is the second type that is required by the '044 patent. *Id.* Patent Owner argues the specification makes clear that the defined and established network recited in claims 1 and 4 includes software-implemented network equipment. *Id.* at 33 (citing Ex. 1001, 3:65–4:13, 4:16–28); *see also* Ex. 2015 ¶¶ 76–78 (Dr. Chao's testimony that the claims and specification of the '044 patent require the virtualized or simulated network to include at least some software to implement network equipment).

Petitioner asserts that Patent Owner repackages its pre-institution argument and that the Board correctly rejected Patent Owner's earlier proposed requirement for "the network to be entirely simulated by software." Reply 6–7 (citing Dec. 7). Petitioner further asserts that Dr. Chao's suggestion that the '044 patent disclaimed virtualization involving "configuring VLAN switches" (Ex. 2015 ¶ 75) contradicts the specification, which describes connections in redundant pairs going through one of two switch fabrics 115a,b. *Id.* at 7 (citing Ex. 1001, 11:57–60). Petitioner asserts that, as confirmed by the named co-inventors, switch fabrics 115a,b are physical switches. *Id.* (citing Ex. 1034, 38:14–39:19; Ex. 1033, 34:2–12). Petitioner argues that testimony by the named co-inventor supports the Board's construction, which allows for the use of physical networking equipment by requiring only partial simulation by software. *Id.* at 7–8.

We are not persuaded by Patent Owner's argument that the '044 patent requires a virtual local area communication network to use software to implement network equipment. The portions of the specification cited by Patent Owner disclose that each processing area network (PAN) "is configured to have a corresponding subset of processors 106 that may communicate via a virtual local area network emulated over the PtP mesh"

and that "[u]nder certain preferred embodiments, software logic . . . emulates switched Ethernet semantics." Ex. 1001, 3:67–4:8. The cited portions further disclose "[c]ertain preferred embodiments allow an administrator to build virtual, emulated LANs using virtual components, interfaces, and connections" and that "the virtual networks so created emulate a switched Ethernet network, though the physical, underlying network is a PtP mesh." *Id.* at 4:16–24. Neither Patent Owner, nor Dr. Chao, explain why the cited portions of the specification require the local area communication network to use software to implement network equipment. *See* PO Resp. 32–34; Ex. 2015 ¶¶ 76–78. Nor do we read such a requirement in the specification.

Although certain preferred embodiments may emulate switched Ethernet semantics, the '044 patent does not require software to implement network equipment. Rather, the '044 patent describes the virtual network emulates a switched network through an underlying PtP mesh, which is a physical network that uses switch fabrics 115a,b. *See* Ex. 1001, 3:20–23, 4:22–24; *see also* Dec. 7 ("[T]he '044 patent describes the virtual local area network is emulated over a PtP mesh (physical network) and thus, there is a physical component to the network."). We agree with Petitioner that the testimony of the '044 patent's co-inventors, Peter Manca and Scott Geng, confirms the fact that switch fabrics 115a,b are physical switches. *See* Ex. 1034, 39:4–19 (Mr. Manca's testimony that the switch fabrics described in column 3, around line 50, are physical components); Ex. 1033, 34:2–12 (Mr. Geng's testimony that "there was connectivity between the Giganet card on the application node and the actual switch itself -- two switches, one connection to each switch"). Because the '044 patent describes the virtual local area communication network uses an underlying physical switch network, we do not agree with Patent Owner that the virtualization software

must implement network equipment itself or that the '044 patent excludes using software to configure a network topology with interconnections of specified computers and network equipment (type 1).

On the complete record, we maintain our construction of "virtual local area communication network" to be "a local area network of computer processors that is at least in part simulated by software." Our construction does not require the use of software to implement network equipment.

2. "computer processor"

This term appears in independent claims 1 and 4. Patent Owner asserts the issue as to this term is whether computer processors may be located on the control node or whether they must be separate from the control node. PO Resp. 34. Patent Owner asserts that the latter is the only reasonable reading of the term. *Id.*

Petitioner asserts we should reject Patent Owner's construction because the claims do not recite a "control node" and it would be improper to read such a limitation into the claims. Reply 8. Petitioner further asserts Patent Owner does not identify any issue relating to the construction of "computer processor," so the term is not in dispute and does not require construction. *Id.*

As noted by Petitioner, the claims do not recite a "control node" limitation; accordingly, we disagree with Patent Owner that there is any issue as to whether the recited "computer processors" reside on an element not set forth in the claim. Rather, we agree with Petitioner that Patent Owner does not identify any issue relating to the proffered construction of "computer processor." *See* PO Resp. 34. To the extent Patent Owner intends its arguments to apply to distinguishing the recited "computer processors" from the recited "configuration logic," Patent Owner does not

include any arguments in its Response that the asserted prior art fails to disclose a computer processor separate from configuration logic. *See id*. Accordingly, we do not find it necessary to construe this term. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (explaining that "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy").

3. *Other terms*

Petitioner proposes a construction for "personality," which appears in claims 3 and 6. Pet. 12. Patent Owner does not address Petitioner's construction. *See* PO Resp.

Patent Owner proposes a construction for "responsive to a failure of a computer processor" / "in response to a failure by a computer processor," which appear in claims 1 and 4, respectively. *See id.* at 30–32. Petitioner has not stated any objection to Patent Owner's construction.

Because these terms are not in controversy, we determine that we need not explicitly construe these terms to resolve the issues before us. *See Vivid Techs.,* 200 F.3d at 803.

D. Obviousness over Aziz and Ma

Petitioner challenges claims 1, 3, 4, and 6 as obvious under 35 U.S.C. § 103(a) over Aziz and Ma. Pet. 22–61.

1. Scope and Content of Aziz

Aziz describes an extensible computing system based on a wide scale computing fabric ("computing grid"). Ex. 1006, 4:13–14, 4:24–25. The computing grid is physically constructed once, and then logically divided up for various organizations on demand. *Id.* at 4:25–27. Each organization's logical portion of the computing grid is referred to as a Virtual Server Farm (VSF), which can change dynamically in terms of numbers of central

processing units (CPUs), storage capacity, and disk and network bandwidth. *Id.* at 4:29–35.

Figure 2 of Aziz is reproduced below:

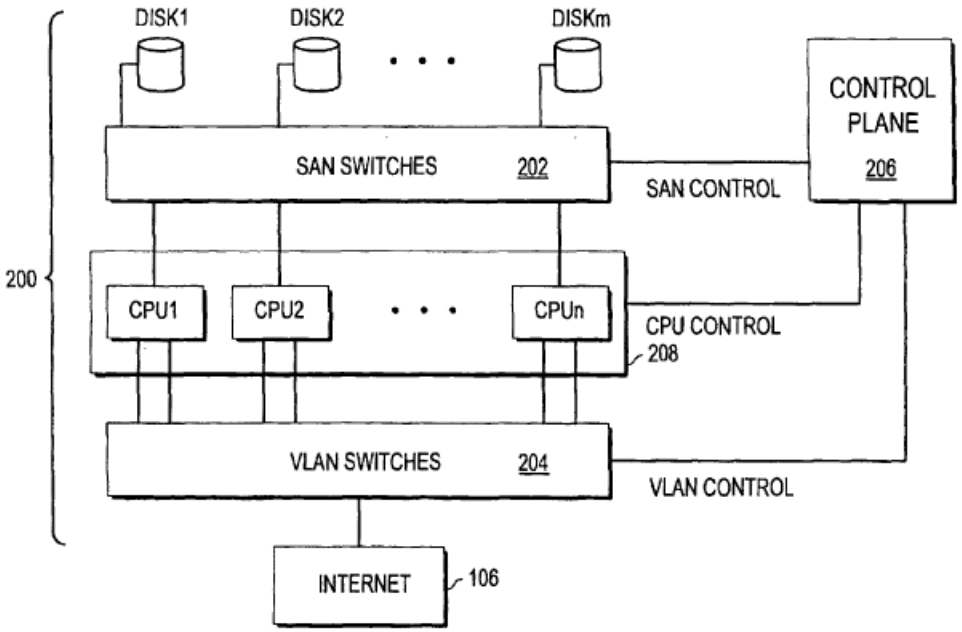

Fig. 2

Figure 2 is a block diagram of one configuration of extensible computing system 200. *Id.* at 5:47–48. Extensible computing system 200 includes local computing grid 208, which is composed of a large number of computing elements (CPU1, CPU2, . . . CPUn). *Id.* at 5:52–54. The computing elements do not store long-lived state information, but instead state information is stored separately on disks (DISK1, DISK2, . . . DISKn) that are coupled to computing elements CPU1–CPUn via a Storage Area Network (SAN) comprising one or more SAN switches 202. *Id.* at 5:56–5:63. All of the computing elements are interconnected to each other through one or more VLAN switches 204, which can be divided up into Virtual Local Area Networks (VLANs). *Id.* at 5:66–6:1. VLAN switches

204 are coupled to Internet 106. *Id.* at 6:1–6:2. Control Plane 206 is coupled by SAN Control path, CPU Control path, and VLAN Control path to SAN switches 202, CPU1–CPUn, and VLAN switches 204, respectively. *Id.* at 6:13–16.

Aziz describes that configuration and control of the computing elements and their associated networking and storage elements is performed by the control plane. *Id.* at 4:54–59. For example, the control plane may configure a VLAN switch to place ports that are each coupled to a computing element on an indicated VLAN. *See id.* at Fig. 5A, 10:1–3. The control plane may similarly configure a SAN switch to place ports that are each coupled to a disk on a specified SAN zone. *See id.* at Fig. 5A, 10:3–5.

Aziz further describes that the computing grid may include an Idle Pool that comprises a large number of computing elements that are kept in reserve. *Id.* at 7:6–8. Computing elements from the Idle Pool may be assigned to a particular VSF to increase CPU or memory capacity, or to deal with failure of a particular computing element in a VSF. *Id.* at 7:8–12. In moving a computing element from the Idle Pool into a VSF (or vice-versa), the control plane configures LAN switches and SAN switches associated with a computing element to be part of the VLAN and SAN zones associated with a particular VSF (or the Idle Pool). *See id.* at 7:31–55.

2. Scope and Content of Ma

Ma describes providing high reliability to management of a cluster of network devices, such as switches, bridges, and routers. Ex. 1007, 1:9–11, 1:20–21. The cluster includes a command network device, with a commander internet protocol (IP) address and a commander media access control (MAC) address. *Id.* at 3:61–63. A virtual IP address and a virtual MAC address are assigned to an "active commander" (command network

device with the highest priority) and the active commander uses the virtual IP address and the virtual MAC address as its source IP and MAC addresses, respectively, instead of its own IP address and MAC address. *See id.* at 6:61–7:7. If the active commander fails, a standby commander takes over the active commander role, and ownership of the virtual IP address and the virtual MAC address is transferred to the new active commander device. *See id.* at 7:24–32, 12:18–25.

3. Prior Art Status of Ma

Patent Owner contends that Ma is not prior art to the '044 patent because the claimed invention was conceived of before the earliest claimed priority date for Ma and thereafter diligently reduced to practice. PO Resp. 36.

In an *inter partes* review, the burden of persuasion is on the petitioner to prove "unpatentability by a preponderance of the evidence," 35 U.S.C. § 316(e), and that burden never shifts to the patentee. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). A petitioner also has the initial burden of production, or the burden of going forward with evidence. *Id.* at 1379. Petitioner met its initial burden of production by offering Ma into evidence and arguing that Ma is prior art under 35 U.S.C. § 102(e) to the '044 patent. *See* Pet. 13. The burden of production then shifted to Patent Owner to produce evidence supporting a date of invention before Ma. *See Dynamic Drinkware*, 800 F.3d at 1379–80; *Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1576–77 (Fed. Cir. 1996).

In order to show prior invention, Patent Owner must either prove: (1) a conception and reduction to practice before the filing date of Ma; or (2) a conception before the filing date of Ma combined with diligence and reduction to practice after that date. *See REG Synthetic Fuels, LLC v. Neste*

Oil Oyj, 841 F.3d 954, 958 (Fed. Cir. 2016) (citing *Taurus IP, LLC v. DaimlerChrysler Corp.*, 726 F.3d 1306, 1323 (Fed. Cir. 2013)). Both parties agree that Ma is entitled to its December 15, 2000, filing date. Pet. 13; PO Resp. 36; *see also* Ex. 1007, (22) (indicating the filed date as December 15, 2000). Thus, under either approach, Patent Owner must establish that conception occurred prior to December 15, 2000.

a. Conception

Conception is "the formation, in the mind of the inventor of a *definite and permanent idea of the complete and operative invention, as it is thereafter to be applied in practice*." *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985) (emphasis in original) (quoting *Gunter v. Stream*, 573 F.2d 77, 80 (C.C.P.A. 1978)). A party claiming conception must show possession of every feature or limitation of the claimed invention. *Davis v. Reddy*, 620 F.2d 885, 889 (C.C.P.A. 1980). "Conception must be proved by corroborating evidence which shows that the inventor disclosed to others his 'completed thought expressed in such clear terms as to enable those skilled in the art' to make the invention." *Coleman*, 754 F.2d at 359 (quoting *Field v. Knowles*, 183 F.2d 593, 601 (C.C.P.A. 1950)). An inventor's testimony, standing alone, is insufficient to prove conception—some form of corroboration must be shown. *Price v. Symsek*, 988 F.2d 1187, 1194 (Fed. Cir. 1993); *see also Mahurkar*, 79 F.3d at 1577 (Fed. Cir. 1996) (corroboration requirement "arose out of a concern that inventors testifying in patent infringement cases would be tempted to remember facts favorable to their case by the lure of protecting their patent or defeating another's patent").

Patent Owner asserts that the subject matter of the claims of the '044 patent was conceived of by November 7, 2000. PO Resp. 5. Patent Owner

states that this is evidenced by internal Egenera documents from mid-to-late 2000 related to Egenera's Interframe (later called Bladeframe). *Id.* at 5–6 (citing Exs. 2009, 2010, 2012, 2013, 2022, 2024). In support of its assertions, Patent Owner provides a chart summarizing where the subject matter of the limitations of each claim of the '044 patent is found in the internal Egenera documents and cites to testimony of Dr. Chao (Ex. 2015) and Mr. Geng (Ex. 2008). PO Resp. 7–24.

Petitioner argues that Patent Owner does not establish conception of "failover logic including logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor," as recited in claim 1, prior to Ma's filing date. Reply 11–13. Petitioner asserts that, at best, the cited sections describe "simulated MAC addresses" and that "spare Application Processors can be configured as standby nodes, and can be rapidly booted with the same software configuration as an existing node," but that neither description corroborates the specific language in the "failover logic" limitation. Reply 12 (citing PO Resp. 11–12, 16). Petitioner further asserts that there is no evidence a "simulated MAC address" would be included in the "software configuration" booted on a standby node, but rather the evidence indicates that a MAC address would not be reassigned from one node to another, since each node's virtual MAC address includes its own "node number." *Id.* at 12–13 (citing PO Resp. 12 (quoting Ex. 2012, 6)); Ex. 2013, 11–12); *see also* Tr. 5 ("[Ex. 2012] says the simulated-MAC address 'will include the node number.' So, the node number, the number of a node, is particular to a MAC address for that node.").

As evidence of conception of "failover logic including logic to assign the virtual MAC address of the failed processor to the processor that

replaces the failed processor" by November 7, 2000, Patent Owner asserts that

> Egenera's Interframe platform included "failover logic," . . . which when a processing blade/node failed, caused another blade/node to replace it, which included taking on the failed blade/node configuration/resources. As discussed in [1c], *supra*, this configuration includes virtual MAC addresses. Failover logic evidence is included in [1f], *supra*. Exemplary evidence is cited below.

PO Resp. 19 (citing Exs. 2008 ¶¶ 14–33, 2009–2014, and 2022–2024). In the cited evidence, Mr. Geng testifies the "N+1 Blade fail over capability for entire Frame" mentioned in the Egenera Product Roadmap "allowed for any number of running servers to utilize a single spare compute node to replace any of the active compute nodes in case of failure." Ex. 2008 ¶¶ 15, 16 (citing Ex. 2011, 9). Mr. Geng further testifies "[t]he newly booted server running on the new compute node maintained the same network and storage personality (including the network MAC address) as the previously failed node." *Id.* ¶ 16; *see also id.* ¶ 18 ("[T]he N+1 BladeFrame failover caused the server definition—including virtual interfaces with their MAC addresses, storage, and other aspects of the personality—to automatically be moved to a new processing node, which would then replace the failed node.").

Patent Owner also cites to testimony of Dr. Chao as evidence of conception of the limitation at issue. PO Resp. 19 (citing Ex. 2015 ¶¶ 116–119). Dr. Chao testifies that

> The Egenera documents support this limitation because they teach and discuss failover logic in the Interframe platform, including software on the Interframe Controller, which is able to respond to the failure of computer processors . . . by providing the replacement computer processor with the virtual, or simulated MAC address that had been used by the failed processor.

> . . .
>
> [U]pon failure Interframe software automatically allocates configurations from the failed computer processor to another computer processor.
>
> . . .
>
> [A] person of ordinary skill in the art would understand that the re-allocated configuration would include the virtual, or simulated MAC addresses.

Ex. 2015 ¶¶ 116–118.

Finally, as further evidence supporting conception antedating the Ma reference, Patent Owner points to "evidence cited in [1c] and [1f], *supra*." PO Resp. 19. The identified sections discuss the conception of "wherein each computer processor in the virtual local area communication network has a corresponding virtual MAC address" (limitation 1c) and "failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed processor" (limitation 1f). *Id.* at 11–13 (discussing conception of limitation 1c), 15–19 (discussing conception of limitation 1f).

Upon review of the evidence, we determine that Patent Owner has provided insufficient corroborating evidence to prove that the inventors of the '044 patent conceived of failover logic "to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor" by December 15, 2000. Although Mr. Geng testifies the Egenera Product Roadmap includes the claimed feature (Ex. 2008 ¶¶ 15, 16, 18), the only corroborating evidence cited by Mr. Geng merely states that the Egenera Product Roadmap includes "High Availability" functionality that has "N+1" Blade fail over capability for entire Frame." *See* Ex. 2011, 9. Such evidence is insufficient to corroborate conception of failover logic that

assigns the virtual MAC address of the failed processor to the replacement processor. Dr. Chao's testimony that a person of ordinary skill would understand the re-allocated configuration would include the virtual, or simulated, MAC addresses is also not supported by evidence; therefore, it is entitled to little weight. *See* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Turning to Patent Owner's citations to Exs. 2009–2014 and 2022–2024 as support for conception of the limitation at issue, Patent Owner fails to provide any explanation of the significance of the evidence as required by our rules. *See* 37 C.F.R. §§ 42.22(a)(2) (requiring that motions include "a detailed explanation of the significance of the evidence"), 42.23(a) (oppositions must comply with the content requirements for motions), 42.120 (a patent owner response is filed as an opposition). We decline to assume the role of archaeologist to determine how the cited Exhibits support Patent Owner's position.

The evidence cited in Patent Owner's discussion of limitations 1c and 1f also fails to support conception of failover logic that assigns the virtual MAC address of the failed processor to the replacement processor. As evidence of conception for these limitations, Patent Owner asserts Egenera's Interframe platform included the use of virtual MAC addresses and that processing blades/nodes may be given simulated or virtual MAC addresses through node configuration. PO Resp. 11–12 (citing Ex. 2012, 6; Ex. 2013, 11–12). Patent Owner further asserts the Interframe Platform included "failover logic . . . which was responsive to a failure of a blade/node, including by allocating another blade/node to replace it." *Id.* at 15–19 (citing e.g., Ex. 2009, 2). The cited evidence states

> [t]he use of multiple nodes provides redundancy and application availability in the event a hardware or software malfunction causes a single node to become unavailable. In this event, spare Application Processors can be configured as standby nodes, and can be rapidly booted with the same software configuration as an existing node.

Ex. 2009, 2. We agree with Petitioner that this passage discussing application availability does not show the "software configuration" booted on the standby node includes a virtual MAC address (a network configuration) of the failed processor. *See* Reply 12. We further agree with Petitioner (*id.* at 12–13) that the cited evidence instead indicates a MAC address would not be reassigned from one node because each node's virtual MAC address includes its own "node number." *See id.* at 12–13; PO Resp. 12 (quoting Ex. 2012, 6); Ex. 2012, 6 ("The format of a simulated MAC address is (to be specified, but **will include the node number**, a Virtual Interface connection number, and a special code reserved by the IETF for designating private MACs).") (emphasis added); *see also* Ex. 2013, 12 ("Thus, the default MAC for each virtual network driver will be its own cabinet/port/VI number.").

We determine Mr. Geng's testimony that the failover logic includes "logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor" is uncorroborated and insufficient to prove conception. *See Price*, 988 F.2d at 1194. Accordingly, we determine Patent Owner fails to prove conception prior to December 15, 2000, of the "failover logic" recited in claim 1 and its dependent claims 2 and 3 by virtue of their dependency.

Patent Owner relies on its analysis of claim 1 for corresponding limitations set forth in independent claim 4. PO Resp. 23–24. For the same

reasons discussed above, we agree with Petitioner that Patent Owner does not prove conception prior to December 15, 2000, of "in response to a failure by a computer processor . . . assigning the MAC address of the failed processor to the processor that replaces the failed processor," as recited in claim 4 and its dependent claims 5 and 6 by virtue of their dependency.[2] *See* Reply 13.

For the foregoing reasons, we determine Patent Owner does not establish the inventors conceived the invention of the challenged claims prior to December 15, 2000.

b. Diligent Reduction to Practice

Patent Owner asserts that following conception, the inventors worked diligently to reduce the invention to practice. PO Resp. 25, 37–38. Our determination that Patent Owner has not established conception of the challenged claims prior to December 15, 2000, is dispositive as to the determination that Ma is prior art to the challenged claims under 35 U.S.C. § 102(e). However, we also note that, for the reasons that follow, Patent Owner does not establish diligent reduction to practice.

Patent Owner asserts that Egenera filed provisional application 60/285,296 ("the '296 provisional application") on April 21, 2001, and that "[b]etween November 7, 2000 and April 21, 2001, and into January 2002—when Egenera filed the non-provisional patent application that led to the '044 patent—Egenera worked on implementing the inventions in the '044

[2] Petitioner also argues that Patent Owner does not establish conception of the "configuration logic" recited in claims 1 and 4. Reply 11, 13. Because we determine Patent Owner does not establish conception of the "failover logic" / "in response to failover by a computer processor" limitations set forth in claims 1 and 4, respectively, we decline to also determine whether Patent Owner establishes conception of the recited "configuration logic."

patent." *Id.* (citing Ex. 2003 ¶¶ 24–26; Ex. 2008 ¶¶ 10–33). Patent Owner asserts that documentation of that work is shown in the weekly status updates and lab notebook entries of Egenera's then Vice President of Software Engineering. *Id.* (citing Ex. 2003 ¶¶ 12–22; Exs. 2004–2007).

Petitioner asserts that Patent Owner fails to show diligence during the critical period from before Ma's filing date (December 15, 2000) to the '044 patent's filing date (January 4, 2002). Reply 14–17. Petitioner argues that Patent Owner fails to explain how its documentation corroborates diligence as to the specific features recited in the claims and that Mr. Manca's notebooks are unwitnessed and have no corroborative value themselves. *Id.* at 15–16. Petitioner asserts that the named inventors confirmed in deposition that the provided evidence relates to overall product development efforts and is not specific to the '044 patent claims. *Id.* at 17. Petitioner further asserts that Mr. Geng's declaration indicates the named inventors stopped working on the "failover idea" at some point during 2001, thus neglecting the requirement for diligence through January 4, 2002. *Id.* at 16–17.

To antedate a reference, a patent owner must show reasonable diligence throughout the entire critical period, which begins just prior to the competing reference's effective date and ends on the date of the invention's reduction to practice. *Perfect Surgical Techniques, Inc. v. Olympus Am., Inc.*, 841 F.3d 1004, 1007 (Fed. Cir. 2016). To satisfy the reasonable diligence requirement, "the work relied on must ordinarily be directly related to reduction to practice of the invention." *Naber v. Cricchi*, 567 F.2d 382, 385 (CCPA 1977). An inventor's testimony regarding his reasonable diligence must be corroborated by evidence. *Perfect Surgical*, 841 F.3d at

1007. Corroboratory evidence must be specific both to facts and to dates. *See Gould v. Schawlow*, 363 F.2d 908, 920 (CCPA 1966).

After consideration of the evidence, we agree with Petitioner that Patent Owner does not establish reasonable diligence from the inventors' purported conception of the invention to their constructive reduction to practice. Patent Owner does not set forth a specific date of the inventors' constructive reduction to practice, but rather appears to be relying on both the filing date of the '296 provisional application (April 21, 2001) and the filing date of the '044 patent (January 4, 2002). *See* PO Resp. 25. Even assuming the challenged claims are entitled to the priority date of the '296 provisional application (an issue on which we do not have arguments or evidence), Patent Owner fails to establish reasonable diligence from just before December 15, 2000 (Ma's filing date) to the critical date of April 21, 2001.

Patent Owner cites to testimony of Mr. Geng that the failover idea was conceived of by the date of the Egenera Product Roadmap and that during the late 2000 time period and into 2001 the engineering team worked to implement the idea. *See* Ex. 2008 ¶ 26; *see also* Ex. 2011 ("Egenera Product Roadmap"; dated August 5, 2000). However, we note that Mr. Geng asserts diligence only "into 2001" and does not specifically assert diligence through April 21, 2001. Mr. Manca testifies that between November 7, 2000, and January 4, 2002, Egenera and its employees had a nearly singular focus on implementing the inventions disclosed in the meeting notes and lab notebooks. Ex. 2003 ¶¶ 21–24. But, there is no explanation of how the cited documents corroborate diligence with evidence that is specific both to facts and dates that the engineering team worked on the claimed features of the '044 patent during the critical time. Rather, Mr.

Manca testifies that the meeting minutes and lab notebooks "talk about almost everything we did from an engineering point of view at that given time," which involved more than just the invention disclosed in the '044 patent. Ex. 1034, 10:9–17, 11:3–10. Such evidence is insufficient to demonstrate the work relied on is directly related to reduction to practice of the invention and to corroborate the testimony of the inventors with evidence that is specific both to facts and to dates. *See Naber*, 567 F.2d at 385–86; *Gould*, 363 F.2d 920. Because Patent Owner does not show conception before the filing date of Ma combined with diligence in reduction to practice, we determine Ma is prior art to the '044 patent. Accordingly, we address below Petitioner's challenge based on Ma.

4. Claim 1

Petitioner contends the combination of Aziz and Ma teaches the limitations recited in independent claim 1. Pet. 30–55. In support of its arguments, Petitioner relies on the testimony of Dr. Shenoy. *See id.* (citing Ex. 1004).

a. "A platform for computer processing, connectable to an external communication network and a storage network and comprising:"

Petitioner contends Aziz discloses this limitation. Pet. 30–33. In particular, Petitioner asserts Aziz teaches a platform for providing "computing power" that includes a flexible and scalable computing grid that is composed of a large number of CPU elements and control plane 206. *Id.* at 30 (citing Ex. 1006, Fig. 2, 5:47–56). Petitioner asserts that Aziz's platform is connected to the Internet (external communication network) and to a storage area network. *See id.* at 31–33. We agree with Petitioner's analysis that Aziz discloses this limitation through its description of

extensible computing system 200 (platform) that includes computing grid 208 and control plane 206 coupled through VLAN switches 204 to Internet 106 (external network) and further coupled to Storage Area Network (SAN) comprising one or more SAN Switches 202. *See* Ex. 1006, Fig. 2, 5:47–6:4. Patent Owner has not raised arguments against this limitation in its Patent Owner Response; therefore, any such arguments are waived. *See Novartis AG v. Torrent Pharm. Ltd.*, 835 F.3d 1316, 1330 (Fed. Cir. 2017); *In re Nuvasive*, 842 F.3d 1376, 1381 (Fed. Cir. 2016).[3]

b. "a plurality of computer processors connected to an internal communication network;"

Petitioner asserts Aziz discloses this limitation because it teaches that computing grid 208 is composed of a large number of computing elements that are interconnected to each other through one or more VLAN switches (internal communication network). Pet. 33–34. We agree with Petitioner's analysis that Aziz discloses this limitation through its description of computing elements CPU1 . . . CPUn (computer processors) that are connected to VLAN switches which can be divided up into Virtual LANs (internal communication network). *See* Ex. 1006, 5:52–54, 5:66–6:1. Patent Owner does not present an argument for this limitation.

c. "configuration logic to define and establish (a) a virtual local area communication network over the internal network,"

Petitioner contends Aziz discloses this limitation through its description of a software-implemented control plane (configuration logic) that defines and establishes a VLAN over the VLAN switches. Pet. 35–39.

[3] As in *Nuvasive*, the Scheduling Order in this proceeding cautioned Patent Owner that "any arguments for patentability not raised in the response will be deemed waived." Paper 8, 6.

Petitioner asserts that because Aziz teaches the VLAN switches of Aziz's internal communication network are divided into VLANs, a person of ordinary skill in the art would have recognized that the VLANs are "over the internal network." *Id.* at 36. Petitioner asserts that Aziz teaches its Virtual LANs are local area communication networks because Aziz describes a computing element that is a member of VLANs can access CPUs, SAN storage devices, and NAS devices associated with the VLANs. *Id.* Petitioner asserts Aziz discloses the control plane is used to define and establish a VLAN (local area communication network). *Id.* at 37–39.

Patent Owner contends that Petitioner does not show Aziz discloses a virtual local area communication network that uses "software to implement network equipment itself," which Patent Owner contends is required under the appropriate reading of the term. PO Resp. 60–64. Patent Owner asserts that despite the similarity in name, the VLANs referenced in Aziz refer to different technology than that claimed in the '044 patent and that Aziz's VLANs are physically-defined computing elements (i.e., processors) networked with physical VLAN switches through physical network interfaces. *Id.* at 61–62. Patent Owner asserts that Petitioner, at best, only shows the virtualization that uses software to control, not simulate, computing elements and physical connections. *Id.* at 65.

Petitioner responds that Aziz teaches a "virtual local area communication network" in accordance with our construction of the term ("a local area network of computer processors that is at least in part simulated by software"). Reply 32. Petitioner asserts that Patent Owner does not dispute Aziz's teachings under the Board's construction. *Id.*

We are persuaded Petitioner establishes, by a preponderance of the evidence, that Aziz teaches "configuration logic to define and establish (a) a

virtual local area communication network over the internal network," as recited in claim 1. As discussed above, we are not persuaded by Patent Owner's arguments that the proper construction of "virtual local area communication network" requires the use of software to implement network equipment. We agree with Petitioner that Aziz's control plane meets the configuration logic limitation and that Aziz'z VLANs meet the "virtual local area communication network" limitation as we construe the term—namely, "a local area network of computer processors that is at least in part simulated by software." Aziz describes that under program control, the supervisory mechanism (control plane) dynamically configures VLAN switches and SAN switches to couple their ports to one or more computing elements (e.g., placing ports v1 and v2, coupled to computer elements A, B, C, on VLAN2). Ex. 1006, Fig. 5A, 3:18–21, 10:2–3. Aziz describes that its computing grid is physically constructed once, and then logically divided up into VLANs on demand, without changing the underlying cabling. *See id.* at 3:5–21. Because the local area network of computer processors (VLAN) is established by dynamic configuration, without changing the underlying cable, the VLAN is at least in part simulated by software. We note Patent Owner acknowledges that a person of ordinary skill in the art would understand "a virtual local area communication network" might include this type of virtualization of using software to configure a network topology. *See* PO Resp. 32, 60. In sum, Patent Owner's arguments that the VLANs described in Aziz are not "virtual local area communication networks" are not persuasive because they rely on an added requirement to our construction (the use of software to implement network equipment), which we do not adopt.

d. "wherein each computer processor in the virtual local area network has a corresponding virtual MAC address and"

Petitioner relies on the combined teachings of Aziz and Ma to meet this limitation. Pet. 39–41. Petitioner asserts Aziz teaches computing elements interconnected to each other that can be divided up into Virtual LANs (virtual local area communication network). *Id.* at 39–40. Petitioner asserts that Ma similarly describes a group of network devices (cluster) that all belong to a VLAN and that "cluster configuration information may include . . . a MAC address of each member network device." *Id.* at 40 (quoting Ex. 1007, 11:59–62).

Petitioner further asserts that Ma teaches a member of the cluster may use a virtual MAC address as its source MAC address instead of its own MAC address and that each member of Ma's VLAN has a MAC address used to communicate with other members of the VLAN. *Id.* Petitioner asserts it would have been obvious to a person of ordinary skill in the art to assign each of Aziz's computing elements in a VLAN a virtual MAC address as taught by Ma. *Id.* Petitioner provides reasons why one of skill in the art would have combined the references in the proposed manner (*see id.* at 26–29, 40–41), which we discuss below in reference to the "failover logic including logic to assign the virtual MAC address" limitation (Section II.d.4.g).

Patent Owner asserts that even if Ma were to be combined with Aziz, the combination would not render obvious the claimed "virtual MAC addresses" for "computer processors." PO Resp. 41–52. Patent Owner argues that Ma's "virtual MAC address" teachings relate to specific types of "network devices" (switches, bridges, and routers) and are distinct from the claimed "computer processors." *Id.* at 42–43, 48–49; *see also* Tr. 27

(asserting Ma's virtual MAC addresses are in the context of network devices, not the claimed computer processors). Patent Owner asserts that both Petitioner and its expert fail to address how Ma's teachings related to "network devices" apply to the claimed "computer processors" or to Aziz's "computing elements." *Id.* at 43–47. Patent Owner asserts a person of ordinary skill in the art would not apply Ma's virtual MAC address teachings to Aziz's computing elements in order to re-create the '044 patent's use of virtual addresses for computer processors. *See id.* at 50–52. According to Patent Owner, applying Ma to Aziz would, at best, have applied Ma's commander/standby switch model (with single virtual MAC address for the entire group) to Aziz's SAN switches or VLAN switches. *See id.* at 50–52.

Petitioner responds that Ma's examples of "network devices" that include "switches, bridges, and routers" are non-limiting and that Ma confirms this by referring to "hosts or other network devices on each LAN switch," which shows that a "host" is also a network device. Reply 22 (citing Ex. 1007, 1:20–22, 2:28–31); *see also* Tr. 9 ("Ma refers to "hosts or other network devices" plainly indicating that that hosts are also within the concepts of network devices."). Petitioner asserts that Dr. Chao agreed in his deposition testimony that a virtual MAC address could be assigned to a host. Reply 23 (citing Ex. 1035, 54:4–10). Petitioner argues that Ma's teachings regarding "a virtual MAC address" for a network device are applicable to Aziz's computing elements for multiple reasons. *Id.* at 24–25.

We are persuaded Petitioner establishes the combination of Ma and Aziz teaches "each computer processor in the virtual local area network has a corresponding virtual MAC address." For the reasons discussed previously, we agree with Petitioner that Aziz discloses computer processors

in a virtual local area network (VLAN). *See* Ex. 1006, Figs. 5A, 3:5–21, 5:52–54, 5:66–6:1. We further agree Ma teaches a network device (active commander) that uses a virtual MAC address to communicate. *See* Ex. 1007, 7:3–12. It is not necessary for us to determine whether Ma also teaches its network device is a host (computer device), because Petitioner relies on Aziz to teach the recited computer processor. *See* Pet. 39–40. Although Patent Owner asserts Ma's network devices are different from Azis's computer elements, Patent Owner does not provide any argument that the virtual MAC addresses taught by Ma cannot be assigned to Aziz's computing elements as in Petitioner's proposed combination. Indeed, Patent Owner's expert, Dr. Chao, admits that there is no reason why one couldn't assign a virtual MAC address to a host. Ex. 1035, 54:4–10; *see also id.* at 52:3–4 (Dr. Chao's testimony that a computer or a server is a host); *id.* at 35:14–17 (Dr. Chao's testimony that a web server has a MAC address). Thus, Patent Owner's arguments that the network devices taught by Ma are distinct from the claimed "computer processors" and Aziz's computing elements are not persuasive because they do not address Petitioner's proposed combination to assign the computing elements of Aziz (computer processors) the virtual MAC address taught by Ma. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981) (one cannot show non-obviousness over a combination of references by attacking references individually). We address Patent Owner's arguments against the combination in Section II.d.4.g *infra*. We note that for the reasons discussed in that section, we determine Petitioner provides sufficient reasons to assign a virtual MAC address, as taught by Ma, to Aziz's computing elements.

e. *"the virtual local area communication network provides communication among a set of computer processors but excludes the processors from the plurality not in the defined set, and*

"[configuration logic to define and establish] (b) a virtual storage space with a defined correspondence to the address space of the storage network; and"

Petitioner contends Aziz teaches the recited virtual local area communication network that provides communications among a set of processors, but excludes processors not in the defined set. Pet. 41–42. We are persuaded that Aziz teaches this limitation through (1) its description of configuring computing elements to be part of the VLAN so that the computing element can access CPUs associated with the VLAN (i.e., providing communications among a set of computer processors) and (2) its description of access restrictions that prevent members of one VSF from accessing the computing resources of another VSF so that computing elements cannot access computing elements not located in the VSF in which they are contained (i.e., excluding the processors not in the defined set). *See* Ex. 1006, 6:46–59, 7:52–67. Patent Owner does not present an argument for this limitation.

We are further persuaded by Petitioner's analysis that Aziz teaches configuration logic that defines and establishes a virtual storage space with a defined correspondence to the address space of the storage network. Pet. 42–48. Aziz describes its control plane (configuration logic) logically partitions (defines and establishes) a subset of storage available on the SAN into a SAN zone ("virtual storage space"). Ex. 1006, 6:17–23, 6:44–52; *see also id.* at 3:18–21 (describing that the control plane dynamically configures SAN switches to couple their ports to one or more computing elements and

storage devices). Aziz further describes that based on its configuration, a computing element "views a different portion of the storage zone on the SAN." *Id.* at 7:52–60. We credit Dr. Shenoy's testimony that a person of ordinary skill in the art would have recognized (1) that Aziz's storage devices provide an addressing mechanism for subdividing the available storage space (address space of the storage network) and (2) that Aziz has a defined correspondence between the SAN zone and the storage devices. *See* Ex. 1004 ¶¶ 114–116. Patent Owner does not present an argument for this limitation.

f. "failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed processor,"

Petitioner asserts Aziz teaches this limitation. Pet. 49–50. Specifically, Petitioner asserts that because Aziz describes its computing elements are assigned automatically from the Idle Pool, and that computing elements are assigned from the Idle Pool "to deal with failures of a particular computing element," a person of ordinary skill in the art would have recognized that Aziz's replacement of a computing element is "responsive to a failure." *Id.* at 49. Petitioner further asserts that a person of skill in the art would have understood that the control plane (logic) performs the assignment of computing elements because Aziz teaches the control plane performs allocation and control of computing elements, such as by automatically assigning computing elements from the Idle Pool to a VSF. *Id.* at 50.

Patent Owner contends Aziz does not teach or render obvious automatically replacing a failed computer processor. PO Resp. 53–57. Patent Owner asserts that the cited statements from Aziz merely reflect that

an administrator may manually place or replace elements in a VSF with those from an Idle Pool after the administrator notices a failure. *Id.* at 54. Patent Owner asserts that Aziz's reference to "under program control" merely refers to the fact that Aziz's control plane is implemented by software and administrator commands are carried out after an administrator provides inputs. *Id.* at 55. Patent Owner further asserts that Petitioner's cited references to "automatically" are related to non-failover embodiments in Aziz and that, when Aziz mentions that no manual intervention is required to increase the number of CPUs and to allocate resources on demand, it merely refers to the fact that an administrator, through the control plane, may allocate resources like CPUs, instead of having to connect new ones. *Id.* at 56–57.

In response, Petitioner reiterates its contention that Aziz teaches automatically replacing a failed computing element. Reply 26–29. Petitioner asserts Aziz's description of high processor availability controlled in real-time by the control plane and its description that a particular VSF is not subjected to manual configuration further show the failover process is automated. *Id.* at 27. Petitioner asserts Aziz discourages manual processes because of the problems induced by human error. *Id.* Petitioner also asserts that Patent Owner admits Aziz automates the steps of adding and removing computing elements and that its expert, Dr. Chao, agrees that failover consists of those two steps. *Id.* at 28 (citing PO Resp. 56–57; Ex. 1035, 14:11–15:6).

We have reviewed the parties' analyses and the supporting evidence and find Petitioner establishes, by a preponderance of the evidence, that Aziz teaches "failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed

processor." Aziz describes each computing element in a VSF is replaceable by any other computing element and that the number of computing elements may change over time under control of the control plane. Ex. 1006, 7:1–5. Aziz further describes "[c]omputing elements from the Idle Pool may be assigned to a particular VSF . . . to deal with failures of a particular computing element in a VSF." Ex. 1006, 7:8–12. Aziz also describes that "[n]o manual intervention is required in order to increase the number of CPUs . . . available to a VSF. All such resources are allocated on demand from . . . resources available in the Idle Pool by the Control Plane." *Id.* at 8:60–65; *see also id.* at 8:66–9:1 ("A particular VSF is not subjected to manual reconfiguration."). Aziz describes the large reserve capacity of the computing grid provides high processor availability and is controlled in real time by the control plane. *Id.* at 8:48–54. Aziz further describes the entire reserve capacity of the computing grid can be used to provide any of the services required by any VSF, which provides a high degree of availability and reliability because each server has potentially thousands of back-up servers able to provide the same service. *Id.* at 8:41–47. Mr. Geng testifies that to provide high availability, any failover would need to be something that is automatic, rather than manual. Ex. 1033, 20:10–14.

We determine the preponderance of the evidence supports Petitioner's position that the failover process described in Aziz is automated. Patent Owner acknowledges that Aziz teaches automation to deal with increase and decrease in loads (automatic growth and shrinkage of a VSF). PO Resp. 56–57; *see* Ex. 1006, 16:1–5 (customer may choose a VSF service plan, such as automatic growth and shrinkage of a VSF between a minimum and maximum number of elements, based on real-time load). Patent Owner's expert, Dr. Chao, admits that failover involves removing the failed

node and replacing it with a new node, i.e., the very same two steps that Aziz discloses are automated. *See* Ex. 1035, 14:11–15:6. In view of Aziz's teachings that adding and removal of processors is automated, that manual intervention is not required to reconfigure a VSF, and that its computing grid provides a high degree of availability, we are not persuaded by Patent Owner's argument that a person of ordinary skill would have understood Aziz to require manual intervention to deal with failure (removing and adding a processor to a VSF). We are also not persuaded by the testimony of Dr. Chao that "[a] person of ordinary skill in the art reading this disclosure in the context of the rest of Aziz would understand it to refer to manual administration re-assignment after an administrator recognizes a computing element has failed." *See* Ex. 2015 ¶ 210. Dr. Chao fails to provide sufficient explanation why the context of the rest of Aziz would lead a person of skill in the art to understand Aziz to disclose manual reassignment; accordingly, it is entitled to little or no weight. *See* 37 C.F.R. § 42.65(a). We give greater weight to the opinion of Dr. Shenoy that the failover process is automated, as it is supported by cited evidence and an explanation of Aziz's teachings. *See* Ex. 1004 ¶¶ 126–130.

For the foregoing reasons, we conclude Petitioner establishes Aziz teaches "failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed processor."

g. "the failover logic including logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor,"

Petitioner contends the combination of Aziz and Ma teaches "failover logic including logic to assign the virtual MAC address of the failed

processor to the processor that replaces the failed processor." Pet 50–51. Petitioner asserts that Ma describes a failover process in which if the active commander fails, the network device having the next highest priority takes over the commander role. *Id.* at 50. Petitioner asserts Ma describes that in the failover process, the ownership of the virtual IP address and the virtual MAC address of the failed network device is transferred to the network device that takes over. *Id.* Petitioner asserts it would have been obvious to combine Ma's teachings with Aziz with the result being that the virtual MAC address of Aziz's failed computing element would be transferred to its replacement computing element and that Aziz's control plane would include the logic to perform this assignment. *Id.* at 51.

Petitioner asserts that it would have been obvious for a person of ordinary skill in the art to combine Aziz and Ma because the combination is merely a use of a known technique to improve a similar device, method, or product in the same way. *Id.* at 26; *see also* Reply 20 (asserting a person of skill in the art would have recognized Aziz suffered from a known problem for which there was a known solution (the reassignable virtual MAC address employed by Ma)). Petitioner asserts a person of ordinary skill in the art would have recognized that Aziz's technique for replacing failed computing elements could lead to the stale IP-MAC address mapping issue that was known in the art, which would have been caused by Aziz's replacement of a failed computing element with a replacement computing element having a different MAC address. Pet. 27. Petitioner asserts the stale IP-MAC address mappings would have caused communication delays and/or network errors for the duration of the time while the mappings were cached and that because of these known issues, a person of skill in the art would have been aware of the conventional way around the problem of stale IP-MAC

addresses to "move the MAC address from the primary to the secondary node." *Id.* (citing Ex. 1009, 89). Petitioner asserts that combining Ma's reassignable virtual MAC addresses with Aziz's computing elements would have been a relatively simple and obvious solution to solve the problem of stale IP-MAC address mappings and would predictably result in Aziz's computing elements each having a virtual MAC address that is transferred to a replacement computing element, with no communication disruption due to IP-MAC address mapping information issues. *Id.* at 28–29; *see also id.* at 40–41 (asserting assigning each of Aziz's computing elements a virtual MAC address would have been advantageous because it would allow the ability to perform failover by assigning the virtual MAC address of failed computing element to its replacement). Petitioner asserts the combination would, therefore, provide noticeable improvements to communication reliability, speed, and error reduction for communications with the computing elements in Aziz's computing grid during and after a failover option. *Id.* at 30. Petitioner's assertions are supported by the testimony of Dr. Shenoy. *See id.* at 26–30, 40–41 (citing Ex. 1004).

Patent Owner contends a person of ordinary skill in the art would not have combined Aziz and Ma. PO Resp. 38–41. Patent Owner asserts Ma is not analogous to either Aziz or the '044 patent, is not from the same field of endeavor, and is not reasonably pertinent to either Aziz or the '044 patent because Aziz and the '044 patent each deal with managing processing resources and Ma deals with managing switches, bridges, and routers. *Id.* at 39–40. Patent Owner further asserts that Petitioner's suggested combination of Ma with Aziz is driven by hindsight because Aziz does not mention "MAC" or include any suggestion of a "stale IP-MAC address mapping

issue" and Aziz already contemplates and addresses how to deal with failure of its computing elements by requiring manual intervention. *Id.* at 40–41.

Petitioner replies that Patent Owner does not address its assertion, supported by testimony of Dr. Shenoy, that a person of ordinary skill in the art would have found the references to be analogous because they all relate to network computing. Reply 21 (citing Pet. 25–26, 64; Ex. 1004 ¶¶ 61, 64, 180). Petitioner asserts Patent Owner's characterization that Ma relates to "management solutions for network devices" does not render Ma non-analogous art because both Dr. Chao and Mr. Manca identify the '044 patent and Aziz as also relating to management of network devices, such as switches. *Id.* at 21 (citing Ex. 1034, 38:8–14; Ex. 1035, 30:7–25, 32:17–20, 34:20–22). Thus, Petitioner asserts that because both Aziz and Ma relate to managing switches, they pertain to the same field of endeavor and are analogous.

Petitioner further asserts that Patent Owner does not dispute Aziz's system is susceptible to stale IP-MAC address issues as discussed in the Petition. Reply 18. Petitioner asserts that Dr. Chao confirms Aziz's computing elements have both IP addresses and MAC addresses and that Dr. Chao agrees that Aziz's system is susceptible to timeouts due to stale IP-MAC address mappings. *Id.* at 18–19. Petitioner asserts that a motivation does not have to be found in the prior art references, but it is sufficient to show that a person of ordinary skill in the art would have recognized that Aziz suffered from a known problem for which there is a known solution (i.e., the reassignable virtual MAC address described by Ma). *Id.* at 20.

We are persuaded Petitioner establishes the combination of Aziz and Ma teaches "failover logic including logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor."

For the reasons discussed previously, Petitioner persuades us that Aziz teaches "failover logic, responsive to a failure of a computer processor, to allocate a computer processor from the plurality to replace the failed processor." Ma also describes a failover process in which, when active commander 21 fails, network device 23 having the next highest priority takes over the commander role and assumes "ownership" of the virtual IP address and the virtual MAC address of the failed active commander. Ex. 1007, 7:24–32. We are persuaded that combining these teachings of Ma with Aziz would meet the recited limitation of "logic to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor."

Petitioner also persuades us that Aziz and Ma are from the same field of endeavor as the '044 patent. Prior art is analogous if is "from the same field of endeavor, regardless of the problem addressed." *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1000 (Fed. Cir. 2016) (internal citations omitted). Patent Owner's assertion that the field of endeavor of Aziz and the '044 patent as "managing processing resources" is unduly narrow and not consistent with the "Field of the Invention" stated in either patent. *See* Ex. 1001, 1:14–19 ("The present invention relates to computing systems for enterprises and application service providers, and more specifically, to processing systems having virtualized communication networks and storage for quick deployment and reconfiguration."); Ex. 1006, 1:6–11 ("The present invention generally relates to data processing. The invention relates more specifically to methods, apparatus, and mechanisms providing an extensible, flexible, and scalable computing system."). In accordance with the written description of Aziz and the '044 patent, we determine the field of endeavor of both is "computing/data processing systems." In providing its

data processing system having virtualized communication networks, Aziz describes configuring LAN switches and SAN switches (i.e., managing switches) to be part of VLANs and SAN zones. *See* Ex. 1007, 3:17–22, 7:52–55; *see also* Ex. 1035, 30:21–22, 32:7–20 (Dr. Chao's admission that Aziz manages VLAN and SAN switches). The '044 patent similarly describes management logic and control node logic that are responsible for establishing, managing, and destroying communication paths, which Mr. Manca testifies is done by managing switch fabrics to set up the paths between the nodes. *See* Ex. 1001, 4:66–5:2; Ex. 1034, 38:5–24; *see also* Ex. 1035, 34:19–22 (Dr. Chao's testimony that the '044 patent talks about managing switches). Thus, Petitioner persuades us the field of endeavor of Aziz and the '044 patent (computing/data processing systems) encompasses the field of endeavor of Ma (management of network devices), and, therefore, we determine Aziz and Ma are analogous art to the '044 patent.

Additionally, Petitioner provides persuasive rationale to combine Aziz with Ma in the proposed manner. We are persuaded the proposed combination is the use of a known solution (Ma's virtual MAC addresses that are reassignable upon failover to a replacement device) to a known problem (stale IP-MAC address mapping issues that result in communication delays for duration of time mappings were cached). *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 419 (2007). Petitioner's assertions that Aziz's technique for replacing failed computing elements could lead to stale MAC address mapping issues are supported by testimony of Dr. Shenoy, which we credit. *See* Ex. 1004 ¶¶ 66, 67. Patent Owner's expert, Dr. Chao, also agrees that if you don't migrate over the MAC addresses, there would be a timeout period during which the replacement server would not be available. Ex. 1035, 40:23–42:2. Petitioner's additional assertions—that a person of

ordinary skill in the art would have been aware a known solution to the problem of stale IP-MAC address is to re-assign the MAC address—are also supported by testimony of Dr. Shenoy, which we likewise credit. Ex. 1035, 68–70. Dr. Shenoy further supports his testimony by citing to a book published on January 31, 2000, by Evan Marcus and Hal Stern (Ex. 1009, "Marcus").[4] *See* Ex. 1004 ¶¶ 43–46, 67–68 (citing Ex. 1009); *see also* Pet. 19– 21 (Petitioner's assertions that Marcus describes a conventional technique known for performing failover in a network to migrate the MAC address to avoid the problem caused by clients that cached the MAC address). Marcus establishes that a known solution to stale cached MAC addresses is to configure the secondary (replacement) machine with the MAC address used by the primary machine node after a failover. *See* Ex. 1009, 88–89. We are persuaded by Dr. Shenoy's testimony that by removing the stale mapping problem, the combination would provide improvements to communication reliability, speed, and error reduction after a failover operation. *See* Ex. 1004 ¶ 72.

Contrary to Patent Owner's contention, it is not necessary for Aziz to mention a stale IP-MAC address mapping issue; instead, the relevant inquiry is whether Petitioner has set forth articulated reasoning with rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (cited with approval in *KSR*, 550 U.S. at

[4] Petitioner provides sufficient evidence to establish Marcus is a book that was published on January 31, 2000. *See* Pet. 19; Ex. 1015 ¶ 1, 12, Appendix A (declaration of Mr. David Bader, librarian at Haynes and Boone, LLP., testifying that Appendix A is a true and accurate copyright registration from the Library of Congress that evidences Marcus was published at least as of January 31, 2000). Patent Owner does not contest the prior art status of Marcus in its Response.

418). We are also unpersuaded by Patent Owner's argument that Aziz already deals with failure of its computing elements with manual intervention because, as already discussed, we are not persuaded the failover performed by Aziz requires manual intervention.

For the foregoing reasons, we conclude Petitioner establishes the combination of Aziz and Ma teaches failover logic "to assign the virtual MAC address of the failed processor to the processor that replaces the failed processor" and that it would have been obvious for one of ordinary skill in the art to combine the teachings of Aziz and Ma in the proposed manner.

h. "logic to assign the virtual storage space and defined correspondence of the failed processor to the processor that replaces the failed processor,"

Petitioner contends Aziz teaches this limitation through its description that a computing element is assigned from the Idle Pool to a VSF to replace a failed computing element and that when a computing element is moved to the VSF from the Idle Pool, the control plane configures SAN switches associated with the computing element to be part of the SAN zones associated with a particular VSF. Pet. 51–53.

Patent Owner argues that Aziz does not teach re-assigning virtual storage space to the replacement computing element, much less in an automated way. PO Resp. 57–58. Patent Owner asserts there is no disclosed automation to Aziz's replacement of failed computing elements, including as to re-assigning virtual storage space to the replacement computing element. *Id.* at 59.

Petitioner replies that, similar to its assertions regarding "automatic" failure of a computing element, assigning the replacement computing

element to its virtual storage space was understood to be automatic because it is part of the failover process. Reply 31.

We determine Petitioner establishes, by a preponderance of the evidence, that Aziz teaches logic that assigns the virtual storage space and defined correspondence of the failed processor to the processor that replaces the failed processor. For the reasons discussed above, we agree with Petitioner that Aziz teaches automatically assigning a computing element from the Idle Pool to a particular VSF to deal with a failure of a computing element. *See* Ex. 1006, 7:8–12; *see also id.* at 8:41–66 (discussing the high availability of the computing grid and that no manual intervention is needed to allocate resources from the Idle Pool to a VSF). We also agree that Aziz further describes that when a computing element becomes part of a VSF, the control plane configures the SAN switches associated with the computing element to be part of the SAN zones (virtual storage space) associated with a particular VSF. *See id.* at 3:18–23; 8:41–66. Patent Owner's arguments that the failover process is not automated are unpersuasive for the reasons discussed previously.

i. "logic to reestablish the virtual local area network to include the processor that replaces the failed processor and to exclude the failed processor."

Petitioner contends Aziz's control plane teaches the "logic" recited in this limitation. Pet. 53–56. In particular, Petitioner asserts Aziz teaches a computing element that replaces a failed computer element is moved from the Idle Pool to a VSF and is assigned to the VLAN (virtual local area network) of the failed computing element. *Id.* at 53–54. Petitioner further asserts that in view of Aziz's teaching that the control plane can remove a computing element from a VSF when it is no longer needed, a person of

ordinary skill in the art would have known to remove the failed computing element from the VLAN to avoid causing network problems. *See* Pet. 53–56.

We determine Petitioner establishes that Aziz teaches this limitation. The cited sections of Aziz describe that control plane moves computing elements from the VSF back into the Idle Pool when it is no longer needed. Ex. 1006, 7:42–44. Aziz further describes that when adding or removing computing elements from a VSF, the control plane configures the LAN switches and SAN switches associated with that computing element to be part of the VLAN associated with a particular VSF or Idle Pool. *Id.* at 7:52–55. We are persuaded a person of skill in the art would have had reason to remove the failed computing element from a VSF when it is no longer needed. We credit the testimony of Dr. Shenoy that failing to remove the failed computer element would have caused multiple problems in the network, including problems caused by having two computing elements with the same address and problems caused by lost network packets (network delays, wasted bandwidth, and reduced network performance). *See* Ex. 1004 ¶ 149. Patent Owner does not present separate arguments for this limitation.

j. Conclusion

For the foregoing reasons, we conclude Petitioner has demonstrated, by a preponderance of the evidence, that claim 1 would have been obvious over Aziz and Ma.

5. Claim 4

Independent claim 4 is a method claim that recites limitations that are substantially similar to the functions performed by the configuration logic and failover logic recited in system claim 1. Petitioner contents Aziz teaches a method of computing processing as set forth in the preamble of claim 4

and refers back to its analysis of claim 1 for the remaining limitations. *See* Pet. 58–61. Patent Owner does not present separate arguments for this claim. We determine Aziz and Ma teach each limitation of claim 4 for the same reasons discussed previously for claim 1.

6. Claims 3 and 6

Claim 3 depends from claim 1 and recites

> wherein the configuration logic establishes a second virtual local area network from a second set of computer processors and a second virtual storage space with a defined correspondence to the storage network address space and wherein the failover logic causes the processor replacing the failed processor to inherit the virtual local area network and the virtual storage personality.

Claim 6 recites substantially similar limitations. Petitioner asserts Aziz teaches these limitations through its description of establishing a second VLAN from a second set of computing elements and a second SAN zone and defined correspondence to SAN address space. Pet. 56–58, 61. Patent Owner does not present separate arguments for these claims. We agree with Petitioner's analysis and find Aziz teaches the limitations recited in claims 3 and 6. *See* Ex. 1006, Fig. 4B (depicting VSF1, VSF2), 22:49–64 (claiming creating a second virtual local area network coupled with a second subset of storage devices).

E. Obviousness over Aziz, Ma, and Von Eicken

Petitioner challenges claims 2 and 5 as obvious under 35 U.S.C. § 103(a) over Aziz, Ma, and Von Eicken. Pet. 62–74.

1. Scope and Content of Von Eicken

Von Eicken is an article published in the IEEE's Computer publication in November of 1998. Pet. 13, 62; *see also* Ex. 1015 ¶¶ 2–6 (declaration of David Bader testifying that the publication information

provided by IEEE indicates that Von Eicken was published in the November 1999 periodical of Computer). Von Eicken describes the evolution of the Virtual Interface Architecture (VIA), a standard for a user-level network that allows applications to send and receive network packets without operating system intervention. Ex. 1008, 61. Using this architecture, computer processes open virtual interfaces (VIs) that represent handles onto the network. *Id.* at 65. Each VI represents a connection to a single other remote VI. *Id.* Von Eicken further describes that "[p]roducts based on the VIA have already surfaced, notably GigaNet's GNN1000 network interface." *Id.* at 61.

2. Claims 2 and 5

Claim 2 depends from claim 1 and recites

> wherein the configuration logic establishes virtual interfaces to define software communication paths among processors of the virtual network and wherein the failover logic includes logic to establish virtual interfaces from the processors in the virtual network to the processor that replaces the failed processor.

Petitioner contends the combination of Aziz, Ma, and Von Eicken teach the limitations set forth in claim 2. Pet. 69–74. Petitioner asserts Aziz teaches a control plane ("configuration logic") that interconnects computing elements in a VLAN using network interfaces. *Id.* at 69. Petitioner asserts Ma teaches assigning a virtual IP address and a virtual MAC address (virtual interfaces) to a network device both as a source address for sending traffic and an address to receive cluster member traffic. *Id.* at 69–70. Petitioner asserts it would have been obvious to establish Ma's virtual address in Aziz's computing grid so that the virtual address could be moved from the failed computing elements to replacement computing elements as described in the contentions for claim 1. *Id.* at 70.

Petitioner further asserts Von Eicken teaches virtual interfaces that are opened to "define communication paths" (software communication paths) among processors for communicating messages. *Id.* Petitioner asserts it would have been obvious to a person of ordinary skill in the art to have Aziz's control plane configure the computing elements with the software that is described by Von Eicken to allow the computing elements to open virtual interfaces for communications among the computing elements. *Id.* at 71. For the "failover logic . . . to establish virtual interfaces from the processors in the virtual network to the processor that replaces the failed processor" limitation, Petitioner asserts it would have been obvious to a person of skill in the art to establish virtual interfaces from the computing elements in Aziz's virtual local area network to the replacement processor so that communications involving the replacement computing element would have the same low-latency advantages that virtual interfaces offered to the failed computing element. *Id.* at 72.

Patent Owner does not provide separate argument for claim 2 or challenge Petitioner's assertions regarding Von Eicken. *See* PO Resp. 25 ("For the purposes of this response, only Aziz and Ma will be discussed.").

We have reviewed Petitioner's analysis and supporting evidence and are persuaded Petitioner establishes by a preponderance of the evidence the combination of Aziz, Ma, and Von Eicken teaches the limitations set forth in claim 2. For example, for substantially similar reasons as the reasons discussed in reference to claim 1, we are persuaded the combination of Aziz and Ma teaches configuration logic that establishes virtual interfaces (virtual MAC and virtual IP addresses). As another example, we agree with Petitioner that Von Eicken teaches virtual interfaces used to open software communication paths through its description of open virtual interfaces that

represent handles onto the network used to send and receive messages. *See* Ex. 1008, 61, 65. We further determine Petitioner provides sufficient reasons why a person of ordinary skill in the art would have combined the teachings of Von Eicken with Aziz and Ma in the proposed manner. *See id.* at 65–69. In particular, we are persuaded a person of ordinary skill in the art would have applied Von Eicken's teachings of virtual interfaces to Aziz's computing elements to reduce communication latency and increase network throughput. *Id.* at 68–69. We are also persuaded it would have been simple to substitute Von Eicken's known virtual interfaces for Aziz's network interfaces because virtual interfaces were designed to be implemented in clustered computing systems. *Id.* at 66; *see also* Ex. 1008, 61 ("[T]he Virtual Interface Architecture [is] an emerging standard for cluster or system-area networks.").

Claim 5 recites substantially similar limitations as claim 2. Petitioner sets forth an analysis of claim 5 that cites to the analysis of claim 2 and provides additional analysis addressing the minor differences in these claims. *See* Pet. 73–74. We determine Petitioner establishes the Aziz-Ma-Von Eicken combination teaches the limitations of claim 5 for the reasons set forth in its analysis, which are substantially similar to the reasons given for claim 2.

We conclude Petitioner has demonstrated, by a preponderance of the evidence, that claims 2 and 5 would have been obvious over the combination of Aziz, Ma, and Von Eicken.

III. PATENT OWNER'S MOTION TO EXCLUDE EVIDENCE

Patent Owner moves to exclude Exhibit 1004 ¶¶ 34–41, 43, 46, 68, 149, and 182; Exhibit 1033, 3:1–16, 17:1–16, 19:5–11, 20:10–15, and 46:7–21; Exhibit 1034, 11:24–12:6, 13:5–9, 13:20–25, and 21:15–23; and Exhibit

1035, 12:16–21, 21:21–22:1, 41:14–42:4, 51:21–23, 52:3–4, and 54:4–10. Mot. to Exclude 2–3, 10–12. Patent Owner further moves to exclude the entirety of Exhibits 1009–1014, 1016, 1019–1022, 1024, 1027–1031, 1036, and 1037. *Id.* at 2–3. Petitioner opposes this motion and asserts the evidence is admissible. *See* Mot. Opp.

We do not rely on Exhibits 1010–1014, 1016, 1019–1022, 1024, 1027–1031, 1036, and 1037 in our Final Written Decision to reach our conclusion that Petitioner has met its burden in demonstrating the challenged claims are unpatentable. Accordingly, we deny Patent Owner's motion to exclude this evidence as moot.

Exhibit 1004 is the Declaration of Petitioner's expert, Dr. Shenoy. Patent Owner asserts paragraphs 34–41, 43, 46, 68, 149, and 182 are inadmissible under Federal Rules of Evidence 401, 403, 702, and 703 to the extent they rely on Exs. 1009–1014, 1016, and 1019–1022, because those exhibits are inadmissible under Federal Rules of Evidence 401–403. Mot. to Exclude 3–4. Petitioner asserts the underlying exhibits are admissible, but that even if the evidence was excluded, that would not provide a basis for excluding any portion of Dr. Shenoy's testimony. Mot. Opp. 14. As noted by Petitioner, facts or data in forming an opinion on the subject need not be admissible for the opinion to be admitted if experts in the field would reasonable rely on those facts or data in forming an opinion. *See* Fed. R. Evid. 703. Furthermore, for the foregoing and following reasons, we deny Patent Owner's motion to exclude the underlying exhibits. Therefore, we deny Petitioner's motion to exclude portions of Exhibit 1004.

Exhibit 1009 is a collection of excerpts from a book authored by Evan Marcus and Hal Stern ("Marcus"). Patent Owner asserts this exhibit is irrelevant under Federal Rule of Evidence 401, and thus inadmissible under

Rule 402, or as confusing or a waste of time under Rule 403. Mot. Opp. 4. Patent Owner asserts Marcus was not relied on by Petitioner as prior art in its Petition or Reply, and the Board did not cite or rely on this exhibit in its Institution Decision. *Id.* at 5. We are not persuaded the evidence is inadmissible. We agree with Petitioner that Exhibit 1009 relates to issues in this case as it demonstrates the knowledge of those of skill in the art and supports Petitioner's assertions it would have been obvious to combine Aziz and Ma. *See* Mot. Opp. 2–3; *see also Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015) ("Art can legitimately serve to document the knowledge that skilled artisans would bring to bear in reading the prior art identified as producing obviousness."). Accordingly, we disagree with Patent Owner that the evidence is not relevant, and deny Patent Owner's motion to exclude Exhibit 1009.

Exhibits 1033–1035 are deposition testimony of Mr. Geng, Mr. Manca, and Dr. Chao, respectively. Patent Owner asserts these exhibits should either be excluded or be considered with the remainder of related recorded statements under Federal Rules of Evidence 106. Mot. to Exclude 10–12. We agree with Petitioner that this objection is baseless because the deposition transcripts have been entered into the record in their entirety. *See* Mot. Opp. 15. We, therefore, deny Patent Owner's motion to exclude these exhibits.

For the foregoing reasons, Patent Owner's Motion to Exclude is *denied*.

IV. CONCLUSION

Petitioner has demonstrated by a preponderance of the evidence that

A. Claims 1, 3, 4, and 6 of the '044 patent are unpatentable under 35 U.S.C. § 103(a) over Aziz and Ma; and

B. Claims 2 and 5 of the '044 patent are unpatentable under 35 U.S.C. § 103(a) over Aziz, Ma, and Von Eicken.

IV. ORDER

It is

ORDERED that, based on a preponderance of the evidence, claims 1–6 of U.S. Patent No. 6,971,044 B2 are unpatentable under 35 U.S.C. § 103(a); and

FURTHER ORDERED that Patent Owner's Motion to Exclude Evidence (Paper 29) is *denied*.

This is a final written decision of the Board under 35 U.S.C. § 318(a), and, therefore, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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