UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01414
Patent 6,208,574

PATENT OWNER'S NOTICE OF APPEAL

IPR2017-01414
Patent 6,208,574

Director of the U.S. Patent and Trademark Office
c/o Office of the General Counsel
Madison Building East, 10B20
600 Dulany Street
Alexandria, VA 22314-5793

Pursuant to 35 U.S.C. §142 and 37 C.F.R. § 90.2(a), Patent Owner ProMOS Technologies, Inc. hereby provides notice of its appeal to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered on November 8, 2018 (Paper 16), and from all underlying orders, decisions, rulings and opinions provided therein.

Pursuant to 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal may include, but are not limited to:

1. The Patent Trial and Appeal Board's determination of unpatentability of claims 1-3 and 30-37 of U.S. Patent No. 6,208,574 under 35 U.S.C. § 103(a).

Simultaneously with this submission, a copy of the Notice of Appeal is being filed with the Patent Trial and Appeal Board. In addition, the required copy of this Notice of Appeal, along with the docketing fee, are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Dated: January 10, 2019

Respectfully submitted,

By: */s/ Kevin C. Jones*
Registration No. 55,308

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Certificate of Filing

I hereby certify that on January 10, 2019, pursuant to 37 C.F.R. § 90.2(a) a copy of Patent Owner's Notice of Appeal was filed with the Patent Trial and Appeal Board pursuant to the procedures provided in 37 C.F.R. § 42.6(b) by filing a copy using the PTAB E2E system.

I hereby certify that the required copies of Patent Owner's Notice of Appeal were filed with the required docketing fee on January 10, 2019 with the Clerk's Office of the United States Court of Appeals for the Federal Circuit.

CERTIFICATE OF SERVICE

I hereby certify that on January 10, 2019, a true and correct copy of the foregoing PATENT OWNER'S NOTICE OF APPEAL was served electronically via email to the Petitioner by serving the correspondence email addresses of record as follows:

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Paper No. 16
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

PROMOS TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2017-01414
Patent 6,208,574 B1

Before JAMESON LEE, KEVIN F. TURNER, and MATTHEW J. McNEILL, *Administrative Patent Judges.*

McNEILL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

On May 12, 2017, Petitioner, Samsung Electronics Co. Ltd., filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 1–3 and 30–37 of U.S. Patent No. 6,208,574 B1 (Ex. 1001, "the '574 patent"). In an initial decision, we instituted *inter partes* review of each of the challenged claims. Paper 6 ("Dec. Inst.").

ProMOS Technologies Inc. ("Patent Owner") filed a Patent Owner Response (Paper 10, "PO Resp."), and Petitioner filed a Reply (Paper 12, "Reply").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued under 35 U.S.C. § 318(a). We determine that Petitioner has shown by a preponderance of the evidence that claims 1–3 and 30–37 of the '574 patent are unpatentable.

B. Related Matters

Petitioner concurrently filed a Petition challenging claims 4–18 and 21–27 of the '574 patent in IPR2017-001415. Pet. 1. Petitioner identifies U.S. Patent No. 6,088,270 ("the '270 patent") as related to the '574 patent. Pet. 2. Petitioner indicates that the '270 patent is the subject of *inter partes* review in IPR2017-00036. *Id*.

Petitioner indicates that Patent Owner asserted the '574 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co.*, No. 1:16-cv-00335-SLR-SRF (D. Del.). Pet. 1. Petitioner indicates Patent Owner has also asserted the following patents in that action: U.S. Patent Nos. 6,069,507; 6,172,554; 6,562,714; 7,375,027; and 6,559,044. *Id.* Petitioner concurrently filed IPR petitions challenging the other asserted

patents in the following *inter partes* review proceedings: IPR2017-01412, IPR2017-01413, IPR2017-01416, IPR2017-01417, IPR2017-01418, and IPR2017-01419. *Id*.

Petitioner also filed several IPR petitions involving patents asserted by Patent Owner against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co.*, No. 1:15-cv-00898-SLR-SRF (D. Del.). Pet. 1–2. Petitioner identifies the following *inter partes* review proceedings for the patents involved in that suit: IPR2017-00032, IPR2017-00033, IPR2017-00035, IPR2017-00036, IPR2017-00037, IPR2017-00038, IPR2017-00039, and IPR2017-00040. *Id.*

C. The ’574 Patent

The ’574 patent relates to sense amplifiers in integrated circuit memories. Ex. 1001, 1:9–11. Integrated circuit memories often include a large number of memory cells set forth in a memory array. *Id.* at 1:14–15. Memory arrays are often organized into rows and columns. *Id.* at 1:35–36. Rows represent the memory cells located along a word line. *Id.* at 1:36–37. Columns are organized perpendicularly to the rows and represent the memory cells located along a bit line. *Id.* at 1:37–40. Generally, each column is connected to a sense amplifier. *Id.* at 1:40–41. In a large memory cell with thousands of columns and rows, the voltage that reaches sense amplifiers at different ends of the array may be appreciably different as a result of resistance along the lines, causing inefficient or slow operation. *Id.* at 2:15–39. The ’574 patent relates to additional circuitry that may be connected to the sense amplifiers to alleviate these issues. *Id.* at 4:61–5:39.

One embodiment of the ’574 patent is represented in Figure 5, which is reproduced below.

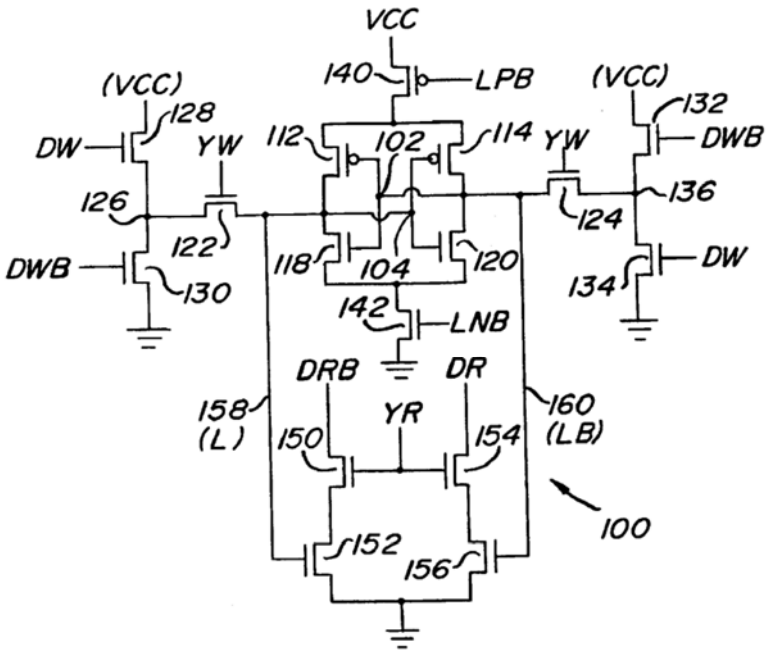


FIG. 5

Figure 5 depicts sense amplifier 100 having a latch formed by transistors 112, 114, 118, and 120. *Id.* at 6:6–9. Node 102 is coupled to the gate electrodes of P-channel transistor 112 and N-channel transistor 118. Node 102 is also coupled to the source-drain path of pass transistor 124. *Id.* at 6:28–31. Node 104 is coupled to the gate electrodes of P-channel transistor 114 and N-channel transistor 120. *Id.* at 6:9–13. Node 104 is also coupled to the source-drain path of pass transistor 122. *Id.* at 6:28–31. Pass transistors 122 and 124 are driven by column write select signal YW. *Id.* at 6:15–16.

Transistor 122 is coupled to node 126 between the source of local data write driver transistor 128 and the drain of local data write driver transistor 130. *Id.* at 6:32–35. Transistors 128 and 130 are N-channel transistors having their source-drain paths coupled in series. *Id.* at 6:35–36. The drain of transistor 128 is coupled to VCC and the source of transistor 130 is

coupled to ground. *Id.* at 6:36–38. Data write signal DW is coupled to the gate electrode of transistor 128, and its complement DWB is coupled to the gate electrode of transistor 130. *Id.* at 6:38–40. Transistors 132 and 134 on the opposite side of sense amplifier 100 have a similar arrangement, though DW and DWB are applied oppositely. *Id.* at 6:40–47.

Figure 5 also depicts local sense amplifier drive transistors 140 and 142. *Id.* at 7:16–18. Transistor 140 is coupled to the source electrodes of transistors 112 and 114. *Id.* at 6:53–55. The source electrode of transistor 140 is coupled to VCC (or LATCHP). *Id.* at 6:55–56. The gate of transistor 140 is coupled to LPB, which is the logical complement of LATCHP. *Id.* at 6:56–57. Transistor 142 is similarly configured with N channel transistors 118 and 120, but the gate electrode of transistor 142 is coupled to signal LNB, the logical complement of LATCHN. *Id.* at 6:59–65.

The lower portion of Figure 5 also depicts a local column read amplifier comprising N channel transistors 150, 152, 154, and 156. *Id.* at 6:66–7:1. The source-drain paths of transistors 150 and 152 are coupled in series, and the drain electrode of transistor 150 receives signal DRB, the logical complement of a data read signal DR. *Id.* at 7:1–4. The gate electrode of transistor 150 is coupled to column read signal Y_R. *Id.* at 7:7–8. The source electrode of transistor 152 is coupled to ground. *Id.* at 7:4–5. The gate electrode of transistor 152 is coupled to node 104. *Id.* at 7:5–7.

The source-drain paths of transistors 154 and 156 are similarly configured, being coupled in series between data read signal DR and ground on the right side of the figure. *Id.* at 7:8–10. The gate electrode of transistor 156 is coupled to node 102. *Id.* at 7:11–13.

Petitioner notes that the '574 patent claims priority to an earlier application filed on November 12, 1992. Ex. 1001, at [62]. As discussed below, Petitioner establishes that the asserted references qualify as prior art assuming that November 12, 1992, is the priority date of the '574 patent. *See* Pet 4.

Claims 1 and 30 of the '574 patent are independent and reproduced below:

> 1. In an integrated circuit memory having a plurality of bit line pairs, a combination comprising a plurality of sense amplifiers; a plurality of local sense amplifier drive transistors; a plurality of local column read amplifiers; and a plurality of local data write driver circuits;
>
> each sense amplifier comprising a latch circuit having a pair of internal nodes coupled to a corresponding pair of bit lines, the latch circuit including a pair of P channel transistors and a pair of N channel transistors;
>
> wherein each sense amplifier is connected to a first said local sense amplifier drive transistor having a source drain path coupled to said P channel transistors of the latch circuit, said first local sense amplifier drive transistor selectively coupling said P channel transistors to a first voltage source;
>
> wherein each sense amplifier is connected to a second said local sense amplifier drive transistor having a source drain path coupled to said N channel transistors of said latch circuit, said second local sense amplifier drive transistor selectively coupling said N channel transistors to a second voltage;
>
> a first control line coupled to control the operation of a plurality of said first local sense amplifier drive transistors;
>
> a second control line coupled to control the operation of a plurality of said second local sense amplifier drive transistors;

a first voltage supply line coupled to said plurality of said first local sense amplifier drive transistors;

a second voltage line coupled to said plurality of second local sense amplifier drive transistors;

wherein each said column read amplifier is responsively coupled to said internal nodes of said latch circuit of a corresponding sense amplifier; and

wherein each said sense amplifier is coupled to a pair of said local data write driver circuits, each local data write driver circuit being configured to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes;

wherein each said local data write driver circuit is coupled to both a respective one of said internal nodes of its corresponding sense amplifier and a corresponding bit line.

30. A sense amplifier arrangement for an integrated circuit memory comprising, for each of a plurality of sense amplifiers:

a sense amplifier latch circuit having first and second latch nodes to which respective bit lines may be coupled;

a local column read amplifier having transistors responsively coupled to at least one of said first and second latch nodes, and receiving at least one data read signal, said local read amplifier being configured to control the current of said data read signal based on the state of said one latch node; and

first and second local data write driver circuits, each being configured to receive a respective data signal at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits, said first and second data write driver circuits being coupled to said first and second latch nodes

to provide signals based on said respective data signal to said first and second latch nodes during a writing operation.

Ex. 1001, 12:57–13:35, 15:52–16:12.

D. Evidence Relied Upon

Petitioner relies on the following prior art:

Japanese Patent Application Publication No. S58-128087, published July 30, 1983 (Ex. 1007, "Inoue");[1]

UK Patent Application Publication No. G.B. 2246005A, published January 15, 1992 (Ex. 1008, "Min"); and

Hamade, U.S. Patent No. 5,323,349, filed August 28, 1992, issued June 21, 1994 (Ex. 1009, "Hamade").

Petitioner also relies upon the testimony of Dr. R. Jacob Baker, Ph.D. Ex. 1002.

E. The Asserted Ground

Petitioner asserts the following ground of unpatentability:

References	Basis	Claims Challenged
Inoue, Min, and Hamade	§ 103(a)	1–3 and 30–37

[1] Petitioner relies on a certified English translation of Inoue. Exhibit 1007 includes an English language version of Inoue (pages 1–6), the Japanese language version of Inoue (pages 7–10), a declaration certifying the English translation (page 11), and a certified correction to the translation (page 12). Our citations refer to the certified English translation of Inoue (pages 1–6 of Exhibit 1007).

II. ANALYSIS

A. Claim Construction

The '574 patent has expired. We review expired patent claims according to the standard applied by the district courts. *See In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Specifically, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

In our Institution Decision, we adopted Petitioner's proposal (*see* Pet. 12–13) to construe the limitation "local data write driver circuit" in claims 1, 4, and 30 to mean "a data write driver circuit that is associated with only one latch circuit." Dec. Inst. 10–11. We were persuaded by Petitioner's evidence from the specification of the '574 patent that local write driver circuits are connected to or associated with a single latch circuit. *Id.* at 10 (citing Ex. 1001, 4:61–63, 5:29–36, 6:5–13, 7:15–16, 11:25–31, Fig. 5). We also were persuaded that Petitioner's proposed construction was consistent with arguments made by the patentee during prosecution. *Id.* at 10–11 (citing Ex. 1006, 274; Ex. 1005, 166–68). We also determined that Petitioner's proposal was consistent with the Board's prior construction from an *ex parte* appeal of the application that matured into the related '270 patent, where "local" was defined as having "a definite spatial form or location." *Id.* at 10.

In its Response, Patent Owner does not dispute that "a local write driver circuit" is disclosed by the cited prior art combination under any asserted construction, including Petitioner's proposed construction and the *ex parte* appeal construction proposed by Patent Owner. PO Resp. 6. Instead, Patent Owner argues "the resolution of the parties' claim construction dispute is immaterial to the questions of [unpatentability] presented to the Board, [so] there is no need to construe [this] term[]." *Id.* at 7. Patent Owner characterizes this claim construction issue as being "relevant only to infringement issues before the district court," such that any construction we adopt would amount to an advisory opinion. *Id.* at 6. Thus, Patent Owner argues we should withdraw our preliminary claim construction of "local write driver circuit," or adopt the Board's earlier construction from the *ex parte* appeal. *Id.* at 7–12.

In its Reply, Petitioner urges us to maintain the construction from our Institution Decision because "there is a dispute between the parties as to the proper construction of [this] term[]." *See* Pet. Reply 4. Petitioner asserts the evidence of record supports our preliminary construction. *Id.* at 4–8.

We are persuaded by Patent Owner's arguments. Whether the prior art teaches a "local write driver circuit" is not disputed in this proceeding. *See* PO Resp. 6. Because Patent Owner did not file a Preliminary Response, as is its right,[2] we construed "local write driver circuit" in our Institution Decision anticipating that this construction might affect the outcome of this case. Now

[2] Patent Owner is not required to file a Preliminary Response. *See* 37 C.F.R. § 42.107(a) ("The patent owner *may* file a preliminary response to the petition.") (emphasis added).

that we have the benefit of Patent Owner's positions from its Response, we see no reason to explicitly construe the term. Importantly, our reviewing court has stated that "claim terms need only be construed 'to the extent necessary to resolve the controversy.'" *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). In the absence of any controversy about Petitioner's unpatentability contentions for a "local write driver circuit," we determine that no construction is necessary.

In our Institution Decision, we also adopted Petitioner's proposed constructions (*see* Pet. 16–21) for the limitations "local column read amplifier" in claims 1, 4, and 30, and "local sense amplifier driver transistor(s)" in claim 1. Dec. Inst. 11–13. However, for the same reasons as "local data write driver circuit," we determine that neither of these limitations, nor any other terms, require explicit construction.

B. Level of Ordinary Skill in the Art

As to the level of ordinary skill in the art, Petitioner states:

> A person of ordinary skill in the art at the time of the alleged invention of the '574 patent ('POSITA') would have had at least a Bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in design of semiconductor memory circuits.

Pet. 4. Petitioner also states that "[m]ore education can supplement practical experience and vice versa." *Id.* at 4. Petitioner's position is supported by Dr. Baker's testimony (Ex. 1002 ¶ 20) and is not disputed by Patent Owner. We find Petitioner's proposed level of skill vague because it relies on the qualifier "at least." The qualifier makes the range of education and the range of working experience unacceptably broad. We adopt Petitioner's

articulation of the level of ordinary skill in the art, as we credit the declaration of Dr. Baker (Ex. 1002 ¶ 20), but without inclusion of the qualifier "at least."

C. Alleged Obviousness of Claims 1–3 and 30–37 over Inoue, Min, and Hamade

We have reviewed the arguments and evidence presented by Petitioner and Patent Owner. Petitioner has shown by a preponderance of the evidence that claims 1–3 and 30–37 would have been obvious over Inoue, Min, and Hamade.

1. Inoue

Inoue is a Japanese patent application publication directed to "a semiconductor device that consumes only a small amount of transient power when writing to a flip-flop." Ex. 1007, 3. Figure 6 of Inoue is reproduced below.

第 6 図

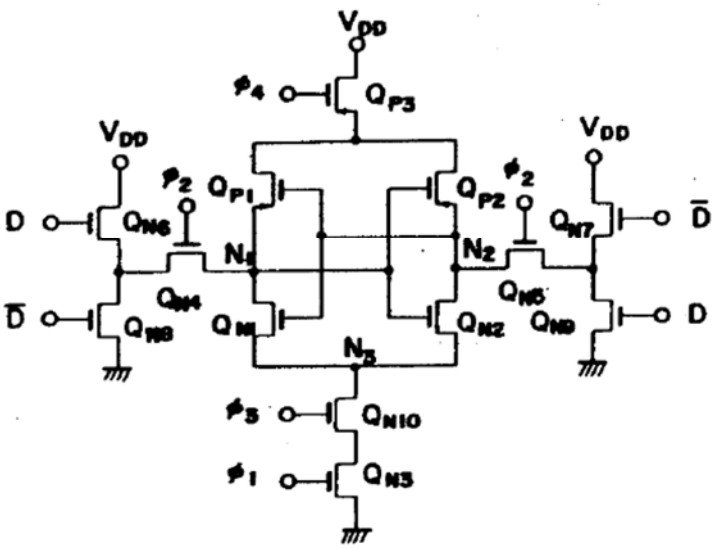


Figure 6 depicts a CMOS flip-flop circuit having supply terminals V_{DD}, nodes N_1–N_3, N-channel transistors Q_{N1}–Q_{N10}, P-channel transistors

Q_{P1}–Q_{P3}, and clocks ϕ_1–ϕ_4. *Id.* at 3–4. D and $\overline{D}$ are input terminals. *Id.* at 4. The circuit in Figure 6 may be applied to a sense amplifier in a dynamic memory, wherein nodes N_1 and N_2 correspond to bit lines and transistors Q_{N6}–Q_{N9} correspond to the output stage for the data input buffer. *Id.*

We agree with Petitioner (Pet. 4) that Inoue qualifies as prior art under at least 35 U.S.C. § 102(b)[3] because Inoue's publication date of July 30, 1983, is more than one year before the earliest possible priority date for the '574 patent, which is November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1007, at [43].

2. Min

Min is a United Kingdom patent application publication directed to a sense amplifier driving circuit for controlling sense amplifiers of a high-density semiconductor memory device. Ex. 1008, Abstract. Figure 3B of Min is reproduced below.

[3] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the priority date of the '270 patent is before the effective date of the applicable AIA amendments, the pre-AIA versions of 35 U.S.C. §§ 102 and 103 apply.

FIG. 3B

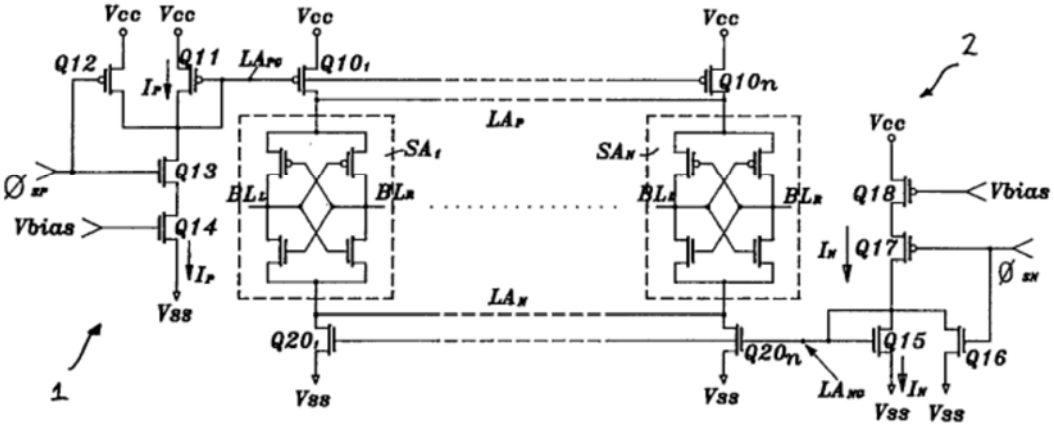


Figure 3B depicts a memory device with a plurality of sense amplifiers SA_1–SA_N. Ex. 1008, 1:4–8, Fig. 3B. Each sense amplifier is coupled to a bit line pair (BL_L and BL_R). Ex. 1008, 2:5–15, Fig. 3B. Each sense amplifier is also coupled to a positive power supply (V_{CC}) via driving transistor $Q10_i$ and to ground (V_{SS}) via driving transistor $Q20_i$. *Id*. at 21:1–13, Fig. 3B. Min discloses a common driving signal from driving transistors $Q10_i$ and $Q20_i$. Ex. 1008, Fig. 3B.

We agree with Petitioner (Pet. 4) that Min qualifies as prior art under at least 35 U.S.C. § 102(a) because Min's publication date of January 15, 1992, is before the earliest possible priority date for the '574 patent, which is November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1008, at [43].

3. Hamade

Hamade discloses a semiconductor memory device. Ex. 1009, 1:8–9. Figure 1 of Hamade is reproduced below.

FIG. 1

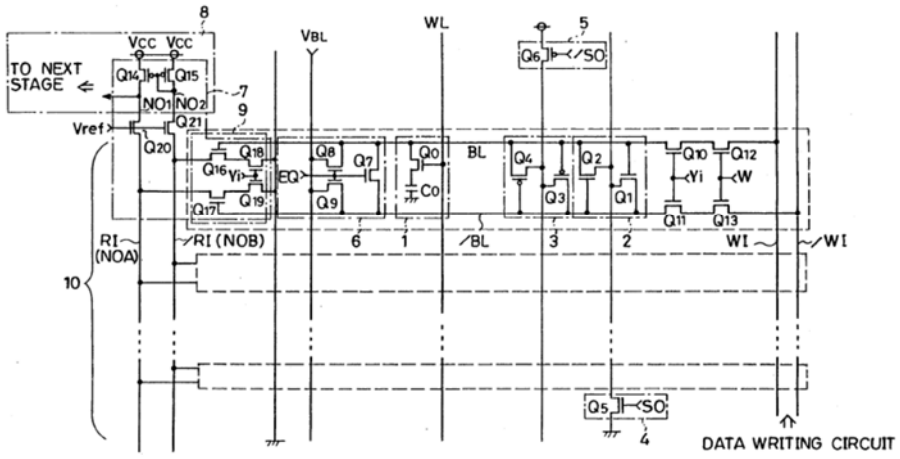


Figure 1 illustrates a "main part" of the device, depicting a pair of bit lines BL and /BL and their associated circuitry. *Id.* at 3:1–5, 7:10–13, Fig. 1. Each bit line pair is associated with n-type sense amplifier 2 and p-type sense amplifier 3. *Id.* at 1:47–52, 7:4–13, Fig. 1. Drive circuit 9, which includes transistors Q_{16}–Q_{19}, is provided for each bit line pair. *Id.* at 7:14–19, Fig. 1. Drive circuit 9 "amplifies the potentials of the associated bit lines." *Id.* Drive circuit 9 "operate[s] to amplify the potentials on bit lines BL and /BL during a read operation, and allow[s] one of read only data lines RI and /RI to be discharged to ground during a read operation." Pet. 33. We agree with Petitioner (Pet. 4) that Hamade qualifies as prior art under at least 35 U.S.C. § 102(e) because Hamade's filing date of August 28, 1992, is before the earliest possible priority date for the '574 patent, which is November 12, 1992. *See* Ex. 1001, at [62]; Ex. 1009, at [22], [45].

4. Independent claim 1

Claim 1 recites: "[i]n an integrated circuit memory having a plurality of bit line pairs." Petitioner asserts that Inoue in combination with Min discloses this limitation. Pet. 21–22.

Inoue discloses a "semiconductor device" in a "dynamic memory." Ex. 1007, 3–4. Inoue discloses an embodiment, illustrated by Figure 6, with multiple sense amplifiers, each comprising a CMOS "F/F" or "latch" that includes a pair of internal nodes "N_1 and N_2 correspond[ing] to bit lines." *Id*. at 4. Inoue discloses that this embodiment "is applied to a sense amp in the dynamic memory." *Id*. Petitioner concedes that Inoue does not expressly disclose a plurality of sense amplifiers or a plurality of bit line pairs corresponding to sense amplifiers. Pet. 23–24.

Min discloses a semiconductor memory device with a plurality of sense amplifiers SA_1–SA_N. Ex. 1008, 1:4–8, Fig. 3B. Each sense amplifier is coupled to a bit line pair (BL_L and BL_R). *Id*. at 2:5–15, Fig. 3B. Each sense amplifier is also coupled to a positive power supply (V_{CC}) via driving transistor $Q10_i$ and to ground (V_{SS}) via driving transistor $Q20_i$. *Id*. at 21:1–13, Fig. 3B. Min discloses a common driving signal from driving transistors $Q10_i$ and $Q20_i$. *Id*. at Fig. 3B.

Petitioner asserts "it would have been obvious to a POSITA to implement *Inoue*'s figure 6 circuit in a multicolumn memory system to create a dynamic memory having a plurality of bit line pairs, each of which is coupled to a respective sense amplifier." Pet. 24. Specifically, Petitioner asserts an ordinarily skilled artisan would have been motivated to implement Inoue's Figure 6 circuitry to implement a multi-column DRAM with multiple sense amplifiers as taught by Min because practical DRAMs had multiple columns. *Id*. at 27. Petitioner asserts an ordinarily skilled artisan would have found it beneficial to use common drive signals for the drive transistors as set forth in Min to reduce the amount of circuitry and, therefore, chip area, when compared to separate clock signals for each latch

circuit. *Id*. Dr. Baker's testimony supports these assertions. Ex. 1002 ¶¶ 34–37, 73, 77. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight.

Petitioner also asserts modifying Inoue's apparatus to use a plurality of sense amplifiers and a plurality of bit line pairs as set forth in Min would have been straightforward for an ordinarily skilled artisan. Pet. 28. Inoue's Figure 6 embodiment describes a single sense amplifier with a single bit line pair and Min discloses a plurality of sense amplifiers, each coupled to respective bit line pairs. *Id.* According to Petitioner, an ordinarily skilled artisan would have understood how to incorporate Inoue's sense amplifier into Min's multi-column memory. *Id.* Petitioner asserts this would have been a predictable combination of known components according to known methods, and would have been consistent with working DRAM features. *Id.* at 29. Dr. Baker's testimony supports these assertions. Ex. 1002 ¶¶ 74, 78. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight.

In an obviousness analysis, there must be articulated reasoning with a rational underpinning to support a conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Petitioner has articulated reasoning with a rational underpinning to support applying Inoue's sense amplifier to a practical multi-column memory because working DRAMs use multi-column arrangements and Min's common driving signals for multiple sense amplifiers and their corresponding bit line pairs would help reduce the amount of circuitry in such a memory, thereby reducing the chip area. Dr. Baker's testimony amply supports this rationale. Ex. 1002 ¶¶ 72–77. We find Dr. Baker's testimony on this point persuasive and afford it

substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations.

Thus, we are persuaded that the combination of Inoue and Min discloses "an integrated circuit memory having a plurality of bit line pairs" and that an ordinarily skilled artisan would have been motivated to combine the teachings of Inoue and Min as proposed by Petitioner.

Claim 1 further recites "a combination comprising a plurality of sense amplifiers." Petitioner asserts that the combined Inoue-Min system discloses this limitation for the reasons set forth with respect to the "integrated circuit memory having a plurality of bit line pairs" limitations. Pet. 29–30. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 79–80. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue and Min discloses "a combination comprising a plurality of sense amplifiers."

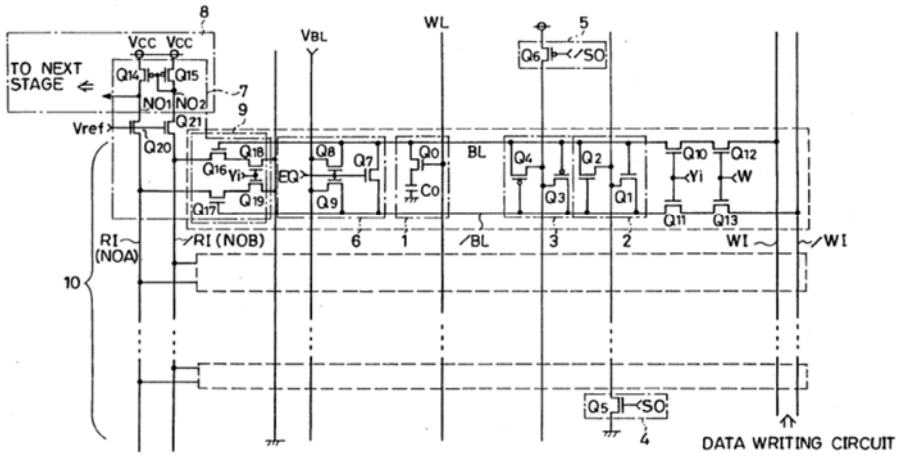
Claim 1 further recites "a plurality of local sense amplifier drive transistors." Petitioner asserts that the combined Inoue-Min system discloses a plurality of sense amplifier drive transistors, where each is associated with only one latch circuit. Pet. 30–31. In particular, Petitioner asserts, "[i]n the combined *Inoue-Min* system, each column has its own driving transistors Q_{P3} and Q_{N10} . . ., and these transistors in respective columns constitute 'a plurality of local sense amplifier drive transistors.'" *Id*. at 31. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶ 81. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary

with respect to these claim limitations. We are persuaded that the combination of Inoue and Min discloses "a plurality of local sense amplifier drive transistors."

Claim 1 further recites "a plurality of local column read amplifiers." Petitioner concedes that "[t]he combined Inoue-Min system does not expressly disclose 'a plurality of local column read amplifiers.'" Pet. 31. However, Petitioner asserts that it would have been obvious to modify the combined Inoue-Min system in view of Hamade to implement a combination comprising a plurality of column read amplifiers with each column read amplifier associated with only one latch circuit. *Id*. at 31–38.

Hamade discloses a semiconductor memory device. Ex. 1009, 1:7–9. Figure 1 of Hamade, shown below, illustrates a "main part" of such a device and depicts a pair of bit lines BL and /BL and their associated circuitry. *Id.* at 3:1–5, 7:4–12, Fig. 1.

FIG. 1



Each bit line pair is associated with n-type sense amplifier 2 and p-type sense amplifier 3. *Id.* at 1:47–52, 7:4–13, Fig. 1. Dr. Baker testifies that an ordinarily skilled artisan would understand that, collectively, these

sense amplifiers form a latch similar to the latch in Inoue's Figure 6. Ex. 1002, ¶ 84.

Hamade also discloses a drive circuit 9 comprised of transistors Q_{16}–Q_{19} is provided for each bit line pair. Ex. 1009, 7:14–19, Fig. 1. Drive circuit 9 "amplifies the potentials of the associated bit lines." *Id*. Petitioner asserts an ordinarily skilled artisan would have understood drive circuit 9 to constitute a "column read amplifier" because drive circuit 9 "operate[s] to amplify the potentials on bit lines BL and /BL during a read operation, and allow[s] one of read only data lines RI and /RI to be discharged to ground during a read operation." Pet. 33 (citing Ex. 1009, 3:61–4:10, 8:8–31, 8:52–54). Petitioner asserts "drive circuit 9 is provided for each **column** because it is provided for each bit line pair (Ex. 1009, 7:22–23), which is 'related to memory cells in one **column** of the memory cell array.' (*Id.*, 1:36–39 (emphasis added), 7:4–9; Ex. 1002 ¶ 87.)." Pet. 34. Dr. Baker's testimony supports these assertions. Ex. 1002 ¶ 87; *see also id.* ¶¶ 82–95. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue and Min discloses "a plurality of local column read amplifiers."

Petitioner also asserts an ordinarily skilled artisan would have been motivated to combine the Inoue-Min system with Hamade's drive circuit at each column because Hamade discloses that "drive circuit 9 [] is provided for each bit line pair." Pet. 35. Petitioner asserts an ordinarily skilled artisan would have known how to assemble and implement all of the relevant circuitry into the combined system without undue experimentation. *Id.* Petitioner asserts an ordinarily skilled artisan would have looked to Hamade

because the combined Inoue-Min system does not disclose read circuitry that would typically be found in a practical DRAM. *Id.* at 37. According to Petitioner, the combined Inoue-Min-Hamade system would allow "fast reading of the data carried by the bit lines." *Id.* at 38. Petitioner asserts the combination would use known components according to known methods to yield predictable results. *Id.*

Patent Owner asserts an ordinarily skilled artisan would not combine Hamade with the Inoue-Min system because the combined system would consume more power, which is contrary to Inoue's express goal of providing a circuit that consumes a small amount of power when sensing. PO Resp. 13–14, 17 (citing Ex. 1007, 3; Ex. 2001 ¶¶ 44–45; Ex. 2003, 75:12–16, 76:5–9, 107:8–108:1). Patent Owner asserts Hamade's high-speed read amplifier uses at least four additional transistors with each bit line pair, increasing current consumption and power requirements compared to a system with a global data path. *Id.* at 14–16 (citing Ex. 1009, 1:8–15, 3:5–7, 7:17–19, 9:55–58; Ex. 2001, ¶¶ 51–53).

In an obviousness analysis, there must be articulated reasoning with a rational underpinning to support a conclusion of obviousness. *In re Kahn*, 441 F.3d at 988. Petitioner has articulated reasoning with a rational underpinning to support applying Hamade's drive circuit 9 to the combined Inoue-Min system, namely adding the drive circuit would allow "fast reading of the data carried by the bit lines." Pet. 38. Dr. Baker's testimony amply supports this rationale. Ex. 1002 ¶¶ 82–95. For example, Dr. Baker testifies an ordinarily skilled artisan would have been motivated to modify the combined Inoue-Min system to implement Hamade's drive circuit 9 because Hamade discloses that drive circuit 9 is provided for each bit line

pair. *Id.* ¶ 88 (citing Ex. 1009, 7:17–18). Dr. Baker testifies an ordinarily skilled artisan would have looked to Hamade to augment and improve the capabilities of the combined Inoue-Min system because Hamade teaches circuitry and functionality applicable to a column of memory such as in the combined Inoue-Min system. *Id.* ¶¶ 93–94. Dr. Baker testifies an ordinarily skilled artisan would have recognized that the combined Inoue-Min system does not disclose read circuitry for reading data carried by bit lines that would typically be found in a practical DRAM, and Hamade discloses such circuitry for reading data at a high rate of speed. *Id.* ¶ 93. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight.

Patent Owner's argument that adding Hamade's drive circuit to the combined Inoue-Min system would defeat the intended purpose of Inoue is unpersuasive for two reasons. First, adding Hamade's drive circuit to the combined Inoue-Min system would not affect Inoue's circuitry that achieves the desired decrease in power consumption. Specifically, Inoue teaches disabling transistors Q_{P3} and Q_{N10} to reduce power consumption during a write operation. Ex. 1013, 116:24–118:3. Inoue teaches that conventional prior art circuits do not have these transistors. *Id.* Petitioner's proposed combination would not modify this portion of Inoue's circuitry, maintaining the reduced power consumption achieved by Inoue's teachings. *See* Reply 11–12. Thus, the proposed combination does not defeat the intended purpose of Inoue because it maintains the circuitry that achieves the desired decrease in power consumption.

Second, even if adding Hamade's drive circuit to the combined Inoue-Min system caused additional power consumption, an ordinarily skilled artisan may embrace this tradeoff to achieve the speed increase taught by

Hamade. The test for obviousness is not whether the goals and objectives of every prior art reference can be accomplished by a proposed combination of prior art teachings. Rather, an ordinarily skilled artisan may be motivated to pursue the desirable properties taught by one prior art reference even if that means foregoing the benefits taught by another prior art reference. *See In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016); *see also Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine."). This is particularly true where, as here, the claims at issue do not require the benefit that is arguably lost in the combination. *See id.* Indeed, a prior art reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect. *EWP Corp. v. Reliance Universal Inc*., 755 F.2d 898, 907 (Fed. Cir. 1985). The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned, as they are a part of the literature and are relevant for all they contain. *In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) (citing *In re Lemelson*, 397 F.2d 1006, 1009 (CCPA 1968)).

Thus, we are persuaded that the combination of Inoue, Min, and Hamade discloses "a plurality of local column read amplifiers" and that an ordinarily skilled artisan would have been motivated to combine the teachings of Inoue, Min, and Hamade as proposed by Petitioner.

Claim 1 further recites "a plurality of local data write driver circuits." Petitioner asserts that the combined Inoue-Min-Hamade system discloses a plurality of data write driver circuits, where each is associated with only one

latch circuit. Pet. 38–39. In particular, Petitioner asserts Q_{N6} and Q_{N8} form one "local data write driver circuit" on the left side of Inoue's Figure 6 and Q_{N7} and Q_{N9} form a second "local data write driver circuit" on the right side of the figure. *Id.* Each of these data write driver circuits is only associated with the sense amplifier depicted in Figure 6. Dr. Baker's testimony supports Petitioner's assertions. Ex. 1002 ¶ 96. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "a plurality of local data write driver circuits."

Claim 1 further recites "each sense amplifier comprising a latch circuit having a pair of internal nodes coupled to a corresponding pair of bit lines, the latch circuit including a pair of P channel transistors and a pair of N channel transistors." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 39–43. In particular, Petitioner asserts

> In the *Inoue-Min-Hamade* combination, each column would have had a corresponding sense amplifier ("each sense amplifier") comprising a flip-flop ("latch circuit") having a pair of internal nodes N_1 and N_2 ("a pair of internal nodes") coupled to a corresponding pair of bit lines, the flip-flop including PMOS transistors Q_{P1} and Q_{P2} ("a pair of P channel transistors") and NMOS transistors Q_{N1} and Q_{N2} ("a pair of N channel transistors").

Id. at 39─40. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 97–100. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that

the combination of Inoue, Min, and Hamade discloses "each sense amplifier comprising a latch circuit having a pair of internal nodes coupled to a corresponding pair of bit lines, the latch circuit including a pair of P channel transistors and a pair of N channel transistors."

Claim 1 further recites "wherein each sense amplifier is connected to a first said local sense amplifier drive transistor having a source-drain path coupled to said P channel transistors of the latch circuit, said first local sense amplifier drive transistor selectively coupling said P channel transistors to a first voltage source." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 43–46. In particular, Petitioner asserts

> In the combined *Inoue-Min-Hamade* system, each column would have had a corresponding sense amplifier ("each sense amplifier") that is connected to a corresponding transistor Q_{P3} ("a first said local sense amplifier drive transistor") having a source-drain path coupled to the transistors Q_{P1}, Q_{P2} ("said P channel transistors of the latch circuit"), transistor Q_{P3} selectively coupling the transistors Q_{P1}, Q_{P2} to V_{DD} ("a first voltage source").

Id. at 43. Dr. Baker's testimony supports Petitioner's assertions. Ex. 1002 ¶¶ 101–104. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "wherein each sense amplifier is connected to a first said local sense amplifier drive transistor having a source drain path coupled to said P channel transistors of the latch circuit, said first local sense amplifier drive transistor selectively coupling said P channel transistors to a first voltage source."

Claim 1 further recites "wherein each sense amplifier is connected to a second said local sense amplifier drive transistor having a source-drain path coupled to said N channel transistors of said latch circuit, said second local sense amplifier drive transistor selectively coupling said N channel transistors to a second voltage." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 46–50. In particular, Petitioner asserts

> In the combined *Inoue-Min-Hamade* system, each column would have had a corresponding sense amplifier ("each sense amplifier") that is connected to a corresponding transistor Q_{N10} ("a second said local sense amplifier drive transistor") having a source-drain path coupled to the transistors Q_{N1} and Q_{N2} ("said N channel transistors of said latch circuit"), transistor Q_{N10} selectively coupling the transistors Q_{N1}, Q_{N2} to ground ("a second voltage").

Id. at 46. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 105–109. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "wherein each sense amplifier is connected to a second said local sense amplifier drive transistor having a source-drain path coupled to said N channel transistors of said latch circuit, said second local sense amplifier drive transistor selectively coupling said N channel transistors to a second voltage."

Claim 1 further recites "a first control line coupled to control the operation of a plurality of said first local sense amplifier drive transistors." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 50–51. In particular, Petitioner asserts

> In the combined *Inoue-Min-Hamade* system, clock ϕ_4 ("a first control line") would have been coupled to control the operation of transistor Q_{P3} in each column ("control the operation of a plurality of said first local sense amplifier drive transistors"). Specifically, clock ϕ_4 would have controlled the turning ON/OFF for each transistor Q_{P3} because when "clock ϕ_4 is made to rise, . . . Q_{P3} is rendered non-conducting."

Id. (citations omitted). Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶ 110. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "a first control line coupled to control the operation of a plurality of said first local sense amplifier drive transistors."

Claim 1 further recites "a second control line coupled to control the operation of a plurality of said second local sense amplifier drive transistors." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 51–52. In particular, Petitioner asserts

> In the combined *Inoue-Min-Hamade* system, clock ϕ_3 ("a second control line") would have been coupled to control the operation of transistor Q_{N10} in each column ("control the operation of a plurality of said second local sense amplifier drive transistors"). Specifically, clock ϕ_3 would have controlled the turning ON/OFF for each transistor Q_{N10} because when "clock ϕ_3 is made to fall, Q_{N10} is made non-conducting."

Id. (citations omitted). Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶ 111. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the

combination of Inoue, Min, and Hamade discloses "a second control line coupled to control the operation of a plurality of said second local sense amplifier drive transistors."

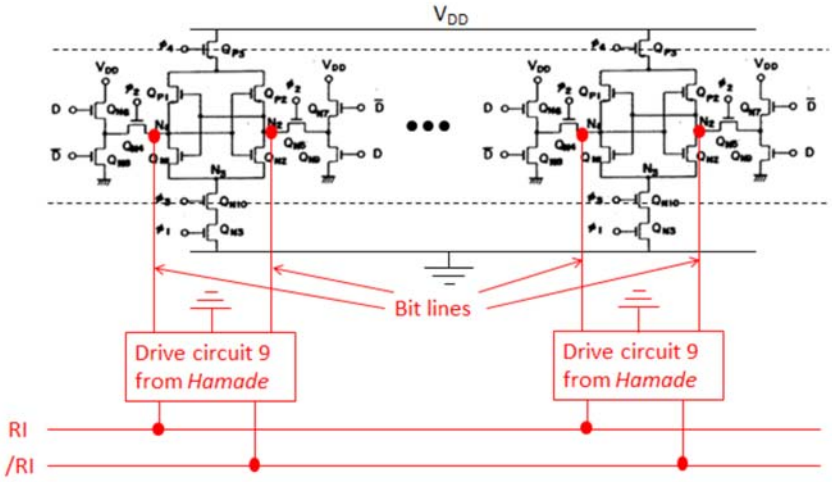
Claim 1 further recites "a first voltage supply line coupled to said plurality of said first local sense amplifier drive transistors." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 52–53. In particular, Petitioner asserts "[i]n the combined *Inoue-Min-Hamade* system, V_{DD} ('a first voltage supply line') would have been coupled to transistors Q_{P3} of respective columns ('said plurality of said first local sense amplifier drive transistors')." *Id.* Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶ 112. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "a first voltage supply line coupled to said plurality of said first local sense amplifier drive transistors."

Claim 1 further recites "a second voltage line coupled to said plurality of second local sense amplifier drive transistors." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 53–54. In particular, Petitioner asserts "[i]n the *Inoue-Min-Hamade* combination, the ground node ('a second voltage supply line') would have been coupled to transistors Q_{N10} of respective columns ('said plurality of second local sense amplifier drive transistors')." *Id.* Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶ 113. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We

are persuaded that the combination of Inoue, Min, and Hamade discloses "a second voltage line coupled to said plurality of second local sense amplifier drive transistors."

Claim 1 further recites "wherein each said column read amplifier is responsively coupled to said internal nodes of said latch circuit of a corresponding sense amplifier." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 54–57. In particular, Petitioner asserts the following, with an annotated figure:

> As is apparent from the annotated figure below, in the combined *Inoue-Min-Hamade* system, each drive circuit 9 (from *Hamade)* as implemented in the combined system would have been responsively coupled to nodes N_1, N_2 for each latch circuit (P-channel transistors Q_{P1}, Q_{P2}, and N-channel transistors Q_{N1}, Q_{N2}) of a corresponding sense amplifier.



Id. at 54–55. The annotated figure shows the combined Inoue-Min-Hamade system, with each drive circuit 9 from Hamade coupled to nodes from the Inoue-Min latch circuit. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 114–116. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not

argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "wherein each said column read amplifier is responsively coupled to said internal nodes of said latch circuit of a corresponding sense amplifier."

Claim 1 further recites "wherein each said sense amplifier is coupled to a pair of said local data write driver circuits." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 57–60. In particular, Petitioner asserts

> *Inoue* discloses that "Q_{N5}, Q_{N7}, Q_{N9} and Q_{N4}, Q_{N6}, Q_{N8} are write circuits that determine the state of the F/F." (Ex.1007, 3, FIG. 6.) The inputs to circuits Q_{N6} and Q_{N8}, and Q_{N7} and Q_{N9}, i.e., "D, $\overline{D}$ [are] write data input terminals used to write data to F/F," where F/F refers to a flip-flop. (*Id.*, 3; Ex.1002, ¶117.) Therefore, a POSITA would have understood that Q_{N6} and Q_{N8}, and Q_{N7} and Q_{N9} constitute a pair of "data write driver circuits."

Id. at 57. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 117–119. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "wherein each said sense amplifier is coupled to a pair of said local data write driver circuits."

Claim 1 further recites "each local data write driver circuit being configured to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 60–63. In particular, Petitioner asserts

> In the *Inoue-Min-Hamade* combination, each pair of transistors Q_{N6}/Q_{N8} or transistors Q_{N7}/Q_{N9} ("each local data write driver circuit") . . . would have been configured to (1) receive data at their gate terminals D and $\overline{D}$ ("receive write data") during a write operation at a gate electrode of a transistor Q_{N6}/Q_{N8} or Q_{N7}/Q_{N9} ("a transistor in said data write driver circuit") in said data write driver circuit, and (2) apply a signal corresponding to a level 'H' or 'L' ("apply a signal") based upon receiving data D or $\overline{D}$ ("based upon receiving said write data") to node N_1 or N_2 of the latch circuit ("one of said latch circuit nodes").

Id. at 60–61. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 120–123. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "each local data write driver circuit being configured to receive write data during a write operation at a gate electrode of a transistor in said data write driver circuit and to apply a signal based upon receiving said write data to one of said latch circuit nodes."

Claim 1 further recites "wherein each said local data write driver circuit is coupled to both a respective one of said internal nodes of its corresponding sense amplifier and a corresponding bit line." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 63–65. In particular, Petitioner asserts

> In the *Inoue-Min-Hamade* combination, each pair of transistors Q_{N6}/Q_{N8} or transistors Q_{N7}/Q_{N9} ("each said local data write driver circuit") for each column would have been coupled to both: 1) one of the internal nodes N_1/N_2 of the sense amplifier of that column ("a respective one of said internal nodes of its corresponding sense amplifier"), and 2) a corresponding bit line of the pair of bit lines associated with that column.

Id. at 63–64. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 124–125. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "wherein each said local data write driver circuit is coupled to both a respective one of said internal nodes of its corresponding sense amplifier and a corresponding bit line."

On these bases, Petitioner submits that the proposed combination of Inoue, Min, and Hamade discloses claim 1. Petitioner has shown, by a preponderance of the evidence, that (1) the combination of Inoue, Min, and Hamade discloses the subject matter of claim 1; and (2) an ordinarily skilled artisan would have combined the teachings of Inoue, Min, and Hamade in the proposed manner. Thus, for the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that claim 1 is unpatentable as obvious over Inoue, Min, and Hamade.

5. Independent claim 30

Claim 30 recites, "[a] sense amplifier arrangement for an integrated circuit memory comprising." Petitioner asserts that the combined Inoue-Min system discloses this limitation. Pet. 74. In particular, Petitioner asserts an ordinarily skilled artisan would have combined Inoue and Min for the reasons discussed above with respect to claim 1. *Id.* Petitioner also asserts:

> *Inoue* discloses "a semiconductor device" comprising a sense amplifier with a flip-flop circuit. (Ex.1007, 1 (Claim 1).) The circuit in figure 6 of *Inoue* is for a sense amplifier in a dynamic memory. (*See id.*, 4; IX.A.1(a); Ex.1002, ¶137.) A POSITA would have understood that "dynamic memory" in *Inoue* refers to a DRAM, which is an integrated circuit memory.

Id. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶ 137. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue and Min discloses "[a] sense amplifier arrangement for an integrated circuit memory comprising."

Claim 30 further recites "for each of a plurality of sense amplifiers: a sense amplifier latch circuit having first and second latch nodes to which respective bit lines may be coupled." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation for the same reasons as discussed above for commensurate limitations in claim 1. Pet. 74–78. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 138–140. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner argues an ordinarily skilled artisan would not have combined Inoue, Min, and Hamade for the same reasons as discussed above with respect to claim 1. PO Resp. 13–17. We are persuaded that the combination of Inoue, Min, and Hamade discloses "for each of a plurality of sense amplifiers: a sense amplifier latch circuit having first and second latch nodes to which respective bit lines may be coupled" for the reasons discussed above for claim 1. We are also persuaded that an ordinarily skilled artisan would have been motivated to combine the teachings of Inoue, Min, and Hamade as proposed by Petitioner for the same reasons as discussed above with respect to claim 1.

Claim 30 further recites

> a local column read amplifier having transistors responsively coupled to at least one of said first and second

> latch nodes, and receiving at least one data read signal, said local read amplifier being configured to control the current of said data read signal based on the state of said one latch node.

Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 78–81. In particular, Petitioner asserts that in the combined system, "for each sense amplifier in a respective column, there is a corresponding drive circuit 9 ('local column read amplifier')." Pet. 79–80. Petitioner also asserts

> drive circuit 9, as combined with *Inoue-Min*, would have included the gates of NMOS transistors Q16 and Q17 . . . coupled to nodes N1 and N2 of figure 6 of *Inoue*, respectively, because gates of transistors Q17 and Q16 in drive circuit 9 receive the bit line signals (Ex.1009, FIG. 1), and *Inoue*'s N1 and N2 correspond to bit lines.

Id. at 80. Petitioner also asserts "the drive circuit 9 ('local column read amplifier') would receive signals on read only data lines RI and /RI ('receiving at least one data read signal') in the combined system." *Id.* Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 141–145. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses

> a local column read amplifier having transistors responsively coupled to at least one of said first and second latch nodes, and receiving at least one data read signal, said local read amplifier being configured to control the current of said data read signal based on the state of said one latch node.

Claim 30 further recites "first and second local data write driver circuits, each being configured to receive a respective data signal at a

respective gate electrode of first write driver transistors in said first and second local data write driver circuits." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 82–83. In particular, Petitioner asserts

> Each of th[e] data write driver circuits at each column in the combined *Inoue-Min-Hamade* system would have been configured to receive data at terminals D and $\overline{D}$ (either of which is "a respective data signal") coupled to a respective gate electrode of transistors Q_{N6}/Q_{N8} and Q_{N7}/Q_{N9} ("at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits") as shown in figure 6 of *Inoue*.

Id. at 82. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 146–147. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "first and second local data write driver circuits, each being configured to receive a respective data signal at a respective gate electrode of first write driver transistors in said first and second local data write driver circuits."

Claim 30 further recites "said first and second data write driver circuits being coupled to said first and second latch nodes to provide signals based on said respective data signal to said first and second latch nodes during a writing operation." Petitioner asserts that the combined Inoue-Min-Hamade system discloses this limitation. Pet. 84–86. In particular, Petitioner asserts that in the combined system:

> for each sense amplifier, the circuit comprising transistors Q_{N6} and Q_{N8} and the circuit comprising transistors Q_{N7} and Q_{N9} ("said first and second data write driver circuits") . . . would have been

> coupled to nodes N_1 and N_2 ("said first and second latch nodes") . . . to provide signals corresponding to level 'H' and level 'L' ("signals") based on data at terminals D and $\overline{D}$ ("based on said respective data signal") to nodes N_1 and N_2, respectively, ("to said first and second latch nodes") during a writing operation, as shown below in figure 6 of *Inoue*.

Id. at 84. Dr. Baker's testimony supports Petitioner's assertion. Ex. 1002 ¶¶ 148–149. We find Dr. Baker's testimony on this point persuasive and afford it substantial weight. Patent Owner has not argued anything to the contrary with respect to these claim limitations. We are persuaded that the combination of Inoue, Min, and Hamade discloses "said first and second data write driver circuits being coupled to said first and second latch nodes to provide signals based on said respective data signal to said first and second latch nodes during a writing operation."

On these bases, Petitioner submits that the proposed combination of Inoue, Min, and Hamade discloses claim 30. Petitioner has shown, by a preponderance of the evidence, that (1) the combination of Inoue, Min, and Hamade discloses the subject matter of claim 30; and (2) an ordinarily skilled artisan would have combined the teachings of Inoue, Min, and Hamade in the proposed manner. Thus, for the foregoing reasons, Petitioner has shown, by a preponderance of the evidence, that the subject matter of claim 30 as a whole is unpatentable as obvious over Inoue, Min, and Hamade.

6. Dependent claims 2, 3 and 31–37

Each of claims 2 and 3 depends from claim 1; and each of claims 31–37 depends, directly or indirectly, from claim 30. In the Petition, Petitioner accounts for the added limitation of claim 2 relative to base claim 1. Pet.

65–71. Petitioner also accounts for the added limitation of claim 3 relative to base claim 2. *Id.* at 71–74. Petitioner accounts for the added limitation of claim 31 relative to base claim 30. *Id.* at 86–89. Petitioner accounts for the added limitation of claim 32 relative to base claim 31. *Id.* at 89–91. Petitioner accounts for the added limitations of claims 33 and 34 relative to base claim 32. *Id.* at 91–96. Petitioner also accounts for the added limitation of claim 35, relative to base claim 30, the added limitation of claim 36, relative to base claim 35, and the added limitation of claim 37, relative to base claim 36. *Id.* at 96–108.

Each of Petitioner's positions set forth above are supported by the testimony of Dr. Baker. Ex. 1002 ¶¶ 126–132 (claim 2), ¶¶ 133–136 (claim 3), ¶¶ 150–151 (claim 31), ¶¶ 152–153 (claim 32), ¶¶ 154–156 (claim 33), ¶¶ 157–160 (claim 34), ¶¶ 44–47, 161–164 (claim 35), ¶¶ 165–170 (claim 36), and ¶¶ 171–175 (claim 37).

Patent Owner has provided no counterargument to Petitioner's arguments and assertions about the obviousness of claims 2, 3, and 31–37 over Inoue, Min, and Hamade. We are persuaded that Petitioner has adequately accounted for the limitations added by each of claims 2, 3 and 31–37, and that Petitioner has shown how the combination satisfies each of the dependent claims. Petitioner has shown, by a preponderance of the evidence, that each of claims 2, 3, and 31–37 is unpatentable as obvious over Inoue, Min, and Hamade.

III. CONCLUSION

Petitioner has shown, by a preponderance of the evidence, that claims 1–3 and 30–37 are unpatentable under 35 U.S.C. § 103(a) as obvious over Inoue, Min, and Hamade.

IV. ORDER

It is

ORDERED that claims 1–3 and 30–37 of the '574 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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