UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.

Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,

Patent Owner.

Case IPR2017-01597
Patent No. 6,023,085

PATENT OWNER'S NOTICE OF APPEAL

Notice is hereby given, pursuant to 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a) and 90.3(a), that Patent Owner Lone Star Silicon Innovations, LLC hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered on January 16, 2019 in IPR2017-01597 (Paper 26) (attached hereto as Exhibit A), and from all underlying orders, decisions, rulings, and opinions that are adverse to Patent Owner, including, without limitation, those within the Decision on Institution of *Inter Partes* Review, entered on January 17, 2018 (Paper 8).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, the Board's claim constructions, the Board's determination that claims 1, 3, 6, and 7 are unpatentable as obvious over the first embodiment of Japanese Patent No. JP H8-64703 (hereinafter "Hemink") and that claim 4 is unpatentable as obvious over the first embodiment of Hemink combined with the teachings of Japanese Patent No. JP H8-64787 (hereinafter "Shudo"), and all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions; the Board's consideration and analysis of the expert testimony, prior art, and other evidence in the record; and the Board's factual findings, conclusions of law, or other determination supporting or relating to the above issues.

This Notice of Appeal is timely pursuant to 37 C.F.R. § 90.3, having been duly filed within 63 days after the Final Written Decision.

A copy of the Notice of Appeal is being filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice of Appeal is being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit, and the required docketing fee will be paid electronically using pay.gov.

If there is any fee due in connection with the filing of this Notice of Appeal, please charge the fee to Deposit Account No. 06-1135.

Respectfully submitted,

Date: March 20, 2019

/Timothy P. Maloney/
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that, pursuant to 37 C.F.R. §§ 42.6(e)(4) and 90.2, the foregoing PATENT OWNER'S NOTICE OF APPEAL and all accompanying documents, were filed by Express Mail on March 20, 2019, with the Director of the United States Patent and Trademark Office, at the following address:

Director of the U.S. Patent and Trademark Office c/o
Office of the General Counsel
P.O. Box 1450
Alexandria, VA 22313-1450

and that a copy of the foregoing Patent Owner's Notice of Appeal and accompanying documents was filed with the Patent Trial and Appeal Board electronically on March 20, 2019, pursuant to 37 C.F.R. 42.6(b)(1), and that the foregoing Notice of Appeal and accompanying documents were served upon the Petitioner pursuant to 37 C.F.R. 42.6(e)(1) via electronic mail on March 20, 2019, by serving the following attorneys of record as follows:

Jeremy Jason Lang
Jared Bobrow
ORRICK, HERRINGTON & SUTCLIFFE LLP
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The undersigned further certifies that a copy of the foregoing Patent Owner's Notice of Appeal and accompanying documents was filed on March 20, 2019 with the United States Court of Appeals for the Federal Circuit through the Court's

CM/ECF filing system and that the filing fee is being paid electronically using pay.gov.

Date: March 20, 2019

/Timothy P. Maloney/
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Exhibit A

Trials@uspto.gov
571-272-7822

Paper No. 26
Entered: January 16, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01597
Patent 6,023,085

Before KRISTINA M. KALAN, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") to institute *inter partes* review of claims 1, 3, 4, 6, and 7 ("the challenged claims") of U.S. Patent No. 6,023,085 B2 (Ex. 1001, "the '085 patent") on multiple grounds. Lone Star Silicon Innovations, LLC,[1] ("Patent Owner") filed a Preliminary Response (Paper 7). Upon consideration of the Petition and Preliminary Response, we instituted review of the challenged claims of the '085 patent on only some of the grounds raised in the Petition. Paper 8, 3, 31 ("Dec. Inst.").

Patent Owner filed a Response to the Petition, addressing the patentability of the challenged claims on those grounds on which we instituted review. Paper 11 ("PO Resp."). Subsequent to Patent Owner's Response, the Supreme Court issued its decision in *SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018), holding that *inter partes* review may not be instituted on fewer than all claims challenged in a petition. The Director has interpreted the *SAS* decision to require the Board to institute review on all claims challenged in a petition based on all grounds raised in the petition.[2] We, therefore, modified our Institution Decision to include review of the challenged claims based on all grounds raised in the Petition. *See* Paper 12, 3. Patent Owner filed a Supplemental Response limited to addressing these additional grounds. Paper

[1] Lone Star Silicon Innovations, LLC also identifies Longhorn IP LLC as a real party-in-interest. Paper 3, 1.

[2] *See* Guidance on the Impact of SAS on AIA Trial Proceedings (April 26, 2018) (available at https://www.uspto.gov/patents-applicationprocess/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial).

15 ("PO Supp. Resp."). Petitioner filed a Reply to the Response and Supplemental Response. Paper 17 ("Pet. Reply"). Pursuant to the parties' agreement and the Board's prior authorization (Ex. 2015), Patent Owner filed a Sur-Reply to Petitioner's Reply. Paper 18. Pursuant to the same agreement and authorization, Petitioner filed a Reply to Patent Owner's Sur-Reply. Paper 22. We held an oral hearing on October 11, 2018, and the hearing transcript is included in the record. *See* Paper 25 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This is a Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons set forth below, we find Petitioner has shown by a preponderance of the evidence that claims 1, 3, 4, 6, and 7 of the '085 patent are unpatentable.

B. Related Matters

Patent Owner identifies the following pending federal court proceedings as matters that could affect, or be affected by, a decision in this proceeding: *Lone Star Silicon Innovations LLC, v. Micron Tech., Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc..,* Appeal No. 2018-1578 (Fed. Cir., filed Feb. 15, 2018). Paper 24, 2–3.

C. Evidence Relied Upon[3]

References		Publication Date	Exhibit
Hemink	JP H8-64703	March 8, 1996	1005

[3] Petitioner also relies upon the Declaration (Ex. 1003) and Reply Declaration (Ex. 1025) of Sanjay Banerjee, Ph.D. Patent Owner relies upon the Declaration (Ex. 2007), Supplemental Declaration (Ex. 2012), and Second Supplemental Declaration (Ex. 2016) of W. R. Bottoms, Ph.D.

References		Publication Date	Exhibit
Shudo	JP H8-64787	March 8, 1996	1006
Tsunoda	JP H8-306889	Nov. 22, 1996	1007

D. Instituted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Reference(s)	Basis	Claim(s) Challenged
Hemink	§ 103(a)	1, 3, 6, and 7
Hemink and Shudo	§ 103(a)	4
Tsunoda	§ 103(a)	1, 3, and 7
Tsunoda and Shudo	§ 103(a)	4
Tsunoda and Hemink	§ 103(a)	6

II. ANALYSIS

A. The '085 Patent

The '085 patent is directed toward a method of manufacturing a NAND-type flash memory device, and the resulting structure of the device. Ex. 1001, 2:57–63. The structure of a prior art NAND-type flash memory device is shown in Figures 1A–1C of the '085 patent. It consists of a substrate having a high density core region surrounded by a low density peripheral region. *Id.* at 1:19–25. The high-density core region contains an array of individually addressable floating-gate type memory cells, and the low-density peripheral region contains input/output circuitry for selectively addressing the memory cells in the memory cell array. *Id.* at 1:25–34. The high density core region is shown in Figures 1B and 2B of the '085 patent, which are reproduced below.

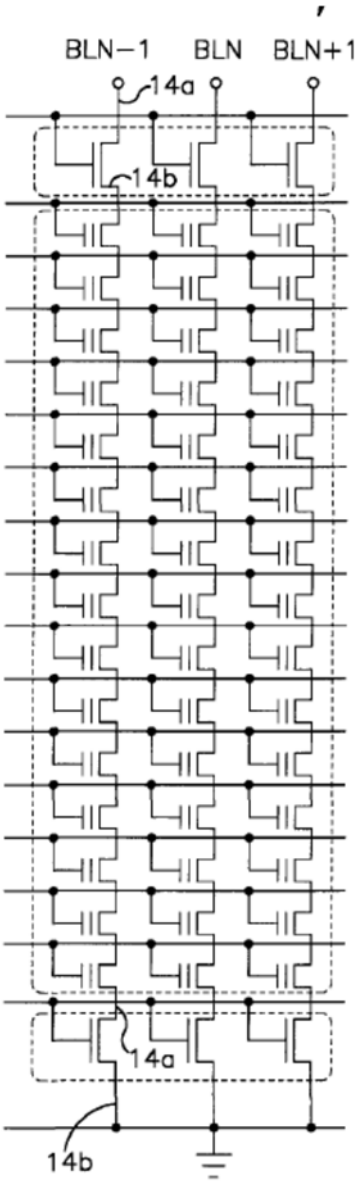


FIGURE 1B

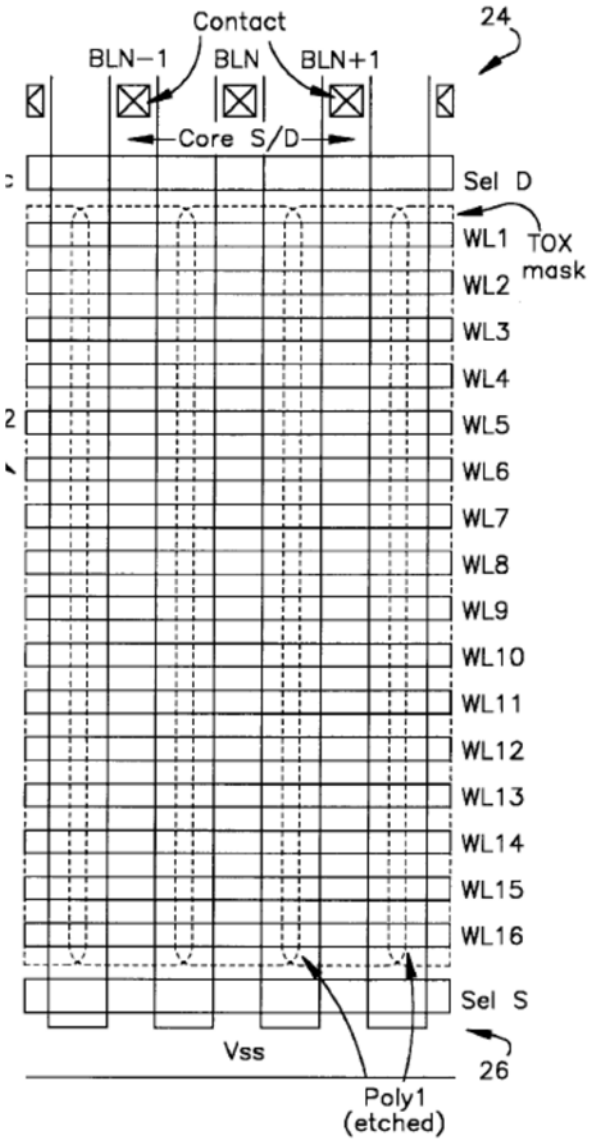


FIGURE 2B

Figure 1B is a plan view of a "prior art NAND-type flash memory circuit," and Figure 2B is a "plan layout view of the core portion of the NAND-type flash memory device of FIG. 2a." Id. at 3:30–31, 3:36–37. Each memory cell 14 in the memory cell array has drain 14a, source 14b, and stacked gate 14c. *Id*. at 1:38–39, Fig. 1C. Each column of the memory cell array consists of a string of memory cells connected in series, including a drain select transistor at one end

of the series and a source select transistor at the other end of the series. *Id.* at 1:40–43. The drains 14a of the drain select transistors of respective columnar memory cell strings are coupled to corresponding bit lines as shown (e.g., BLN-1, BLN, BLN+1), and the sources 14b of the source select transistors of respective columnar memory cell strings are coupled to a common source line Vss. *Id.* at 1:42–46, Fig. 1B; Fig. 2B. For each row of the memory cell array, a common word line (e.g., WL1 . . . WL16) couples the stacked gates 14c of the memory cells across all of the columns of the memory cell array in the respective row. *Id.* at 1:43–44, Fig. 1B; *see also* Fig. 2B.

The ’085 patent discloses that the source and drain select transistors can have a stacked gate structure similar to the individual memory cells in the memory cell array. *Id.* at 5:6–11, Figs. 3A, 3B. A select gate transistor having a stacked gate structure is shown in Figure 3B of the ’085 patent, which is reproduced below.

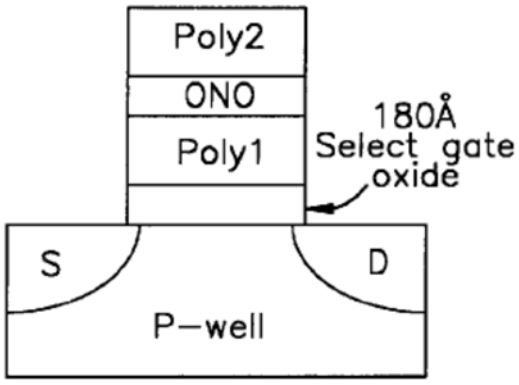


FIGURE 3B

Figure 3B is a cross-sectional view of a select gate transistor having a stacked gate structure. *Id.* at 3:40–42, 5:47–50. The select gate transistor consists of a source (S), a drain (D), a P-well in a silicon substrate, and a stacked gate structure consisting of a gate oxide, a first polysilicon layer (“poly1”), an oxide-

nitride-oxide ("ONO") dielectric layer, and a second polysilicon layer ("poly2"). *Id.* at Fig. 3B; *see also id.* at 1:51–65, Fig. 1C (describing and showing stacked gate structure of prior art memory cell). Despite its stacked gate structure, the select gate transistor functions like a conventional MOS transistor because the first and second polysilicon layers (i.e., poly1 and poly2, respectively) are short-circuited. *Id.* at 3:40–42, 5:15–21, 5:47–50. According to the '085 patent, a dual core cell oxide process is used to form the memory cell oxides and the select gate transistor oxides, which have different thicknesses. *Id.* at 4:61–67, 5:23–30.

The '085 patent further discloses an improved structure and process for manufacturing a NAND-type flash memory device. In particular, it suggests fabricating "a new core cell structure [that] eliminates a stacked gate structure for the select gate transistors while eliminating a core dual oxide manufacturing step." Ex. 1001, 1:7–12. This fabrication method "simplifies the process, eliminates associated tunnel oxide reliability concerns and shrinks the size of the select gate transistor by eliminating the need for a poly1 contact." *Id.* at 1:12–16. A select gate transistor fabricated according to the disclosed method has "a structure like that of the periphery low voltage transistor and is fabricated using essentially the same steps as those used in fabricating the periphery low voltage transistor." *Id.* at 2:57–63. The structures of a memory cell, select gate transistor, low voltage transistor, and high voltage transistor formed according to this method are shown in Figures 7A–7D of the '085 patent, which are reproduced below.

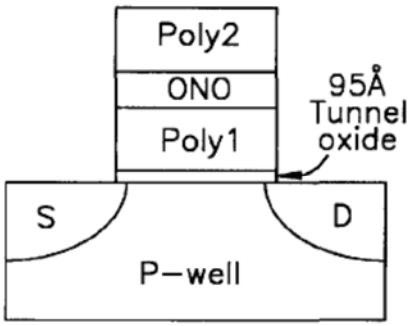


FIGURE 7A

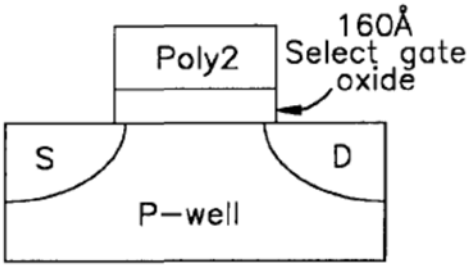


FIGURE 7B

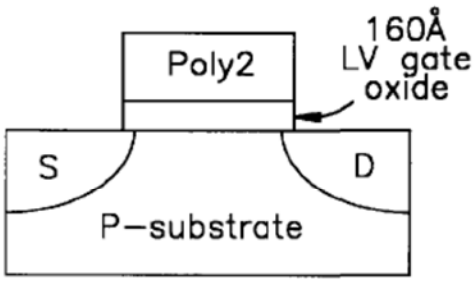


FIGURE 7C

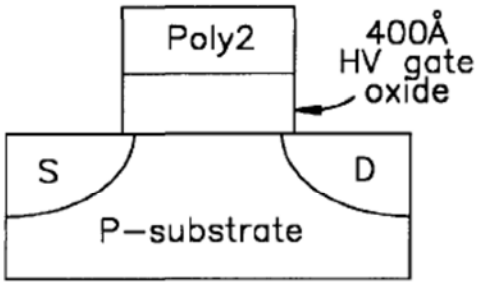


FIGURE 7D

Figures 7A–7D, respectively, are cross-sectional views of a stacked gate flash memory cell, a select gate transistor, a low voltage transistor, and a high voltage transistor, fabricated according to a process described in the '085 patent. *Id.* at 3:59–67. The gate structure of the stacked gate flash memory cell shown in Figure 7A consists of a thin tunnel oxide layer, a poly1 layer, an ONO dielectric layer, and a poly2 gate. The gate structures of the select gate and low voltage transistors, respectively shown in Figures 7B and Figure 7C, are identical, and consist of a gate oxide that is thicker than the tunneling gate oxide of the memory cell and a poly2 gate. The gate structure of the high voltage transistor shown in Figure 7D consists of an even thicker gate oxide layer and a poly2 gate.

Of the challenged claims, claims 1 and 7 of the '085 patent are independent. The other challenged claims depend directly from claim 1. Claim 1 is reproduced below.

> 1. A NAND-type flash memory device, comprising:
>
> a core region comprising a stacked gate flash memory cell structure and a select gate transistor; and
>
> a periphery region comprising a low voltage transistor and a high voltage transistor, wherein the select gate transistor and the low voltage transistor both have a gate oxide layer and a gate electrode layer,
>
> wherein a thickness of the gate oxide layer of the select gate transistor and the low voltage transistor are substantially the same, and a thickness of the gate electrode layer of the select gate transistor and the low voltage transistor are substantially the same.

Ex. 1001, 11:18–29. Claim 3 depends from claim 1, and requires the stacked gate flash memory cell to have a tunnel oxide layer, a floating gate layer over the tunnel oxide layer, an insulating layer over the floating gate layer, and a control gate layer over the insulating layer. *Id.* at 11:32–12:2. Claim 7 is an independent claim, having substantially the same scope as claim 3. *Compare id.* at 12:15–34, *with id.* at 11:18–29, 11:32–12:2 (where the poly1 layer of claim 7 is the floating gate layer of claim 3 and the poly2 layer of claim 7 is the control gate layer of claim 3).

B. Claim Construction

The '085 patent has expired, and its claims cannot be amended. For claims of an expired patent, the Board's claim construction analysis mirrors a district court's analysis. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Accordingly, the Board generally construes the claims to have their

ordinary and customary meaning as understood by one of ordinary skill in the art in the context of the entire patent disclosure. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005). Only claim terms which are in controversy need be construed and only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner and Patent Owner propose differing constructions for various claim terms as further discussed below.

1. core region

Petitioner argues this term means "the region of the memory device that contains a stacked flash memory cell structure and a select gate transistor." Pet. 16. We declined to construe this term in our Institution Decision because express construction was not necessary to resolve any dispute between the parties. Dec. Inst. 8–9. Neither party disputes that determination, which we maintain here. *See* PO Resp. 19–20; Reply 3–16.

2. plurality of select gate transistors [that] share a common conductive gate region to form a select gate word line

Petitioner argues this term should be construed to include a plurality of select gate transistors having a conductive member lying on their gates because this is the only embodiment disclosed in the '085 patent. Pet. 45 (citing Ex. 1001, 1:36–50, 7:49–8:29, Figs. 2B, 6B). We construed this limitation in our Institution Decision to include "a plurality of select gate transistors whose gates are tied to a common conductive member, such as a bus, interconnect or circuit board trace." Dec. Inst. 14–15. Patent Owner disputes that construction. PO Resp. 34–37. Moreover, Patent Owner argues that express construction is not necessary because Patent Owner's arguments for the patentability of claim

6, which includes this claim term, do not depend on the meaning of this term. *Id.* at 33–34 ("Neither the Petitioner nor the Board has identified any controversy that needs resolution, let alone how the construction resolves that controversy. Neither LSSI's preliminary response nor the instant paper offers any independent argument related to claim 6.").

We agree with Patent Owner that the precise meaning of this term is not necessary to resolve any dispute between the parties. In particular, Patent Owner does not dispute Petitioner's contention that Hemink teaches a NAND-type flash memory device that includes a plurality of select gate transistors that "share a common conductive gate region to thereby form a select gate word-line" as recited in claim 6. *See* Pet. 44–48, 83–85; PO Resp. 53; PO Supp. Resp. 14, 23. Accordingly, although we provided a preliminary construction for this term in our Institution Decision, we do not reach a final determination on its construction because doing so is not necessary to render this Final Written Decision. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'")).

3. select gate transistor

Petitioner argues the term "select gate transistor" means "a select gate transistor that (a) is not formed using a dual core oxide process and (b) is not of a stacked gate structure with multiple polysilicon layers." Pet. 16. Petitioner argues this is so because "[t]he purported invention of the '085 patent *is* a flash memory structure and method of fabrication wherein the 'core cell structure eliminates a stacked gate transistor structure for the select gate transistors,' and eliminates 'a core dual oxide manufacturing step.'" *Id.* at 17 (quoting Ex. 1001,

1:7–16; citing Ex. 1003 ¶¶ 55–59). Petitioner further argues the inventor disclaimed any broader interpretation for this claim term during prosecution by arguing that the claims were patentable because "[t]he present invention . . . eliminates the need for a dual core oxide process. . . . In addition, the device eliminates the stacked gate structure for the select gate transistors. . . ." *Id.* at 18 (quoting Ex.1002, 79–80).

Patent Owner argues "[n]either the specification nor the prosecution history of the '085 patent manifests clear and unmistakable exclusion of a stacked gate structure from the invention." PO Resp. 20–21. Patent Owner argues the Specification describes "the elimination of dual core oxide process steps and the elimination of stacked gate select gate structures as two separate 'aspect[s] of the present invention'" that "confer distinct benefits and can be practiced separately." *Id.* at 22–23 (citing Ex. 1001, 4:11–45, 4:25–29, 4:39–45; Ex. 2002 ¶ 50). Patent Owner further argues the statements made by the patentee during prosecution merely provide context for the invention, do not address specific claim limitations, and describe "eliminating the dual core oxide process and eliminating the stacked select gate structure as having ***separate*** advantages over . . . the conventional process." *Id.* at 27 (citing Ex. 1002, 79–80). Therefore, Patent Owner argues, no claim scope has been disclaimed, and "select gate transistor" means "a transistor configured to enable transistors in a bit line." *Id.* at 20, 28 (citing Ex. 1001, 1:34–46, 4:50–59; Ex. 2007 ¶¶ 43–44).

In our Institution Decision, we agreed with Petitioner that Patent Owner disavowed select gate transistors having a stacked gate structure, and construed "select gate transistor" to mean "a transistor that enables transistors in a memory array bit line that does not have a stacked gate structure." *See* Dec. Inst. 9–13. This decision was based, in part, on our preliminary understanding

that the NAND-type flash memory device shown in Figures 3A–3D of the '085 patent, in which the select gate transistor does have a stacked gate structure, was a description of a conventional or prior art NAND-type flash memory device. *See id*. at 4 ("The structures of a conventionally made memory cell, select gate transistor, low voltage transistor, and high voltage transistor are shown in Figures 3A-3D, which are reproduced below."). Unlike Figures 1A and 1C, however, Figures 3A–3D are not identified as prior art in the '085 patent. Moreover, the '085 patent states "[t]he present invention may best be understood and its advantages appreciated in conjunction with the core structure and process of FIGS. 2*a*–5*k*," a range of figures that includes Figure 3B depicting the structure of a stacked gate select gate transistor. This suggests that the patentee sought to distinguish the flash memory device shown in Figures 2*a*–5*k*, from the prior art flash memory device shown in Figures 1A–1C, and that the patentee may not have disavowed select gate transistors having a stacked gate structure in the Specification of the '085 patent.

Given the discussion above, it is not clear whether the patentee has disavowed select gate transistors having a stacked gate structure. Regardless, we need not decide that issue to resolve the parties dispute because Petitioner argues the prior art teaches a NAND-type flash memory device having a "select gate transistor" regardless of whether such disavowal has occurred. *See* Pet. 31–32 (contending that Hemink's first and second embodiments disclose "select gate transistors" that respectively have, and do not have, stacked gate structures). Hemink's first and second embodiments are shown in Figures 2(f) and 8(e), respectively, which are reproduced below.

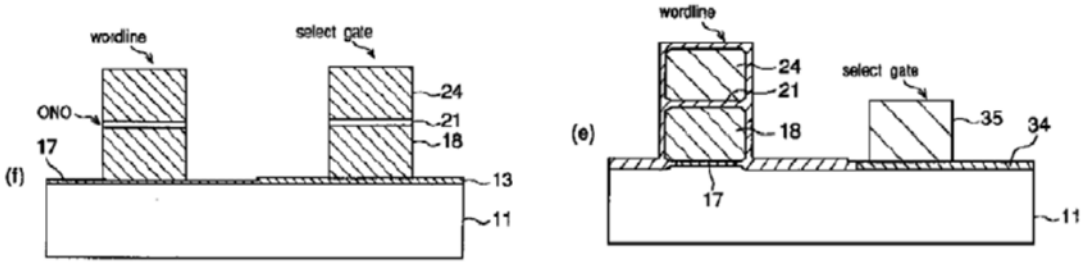


Figure 2(f) of Hemink (shown on the left) is a cross-sectional view of a "memory cell [wordline] and select gate [transistor] in the bitline direction of the EEPROM in embodiment example 1," in which the select gate transistor has a stacked gate structure consisting of gates 18 and 24. *See* Ex. 1005, 8, Fig. 2(f). Figure 8(e) of Hemink (shown on the right) is a cross-sectional view of a "memory cell [wordline] and select gate [transistor] in the bitline direction of the EEPROM in embodiment example 2," in which the select gate transistor does not have a stacked gate structure, i.e., it has a single gate 35.

During oral argument, Petitioner confirmed that its unpatentability positions in this case do not depend on its proposed construction of "select gate transistor."

> JUDGE ROESEL: So Petitioner is not relying on its proposed construction for a select gate transistor to support its positions in this case. Is that -- I mean, Petitioner contends that the claims are obvious regardless of which construction we adopt.
>
> MR. LANG: That's right. That's right, Your Honors.

Tr. 29:22–25.

As discussed above, Patent Owner argues the full scope of the term "select gate transistor" should not be limited because no claim scope was disavowed in the Specification of the '085 patent or during prosecution. PO

Resp. 20–28. Like Petitioner, however, Patent Owner does not rely upon its proposed construction for "select gate transistor" for any position it advocates in this proceeding. *See* Tr. 19:1–5 (Patent Owner concedes that the purpose of advocating a broader construction is not for these proceedings).

Accordingly, although we provided a preliminary construction for the term "select gate transistor" in our Institution Decision, we do not reach a final determination on the construction of that term because resolving its construction is not necessary to render this Final Written Decision. *See, e.g.*, *Nidec Motor*, 868 F.3d at 1017 ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'").

4. low/high voltage transistor

Petitioner argues a "low voltage transistor" is "a transistor having an operating voltage less than that of the high voltage transistor," and a "high voltage transistor" is "a transistor having an operating voltage higher than that of the low voltage transistor." Pet. 19. At the oral hearing, Petitioner revised its proposed constructions, arguing that a "low voltage transistor" is a "transistor designed to operate on a low voltage regime," and a "high voltage transistor" is a "transistor designed to operate on high voltage regime." Tr. 26:22–27:7. Patent Owner argues a "low voltage transistor" is "a transistor used for low voltage logic operations," and a "high voltage transistor" is "a transistor used for relatively higher voltage operations on a memory cell." PO Resp. 29.

In our Institution Decision, we declined to construe the terms "low voltage transistor" and "high voltage transistor" because no construction was necessary to resolve a dispute between the parties. Dec. Inst. 13–14. Petitioner does not contest that decision, but seeks clarification of a preliminary

construction we provided in a related case. *See* Reply 12–16 (seeking clarification of a preliminary construction of low/high voltage transistors provided in *Toshiba Corp. v. Lone Star Silicon Innovations, Inc.*, Case IPR2018-00056, Paper 8, *slip op*. at 11–14 (PTAB, May 1, 2018)).[4] Patent Owner argues the terms "low voltage transistor" and "high voltage transistor" require construction to resolve Patent Owner's contention that Hemink fails to "describe the operational uses of any transistor in its device" and fails to provide any "description of using a specific transistor for the programming/erasing of memory cells." PO Resp. 29, 48–49.

We find constructions of the terms "low voltage transistor" and "high voltage transistor" are not necessary to resolve any dispute between the parties in this proceeding. First, the parties do not dispute that Hemink's flash memory device includes a low voltage transistor. *See* Pet. 32–34; *see also* PO Resp. 40–58. Thus, we need not construe this term.

Second, although the parties dispute whether Hemink's device includes a high voltage transistor, that dispute can be resolved without expressly construing this term. Indeed, despite the differences in their proposed constructions, the parties and their respective experts agree that a person of ordinary skill in the art would have known that high voltage transistors in NAND-type flash memory devices were transistors used to program and erase memory cells. *See* Pet. 32–33 (citing Ex. 1003 ¶¶ 95–98) (a person of ordinary skill in the art would have known that "high voltage transistors are used in the programming/erasing of memory cells, and this process requires boosted voltages of 18 or 20 volts"); *see also* PO Resp. 30 (citing Ex. 2007 ¶ 57) (a

[4] Case IPR2018-00056 has been terminated due to settlement.

person "skilled in the art would understand that . . . high voltage transistors are used for relatively higher voltage operations on a memory cell"). The parties' dispute over Hemink does not concern whether Hemink discloses a transistor that performs the *functions or operations* of a high voltage transistor in a flash memory device. Rather the parties' dispute is whether Hemink discloses or suggests a high voltage transistor *structure* at all, and if it does, whether that structure is located in the periphery region of the device. To resolve this dispute, it is not necessary to construe the term "high voltage transistor."

Accordingly, for the reasons discussed above, we need not expressly construe the meaning of the terms "low voltage transistor" and "high voltage transistor" because doing so is not necessary to resolve any dispute between the parties that is needed to render this Final Written Decision. *See, e.g.*, *Nidec Motor*, 868 F.3d at 1017.

C. Level of Ordinary Skill in the Art

Petitioner and Patent Owner agree on the qualifications of a person of ordinary skill in the art at the time of the invention. Pet. 20 (citing Ex. 1003 ¶ 19); PO Resp. 15–16. Such a person would have had a Bachelor of Science degree in electrical engineering, computer engineering, physics, or a closely related field and at least 5 years of experience in the design and fabrication of semiconductor devices, or a more advanced degree in one of these fields and fewer years of experience. *Id.* We adopted this definition in our Institution Decision, and neither party objects to that finding, which we maintain for purposes of this Final Decision. Dec. Inst. 16.

D. Overview of the Prior Art

1. Hemink

Hemink is a published Japanese Patent Application that discloses a method of making a NAND-type electrically erasable programmable read-only memory (EEPROM). Ex. 1005 ¶¶ 1–2, 15–16. The memory consists of an array of memory cells shown in planar view in Figure 13. A cross-sectional view of a column of memory cells in that array is shown in Figure 14(a), which is reproduced below.

(FIG. 14)

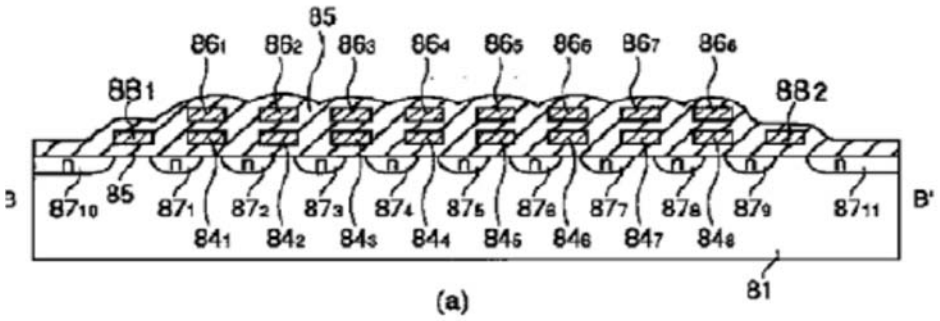


Figure 14(a) is a cross-sectional view of one column of a NAND-type memory cell array. *Id.* ¶ 2. The column consists of a plurality of stacked gate memory cells M1–M8 connected in series with a pair of select gate transistors S1 and S2 at each end of the series. *Id.* ¶ 3, Figs. 13, 14(a). Each memory cell consists of a stacked gate transistor with control gate 86_i (e.g., 86_4) and floating gate 84_i (e.g., 84_4). Each select gate transistor consists of a single control gate 88_j (e.g., 88_1). *Id.*

As discussed in § II.B.3, *supra*, Hemink discloses two embodiments for a NAND-type flash memory device—a first embodiment having a stacked gate select gate transistor, and a second embodiment having a non-stacked gate

select gate transistor. The structure of a memory cell and select gate transistor in the first embodiment is shown in Figure 2(f), which is reproduced below.

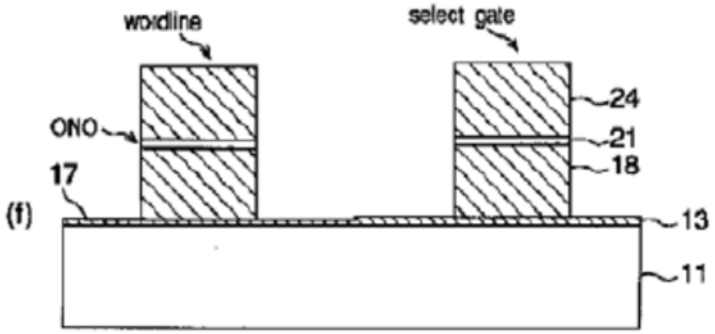


Figure 2(f) is a cross-sectional view of a "memory cell [wordline] and the select gate [transistor] in the bitline direction of the EEPROM in embodiment example 1." *Id.* at 8. The memory cell includes tunnel oxide film 17, first polysilicon layer 18, ONO (oxide-nitride-oxide) film 21, and second polysilicon layer 24. *Id.* ¶¶ 29–32. The select gate transistor includes low voltage gate oxide film 13, first polysilicon layer 18, ONO film 21, and second polysilicon layer 24. *Id.* ¶¶ 28–32. Hemink discloses using the same process steps to simultaneously make first polysilicon layer 18, ONO film 21, and second polysilicon layer 24 in the memory cell and select gate transistors. *Id.* ¶¶ 28–32, Figs. 1(a)–1(c), 2(d)–2(f). Moreover, Hemink discloses using the same process steps to "simultaneously form the stacked gate memory cell structure and [a] peripheral transistor." *Id.* ¶ 25. As a result, "a peripheral circuit [is] provided on the peripheral portion of th[e] memory cell array" such that "the select transistor and peripheral circuit transistor have a gate with a structure wherein first and second poly-Si layers 18, 24 are laminated, as in the case of the [memory] cell transistor." *Id.* at [54], [57].

2. Shudo

Shudo discloses a semiconductor memory device having a high voltage

V_{pp} transistor with reduced substrate bias. Ex. 1006, at [57]. A planar diagram of Shudo's memory device is shown in Figure 10, which is reproduced below. *Id.* ¶ 57.

(FIGURE 10)

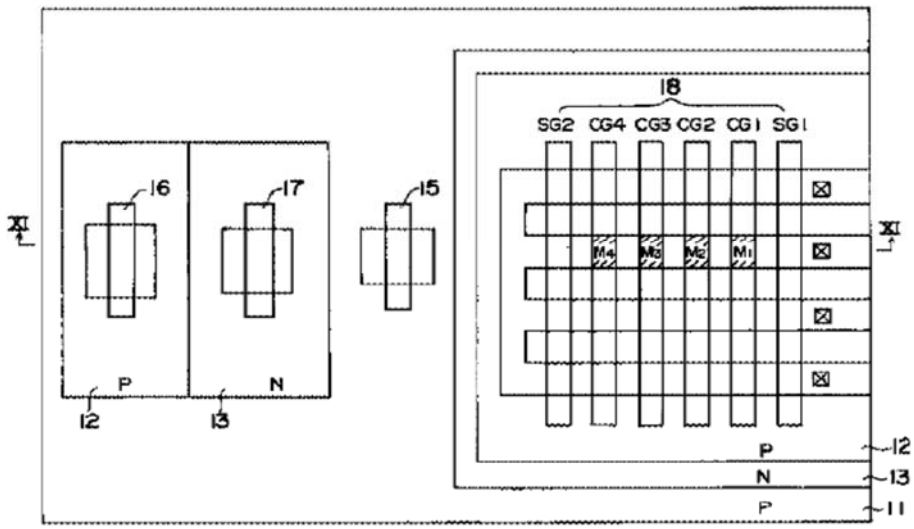


Figure 10 is a planar diagram that schematically illustrates Shudo's semiconductor memory device. *Id.* A cross-sectional view taken along line XI–XI of Figure 10 is shown in Figure 11 of Shudo, which is reproduced below. *Id.*

(FIGURE 11)

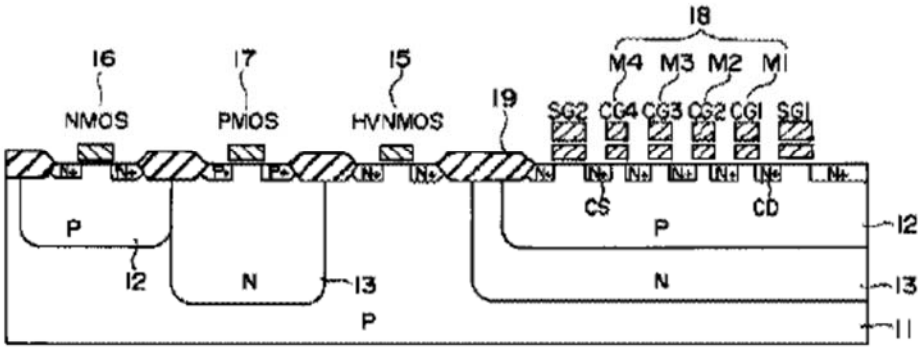


Figure 11 is a cross-sectional view of Shudo's memory device taken along line XI–XI of Figure 10. *Id.* Memory array 18 is a NAND-type array, where each

row of the array consists of a string of memory cells M_1–M_4 connected in series, with first bit line select gate transistor SG_1 coupled to one end of the series and second bit line select gate transistor SG_2 coupled to the other end of the series. *Id.* ¶¶ 41–42. Control gates CG_1–CG_4 of memory cells M_1–M_4 intersect the bit lines of memory array 18 to form word lines. *Id.* ¶ 42. The memory cells and select gate transistors of memory array 18 are formed in a core area of substrate 11, and transistors 15–17 are formed in a peripheral area of substrate 11. *Id.* ¶¶ 20, 41–43, Figs. 10–11. Peripheral transistor 15 supplies a high voltage V_{pp} (e.g., 18V), and has a 40–50 nm (i.e., 400–500 Å) thick gate oxide. *Id.* ¶¶ 3–4, 31–32.

E. Patentability of Claims 1, 3, 6, and 7 over Hemink

Petitioner argues claims 1, 3, 6, and 7 are unpatentable as obvious over Hemink. Pet. 26–55. As discussed in § II.B.3, *supra*, Petitioner relies on Hemink to disclose a NAND-type flash memory device having select gate transistors with both stacked gate (embodiment 1) and non-stacked gate (embodiment 2) structures. Pet. 31–32. Patent Owner does not dispute Petitioner's contention that the claims read on memory devices having select gate transistors with stacked gate structures. *See* PO Resp. 20 (arguing there was no disclaimer or disavowal of select gate transistors having stacked gate structures). Accordingly, we analyze Petitioner's contentions regarding Hemink based on the teachings of embodiment 1.

As discussed below, the parties dispute whether Hemink teaches or suggests a high voltage transistor in the periphery region, as recited in claim 1, and whether the limitations of claim 7 are met by the select gate transistor of Hemink's first embodiment. Patent Owner does not dispute Petitioner's contentions that Hemink's first embodiment teaches or suggests the remaining

elements of claims 1, 3, 6, and 7. For the reasons discussed below, we determine Petitioner has demonstrated by a preponderance of evidence that claims 1, 3, 6, and 7 are unpatentable as obvious over the first embodiment of Hemink.

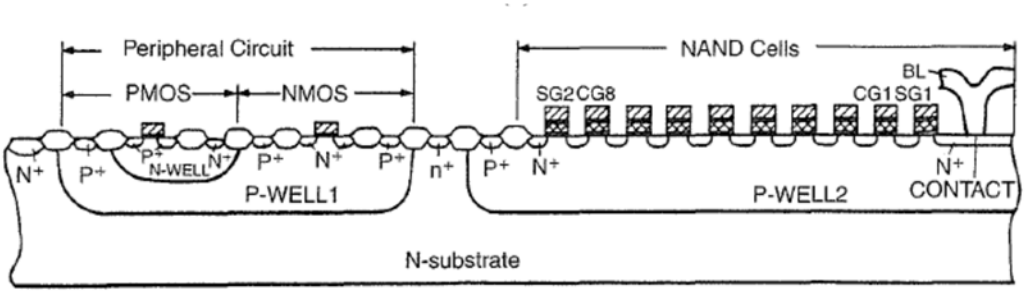
1. Claim 1

Claim 1 recites a NAND-type flash memory device, and requires the device to have a core region comprising a stacked gate flash memory cell and a select gate transistor. Ex. 1001, 11:18–20. Petitioner argues Hemink discloses these limitations. *See* Pet. 29–31 (citing Ex. 1003 ¶¶ 90–91; Ex. 1005 ¶¶ 2, 23, 35, Figs. 2(e), 14(a); Ex. 1010, 11–12, 15–20). Patent Owner does not dispute this. *See* PO Resp. 40–53.

Hemink discloses an improved method for manufacturing a NAND-type flash memory device comprising eight memory cells (M1–M8) and two select gate transistors (S1 and S2) by reducing the number of mask processing steps. Ex. 1005, at [57], ¶ 2, Fig. 14(a). Memory cells M1–M8 have a stacked gate structure containing two gate electrodes—a floating gate and a control gate—in a stacked gate configuration. *Id.* ¶¶ 23, 35, Fig. 2(e). Memory cells M1–M8 and select gate transistors S1 and S2 connect to a "peripheral circuit on [a] peripheral portion of this memory cell array." *Id.* at 2 (claims 1–3).

According to Dr. Banerjee's unrebutted testimony, a person of ordinary skill in the art would have understood that memory cells M1–M8 and select gate transistors S1 and S2 are located in a core region of Hemink's memory device because "[t]he core-periphery division was and remains a conventional feature in NAND memory devices." Ex. 1003 ¶90; *see also id.* ¶¶ 26–29 (discussing structure of NAND memory devices). Dr. Banerjee's testimony is

supported, for example, by Figure 3-31(b) of Sharma[5] (Ex. 1010), which is reproduced below. *See* Pet. 30 (citing Ex. 1010, 11–12); *see also* Ex. 1003 ¶ 27 (citing Ex. 1010, Fig. 3-31).



(b)

Figure 3-31(b) of Sharma is a cross-sectional view of a prior art NAND-type flash memory circuit. Ex. 1010, 11, Fig. 3-31(b). The figure discloses a "NAND cell array and peripheral CMOS circuitry . . . located in separate p-wells". *Id.* at 12.

For the reasons discussed above, Petitioner demonstrates by a preponderance of evidence that Hemink teaches a NAND-type flash memory device having a core region that includes a stacked gate flash memory cell and a select gate transistor as required by claim 1.

Claim 1 further requires the flash memory device to have a periphery region comprising a low voltage transistor and a high voltage transistor, and requires both the low voltage and select gate transistors to have gate oxide and gate electrode layers. Ex. 1001, 11:21–24.

Petitioner, relying on the testimony of Dr. Banerjee, argues Hemink teaches or suggests these limitations by disclosing a "peripheral circuit provided on the peripheral portion of th[e] memory cell" that includes a "peripheral

[5] Ashok K. Sharma, *Semiconductor Memories, Technology, Testing, and Reliability* 119 (1997)

circuit transistor," and by disclosing a low voltage peripheral transistor and high voltage gate oxide. Pet. 32–34 (citing Ex. 1005 claims 1–3, ¶¶ 18, 19, 25; Ex. 1003 ¶¶ 26–29, 95–98). Petitioner argues a person of ordinary skill in the art would have known that Hemink formed high voltage transistors in the periphery of its memory device because doing so "was and remains a conventional feature in NAND memory devices." *Id.* at 34 (citing Ex. 1003 ¶¶ 26–29, 97–98; Ex. 1010, 11–12, 15–20); *see also* Reply 17–18 (citing Ex. 1019, 1; Ex. 1031, 1:9–43; Ex. 1025 ¶¶ 38–39). Finally, Petitioner argues Hemink discloses the low voltage and select gate transistors both include gate oxide and gate electrode layers. Pet. 34–36 (citing Ex. 1005 ¶¶ 26, 28, 30, 33, Figs. 2(f), 6(f)).

Patent Owner does not dispute that Hemink discloses a flash memory device having a peripheral region comprising a low voltage transistor, where the low voltage transistor and select gate transistor both include gate oxide and gate electrode layers. *See* PO Resp. 40–53. Rather, Patent Owner argues that Hemink fails to teach or suggest a high voltage transistor in the peripheral region. *Id.* We discuss the relative merits of the parties' arguments below.

Patent Owner first argues that Hemink fails to disclose a high voltage transistor in a memory device. *See* PO Resp. 47–49. In particular, Patent Owner argues that although Hemink discloses a "high-voltage gate oxide film," Hemink fails to disclose a high voltage transistor or "the operational uses of any transistor in its device."[6] *Id*. at 47–48. Although we agree that Hemink does

[6] We note that the '085 patent itself lacks any disclosure of the operational use of any transistor in the *claimed* device. The portions of the '085 patent cited by Patent Owner as disclosing the functions performed by the *claimed* high voltage transistor describe little more than the use of high voltage to program and erase

not expressly disclose a high voltage transistor formed in a peripheral region of a memory device, Petitioner does not rely on Hemink for such an express disclosure. Rather, Petitioner argues that Hemink teaches or suggests a high voltage transistor formed in a peripheral region of its memory device because Hemink expressly teaches the memory device includes a high voltage gate oxide, and because it was conventional to form high voltage transistors having high voltage gate oxides in peripheral regions of memory devices. *See* Pet. 32–33[7] (citing Ex. 1003 ¶¶ 26–29, 95–98); Pet. Reply 17–19 (citing Ex. 1025 ¶¶ 37–41); *see also* Ex. 1003 ¶¶ 26–29 (describing the structure of a conventional NAND-type flash memory device).

Patent Owner disputes that it was conventional to form high voltage transistors in the peripheral regions of NAND-type flash memory devices. *See* PO Resp. 49–53. In particular, Patent Owner argues Hemink teaches making a conventional flash memory device that does not form a high voltage transistor in a peripheral region because Hemink teaches removing the high voltage gate oxide from the peripheral region. *Id.* at 50 (citing Ex. 1005 ¶ 10). Patent Owner further argues that Prince[8] teaches forming a high voltage transistor in

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prior art NAND-type flash memory cell 14, shown in Figure 1C, without identifying the source of the high voltage or the location of that source. *See* PO Resp. 32–33 (citing Ex. 1001, 2:9–12, 2:36–41); *see also* Ex. 1001, 2:9–12 (disclosing programming prior art memory cell 14 by "applying a relatively high voltage V_G . . . to the control gate 17*d* and connecting the drain, source, and P-well to ground"); *id*. at 2:36–41(disclosing erasing prior art memory cell 14 by applying "a relatively high voltage V_g . . . to the P-well 16 and the control gate 17*d* with a voltage applied between the source 14*b* and the drain 14*a*").

[7] Petitioner cites to Section V.A.1 of the Banerjee Declaration, which is paragraphs 26–29 of that Declaration. *See* Ex. 1003 ¶¶ 26–29.

[8] Betty Prince, *Semiconductor Memories, A Handbook of Design, Manufacture,*

the core region rather than the peripheral region of a conventional memory device by teaching the core region includes structures such as "erase gates" and "erase lines," i.e., structures for erasing memory cells using high voltages. *Id.* at 50–51 (citing Ex. 2010, 591, 599, Figs. 11.45, 11.53).

Upon consideration of the evidence and arguments presented, we are persuaded by Petitioner's contention that a person of ordinary skill in the art would have understood that it was conventional to form high voltage transistors in the peripheral region of Hemink's flash memory device. *See* Pet. 34 (citing Ex. 1003 ¶¶ 26–29, 97–98; Ex. 1010, 11–12, 15–20); Pet. Reply 17–18 (citing Ex. 1019, 1; Ex. 1031, 1:9–43). Petitioner's contention is persuasively supported by the testimony of Dr. Banerjee. *See* Ex. 1003 ¶ 28 (citing Ex. 1007 ¶ 3; Ex. 1008 ¶ 41; Ex. 1014 ¶¶ 18, 39–40; Ex. 1018, 5, 9). Indeed, Patent Owner's expert, Dr. Bottoms, admits that it was conventional to form high voltage transistors in the peripheral regions of flash memory devices. Ex. 1024, 11:8–14 (testifying that "[t]he peripheral of a flash device contains transistors that are not located in the core," and that "the high-voltage transistors would be there and the low-voltage logic level devices would be there").

Petitioner's contention is also persuasively supported by the prior art cited by Petitioner and Dr. Banerjee, including Prince (Exs. 1018 and 2010),[9] Sharma (Ex. 1010), Iwata (Ex. 1019), Aritome (Ex. 1014), and Tsunodo (Ex. 1007). *See* Pet. 34; Reply 17–18. Prince teaches "[a]ll MOS memory architectures on occasion use on-chip voltage generation," including "the high

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and Application (2nd Ed.)(1991).

[9] Both Petitioner and Patent Owner cite to portions of Prince. Patent Owner cites to portions introduced as Exhibit 2010 (*see* n.8, *supra*), and Petitioner cites to portions introduced as Exhibit 1018.

programming voltages required for EPROM programming." Ex. 1018, 5. Sharma teaches that the type of on-chip high voltage generation described by Prince occurs in the peripheral region of a memory device, away from the core region containing the memory cell array. *See* Ex. 1010, 18, Fig. 3-37. This is shown in Figure 3-37 of Sharma, which is reproduced below.

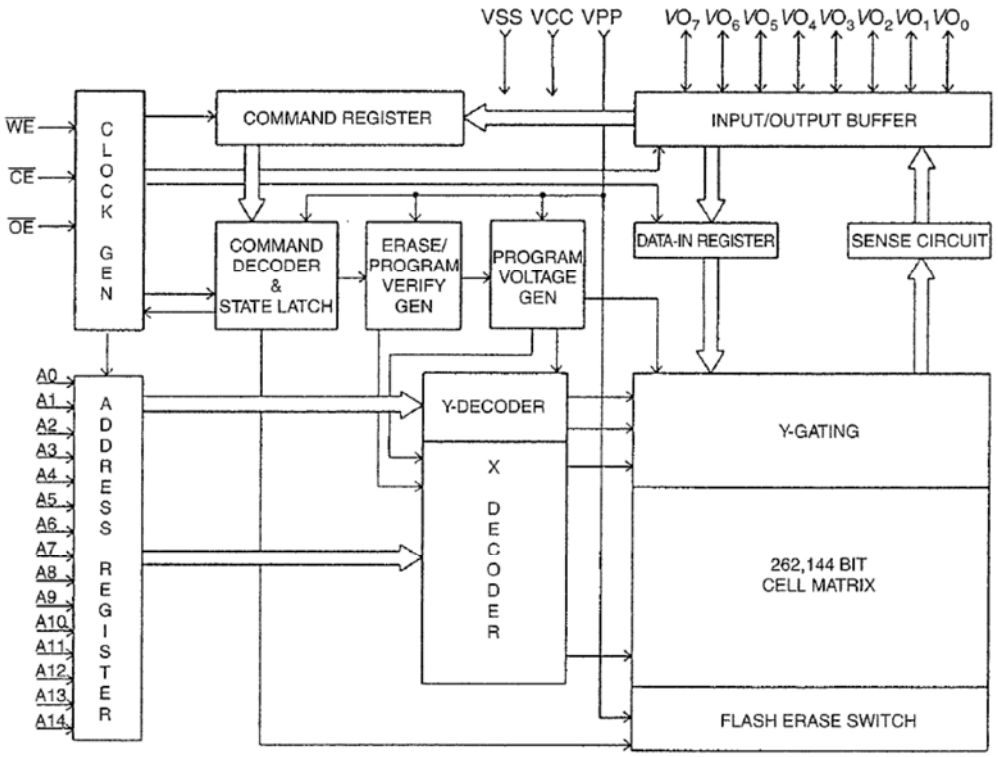

Figure 3-37. A 256K CMOS flash memory Intel chip block diagram. (From [88], with permission of IEEE.)

Figure 3-37 of Sharma is a schematic illustration of a 256k flash memory chip. The chip has a core region containing a 256k memory cell array (i.e., the "262,144 BIT CELL MATRIX"). *Id.*, Fig. 3-37. The chip also has a peripheral region that includes blocks for generating the high voltages needed to program and erase the memory cell array (e.g., the "ERASE/PROGRAM VERIFY GEN" and "PROGRAM VOLTAGE GEN" blocks). *Id.* Iwata teaches that peripheral memory device blocks contain CMOS logic circuits, including

"transistors for generating and transferring severe program/erase voltages," i.e., high voltage transistors. Ex. 1019, 1–2, Fig. 1. Aritome, likewise teaches forming memory cells and high voltage transistors in different regions or blocks of a flash memory device. *See* Ex. 1014 ¶ 18 (teaching the formation of a "second MOS transistor portion (high potential VPP system) in the peripheral circuitry" of a NAND-type flash memory cell). So does Tsunodo. *See* Ex. 1007 ¶ 3, Fig. 16 (teaching forming field oxides to segment a flash memory device into different functional areas, including "a cell area" containing select gate transistor 18 and memory cell transistor 19, and a "high voltage circuit area" containing Vpp transistor 21).

As discussed above, Petitioner relies on Hemink's first embodiment to teach or suggest growing a high voltage transistor in a peripheral region of a memory device. *See* Pet. 32–36 (citing Ex. 1005 ¶¶ 18, 25, 26, 28, 30, 33, Figs. 2(f), 6(f)). In Hemink's first embodiment, a high voltage gate oxide is grown on the entire silicon substrate 11 (step 1), the substrate is masked to prescribe a low voltage gate oxide area (step 2), and the high voltage gate oxide is removed from the prescribed area (step 3) where the low voltage gate oxide 13 is grown (step 5). Ex. 1005 ¶ 28. Hemink teaches low voltage gate oxide 13 forms part of a low voltage transistor in the peripheral region of the memory device. *Id.* ¶¶ 25–26, Fig. 6(f). Thus, Hemink's high voltage gate oxide is not removed from the entire peripheral area, only from those areas where low voltage gate oxides and transistors are formed. *Id.* ¶ 28. As a result, a high voltage gate oxide is grown in portions of the peripheral area to a thickness that is "determined by the high-voltage gate oxide film growth process (step 1), the low-voltage gate oxide film growth process (step 5)," and a subsequent "tunnel oxide film growth process (step 9)." *Id.* ¶ 35. Moreover, as discussed above,

Petitioner shows a person of ordinary skill in the art would have known that the high voltage gate oxide was a component of a high voltage transistor, and that it was conventional to form high voltage transistors in the peripheral region of flash memory devices. *See* Pet 34 (citing Ex. 1003 ¶¶ 26–29, 97–98; Ex. 1010, 11–12, 15–20); *see also* Reply 17–18 (citing Ex. 1019, 1; Ex. 1031, 1:9–43; Ex. 1025 ¶¶ 38–39).

Patent Owner argues that Hemink's paragraph 10 contradicts Petitioner's contention that it was conventional to form high voltage transistors in the periphery of NAND-type flash memory devices. PO Resp. 50. We disagree for at least two reasons. First, the overwhelming majority of evidence, described above, supports Petitioner's argument that it was conventional to form high voltage transistors in the peripheral region of flash memory devices. Second, Hemink's description of a conventional process (Ex. 1005 ¶¶ 6–14) does not contradict Hemink's first embodiment process (*id.* ¶¶ 25–36), which Petitioner relies on for teaching or suggesting a high voltage transistor in the peripheral region of Hemink's memory device. Pet. 32–34; Reply 17–18. As explained in the preceding paragraph, in Hemink's first embodiment process, high voltage gate oxides are formed and left in portions of the peripheral region where low voltage gate oxides are not formed. *See* Ex. 1005 ¶¶ 25–28.

We also disagree with Patent Owner's argument that Prince teaches forming high voltage transistors in the core region of flash memory devices by teaching the core region includes structures such as "erase gates" and "erase lines." *See* PO Resp. 50–51 (citing Ex. 2010, 591, 599, Figs. 11.45, 11.53). Instead, we agree with Petitioner that the disclosed erase gates and lines "are not high voltage transistors," but are rather "conductive elements that carry programming voltages from the periphery to the core." Pet. Resp. 22; Ex. 1025

¶ 45. For example, Prince describes Figure 11.45 as illustrating a "triple level polysilicon structure one-transistor floating gate [memory] *cell*." *See* Ex. 2010, 20, 22, 38 (emphasis added) (citing Masuoka *et al*., *A 256k Flash EEPROM cell using triple polysilicon technology*, IEDM Proceedings, 464 (1984)). The program/erase circuitry for this memory cell, which is shown in Figure 11.46(a), includes a Vpp pin that supplies a high voltage to the memory cell from an external source. *Id.* at 20, 23, Fig. 11.46(a). Similarly, Prince describes Figure 11.53 as illustrating a "flash *memory cell* with split level control gate and shared erase gate." *Id.* at 30, 39 (emphasis added) (citing Kazerounian, R. *et al*., *A 5 Volt High Density Poly-Poly Erase Flash EPROM Cell*, IEDM Proceedings, 436 (1988)). Figure 11.53(c) of Prince illustrates the memory device's memory cell "array structure showing [the] shared erase line." *Id.* According to the testimony of Patent Owner's expert, Dr. Bottoms, the shared "erase line" shown in Figure 11.53 of Prince is an electrical connection, not a high voltage transistor. Ex. 1024, 35:9–14.

Accordingly, for the reasons discussed above, we find Petitioner demonstrates by a preponderance of evidence that Hemink teaches or suggests a NAND-type flash memory device having a periphery region comprising a low voltage transistor and a high voltage transistor, and low voltage and select gate transistors having gate oxide and gate electrode layers as required by claim 1.

Claim 1 further requires the gate oxide layers and the gate electrode layers of the low voltage and select gate transistors to have substantially the same thickness. Ex. 1001, 11:25–29. Petitioner argues Hemink discloses these limitations. *See* Pet. 38–40 (citing Ex. 1005 ¶¶ 28, 30, 33, 35, Figs. 2(f), 6(f); Ex. 1003 ¶¶ 105–106). Patent Owner does not dispute this. *See* PO Resp. 40–53.

Hemink discloses the first embodiment process for manufacturing a NAND-type flash memory device allows "simultaneously form[ing] the stacked gate memory cell structure and the peripheral transistor." Ex. 1005 ¶ 25. As a result, Hemink discloses using the same process steps to form the same gate oxide layer for both the select gate and low voltage transistors. For example, the select gate and low voltage transistors both include gate oxide layer 13, and Hemink describes growing gate oxide 13 in steps 5 and 9 for both the select gate and low voltage transistors. *Id.* ¶¶ 28–30, 35, Figs. 2(f), 6(f)). Indeed, Hemink discloses "[t]he final *thickness of the low-voltage (or select) gate oxide film* is determined only by the low-voltage gate oxide film growth process (step 5) and the tunnel oxide film growth process (step 9)." Ex. 1005 ¶ 46 (emphasis added).

Hemink similarly discloses using the same process steps to form the same gate electrode layers for the select gate and low voltage transistors. For example, the select gate and low voltage transistors both include stacked gate electrodes 18 and 24, and Hemink describes depositing the polysilicon for stacked gate electrodes 18 and 24 in steps 10 and 18 for both the select gate and low voltage transistors. *Id.* ¶¶ 30–33, 35, Figs. 2(f), 6(f)). Hemink further discloses the "second polysilicon layer 24 is used in the formation of the wordline [memory cell], select gate, and peripheral transistor gate." *Id.* ¶ 32.

According to the unrebutted testimony of Dr. Banerjee, gate oxide 13 and gate electrodes 18 and 24 in the select gate and low voltage transistors in Hemink's first embodiment would have had substantially the same thickness. Ex. 1003 ¶ 105. This is because Hemink discloses the same growing steps for gate oxide 13, depositing steps for gate electrodes 18 and 24, and processing

steps for these layers of the select gate and low voltage transistors in Hemink's first embodiment. *Id*.

Accordingly, for the reasons discussed above, Petitioner has shown by a preponderance of evidence that Hemink teaches the gate oxide layer and gate electrode layers of Hemink's select gate and low voltage transistors are of substantially the same thickness. Moreover, Petitioner has shown by a preponderance of evidence that Hemink teaches or suggests all of the limitations of claim 1, and that claim 1 is unpatentable as obvious over Hemink.

2. Claim 3

Claim 3 depends from claim 1, and requires the stacked gate flash memory cell to include a tunnel oxide layer, a floating gate layer over the tunnel oxide layer, an insulating layer over the floating gate layer, and a control gate layer over the insulating layer. Ex. 1001, 11:32–12:2. Petitioner argues Hemink teaches these limitations. *See* Pet. 42–44 (citing Ex. 1005 ¶¶ 29–32, Fig. 2(f)). Patent Owner argues Petitioner has failed to demonstrate the obviousness of claim 3 over Hemink for the same reasons discussed above with respect to claim 1. *See* PO Resp. 53. We considered Patent Owner's arguments regarding claim 1 in § II.E.1, *supra*, and found them unpersuasive for the reasons discussed there.

In the first embodiment, Hemink forms the stacked gate flash memory cell by forming tunnel oxide 17 in step 9, floating gate 18 in step 10, ONO insulating layer 21 in step 14, and control gate 24 in step 18. Ex. 1005 ¶¶ 29–33. Hemink illustrates the resulting stacked gate flash memory cell and accompanying select gate transistor in Figure 2(f), which is reproduced below.

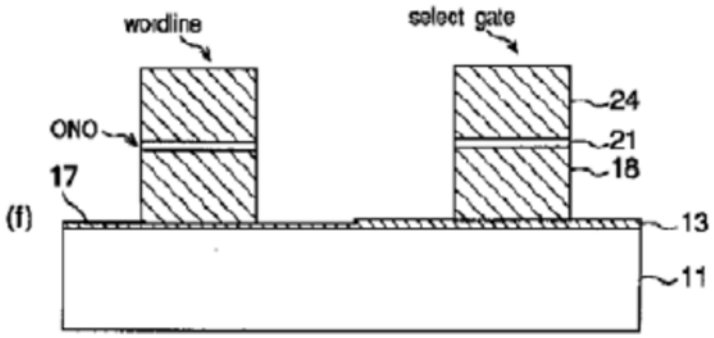

Figure 2(f) of Hemink is a cross-sectional view of a memory cell (wordline) and select gate transistor formed according to the process described in the first embodiment. *Id.* at 8. The memory cell includes tunnel oxide layer 17, floating gate layer 18, ONO insulating layer 21, and control gate layer 24.

For the reasons discussed above, Petitioner has demonstrated by a preponderance of evidence that Hemink teaches all the limitations of claim 3, and that claim 3 is unpatentable as obvious over Hemink.

3. Claim 6

Claim 6 depends from claim 1, and requires a plurality of select gate transistors that share a common conductive gate region to allow the select gate transistors to form a select gate word line. Ex. 1001, 12:10–14. Petitioner argues Hemink teaches this limitation. *See* Pet. 44–48 (citing Ex. 1005 ¶ 4, Fig. 13; Ex. 1003 ¶ 119). Patent Owner argues Petitioner has failed to demonstrate the obviousness of claim 6 over Hemink for the same reasons discussed above with respect to claim 1. *See* PO Resp. 53. We considered Patent Owner's arguments regarding claim 1 in § II.E.1, *supra*, and found them unpersuasive for the reasons discussed there.

Hemink discloses a prior art NAND-type memory device having two NAND-type memory strings, each of which includes two select gate transistors S_1 and S_2, where a plurality of select gate transistors from each string (e.g.,

transistors S_1) are connected together via a common conductive member to form a select gate word line. Ex. 1005 ¶ 4, Fig. 13. According to the unrebutted testimony of Dr. Banerjee, Hemink Figure 13 "depicts a conductive strip that runs horizontal to the gate electrodes, and would have been understood to contact the gates (forming gate regions) to electrically connect the gates." Ex. 1003 ¶ 119. Moreover, a person of ordinary skill in the art would have understood that Hemink's first embodiment process would have produced the same type of structure shown in Figure 13, including the common select gate word line, because it would not have changed the overall structure or architecture of the prior art device shown in Figure 13. *Id.* ¶¶ 83–86. It would have simply improved the method for making the transistors in that prior art device. *Id*. We credit Dr. Banerjee's unrebutted testimony on these points.

For the reasons discussed above, Petitioner has demonstrated by a preponderance of evidence that Hemink teaches all the limitations of claim 6, and that claim 6 is unpatentable as obvious over Hemink.

4. Claim 7

As discussed in § II.A, *supra*, claim 7 is an independent claim that is substantially similar in scope to claim 3, which depends from independent claim 1. Petitioner, citing essentially the same evidence cited in its analysis of claims 1 and 3, argues claim 7 is unpatentable as obvious over Hemink for the same reasons claims 1 and 3 are obvious over Hemink. *See* Pet. 48–53. For the claim 7 limitation requiring the core region of the memory device to have a select gate transistor with a gate oxide layer and a second conductive material forming a gate overlying the gate oxide layer, Petitioner identifies the select gate transistor in Hemink's first embodiment, and its gate oxide layer 13 and

poly2 layer 24, respectively. *Id*. at 50 (citing Ex. 1005 ¶¶ 28, 30, 33, 35, Fig. 2(f).

Patent Owner first argues Petitioner has failed to demonstrate the obviousness of claim 7 over Hemink for the same reasons Petitioner has failed to demonstrate the obviousness of claim 1 over Hemink. *See* PO Resp. 54. We considered Patent Owner's arguments regarding claim 1 in § II.E.1, *supra*, and found them unpersuasive for the reasons discussed there.

Patent Owner next argues that Petitioner has failed to demonstrate the obviousness of claim 7 over Hemink because the select gate transistor in Hemink's first embodiment does not have a "second conductive material forming a gate layer overlying the gate oxide layer" of the select gate transistor. *Id.* at 55–56. Patent Owner argues claim 7 requires the "second conductive material" that forms the select gate transistor's gate layer to be the same "second conductive material forming a poly2 layer overlying the insulating layer" of the stacked gate memory cell.[10] *Id.* at 55. Patent Owner construes the term "overlie" to mean "lie on top of." *Id.* (citing Ex. 2011, 4). Despite this broad construction, Patent Owner contends poly2 layer 24 is not the "second conductive material" forming the gate of the select gate transistor as required by

[10] Petitioner disputes this construction, and argues the "second conductive material need only be the same material (e.g., polysilicon) that overlies the stacked gate memory cell's insulating layer, regardless of the process step in which it is deposited. *See* Pet. Reply 4–5. We need not resolve this dispute, however, because the second conductive material identified by Petitioner as forming the select gate transistor's gate (i.e., Hemink's poly2 layer 24) is a second conductive material under either proposed construction. That is, poly2 layer 24 is the same material (polysilicon) overlying the stacked gate memory cell's insulating layer as Petitioner contends, and is deposited in the same process step as Patent Owner contends.

claim 7 because it "does not *directly* lie on top of the gate oxide layer 13" of the select gate transistor. *Id.* (emphasis added).

Petitioner responds that the plain and ordinary meaning of "overlying" is "lying over . . . but not necessarily *directly* on top of." Reply 3–4 (citing Exs. 1026–1029) (emphasis added). Petitioner argues the disclosure of the '085 patent is consistent with this plain and ordinary meaning. *Id.* at 3 (quoting Ex. 1001, 2:41–48, Fig. 1C) (emphasis omitted). In particular, Petitioner argues that when describing the operation of prior art memory cell 14 shown in Figure 1C, the '085 patent describes a "portion of the floating gate 17b overlying the source region 14b" of memory cell 14 even though floating gate 17b does not lie directly on top of source region 14b. *Id.*

Upon consideration of the arguments and evidence presented by Petitioner and Patent Owner, we find the plain and ordinary meaning of "overlying" means "on top of," but not necessarily "directly on top of." First, both the intrinsic and extrinsic evidence support "overlying" to mean lying "on top of," but not necessarily "directly on top of." For example, Figure 1C of the '085 patent shows floating gate 17b lying "directly on top of" tunnel oxide 17a, which in turn lies "directly on top of" channel 15 and portions of drain 14a and source 14b. Ex. 1001, Fig. 1C. Although no portion of floating gate 17b lies "directly on top of" source 14b, the '085 patent describes a "portion of the floating gate 17b *overlying* the source region 14b." *Id.* at 2:42–47. Thus, the '085 patent uses "overlying" to mean lying "on top of," but not necessarily "directly on top of." Second, the extrinsic evidence is consistent with this usage of the term. For example, the Concise Oxford Dictionary relied on by Patent Owner defines "overlay" to mean "lie on top of," not to lie *directly* on top of. Ex. 2011, 4. Webster's Ninth New Collegiate Dictionary defines "overlay" to

mean "to lay or spread over or across," not to lay *directly* over or across. Ex. 1026, 3. The American Heritage Dictionary defines "overlay" to mean "[t]o lay or spread *over or on*," not to lay *directly* over or on. Ex. 1028, 3 (emphasis added). Thus, the "gate layer overlying the gate oxide layer" of the select gate transistor recited in claim 7 is a gate later that "lies on top of" or that is "spread over" or that "lays *over*" the gate oxide layer, without necessarily lying *directly* on the gate oxide layer as Patent Owner contends.

Given our understanding that the plain and ordinary meaning of "overlying" means lying "on top of," but not necessarily "directly on top of," we find poly2 layer 24 of the select gate transistor in Hemink's first embodiment is a "second conductive material forming a gate layer overlying the gate oxide layer" 13 because it lies on top of gate oxide layer 13, even though it does not lie directly on top of gate oxide layer 13.

Accordingly, for the reasons discussed above and in § II.E.1, *supra*, Petitioner has demonstrated by a preponderance of evidence that Hemink teaches or suggests a NAND-type flash memory device having all the limitations recited in claim 7, and that claim 7 is unpatentable as obvious over Hemink.

F. Patentability of claim 4 over Hemink and Shudo

Petitioner argues claim 4 is unpatentable as obvious over Hemink and Shudo. Pet. 55–59. As discussed in § II.B.3, *supra*, Petitioner relies on Hemink for disclosing a NAND-type flash memory device having select gate transistors with both stacked gate (embodiment 1) and non-stacked gate (embodiment 2) structures. Patent Owner does not dispute Petitioner's contention that the claims read on memory devices having select gate transistors with stacked gate structures. Accordingly, we analyze Petitioner's contentions

regarding Hemink based on the teachings of embodiment 1, and find, for the reasons discussed below, Petitioner has demonstrated by a preponderance of evidence that claim 4 is unpatentable as obvious over the combined teachings of Hemink's first embodiment and Shudo.

1. Claim 4

Claim 4 depends from claim 1, and requires the high voltage transistor to have about a 400 Å gate oxide layer, and a conductive gate region over the gate oxide layer. Ex. 1001, 12:3–6.

Petitioner argues this limitation would have been obvious in view of the combined teachings of Hemink's first embodiment and Shudo. Pet. 55–57 (citing Ex. 1005 ¶¶ 28, 35). In particular, Petitioner argues Hemink's first embodiment teaches or suggests forming a high voltage transistor having a high voltage gate oxide, floating gate 18, insulating ONO layer 21, and control gate 24 in process steps 1, 10, 14, and 18, relying on the same analysis discussed above in § II.E.1, *supra*. *Id.* at 56 (citing Ex. 1005 ¶¶ 28, 35). Petitioner acknowledges Hemink does not teach or suggest growing the high voltage gate oxide to any particular thickness. *Id.* Nonetheless, Petitioner argues it would have been obvious to grow the high voltage gate oxide to a thickness of about 400 Å as required by claim 4 for two reasons. First, Petitioner argues a person of ordinary skill in the art would have known that a conventional high voltage gate oxide was about 500 Å thick, which is itself "about" 400 Å thick. *Id.* at 57 (citing Ex. 1003 ¶¶ 142–143; Ex. 1006 ¶ 4; Ex. 1008 ¶¶ 20, 28). Second, Petitioner argues Shudo teaches a 400 Å thick high voltage gate oxide, and a person of ordinary skill in the art would have found it obvious to replace Hemink's gate oxide with Shudo's as a simple substitution of one element for another known in the prior art to obtain a predictable result. *Id.* at 56–58 (citing

Ex. 1006 ¶ 32). Petitioner argues a person of ordinary skill in the art would have made the substitution in response to market forces driving device miniaturization. *Id*. at 57–58 (citing Ex. 1003 ¶¶ 142–147). Petitioner further argues a person of ordinary skill in the art would have made the substitution to achieve the advantages taught by Shudo, including minimizing punch-through, substrate bias effects, and threshold voltage variability in high voltage transistors. *Id.* at 58.

Patent Owner argues Petitioner has failed to demonstrate the obviousness of claim 4 over Hemink and Shudo for the same reasons Petitioner has failed to demonstrate the obviousness of claim 1 over Hemink discussed in § II.E.1, *supra*. PO Resp. 59–61. That is, Patent Owner argues Petitioner has "fail[ed] to establish how Hemink, modified or otherwise, teaches or suggest[s] a high voltage transistor with 'a conductive gate region overlying the gate oxide layer' as recited in [] claim 4." *Id.* at 61. Patent Owner further argues that—assuming Hemink does teach or suggest a high voltage transistor having a high voltage gate oxide—Petitioner has failed to show that it would have been obvious to replace it with Shudo's. *Id.* at 61–62. Patent Owner argues that Shudo's high voltage transistor with a 400 Å gate oxide operates at 18V, and Petitioner has not shown that Hemink's memory device would work with a high voltage transistor having a 400 Å gate oxide operating at 18V. *Id.* at 62–64.

Upon consideration of the evidence and arguments presented by Petitioner and Patent Owner, we find the combination of Hemink and Shudo teaches a flash memory device having a high voltage transistor in the periphery of the device having a 400 Å gate oxide. As discussed above, Hemink teaches forming a low voltage transistor and a high voltage gate oxide in the peripheral area of a memory device, and a person of ordinary skill in the art would have

known that it was conventional to form low voltage transistors and high voltage transistors in the peripheral areas of memory devices. *See* § II.E.1, *supra*.

We credit the testimony of Dr. Banerjee that the gate oxide thickness of a conventional memory device's high voltage transistor was about 500 Å. *See* Ex. 1003 ¶ 143 (citing Ex. 1006 ¶ 4; Ex. 1008 ¶ 28). For example, Shudo and Aritome both teach the gate oxide thickness of prior art high voltage transistors was 500 Å. Ex 1006 ¶ 4; Ex. 1008 ¶ 28. Additional prior art of record in this proceeding is consistent with these teachings, and shows the gate oxide thickness of prior art high voltage transistors was in the 300–500 Å range. *See* Ex. 1007 ¶ 15 (350 Å); Ex. 1014 ¶ 36 (450 Å); Ex. 1019, 1–2 (420 Å); Ex. 1032, 9:39–42 (300 Å). Thus, Shudo's 400 Å gate oxide is squarely within the range of high voltage gate oxide thicknesses disclosed in the prior art. Moreover, Dr. Banerjee credibly testifies that a person of ordinary skill in the art would have been motivated to use Shudo's process to make Hemink's high voltage transistor with a 400 Å gate oxide in order to minimize the size, threshold variability, substrate bias effects, and punch-through of the high voltage transistor, as taught by Shudo. Ex. 1003 ¶¶ 142, 147–149; Ex. 2014, 6.

For the reasons discussed above, Petitioner has demonstrated by a preponderance of evidence that the combination of Hemink's first embodiment and Shudo teaches a memory device having a peripheral high voltage transistor with a 400 Å gate oxide and a conductive gate over the gate oxide as required by claim 4. Accordingly, Petitioner has shown that claim 4 is unpatentable as obvious over the combination of Hemink's first embodiment and Shudo.

G. Additional Patentability Challenges of claims 1, 3, 4, 6, and 7

In addition to challenging the patentability of claims 1, 3, 4, 6, and 7 over Hemink's first embodiment alone or in combination with Shudo, Petitioner

challenges the patentability of these claims over Hemink's second embodiment alone or in combination with Shudo. *See* Pet. 26–59. Petitioner further challenges the patentability of these claims over Tsunodo alone or in combination with Shudo or Hemink. *Id.* at 59–85.

As discussed in §§ II.E and II.F, *supra*, we conclude Petitioner has shown by a preponderance of evidence that claims 1, 3, 6, and 7 are unpatentable as obvious over Hemink's first embodiment, and that claim 4 is unpatentable as obvious over Hemink's first embodiment combined with the teachings of Shudo. This conclusion is dispositive of Petitioner's challenge to the patentability of all challenged claims. Accordingly, we need not address whether Petitioner has further shown, by a preponderance of evidence, that the challenged claims are also unpatentable as obvious over Hemink's second embodiment alone or in combination with Shudo, or over Tsunodo alone or in combination with Shudo or Hemink. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984) (finding an administrative agency is at liberty to reach a decision based on a single dispositive issue because doing so "can not only save the parties, the [agency], and [the reviewing] court unnecessary cost and effort," but can "greatly ease the burden on [an agency] faced with a . . . proceeding involving numerous complex issues and required by statute to reach its conclusion within rigid time limits").

III. CONCLUSION

We have reviewed the Petition, Patent Owner's Response and Supplemental Response, Petitioner's Reply, Patent Owner's Sur-Reply and Petitioner's Reply to the Sur-Reply, and the evidence before us. We have considered all of the evidence and arguments presented by Petitioner and Patent Owner, and have weighed and assessed the entirety of this evidence as a whole.

For the reasons discussed in § II.E, *supra*, Petitioner has demonstrated by a preponderance of evidence that claims 1, 3, 6, and 7 are unpatentable as obvious over Hemink. For the reasons discussed in §II.F, *supra*, Petitioner has demonstrated by a preponderance of evidence that claim 4 is unpatentable as obvious over Hemink and Shudo.

IV. ORDER

It is hereby:

ORDERED that claims 1, 3, 4, 6, and 7 of the '085 patent are unpatentable;

FURTHER ORDERED that because this Decision is final a party to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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