UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION and
RENESAS ELECTRONICS AMERICA, INC.
Petitioners,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01869
Patent No. 6,388,330 B1

PATENT OWNER'S NOTICE OF APPEAL

Notice is hereby given, pursuant to 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a) and 90.3(a), that Patent Owner Lone Star Silicon Innovations, LLC hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered on March 25, 2019 in IPR2017-01869 (Paper 33) (attached hereto as Exhibit A), and from all underlying orders, decisions, rulings, and opinions that are adverse to Patent Owner, including, without limitation, those within the Decision on Institution of *Inter Partes* Review, entered on April 10, 2018 (Paper 6).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, the Board's claim constructions, the Board's determination that claims 1, 4–6, 9, and 10 are unpatentable as obvious over M. Igarashi, et al., *The Best Combination of Aluminum and Copper Interconnects for a High Performance 0.18μm CMOS Logic Device*, IEEE Electron Devices Meeting, pp. 829–832 (Dec. 1998), Ex. 1021 ("Igarashi") and M. Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1017 ("Tanaka (1999)"), and all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions; the Board's consideration and analysis of the expert testimony, prior art, and other evidence in the record; and the Board's factual

findings, conclusions of law, or other determination supporting or relating to the above issues.

This Notice of Appeal is timely pursuant to 37 C.F.R. § 90.3, having been duly filed within 63 days after the Final Written Decision. A copy of the Notice of Appeal is being filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice of Appeal is being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit, and the required docketing fee will be paid electronically using pay.gov.

If there is any fee due in connection with the filing of this Notice of Appeal, please charge the fee to Deposit Account No. 06-1135.

Respectfully submitted,

Date: May 28, 2019

/Timothy P. Maloney/
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that, pursuant to 37 C.F.R. §§ 42.6(e)(4) and 90.2, the foregoing PATENT OWNER'S NOTICE OF APPEAL and all accompanying documents, were filed by Priority Mail Express on May 28, 2019, with the Director of the United States Patent and Trademark Office, at the following address:

Director of the U.S. Patent and Trademark Office c/o
Office of the General Counsel
P.O. Box 1450
Alexandria, VA 22313-1450

and that a copy of the foregoing Patent Owner's Notice of Appeal and accompanying documents was filed with the Patent Trial and Appeal Board electronically on February 13, 2019, pursuant to 37 C.F.R. 42.6(b)(1), and that the foregoing Notice of Appeal and accompanying documents were served upon the Petitioner pursuant to 37 C.F.R. 42.6(e)(1) via electronic mail on May 28, 2019, by serving the following attorneys of record as follows:

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The undersigned further certifies that a copy of the foregoing Notice of Appeal and accompanying documents were filed on May 28, 2019 with the United States Court of Appeals for the Federal Circuit through the Court's CM/ECF filing system and that the filing fee is being paid electronically using pay.gov. In accordance with Fed. Cir. Rule 15(a)(1), a paper copy of the foregoing Notice and accompanying documents are also being sent via Priority Mail Express to the clerk of the Federal Circuit at:

Clerk of Court
United States Court of Appeals for the Federal Circuit
717 Madison Place NW
Washington, DC 20439

Date: May 28, 2019

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Exhibit A

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Paper No. 33
Entered: March 25, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION and
RENESAS ELECTRONICS AMERICA, INC.,
Petitioner,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2017-01869
Patent 6,388,330 B1

Before JON B. TORNQUIST, JOHN F. HORVATH, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

Renesas Electronics Corporation and Renesas Electronics America, Inc. ("Petitioner") challenges the patentability of claims 1, 2, 4–7, 9, and 10 ("the challenged claims") of U.S. Patent No. 6,388,330 B1 (Ex. 1001, "the '330 patent"), assigned to Lone Star Silicon Innovations, LLC ("Patent Owner").[1]

We have jurisdiction under 35 U.S.C. § 6. This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

For the reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that the claims 1, 4–6, 9, and 10 of the '330 patent are unpatentable, but has not shown that claims 2 and 7 are unpatentable.

I. BACKGROUND

A. *Procedural History*

Petitioner filed a Petition seeking *inter partes* review of claims 1, 2, 4–7, 9, and 10 of the '330 patent. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 5 ("Prelim. Resp."). We instituted *inter partes* review of claims 1, 4–6, 9, and 10 and denied institution as to claims 2 and 7. Paper 6 ("Institution Decision" or "Dec.").

Following the Supreme Court's decision in *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018), we modified our Institution Decision to include review of all challenged claims on all grounds presented in the Petition. Paper 8.

[1] Patent Owner identifies Longhorn IP LLC as an additional real party-in-interest. Paper 21, 1.

Patent Owner filed a Response. Paper 19 ("PO Resp."). Petitioner filed a Reply. Paper 23 ("Pet. Reply"). With the Board's prior authorization (Ex. 2016), Patent Owner filed a Sur-Reply, and Petitioner filed a Sur-Sur-Reply. Paper 25 ("PO Sur-Reply"); Paper 28.

With the Petition, Petitioner filed a declaration of Dean Neikirk, Ph.D. Ex. 1011. Patent Owner cross-examined Dr. Neikirk and filed a transcript of his deposition testimony as Exhibit 2015 with the Patent Owner Response. With the Reply, Petitioner filed a reply declaration of Dr. Neikirk. Ex. 1028.

With the Preliminary Response, Patent Owner filed a declaration of Wilmer R. Bottoms, Ph.D. Ex. 2001. With the Patent Owner Response, Patent Owner filed a second declaration of Dr. Bottoms. Ex. 2011.

Patent Owner filed a motion to exclude evidence. Paper 24 (PO Mot.).

Oral argument was held January 9, 2019, and a transcript was entered in the record. Paper 32 ("Tr.").

B. Related Matters

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following pending federal court proceedings involving the '330 patent: *Lone Star Silicon Innovations, LLC v. Renesas Electronics Corp.*, Appeal No. 2018-1580 (Fed. Cir., filed Feb. 15, 2018) and *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal., filed Mar. 16, 2018). Paper 21, 2–4. In addition, Patent Owner identifies Federal Circuit Appeal Nos. 2018-1578, 2018-1581, and 2018-1582, in which the defendant-appellees are Micron Technology, Inc., Nanya Technology Corp., and United Microelectronics Corp., respectively. *Id.*; *see also* Paper 31 (Petitioner's updated mandatory notices), 6–7.

Pursuant to 37 C.F.R § 42.8(b)(2), Patent Owner identifies the following *inter partes* review proceedings involving the ’330 patent: *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01566 and *Nanya Technology Corp. v. Lone Star Silicon Innovations, LLC*, Case IPR2018-00062. Paper 21, 2; *see also* Paper 31, 2. Claims 1, 2, 5–7, and 10 of the ’330 patent were found unpatentable in a final written decision entered January 14, 2019, in *Micron Technology, Inc. v. Lone Star Silicon Innovations, LLC*, Case IPR2017-01566 (Paper 24).

C. The ’330 Patent (Ex. 1001)

The ’330 patent is titled “Low Dielectric Constant Etch Stop Layers in Integrated Circuit Interconnects” and was issued May 14, 2002, from Application No. 09/776,012, filed February 1, 2001. Ex. 1001, at (21), (22), (45), (54).

The ’330 patent relates to semiconductor technology and, more specifically, to etch stop layers in integrated circuits. *Id.* at 1:6–8. According to the ’330 patent, semiconductor devices fabricated in and on a semiconductor substrate may be interconnected using a “damascene” technique of metallization. *Id.* at 1:11–29. A “single damascene” technique is used to form a single layer of conductive interconnects, and a “dual damascene” technique is used to form multiple layers of conductive interconnects that are separated by interlayer dielectric layers, including etch stop layers, in vertically separated planes and interconnected by vertical connections or “vias.” *Id.* at 1:30–34, 2:30–51. The ’330 patent discloses that closely positioned, parallel conductive channels suffer from capacitive coupling effects, which can be reduced by reducing the dielectric constant of the silicon nitride etch stop layers between the channels. *Id.* at 3:32–42,

3:49–60. More specifically, the ’330 patent represents that “currently used silicon nitride . . . has a dielectric constant in excess of 7.5” (*id.* at 3:39–41) and discloses that capacitive coupling effects are reduced by using an etch stop layer having a dielectric constant below 5.5 (*id.* at 3:53–54, 3:58–59).

Figure 2 of the ’330 patent shows a “prior art” structure, and Figure 3 shows the invention. Ex. 1001, 4:14–20. Figures 2 and 3 of the ’330 patent are reproduced below:

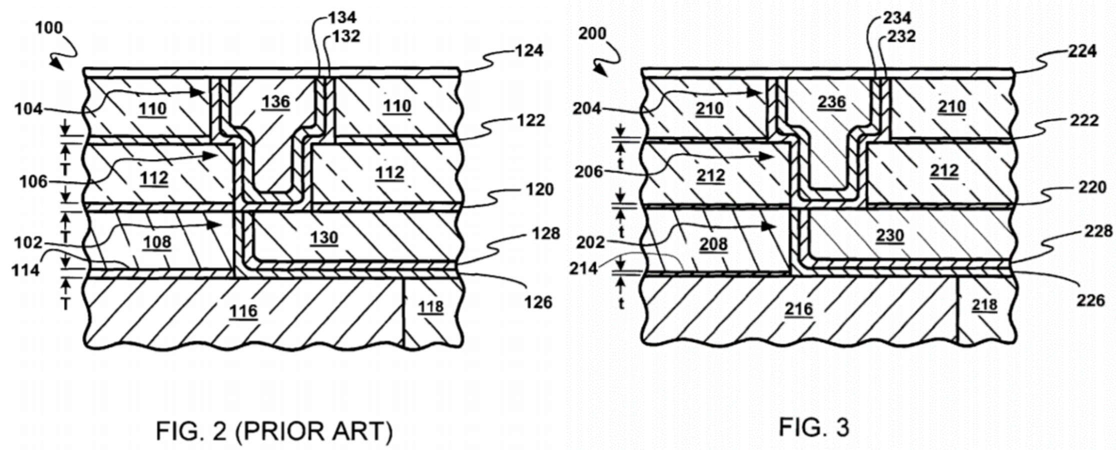


FIG. 2 (PRIOR ART)

FIG. 3

Figures 2 and 3, above, show semiconductor wafers 100, 200, including dielectric layers 108, 110, 112, 208, 210, and 212; conductor cores 130, 136, 230, 236; and etch stop layers 114, 120, 122, 124, 214, 220, 222, and 224.[2] *Id.* at 4:24–32, 4:42–5:4, 5:21–53. According to the ’330 patent, Figure 3 is “similar” to Figure 2, except for the thickness of the etch stop layers, which is shown as “T” in Figure 2 and “t” in Figure 3. *Id.* at 4:18, 5:17–23, 5:66–6:2.

[2] Structures with 100-series reference numerals are shown in Figure 2, and structures with 200-series reference numerals are shown in Figure 3.

Regarding the etch stop layers, the '330 patent discloses:

> In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.
>
> For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

Id. at 5:60–65. The '330 patent discloses processes that can be used to produce etch stop layers with a dielectric constant under 5.5, including successive deposition of multiple layers of silicon nitride, which "eliminates pinholes and produces a denser film." *Id.* at 5:66–6:7.

D. Illustrative Claim

The Petition challenges claims 1, 2, 4–7, 9, and 10 of the '330 patent, of which claims 1 and 6 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An integrated circuit comprising:
>
> a semiconductor substrate having a semiconductor device provided thereon;
>
> a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;
>
> a first conductor core filling the first opening and connected to the semiconductor device;
>
> an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;
>
> a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;
>
> a second conductor core filling the second opening and connected to the first conductor core.

Ex. 1001, 6:54–7:2.

Claim 6 is similar to claim 1, except that it recites an additional dielectric layer (called a via dielectric layer) and an additional etch stop layer (called a channel etch stop layer), and the second conductor core fills openings in both the via and second dielectric layers. *Id.* at 7:15–8:11.

E. Asserted Prior Art References

Petitioner's asserted grounds of unpatentability are based on the following references:

Chooi et al., U.S. Patent No. 6,436,824 B1, issued August 20, 2002, filed July 2, 1999, Ex. 1014 ("Chooi");

Hasegawa, Japanese Application H11-233630, published August 27, 1999, Ex. 1015, Petitioner's certified English translation, Ex. 1016, Patent Owner's certified English translation, Ex. 2008 ("Hasegawa");[3]

M. Tanaka et al., *Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD*, 1999 Symposium on VLSI Technology, Digest of Technical Papers, Session 4B-4, pp. 47–48, Ex. 1017 ("Tanaka (1999)");

M. Tanaka et al., *Film Properties of Low-k Silicon Nitride Films Formed by Hexachlorodisilane and Ammonia*, J. Electrochem. Soc., v. 147, pp. 2284–2289 (2000), Ex. 1018 ("Tanaka (2000)");

[3] Patent Owner asserts that paragraphs 21, 30, and 33 of Petitioner's certified translation of Hasegawa contain translation errors and provides its own independent certified translation. PO Resp. 43 n.5. Because Petitioner bears the burden of proof in this proceeding, and its briefs do not respond to Patent Owner's assertion regarding translation errors, we accept Patent Owner's certified translation of Hasegawa (Ex. 2008) for purposes of this Decision.

M. Igarashi, et al., *The Best Combination of Aluminum and Copper Interconnects for a High Performance 0.18μm CMOS Logic Device*, IEEE Electron Devices Meeting, pp. 829–832 (Dec. 1998), Ex. 1021 (“Igarashi”); and

Ishikawa, Japanese Application 2000-04001, published January 7, 2000, Ex. 1023, certified English translation, Ex. 1024 (“Ishikawa”).

Tanaka (2000) is asserted as prior art to the ’330 patent under 35 U.S.C. § 102(a). Pet. 23. Hasegawa, Tanaka (1999), Igarashi, and Ishikawa are asserted as prior art under 35 U.S.C. § 102(b). *Id.* Chooi is asserted as prior art under 35 U.S.C. § 102(e). *Id.* Petitioner also relies on certain disclosures in the ’330 patent as Admitted Prior Art (“APA”). *Id.* at 11–12.

Petitioner refers to Tanaka (1999), Tanaka (2000), or Chooi, in the alternative, as the “Low-K References.” *Id.* at 12.

F. Instituted Grounds of Unpatentability

We instituted *inter partes* review of the challenged claims based on all grounds of unpatentability asserted in the Petition, which are as follows:

	Reference(s)	**Statutory Basis**	**Claims**
1	APA and Low-K References	35 U.S.C. § 103(a)	1, 5, 6, and 10
2	APA, Low-K References, and either Ishikawa or Hasegawa	35 U.S.C. § 103(a)	2 and 7
3	APA and Chooi	35 U.S.C. § 103(a)	4 and 9
4	Chooi	35 U.S.C. § 102(e)	1, 5, 6, and 10
5	Chooi	35 U.S.C. § 103(a)	4 and 9

	Reference(s)	Statutory Basis	Claims
6	Chooi and either Ishikawa or Hasegawa	35 U.S.C. § 103(a)	2 and 7
7	Igarashi and Tanaka (1999)	35 U.S.C. § 103(a)	1, 4–6, 9, and 10

Pet. 23; Dec. 5; Paper 8.

II. ANALYSIS

A. *Claim Construction*

In this *inter partes* review, the ’330 patent has not yet expired, and claim terms are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b) (2017).[4] Under that standard, we generally give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner contends that the term “silicon nitride” should be construed as “a material having a composition SiN or Si_xN_y.” Pet. 11.

Patent Owner contends that the phrase “etch stop layer of silicon nitride” should be construed as “etch stop layer characterized by the presence of silicon atoms bonded to nitrogen atoms throughout the layer.” PO Resp. 8–9.

[4] A recent amendment to this rule does not apply here, because the Petition was filed before November 13, 2018. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 100(b) effective November 13, 2018).

In the Institution Decision, we determined that it was not necessary to resolve the parties' claim construction dispute. Dec. 9–10. Neither party challenges that determination. Petitioner contends that the asserted grounds of unpatentability apply under either party's construction for the phrase "etch stop layer of silicon nitride." Pet. 25 n.3. Patent Owner argues that this phrase is not limited to a layer of pure silicon nitride and allows for the presence of dopants and/or impurities. PO Resp. 8–10. Patent Owner does not, however, rely on its proposed claim construction for any patentability argument. In fact, Patent Owner acknowledges that the silicon nitride materials disclosed in the Low-K References satisfy Patent Owner's proposed construction. PO Resp. 10. Under these circumstances, we agree with Petitioner that we do not need to resolve the parties' claim construction dispute. Pet. Reply 2. Accordingly, consistent with the Institution Decision, we determine that we do not need to provide an express construction for any claim term for purposes of resolving the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Principles of Law

Petitioner bears the burden of proving unpatentability, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail, Petitioner must establish the facts supporting its challenge by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Neikirk, testifies that a person of ordinary skill in the art ("POSA") would have had a graduate degree in physics, material science, electrical engineering, or a related degree, with some emphasis in semiconductor device fabrication, or an undergraduate degree in one of these fields and two to three years of experience in semiconductor device design and fabrication. Ex. 1011 ¶ 48. Dr. Neikirk further testifies that a POSA would have had at least a basic understanding, through education or experience, of the materials that comprise forming interconnect conductors, dielectrics, and etch stop layers and their properties. *Id.* Patent Owner's declarant, Dr. Bottoms, testifies that a POSA would have held at least a Bachelor's degree in electrical engineering, material science, physics, chemistry or a closely related field and at least five years of industry experience in the fabrication of semiconductor devices. Ex. 2011 ¶ 35. Dr. Bottoms further testifies that an individual with an advanced degree in a

relevant field would require less experience in semiconductor fabrication. *Id*.

For purposes of our Institution Decision, we accepted the definition of a POSA provided by Dr. Bottoms. Dec. 10–11 (citing Ex. 2001 ¶ 31). Dr. Bottoms provides a "clarification" of the Board's description, testifying that "[t]he specific industry experience would require process design experience—which is experience beyond managing fabrication equipment." Ex. 2011 ¶ 36. Dr. Bottoms' clarification is consistent with the level of skill reflected by the '330 patent, which discloses process design options for making a low dielectric constant silicon nitride etch stop. Ex. 1001, 5:66-6:24. Dr. Neikirk testifies that, under Dr. Bottoms' definition, a POSA has a higher degree of skill than under Dr. Neikirk's definition, and the Board's adoption of Dr. Bottoms' definition would not change his opinions regarding obviousness. Ex. 1028 ¶ 14.

We find there is little difference between the declarants' definitions of a POSA, and the outcome of our patentability determinations would be the same, regardless of which definition we accept. For the sake of clarity, we adopt Dr. Bottoms' definition of a POSA, including the recent clarification. Ex. 2011 ¶¶ 35, 36. We also rely on the cited prior art references as reflecting the level of ordinary skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

After reviewing the qualifications of Dr. Neikirk and Dr. Bottoms, as set forth in each witness's declaration and curriculum vitae, we find that each of these declarants has sufficient education and experience related to the subject matter of the '330 patent to testify regarding the perspective of a POSA at the time of the invention. Ex. 1011 ¶¶ 2, 3; Ex. 1012; Ex. 2002;

Ex. 2011 ¶¶ 8–20. *See Trial Practice Guide Update*, 83 Fed. Reg. 39,989 (Aug. 13, 2018), *available at* https://go.usa.gov/xU7GP ("TPG Update"), 3 ("A person may not need to be a person of ordinary skill in the art in order to testify as an expert under Rule 702, but rather must be 'qualified in the pertinent art.'" (quoting *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008))).

D. Overview of Asserted Prior Art References

Below we provide an overview of Tanaka (1999), Igarashi, Ishikawa, and Hasegawa. It is not necessary to summarize the remaining prior art references for purposes of resolving the controversy.

1. Tanaka (1999) (Ex. 1017)

Tanaka (1999) is an article titled, "Low-k SiN Film for Cu Interconnects Integration Fabricated by Ultra Low Temperature Thermal CVD." Ex. 1017.[5] Tanaka (1999) addresses the problem of parasitic capacitance associated with copper (Cu) interconnects formed by a conventional damascene process that uses "high-k SiN film" for the etch stopper layers. *Id.* at 47-1.[6] Tanaka (1999) cites Igarashi as an example of a

[5] In Tanaka (1999) and other references, the letter "k" is used to refer to permittivity or dielectric constant. Ex. 1017 (Title, Abstract); Ex. 1018 (Title, Abstract); Ex. 1019, 4:32; Ex. 1021, 829-1. Dr. Neikirk explains, "[w]hen Tanaka (1999) refers to the 'permittivity' of silicon nitride, he refers to its relative dielectric constant" and "[p]ermittivity and dielectric constant are synonymous, in this context." Ex. 1011 ¶ 77. Dr. Bottoms agrees that "[p]ermittivity as used in Tanaka (1999) means relative permittivity and is synonymous with dielectric constant." Ex. 2011 ¶ 79 n.1.

[6] We cite to Tanaka (1999) and other non-patent references using a page number of the original document followed by a hyphenated suffix ("-1" or "-2") to indicate the first or second column.

copper interconnect that is degraded by parasitic capacitance due to the high permittivity of silicon nitride. *Id.* at 47-1 n.1. To solve this problem, Tanaka (1999) discloses a "[n]ew low-k SiN film with a permittivity of 5.4 and high immunity for Cu diffusion and oxidation . . . ." *Id.* at 47-1, 47-2. The silicon nitride film is formed by an ultra low temperature thermal chemical vapor deposition ("CVD") process using HexaChloroDisilane (HCD, Si_2Cl_6) as a silicon source. *Id.* at 47-1. Tanaka (1999) refers to the new film as "HCD-SiN" and discloses a deposition process and film properties for the new film. *Id.* at 47-1, 47-2, Figs. 2–8.

Figure 1 of Tanaka (1999) is reproduced below:

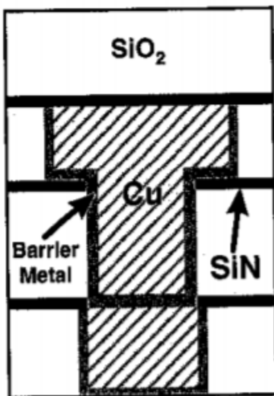


Fig.1 A schematic drawing of Cu interconnects formed by damascene process

Figure 1 of Tanaka (1999) shows copper interconnects formed by a conventional damascene process, which requires "plural layers of high-k SiN film for a groove etch stopper and a barrier of Cu diffusion and oxidation." Ex. 1017, 47-1. As explained above, Tanaka (1999) proposes improving this conventional process by using "HCD-SiN as the etch-stop

and the barrier layer . . . to realize Cu damascene interconnects for high performance VLSIs."[7] *Id.*

2. Igarashi (Ex. 1021)

Igarashi is an article titled, "The Best Combination of Aluminum and Copper Interconnects for a High Performance 0.18µm CMOS Logic Device."[8] Ex. 1021. Igarashi discloses a six-level interconnect system consisting of four-level aluminum (Al) interconnects made by a conventional process and two-level copper (Cu) interconnects made by a dual damascene process. *Id.* at 829-1. Igarashi acknowledges that formation of Cu interconnects by a damascene process requires the use of high-k dielectric films, e.g., silicon nitride (Si_3N_4), for etch stoppers and for prevention of Cu oxidation and diffusion. *Id.* Igarashi investigates the influence of high-k dielectric films on the interconnect delay time and proposes "the best combination of Al and Cu interconnects" for high speed devices. *Id.*

Figure 1 of Igarashi is reproduced below:

[7] The acronym VLSI refers to very large scale integrated devices. *See* Ex. 1018, 2284-1.

[8] The acronym CMOS refers to Complementary Metal Oxide Semiconductor.

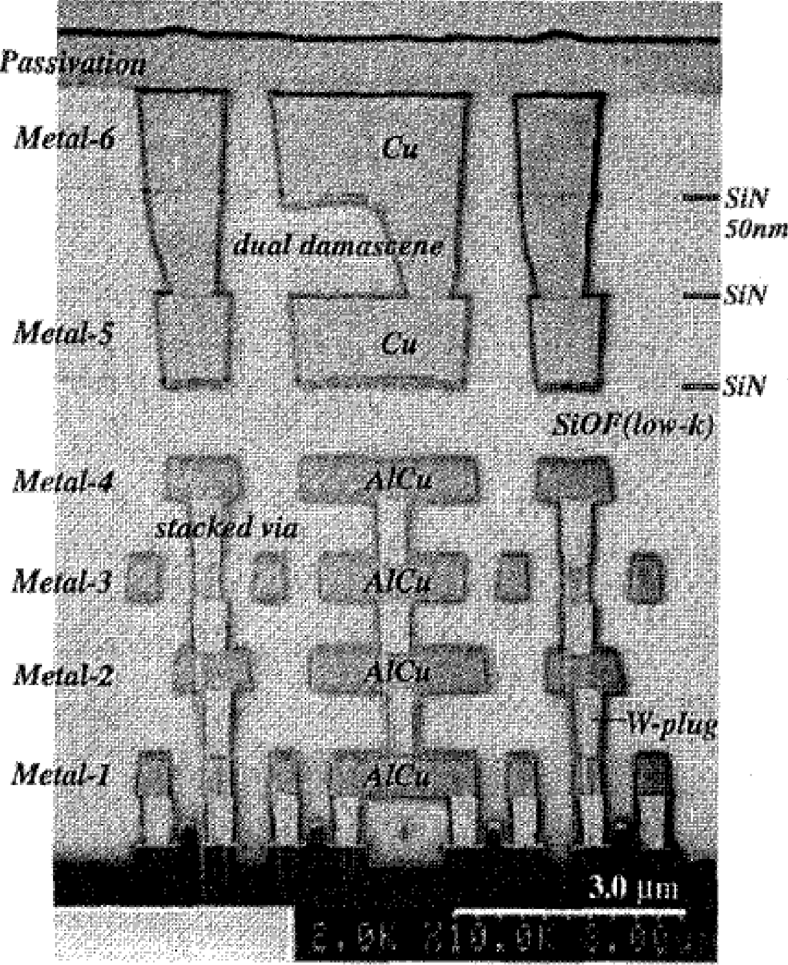


Fig. 1 : Cross sectional view of CMOS structure with six-level interconnects

Igarashi Figure 1 shows a cross sectional view of a CMOS structure with six-level interconnects, including four-level Al interconnects and two-level Cu interconnects. Ex. 1021, 829-2, 831-1 (Fig. 1). Igarashi discloses that the CMOS structure of Figure 1 uses a SiOF intermetal dielectric film with a dielectric constant of 3.5 to reduce parasitic capacitance. *Id.* at 829-2. According to Igarashi, tungsten (W) plugs for contact and via holes are employed for the Al interconnects and Cu plugs and Cu wiring are formed by a dual damascene process. *Id.* Igarashi discloses that Si_3N_4 films for the

Cu interconnect system act as a damascene etching stopper and prevent Cu oxidation and diffusion. *Id.*

Igarashi states that Si_3N_4 films are necessary for Cu interconnects, but "it is not desirable for the interconnects to contain such a Si_3N_4 film with a 'high-k' dielectric, because the effective dielectric constant clearly increases." Ex. 1021, 829-2. To address this problem, Igarashi studies the Al and Cu wiring structure, including thickness and pitch, that minimizes parasitic resistance and inverter delay time. *Id.* at 829-2–830-1. Igarashi concludes that "Al interconnects with lower parasitic capacitance are suitable for fine metal pitch and short distance wiring, and Cu interconnects with lower resistivity are useful for coarse metal pitch and long distance wiring." *Id.* at 830-2.

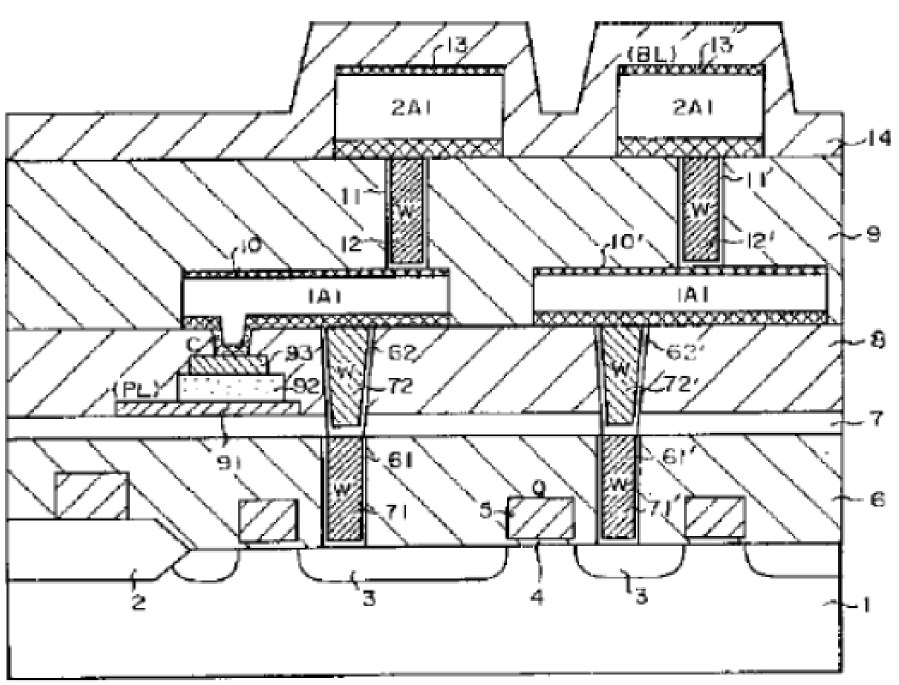
3. Ishikawa (Ex. 1024)

Ishikawa is a Japanese patent publication titled, "Semiconductor memory device and production method thereof." Ex. 1024, at (54). Ishikawa discloses a semiconductor memory device having first and second contact holes. *Id.* at (57), ¶ 1. The problem addressed by Ishikawa is to suppress "connection wiring material in the first contact holes [from] piercing a barrier metal layer and diffusing into an impurity diffusion region." *Id.* at (57). The solution proposed by Ishikawa is an insulating film comprising a silicon nitride film formed by a low-pressure CVD method and a silicon nitride film formed by a plasma CVD method. *Id.* The film is used as an intermediate insulating film between insulating films having first and second contact holes formed therein and as a mask when etching the second contact holes. *Id.* According to Ishikawa, "[s]ince the plasma CVD method is performed at approximately 200 to 300°C, the barrier metal layer in the

first contact holes is not destroyed, and the diffusion of connection wirings made of W or the like is not activated." *Id.*

Figure 12 of Ishikawa is reproduced below:

[FIG. 12]



Ishikawa Figure 12 depicts a conventional semiconductor memory device, including semiconductor substrate 1 and transistor Q consisting of source/drain impurity diffusion region 3, gate oxide film 4, and gate electrodes 5. Ex. 1024, p. 10 (Brief Description of the Drawings), ¶¶ 4, 5. The layers above semiconductor substrate 1 include sequentially: first insulating film 6, intermediate insulating film 7, and second insulating film 8. *Id.* ¶¶ 4–6, Fig. 12. First contact holes 61 and 61' are formed in first insulating film 6, and second contact holes 62 and 62' are formed in second insulating film 8 and intermediate insulating film 7. *Id.* ¶¶ 4, 6. Connection wirings 71 and 71' are embedded in contact holes 61 and 61', respectively,

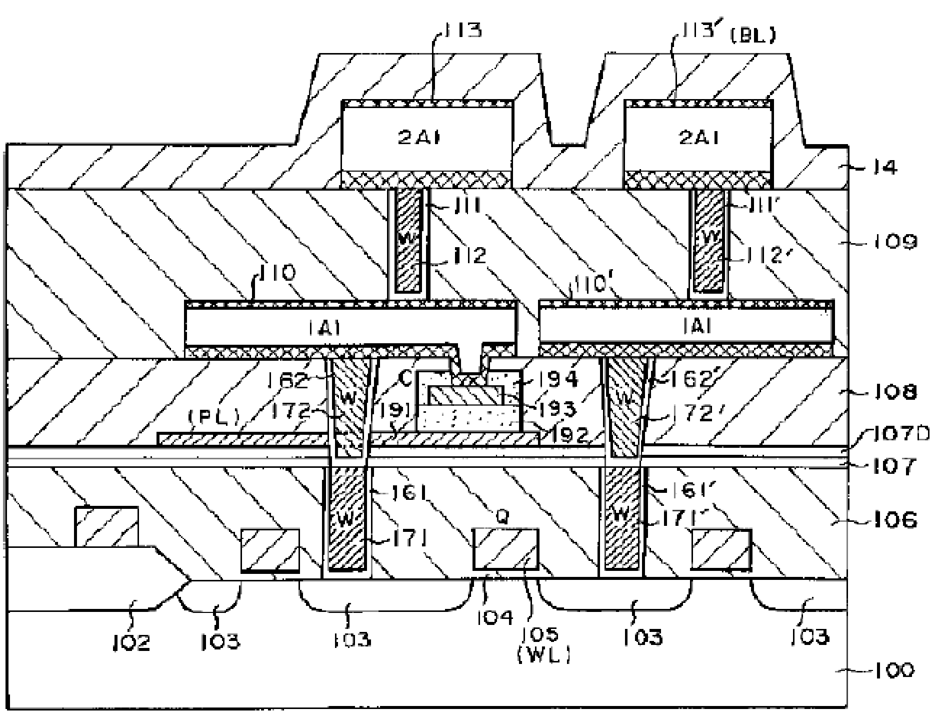
and are connected to connection wirings 72 and 72' embedded in contact holes 62 and 62'. *Id.* The embedded wirings include three layers: a titanium (Ti) film, a titanium nitride (TiN) film, and a tungsten (W) film. *Id.* ¶¶ 5, 6. Ishikawa explains that "intermediate insulating film 7 is formed as a protective film on the first insulating film 6 in order to suppress the oxidation of the tungsten film embedded in the first contact holes 61 and 61'." *Id.* ¶ 5. Intermediate insulating film 7 is a silicon nitride film formed by low-pressure CVD at a film forming temperature of 700 to 780°C and a film forming rate of 0.8 to 1.5 nm/min. *Id.*

Ishikawa addresses a problem that arises in fabricating the above-described structure, namely: "when a silicon nitride film (SiN) deposited by a low-pressure CVD method is used for the etching mask when forming the second contact holes, the tungsten pierces the barrier metal layer (Ti film/TiN film) at the bottom corners of the first contact holes and is diffused to the impurity diffusion region formed on the semiconductor substrate." Ex. 1024 ¶ 10. Ishikawa's proposed solution is "an insulating film comprising a silicon nitride film formed by a low-pressure CVD method and a silicon nitride film formed by a plasma CVD method [that] is used as an intermediate insulating film which is inserted between insulating films having first and second contact holes formed therein and used for a mask when etching the second contact holes." *Id.* ¶ 11. More particularly, Ishikawa discloses that the intermediate insulating film comprises first and second silicon nitride films formed by a low-pressure CVD method and a third silicon nitride film sandwiched by the first and second silicon nitride films and formed by a plasma CVD method. *Id.* ¶ 13. According to Ishikawa, "[s]ince the plasma CVD method is performed at a low

temperature (approximately 200 to 300°C), the barrier metal layer formed in the first contact holes is not destroyed, and the diffusion of connection wiring made of tungsten or the like is not activated." *Id.* ¶ 11.

Figure 1 of Ishikawa is reproduced below:

[FIG. 1]

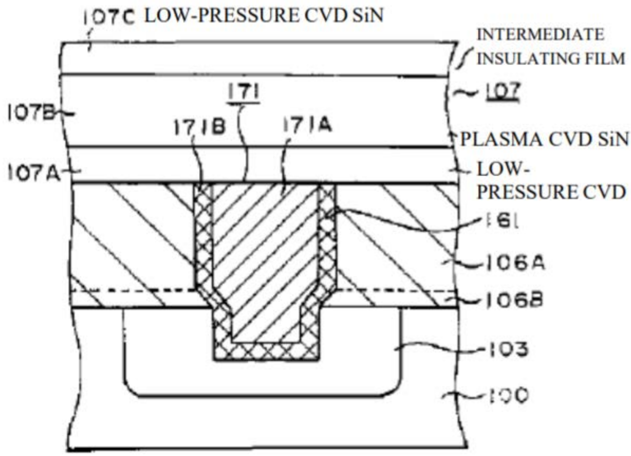


Ishikawa Figure 1 depicts a semiconductor memory device according to Ishikawa's invention. Ex. 1024, p. 10 (Brief Description of the Drawings). The device includes intermediate insulating film 107, which is formed as a protective film on the first insulating film 106 in order to suppress the oxidation of the tungsten film embedded in the first contact holes 161 and 161'. *Id.* ¶¶ 16, 18. According to Ishikawa, the intermediate insulating film 107 is made of a silicon nitride film (PCVDSiN) formed by a plasma CVD method and a silicon nitride film (LPCVDSiN) formed by a low-pressure

CVD method. *Id.* ¶ 18. The device further includes TEOS film 107D. *Id.* ¶ 23.[9]

Figure 6 of Ishikawa is reproduced below.

[FIG. 6]



Ishikawa Figure 6 depicts a portion of a semiconductor device, including a semiconductor substrate having an intermediate insulating film formed on a contact hole. Ex. 1024, p. 10 (Brief Description of the Drawings), ¶ 20. With reference to Figure 6, Ishikawa discloses that intermediate insulating film 107 is made of three layers of CVD films, the first layer of which is a silicon nitride film (LPCVDSiN) 107A formed by a low-pressure CVD method, the second layer of which is a silicon nitride film (PCVDSiN) 107B formed by a plasma CVD method, and the third layer of which is a silicon nitride film (LPCVDSiN) 107C formed by a low-pressure CVD method. *Id.* ¶ 22. According to Ishikawa, "by using a silicon nitride film formed by a plasma CVD method in addition to silicon nitride films formed by a

[9] Ishikawa explains that "TEOS film" refers to a silicon oxide (SiO_2) film formed by thermally decomposing tetraethoxysilane ($Si(OC_2H_5)_4$), which is abbreviated as TEOS. Ex. 1024 ¶ 6.

conventional low-pressure CVD method so as to establish a three-layer structure, it is possible to suppress the piercing of the barrier metal layer by tungsten in the corner edge portions of the base surfaces of the first contact holes due to the effects of thermal stress." *Id.* ¶ 27.

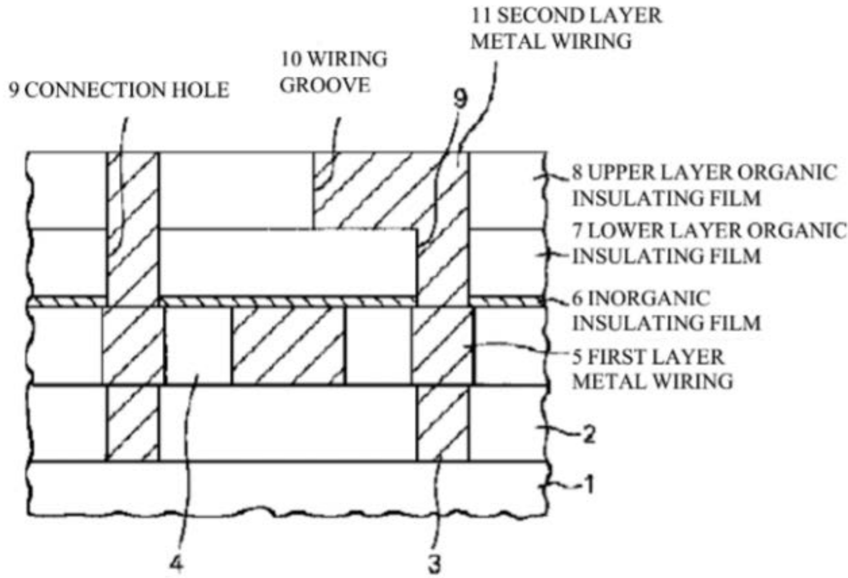
4. Hasegawa (Ex. 2008)

Hasegawa is a Japanese patent publication titled, "Method of Manufacturing Semiconductor Device and Semiconductor Device Using the Same." Ex. 2008, at (54). Hasegawa explains that, to meet the demand for low power consumption, high speed semiconductor devices, it is necessary to use low resistance wiring materials and interlayer insulating film materials having a low dielectric constant. *Id.* ¶ 2. According to Hasegawa, organic insulating film materials are one type of low dielectric constant material. *Id.* ¶¶ 3, 5.

The problem addressed by Hasegawa is preventing oxidation of metal wiring when opening a contact hole in an organic insulating film on oxidizable metal wiring, such as copper (Cu) wiring formed in a dual damascene process. *Id.* at (57), ¶¶ 11–13. Hasegawa's solution is to provide a thin inorganic insulating film beneath the organic insulating film such that the final contact hole-opening step can be conducted by dry etching without the use of an oxygen active species. *Id.* at (57), ¶¶ 14, 21. Hasegawa provides examples of inorganic insulating films, including silicon oxide, silicon oxynitride, and silicon nitride. *Id.* ¶ 16. Hasegawa states that "these insulating films can be used with single layer or multiple layers." *Id.*

Figure 1 of Hasegawa is reproduced below:

[FIG. 1]



Hasegawa Figure 1 is a cross-sectional view illustrating the main parts of a semiconductor device. Ex. 2008, p. 14 (Brief description of the drawings). More particularly, Figure 1 shows silicon semiconductor substrate 1, lower layer interlayer insulating film 2, lower layer contact plug 3, first layer interlayer insulating film 4, first layer metal wiring 5, inorganic insulating film 6, lower layer organic insulating film 7, upper layer organic insulating film 8, connecting hole 9, wiring groove 10, and second layer metal wiring 11. *Id.* ¶¶ 25–27. According to Hasegawa, first layer metal wiring 5 is Cu-based metal. *Id.* ¶ 29. Hasegawa discloses that interlayer insulating film 6 functions to protect first layer metal wiring 5 from oxygen active species in the later process. *Id.* ¶ 30. In Hasegawa's embodiment 1, inorganic insulating film 6 can be silicon oxide, silicon oxide nitride, and/or silicon nitride. *Id.* ¶¶ 31–33.

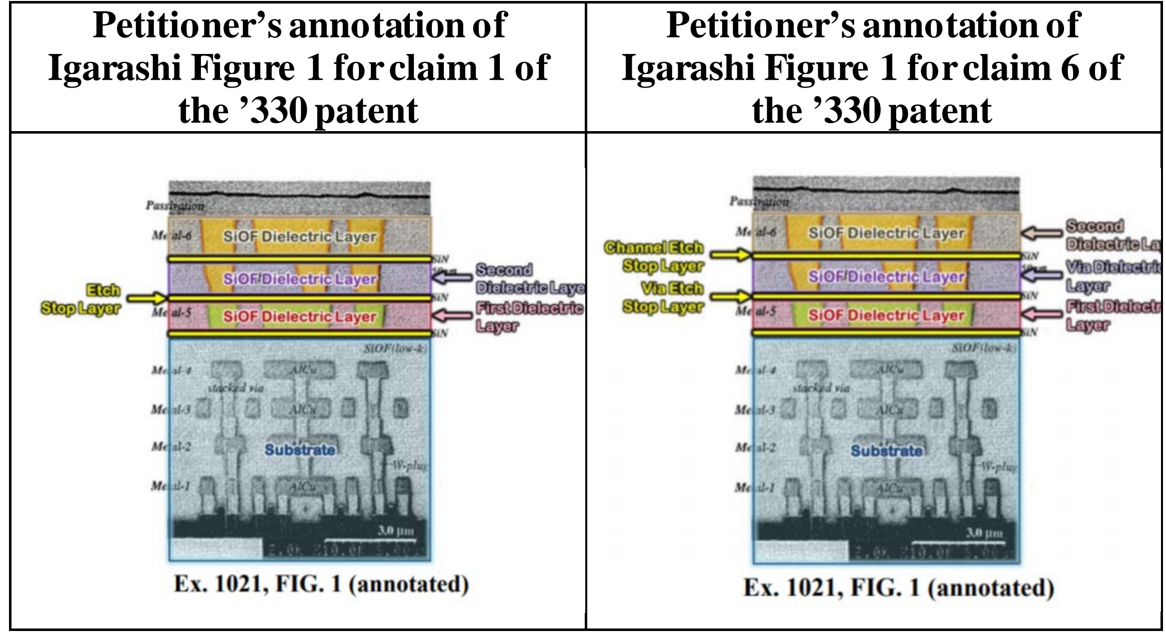
E. Petitioner's Challenge Based on Igarashi and Tanaka (1999)

Petitioner contends that claims 1, 4–6, 9, and 10 of the '330 patent are unpatentable as obvious in view of Igarashi and Tanaka (1999). Pet. 53–64. We address each of these claims below.

1. Claims 1 and 6

Petitioner contends that Igarashi teaches all elements of independent claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 55–62; *see also id.* at 17–18 (summarizing Igarashi). As support for that contention, Petitioner provides the following annotations of Igarashi Figure 1:

Petitioner's annotation of Igarashi Figure 1 for claim 1 of the '330 patent	**Petitioner's annotation of Igarashi Figure 1 for claim 6 of the '330 patent**



Ex. 1021, FIG. 1 (annotated)

Ex. 1021, FIG. 1 (annotated)

Id. at 55, 58; Ex. 1011 ¶¶ 356, 397. Igarashi Figure 1 shows a cross sectional view of a CMOS structure and is annotated by Petitioner to identify a substrate, three dielectric layers, and two etch stop layers.

Petitioner contends that Tanaka (1999) "teaches to modify Igarashi's integrated circuit to provide silicon nitride etch stop layers . . . having a

dielectric constant of 5.4." Pet. 57, 60. Petitioner asserts that a POSA would have had a reason to combine the teachings of Tanaka (1999) and Igarashi because "Tanaka (1999) cites Igarashi expressly as an example of a copper interconnect system that is degraded by parasitic effects through use of silicon nitride films with high dielectric constants." *Id.* at 53 (citing Ex. 1017, 47-1 n.1). Petitioner further asserts that a POSA would have been motivated to employ the low dielectric constant silicon nitride film of Tanaka (1999) in the interconnect system of Igarashi to overcome the problems experienced by Igarashi. *Id.* at 54.

Patent Owner argues Petitioner fails to establish that a POSA would have had a reasonable expectation of success when implementing the materials disclosed in the Tanaka (1999) in the structure disclosed in Igarashi. PO Resp. 65. According to Patent Owner, a POSA "would not expect success based on the disclosures in Tanaka (1999) because it discloses preliminary and incomplete information related to the HCD-SiN material." *Id.* (cross-referencing § III.B.3. of the Response); *see also id.* at 29–37 (§ III.B.3.).

Patent Owner does not dispute Petitioner's contention that Igarashi discloses an integrated circuit that meets all limitations of claims 1 and 6, except for the dielectric constant of the silicon nitride etch stop layer. Pet. 17–18, 55–62; *see* PO Resp. 64–66. Relying on Petitioner's annotated versions of Igarashi Figure 1 (reproduced above) and evidence cited by Petitioner, we find Petitioner has shown by a preponderance of the evidence that all limitations of claims 1 and 6 are disclosed by Igarashi, except for the

dielectric constant of the silicon nitride etch stop layer. Pet. 17–18, 55–62; Ex. 1011 ¶¶ 88–95, 354–383, 395–427;[10] Ex. 1021, 829–831, Fig. 1.

Patent Owner does not dispute Petitioner's contention that Tanaka (1999) discloses a silicon nitride etch stop layer having a dielectric constant of 5.4, i.e., below 5.5, as recited in claims 1 and 6. Pet. 12, 53; *see* PO Resp. 14, 17 (agreeing Tanaka (1999) discloses HCD-SiN film having permittivity (dielectric constant) of 5.4, which can function as an etch stop). Relying on evidence cited by Petitioner, we find Petitioner has proven its contention by a preponderance of the evidence. Pet. 12, 53; Ex. 1011 ¶¶ 74–79, 351; Ex. 1017, 47-1 (disclosing "[n]ew low-k SiN film, with permittivity of 5.4" as an etch stop layer for copper damascene interconnects).[11]

Patent Owner does not dispute Petitioner's contention that a POSA would have had a reason to combine the teachings of Tanaka (1999) and Igarashi and would have been motivated to employ the low dielectric constant silicon nitride film of Tanaka (1999) in the interconnect system of Igarashi. Pet. 53–55, 57–58, 60; *see* PO Resp. 64–66. Petitioner's contention is supported by the unrebutted testimony of Dr. Neikirk. Ex. 1011 ¶¶ 351, 353, 356, 373, 397, 414, 422.

Petitioner's contention is also supported by the express disclosures of Tanaka (1999) and Igarashi relied upon by Petitioner. Igarashi states that

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[10] Petitioner cites Dr. Neikirk's testimony (Ex. 1011) by section number, and we cite to the same testimony by paragraph number. Although Petitioner cites Ex. 1011 § XV.D. in its claim chart for claim 6 (Pet. 58–62), we understand the correct citation is Ex. 1011 § XV.E., which corresponds to paragraphs 395–427 of Dr. Neikirk's testimony.

[11] In Tanaka (1999), "permittivity" and the letter "k" refer to dielectric constant. *See* p. 14 n.6, *supra*.

copper interconnects need silicon nitride films as an etch stop, but that such films have a high dielectric constant, which causes an undesirable increase in the effective dielectric constant of the interconnect structure and increased parasitic capacitance, as compared with aluminum interconnects. Ex. 1021, 829-1, 829-2; *see* Pet. 18; Ex. 1011 ¶¶ 92, 93. As Petitioner correctly points out (Pet. 53–54), Tanaka (1999) cites Igarashi as an example of a copper interconnect system that is degraded by parasitic capacitance due to the high permittivity (dielectric constant) of silicon nitride etch stop films. Ex. 1017, 47-1 n.1. Tanaka (1999) discloses a low dielectric constant silicon nitride etch stop film as a solution to the problem of parasitic capacitance in copper damascene interconnect structures, such as Igarashi's. *Id.* at 47-1, 47-2 ("New low-k SiN film, with a permittivity of 5.4 . . . should be the solution to realize Cu damascene interconnects . . . ."). Consistent with these express disclosures, Dr. Neikirk persuasively testifies that "Igarashi identifies a need for a low-k dielectric etch stop layer" and "Tanaka (1999) meets this need." Ex. 1011 ¶ 94; *see* Pet. 18 (citing Ex. 1011, § VIII.C., which contains paragraph 94 of Dr. Neikirk's testimony).

Accordingly, we find Petitioner has shown by a preponderance of the evidence that a POSA would have been motivated to use the low dielectric constant silicon nitride etch stop film of Tanaka (1999) as the etch stop layer in the interconnect system of Igarashi.

Patent Owner disputes whether Petitioner has established a reasonable expectation of success for the combination of Tanaka (1999)'s low dielectric constant silicon nitride etch stop film and Igarashi's interconnect structure. PO Resp. 65. Although the Petition does not expressly discuss whether one of ordinary skill in the art would have had a reasonable expectation of

success in combining Tanaka and Igarashi to arrive at the claimed invention, Petitioner shows a very close relationship between the teachings of Tanaka (1999) and Igarashi. Pet. 12–13, 17–18, 53–62. As discussed above and argued by Petitioner, Tanaka (1999): (1) cites Igarashi as an example of a copper interconnect system that suffers from parasitic capacitance due to the high dielectric constant of silicon nitride etch stop films, and (2) discloses a low dielectric constant silicon nitride etch stop film as a solution to the parasitic capacitance problem exemplified by Igarashi. Pet. 13, 18, 53–54; Ex. 1011 ¶¶ 74–79, 88–94; Ex. 1017, 47-1 & n.1; Ex. 1021, 829-1, 829-2. Petitioner establishes a reasonable expectation of success for the combination of Tanaka (1999) and Igarashi by demonstrating a strong correlation between the problem discussed by Igarashi—the high dielectric constant of silicon nitride films when used as etch stops for copper interconnects—and the solution disclosed by Tanaka (1999)—a low dielectric constant silicon nitride film for use as an etch stop layer in copper damascene interconnect structures. *In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001) ("[T]he strength of the correlation between the references gives rise to a reasonable expectation of success from combining them.").

Patent Owner does not separately develop its argument challenging Petitioner's combination of Igarashi and Tanaka (1999), relying instead on arguments directed to the combination of the APA and the Low-K References. PO Resp. 65 (cross-referencing § III.B.3. of the Response); *id.* at 29–37 (§ III.B.3.); *see also id.* at 14–23 (summary and criticism of Tanaka (1999) and Tanaka (2000)). We address Patent Owner's arguments only to

the extent they are relevant to Petitioner's combination of Igarashi and Tanaka (1999).

Patent Owner argues that Tanaka (1999) presents only "preliminary findings" and "prospective statements" and lacks sufficient information to prove that Tanaka (1999)'s low dielectric constant HCD-SiN material would function as an etch stop layer. PO Resp. 17, 20, 29, 31 (citing Ex. 2011 ¶¶ 84, 85, 109, 124). Patent Owner argues that Tanaka (1999)'s HCD-SiN functions as an etch stop layer "only" when used with one type of silicon oxide film—TEOS-SiO.[12] *Id.* at 17 (citing Ex. 2011 ¶ 84). In addition, Patent Owner identifies factors it contends are critical to the ability of a silicon nitride film to act as an etch stop, suggesting that Tanaka (1999)'s disclosure is deficient as to these factors. *Id.* at 32–33 (citing Ex. 2011 ¶¶ 113, 127).

We agree with Petitioner that Patent Owner's arguments do not accurately characterize Tanaka (1999), which undisputedly teaches the use of a low dielectric constant silicon nitride film as an etch stop layer. Pet. Reply 4, 25; PO Resp. 30–31 (Tanaka (1999) "disclose[s] an HCD-SiN material that 'should be' usable as an etch stop layer."); Ex. 1017, 47-1 (Abstract: "HCD-SiN as the etch-stop and the barrier layer should be the solution to realize Cu damascene interconnects for high performance VLSIs."). Tanaka (1999) backs up this assertion with more detailed disclosures regarding the ability of the low dielectric constant silicon nitride film to function as an etch stop. For example, Tanaka (1999) states that

[12] According to Patent Owner and its expert, TEOS refers to tetraethyl orthosilicate, which is a precursor used to form one type of silicon oxide film, referred to as TEOS-SiO. PO Resp. 17; Ex. 2011 ¶ 84.

"HCD-SiN has same RIE etching resistance as conventional LPCVD SiN." *Id.* at 47-1 (Abstract); *see* Pet. Reply 10–11 (quoting Tanaka (1999) Abstract). In Figure 6, Tanaka (1999) compares the etching rate selectivity for HCD-SiN films to the etching rate selectivity for a DCS-SiN film.[13] Ex. 1017, 48, Fig. 6. Based on Figure 6, Tanaka (1999) states that "selectivity of RIE etching rate showed no significant deposition temperature dependence." *Id.* at 47-2. From this result, Tanaka (1999) concludes that HCD-SiN has "enough ability for etching stopper." *Id.*; *see* Pet. Reply 6 (quoting Tanaka (1999)). Petitioner accurately characterizes Tanaka (1999) as "bullish" that he "successfully developed" a low dielectric constant silicon nitride film that "works well as an etch-stop." Pet. Reply 11, 25 (citing Ex. 1017, 47-2).

As to the suitability of Tanaka (1999)'s HCD-SiN film as an etch stop with dielectric layers other than TEOS-SiO, we credit the unrebutted testimony of Dr. Neikirk that "knowing how HCD-SiN works with TEOS informs a POSITA of how it would work with other insulators, especially oxides deposited using other source gases than TEOS" and a "POSITA would view the HCD-SiN layer as suitable for use not only with TEOS oxides, but a wide range of oxides deposited using other techniques." Ex. 1028 ¶ 19; *see* Pet. Reply 6 (relying on paragraph 19 of Dr. Neikirk's testimony).

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[13] Patent Owner explains that DCS-SiN film would be understood to be a conventional SiN material. PO Resp. 33. According to Tanaka (2000), "DCS-SiN" refers to a silicon nitride film deposited by chemical vapor deposition using dichlorosilane (DCS, SiH_2Cl_2) as a silicon source. Ex. 1018, 2284-1.

Patent Owner's arguments demand more from the prior art disclosure in Tanaka (1999) than is provided by the sparse disclosure of the '330 patent. Most of the information Patent Owner argues is missing from Tanaka (1999) to establish its suitability as an etch-stop layer is not disclosed by the '330 patent. For example, the '330 patent does not disclose etch chemistries, etch selectivity, or the thickness of the dielectric layers being etched. *Cf.* PO Resp. 33 (listing chemistry of the etchant and relative thickness of the materials as factors affecting suitability as an etch stop); *id.* at 17 (asserting that Tanaka (1999) does not disclose etch selectivity of HCD-SiN relative to any type of silicon oxide other than TEOS-SiO). Nor does the '330 patent disclose any information regarding the barrier property of silicon nitride etch stop layers. *Cf.* PO Resp. 33 (asserting that the barrier property is "critical"). Tanaka (1999) provides at least as much, if not more, information than the '330 patent regarding suitability of low dielectric constant silicon nitride as an etch stop layer. Ex. 1017, 47-2, 48, Fig. 6 ("Selectivity of RIE etching rate versus TEOS"). The '330 patent's sparse disclosure, as compared with Tanaka (1999)'s more detailed disclosure, persuades us that Tanaka (1999)'s disclosure is sufficient to provide a reasonable expectation of success of achieving the claimed invention. *See Trustees of Columbia Univ. in City of New York v. Illumina, Inc.*, 620 F. App'x 916, 929 (Fed. Cir. 2015) (relying on disclosure of challenged patent as substantial evidence sufficient to support PTAB's finding of a reasonable expectation of success in combining prior art references and synthesizing the claimed nucleotide).

Patent Owner criticizes Tanaka (1999) for not disclosing an "actual application" or "finished device" and faults Petitioner for not submitting

evidence that the HCD-SiN disclosed in Tanaka (1999) "was ever implemented as an etch stop layer in a commercial product." PO Resp. 30–31, 36; *see also* Tr. 25:20-21 (Patent Owner: "you're not going to make an integrated circuit in a way that simply isn't going to make you money"). We agree with Petitioner, however, that Patent Owner's criticisms are legally irrelevant to the question of reasonable expectation of success. Pet. Reply 5. The prior art does not need to disclose "actual success" in making the claimed invention. *AstraZeneca LP v. Breath Ltd.*, 603 F. App'x 999, 1002 (Fed. Cir. 2015). What is required is proof that "a skilled artisan would have perceived a reasonable expectation of success in making the invention in light of the prior art." *Id.* (quoting *Amgen Inc. v. F. Hoffman–La Roche Ltd.*, 580 F.3d 1340, 1362 (Fed. Cir. 2009)). Under that standard, there is no requirement that a POSA have a reasonable expectation of success in developing a commercial product. *Allergan, Inc. v. Sandoz Inc.*, 726 F.3d 1286, 1292 (Fed. Cir. 2013). And the teachings of the prior art should not be discounted merely because a prior art device or process "was not practical and could not be used successfully commercially." *Trojan, Inc. v. Shat-R-Shield, Inc.*, Nos. 88-1528, 88-1529, 1989 WL 12862213, *2 (Fed. Cir. Oct. 31, 1989) (unpublished).

Patent Owner criticizes Tanaka (1999) as disclosing HCD-SiN material having a low dielectric constant "only when that material is formed at low temperatures." PO Resp. 29; *see also id.* at 14 ("[W]hile Tanaka (1999) discloses that the HCD-SiN film may have a permittivity of 5.4, that property only occurs in films deposited at 450 degrees Celsius."); *id.* at 21, 33, 36 (same); *id.* at 34 ("Tanaka (1999) teaches that dielectric constant increases with decreased deposition temperature."). Similarly, Patent Owner

argues that Tanaka (1999)'s HCD-SiN film with a permittivity of 5.4 was formed at a deposition rate of "only 0.6 nm/min.," which is below what Tanaka (1999) characterizes as a "practical" deposition rate of 1.4 nm/min. *Id.* at 36–37 (citing Ex. 1017, 47-1, 48, Fig. 2); *see also id.* at 14 ("The deposition rate for the material disclosed in Tanaka (1999) is substantially lower than deposition rates associated with conventional SiN materials.") We agree with Petitioner, however, that Patent Owner's arguments are irrelevant in view of the breadth of the challenged claims. Pet. Reply 5. The claims recite no limit on the deposition temperature or the deposition rate of the silicon nitride etch stop layer. As Patent Owner correctly observes, for purposes of establishing a reasonable expectation of success, the "relevant aspects of the invention are those that are claimed." PO Resp. 30 (citing *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016)).

Patent Owner argues "[l]ater research identified detrimental effects . . . which likely served as a deterrent that prevented adoption" of Tanaka (1999)'s HCD-SiN material. PO Resp. 31–32 (citing Ex. 2011 ¶ 110; Ex. 2012,[14] 2, 4, Fig. 7; Ex. 2013,[15] 1). Patent Owner's characterization of Tanaka III and Mise as "later" is accurate. As Petitioner correctly notes,

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[14] Masayuki Tanaka et al., *Suppression of SiN-Induced Boron Penetration by Using SiH-Free Silicon Nitride Films Formed by Tetraschlorosilane and Ammonia*, 49 IEEE Transactions in Electron Devices 1526–31 (2002) ("Tanaka III").

[15] N. Mise, et al., *Suppression of Gate-Edge Metamorphoses of Metal/High-k Gate Stack by Low-Temperature, Cl-Free SiN Offset Spacer and its Impact on Scaled MOSFETs*, Extended Abstracts of the 2007 Int'l Conf. on Solid State Devices and Materials, Tsukuba, 724–25 (2007) ("Mise").

Tanaka III is not prior art. Pet. Reply 8. The same is true of Mise. Both references were published after the filing date of the '330 patent, which means they are not relevant to the issue of reasonable expectation of success at the time of the invention. *Bristol-Myers Squibb Co. v. Teva Pharm., Inc.*, 752 F.3d 967, 976 (Fed. Cir. 2014) ("[T]he skilled artisan's reasonable expectation of success is measured 'as of the date of the invention.'" (quoting *Amgen*, 580 F.3d at 1362)). Moreover, neither Patent Owner nor its expert explains how the later research (Exs. 2012, 2013) relates to a reasonable expectation of success for HCD-SiN film as an etch stop layer in copper damascene interconnect structures. We credit Dr. Neikirk's summary of Tanaka III (Ex. 1028 ¶¶ 24–27), which supports his conclusion that a POSA "would understand that the disclosure of Tanaka III has no relevance to the use of SiN in copper damascene interconnect processing" (*id.* ¶ 28).

Patent Owner argues there are inconsistencies between Tanaka (1999) and Tanaka (2000), contending a POSA "would not understand how both of these publications could be correct and would therefore would not want to rely on these data." PO Resp. 33–34 (citing Ex. 2011 ¶ 121). More specifically, Patent Owner asserts a "contrast" exists between Tanaka (1999) Figure 6 and Tanaka (2000) Figure 13 relating to etch rates and etch selectivity. PO Resp. 33. Dr. Bottoms similarly asserts a "discrepancy" exists between Tanaka (1999) and Tanaka (2000) relating to etch rates. Ex. 2011 ¶ 121. Patent Owner's argument and Dr. Bottoms' testimony are persuasively rebutted by Dr. Neikirk, who testifies that Tanaka (1999) Figure 6 is consistent with Tanaka (2000), both of which disclose an etch rate selectivity of six for HCD-SiN versus TEOS-SiO. Ex. 1028 ¶ 18 (citing

Ex. 1017, 48, Fig. 6; Ex. 1018, 2287). Dr. Neikirk's testimony is supported by the references. Ex. 1017, 48, Fig. 6 (plot of "selectivity of RIE etching rate (TEOS/SiN)" versus "deposition temperature (°C)" with a point plotted at a selectivity of six for a deposition temperature of 450°C); Ex. 1018, 2287-2 ("The RIE rate slightly increased for [HCD-SiN] films deposited at 450°C with almost a same selectivity [against TEOS-SiO_2] of six," discussing Figure 13.).

Dr. Bottoms also asserts that a "contrast" exists between Tanaka (1999) Figure 5 and Tanaka (2000) Figure 8. Ex. 2011 ¶ 121; *see also* PO Resp. 34 (relying on Dr. Bottoms' testimony to argue unpredictability). Like the asserted discrepancy between Tanaka (1999) Figure 6 and Tanaka (2000) Figure 13, this alleged discrepancy is not supported by the references. Dr. Bottoms asserts that Tanaka (1999) Figure 5 and Tanaka (2000) Figure 8 show opposite trends, when permittivity is plotted against deposition temperature. Ex. 2011 ¶ 121. These figures do not, however, show the same temperature range. Whereas Tanaka (1999) Figure 5 shows that permittivity decreases with increasing deposition temperature in the range from 250°C to 450°C, Tanaka (2000) Figure 8 shows that permittivity increases with increasing deposition temperature in the range from 450°C to 700°C. Ex. 1017, 48, Fig. 5; Ex. 1018, 2286-2, Fig. 8. As Dr. Neikirk testifies, both diagrams show a permittivity below 5.5 corresponding to a deposition temperature of 450°C. Ex. 2015, 51:11–14 (discussing Tanaka (1999) Figure 5); *id.* at 58:8–14 (discussing Tanaka (2000) Figure 8).

Patent Owner asserts that Tanaka (2000) "discloses that the etch rate of HCD-SiN in HF and the chemical mechanical polish rate are substantially higher at the temperatures used to form the low-k HCD-SiN layer." PO

Resp. 34 (citing Ex. 2011 ¶ 121). Patent Owner's argument is not supported by the cited paragraph of Dr. Bottoms' testimony, which does not discuss HF (hydrofluoric acid) etch rate or chemical mechanical polish rate. Furthermore, Patent Owner does not explain how its assertion about HF etch rate and chemical mechanical polish rate weighs against a finding of a reasonable expectation of success for Petitioner's combination of Igarashi and Tanaka (1999).

Relying on disclosures in Tanaka (1999) and Tanaka (2000) regarding the copper and chlorine content of the HCD-SiN film, Patent Owner argues that a POSA would have had "reason to doubt" the film's barrier ability and its long-term stability in view of supposed problems with copper diffusion and corrosion. PO Resp. 16, 18, 22–23, 34–36 (citing Ex. 2011 ¶¶ 81, 110, 114, 122; Ex. 1017, 47-2, 48, Figs. 4 and 7; Ex. 1018, 2288, Fig. 15). We agree with Petitioner that Patent Owner's argument is not supported by Tanaka (1999) or Tanaka (2000), neither of which describes any problem with copper diffusion or corrosion. Pet. Reply 6. We find that Patent Owner's argument is contradicted by Tanaka (1999)'s express disclosure that HCD-SiN has "higher barrier ability for Cu diffusion than plasma-SiN" and its reliance on a bias-temperature stress test to show an improvement in the film's ability to prevent copper diffusion. Ex. 1017, 47-1, 47-2, 48 (Fig. 8). We find that Patent Owner's argument is further contradicted by Tanaka (1999)'s discussion of thermal stability tests, which Tanaka (1999) states showed that chlorine "was not detected over the detection limit up to 1000 °C, and is concluded to be thermally stable." *Id.* at 47-2. Moreover, Patent Owner's argument is inconsistent with the legal standard for a reasonable expectation of success, which does not require certainty of

success. *In re Kubin*, 561 F.3d 1351, 1360 (Fed. Cir. 2009) ("Obviousness does not require absolute predictability of success . . . all that is required is a reasonable expectation of success." (citing *In re O'Farrell*, 853 F.2d 894, 903–04 (Fed. Cir. 1988))); *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) ("certainty of success" is not required).

Similarly, Patent Owner argues that changes in parameters, such as deposition rate, deposition pressure, deposition temperature, and layer thickness, would "likely affect" or "might affect" the dielectric constant of Tanaka's HCD-SiN material. PO Resp. 15, 37 (citing Ex. 1017, 48, Fig. 2; Ex. 2011 ¶¶ 80, 117, 118, 120; Ex. 2015, 49:6–50:10, 55:23–56:3). Again, Patent Owner's arguments are inconsistent with the legal standard for a reasonable expectation of success, which does not require manufacturability at practical deposition rates, nor absolute certainty of success. *Kubin*, 561 F.3d at 1360; *Medichem*, 437 F.3d at 1165; *Trojan*, 1989 WL 12862213 at *2. Furthermore, Patent Owner's argument is credibly rebutted by the testimony of Dr. Neikirk that slower deposition rates can have their own benefits. Ex. 1028 ¶ 22 (citing and quoting Ex. 1018, 2289).

After considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that a POSA would have had a reasonable expectation of success of achieving the claimed subject matter by combining Tanaka (1999)'s low dielectric constant silicon nitride etch stop film with Igarashi's interconnect structure.

Accordingly, we are persuaded Petitioner has established by a preponderance of the evidence that claims 1 and 6 of the '330 patent are unpatentable as obvious in view of Igarashi and Tanaka (1999).

2. *Claims 4 and 9*

Claim 4 depends from claim 1 and recites "wherein the first and second dielectric layers are of a material having a dielectric constant under 3.9." Ex. 1001, 7:8–10. Claim 9 depends from claim 6 and recites "wherein the first, via, and second dielectric layers are of a material having a dielectric constant under 3.9." *Id.* at 8:17–19.

Petitioner directs us to substantial evidence that Igarashi teaches the limitations of claims 4 and 9 by disclosing an interconnect structure that uses an "SiOF intermetal dielectic film with a dielectric constant of 3.5 to reduce parasitic capacitance." Pet. 62–63 (emphasis omitted) (quoting Ex. 1021, 829). Patent Owner does not contest that evidence and submits no arguments regarding claims 4 and 9 separately from its arguments regarding claims 1 and 6. *See* PO Resp. 65–66. We determine Petitioner has demonstrated by a preponderance of the evidence that the limitations of claims 4 and 9 are taught by Igarashi.

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 4 and 9 of the '330 patent are unpatentable as obvious in view of Igarashi and Tanaka (1999).

3. Claims 5 and 10

Claim 5 depends from claim 1 and recites "wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof." Ex. 1001, 7:11–14. Claim 10 depends from claim 6 and recites "wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof." *Id.* at 8:20–23.

Petitioner directs us to substantial evidence that Igarashi and Tanaka (1999) both teach the limitations of claims 5 and 10 by disclosing copper interconnects and plugs. Pet. 63–64 (quoting Ex. 1021, 829; Ex. 1017, 47-1). Patent Owner does not contest that evidence and submits no arguments regarding claims 5 and 10 separately from its arguments regarding claims 1 and 6. *See* PO Resp. 65–66. We determine Petitioner has demonstrated by a preponderance of the evidence that the limitations of claims 5 and 10 are taught by Igarashi and Tanaka (1999).

Accordingly, after considering the parties' arguments and evidence and the record as a whole, we are persuaded Petitioner has established by a preponderance of the evidence that claims 5 and 10 of the '330 patent are unpatentable as obvious in view of Igarashi and Tanaka (1999).

F. Petitioner's Remaining Challenges to Claims 1, 4–6, 9, and 10

In view of our determination that Petitioner's challenge to claims 1, 4–6, 9, and 10 succeeds based on the combination of Igarashi and Tanaka (1999), we do not reach Petitioner's remaining challenges to claims 1, 4–6, 9, and 10, which are based on the APA or Chooi as the lead or sole reference.

G. Petitioner's Challenges to Claims 2 and 7

Claim 2 depends from claim 1 and recites "wherein the etch stop layer is a multilayer structure." Ex. 1001, 7:3–4. Claim 7 depends from claim 6 and recites "wherein the via and channel etch stop layers are a multilayer structure." *Id.* at 8:12–13.

The Petition asserts that claims 2 and 7 are unpatentable as obvious in view of the APA, the Low-K References, and either Ishikawa or Hasegawa. Pet. 35–38. Alternatively, the Petition asserts that claims 2 and 7 are unpatentable as obvious in view of Chooi and either Ishikawa or Hasegawa. *Id.* at 51–53. Petitioner's declarant concedes that the APA, the Low-K References (Tanaka (1999), Tanaka (2000), and Chooi do not teach multi-layer etch stops. Ex. 1011 ¶¶ 218, 223, 343, 348; *see also* Pet. 38, 53 (citing sections of Exhibit 1011 containing these paragraphs of testimony). The Petition relies on either Ishikawa or Hasegawa to teach a multilayer structure of the etch stop layer, as recited in claims 2 and 7. Pet. 18–21, 35–38, 51–53.

In the Institution Decision, we agreed with Patent Owner that the Petition does not sufficiently establish a reason or motivation to combine the selected teachings of Ishikawa or Hasegawa with the teachings of the APA and the Low-K References or with Chooi. Dec. 32–33, 42. We provided the following analysis in support of that determination:

> First, Petitioner asserts that a POSA would have reason to consider the teachings of Ishikawa and Hasegawa together with those of the APA and the Low-K References because "[a]ll of these references are directed to the same designs—multi-layer interconnects for integrated circuits." Pet. 35; see also Ex. 1011 ¶ 211 (same). Petitioner, thereby, establishes that these references can be used in an obviousness combination. *Tinnus*

Enterprises, LLC v. Telebrands Corp., 846 F.3d 1190, 1207 (Fed. Cir. 2017) (prior art reference "can be used in an obviousness combination" if it is from the same field of endeavor as the inventor's). Petitioner's assertion is not sufficient, however, to establish a reason to combine the prior art teachings in the way the claimed invention does. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–19 (2007); *see also Securus Techs., Inc. v. Glob. Tel*Link Corp.*, No. 2016-2573, 701 F. App'x 971, 977 (Fed. Cir. July 14, 2017) (unpublished) (characterization of prior art references as falling within the same field, "without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion"); *Microsoft Corp. v. Enfish, LLC*, No. 2015-1734, 662 Fed. App'x 981, 990 (Fed. Cir. Nov. 30, 2016) (unpublished) (statement that the references are "directed to the same art or same techniques" does not articulate a sufficient motivation to combine).

Next, Petitioner argues that the high dielectric constant of conventional silicon nitride and the solution to this problem proposed by the Low-K References "would motivate a person of skill to use . . . 'low-k' silicon nitride materials in the multilayer structures of Hasegawa and Ishikawa." Pet. 35–36; *see also id.* at 36 (a POSA "would be motivated to use the silicon nitride of the Low-K References in Ishikawa's and Hasegawa's designs"); *see also* Ex. 1011 ¶¶ 212, 215 (same). At best, Petitioner's argument supports a motivation to combine the low dielectric constant silicon nitrides taught by the Low K References with the multilayer structures taught by Ishikawa and Hasegawa. Petitioner still does not, however, show a reason or motivation to use a multilayer, low dielectric constant, silicon nitride film as an etch stop layer, as recited in claims 2 and 7.

Lastly, Petitioner argues that a POSA would be motivated to use a multilayer, low dielectric constant, silicon nitride film (as taught by the combination of Ishikawa, Hasegawa, and the Low K References) as an etch stop layer in the APA structure "because Ishikawa teaches that such structures have additional benefits, such as preventing surface oxidation of conductors in lower interconnect layers." Pet. 36; *see also* Ex. 1011 ¶¶ 214, 215 (same). Although Petitioner provides no citation to

Ishikawa, it appears that Petitioner relies on Ishikawa paragraph 9, which is cited in Petitioner's claim chart. Pet. 37 (citing Ex. 1024 ¶ 9).[16]

Contrary to Petitioner's argument, Ishikawa does not teach that preventing surface oxidation of conductors in lower interconnect layers is a benefit provided by a multilayer structure. Instead, Ishikawa teaches that suppressing surface oxidation of tungsten is the purpose of silicon nitride films generally, including prior art films that do not have a multilayer structure. Ex. 1024 ¶ 5 (describing conventional semiconductor device); *id.* ¶ 9 (describing problems to be solved by the invention). Petitioner and its declarant do not explain why a POSA would apply a multilayer silicon nitride film to the interconnect structure of the APA, when a single layer silicon nitride film would have provided the same benefit. *Id.* ¶ 5.

According to Ishikawa, the three-layer silicon nitride film is advantageous over a single layer silicon nitride film because it avoids destroying the titanium/titanium nitride (Ti/TiN) barrier film, thereby preventing diffusion of tungsten into the diffusion region of the semiconductor substrate. *Id.* at (57), ¶¶ 10, 11, 30, 34. However, Petitioner does not rely upon this disclosure as a motivation to combine a multilayer etch stop with the

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[16] Petitioner's claim chart includes what purports to be a block quote from Ishikawa paragraph 9. Pet. 37 ("As described above, in order to suppress surface oxidation of tungsten buried in the first contact hole, it is necessary to form a dense and oxidation-resistant silicon nitride."). This indented text presented in the Petition is not, however, a quote from Ishikawa (Ex. 1024), which nowhere includes the word, "dense." The relevant portion of Ishikawa paragraph 9 states:

> [PROBLEMS TO BE SOLVED BY THE INVENTION] As described above, in order to suppress the surface oxidation of the tungsten embedded in the first contact holes, a fine silicon nitride film (SiN) having oxidation resistance is ordinarily deposited on the front surface thereof, and a TEOS film is ordinarily deposited thereon as an interlaminar insulating film.

Ex. 1024 ¶ 9.

> interconnect structure of the APA and the low dielectric constant silicon nitride of the Low-K References. Furthermore, Petitioner does not explain whether or how Ishikawa's multilayer silicon nitride film would both maintain its barrier layer preservation properties and have a dielectric constant below 5.4, when both of these properties are dependent on the chemical composition of the CVD precursors and/or the deposition temperature and/or pressure. Ex. 1014, 3:21–4:4; Ex. 1017, 47, Fig. 5; Ex. 1018, 2284-1, 2286-1, Fig. 8; Ex. 1024, at (57), ¶¶ 5, 10, 11, 18, 19, 22, 27, 30.

Dec. 33–36. Based on the foregoing analysis, we determined that Petitioner had not demonstrated a reasonable likelihood of prevailing on its contentions that claims 2 and 7 are unpatentable as obvious in view of the APA, the Low-K References, and either Ishikawa or Hasegawa, or in view of Chooi and either Ishikawa or Hasegawa. *Id.* at 36, 42.

Petitioner did not seek rehearing of our decision denying institution as to claims 2 and 7. These claims were brought back into the case only as a result of our post-*SAS* order modifying the Institution Decision to include review of all challenged claims on all grounds presented in the Petition. Paper 8.

In the Response, Patent Owner reiterates the arguments that led to our denial of institution as to claims 2 and 7. PO Resp. 47–50; *see also* Prelim. Resp. 53–56.

Petitioner's Reply does not address the deficiencies identified in the Institution Decision (Dec. 33–36), nor respond to most of Patent Owner's arguments regarding Ishikawa, Hasegawa, motivation to combine, and reasonable expectation of success (PO Resp. 39–52, 62–63). Instead, Petitioner switches gears, presenting a new argument regarding motivation to combine that was not presented in the Petition. Specifically, Petitioner

argues that multilayer deposition protects against pinholes, which were known defects in an etch-stop layer. Pet. Reply 12–13, 23 (citing Ex. 1011 at ¶¶ 96, 97; Ex. 1028 ¶¶ 39–41, 44–46; Ex. 2015, 61:1–62:13, 62:23–65:20, 67:6–21). Petitioner relies on new evidence not cited in the Petition to support its contention that multilayer etch stops were known in the art. *Id.* at 13 (citing Exs. 1031[17] and 1032[18]).

Although the Petition asserts that multilayer silicon nitride etch stops are "a conventional practice in semiconductor manufacture" (Pet. 18), it does not point to any evidentiary support other than Ishikawa and Hasegawa. Dr. Neikirk discusses this conventional practice in paragraphs 96 and 97 of his testimony, explaining that, in the 1980s, he taught and was taught to deposit materials as multi-layer structures to prevent pinhole defects. Ex. 1011 at ¶¶ 96, 97. That testimony was not, however, cited or discussed in the Petition. Petitioner concedes that paragraphs 96 and 97 of Dr. Neikirk's testimony were not cited in the Petition. Tr. 18:6–8. Petitioner also agrees that the Petition does not rely on pinhole defects as a reason for using a multilayer structure for the silicon nitride etch stops. *Id.* at 18:9–11.

Under the rules governing this proceeding, "[a] reply may only respond to arguments raised in the corresponding . . . patent owner response." 37 C.F.R. § 42.23(b). The August 2018 Trial Practice Guide Update states: "Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case

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[17] Declaration of Richard Fair, Ph.D., *Micron Tech, Inc. v. Lone Star Silicon Innovations LLC*, Case IPR2017-01566 (Ex. 1003).

[18] *Continuous Process CVD System*, Solid State Tech., Oct. 1987.

of unpatentability." TPG Update, 14. According to the Trial Practice Guide Update, "[e]xamples of new issues are new theories or arguments necessary to make out petitioner's case-in-chief for the unpatentability of an original or proposed substitute claim, such as a newly raised rationale to combine the prior art references that was not expressed in the petition." *Id.* at 15. The Trial Practice Guide Update explains: "It is also improper to present in reply new evidence (including new expert testimony) that could have been presented in a prior filing, for example newly cited prior art references intended to 'gap-fill' by teaching a claim element that was not present in the prior art presented with the petition." *Id.*

In our view, Petitioner's Reply exceeds the scope permitted under 37 C.F.R. § 42.23(b) and the August 2018 Trial Practice Guide to the extent it relies on evidence other than Hasegawa and Ishikawa to establish that multilayer silicon nitride etch stops were a conventional practice in the semiconductor industry. Paragraphs 96 and 97 of Dr. Neikirk's testimony (Ex. 1011 ¶¶ 96, 97) and Exhibits 1031 and 1032, for example, are cited for the first time in the Reply, even though they were available to Petitioner more than three months before the Petition was filed. *See Micron Techs. Inc. v. Lone Star Silicon Innovations LLC*, Case IPR2017-01566 (Petitioner's Exhibits 1003 and 1008 filed June 9, 2017). Petitioner's Reply also exceeds its proper scope to the extent it relies on pinhole defects as a reason or motivation for using a multilayer structure for the silicon nitride etch stop layer. Although Patent Owner requested and received the opportunity to file a sur-reply (Ex. 2016), Patent Owner maintained its objection to Petitioner's Reply as exceeding the proper scope of a reply brief. PO Sur-Reply 1–3. Under our rules, the filing of a sur-reply does not

cure or excuse a reply brief that exceeds the scope permitted under 37 C.F.R. § 42.23(b) and the August 2018 Trial Practice Guide.

When Petitioner's improper reply arguments and evidence are disregarded, as required by our rules, we are left with two reply arguments, neither of which persuades us that Petitioner has met its burden of proof.

First, Petitioner relies on Ishikawa and Hasegawa to argue that fabrication of etch stops as a multilayer structure was a well-known, standard technique (Pet. Reply 13–14, 23), but fails to address Patent Owner's counterarguments. Patent Owner presents a credible, evidence-supported argument that Hasegawa would have been understood as disclosing multiple layers of different materials, not multiple layers of silicon nitride. PO Resp. 44–47 (citing Ex. 2008 ¶¶ 16, 31–33; Ex. 2011 ¶¶ 137, 139). Petitioner does not address Patent Owner's argument. Accordingly, based on Patent Owner's unrebutted argument and evidence (*id.*), we find that Hasegawa does not disclose an etch stop layer of silicon nitride having a multilayer structure, as recited in claims 2 and 7 of the '330 patent.

Patent Owner also presents a credible, evidence-supported argument that the benefits provided by Ishikawa's multilayer silicon nitride film are derived from the specific processes, including temperatures and pressures, used to form the layers. PO Resp. 41, 48 (citing Ex. 1024 ¶¶ 5, 19, 22, 30; Ex. 2011 ¶ 143); PO Sur-Reply 5–6. Petitioner does not address Patent Owner's argument. Accordingly, based on Patent Owner's unrebutted argument and evidence (*id.*), we find Petitioner has not shown that Ishikawa's specific multilayer deposition process was a conventional or standard technique for forming an etch stop layer. Our finding is further

supported by Ishikawa's disclosure of a conventional embodiment that does not have a multilayer silicon nitride etch stop. Ex. 1024 ¶¶ 4, 5, 20, 27, Fig. 12; *compare id.* Fig. 6 (embodiment with silicon nitride film 107 having a three-layer structure), *with id.* Fig. 7 (conventional embodiment with silicon nitride film 7 having a single layer structure). Although Petitioner argues "[w]e don't have any evidence that it wasn't" a conventional practice to make multiple layer etch stops (Tr. 18:11–15), that argument improperly attempts to shift the burden of proof to Patent Owner.

Second, Petitioner argues that Ishikawa's multilayer etch stop structure is not incompatible with the silicon nitride films disclosed by Tanaka (1999), Tanaka (2000), and Chooi. Pet. Reply 13–14 (citing PO Resp. 48). Petitioner does not, however, address the specific incompatibilities identified by Patent Owner and its declarant, which we find to be sufficiently credible and substantiated as to warrant a substantive response by Petitioner. PO Resp. 48–49; Ex. 2011 ¶¶ 143–45.

Accordingly, for all of the foregoing reasons, we are not persuaded that Petitioner has met its burden of proof to establish that claims 2 and 7 of the '330 patent are unpatentable based on either: (1) the APA and the Low-K References in view of Ishikawa or Hasegawa, or (2) Chooi in view of Ishikawa or Hasegawa.

H. Patent Owner's Motion to Exclude

Patent Owner moves to exclude Exhibits 1031 and 1032 and Dr. Neikirk's redirect testimony (Ex. 2015, 61:7–74:22). PO Mot. 11. Patent Owner argues that Exhibits 1031 and 1032 are untimely evidence relied upon to establish Petitioner's prima facie case of unpatentability (*id.* at 4–5, 6–8) and that Dr. Neikirk's redirect testimony is outside the scope of

Patent Owner's cross-examination (*id.* at 9–11).[19] For the reasons discussed above, we determine that Petitioner's arguments that rely upon Exhibits 1031 and 1032 and Dr. Neikirk's redirect testimony (Ex. 2015, 61:7–74:22) are untimely and exceed the proper scope of a reply brief. For these reasons, we do not rely on Exhibits 1031 and 1032 or Dr. Neikirk's redirect testimony (Ex. 2015, 61:7–74:22) as support for this Decision. Accordingly, we *dismiss as moot* Patent Owner's motion to exclude.

III. CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 1, 4–6, 9, and 10 of the '330 patent are unpatentable. Petitioner has not shown by a preponderance of the evidence that claims 2 and 7 of the '330 patent are unpatentable.

IV. ORDER

Accordingly, in consideration of the foregoing, it is hereby:

ORDERED that, based on a preponderance of the evidence, claims 1, 4–6, 9, and 10 of the '330 patent are unpatentable;

FURTHER ORDERED that, on the record before us, Petitioner has not shown by a preponderance of the evidence that claims 2 and 7 of the '330 patent are unpatentable;

FURTHER ORDERED that Patent Owner's motion to exclude (Paper 24) is *dismissed as moot*;

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[19] We note that, under our rules, a motion to exclude should not be used to address arguments or evidence that a party believes exceeds the proper scope of a reply. TPG Update, 16.

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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