UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIERRA WIRELESS, INC. AND SIERRA WIRELESS AMERICA, INC.,
Petitioner

v.

KONINKLIJKE KPN N.V.,
Patent Owner

Case No. IPR2018-00320
Patent No. 6,212,662 B1

PETITIONER'S NOTICE OF APPEAL

Pursuant to 37 C.F.R. §§ 90.2(a), 90.3(a) and 35 U.S.C. §§ 141(c), 142, and 319, Petitioner Sierra Wireless, Inc. and Sierra Wireless America, Inc., ("Sierra") hereby appeals to the United States Court of Appeals for the Federal Circuit the Board's April 30, 2019 Final Written Decision (Paper 42) and all other orders, decisions, rulings, and opinions that are adverse to Sierra. This notice is timely filed within 63 days of the Board's final written decision. 37 C.F.R. § 90.3(a)(1).

For the limited purpose of 37 C.F.R. § 90.2(a)(3)(ii) ("sufficient information to allow the Director to determine whether to exercise the right to intervene in the appeal"), issues Sierra may raise on appeal include the Board's determination that claims 2-4 of U.S. Patent No. 6,212,662 were not shown to be unpatentable, the Board's claim construction of "wherein the varying device is further configured to modify the permutation in time," the Board's application of that construction, and the Board's analysis and conclusions regarding motivation to combine.

Per 37 C.F.R. § 90.2(a)(1), Fed. R. App. P. 15, and Fed. Cir. Rules 15 and 52, simultaneous with this submission, Petitioner is serving a true and correct copy of this Notice of Appeal on the Director of the U.S. Patent and Trademark Office and electronically filing the same, along with the required docketing fees, with the Clerk of the Federal Circuit as set forth in the accompanying Certificate of Service.

Date: June 28, 2019

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **PETITIONER'S NOTICE OF APPEAL** is being served on June 28, 2019, by filing this document through the PTAB End to End filing system as well as via email directed to counsel of record for the Petitioner at the following:

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The undersigned further hereby certifies that this document is being served upon the Director of the U.S. Patent and Trademark Office via Hand Delivery and Federal Express on June 28, 2019 at:

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The undersigned also hereby certifies that a true and correct copy of this document is being filed via CM/ECF with the Clerk's Office of the U.S. Court of Appeals for the Federal Circuit on June 28, 2019 and that the filing fee is being filed via the electronic filing system.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SIERRA WIRELESS, INC. and SIERRA WIRELESS AMERICA, INC.,
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KONINKLIJKE KPN N.V.,
Patent Owner.

Case IPR2018-00320
U.S. Patent 6,212,662 B1

Before CHRISTOPHER M. KAISER, NORMAN H. BEAMER, and JACQUELINE T. HARLOW, *Administrative Patent Judges*.

BEAMER, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

On December 15, 2017, Sierra Wireless, Inc. and Sierra Wireless America, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of claims 1–4 of U.S. Patent No. 6,212,662 B1 ("the '662 patent"). On March 19, 2018, Koninklijke KPN N.V. ("Patent Owner") filed a Preliminary Response (Paper 10). On June 11, 2018, applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we instituted an *inter partes* review of claims 1–4. Paper 15 ("Institution Dec."). In the Institution Decision, we determined Petitioner demonstrated a reasonable likelihood that it would prevail as to claim 1, but not claims 2–4, and we instituted trial on all four claims. Institution Dec. 28.

Following institution, Patent Owner disclaimed claim 1. Paper 19; Ex. 2004. Also, Patent Owner filed a Response to the Petition (Paper 29, "PO Resp.") and Petitioner filed a Reply (Paper 33 "Pet. Reply"). An Oral Hearing took place on March 11, 2019. The Hearing Transcript ("Tr.") is included in the record as Paper 41. Having considered the evidence of record, and for the reasons set forth below, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 2–4 of the '662 patent are unpatentable.

II. BACKGROUND

A. The '662 Patent

The '662 patent, titled "Method And Devices For The Transmission Of Data With Transmission Error Checking," was filed July 26, 1999, and issued April 3, 2001. Ex. 1003. The '662 patent is a division of U.S. Patent

Application No. 08/670,574, filed on June 26, 1996, and therefore the ’662 patent has expired. *Id.* at [62]; *see also* Pet. 6. In addition, the ’662 patent claims priority to a Dutch Patent Application No. NL 1000669, filed on June 26, 1995. *Id*. at Certificate of Correction.

The ’662 patent describes transmission error detection, in data streams or data packets, using an error detection function that varies in time based on the transmitted data itself. *Id.* at [57]. For example, the error detection function can vary as a function of an index of each data packet, a time indication, or a channel number. *Id.* at 3:18–20. The error detection method of the ’662 patent “involv[es] the generation of supplementary data at the transmitting and the receiving end [of a transmission channel] by a first and a second function respectively, and the comparison of the supplementary data generated by said functions in order to detect transmission errors.” *Id.* at 1:12–18.

An exemplary device for error checking in accord with the ’662 claims is depicted in Figure 3 of the ’662 patent, reproduced below.

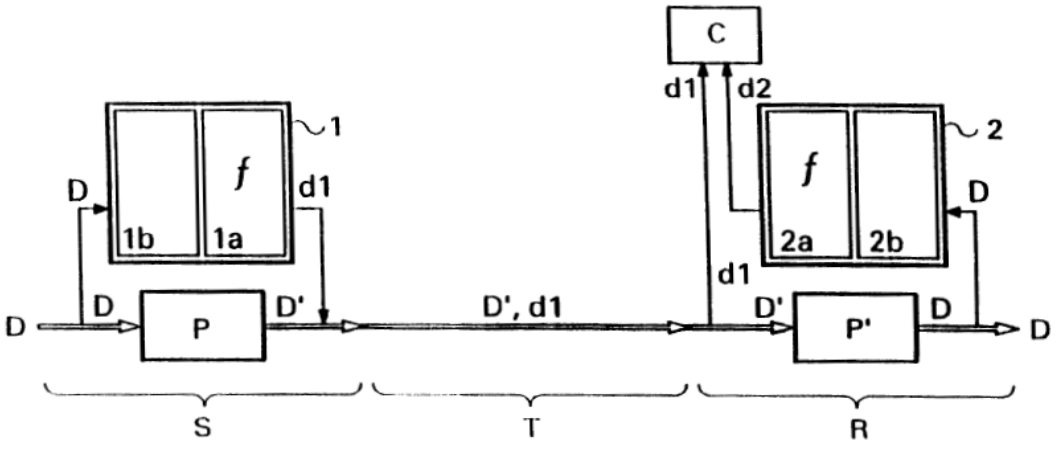

FIG. 3

Figure 3 is a diagrammatic representation of the transmission of original data D, and supplementary data d1, from transmitting end S to receiving end R over transmission path T. *Id.* at 3:29–37, 5:54–57. At transmitting end S, original data D are encoded by process P, and, separately, by function 1. *Id.* at 4:24–29, 5:55–60. Function 1 can "consist of a fixed part **1**a and a variable part **1**b." *Id.* at 5:55–57. Fixed part 1a "generates supplementary data d1." *Id.* at 3:59–62, 5:57–59. The '662 patent specification provides further explanation for variable part 1b:

> [T]he variable part 1b, which brings about a variation in the data, comprises a permutation of the data D. In this connection, bit positions within a data block are interchanged, for example as follows: bit 1 to position 2, bit 2 to position 4, bit 3 to position 1 and bit 4 to position 3. A bit string represented by ABCD thus has the sequence CADB after one permutation, the sequence DCBA after two permutations, and so on.

Id. at 5:58–65. Downstream, comparator C, at receiving end R, compares supplementary data d1 to supplementary data d2 to check for errors in the transmitted data (where d2 is generated by fixed function part 2a, subsequent to permutation of reconstructed data D by variable function part 2b, where D is generated by the processing of received data D' by process P'). *Id.* at 6:14–35, 4:7–8.

In a disclosed embodiment, the permutations performed in the above-labeled "variable part 1b" and "variable part 2b" are continuously changed, in a synchronized and coordinated fashion, for every block of data, where each block of data consists of the same number of bits, and where the particular permutation for a particular block is generated as a function of an index associated with the block, such as "the channel number, a sequence number, a time indication, and so on." *Id.* at 4:61–66, 5:65–6:9.

The continuous alteration of the variable part 1b permutations for each block purports to address a problem arising from "systematic errors [that] are sometimes not detected." *Id.* at 1:47–48. In particular,

> Systematic errors, that is to say, errors which repeat themselves, can arise inter alla [sic] through an error which repeats itself in the transmission channel (for example an interference signal with a certain frequency) or through an equipment error. For (binary) data it holds that there is always a probability that erroneous data are considered to be correct data because the supplementary data may be correct by coincidence (the supplementary data are always restricted in length and therefore a finite number of supplementary data can be distinguished). With systematic errors the case may therefore arise that an error once not recognized as such, is continually not detected.

Id. at 1:48–59. The solution to this problem offered by the '662 patent is the use of the above-described constantly varying permutations in variable parts 1b and 2b:

> In this way it is achieved that the detection probability of systematic errors in particular increases considerably, since (erroneous) data are always varied in time, and are thus effectively checked by a different function each time. The probability that an error, once not recognized as such, is continually not detected, has hereby become minimal.
>
> The invention is therefore based on the insight that an error which repeats itself, once not detected by a normal (fixed) checking function, will repeatedly go undetected. The invention is also based on the insight that a variable checking function can almost always prevent the non-detection of repetitive errors. . . .
>
> . . . .
>
> The embodiments of the invention shown above provide a reliable check on the transmitted data. Error patterns which, in combination with data, result in erroneous data which are not

> recognized as such by conventional means, can also be detected by the method according to the invention.

Id. at 2:42–53, 6:30–36.

B. The Claims

Independent claim 1, now disclaimed, is reproduced below.

> 1. A device for producing error checking [data] based on original data provided in blocks with each block having plural bits in a particular ordered sequence, comprising:[1]
>
> a generating device configured to generate check data; and
>
> a varying device configured to vary original data prior to supplying said original data to the generating device as varied data;
>
> wherein said varying device includes a permutating device configured to perform a permutation of bit position relative to said particular ordered sequence for at least some of the bits in each of said blocks making up said original data without reordering any blocks of original data.

Ex. 1003, 7:4–8:3. The above described data d1 is an example of "check data"; the "fixed part 1a" exemplifies the "generating device"; and the "variable part 1b" exemplifies the "varying device," including the "permutating device."

Challenged claims 2–4 depend from claim 1 and are reproduced below:

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[1] Although not corrected in the Certificate of Correction, the record shows that the word "data" appeared after "checking" in the preamble of the original application claim corresponding to issued claim 1, but was omitted later in prosecution, and not included in the issued claim, although never deleted by amendment. *See* Ex. 1004, 31, 63, 79. Although not dispositive to our Decision, we note that "producing error checking data" appears to be more appropriate in this context than "producing error checking."

> 2. The device according to claim 1, wherein the varying device is further configured to modify the permutation in time.
>
> 3. The device according to claim 2, wherein the varying is further configured to modify the permutation based on the original data.
>
> 4. The device according to claim 3, wherein the permutating device includes a table in which subsequent permutations are stored.

Id. at 8:4–12. These dependent claims are exemplified by the disclosed operation of Figure 3 described above, in which the permutations are continuously changed for every block of data, where the particular permutation for a particular block is read out from a table using an index associated with the block. *Id.* at 5:65–6:2.

C. Prior Art Relied Upon

Petitioner relies upon the following prior art references (Pet. 5):

- Divsalar et al., *Turbo Codes for PCS Applications* ("Divsalar"), published as part of the 1995 IEEE International Conference on Communications held June 18–22, 1995. Ex. 1005.
- U.S. Patent No. 5,596,604 ("Cioffi"), filed August 17, 1993, issued January 21, 1997. Ex. 1007.
- Barbulescu et al., *Rate-Compatible Turbocodes* ("Barbulescu"), Electronic Letters Vol. 31, No. 7, published March 30, 1995. Ex. 1008.
- U.S. Patent No. 5,392,299 ("Rhines"), filed January 15, 1992, issued February 21, 1995. Ex. 1010.

In addition, both parties also rely on declaration testimony. Petitioner provides an expert declaration of Dr. Stephen Wicker. Ex. 1001 (hereafter "Wicker Decl."). Patent Owner relies on the expert declaration of

Dr. Radostin Pachamanov. Ex. 2005 (hereafter "Pachamanov Decl."). The record also includes deposition transcripts for these witnesses.[2]

D. Asserted Grounds of Unpatentability

Petitioner's remaining challenges are directed to claims 2–4 on the following grounds of unpatentability (Pet. 6):

Claim(s)	Reference(s)	Basis
2–4	Divsalar and Cioffi	§ 103(a)
4	Divsalar, Cioffi, and Rhines	§ 103(a)
2–4	Barbulescu and Cioffi	§ 103(a)
4	Barbulescu, Cioffi, and Rhines	§ 103(a)

E. Real Parties in Interest

Petitioner identifies Sierra Wireless, Inc. and Sierra Wireless America, Inc. as real parties in interest in this proceeding. Paper 40, 2. Patent Owner identifies itself as a real party in interest. Paper 14, 2.

F. Related Proceedings

The parties identify the following pending judicial matters as involving the '662 patent:

- *3G Licensing, SA et al. v. BlackBerry Ltd. et al.*, Civil Action No. 1-17-cv-00082 (D. Del.);
- *3G Licensing, SA et al. v. HTC Corp. et al.*, Civil Action No. 1-17-cv-00083 (D. Del.);
- *3G Licensing, SA et al. v. Lenovo Group Ltd. et al.*, Civil Action No. 1-17-cv-00084 (D. Del.);

[2] Ex. 2009 ("Wicker Dep."); Ex. 1029 ("Pachamanov Dep.").

- *3G Licensing, SA et al. v. LG Elecs., Inc. et al.*, Civil Action No. 1-17-cv-00085 (D. Del.);
- *Koninklijke KPN NV v. Gemalto NV et al.*, Civil Action No. 1-17-cv-00086 (D. Del.) (on appeal to the Federal Circuit, Case No. 18-1863, docketed on April 23, 2018);
- *Koninklijke KPN NV v. OnePlus Techn. (Shenzen) Co., Ltd.*, Civil Action No. 1-17-cv-00089 (D. Del.);
- *Koninklijke KPN NV v. Sierra Wireless, Inc. et al.*, Civil Action No. 1-17-cv-00090 (D. Del.);
- *Koninklijke KPN NV v. TCL Corp. et al.*, Civil Action No. 1-17-cv-00091 (D. Del.) (on appeal to the Federal Circuit, Case No. 18-1864, docketed on April 23, 2018, consolidated with Case No. 18-1863); and
- *Koninklijke KPN NV v. Telit Wireless Solutions Inc. et al.*, Civil Action No. 1-17-cv-00092 (D. Del.) (on appeal to the Federal Circuit, Case No. 18-1865, docketed on April 23, 2018, consolidated with Case No. 18-1863).

Paper 40, 2–3; Paper 14, 3–4.

In addition, the ’662 patent was at issue in the following previous judicial matters:

- *Koninklijke KPN N.V. v. Kyocera Corp. et al.*, Civil Action No. 1-17-cv-00087 (D. Del.) (settled and dismissed);
- *Koninklijke KPN NV v. NEC Corp. et al.*, Civil Action No. 1-17-cv-00088 (D. Del.) (settled and dismissed);
- *Koninklijke KPN N.V. v. Samsung Electronics America, Inc.*, Case No. 2:14-cv-01165-JRG, in the U.S. District Court for the Eastern District of Texas (the “1165 Action”) (Claim Construction Order issued, then settled and dismissed). Ex. 2008.
- *Koninklijke KPN N.V. v. Samsung Electronics America, Inc.*, Case No. 2:15- cv-00948-JRG in the U.S. District Court for the

Eastern District of Texas (later consolidated with the 1165 Action, settled and dismissed).

Paper 40, 2; Paper 14, 4.

Also, *inter partes* review of the '662 patent was sought in the following:

- *Samsung Electronics Co., Ltd. v. Koninklijke KPN N.V.*, IPR2016-00392 (terminated pursuant to settlement before final written decision issued). Exs. 1011, 1012, 1013.
- *NEC Corporation v. Koninklijke KPN N.V.* (terminated pursuant to settlement prior to institution). *Id.*; IPR2017-02089, Paper 12.
- *LG Electronics, Inc. et al. v. Koninklijke KPN N.V.*, IPR2018-00554; *LG Electronics, Inc. et al. v. Koninklijke KPN N.V.*, IPR2018-00553; and *LG Electronics, Inc. et al. v. Koninklijke KPN N.V.*, IPR2018-00551 (institution denied).
- *TCL Communication, Inc. et al. v. Koninklijke KPN N.V.*, IPR2018-00757 ("TCL IPR") (institution denied).

Paper 40, 3; Paper 14, 4.

We note on March 22, 2018, all claims of the '662 Patent were invalidated pursuant to 35 U.S.C. § 101 by the Court in the aforementioned cases in the District of Delaware, which Judgment is on appeal. Paper 40, 3.

III. ANALYSIS

A. Claim Construction

In an *inter partes* review of an expired patent, our claim interpretation is similar to that of a district court. *See In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution

history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc)). In particular, claim interpretation "is an interpretation that corresponds with what and how the inventor describes his invention in the specification." *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382–83 (Fed. Cir. 2017). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Otherwise, terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Claim terms need only be construed to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).

Prior to institution, Petitioner submitted that no claim construction was necessary. Pet. 7. Patent Owner did not raise any claim construction issues. In the Institution Decision, we construed the claim 2 requirement "wherein the varying device is further configured to modify the permutation in time" to require "varying the permutation from each block to the next." Institution Dec. 11. Both parties disagree with this construction as unduly narrow. PO Resp. 3–4; Pet. Reply 2–5. For example, the construction excludes varying the permutation for every other block, which would arguably also be effective in detecting systematic errors. *See* Pachamanov Dep. 24. On further consideration of the record, we withdraw our previous

claim construction and apply the ordinary meaning of the phrase.[3] As discussed *infra*, while the ordinary meaning of "modify the permutation in time" does not require varying the permutation from each block to the next, it also does not encompass occasional and time-independent switching from one transmission speed to another, or from video to audio transmissions. In reaching this conclusion, as discussed further *infra*, we are informed by the same considerations that led to our construction articulated in the Institution Decision.

B. Obviousness – In General

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results ("the *Graham* factors").[4] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

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[3] In the 1165 Action, the Court construed "modify the permutation in time" to mean "change the permutation from time to time." Ex. 2008, 35. Our Decision would reach the same result under this construction.

[4] Neither party presented evidence on the fourth *Graham* factor. We therefore do not consider that factor in this decision.

If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *KSR*, 550 U.S. at 418. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

"[A] combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 416. "[I]n many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id.* at 420–421.

"The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . . Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). "Combining the *teachings* of references does not involve an ability to combine their specific structures." *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973).

C. Level of Skill

Petitioner's expert opines that a person of ordinary skill in the art of the '662 Patent as of June 26, 1995 priority date would be as follows:

> [A] person with a bachelor's degree in electrical engineering or a closely related field such as computer engineering, and two to

> three years of experience in the field of network engineering, information networks, or data communications, or a Master's degree in Electrical Engineering or a related field. A person with less education but more relevant practical experience may also meet this standard.

Wicker Decl. ¶ 70. Patent Owner's expert provides a similar formulation. Pachamanov Decl. ¶ 33. We find the above-quoted formulation supported by the record and adopt it.

D. Obviousness Over Divsalar and Cioffi

Petitioner challenges claims 2–4, including the limitations of disclaimed claim 1 by dependency, as obvious over the combination of Divsalar and Cioffi. Pet. 20–42. Divsalar, titled "Turbo Codes for PCS Applications," is alleged to have a United States publication date no later than June 22, 1995.[5] Pet. 5; Exs. 1005, 1006 (Declaration of Gerald P. Grenier).

As a threshold issue, Patent Owner argues Petitioner has failed to demonstrate by a preponderance of the evidence that Divsalar was publicly accessible prior to the critical date of the '662 Patent. PO Resp. 6–9. However, Petitioner has presented evidence that Divsalar was part of the printed Proceedings of the 1995 IEEE International Conference on Communications, held from June 18–22, 1995, which Proceedings were available to attendees at least by the last day of the conference, prior to the June 26, 1995 priority date. Pet. Reply 6–7; Exs. 1005, 1006, 1014, 1024; *see also* Ex. 2010, 17:20–18:12. Petitioner also submitted evidence that the

[5] Petitioner states that PCS stands for "personal communications systems" (Pet. 23).

Conference was attended by a wide representation of practitioners in the pertinent art of data communications. Exs. 1014, 1015, 1020; Pachamanov Dep. 119–120. The preface to the Proceedings includes "Greetings from the ICC '95 General Chairman," which reasonably implies broad, representative attendance by the pertinent audience:

> The ICC '95 program promises to be outstanding. . . . The core of our technical program consists of fifty-four sessions, including more than 350 contributed presentations. Eighteen tutorials and workshops, covering everything from ATM to Wireless PCS, supplement the technical sessions. . . .
>
> . . . .
>
> Our outstanding technical program, and the opportunity to meet with many colleagues from all over the world, are just two of the reasons I hope you join us for ICC '95.

Ex. 1014, iii; *see also* "ICC '95 Technical Program Chairman's Message," *Id.* at iv; Conference Author Index," Ex. 1015.

We therefore find Petitioner has shown by a preponderance of the evidence that Divsalar is a prior art publication. *Bruckelmyer v. Ground Heaters, Inc.*, 445 F.3d 1374, 1378 (Fed. Cir. 2006) (a reference is publicly accessible if it "has been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it"); *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1381 (Fed. Cir. 2018) (distribution at a conference may satisfy the public availability requirement).

Generally, Divsalar discloses the use of turbo codes for error correction, and discusses the effect of interleaver choice and unequal rate codes on performance. Ex. 1005, Abstract. In challenging the claims,

Petitioner relies, *inter alia*, on Figure 1 of Divsalar, reproduced below. Pet. 25.

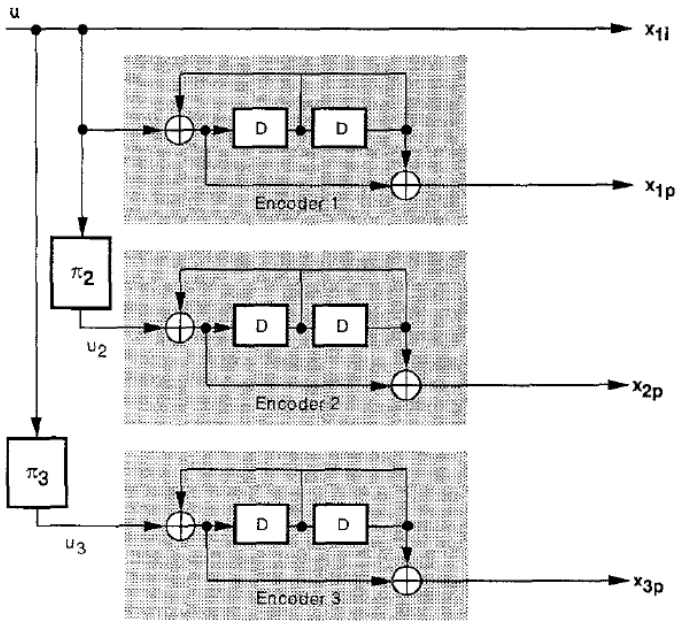


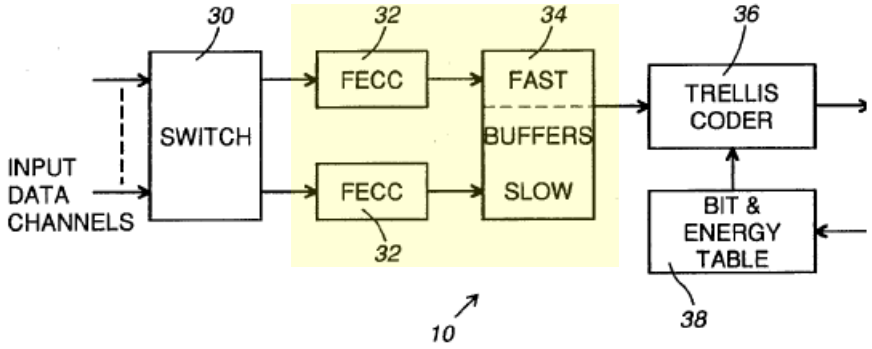
Figure 1 illustrates an example of an encoder with three "recursive binary convolutional encoders" (labelled Encoders 1, 2, and 3), with the input bit sequence u applied directly to Encoder 1, and via interleavers π_2 and π_3 to Encoders 2 and 3, respectively. Ex. 1005, 54.[6] The output bit sequences, consisting of $x_{1i,}$ $x_{1p,}$ $x_{2p,\text{ and }}$ $x_{3p,}$ together form a "rate ¼ code," meaning that there are 3 error correction bits for each data bit — i.e., one data bit per 4-bit output. *Id.*; Wicker Decl. ¶ 85.

Cioffi, titled "Multicarrier Modulation Transmission System With Variable Delay," was filed August 17, 1993, and issued January 21, 1997, and therefore is prior art under 35 U.S.C. § 102(e). Ex. 1007. Generally, Cioffi discloses varying combinations of error correction encoders and

[6] We cite to the original pagination of Divsalar rather than to the page numbers of the exhibit added by Petitioner.

interleavers, which vary depending on the sensitivity to errors of the input information, such as video, data or control information. *Id.* at Abstract.

In challenging the claims, Petitioner relies, *inter alia*, on the highlighted portion of Figure 2, reproduced below:



Pet. 29. Figure 2 is block diagram of a telephone central office transmitter, in which switch 30, controlled by signals in a control channel, selects various input data channels, each of which has different characteristics relating to vulnerabilities to transmission errors (e.g., vulnerable compressed video signals, versus voice signals less sensitive to error), and routes each channel to an associated "FECC" (Forward Error Correction Code) encoder 32, and thence to a corresponding one of the fast/slow buffers 34, which perform different degrees of interleaving. Ex. 1007, Fig. 2, 2:19–21, 2:63–3:2, 3:33–36, 5:29–32, 6:9–46, 8:51–58, 10:18–33. The interleavers spread out the bits in individual codewords, interleaving them with that of other codewords, to reduce the effect of error bursts on individual codewords. *Id.* at 1:59–67. Data on any one channel can change from (for example) video to voice, which would cause the channel path to be switched from one encoder/interleaver combination to another. *Id.* at 6:20–24 ("signals on a single channel [switch to different encoder/interleaver combinations] at different times").

1. Independent Claim 1

Although claim 1 is disclaimed, its limitations are incorporated into the challenged dependent claims, and so must be considered. *See* MPEP § 2260.01 (9th Ed., Rev. 08.2017). Prior to the disclaimer of claim 1, Petitioner argued Divsalar alone rendered each limitation of claim 1 obvious. Pet. 21–22, 24–25, 26–29, 30–31. Petitioner also made obviousness arguments directed to Cioffi alone, and to the combination of Divsalar and Cioffi. *Id*. at 22–24, 26, 29–30, 32–33. However, as discussed in our claim 2 analysis, Cioffi, whether consider alone or in combination with Divsalar, does not teach or suggest the subject matter of the '662 patent, and in any event it is sufficient for our analysis of the limitations of claim 1 to consider Divsalar alone.

To the extent that "producing error checking" in the preamble of claim 1 is a claim requirement, Divsalar does not relate to a "device for producing error checking," but rather to error *correction* devices. Nevertheless, we find that Petitioner has demonstrated by a preponderance of the evidence that the disclosure of error correction teaches or suggests error detection. Pet. 21; Wicker Decl. ¶¶ 122–127, 163. It is well known in the art that error correction algorithms include an error detection stage. Wicker Decl. ¶¶ 124–125; Ex. 1010, Abstract; Ex. 1016, 5; *see also* Ex. 1007, 1:59–63 ("it is known to apply forward error correction coding (FECC) and interleaving techniques in which a block of input data to be transmitted is augmented with parity data that enables one or more errors in the block to be *detected and corrected*" (emphasis added)).

Petitioner also presents evidence that the remaining limitations of claim 1 are taught or suggested by Divsalar — indeed, they are disclosed in

that reference. The additional requirement in the preamble of "data provided in blocks with each block having plural bits in a particular ordered sequence," is disclosed in Divsalar Figure 1 and the accompanying description of the input "bit sequence u = (u_1, . . . , u_N) of length N." Pet. 21–22; Wicker Decl. ¶ 161; Ex. 1005, 54. In addition, the encoders of Figure 1 (Encoder 1, 2, and 3) disclose the "generating device" limitation of claim 1. Pet. 24–26; Wicker Decl. ¶¶ 171–174. As stated in Divsalar, the encoders "generate a (n $(N + M)$, N) block code." Ex. 1005, 55. Finally, the interleavers, π_2 and π_3, disclose both the varying device limitation and the permutation device limitation of claim 1. Pet. 26–31; Wicker Decl. ¶¶ 178–179, 182–183. As stated in Divsalar, "[t]he interleaver is a pseudo-random block scrambler defined by a *permutation* of N elements with no repetitions: a complete block is read into the . . . interleaver and read out in a specified (fixed) random order." Ex. 1005, 54 (emphasis added).

As discussed above, Patent Owner has disclaimed claim 1, and Patent Owner does not address Petitioner's obviousness arguments regarding the specific claim 1 limitations in its Response. However, Patent Owner argues that Petitioner has failed to show with particularity why the '662 patent is unpatentable, and in particular refers to "Petitioner's lack of precision and convoluted arguments for the unpatentability of Claim 1." PO Resp. 5. We are not persuaded by Patent Owner's argument — as discussed above, we focus on Petitioner's evidence that the limitations of claim 1 are taught or suggested by Divsalar alone, which is marshaled with sufficient particularity and supported by the record.

Therefore, based on the record before us, we determine that Petitioner has demonstrated by a preponderance of the evidence that the subject matter

of claim 1 — and hence that subject matter as included in the dependent claims — would have been obvious over Divsalar, and *ipso facto* obvious over Divsalar and Cioffi.

2. Dependent Claim 2

Claim 2 depends from claim 1 and additionally requires "wherein the varying device is further configured to modify the permutation in time." Ex. 1003, col. 8, ll. 4–6. Petitioner asserts "Divsalar and Cioffi, each in view of the knowledge of a POSITA, render claim 2 obvious." Pet. 33. Petitioner also argues "it would have been obvious to combine the teachings of Divsalar with Cioffi." *Id.* at 35; *see also* Pet. Reply 8. We consider each of these alternative arguments.

(a) Divsalar alone

First, Petitioner asserts the interleavers of Divsalar satisfy this limitation because, in certain embodiments in Divsalar that describe "random or pseudo-random interleavers," "the interleaving is changed over time." Pet. 33–34; Pet. Reply 10; Wicker Decl. ¶¶ 186–189. This is a mischaracterization of Divsalar — as Patent Owner demonstrates, Divsalar provides:

> [T]he interleaver is a pseudo-random block scrambler defined by **a permutation** of *N* elements with no repetitions: a complete block is read into the [sic] interleaver and read out in a specified **(fixed)** random order. The **same interleaver is used repeatedly** for all subsequent blocks.

PO Resp. 12; Ex. 1005, 54. The references in Divsalar to pseudorandom or random interleavers "refer[] to the random selection of the single, fixed permutation each interleaver is to apply, not how these interleavers operate in time." PO Resp. 12. Divsalar is directed to discussions of how to design

the optimum interleaver for particular applications, but once the choice is made, there is no teaching or suggestion in Divsalar of having an interleaver in any particular application change over time. PO Resp. 11–17; Pachamanov Decl. ¶¶ 78–82.

In attempting to show otherwise, Petitioner relies on the discussion in Divsalar of "Unequal Rate Encoders," in which a 192-bit interleaver is used for voice transmissions encoded at a rate of 9.6 Kbps and a 256-bit interleaver is used for 13 Kbps. Pet. 34–35; Pet. Reply 8–10; Wicker Decl. ¶ 190. However, as Patent Owner argues, "Divsalar only suggests turbo encoders that accept data at a 9.6 Kbps **or** a 13 Kbps compression rate. Divsalar does not disclose a turbo encoder capable of changing the compression rate of the data the turbo encoder accepts during operation." PO Resp. 17 (citation omitted). The discussion of unequal rate decoders in Divsalar is part of the above-described overall discussion of selecting a single desired interleaver for a particular application (in this case voice transmission at different bit rates), and has nothing to do with the design of devices capable of switching between different speeds. PO Resp. 17–20; Pachamanov Decl. ¶¶ 84–85.

Petitioner nonetheless argues one of ordinary skill in the art "would have known that in a cellular phone transmitter system transmitting data at both 9.6 and 13 Kbps, switching between the encoding rates — and thus between the two interleaving functions — would occur over time." Pet. 34–35; Wicker Decl. ¶ 190. Petitioner's expert further testified, "[t]o the extent the Divsalar does not expressly disclose this element, it would have been obvious to one of ordinary skill in the art to modify the turbo encoder disclosed by Divsalar such that the varying device is configured to modify

the permutation in time by varying the interleaver size." Wicker Decl. ¶ 191. We find no support in the record for this conclusory opinion. As discussed, Divsalar is concerned with selecting optimum interleavers for particular applications, and has no teaching or suggestion of designing devices that switch between interleavers. PO Resp. 19–20; Pachamanov Decl. ¶¶ 82, 85.

Moreover, Patent Owner's expert testified that in 1995 it "wasn't that easy" to have voice transmission devices capable of operating at different speeds, and usually devices were designed to serve a specific purpose. Pachamanov Dep. 57–58. Moreover, even if it were to have occurred to a designer to create a device that could switch between, for example, 9.6 and 13 Kbps transmission speeds, there is nothing in the record to show how, or if, such a device would have modified permutations in time. Although Divsalar separately "selected 192 and 256 bits interleavers as an example," the article notes "that this small difference of interleaver size does not affect significantly the performance." Ex. 1005, 58. Petitioner has not demonstrated that one of ordinary skill would have introduced the complexity of a single device with changeable interleaver sizes for such a small difference in performance. Pachamanov Decl. ¶ 82. In addition, Patent Owner's expert testified that changing interleaver bit-size does not necessarily involve changing permutations, because the different bit numbers may be simply a result of different block sizes, rather than different permutation patterns. Pachamanov Dep. 53–54.

Therefore, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claim 2 would have been obvious over Divsalar alone.

(b) Cioffi alone

Petitioner also relies on Cioffi as teaching or suggesting varying the type of interleaving, and thus varying permutations, over time, because, as discussed above, data on any one channel can change from (for example) compressed video data to voice data, which would cause the channel path to be switched from one encoder/interleaver combination to another. Pet. 35–36; Pet. Reply 11–13; Wicker Decl. ¶¶ 193–194. However, as discussed below, the variation of interleavers in Cioffi is not relevant to the subject matter of claim 2 of the '662 patent.

In the first place, as discussed above, and as Petitioner admits, the interleaver/buffers 34 of Cioffi are placed downstream of the encoders 32, whereas the claims require the varying device (alleged to be the interleavers in this instance) to vary the original data *prior to* supplying the data to the generating device (alleged to be the encoders). Pet. 26, 30; Wicker Decl. ¶¶ 175, 180; *see also* Pachamanov Decl. ¶¶ 89–90.

In addition, Petitioner admits that

> Cioffi's . . . system interleaves the blocks of data by writing them to the buffers in one order and reading them out in another order. "[C]odewords are interleaved for transmission to reduce the effect of bursts on individual codewords." (*Id*. at 1:59–67, 6:39-46, 7:53-62.) In a further example, Cioffi taught that "FECC codewords are stored in the RAM 74 under the control of control unit 68, which also implements convolutional interleaving of at least some of the codewords." (*Id*. at 9:13–16.)

Pet. 29–30 (emphasis omitted); *see also* Wicker Decl. ¶ 180 ("the particular implementation . . . taught by Cioffi generally interleaves the *codewords*" (emphasis supplied)); Pachamanov Decl. ¶¶ 72–73. As stated in Cioffi:

> A well known problem in the art of transmission systems is that of impulse noise, which can produce bursts of errors on transmission channels. In order to address this problem, it is known to apply forward error correction coding (FECC) and interleaving techniques in which a block of input data to be transmitted is augmented with parity data that enables one or more errors in the block to be detected and corrected, the input data and parity data constituting a codeword, and over time parts of *different codewords are interleaved* for transmission to reduce the effect of error bursts on individual codewords. . . .
>
> . . . .
>
> . . . In the interleaving process, the k-th byte in each FECC codeword is delayed by l+(d-l)k bytes, where d is an integer referred to as the depth of interleaving.[7]

Ex. 1007, 1:57–67, 9:23–26 (emphasis added).

Thus, the interleavers of Cioffi do not comply with the claim 1 requirement that the "permutating device [is] configured to perform a permutation of bit position relative to said particular ordered sequence for at least some of the bits *in each of said blocks* making up said original data *without reordering any blocks of original data*." Ex. 1003, 7:12–8:3 (emphasis supplied).

The significance of this difference between Cioffi and the claimed subject matter is revealed by reference to the prosecution history of the '662 patent application that led to the claim limitations that distinguish Cioffi. Ex. 1004. The original counterpart to issued claim 1 was application claim 13, submitted in a July 26, 1999 preliminary amendment:

[7] "Depth" in this context refers to the number of codewords that are interleaved together. Berlekamp 3:16–25 (referring to Berlekamp U.S. Patent 4,916,702, discussed further below, filed as Exhibit 2002 in the related IPR757 proceeding).

> 13. A device for producing error checking data based on *original data*, comprising:
>
> a generating device configured to generate check data; and
>
> a varying device configured to vary *original data* prior to supplying said *original data* to the generating device;
>
> wherein said varying device includes a permutating device configured to perform a permutation of said *original data*.

Id. at 31–32 (emphasis supplied; amendment notations omitted); Wicker Decl. ¶ 139. Thus, the as-filed claims of the '662 patent application had no requirement that the original data be organized in blocks, or that blocks not be reordered.

In a June 1, 2000 amendment, in response to rejection of application claim 13 over Silvano U.S. Patent 5,535,227 ("Silvano"), the claim was amended:

> 13. A device for producing error checking [data][8] based on original data <u>provided in blocks with each block set having plural bits</u>, comprising:
>
> a generating device configured to generate check data; and
>
> a varying device configured to vary original data prior to supplying said original data to the generating device;
>
> wherein said varying device includes a permutating device configured to perform a permutation <u>of bit position for at least some of the bits in said blocks making up</u> said original data.

[8] The square brackets enclosing "data" are not part of the amendment, but rather indicate, as discussed above, that the word "data" was dropped at this point in the prosecution without indication that the omission was intentional.

Ex. 1004, 44, 63–64; Wicker Decl. ¶¶ 140–141. Applicants argued Silvano did not teach or suggest the permutation requirements of the claim, in part supporting this argument by referring to the new requirement that the original data be provided in blocks, *and the permutations be performed on bits within a data block*. Ex. 1004, 65–66; Wicker Decl. ¶ 142. To establish that the amendment did not introduce new matter, applicants argued:

> [T]he present invention is particularly concerned with the Figure 3 embodiment which includes a portion (l a) to provide variable data in which *the variation includes permutation of at least some data bit positions within a data block*. Note, for example, the discussion of Fig. 3 appearing at page 8, lines 13-32 of the original specification.

Ex. 1004, 65 (emphasis added). The portion of the original specification referred to in the last sentence of the above quote provides in pertinent part,

> In Fig. 3, a second exemplary embodiment of the invention is diagrammatically shown. . . . In the example of Fig. 3, the variable part 1b, which brings about a variation in the data, comprises a permutation of the data D. In this connection, *bit positions within a data block are interchanged*, for example as follows: bit 1 to position 2, bit 2 to position 4, bit 3 to position 1 and bit 4 to position 3. A bit string represented by ABCD thus has the sequence CADB after one permutation, the sequence DCBA after two permutations, and so on. . . . *The said permutations can be applied to a data block or to a part of a data block.*

Id. at 15 (emphasis added).[9]

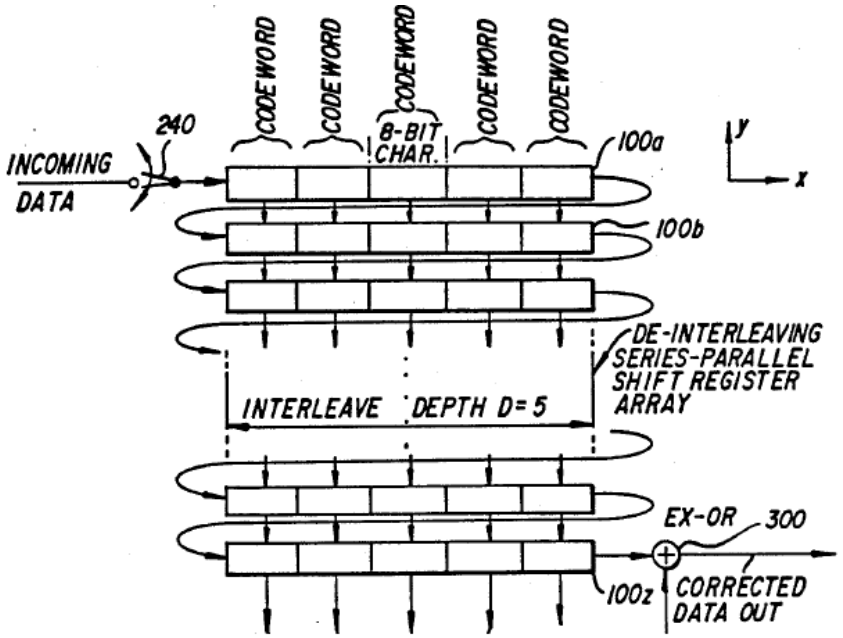
In a November 1, 2000 amendment, the claim was further amended, resulting in the final wording of issued claim 1:

[9] This portion of the original specification corresponds to column 5, line 54 to column 6, line 5 of the issued patent. Ex. 1003.

> 13. A device for producing error checking [data][10] based on original data provided in blocks with each block [set] having plural bits in a particular ordered sequence, comprising:
>
> a generating device configured to generate check data; and
>
> a varying device configured to vary original data prior to supplying said original data to the generating device as varied data;
>
> wherein said varying device includes a permutating device configured to perform a permutation of bit position relative to said particular ordered sequence for at least some of the bits in each of said blocks making up said original data without reordering any blocks of original data.

Ex. 1004, 79–80; Wicker Decl. ¶ 143. This requirement was added during the '662 patent prosecution to overcome the Examiner's rejection of the pending claims in light of Berlekamp U.S. Patent 4,916,702 ("Berlekamp"). Ex. 1004, 81–82; Wicker Decl. ¶ 142. Berlekamp discloses an approach in which a number of data blocks are interleaved with each other prior to transmission, as illustrated in Figure 3, a portion of which is reproduced below:

[10] Again, the square brackets around "data" are not part of the amendment. However, the square brackets around the word "set" indicate intentional deletion by amendment.



This portion of Figure 3 shows an example of block interleaving, in which five code words (i.e., output blocks of original data and check data) are interleaved together before transmission, and then are de-interleaved at the receiving end. Berlekamp, 3:17–25.

To distinguish this approach, applicants argued:

> Turning to the outstanding rejection of Claim 13 [issued claim 1] over Berlekamp, the action mistakenly assumes that the present invention has something to do with an interleaving process like that associated with the Berlekamp interleaving in which code words are interleaved in a serial fashion to be subject to de-interleaving upon receipt to form the five parallel codewords . . . . *However, the permutation being claimed has nothing to do with such serial-parallel interleaving/de-interleaving*. . . .
>
> . . . In order to even more clearly define the present invention, Claim 13 [issued claim 1] has been further amended to emphasize that the plural bits that make up a block of data are in a particular order where the varying device that generates the varied data from the original data must include a permutating device that must perform a permutation . . . *without any blocks of*

> *the original data being reordered. This is in clear contradistinction to Berlekamp which teaches the simple reordering of codeword blocks so as to interleave and de-interleave the codeword rendered . . . .*

Ex. 1004, 81–82 (emphasis supplied).

Significantly, the interleaver approach disclosed in Cioffi is essentially identical to that of Berlekamp. Instead of only permutating the bits within each block, and avoiding reordering (i.e., permutating) the blocks themselves, Cioffi interleaves (reorders) the blocks, leaving the order of bits within the blocks unchanged. This is precisely the opposite of what claim 1, and thus claim 2, requires. *See* Pachamanov Decl. ¶ 73.

Therefore, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claim 2 would have been obvious over Cioffi alone.

(c) The combination of Divsalar and Cioffi

In arguing claim 2, Petitioner further asserts "it would have been obvious to combine the teachings of Divsalar with Cioffi." Pet. 35; *see also* Pet. Reply 8, 13–15. However, as Patent Owner argues, nothing is offered concerning such a combination beyond what the two references separately teach or suggest:

> Petitioner fails to identify which elements of the alleged combinations are being drawn from each of the references, instead alleging only that various elements are present in one or both of the primary and secondary references and leaving it to the Board and the Patent Owner to speculate . . . .

PO Resp. 5 (emphasis omitted); *see also* PO Resp. 23. Indeed, the discussion following Petitioner's one-sentence assertion that it would be obvious to combine the references is limited to the above-discussed

argument based on Cioffi alone. Pet. 35. As discussed above, we find that argument unpersuasive.

Petitioner generally argues one of ordinary skill would have been motivated to combine Divsalar and Cioffi, because both are in the field of error correction in communication systems, and discuss optimizing the use of coding and interleaving techniques. Pet. 22–24, 26, 29–30, 32–33, 35, 38–39. Petitioner relies on Dr. Wicker's opinion that it would have been obvious to combine the teachings of Cioffi and Divsalar. *E.g.*, Wicker Decl. ¶¶ 168–169, 175, 180, 184, 193.

However, Divsalar uses convolutional coding whereas Cioffi uses block encoding, which techniques have significant differences. Pachamanov Decl. ¶¶ 62–71; Tr. 50–51; Ex. 2001, 22–24. In addition, Divsalar locates the interleavers prior to the encoders, whereas Cioffi locates the interleavers after the encoders, and, as discussed above, the interleavers of Cioffi interleave (reorder) the blocks, leaving the order of bits within the blocks unchanged, instead of only permutating the bits within each block, and avoiding reordering (i.e., permutating) the blocks themselves. Pachamanov Decl. ¶¶ 72–73, 75; Tr. 51–52. Therefore, Petitioner's general arguments to the effect that one of ordinary skill would have looked to a combination of Divsalar and Cioffi are without merit.

Specifically addressing the "modify the permutation in time" requirement of claim 2, Petitioner's expert testifies that "while the particular implementation . . . taught by Cioffi generally interleaves the codewords after they are encoded, rather than before as is taught by Divsalar, it would have been obvious to implement the structure and order of operations in Divsalar, while implementing the particular interleaving techniques

described in Cioffi." Wicker Decl. ¶ 180. Again, however, this conclusory assertion is unpersuasive, given the completely different nature of the interleaving techniques of Cioffi discussed above. Even if the order of encoders and interleavers were changed in Cioffi, the interleavers would still be reordering the blocks and leaving the bits within each block unchanged, in contravention of the requirements of claim 1. Ex. 1003, 7:12–8:3; Pachamanov Decl. ¶¶ 75, 94–95.[11]

Petitioner also cites the testimony of Patent Owner's expert to the effect that one of ordinary skill, "looking at Divsalar would be motivated to provide that extra layer of protection [of Cioffi] against burst errors." Pet. Reply 14; Pachamanov Dep. 163. However, that testimony merely indicates that one of ordinary skill could have separately used the "completely different concept" of Cioffi to add "another level of interleaver" following the Divsalar encoder, as "a completely different thing" — as a "separate element of the whole system." Pachamanov Dep. 160, 162, 163. Such an aggregation of two separate modules, performing independent functions, would not fall within the subject matter of claim 2. Pachamanov Decl. ¶¶ 75, 94.

In any event, switching interleavers — even if resulting in varying the permutation — as different operating modes of a device are actuated does

[11] We previously articulated a preliminary view that, in light of the disclosure in Cioffi of selecting different interleavers depending on the nature of the data input, one of ordinary skill in the art would have been motivated to adapt Divsalar to switch interleavers depending on data input. Institution Dec. 15. Based on further review of the more complete record now before us, and for the reasons stated herein, we no longer adhere to that view.

not teach or suggest the limitation recited in claim 2, which requires the permutating device to modify the permutation in time. This claim requirement ensures that erroneous data are consistently varied in time, and are thus continuously checked by a different function, to prevent the non-detection of repetitive errors. Ex. 1003, 2:42–53. Merely varying the permutation on occasion does not address the error correction problems described in the Specification, the solution to which is embodied in claim 2. *In re Smith Int'l, Inc.*, 871 F.3d at 1382–83 (claim interpretation "is an interpretation that corresponds with what and how the inventor describes his invention in the specification"). As Petitioner's counsel conceded during the Hearing, concerning interpretation of this claim limitation,

> [T]he key here is that the patent says that what you do is you vary the function in time. And because at some point the permutation function is different, the odds are very, very low that it will continue to be erroneously determined to be correct data.
>
> . . . .
>
> I think you have to view this from the perspective of a person of skill in the art. A person of skill in the art would agree, I think as you were suggesting, that [varying the function in time is] during the transmission of the data in question, it's not, you know, some other completely unrelated data months down the line or years down the line or any kind of hypothetical situation like that.

Tr. 7, 8. Patent Owner also agrees that the application, to a particular prior art reference, of the requirement that permutations are modified in time, must be from the perspective of one of ordinary skill in the art. Tr. 42–45. From the perspective of a person of skill in the art, the occasional and time-independent switching from one transmission speed to another, or from video to audio transmissions, would not be considered to fall within the

scope of claim 2 — it would not make the "odds are very, very low that [data] will continue to be erroneously determined to be correct data." Tr. 7.

In sum, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claim 2 would have been obvious over the combination of Divsalar and Cioffi.

3. Dependent Claims 3 and 4

Claim 3 depends from claim 2 and additionally requires "wherein the varying is further configured to modify the permutation based on the original data." Claim 4 depends from claim 3 and additionally requires "wherein the permutating device includes a table in which subsequent permutations are stored." Ex. 1003, col. 8, ll. 7–12. Petitioner again asserts Divsalar and Cioffi, taken alone or in combination, render claims 3 and 4 obvious. Pet. 36–42.

Petitioner's arguments and evidence for claims 3 and 4 do not address the above-discussed shortcomings of the combination of Divsalar and Cioffi with respect to claim 2. Therefore, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claims 3 or 4 would have been obvious over Divsalar and Cioffi.

E. Obviousness of Claim 4 Over Divsalar, Cioffi, and Rhines

Petitioner alternatively relies on the combination of Divsalar, Cioffi, and Rhines as rendering the subject matter of claim 4 obvious. Pet. 42–45. Rhines, titled "Triple Orthogonally Interleaved Error Correction System," was filed June 15, 1992, and issued February 21, 1995, and therefore we treat this reference as prior art under 35 U.S.C. § 102(a) for purposes of this Decision. Ex. 1010. Rhines discloses an error "detection and correction"

system that has three stages of encoding with two different interleaving steps preformed between the encoding steps. *Id.* at Abstract. Figure 6 illustrates an interleaver circuit:

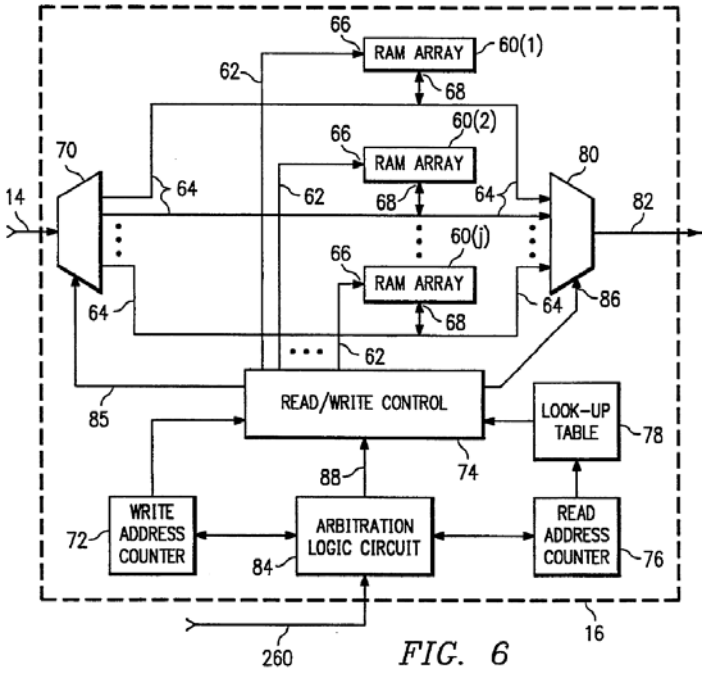


FIG. 6

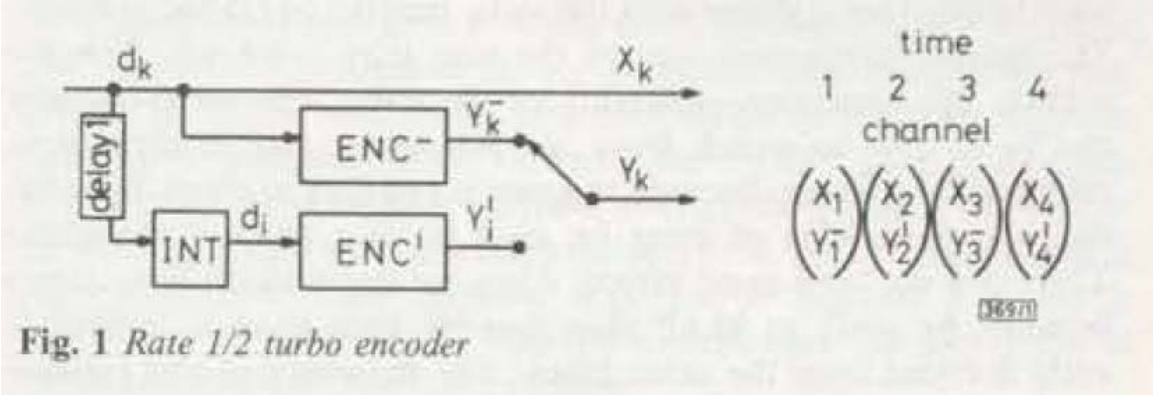
Figure 6 includes a look-up table 78 that is addressed using counts generated by the read access counter 76 to in turn generate read addresses to the RAM arrays 60 so as to interleave the data. *Id.* at 11:62–12:12.

As Patent Owner argues, Rhines does not disclose varying the interleaver shuffling algorithm in a single embodiment or implementation of the disclosed system. PO Resp. 35–36. Nor has Petitioner otherwise provided evidence that the combination of Divsalar, Cioffi, and Rhines teaches or suggests the time-varying limitation of claim 2. Therefore, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claim 4, which depends indirectly from claim 2, is obvious over Divsalar, Cioffi, and Rhines.

F. Obviousness of Claims 1–4 Over Barbulescu and Cioffi

Petitioner alternatively argues obviousness of claims 1–4 over the combination of Barbulescu and Cioffi. Pet. 45–63. As stated above, although claim 1 has been disclaimed, it is necessary to consider the limitations of claim 1 in analyzing dependent claims 2–4.

Barbulescu, titled "Rate-Compatible Turbocodes," has a publication date of March 30, 1995, and no objection has been raised as to its prior art status — therefore we treat this reference under 35 U.S.C. § 102(a). Ex. 1008. Petitioner relies on Barbulescu Figure 1, reproduced below, and accompanying description:



Pet. 46–47. Figure 1 depicts a "Rate ½ turbo encoder" (meaning that each information bit X_k has one associated coded bit Y_k), which includes turbo encoders ENC^- and $ENC^{|}$, the latter encoder preceded by an interleaver INT; Figure 1 also includes a multiplexer (indicated as a switch in the figure) selecting which encoder output (Y_k^- or $Y_i^{|}$) is connected to the Y_k output. Ex. 1008, 535; Wicker Decl. ¶¶ 85, 241, 247.[12]

[12] We cite to the original pagination of Barbulescu rather than to the page numbers of the exhibit added by Petitioner.

Petitioner's arguments with respect to this combination are similar to those for the Divsalar/Cioffi combination discussed above, including, *inter alia,* alternative reliance on Barbulescu alone for obviousness, and the argument that error correction references are effective against error detection subject matter. Pet. 46–47; Wicker Decl. ¶¶ 228, 232–233. As with the Divsalar/Cioffi combination, it is sufficient to consider Barbulescu alone for obviousness of the claim 1 limitations, with the Cioffi reference neither adding to nor detracting from the analysis for the reasons stated above.

Petitioner further provides evidence that Barbulescu satisfies the additional requirement in the claim 1 preamble of "data provided in blocks with each block having plural bits in a particular ordered sequence." Pet. 46–47; Wicker Decl. ¶ 231; Ex. 1008, Fig. 4, 535–36. Petitioner relies on the encoders and multiplexers of Barbulescu Figure 1 (ENC^{l} and the downstream switch) as disclosing the "generating device" limitation of claim 1. Pet. 49–50; Wicker Decl. ¶¶ 240–244. Finally, Petitioner relies on the interleaver, INT, as disclosing the varying device limitation, including the permutation device limitation, of claim 1. Pet. 52–55; Wicker Decl. ¶¶ 247–248, 251–254.

For the claim 2 requirement of "modify[ing] the permutation in time," Petitioner argues Barbulescu "taught modifying the permutation by using a single interleaver and altering in time the multiplexing of data output from the encoders." Pet. 56; Wicker Decl. ¶ 259. However, similar to the operation of Cioffi discussed above, as shown in Figure 1 of Barbulescu, the multiplexer that changes the coding rate from rate ½ to rate ⅓ is placed downstream of the encoders, whereas the claims require the varying device to vary the original data *prior to* supplying the data to the generating device.

PO Resp. 43–44; Ex. 1003, 7:9–11. In addition, the claims require the permutations to be performed on *original data*, and as shown in Figure 1 of Barbulescu, the original data is not changed by the multiplexer. *Id.*

Petitioner also argues that an alternative approach in Barbulescu, illustrated in Figure 4, using two different interleavers for different sub-blocks of each data block, teaches or suggests the claim 2 requirement of modifying the permutation in time. Pet. 58–59; Wicker Decl. ¶ 260.

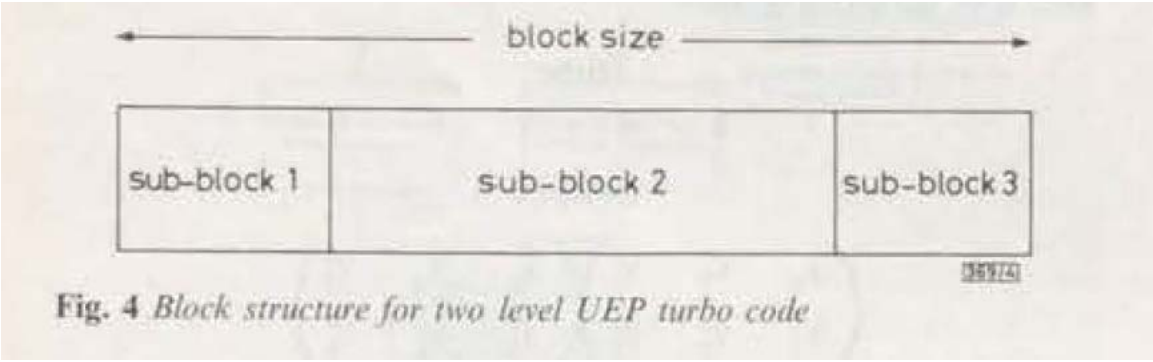


Fig. 4 *Block structure for two level UEP turbo code*

Figure 4 illustrates a block of data that is subdivided into three sub-blocks, where sub-blocks 1 and 3 are encoded with a rate third code, and sub-block 2 is encoded with a rate half code.[13] Ex. 1008, 536. This aspect of Barbulescu is directed to an "unequal error protection" application that requires the information bits at the beginning and at the end of a transmitted block to have a higher level of error protection than the bits in the middle of the block (e.g., "applications such as speech or image compression require some bits to have a higher level of protection than others"). *Id.* at Fig. 4, 535–36. In this case the alleged "permuting device" would consist of two interleavers rather than one:

[13] The lower the code rate, the greater the error control capability. Wicker Decl. ¶ 86. Thus, a rate third code has a better error control capability than a rate half code.

> The information bits are organized as in Fig. 4. The bits included in sub-blocks 1 and 3 will be encoded by a rate third code and interleaved by interleaver I1. The bits included in sub-block 2 will be encoded by a rate half code and interleaved by interleaver I2.

Id. at 536. In particular, in Figure 4, sub-block 1 consists of 72 bits, sub-block 2 has 312 bits, and sub-block 3 has 48 bits. Sub-blocks 1 and 3 are combined and interleaved in a 120-bit interleaver (because 72 bits plus 48 bits totals 120 bits), and sub-block 2 is interleaved in a 312-bit interleaver. *Id.*

Petitioner argues that because the two interleavers are of different size, the permutations from one sub-block to the next are modified, thus resulting in satisfying the claim 2 requirement of modifying the permutation of the data blocks in time. Pet. 58; Pet. Reply 21; Wicker Decl. ¶ 260.

Patent Owner argues that, if the sub-blocks of Figure 4 are to be treated as the blocks of original data under the '662 patent claims, then they are reordered in contravention of the claim 1 requirement that the data blocks not be reordered:

> [T]he bits in sub-blocks 1 and 3 will be interleaved together and reordered amongst themselves, such that some bits from sub-block 3 will be in front of some bits from sub-block 1 and vice versa. This not only destroys the integrity of the original sub-blocks, it reorders them.

PO Resp. 40 (citation omitted). The fact, as stated above, that the 72 bits of sub-block 1 are combined with the 48 bits of sub-block 3 into the single 120-bit interleaver establishes that those two blocks are reordered. PO Resp. 41; Pachamanov Decl. ¶¶ 144–146.

Petitioner argues that even if sub-blocks 1 and 3 are interleaved, they are not reordered, relying on the statement in Barbulescu, "As long as the ***interleaved sequence of information*** bits follows the ***same pattern*** (i.e. belong to the ***same sequence***) as the ***straight sequence of information bits***, the two outputs of the two interleavers can be connected in series." Pet. Reply 20 (quoting Ex. 1008, 536). Petitioner's interpretation of this passage is unsound — it is inconsistent with the unchallenged fact that sub-blocks 1 and 3 are interleaved together, as described above. It is also inconsistent with the very next sentence in Barbulescu, which states, "[a]t the receiver end, the data are split according to the sub-block they belong to in order to be properly deinterleaved"; i.e., they are reordered at the transmitter and only reassembled at the receiver. Ex. 1008, 536. Petitioner cites testimony of Patent Owner's expert in support of its interpretation of the above quoted passage in Barbulescu. Pet. Reply 20–21. That testimony fails to demonstrate to us that Petitioner's interpretation is correct.

We note that there is an alternative way to apply Figure 4 of Barbulescu to the issues here: rather than treating the three sub-blocks shown in the figure as the claimed data blocks, the entire block shown in Figure 4 (the concatenation of sub-blocks 1, 2 and 3) can be so treated. If so viewed, then each block is treated exactly the same, and there is no modification of the permutation in time, as required by claim 2. PO Resp. 42–43; Pachamanov Decl. ¶¶ 141–143. That is, although different interleavers are applied to different groups of bits within each block, the same overall permutation is performed on each block. There is no "modify[ing] the permutation in time," as required by claim 2, because claim 1 requires that the permutation in question is a "permutation of bit

position relative to said particular ordered sequence for *at least some of the bits in each of said blocks*." Ex. 1003, 7:12–8:6 (emphasis added). The fact that for every block, one permutation is applied to one part of the data block, and a different permutation to another part, does not achieve the required modification of the permutation in time. *See id.* at 6:4–5 ("The said permutations can be applied to a data block or to a part of a data block.").

In sum, we agree with Patent Owner that, "if the sub-blocks are defined as blocks, then the blocks themselves are reordered, and if the sub-blocks 1–3 are a single block, then, the permutation is not modified as each subsequent block has the same permutation applied." PO Resp. 39; Pachamanov Decl. ¶¶ 141–146.

Petitioner also repeats its arguments that Cioffi, alone or in combination with Barbulescu, renders claim 2 obvious. Pet. 47–49, 59. However, as discussed above in connection with the combination with Divsalar, Cioffi does not teach or suggest the subject matter of claim 2, and one of ordinary skill would not be motivated to combine Cioffi with Barbulescu for the same reasons as discussed for the combination of Cioffi and Divsalar. Pachamanov Decl. ¶¶ 133–137. In addition, aside from considering each of Barbulescu and Cioffi individually, Petitioner provides no separate rationale demonstrating that the subject matter of claim 2 would have been obvious over the combination of Barbulescu and Cioffi. PO Resp. 37–38.

Therefore, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claim 2 would have been obvious over Barbulescu and Cioffi. Accordingly, we also determine that Petitioner has not demonstrated by a preponderance of the evidence that

the subject matter of claim 3, which depends from claim 2, or claim 4, which depends from claim 3, would have been obvious over Barbulescu and Cioffi.

G. Obviousness of Claim 4 Over Barbulescu, Cioffi, and Rhines

Petitioner alternatively argues the subject matter of claim 4 would have been obvious over the combination of Barbulescu, Cioffi, and Rhines. Pet. 63–66. Petitioner's arguments and evidence for this ground do not address the shortcoming identified above with respect to claim 2. Therefore, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the subject matter of claim 4, which indirectly depends from claim 2, would have been obvious over Barbulescu, Cioffi, and Rhines.

IV. OTHER MATTERS

In addition to the arguments addressed above, Patent Owner raises a constitutional argument: "Patent Owner respectfully objects to this tribunal's exercise of jurisdiction to adjudicate the patentability of the '662 Patent because it would violate Patent Owner's rights under the Takings clause of the Fifth Amendment." PO Resp. 53.

We decline to address this argument. As the Supreme Court has cautioned, "[c]onstitutional questions obviously are unsuited to resolution in administrative hearing procedures and, therefore, access to the courts is essential to the decision of such questions." *Califano v. Sanders*, 430 U.S. 99, 109 (1977).

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that Petitioner has not proved by a preponderance of the evidence that claims 2–4 of U.S. Patent No. 6,212,662 B1 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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