UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NANYA TECHNOLOGY CORPORATION,
NANYA TECHNOLOGY CORPORATION U.S.A., and,
NANYA TECHNOLOGY CORPORATION DELAWARE,
Petitioners,

v.

LONE STAR SILICON INNOVATIONS, LLC,
Patent Owner.

Case IPR2018-00063
Patent No. 6,097,061

PATENT OWNER'S NOTICE OF APPEAL

Notice is hereby given, pursuant to 35 U.S.C. §§ 141(c), 142, and 319, and 37 C.F.R. §§ 90.2(a) and 90.3(a), that Patent Owner Lone Star Silicon Innovations, LLC hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered on May 15, 2019 in IPR2018-00063 (Paper 25) (attached hereto as Exhibit A), and from all underlying orders, decisions, rulings, and opinions that are adverse to Patent Owner, including, without limitation, those within the Decision on Institution of *Inter Partes* Review, entered on May 17, 2018 (Paper 9).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, the Board's claim constructions, the Board's determination that claims 1, 3, 4, 11, 13, and 14 are unpatentable as anticipated by and obvious over U.S. Patent No. 5,300,447 ("Anderson"), the Board's determination that claims 1, 3, 11, and 13 are unpatentable as anticipated by U.S. Patent No. 5,408,116 ("Tanaka"), the Board's determination that claims 11 and 13 are unpatentable as obvious over Tanaka, the Board's determination that claims 1, 3, 11, and 13 are unpatentable as anticipated by U.S. Patent No. 5,998,835 ("Furukawa"), the Board's determination that claims 11 and 13 are unpatentable as obvious over Furukawa, and all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions; the Board's consideration and analysis of the expert testimony, prior art, and other

evidence in the record; and the Board's factual findings, conclusions of law, or other determination supporting or relating to the above issues.

This Notice of Appeal is timely pursuant to 37 C.F.R. § 90.3, having been duly filed within 63 days after the Final Written Decision.

A copy of the Notice of Appeal is being filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice of Appeal is being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit, and the required docketing fee will be paid electronically using pay.gov.

If there is any fee due in connection with the filing of this Notice of Appeal, please charge the fee to Deposit Account No. 06-1135.

Respectfully submitted,

Date: July 17, 2019

/s/Timothy P. Maloney
Timothy P. Maloney
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that, pursuant to 37 C.F.R. §§ 42.6(e)(4) and 90.2, the foregoing PATENT OWNER'S NOTICE OF APPEAL and all accompanying documents, were filed by Priority Mail Express on July 17, 2019, with the Director of the United States Patent and Trademark Office, at the following address:

Director of the U.S. Patent and Trademark Office
Office of the General Counsel
P.O. Box 1450
Alexandria, VA 22313-1450

and that a copy of the foregoing Patent Owner's Notice of Appeal and accompanying documents was filed with the Patent Trial and Appeal Board electronically on July 17, 2019, pursuant to 37 C.F.R. 42.6(b)(1), and that the foregoing Notice of Appeal and accompanying documents were served upon the Petitioner pursuant to 37 C.F.R. 42.6(e)(1) via electronic mail on July 17, 2019, by serving the following attorneys of record as follows:

Vincent Yip
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The undersigned further certifies that a copy of the foregoing Patent Owner's Notice of Appeal and accompanying documents was filed on July 17, 2019 with the United States Court of Appeals for the Federal Circuit through the Court's CM/ECF filing

system and that the filing fee is being paid electronically using pay.gov. In accordance with Fed. Cir. Rule 15(a)(1), a paper copy of the foregoing Notice and accompanying documents are also being sent via Priority Mail Express to the clerk of the Federal Circuit at:

Clerk of Court
United States Court of Appeals for the Federal Circuit
717 Madison Place NW
Washington, DC 20439

Date: July 17, 2019

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Exhibit A

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Paper No. 25
Entered: May 15, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NANYA TECHNOLOGY CORPORATION,
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LONE STAR SILICON INNOVATIONS LLC,
Patent Owner.

Case IPR2018-00063
Patent 6,097,061

Before GRACE KARAFFA OBERMANN, KRISTINA M. KALAN, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Determining That Claims 1, 3, 4, 11, 13
And 14 Are Proven Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

This is an *inter partes* review of claims 1, 3, 4, 11, 13, and 14 ("the challenged claims") of U.S. Patent No. 6,097,061 (Ex. 1001, "the '061 patent"). We instituted review based on grounds set forth in the Petition (Paper 1, "Pet."). Paper 9 ("Dec."), 6–7, 25. We have jurisdiction under 35 U.S.C. § 6. For reasons that follow, we determine that Petitioner shows by a preponderance of the evidence that the challenged claims are unpatentable under both parties' proposed constructions of a key disputed claim phrase. There are no outstanding interlocutory motions.

A. Overview of the Sequence of Briefing

The challenged claims require a semiconductor transistor comprising "a channel region formed in the semiconductor substrate" ("the disputed claim phrase"). Ex. 1001, 7:60, 8:46 (claims 1 and 11, the independent challenged claims). Petitioner does not propose an express construction for the disputed claim phrase in the Petition, but sets forth claim charts that map the phrase to disclosures in the asserted prior art in a manner that alludes to a construction based on the plain and ordinary meaning of the words. *See* Pet. 18–19 (claim construction section), 24–25, 33–34 (claim charts). In the Institution Decision, we invited briefing on specific issues surrounding the meaning of the disputed claim phrase. Dec. 12. Thereafter, in timely sequence, Patent Owner filed a Response (Paper 12, "Resp.") and Petitioner filed a Reply (Paper 15, "Reply") that expressly address the meaning of the disputed claim phrase. Resp. 15–27; Reply 1–9.

After the Reply was filed, but before a final hearing was conducted in this review, the Board issued a final written decision in a co-pending *inter partes* review in which a different petitioner challenged claims 1, 3–6, 11,

and 13–16 of the '061 patent—a decision that declares unpatentable each patent claim challenged here. *See Micron Tech., Inc. v. Lone Star Silicon Innovations LLC*, Case IPR2017-01562, slip op. at 40 (PTAB Dec. 13, 2018) ("*Micron* IPR" or "IPR1562") (Paper 30); *see also* IPR1562, Paper 31 (Patent Owner's Notice of Appeal). In the *Micron* IPR, we construed the disputed claim phrase, "a channel region formed in the semiconductor substrate." IPR1562, Paper 30, 8–24; *see id*. at 23–24 ("We assign the words 'a channel region formed in the semiconductor substrate' (Ex. 1001, claims 1 and 11) their plain and ordinary meaning," which is "broad enough to embrace the area—delineated by the 'spa[t]ial arrangement' of the source, drain, gate, and gate oxide—created to accommodate a channel." (quotation omitted)).

Shortly thereafter, in a teleconference with the Board, the parties requested guidance regarding what effect, if any, the construction of the disputed claim phrase adopted in the *Micron* IPR would have in this proceeding. Paper 20. As a result, we authorized, without any objection from Patent Owner, the simultaneous filing of Petitioner's Supplemental Claim Construction Brief (Paper 21, "Pet. Supp. Br.") and Patent Owner's Supplemental Claim Construction Brief (Paper 22, "PO Supp. Br.")).

Thereafter, also with Board authorization, Patent Owner filed a Response to Petitioner's Supplemental Claim Construction Brief (Paper 23, "PO Resp. Supp. Br."). Although authorized to do so (Paper 20, 5), Petitioner did not file a response to Patent Owner's Supplemental Claim Construction Brief. We conducted a final hearing on February 21, 2019. Paper 24 ("Tr.").

B. Related Proceedings

As explained above, in the *Micron* IPR, we issued a final written decision declaring unpatentable claims 1, 3–6, 11, and 13–16 of the '061 patent, which includes every claim challenged in this review. IPR1562, Paper 30, 40; Pet. 7, 21–57. Patent Owner noticed an appeal in the *Micron* IPR on February 14, 2019. IPR1562, Paper 31.

Patent Owner identifies twenty-three (23) additional petitions for *inter partes* review filed against claims of other patents owned by Patent Owner. Paper 3, 1–2; *see* Paper 13, 1–2 (identifying thirteen (13) additional petitions in an updated mandatory notice). Petitioner, by contrast, identifies no related *inter partes* review proceedings, but indicates an intention to file petitions against three patents "not related to the '061 Patent family." Pet. 6.

Patent Owner further identifies five "actions" involving the '061 patent: (1) *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:17-cv-05458 (N.D. Cal. Oct. 7, 2016) (dismissed without prejudice); (2) *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, Appeal No. 2018-1578 (Fed. Cir. Feb. 15, 2018); (3) *Lone Star Silicon Innovations, LLC v. Micron Technology, Inc.*, No. 3:18-cv-01680 (N.D. Cal. Mar. 16, 2018); (4) *Lone Star Silicon Innovations, LLC v. Nanya Technology Corp.*, No. 3:17-cv-04032 (N.D. Cal. Oct. 7, 2016) (dismissed without prejudice); and (5) *Lone Star Silicon Innovations, LLC v. Nanya Technology Corp.*, Appeal No. 2018-1581 (Fed. Cir. Feb. 15, 2018). Paper 6, 2–3; Paper 13, 2–3. Petitioner identifies as related only the first and fourth actions enumerated above. Pet. 5–6.

C. The '061 patent (Ex. 1001)

The '061 patent, titled "Trenched Gate Metal Oxide Semiconductor Device and Method," was filed March 30, 1998, and issued August 1, 2000. Ex. 1001, at [21], [22], [45], [54]. The '061 patent relates to metal oxide semiconductor ("MOS") devices having a trenched gate. *Id.* at [57].

Figure 2B of the '061 patent is reproduced below.

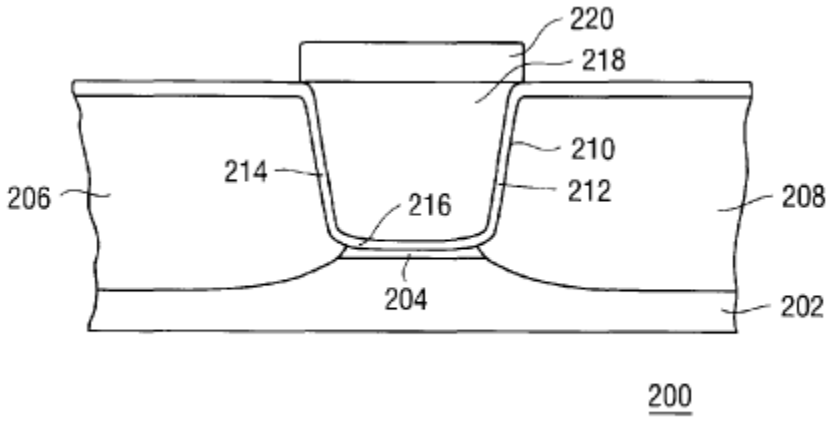


FIG. 2B

Figure 2B, above, is a cross-sectional view of a MOS transistor fabricated according to the principles described in the '061 patent. *Id.* at 2:65–67.

As seen in Figure 2B, semiconductor structure 200 includes substrate 202, channel region 204, source region 206, drain region 208, trench 210, trench-to-gate insulating layer 212, and trenched gate electrode 218. *Id.* at 3:2–8. "Trench-to-gate insulating layer 212 preferably comprises a trench dielectric spacer 214 formed on the vertical surfaces inside trench 210 and a trench gate dielectric 216 formed on the bottom surface inside trench 210." *Id.* at 3:30–33. Tungsten silicide layer 220 may be formed on a top surface of trenched gate electrode 218. *Id.* at 3:60–61.

"Source region 206 and drain region 208 are diffusion regions of semiconductor material that are doped with impurities that have a

conductivity opposite to the conductivity of substrate 202" and "have a depth substantially equal to or greater than the depth of trench 210 and partially extend laterally underneath the bottom of trench 210 to form source and drain junctions disposed along portions of the sidewalls and bottom surface of trench 210." *Id.* at 3:5–8, 3:15–20. In a description of the preferred embodiment of the invention, the specification further refers to "[c]hannel region 204" as "an implanted region formed beneath the bottom surface of trench 210 and as immediately contiguous source region 206 and drain region 208." *Id.* at 3:20–22.

According to the '061 patent, a "trenched polysilicon gate structure improves the overall topography of the structure for better process control and improved manufacturability," "improves the device packing density and scaleability [sic] by reducing the lateral diffusion of the source and drain regions under the trenched polysilicon gate," and "minimizes the process variations of overlaps between the trenched polysilicon gate and the source and drain regions." *Id.* at 1:49–57; *see id.* at 4:30–52; *see also id.* at 1:24–42 (discussing limitations on packing density and performance of conventional transistors formed on top surface of substrate).

D. Illustrative Claim

Of the challenged claims, only claims 1 and 11 are independent. Claims 3 and 4 depend directly from claim 1, whereas claims 13 and 14 depend directly from claim 11. Independent claim 1 of the '061 patent is illustrative of the claimed subject matter and reproduced below.

> 1. A semiconductor transistor comprising:
> a semiconductor substrate of a first conductivity type;

> a source region of a second conductivity type in the semiconductor substrate;
>
> a drain region of the second conductivity type spaced from the source region in the semiconductor substrate;
>
> a trench having substantially upright vertical surfaces and a bottom surface formed in the semiconductor substrate intermediate the source and drain regions;
>
> ***a channel region formed in the semiconductor substrate***, the channel region forming a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions;
>
> a trench-to-gate insulating layer formed on the substantially upright vertical surfaces and the bottom surface inside the trench, the trench-to-gate insulating layer forming a contiguous layer inside the trench; and
>
> a trenched gate electrode having a top surface and formed on the trench-to-gate insulating layer inside the trench.

Ex. 1001, 7:50–8:2 (emphasis added).

E. Overview of the Evidence

Petitioner relies on the following asserted prior art references in the grounds of unpatentability stated in the Petition.

Reference	**Issue Date**	**Exhibit**
U.S. Patent No. 5,300,447 ("Anderson")	Apr. 5, 1994	Ex. 1004
U.S. Patent No. 5,408,116 ("Tanaka")	Apr. 18, 1995	Ex. 1005
U.S. Patent No. 5,998,835 ("Furukawa")	Dec. 7, 1999 (filed Feb. 17, 1998)	Ex. 1006

Pet. 7.

The Petition is supported by a Declaration of Mr. Ron Maltiel, M.S., E.D.[1] Ex. 1003. The Response is supported by two Declarations of W.R. Bottoms, Ph.D. Exs. 2001, 2006. As an initial matter, based on the witnesses' asserted qualifications and information supplied in their curricula vitae, we find Mr. Maltiel and Dr. Bottoms qualified to opine about the perspective of a person of ordinary skill in the art at the time of the invention of the '061 patent. *See* Ex. 1003 ¶¶ 2–13 (Mr. Maltiel's statement of qualifications), Attachment A (Mr. Maltiel's curriculum vitae); Ex. 2001 ¶¶ 6–19 (Dr. Bottoms' statement of qualifications); Ex. 2002 (Dr. Bottoms' curriculum vitae).

F. The Asserted Grounds of Unpatentability

The Petition asserts the following challenges to claims 1, 3, 4, 11, 13, and 14 of the '061 patent.

Reference	**Basis**	**Claims Challenged**
Anderson	§ 102(b)	1, 3, 4, 11, 13, 14
Anderson	§ 103	1, 3, 4, 11, 13, 14
Tanaka	§ 102(b)	1, 3, 11, 13
Tanaka	§ 103	11, 13
Furukawa	§ 102(e)	1, 3, 11, 13
Furukawa	§ 103	11, 13

[1] Mr. Maltiel explains that an Engineer Degree ("E.D.") is a type of degree awarded by Stanford University upon completion of a thesis and two years of additional study beyond a Master's Degree. Ex. 1003 ¶ 3. The focus of an E.D. "is primarily on professional engineering work as opposed to a Ph.D.'s primary focus on theoretical research or university teaching." *Id*.

Pet. 7, 21–57. We instituted review of all of the challenged claims on all grounds set forth in the Petition. Dec. 25.

II. ANALYSIS

In our reproduction of claim 1 above (*supra*, Section I.D), we emphasize the disputed claim phrase, "a channel region formed in the semiconductor substrate." Ex. 1001, claim 1. We organize our analysis into four main sections. First, we resolve the level of ordinary skill in the art. Second, we resolve the meaning of the disputed claim phrase. Third, we provide an overview of the asserted prior art. Fourth, we explain why the challenged claims are proven unpatentable by a preponderance of the evidence not only under the claim construction proposed by Petitioner, but also under the narrower construction advanced by Patent Owner.

In that second section, which resolves the meaning of the disputed claim phrase, we explain why we adopt Petitioner's proposed construction, which is consistent with the meaning assigned in the *Micron* IPR and corresponds to the plain and ordinary meaning of the phrase. Specifically, we determine that "a channel region formed in the semiconductor transistor" means the area created to accommodate a channel; that is, the area "through which current can flow between the source and the drain when a voltage is applied to a gate electrode," as argued by Petitioner in its Supplemental Claim Construction Brief. Pet. Supp. Br. 1.[2] We further explain why we

[2] We recognize that, in the *Micron* IPR, we phrased the construction slightly differently. Pet. Supp. Br. 1 n.1 (quoting IPR1562, Paper 30, 23–24 (construing "a channel region" as "the area – delineated by the "spa[t]ial arrangement" of the source, drain, gate, and gate oxide – created to accommodate a channel")). We agree with Petitioner, however, that "there is no effective difference between the two constructions." *Id.*

reject Patent Owner's counterview that the word "formed" imports implied limitations into the claims, including a requirement that the "channel region" must be created by implantation of separate channel dopants.[3]

A. Level of Ordinary Skill in the Art

We consider the grounds of unpatentability in view of the understanding of a person of ordinary skill in the art at the time of the invention. Petitioner asserts that an ordinarily skilled artisan "would have had at least a Bachelor of Science degree in electrical engineering, physics, chemistry, chemical engineering, material science, or a closely related field and at least 5 years of experience in semiconductor fabrication. Additional appropriate graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education." Pet. 16–17; *see* Ex. 1003 ¶ 47. Patent Owner agrees generally with Petitioner's proposed level of ordinary skill in the art. *See* Resp. 11 (citing Ex. 2006 ¶ 31). We adopt Petitioner's proposed definition of the level of ordinary skill in the art, which is consistent with the level of skill reflected in the specification of the '061 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect the appropriate level of ordinary skill in the art).

B. Meaning of the Disputed Claim Phrase

The '061 patent has expired. Resp. 13; Ex. 1001, at [22] (filing date of March 30, 1998). Accordingly, we apply a district court-type claim

[3] The term "separate channel dopants" is used herein to mean dopants "separate and additional to the general doping of the substrate." Resp. 2–3.

construction approach.[4] *Wasica Finance GmbH v. Continental Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017) ("The Board construes claims of an expired patent in accordance with *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc)."). Under the *Phillips* standard, we assign claim terms their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1312–19; *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

The parties disagree about the meaning of the disputed claim phrase, "a channel region formed in the semiconductor substrate," which is required by the independent claims and inherited by each challenged dependent claim. Ex. 1001, claims 1 and 11 (the independent challenged claims). Patent Owner submits that the disputed claim phrase requires a "channel region" formed by implantation of channel dopants "separate and additional to the general doping of the substrate." Resp. 16. Petitioner disagrees, arguing that the ordinary and customary meaning of the disputed claim phrase applies and is broad enough to embrace a channel region formed without separate channel dopants. Pet. Supp. Br. 1. Specifically, in Petitioner's view, a "channel region" is an area created—and delineated by the placement of the source, drain, gate, and gate oxide—to accommodate a

[4] A recent rule change that makes applicable the *Phillips* standard in all trial proceedings before the Board does not apply here, because the Petition was filed before November 13, 2018. *See* "Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board," 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b), effective November 13, 2018).

channel where current flows when a voltage is applied to the gate electrode in a MOS transistor. *Id.* ("the plain and ordinary meaning of 'channel region'" is "the region through which current can flow between the source and the drain when a voltage is applied to a gate electrode"); *see* Pet. 24–25, 33–34 (claim charts); Reply 1–9 (argument and evidence on the ordinary and customary meaning); PO Supp. Br. 1–9 (additional evidence on point).

We find significant that Dr. Bottoms, Patent Owner's witness, confirms that plain and ordinary meaning of the disputed claim phrase. On that point, Dr. Bottoms explains that the area delineated by gate, substrate, source, and drain is customarily recognized as "a channel region" in a MOS transistor and the channel region becomes a channel when "current is flowing." Ex. 1016, 87:14–18; *see* Pet. Supp. Br. 2–3 (quoting that testimony). In other words, the parties agree about the meaning of the disputed claim phrase in typical use. Patent Owner argues, however, that the disputed claim phrase must be assigned a meaning "different from its typical use." Resp. 21. In that regard, Patent Owner focuses on the word "formed" in the disputed claim phrase. *See* PO Supp. Br. 2–3.

In Patent Owner's view, the word "formed" in the phrase, "a channel region formed in the semiconductor substrate," imposes three unstated limitations on the formation of the claimed "channel region"—namely, "channel region" formation must (1) occur during manufacture of the transistor, (2) result in a structural feature that exists whether or not the transistor is in use, i.e., whether or not a voltage is applied to the gate, and (3) be accomplished by implanting separate channel dopants. *Id.*; Resp. 16, 19, 21, 25. Patent Owner does not identify persuasive evidence, however, that the single word "formed," properly construed, imports into the claims a

host of unstated requirements on channel region formation. *See* Resp. 16, 19, 21, 25 (and evidence cited therein); PO Supp. Br. 2–3 (same).

In any event, under the correct construction assigned here and in the *Micron* IPR, a "channel region" is formed during manufacture as a structural feature of the transistor (meeting Patent Owner's first proposed unstated limitation). The structure—delineated by the placement of source, drain, gate, and gate oxide—is designed to accommodate a channel and, accordingly, exists whether or not current is flowing between the source and drain regions (meeting Patent Owner's second proposed unstated limitation). That leaves only Patent Owner's third proposed unstated limitation; namely, that the word "formed" in the phrase, "a channel region formed in the semiconductor substrate," effectively rewrites the claim language to require "a channel region formed ***by implanting a separate channel dopant*** in the semiconductor substrate." Ex. 1001, claims 1 and 11 (the independent claims) (emphasizing the additional limitation imported under Patent Owner's proposed construction of the word "formed)).

That argument is unpersuasive. The claims recite "a semiconductor substrate of a first conductivity type," source and drain regions "of a second conductivity type," and "a channel region formed in the semiconductor substrate . . . immediately contiguous to the source and drain regions." Ex. 1001, claims 1 and 11 (the independent challenged claims). The claims do not, however, specify a conductivity type of the channel region different from the substrate, nor do they require implantation of a separate channel dopant. *Id*. Further, although the '061 patent describes a channel region that is "formed using an implant of boron," (i.e., a separate channel dopant), that description is consistently identified as merely "one" or a "preferred

embodiment" of the invention. Ex. 1001, 1:58, 1:62–64 ("[i]n one embodiment of the present invention," a channel region "is implanted in the substrate beneath the bottom surface of the trench"), 2:40–41, 3:20–23 ("[p]referred [e]mbodiment" includes a "[c]hannel region" that is "an implanted region formed beneath the bottom surface of [the] trench"), 4:55, 4:65–66, 5:36–45 ("one embodiment" or "a preferred embodiment of the present invention" includes a channel region formed using a boron implant), 7:29–28, 7:40–41 (in "one embodiment" "the substrate is ion implanted to form 414 the channel region for the device.").

Those disclosures expressly confine the use of separate channel dopants to certain, but not all, individual embodiments of the invention, and persuade us that the patentee did not disavow other ways of creating the claimed "channel region." Nor does the patentee expressly redefine the disputed claim phrase to exclude a channel region formed as a region of the substrate where current flows between the source and drain regions when a voltage is applied to the gate. Resp. 5 (Patent Owner, acknowledging that "an induced channel with a length defined by the distance between the source and drain is created when the current flows between the source and drain regions").

"The standards for finding lexicography and disavowal are exacting" and it may be "improper to import limitations even from [a] sole embodiment." *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004). In *Thorner*, moreover, our reviewing court reversed a decision that narrowed the plain and ordinary meaning of a claim term to comport with the manner in which the term was "consistently use[d]" in "the

embodiments in the specification." *Thorner*, 669 F.3d at 1365. The principles set forth in the *Thorner* decision guide our resolution of the correct construction of the disputed claim phrase. *See id*. There, "the district court improperly limited" the claim terms in view of embodiments described in the specification. *Id*. at 1369. We decline to do so here.

The patentee did not, through "lexicography or disavowal" (*id*. at 1367–68), narrow the plain and ordinary meaning of the phrase "a channel region formed in the semiconductor substrate." We recognize that the specification repeatedly describes a channel region characterized by separate channel dopants—and, to be sure, a separately doped channel region may fall within the scope of the challenged claims. But we cannot ignore that the patentee consistently describes a channel region implanted with separate channel dopants as merely "one embodiment" or a "preferred embodiment" of the claimed invention. Ex. 1001, 1:58, 61–64, 3:20–23, 5:40–42, 7:28–29, 7:40–41. That circumstance, combined with the breadth of the claim language itself, persuades us that the patentee set forth in the specification a preferred embodiment that is "exemplary in nature," but did not convey, with sufficient clarity or deliberateness, an intent to "define the outer limits of the claim term." *Phillips*, 415 F.3d at 1323.

We recognize that "there is sometimes a fine line between reading a claim in light of the specification, and reading a limitation into the claim from the specification." *Phillips*, 415 F.3d at 1323 (quoting *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186–87 (Fed. Cir. 1998)). The plain language of the claims at issue here, however, neither limits the "channel region" to an area formed by implantation of separate channel dopants nor excludes a "channel region" that is "created to accommodate a

channel" (Pet. Supp. Br. 1 n.1) formed "[w]hen voltage is applied between the source and drain regions and to the gate" in a MOS transistor (Resp. 25).

Because "[t]he claims themselves set forth the limits of the patent grant" (*Phillips*, 415 F.3d at 1323), we come back again to the broad language of the claims. On that point, Patent Owner argues that Petitioner's interpretation of the disputed claim phrase "renders superfluous" the claim limitation requiring that the "channel region" must be "formed in the semiconductor substrate" as "a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions." PO Supp. Br. 2 (citing Ex. 1001, claims 1 and 11). That argument does not take account of the prosecution history of the '061 patent, during which the additional limitation was amended to distinguish the Yin reference.[5] Pet. 15–16 (discussing claim amendment and arguments distinguishing Yin during prosecution). Specifically, during patent prosecution, "the application leading to the '061 patent was initially rejected over the Yin reference," which "'discloses a fundamentally different type of transistor'—a thin layer of conductive material as the channel, rather than a conductive substrate." Reply 5 (quoting Ex. 2006 ¶ 46); *see also* Resp. 12–13 (discussing Patent Owner's annotated reproduction of Yin's Figure 2).

The additional limitation identified by Patent Owner is not "superfluous" when the disputed claim phrase is assigned its ordinary and customary meaning as proposed by Petitioner. PO Supp. Br. 2. On the contrary, the additional limitation continues to distinguish the claimed MOS transistor from Yin's thin-film transistor. Reply 4–5 ("the patentee added

[5] U.S. Patent No. 5,883,399 (Ex. 2005, "Yin").

the additional limitation that the channel region be a contiguous region" to traverse the rejection based on Yin) (citing Ex. 1001, 1:24–34; Ex. 1002, 73–75, 94, 100–102; Ex. 2005, 1:29–33, 3:19–21; Ex. 2006 ¶ 46; Resp. 11–13). As Petitioner persuasively points out, even though Yin discloses an undoped channel, the patentee distinguished Yin based on the structure of the channel region as contiguous, not based on any requirement for separate channel doping. Reply 4; *see* PO Supp. Br. 7 (prosecution argument emphasized that the channel region is a "contiguous" region, suggesting that it has "a particular structure"); PO Resp. Supp. Br. 3 (describing structure of Yin's first and second channel layers). Nothing about "the context in which" the disputed claim phrase "is used in the asserted claim" supports Patent Owner's view that the phrase requires "a channel region defined by the presence of dopants that are separate or additional relative to the semiconductor substrate of a first conductivity type." PO Resp. Supp. Br. 2 (quoting *Phillips*, 415 F.3d at 1314); 6.

Patent Owner argues, and we agree, that there is a preference for assigning meaning to all terms in a patent claim, and that an "interpretation that renders the other phrases of the claim 'superfluous' is disfavored." PO Supp. Br. 2 (quoting *Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007). That preference, however, "is not an inflexible rule that supersedes all other principles of claim construction." *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016) (citation omitted). Patent Owner identifies no persuasive reasons why the preference comes into play here, but even if it does, the preference does not supersede the principle of construction that requires a patentee to set forth with reasonable clarity and precision in the specification any special

definitions that narrow the plain and ordinary meaning of words that appear in a patent claim.

We recognize that, in our Institution Decision, we preliminarily determined that the challenged claims "require something 'more than a channel region that is merely a place within the semiconductor substrate.'" Dec. 25. We made that finding on a preliminary record and invited the parties to further brief that specific issue. *Id*. at 12. In addition, we authorized a supplemental round of briefing, beyond that generally provided by our rules, after we construed the disputed claim phrase in the *Micron* IPR and before the final hearing in this review. Paper 20.

Based on the entirety of the information presented by both parties in this proceeding, we are persuaded that the disputed claim phrase should be assigned its ordinary and customary meaning at the time of the invention. Based on the evidence of that meaning adduced at trial, we determine that the claim phrase, "a channel region formed in the semiconductor substrate," is the area created in a semiconductor substrate—as delineated by source, drain, gate, and gate oxide—designed to accommodate a channel, whether or not the channel is created by implanting separate channel dopants.

The parties propose express constructions for other claim terms. Pet. 17–19; Resp. 27–30. For example, Patent Owner argues that "the word 'contiguous' means 'being in actual contact: touching along a boundary or at a point.'" Resp. 27. We determine, however, that, except for the disputed claim phrase discussed above, no other claim term requires express construction for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the

extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). To the extent any other claim term requires discussion, however, we provide it in our analysis of the patentability challenges.

We next turn to the patentability challenges, explaining why Petitioner proves by a preponderance of the evidence that the challenged claims are unpatentable under Petitioner's proposed construction of the disputed claim phrase and, alternatively, under the narrower construction proposed by Patent Owner.

C. Overview of the Asserted Prior Art References

Anderson (Ex. 1004)

Anderson relates to an "extremely small minimum scaled Metal-Oxide-Semiconductor, MOS, transistor." Ex. 1004, at [57]. Figures 1a and 1b of Anderson are reproduced below.

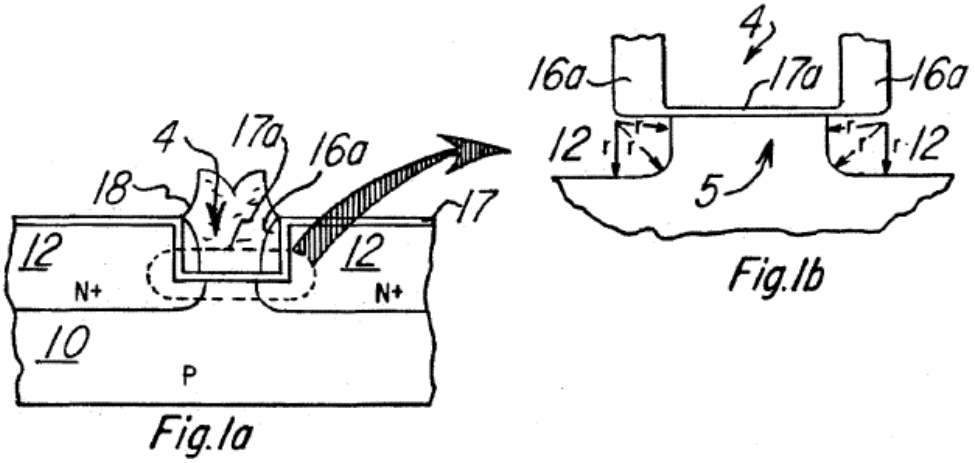


Figure 1a, above, is a sectional view of a semiconductor device according to Anderson, and Figure 1b, also above, is an enlarged view of the channel area of the semiconductor device of Figure 1a. *Id.* at 2:46–50. As seen in the figures, the semiconductor device includes p-type substrate 10, gate

conductor 18 formed in trench 4, doped regions 12 (source and drain), channel 5, and insulators 16a, 17a. *Id.* at 2:58–3:43.

Tanaka (Ex. 1005)

Tanaka relates to a "grooved gate transistor" having particular shape characteristics such that the threshold voltage does not decrease and the threshold voltage can be adjusted by shape. Ex. 1005, at [57].

Figures 1A and 7A of Tanaka are reproduced below.

FIG. 1A

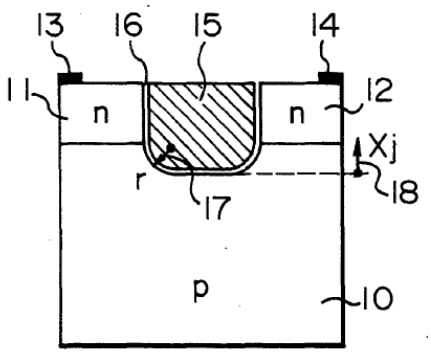
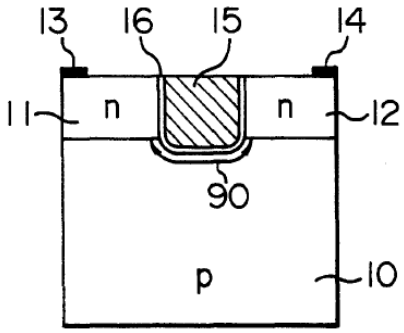


FIG. 7A



Figures 1A and 7A, above, are sectional views of a semiconductor device according to Tanaka. *Id.* at 3:8–19, 3:27–30. As seen in each of Figures 1A and 7A, the semiconductor device includes p type-silicon substrate 10, n type-diffused layers 11, 12, source electrode 13, drain electrode 14, gate electrode 15, and oxide 16. *Id.* at 3:50–58. Figure 1A further illustrates a junction depth X_j 18 of diffused layers 11, 12 relative to the groove bottom and a radius of curvature r 17 of gate electrode 15, each of which is related to the particular shape of gate electrode 15 according to the embodiments of Tanaka. *Id.* at 3:59–68. Channel length 90 is illustrated in Figure 7A. *See id.* at 1:46–47, 3:27–30.

Furukawa (Ex. 1006)

Furukawa relates to a "MOSFET device and a method of manufacturing the device." Ex. 1006, at [57]. Figure 3 of Furukawa is reproduced below.

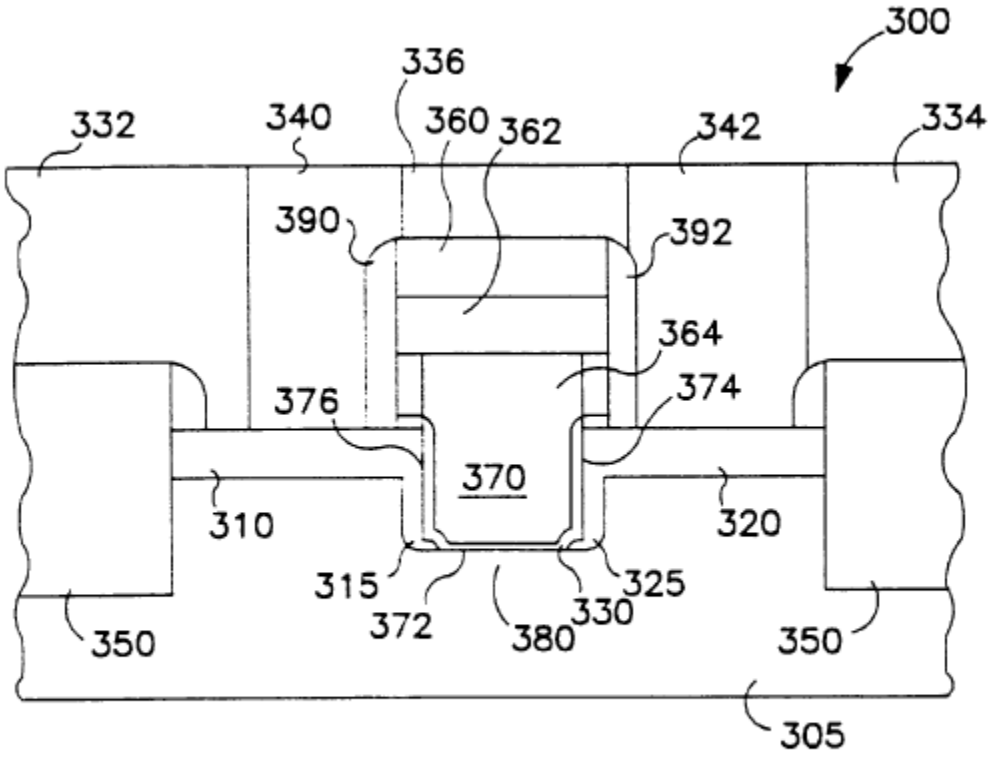


FIG. 3

Figure 3, above, is a sectional view of a semiconductor device according to Furukawa. *Id.* at 2:48, 2:52–53. As seen in Figure 3, apparatus 300 includes, in relevant part, substrate 305 of a first polarity type, trench 370, dielectric layer 330 coating sidewalls 374, 376 and bottom 372 of the trench, conductor 364, diffusion layers 310, 320 of a second polarity type, and diffusion extensions 315, 325 also of a second polarity type. *Id.* at 3:9–45.

As described in Furukawa, "device channel 380 is formed adjacent the bottom of a trench 370 in a substrate 305." *Id.* at 3:12–13. Further, "diffusion layers 310, 320 are connected to the edge of the device channel 380 by diffusion extensions 315, 325." *Id.* at 3:16–18. Regarding the method of manufacture of the semiconductor device, Furukawa describes, as a separately enumerated step, "forming a device channel under the bottom of the trench." *See id.* at 4:43–53.

D. Assessment of the Asserted Grounds of Unpatentability

We next turn to an assessment of the asserted grounds of unpatentability stated in the Petition. As an initial matter, we observe that neither party directs our attention to any objective evidence of non-obviousness. *See, e.g.*, Resp. Because we have no objective evidence of non-obviousness to consider, we focus our discussion on the asserted grounds of unpatentability based on the prior art asserted in the Petition.

1. Asserted Grounds Based on Anderson

Petitioner asserts that claims 1, 3, 4, 11, 13, and 14 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Anderson. Pet. 7, 21–36. Petitioner further asserts that the subject matter of those claims would have been obvious under 35 U.S.C. § 103 in view of Anderson. *Id.* at 7, 36–38.

The following table provides a summary of Petitioner's mapping of Anderson to the structural elements of claim 1, to the extent not specifically disputed by Patent Owner in the Response.

Claim 1 structure	Disclosure in Anderson cited by Petitioner
semiconductor transistor	"An extremely small minimum scaled Metal-Oxide-Semiconductor, MOS, transistor." (Ex. 1004, at [57])
semiconductor substrate	semiconductor substrate 10 (p-type) (*id.* at 2:58–66, Fig. 1a)
source region	doped region 12 (n-type) [one of the two doped regions 12 is the source] (*id.* at 3:8–11, Fig. 1a)
drain region	doped region 12 (n-type) [the other of the two doped regions 12 is the drain] (*id.* at 3:8–11, Fig. 1a)
trench	trench 4 (*id.* at 3:3–15, Fig. 2)
trench-to-gate insulating layer	gate oxide layer 15 and gate oxide layer 17a (*id.* at 4:23–30, 4:34–46, Fig. 4) -or- gate oxide layer 15, nitride sidewalls 16a, and gate oxide layer 17a (*id.* at 4:23–30, 4:34–46, 5:15–18, 5:21–26, Fig. 4)
trenched gate electrode	gate conductor 18 (*id.* at 2:58–3:7, 4:48–56)

See Pet. 21–28 (citing Ex. 1003 ¶¶ 61–63, 65, 67, 69, 73); *see* Resp. 33–42.

Claim 1 also includes the disputed claim phrase, "a channel region formed in the semiconductor substrate." Ex. 1001, 7:60. For that feature, Petitioner relies on channel 5 of Anderson. Pet. 24–25; Ex. 1003 ¶ 65. Petitioner identifies disclosures in Anderson, which teach that "[t]he channel is formed under the recess" (in which gate conductor 18 is later formed) "by an anneal step which drives the [source/drain] dopant into the semiconductor substrate and around the recess corners" (Pet. 24 (citing Ex. 1004, at [57])) and "[t]he bottom of the N+ source/drain regions 12 next to channel 5

extend below the trench 4 on either side" (*id.* (citing Ex. 1004, 3:12–14)). *See* Ex. 1004, 2:22–34 ("Summary of the Invention," explaining that Anderson fabricates a MOS transistor in which a "channel is formed under the recess" of a trench and "places source/drain" regions "on either side of the recess"); *see also id.*, Fig. 1b, Fig. 6 (illustrating the arrangement in which channel 5 is in direct physical contact with the source, drain, and bottom of the trench); Pet. 24 (citing and discussing those disclosures).

Those cited passages persuasively demonstrate that Anderson discloses "a channel region formed in the semiconductor substrate" (Ex. 1001, claims 1 and 11) that is created by defining an area—delineated by source, drain, gate, and gate oxide—designed to accommodate a channel. That area is created at the time of manufacture of the MOS transistor (by Anderson's annealing step) and Anderson's channel 5 exists whether the transistor is idle or in use. *See, e.g.*, Ex. 1004, Fig. 1b, Fig. 6. We are persuaded, therefore, that Anderson's channel 5 meets the disputed claim phrase. *See* Pet. 24–25, 33–34 (claim charts).

Patent Owner does not dispute those facts. Resp. 33–41. Instead, Patent Owner argues, "Anderson must be proven to have a channel region formed in the semiconductor substrate" that is "defined by a region with additional dopants." *Id.* at 37–38. For reasons stated above, however, claim 1 does not require a "channel region" defined by separate channel dopants. Anderson defines a region by the spatial arrangement of source, drain, gate, and gate oxide, and that region is designed to accommodate the flow of current when a voltage is applied to the transistor during normal use.

Petitioner also persuasively maps the features of the dependent challenged claims (namely, claims 3, 4, 13, and 14) to disclosures in

Anderson, and Patent Owner raises no persuasive evidence refuting those points. *Compare* Pet. 28–36 (claim charts), *with* Resp. 30–32, 35–41 (offering no countervailing information, except to argue that "Anderson's channel 5 is not a doped region formed in the semiconductor substrate" and, therefore, "Anderson does not anticipate" any challenged claim). Accordingly, we find Petitioner shows by a preponderance of the evidence that Anderson anticipates claims 1, 3, 4, 11, 13, and 14 of the '061 patent.

Petitioner provides additional information that those claims are unpatentable as obvious in view of Anderson. Pet. 7, 36–38. Specifically, Petitioner directs us to persuasive evidence that, to the extent that Anderson does not expressly disclose the "trench-to-gate insulating layer" required by claims 1, 3, and 4, an ordinarily skilled artisan would have been led to modify Anderson's MOS transistor in a series of steps that results in the subject matter of those claims. Pet. 37 (citing Ex. 1003 ¶ 68). As to claims 11, 13, and 14, Petitioner also identifies evidence that an ordinarily skilled artisan would have been led by Anderson's disclosure to "a structure having 'an array of multiple device structures supported on a semiconductor substrate . . ., each device structure spaced from other device structures'" as required by those claims. *Id*. at 37–38 (citing Ex. 1004, 1:19–32 (Anderson's disclosure that "[s]emiconductor devices are widely used throughout the electronics industry. One factor driving their use is the ability to put more and more circuits on a silicon chip" and some "microprocessors are now produced that have more than one million transistors on a chip"); Ex. 1003 ¶ 77 (Dr. Maltiel's declaration testimony)).

Patent Owner does not refute those facts, which are supported by a preponderance of the evidence, and which we accept in the absence of

contradictory evidence. Instead, Patent Owner asserts that the challenged claims require a "channel region" implanted with separate channel dopants. Resp. 41–42. Our reasoning above applies with equal force to the challenge based on obviousness—that is, the claims do not require a "channel region" formed by implantation of separate channel dopants. Accordingly, we determine that Petitioner shows by a preponderance of the evidence that claims 1, 3, 4, 11, 13, and 14 are unpatentable as obvious over Anderson.

In reaching our ultimate conclusion that the challenged claims are anticipated by, and obvious over, the disclosure of Anderson, we find persuasive that Patent Owner "admits that there is a region between the source and drain regions" in Anderson "where current will flow when a voltage is applied to the gate." Reply 11–12 (emphasis omitted); *see* Resp. 37–38 (Patent Owner stating that Anderson's device "induces a channel between the source and the drain" (*id*. at 37) or "will induce a channel between the source and drain" (*id*. at 38)). However, even if we accept Patent Owner's view that the claimed "channel region" is formed by implantation of separate channel dopants, our ultimate conclusion that the claims are unpatentable over Anderson would not change. That is because Petitioner directs us to persuasive evidence that Anderson anticipates, or would have made obvious, the subject matter of the challenged claims even under Patent Owner's narrower interpretation of the disputed claim phrase.

Specifically, on that point, Petitioner shows persuasively that Anderson discloses, or at least suggests, "additional doping of the channel region." Reply 12. Anderson states, "it may be desirable to perform a voltage threshold, Vt, step to adjust the threshold of the transistor." *Id*. (citing Ex. 1004, Fig. 2; quoting Ex. 1004, 4:15–19). Anderson further

explains that this step may be accomplished by using "[a]n ion implant with or without a thin screen oxide." *Id*. Any doubt that Anderson implants a separate channel dopant in a "channel region" is laid to rest by the testimony of Patent Owner's own witness. Dr. Bottoms admits that, in Anderson's transistor, "the doping profile of the region between the source and drain may contain a channel implant." Reply 12 (quoting Ex. 2006 ¶ 93); *see* Ex. 1016, 116:16–117:16 (Dr. Bottoms testifying that "one of the ways" that Anderson forms a channel region "is through an ion implant").

In other words, Anderson discloses a "channel region" in a MOS transistor created by implanting separate channel dopants. Anderson's implanted channel region directly contacts the source and drain regions and spans the entire length beneath the trench. Resp. 27 (arguing that "contiguous" in the claims means "direct contact"); Pet. 24 (claim chart, and evidence cited therein); Ex. 1004, 2:25–41 (Anderson's summary of invention, explaining those relationships), Figs. 1b and 6 (illustrating the spatial relationship between regions). Taken together, those disclosures in Anderson describe a transistor that meets the challenged claims even under Patent Owner's narrower construction of the disputed claim phrase. *See, e.g.*, Ex. 1016, 116:16–117:16 (Dr. Bottoms testifying that "one of the ways" that Anderson forms a channel region "is through an ion implant").

Our conclusion that each challenged claim is unpatentable on the grounds based on Anderson resolves the parties' dispute. *See* 35 U.S.C. § 318(a) ("if a review is instituted and not dismissed, the Board must issue a final written decision with respect to the patentability of any patent claim challenged by petitioner"). For completeness, however, we provide below an analysis of the grounds based on Tanaka and Furukawa, which supplies

further support for our ultimate conclusion as it pertains to a subset of the challenged claims—specifically, claims 1, 3, 11, and 13—and our determination that those claims are proven unpatentable by a preponderance of the evidence, regardless of which construction advanced by the parties is applied to the disputed claim phrase, "a channel region formed in the semiconductor substrate."

2. Asserted Grounds Based on Tanaka

Petitioner asserts that claims 1, 3, 11, and 13 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Tanaka. Pet. 7, 38–46. In addition, Petitioner asserts that the subject matter of claims 11 and 13 would have been obvious under 35 U.S.C. § 103 in view of Tanaka. *Id.* at 46–47.

The following table provides a summary of Petitioner's mapping of Tanaka to the structural elements of claim 1, to the extent not specifically disputed by Patent Owner in the Response.

Claim 1 structure	**Disclosure in Tanaka cited by Petitioner**
semiconductor transistor	"The present invention relates to a semiconductor device, or more in particular to a fine-structured MOS transistor." (Ex. 1005, 1:7–9, Fig. 1)
semiconductor substrate	p type-silicon substrate 10 (*id.* at 4:5–8; *see also id.* at 3:45–53)
source region	n type-diffused layer 11 (*id.* at 4:13–15, 4:20–28, 3:49–54, 3:56–58)
drain region	n type-diffused layer 12 (*id.* at 4:13–15, 4:20–28, 3:49–54, 3:56–58)
trench	groove in which gate electrode 15 is formed (*id.* at 4:20–30, 4:5–8, Fig. 1A)

Claim 1 structure	**Disclosure in Tanaka cited by Petitioner**
trench-to-gate insulating layer	gate oxide 16 (*id.* at 4:20–31, Fig. 1A)
trenched gate electrode	gate electrode 15 (*id.* at 4:20–36)

See Pet. 38–43 (citing Ex. 1003 ¶¶ 80–84, 86–87); *see* Resp. 42–57.

Claim 1 further includes the disputed claim phrase. Regarding that feature, Petitioner directs us to Tanaka's channel region 90, located at the bottom of a gate trench. Pet. 42 (citing Ex. 1005, Figs. 1A, 7A; Ex. 1003 ¶ 85). Petitioner also points out Tanaka's disclosure that "Boron (B) . . . is injected . . . to form a p type-impurity region as channel doping." *Id.* (quoting Ex. 1005, 4:31–33). Petitioner argues that an ordinarily skilled artisan "would understand that channel region 90 is contiguous and directly connects to the source region (11) and drain region (12)." *Id.* (citing Ex. 1003 ¶ 85). Further, Patent Owner admits that Tanaka discloses "a channel length 90 that extends from the doped source region 11 to the doped drain region 12 around the bottom surface of the groove." Resp. 46 (referring to embodiments depicted in Tanaka's Figures 7A and 7B).

There is no dispute that those disclosures in Tanaka describe a region of the semiconductor substrate—delineated by source, drain, gate, and gate oxide—that is formed to accommodate a channel. Instead, here again, Patent Owner argues that the asserted prior art reference fails to disclose the claimed "channel region," which, in Patent Owner's view, must be "formed by including doping separate from the general doping of the semiconductor substrate." Resp. 52; *see id.* at 46–53 (for repetitions of that argument). In that regard, Patent Owner submits, "Tanaka identifies a channel (depicted by induced channel length 90 at the bottom of the gate trench) that does not

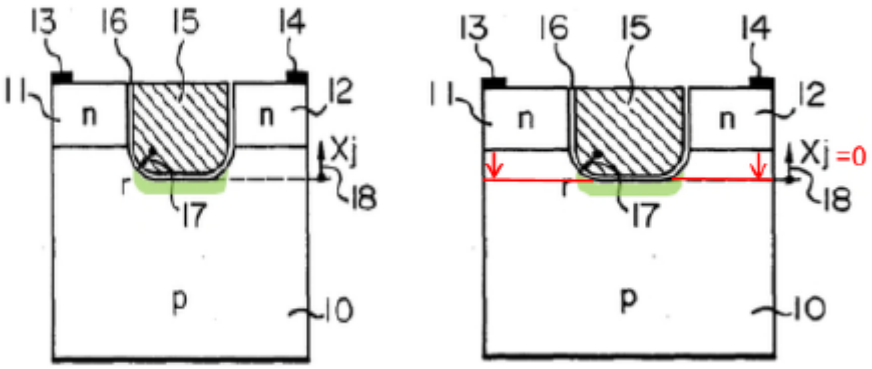
have doping separate and additional to the general doping of the semiconductor substrate." *Id*. at 53. Patent Owner further argues, "[n]o channel exists" in Tanaka's transistor "unless the appropriate voltages are applied to the source, drain, and gate to include a channel and allow current to flow." *Id*. at 46–47.

Significantly, however, Patent Owner also acknowledges that "Tanaka discloses" at least "two embodiments having a separately implanted channel dopant." *Id*. at 48; *see id*. at 49 (Patent Owner admitting "Tanaka discloses providing a separately implanted channel region directly beneath" the trench). Regarding those embodiments, Patent Owner argues that Tanaka fails to describe separate channel dopant implanted "along the side" portion "of a gate electrode groove." *Id*. at 49 (including an annotated reproduction of Tanaka's Figure 1A). Patent Owner submits, on that basis, that Tanaka's channel region, even if formed using separate channel dopants, does not "contact the source and drain regions." *Id*. (citing Ex. 2006 ¶ 81; Ex. 1005, Fig. 1A); *see id*. at 49–51 (presenting similar arguments in connection with Tanaka's Figures 4A, 4B, 7A, and 7B) (also citing Ex. 1005, 6:40–49).

We disagree with Patent Owner's position, because it does not take account of the entirety of Tanaka's disclosure. Specifically, Patent Owner focuses on Tanaka's figures, without considering adequately corresponding disclosures in Tanaka's text. In that regard, we agree with Patent Owner that Tanaka's figures depict embodiments in which the source and drain regions extend to a depth less than the depth of the gate groove—resulting in a "junction depth" that is "above the groove bottom." Reply 15 (reproducing Ex. 1005, Fig. 1A); *see* Resp. 42–51 (for Patent Owner's argument); *see id*. at 47 (citing Ex. 1005, Figs. 1A, 2, 5, 7A, 7B, and 10–11). Tanaka's text,

however, expressly teaches the desirability of forming the source and drain regions below the bottom of the gate. Reply 16–17 (citing Ex. 1005, 5:14–20). As Petitioner explains, that configuration, expressly described in Tanaka, results in a MOS transistor in which the source and drain regions "end below the bottom of the gate" and without any "vertical component" separating the channel region from the source and drain regions. *Id*. at 17.

We agree with Petitioner that Tanaka, fairly read in its entirety, discloses a MOS transistor having the claimed "channel region" formed as "a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions," as required by independent claim 1. *Id*. at 13–19 (discussing Ex. 1005, Figs. 1A, 6, and 7A as explained by textual disclosures at 3:59–60, 5:14–20); Ex. 1001, 7:60–63 (claim 1) (for quoted limitation). That point is driven home by comparing Patent Owner's annotated version of Tanaka's Figure 1A with Petitioner's annotated version of that same figure:



Resp. 49; Reply 19. The above figure is a side-by-side comparison of the Patent Owner's (left) and Petitioner's (right) annotated versions of Tanaka's Figure 1A, which is a sectional view of a MOS transistor. Both Patent Owner and Petitioner annotate Tanaka's Figure 1A to include a green shaded

area that represents a channel region beneath the trench. Petitioner further emphasizes the junction depth, "X_j," by inclusion of red annotations.

Patent Owner's annotated version of Tanaka's Figure 1A does not illustrate the full scope of Tanaka's disclosure, including the embodiment in which junction depth X_j is greater than zero. Textual disclosures in Tanaka expressly contemplate such an embodiment, which anticipates a "channel region" as specified in claim 1. Reply 19; Ex. 1005, 3:59–60 (discussing an embodiment in which "X_j <0," i.e., "the junction depth is above the grooved bottom" of the trench), 5:14–20 (discussing an embodiment in which "the junction depth X_j>0," which results in the trench bottom and source and drain regions being in direct contact with the green-shaded channel in the parties' reproductions of Figure 1A). Stated somewhat differently, when the junction depth (annotated in red by Petitioner in the above reproduction of Tanaka's Figure 1A) is greater than zero, Tanaka's channel region is "immediately contiguous to the source and drain regions," as required by the independent claims. Ex. 1001, 7:62–63; 8:48–49.

In sum, there is agreement that Tanaka discloses the implantation of separate channel dopants. Pet. 42 (claim chart, quoting Ex. 1004, 4:32–34 (Tanaka's disclosure of boron implantation "to form a p type-impurity region as channel doping")); *see id*. (citing Ex. 1003 ¶ 85 (Dr. Maltiel's persuasive explanation of the prior art disclosures)); *compare* Resp. 48–51 (Patent Owner admitting that Tanaka discloses the implantation of separate channel dopants), *with* Reply 17 (explaining why the disputed claim phrase is met by Tanaka even under Patent Owner's construction, which requires separate channel dopants).

Moreover, Petitioner directs us to persuasive evidence that Tanaka teaches an embodiment in which an implanted channel dopant, in fact, spans the length of the channel region from source to drain and beneath the trench. Reply 17–19 (and evidence cited therein, including Tanaka's Figure 1A (annotated) and explanatory textual disclosures (Ex. 1005, 3:59–60, 5:14–20)). Taking account of the parties' respective positions, and in view of a fair reading of the entirety of Tanaka's disclosure, we find that Tanaka teaches a channel region formed as a "contiguous region beneath the bottom surfaces of [a] trench and immediately contiguous to the source and drain regions." Ex. 1001, 7:61–63 (claim 1), 8:47–49 (claim 11, omitting "to").

Accordingly, we determine that Tanaka anticipates independent claims 1 and 11. Pet. 38–46 (claim charts, mapping claims 1 and 11 to disclosures in Tanaka). Further, given that Patent Owner does not challenge Petitioner's persuasive showing that Tanaka discloses the limitations of dependent claims 3 or 13, we determine that Tanaka also anticipates those dependent claims. *Compare* Pet. 43–46 (claim charts, mapping claims 3 and13 to disclosures in Tanaka), *with* Resp. 42–51 (confining counterarguments to features of claims 1 and 11). Further, as explained above, we determine that Tanaka anticipates claims 1, 3, 11, and 13, even under Patent Owner's proposed construction of the disputed claim phrase.

Petitioner also directs us to persuasive evidence that claims 11 and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Tanaka. Pet. 46–47. Here, Petitioner addresses the question whether the preamble of claim 11 is limiting. *Id*. Petitioner explains why the subject matter of claims 11 and 13 would have been obviousness over Tanaka, however, even if we determine that the preamble—which describes "an array of multiple

devices" in which "each device structure" is "spaced from other device structures"—is, in fact, limiting. Ex. 1001, 8:33–36; Pet. 46–47; Ex. 1003 ¶¶ 91–92 (Dr. Maltiel's declaration testimony on that point); Ex. 1005, 6:19–23 (Tanaka, disclosing that "[t]he grooved gate transistor . . . can be assembled in a memory such as DRAM or SRAM" and, further, applied "to a stacked capacitor"). Significantly, Patent Owner does not dispute Petitioner's contention that the preamble of claim 11 is non-limiting. Reply 19–20 n.3 (correctly observing that Patent Owner "does not argue that the preamble of Claim 11 should be considered a limitation").

Patent Owner, in fact, raises no arguments or evidence specifically directed to the ground of unpatentability based on obviousness over Tanaka—with one exception. Resp. 51–57. Patent Owner argues that Tanaka, when discussing a channel region formed by implantation of boron as a separate channel dopant, fails to recite "details of the ion implant" that are sufficient to meet the challenged claims. *Id*. at 55. As an initial matter, that argument is unpersuasive because Patent Owner focuses on details of ion implantation that are not recited in any challenged claim. *Id*. at 51–57. In any event, Tanaka discloses details of boron channel doping that are comparable to those provided in the specification of the '061 patent, which describes boron "implanted in [a] conventional manner to form a channel region." *Compare* Ex. 1005, 4:20–34, *with* Ex. 1001, 5:33–47 (including quoted disclosure); *see* Ex. 1003 ¶ 86 (Dr. Maltiel, explaining Tanaka's disclosure of a boron implanted channel). In our view, on this record, any missing details in Tanaka regarding how to implant boron to form a separately doped channel would have been "conventional" and, thus, fully within the grasp of an ordinarily skilled artisan. Ex. 1001, 5:38.

Tanaka teaches or suggests every limitation of claims 11 and 13, including a region created to accommodate a channel, which may be formed by implanting separate channel dopants. Pet. 42 (claim chart); Resp. 42–51; Reply 16–19. Accordingly, we determine that the subject matter of claims 11 and 13 would have been obvious over the disclosure of Tanaka, regardless of whether we apply the plain and ordinary meaning of the disputed claim phrase resolved above or, alternatively, the narrower construction proposed by Patent Owner.

3. Asserted Grounds Based on Furukawa

Petitioner asserts that claims 1, 3, 11, and 13 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Furukawa. Pet. 7, 47–56. Petitioner also argues that the subject matter of claims 11 and 13 would have been obvious under 35 U.S.C. § 103 in view of Furukawa. *Id.* at 56–57.

The following table provides a summary of Petitioner's mapping of Furukawa to the structural elements of claim 1, to the extent not specifically disputed by Patent Owner in the Response.

Claim 1 structure	**Disclosure in Furukawa cited by Petitioner**
semiconductor transistor	"A MOSFET device and a method of manufacturing the device." (Ex. 1006, at [57], Fig. 3)
semiconductor substrate	substrate 305, which has "a first polarity type" (*id.* at 3:19–20, 3:53–54)
source region	diffusion layer 310, which has "a second polarity type" (*id.* at 3:28–30), with diffusion extension 315 also of a second polarity type (*id.* at 3:33–41, 3:64–4:1)

Claim 1 structure	Disclosure in Furukawa cited by Petitioner
drain region	diffusion layer 320, which has "a second polarity type" (*id.* at 3:28–30), with diffusion extension 325 also of a second polarity type (*id.* at 3:33–41, 3:64–4:1)
Trench	trench 370 in silicon substrate 305 (*id.* at 3:64–4:1, 5:17–18, Fig. 3)
trench-to-gate insulating layer	dielectric layer 330 (*id.* at 3:20–23, 3:53–55, 6:14–17, Fig. 3)
trenched gate electrode	conductor 364 (*id.* at 6:25–27, Fig. 3)

See Pet. 47–53 (citing Ex. 1003 ¶¶ 94–101); *see* Resp. 58–64.

Claim 1 further recites "a channel region formed in the semiconductor substrate, the channel region forming a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions." Regarding that claim feature, Petitioner relies on channel 380 of Furukawa. Pet. 50–51; Ex. 1003 ¶ 99. For example, Petitioner points us to Furukawa's disclosure that "device channel 380 is formed adjacent the bottom of a trench 370 in a substrate 305." Pet. 50 (citing Ex. 1006, 3:12–13, Fig. 3); *see* Ex. 1006, 3:33–41, 3:62–4:1 (Furukawa describing a process for fabricating a channel region that extends contiguously from source to drain and beneath a trench).

Patent Owner, for its part, argues that Furukawa does not disclose a channel region that meets the disputed claim phrase. *See* Resp. 58–64. Here again, however, Patent Owner argues that the claimed "channel region" must be "defined by the presence of" separate channel dopants (*id.* at 61). *See id.* at 58–64; *see also id.* at 62 (first full paragraph, acknowledging Petitioner's evidence relating to the location of the channel region in Furukawa's MOS

transistor, but arguing that such evidence "does not establish that the semiconductor substrate" in Furukawa "is doped separate or in addition to the substrate's general dopant"). Properly construed, the disputed claim phrase does not require a "channel region" defined by the presence of separate channel dopants. Based on the entirety of the information advanced by the parties in this proceeding, we are persuaded that a preponderance of the evidence shows that Furukawa discloses a "channel region formed in the semiconductor substrate" to accommodate a channel created when a voltage is applied to the gate electrode of a MOS transistor. *See, e.g.*, Ex. 1006, 3:12–13, 4:43–53; *see* Pet. 50–51 (including a reproduction of Furukawa's Figure 3, showing a "channel region" (purple annotation) formed in the semiconductor substrate and defined by the placement of the source, drain, gate, and gate oxide); Reply 20 (and evidence cited therein).

Patent Owner's counterview that Furukawa "does not disclose the bounds of the channel or how the channel is formed" is not persuasive. Resp. 58, 61. On that point, Patent Owner contends, "Furukawa does not disclose dopants associated with the channel" and, therefore, an ordinarily skilled artisan would have understood Furukawa's channel region to accommodate "only the induced channel formed during operation of the transistor." *Id.* at 59; *see id.* at 58–62 (for repetitive variations of Patent Owner's argument that the claims require a "channel region" formed by implanting separate channel dopants).

As we explain above, however, the claims encompass, but do not require, a channel region formed by separate channel doping. Petitioner directs us to persuasive evidence that Furukawa discloses a MOS transistor that includes an area formed in the substrate that is designed to

accommodate a channel. Pet. 47, 50–51 (claim chart, including citations to persuasive evidence showing that Furukawa discloses a channel region formed in the substrate, as delineated by the source, drain, gate, and gate oxide, to accommodate a channel). Petitioner need not demonstrate that Furukawa's channel 380 is formed by implanting separate channel dopants, because such dopants are not required by the disputed claim phrase. *See id.*

In addition, a preponderance of the evidence supports Petitioner's view that Furukawa's channel 380 meets the further requirement that the "channel region" must be "a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions." Ex. 1001, 7:61–63 (claim 1), 8:47–49 (claim 11, omitting the word "to"); *see, e.g.*, Ex. 1006, 3:12–18 (explaining that Furukawa's channel 380 is "formed adjacent the bottom of a trench 370" and that "diffusion layers 310, 320 are connected to the edge of the device channel 380 by diffusion extensions 315, 325"); Pet. 50–51; Reply 20. The claims require no additional restrictions on the boundaries of the "channel region." We reproduce below Petitioner's annotated version of Furukawa's Figure 3, which highlights in purple the "channel region formed in the semiconductor substrate" within the meaning of the claims.

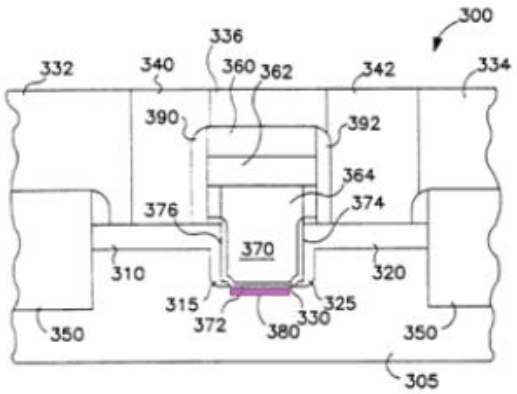


FIG. 3

Pet. 51 (claim chart, mapping the features of claim 1 to disclosures in Furukawa). Figure 3 is "a sectional view illustrating an apparatus according to" Furukawa's invention. Ex. 1006, 2:52–53. Figure 3 identifies "device channel 380" as "formed adjacent the bottom of a trench 370 in a substrate 305." *Id*. at 3:12–13. "[D]iffusion layers 310, 320 and [] diffusion extensions 315, 325" represent "the source region" located "on one side of the trench" and "the drain region" located on "the opposite side of the trench." *Id*. at 3:62–4:5.

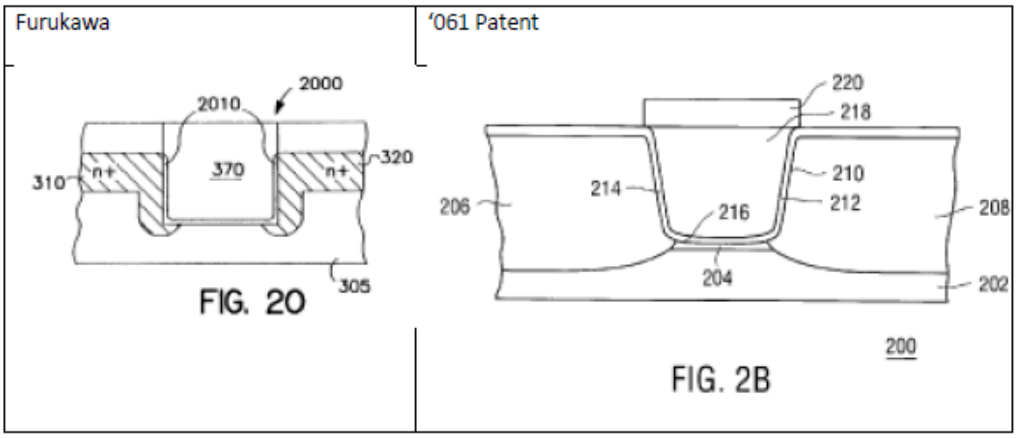
To the extent Patent Owner argues Furukawa does not adequately "disclose the bounds of the channel 380" (Resp. 61), that argument is without merit. *Compare* Ex. 1006, Fig. 3, 3:12–13 (Furukawa disclosing "device channel 380" as "formed adjacent the bottom of a trench 370 in a substrate 305"); *with* Ex. 1001, claims 1 and 11 (independent claims, requiring "a channel region formed in the semiconductor substrate"). First and foremost, Petitioner asserts that Furukawa lacks a feature that is not recited in the challenged claims. *Compare* Pet. 50–51 (providing persuasive evidence that Furukawa's MOS transistor includes a channel region that is both created to accommodate a channel and formed as a contiguous region beneath the bottom surface of a trench and immediately contiguous to source and drain regions), *with* Resp. 58, 61–62 (Patent Owner presenting arguments concerning the "bounds of the channel" that hinge on an overly-narrow view that the claims require a "channel region" defined by separate channel dopants).

Patent Owner's argument, in that regard, is nothing more than an alternative way of expressing its view that the boundaries of the claimed "channel region" must be defined by implantation of separate channel

dopants—a view we reject for reasons stated above in our claim construction section. We agree with Petitioner that the purple box in Petitioner's annotated version of Furukawa's Figure 3 (reproduced above) identifies a "channel region" within the meaning of the challenged claims. Pet. 51. On that point, Furukawa describes, as a separately enumerated step, "forming a device channel under the bottom of the trench." Ex. 1006, 4:43–53.

In the alternative, we determine that, even under Patent Owner's proposed narrower construction of the disputed claim phrase, under which the claimed "channel region" must be formed by implantation of separate channel dopants, Petitioner shows by a preponderance of the evidence that Furukawa anticipates claims 1, 3, 11, and 13. As Petitioner explains, Furukawa teaches an embodiment in which a channel region is formed by implanting separate channel dopants. Reply 20 ("Furukawa discloses implantation (i.e., doping) of the channel region."). Specifically, Petitioner identifies Furukawa's disclosure of a MOS transistor that includes a "gate tailor implant [] made at the bottom of the trench." Reply 20 (quoting Ex. 1006, 6:9–13); *see* Ex. 1006, 7:37–39 (same); *see* Resp. 62–63 (Patent Owner raising Furukawa's "gate tailor implant" as, possibly, supporting an argument that Furukawa "suggest[s] a channel region defined by the presence of" separate channel dopants).

Petitioner further directs us to persuasive evidence that Furukawa discloses a MOS transistor in which "the source and drain regions" are depicted as "wrapping around the corners of the trench in the same fashion shown in the '061 patent." Reply 21–22; *compare* Ex. 1006, Fig. 20, *with* Ex. 1001, Fig. 2B. We reproduce below a comparative illustration advanced by Petitioner in that regard.



Reply 22. The above illustration is a side-by-side comparison of Figure 20 from Furukawa and Figure 2B from the '061 patent. Both figures are a schematic cross-sectional view of a MOS transistor in which the source, drain, and trench bottom directly contact the area where current flows during normal operation of the device.

The above illustration shows persuasively that Furukawa forms a "channel region" as a contiguous region beneath a trench and immediately contiguous to the source and drain regions. Furukawa discloses a "gate tailor implant" formed "at the bottom of the trench." Ex. 1006, 6:5–13, 7:35–39. Furukawa sets forth no additional details regarding the gate tailor implant—a circumstance that suggests to us that the details of selecting and forming the implant were committed by Furukawa to the general knowledge and understanding of an ordinarily skilled artisan. *See id.* That is consistent with disclosure in the '061 patent specification, stating that in a MOS transistor, separate channel dopants may be "implanted in [a] conventional manner to form a channel region." Ex. 1001, 5:33–47.

On that point, significantly, neither Patent Owner nor its witness, Dr. Bottoms, contests that Furukawa's "gate tailor implant" represents a separate channel dopant in Furukawa's MOS transistor. Resp. 62 (citing

Ex. 2006 ¶¶ 118–119). Instead, Dr. Bottoms takes issue with "whether the implanted dopants" represented by Furukawa's "gate tailor implant" would, in fact, be formed "immediately contiguous the drain." Ex. 2006 ¶ 118 (bare opinion testimony that a "sacrificial oxide," which "is not shown" in Furukawa's Figure 7, "is likely to block doping immediately contiguous to the drain"). Dr. Bottoms' opinion depends on "likely" blocking of channel dopant that may occur due to a feature "not shown" in Furukawa's Figure 7. *Id*. That opinion is speculative, unsupported by objective proof, and insufficient to undercut Furukawa's express disclosure that the "gate tailor implant is made at the bottom of the trench." Reply 20 (quoting Ex. 1006, 6:9–13); *see* Ex. 1006, 7:37–39 (Furukawa reiterating that the "gate tailor implant is made at the bottom of the trench"). A preponderance of the evidence, thus, supports a finding that Furukawa teaches the implantation of separate channel dopants beneath the trench, which as illustrated in Figure 20 of Furukawa, spans the length between the source and drain. We are not persuaded that Furukawa lacks "details to identify where the disclosed 'gate tailor implant' would reside within the substrate" or that, given the above express disclosures, an ordinarily skilled artisan "would not necessarily know whether the implanted dopants would be contiguous the source and drain regions." Resp. 62; *see* Reply 20 (citations to express disclosures in Furukawa); 22 (comparison illustration); Ex. 1006, Fig. 20.

Accordingly, we determine that Petitioner demonstrates by a preponderance of evidence that claims 1, 3, 11, and 13 are anticipated by Furukawa, regardless of whether we apply the plain and ordinary meaning of the disputed claim phrase proposed by Petitioner or the narrower construction proposed by Patent Owner.. *See* Pet. 47–56; *see id*. at 50–51

(mapping disputed claim phrase to disclosures in Furukawa); Reply 20 (citing Ex. 1006, 3:12–18, 6:9–13, 7:37–39).

Petitioner directs us to further information that claims 11 and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Furukawa. Pet. 56–57. As it did in connection with Tanaka, Petitioner shows, by reference to express disclosures in the reference and witness testimony backed up by objective proof, that Furukawa suggests "an array of multiple device structures supported on a semiconductor substrate . . ., each device structure spaced from other device structures" as required by claim 11 and inherited by dependent claim 13. *Id*. (citing Ex. 1006, 4:15–22 (referring to the assembly of "adjacent apparatus on a chip" (emphasis omitted)); Ex. 1003 ¶¶ 104–105 (Dr. Maltiel explaining persuasively the import of Furukawa's disclosure).

Patent Owner does not contest that information, except to argue that "Furukawa does not disclose a channel region formed in the substrate." Resp. 63. For reasons set forth above, Patent Owner's argument is not persuasive. Accordingly, we accept Petitioner's view (which is supported by persuasive evidence) that the subject matter of claims 11 and 13 would have been obvious over Furukawa. Pet. 56–57 (and evidence cited therein).

III. CONCLUSION

For the above reasons, we hold that Petitioner establishes by a preponderance of the evidence that claims 1, 3, 4, 11, 13, and 14 of the '061 patent are unpatentable.

IV. ORDER

It is

ORDERED that claims 1, 3, 4, 11, 13, and 14 of the '061 patent are unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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