UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.
Patent Owner.

Case IPR. No. 2018-01005
U.S. Patent No. 7,171,526 B1

Before MICHAEL R. ZECHER, GARTH D. BAER, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), Patent Owner North Star Innovations, Inc. ("North Star" or "Patent Owner") hereby respectfully gives notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Patent Trial and Appeal Board's ("Board") Final Written Decision entered on October 24, 2019 (Paper No. 34), as well as from all other underlying orders, decisions, rulings, and opinions that are adverse to Patent Owner regarding U.S. Patent No. 7,171,526 in IPR 2018-01005.

For the limited purpose of providing the Director with the information requested in 37 C.F.R. § 90.2(a)(3)(ii), the issues on Patent Owner's appeal may include, but are not limited to:

(1) the Board's determination of unpatentability of Claims 15-19;

(2) any and all findings or determinations supporting or related to the aforementioned issues, as well as other issues decided adversely to Patent Owner in any orders, decisions, rulings, or opinions; and

(3) the unconstitutional appointment of the panel of administrative patent judges under the appointments clause. See *Arthrex, Inc., v. Smith & Nephew, Inc., Arthrocare Corp.*, Case No. 2018-2140 (Fed. Cir. Oct. 31, 2019).

Simultaneous with this submission, a copy of the Notice of Appeal is being filed electronically with the Patent Trial and Appeal Board. In addition, a copy of

this Notice of Appeal, along with the required docketing fees, is being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Dated: December 23, 2019

Respectfully Submitted,

/s/ Philip E. Levy
Philip E. Levy (PA ID # 73605)
Reg. No. 40,700
Eckert Seamans Cherin & Mellott, LLC
600 Grant Street, 44th Floor
Pittsburgh, PA 15219
plevy@eckertseamans.com
Tel: 412.566.6000
Fax: 412.566.6099
Customer No. 03705

Counsel for North Star Innovations, Inc.

Certificate of Service

I hereby certify that, in addition to being electronically filed through the Board's E2E System, a true and correct copy of the Patent Owner's Notice of Appeal was mailed via United States Postal Service Priority Express Mail on December 23, 2019 to the Director of the United States Patent and Trademark Office at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
PO Box 1450
Alexandria, VA 22313-1450

I hereby certify that on December 23, 2019, a true and correct copy of the foregoing Patent Owner's Notice of Appeal, and the filing fee, were filed with the Clerk's Office of the United States Court of Appeals for the Federal Circuit, via CM/ECF.

I also hereby certify that a true and correct copy of the foregoing Patent Owner's Notice of Appeal was served by electronic mail on December 23, 2019 to the Petitioner by serving Petitioner's counsel of record at the e-mail address set forth below for IPR2018-01005.

Attorney of Record

Jeremy Jason Lang
Jared Bobrow
Orrick, Herrington & Sutcliffe, LLP
1000 Marsh Road
Menlo Park, CA 94025
Tel: 650.614.7400
Fax: 650.614.7401
PTABDocketJJL2@orrick.com
PTABDocketJ3B3@orrick.com
Micron-NorthStar_OHS@orrick.com

Christopher J. Siebens
Orrick, Herrington & Sutcliffe, LLP
Columbia Center
1152 15th Street, N.W.
Washington, D.C. 20005
Tel: 202.339.8400
Fax: 202.339.8500
29CPTABDocket@orrick.com

K. Patrick Herman
Orrick, Herrington & Sutcliffe, LLP
51 West 52nd Street
New York, NY 10019
Tel: 212.506.5000
Fax: 212.506.5151
P52PTABDocket@orrick.com

Respectfully Submitted,
Eckert Seamans Cherin & Mellott, LLC

/s/ Philip E. Levy
Philip E. Levy
PA ID No. 73605
Reg. No. 40,700
600 Grant Street, 44th Floor

Pittsburgh, PA 15219
plevy@eckertseamans.com
Tel: 412.566.6000
Fax: 412.566.6099

EXHIBIT 1

Trials@uspto.gov
571-272-7822

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS INC.,
Patent Owner.

IPR2018-01005
Patent 7,171,526 B2

Before MICHAEL R. ZECHER, GARTH D. BAER, and STEVEN M. AMUNDSON, *Administrative Patent Judges.*

BAER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Petitioner Micron Technology, Inc., filed a Petition (Paper 1, "Pet.")[1] requesting *inter partes* review of claims 15–19 of U.S. Patent No. 7,171,526 B2 (Ex. 1001, "the '526 patent"). Pursuant to 35 U.S.C. § 314(a), we determined Petitioner showed a reasonable likelihood that it would prevail in establishing the unpatentability of all challenged claims and instituted an *inter partes* review. Paper 11, 15. Patent Owner, North Star Innovations Inc., filed a Response (Paper 19, "PO Resp."), and Petitioner filed a Reply to Patent Owner's Response (Paper 27, "Pet. Reply"). Patent Owner then filed a Sur-reply to Petitioner's Reply. Paper 30 ("Sur-reply"). An oral hearing was held before the Board. Paper 33 ("Tr.").

We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. Having considered the record before us, and as explained below, we determine Petitioner has shown by a preponderance of the evidence that claims 15–19 of the '526 patent are unpatentable. *See* 35 U.S.C. § 316(e).

A. RELATED PROCEEDINGS

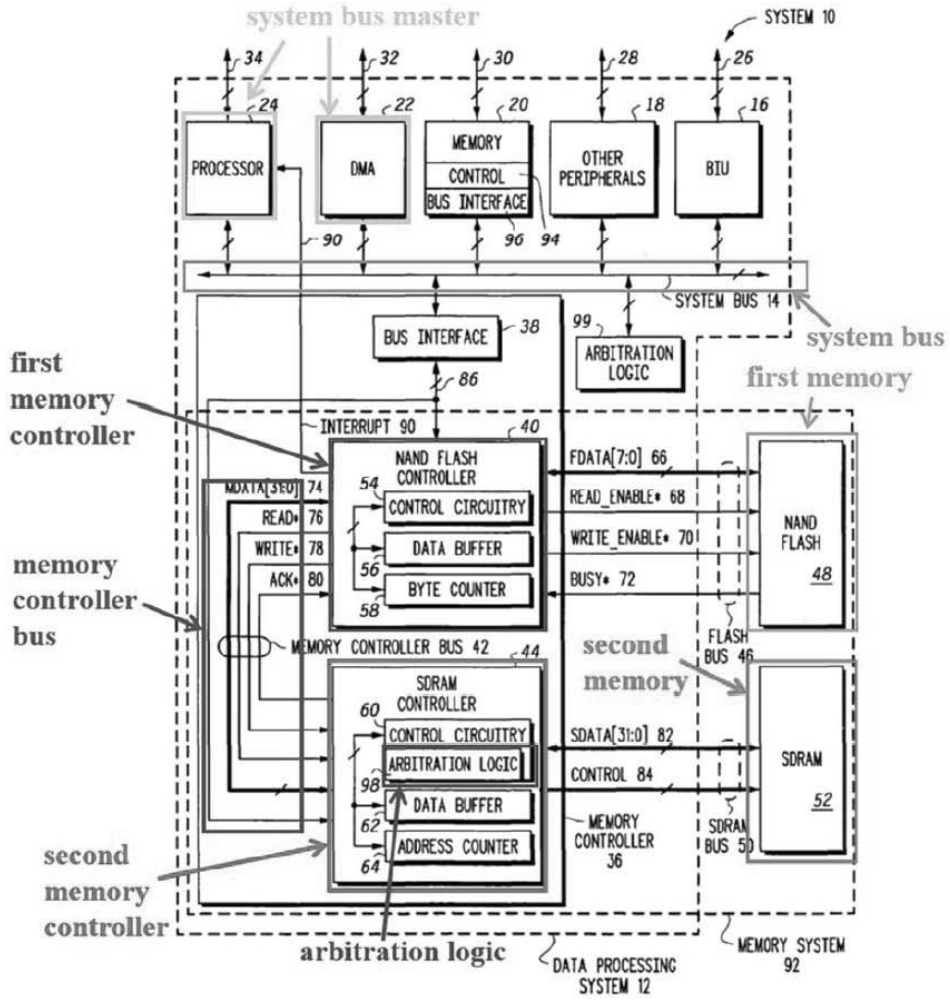
As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 2–3; Paper 5, 1.

B. THE '526 PATENT

The '526 patent relates to a memory controller useable in a data processing system. Ex. 1001, 1:6–8. It describes a data processing system

[1] Petitioner filed redacted and un-redacted versions of the Petition (Papers 1 and 2), along with a Motion to Seal and a request to enter a Default Protective Order (Paper 4). Throughout this Decision, we only refer to the redacted version of the Petition (Paper 1).

using an independent memory controller bus that enables efficient data transfer between two memories, thus eliminating the need for DMA (Direct Memory Access) when transferring between two memories. *Id.* at [57], 2:29–39. Figure 1 of the '526 patent is reproduced below, with colored annotations added by Petitioner identifying various components required by the challenged claims. Pet. 11.



Ex. 1001, Fig. 1 (with annotations)

FIG. 1 illustrates, in block diagram form, a system 10 in accordance with one embodiment of the present invention. System 10 includes a data processing system 12, a NAND [Not And] Flash 48, and a synchronous dynamic random access

> memory (SDRAM) 52. Data processing system 12 includes a processor 24, a DMA 22, a memory 20, other peripherals 18, a memory controller 36, arbitration logic 99, and a bus interface unit (BIU) 16, each bidirectionally coupled to a system bus 14. Processor 24, DMA 22, memory 20, other peripherals 18, and BIU 16 are coupled to bidirectional data processing system terminals 34, 32, 30, 28, and 26, respectively, so that they may communicate to circuitry external to data processing system 12.

Ex. 1001, 2:40–52.

DMA 22 transfers data to and from memories coupled to system bus 14, such as memory 20. *Id.* at 3:10–12. DMA 22, however, does not perform data transfers between NAND Flash 48 and SDRAM 52. *Id.* at 3:12–17. Instead, data transfers are controlled by memory controller 36, which includes NAND Flash controller 40, SDRAM controller 44, and memory controller bus 42. *Id.* at 3:17–18, 4:48–50.

Data is transferred between the two memory controllers via memory controller bus 42 in a manner that is independent of system bus 14. Also, the data transfer operations between the two memories are performed within memory controller 36, and are distributed between the two memory controllers. Thus, a separate DMA unit is not needed for the two memories and, as a result, less circuitry is required as compared to using a full-fledged DMA unit (e.g., DMA 22). *Id.* at 4:50–5:3.

The '526 patent also describes using SDRAM 52 as a cache for transferring data out of NAND Flash 48. Specifically, data retrieved from NAND Flash 48 is first transferred into SDRAM 52, after which processor 24 can read the data from SDRAM 52. *Id.* at 4:40–47. The '526 patent further describes that both processor 24 and NAND Flash controller 40 may request data transfers to and/or from SDRAM 52 at the same time. In such a scenario, arbitration logic 98 within SDRAM controller 44 arbitrates

between processor 24 and NAND Flash controller 40 for access to SDRAM 52. *Id*. at 5:4–22.

C. Illustrative Claim

Of the challenged claims, claims 15 and 19 are independent. Independent claim 15 is illustrative of the claimed subject matter and is reproduced below.

> 15. A data processing system, comprising:
>
> a system bus;
>
> a system bus master, coupled to the system bus;
>
> a first memory controller, coupled to the system bus, for controlling a first memory;
>
> a second memory controller, coupled to the system bus, for controlling a second memory;
>
> arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory; and
>
> a memory controller bus operating independent of the system bus, said memory controller bus being coupled to the first memory controller and to the second memory controller, said memory controller bus transferring data between the first memory controller and the second memory controller.

Id. at 12:45–62.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Claims Challenged	35 U.S.C. §	Reference(s)
15, 17, and 18	103(a)	Callison[2]
16 and 19	103(a)	Callison and Shanley[3]

Pet. 3–4.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art at the time of the '526 patent would have had "at least a Bachelor of Science or Engineering degree in computer science, computer engineering, electrical engineering, or a closely related field, along with at least 5 years of experience in the field of computer systems and computer memory." Pet. 19. In addition, according to Petitioner, "[a]n individual with an advanced degree in the above fields would require less (*e.g.*, by 1 to 2 years) experience in the field of computer systems and computer memory." *Id.* (citing Ex. 1003 ¶¶ 31–33). Patent Owner does not provide its own formulation of a person of ordinary skill or contest Petitioner's assertion. PO Resp. 34. We agree with and adopt Petitioner's proposal because it is consistent with the '526 patent, as well as the problems and solutions in the prior art of record. *See Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

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[2] U.S. Patent No. 5,737,744 (issued Apr. 7, 1998) (Ex. 1005, "Callison").
[3] Tom Shanley & Don Anderson, *EISA System Architecture*, 2–6, 9–21, 24–31, 117–21, 123–32 (2d ed. 1995) (Ex. 1007, "Shanley").

B. Claim Construction

1. *Applicable Standard*

In an *inter partes* review based on a petition filed before November 13, 2018, we interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b) (2017).[4] We presume a claim term carries its "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question" at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

2. *"memory controller bus operating independent of the system bus"*

Independent claims 15 and 19 require a "memory controller bus operating independent of the system bus." Petitioner proposes we construe this term to mean "a bus for transferring data between two or more memory controllers where said data transfer does not use the system bus." Pet. 19. As Petitioner explains, the specification and claims support Petitioner's construction. *See id.* at 18 (citing Ex. 1001, [57], 2:29–33, 11:42–47). Patent Owner does not challenge Petitioner's construction. For the reasons stated in the Petition, we agree with Petitioner and construe "memory controller bus operating independent of the system bus" as "a bus for

[4] A recent amendment to this rule does not apply here because the Petition was filed before November 13, 2018. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (codified at 37 C.F.R. pt. 42 (2019)) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018).

transferring data between two or more memory controllers where said data transfer does not use the system bus."

3. *"arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory"*

Independent claim 15 requires "the second memory controller comprises arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory." Independent claim 19 has a similar limitation. Although neither party proposes an explicit construction for this arbitration limitation, the parties' dispute centers on Patent Owner's implicit construction. Specifically, Patent Owner's argument that the asserted prior art fails to teach the arbitration limitation is premised on "access to the second memory" precluding indirect access to the second memory using intermediary components. *See* PO Resp. 40 (arguing that the asserted prior art does not teach the arbitration limitation because "disk read and write operations, including the transfer of data from host computer 101 to disk controller board 10, are managed by and carried out by disk controller board 10" rather than the host computer itself); *id.* at 42 (arguing that "[a]lthough data from host computer 101 is written to DRAM 116, it is PCI bus master 126, not host computer 101, that actually writes the data to DRAM 116"); *id.* at 43 (arguing that in the prior art, "all access to DRAM 116 must be made through components within DRAM interface 118" rather than directly); 44 (arguing that in the prior art, "it is bus slave write FIFO 132, not SCSI controllers 112A-E that has the capability to access and write to DRAM 116"). We disagree with Patent Owner's construction for three reasons.

First, Patent Owner's construction reads in a limitation requiring *direct* access from the system bus master and first memory controller to the

second memory controller. The claim element at issue, however, requires only "arbitration logic arbitrating/performing arbitration between the system bus master and the first memory controller for access to the second memory." Although the claim's plain language requires that the system bus master and the first memory controller must be the origin of the arbitrated requests, nothing in the claim's plain language precludes access using intermediary components.

Second, other claim limitations undermine Patent Owner's construction. In addition to the arbitration limitation, claim 15 recites "transferring data between the first memory controller and the second memory controller." Claim 19 recites a similar limitation: "transferring data between the first memory and second memory by way of the first memory controller and the second memory controller." These limitations suggest that access from the first memory controller to the second memory will not be direct, but will use the second memory controller as an intermediary.

Last, the '526 patent's specification undermines Patent Owner's direct-access argument because it includes embodiments in which the system bus master and first memory controller access the second memory using intermediary components. As Petitioner's expert, Pinaki Muzumder, Ph.D., notes, when the '526 patent's system bus master accesses the second memory, it does so indirectly, through an intermediary bus interface and through a second memory controller. Ex. 1040 ¶ 16 (citing Ex. 1001, 4:43–47, 8:41–47). Similarly, the specification describes the first memory controller accessing the second memory through an intermediary data buffer within the second memory controller (i.e., data buffer 62 in Figure 1). *Id.*

¶ 17 (citing Ex. 1001, 8:23–26); *see* Ex. 1001, Fig. 1. Absent in the specification is any embodiment in which the system bus master or first memory controller accesses the second memory without involving intermediary components. Ex. 1040 ¶ 19. We decline to read into the claims a direct-access requirement that would exclude every specification embodiment. *See Nellcor Puritan Bennett, Inc. v. Masimo Corp.*, 402 F.3d 1364, 1368 (Fed. Cir. 2005) ("[A] construction that excludes all of the embodiments of an invention is rarely, if ever, correct." (internal quotation marks omitted)).[5]

C. ASSERTED PRIOR ART

1. Callison (Ex. 1005)

Callison relates to a memory controller useable in a data processing system and, more particularly, a disk controller used in a computer system. Ex. 1005, 1:8–12, 2:22–25. Callison's system includes a host computer and a disk controller board, where the disk controller board controls accesses to a group of hard disk drives from the host computer. *Id.* at 4:9–11, 30:11–12, Fig. 1.

Callison's Figure 1 is reproduced below, with colored annotations added identifying various components that Petitioner asserts correspond to claim 15's limitations. Pet. 21.

[5] In its Sur-reply, Patent Owner appears to shift its argument by asserting that, unlike in Callison, in the challenged patent, "[b]y the time data is sent to those intermediate components, however, arbitration logic 98 has already arbitrated between processor 24 and NAND flash controller 40." Sur-reply 16. We disagree with Patent Owner's argument because the claim language does not restrict sequencing of arbitration and data flow. Rather, it simply requires arbitration between two end points for access to memory. The claim is agnostic to whether data flow begins before arbitration.

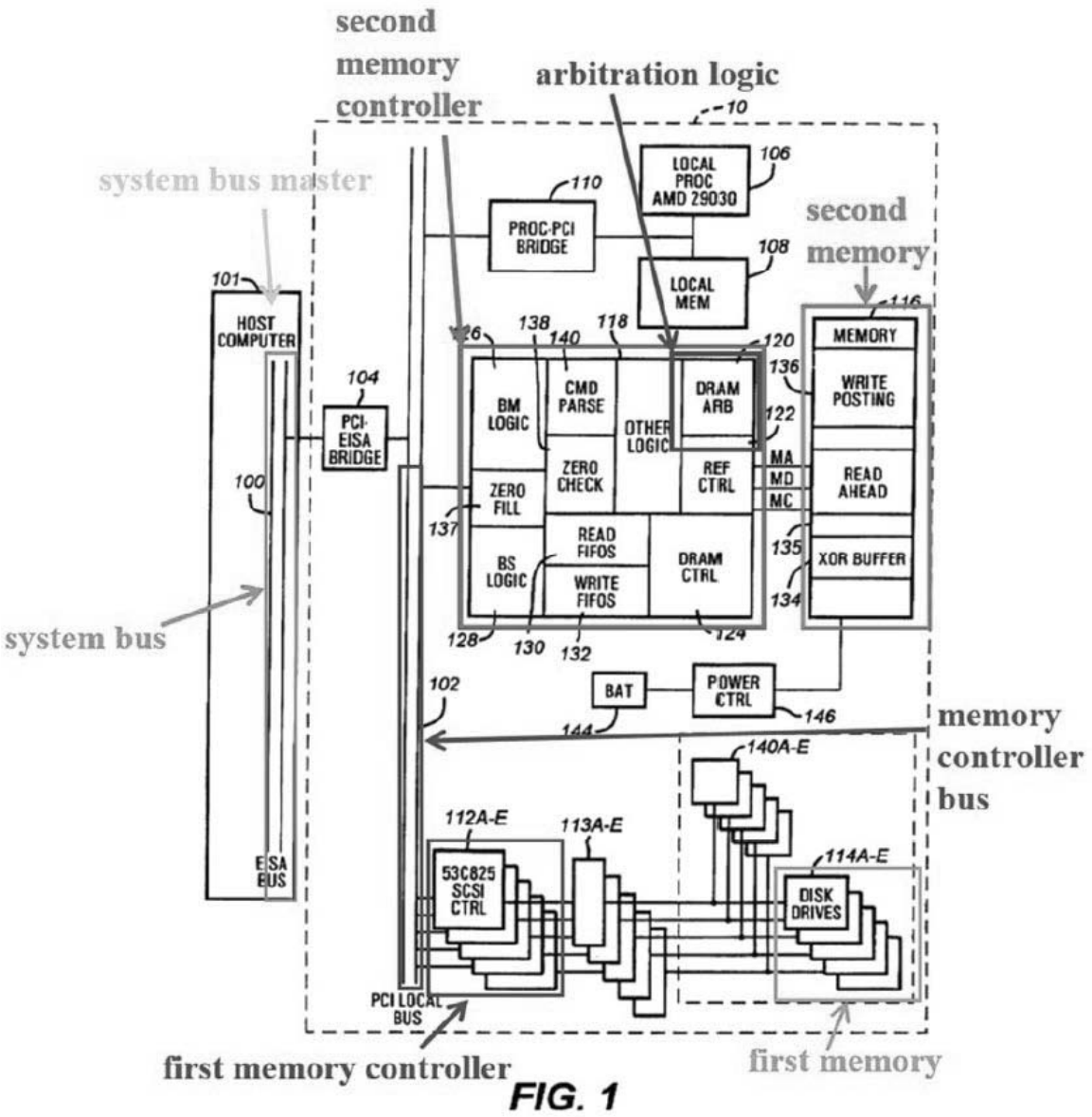

FIG. 1

Figure 1 "is a block diagram of a disk controller board." Ex. 1005, 2:66–67. As shown in Figure 1, Callison's computer system includes host computer 101 and disk controller board 10. Host computer 101 includes Extended Industry Standard Architecture (EISA) bus 100 that provides the communications channel to other components within host computer 101. *Id.* at 3:22–26. Disk controller board 10 includes a group of small computer system interface (SCSI) controllers 112A–E for controlling a group of hard

disk drives 114A–E, Dynamic Random-Access Memory (DRAM) interface 118 for controlling DRAM 116, and peripheral component interconnect (PCI) local bus 102, which connects the two memory controllers. *Id*. at 4:9–14, 5:9–10, 6:22–26, Fig. 1.

Callison's DRAM 116 is used as a cache (e.g., a posted write buffer, a read ahead cache) when data is transferred between host computer 101 and hard disk drives 114A–E. For example, when host computer 101 writes data to hard disk drives 114A–E, data is first transferred from a system memory of host computer system 101 to DRAM 116, and then transferred from DRAM 116 to hard disk drives 114A–E. *Id*. at 1:59–2:2, 2:32–34, 4:36–63, 5:33–37, 31:58–61. Callison describes that such a method improves overall system performance because the access time of DRAM 116 is much better than that of hard disk drives 114A–E. *Id*. at 2:2–4, 4:56–59.

In using DRAM 116 as a cache for data transfers between host computer 101 and hard disk drives 114A–E, Callison discloses that DRAM interface 118 includes DRAM arbiter 120 for arbitrating between host computer 101 and SCSI controllers 112A–E for access to DRAM 116. *Id*. at 6:28–30, 6:52–53.

2. Shanley (Ex. 1007)

Petitioner relies on Shanley for its teaching that an EISA system includes one or multiple bus masters for the EISA bus, such as a main CPU and DMA controller. Ex. 1007, 28–31.[6]

[6] All references to the page numbers in Shanley refer to the original page numbers in the bottom, right-hand or left-hand corner of each page in Exhibit 1007.

D. Asserted Grounds

Petitioner relies primarily on Callison's computer system to show the claimed data processing system. *See* Pet. 26–55. Petitioner reads the '526 patent's claimed system bus onto Callison's EISA bus, the claimed first memory onto Callison's hard disk drives, and the claimed second memory onto Callison's DRAM. *See id.* Petitioner further identifies Callison's SCSI controllers as the claimed first memory controller and Callison's DRAM controller as the claimed second memory controller. *Id.* at 32–37, 49–54. Petitioner relies on Shanley only to teach specific dependent claims' features. *Id.* at 45–48.

Patent Owner disputes a single limitation. According to Patent Owner, Callison does not teach "'arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory,' as is recited in claim 15 of the '526 patent," and similarly recited in claim 19 of the '526 patent. PO Resp. 35; *see id.* at 35–50.

For the reasons explained below, we disagree with Patent Owner and conclude that Petitioner has shown by a preponderance of evidence that claims 15–19 would have been obvious over the asserted prior art.

1. Obviousness of Claims 15, 17, and 18 Based on Callison

a. Claim 15

i. Undisputed Preamble, Bus, and Memory Elements

The preamble of claim 15 recites "[a] data processing system." Petitioner identifies Callison's computer system where a disk array controller performs disk read and disk write operations on disk memories as "[a] data processing system." Pet. 26–37. For the recited "system bus,"

Petitioner identifies Callison's "EISA bus 100," which "includes at least a system data bus and a system address bus." *Id*. at 28. Patent Owner does not dispute these teachings. We agree with Petitioner that Callison discloses a "data processing system" and "system bus."

Petitioner contends Callison discloses the recited "system bus master, coupled to the system bus" because Callison's host computer writes data to hard disk drives and functions as a bus master to perform these write operations. *Id*. at 30. According to Petitioner, "when [Callison's] host computer 101 writes data to hard disk drives 114A–E, host computer 101 controls data transfer on EISA bus 100, and thus is a system bus master." *Id*. at 30–31. Petitioner contends further that, to the extent that Callison does not expressly disclose a specific device in host computer 101 that serves as the bus master, a person of ordinary skill in the art "would have understood that host computer 101 would necessarily include a device, such as a processor or DMA, which is coupled to EISA bus 100 to control the operations of the bus." *Id*. at 32 (citing Ex. 1007, 28–31, Fig. 2-1). Patent Owner does not dispute Petitioner's assertions in these regards. We agree with Petitioner that Callison teaches a "system bus master, coupled to the system bus."

Petitioner identifies Callison's SCSI controllers 112A–E for controlling hard disk drives 114A–E as the claimed "first memory controller, coupled to the system bus, for controlling a first memory." *Id*. at 33–34. Petitioner identifies Callison's DRAM interface 118, which includes DRAM controller 124 for controlling DRAM 116, as the claimed "second memory controller, coupled to the system bus, for controlling a second memory." *Id*.

at 35–37. We agree with Petitioner that Callison teaches the claimed first memory controller and second memory controller, as recited in claim 15.

Petitioner identifies Callison's PCI local bus 102 coupled to SCSI controllers 112A–E and DRAM interface 118 as the claimed "memory controller bus operating independent of the system bus, said memory controller bus being coupled to the first memory controller and to the second memory controller, said memory controller bus transferring data between the first memory controller and the second memory controller." *Id*. at 41–43. Petitioner notes that in Callison, PCI local bus 102 operates independent of EISA bus 100 (system bus) because, "as shown in [Figure] 1, when data is transferred between SCSI controllers 112A–E ('first memory controller') and DRAM interface 118 ('second memory controller'), data is transferred exclusively on PCI local bus 102 ('memory controller bus')" and "such a data transfer does not use EISA . . . bus 100." *Id*. at 43. Patent Owner does not dispute Petitioner's assertions in these regards. We agree with Petitioner that Callison teaches the claimed memory controller bus, as recited in claim 15.

ii. Disputed Arbitration Logic Element

Claim 15 further requires "arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory." Petitioner explains that Callison teaches this limitation because Callison's host computer 101 (system bus master) and SCSI controllers 112A–E (first memory controller) both access DRAM 116 (second memory). *Id*. at 38–41 (citing Ex. 1005, 2:32–34, 5:35–37, 4:36–51, 6:59–67, 10:4–20, 31:58–61; Ex. 1003, A20–A22). In addition, as Petitioner notes, Callison teaches that

DRAM arbiter 120 (arbitration logic) "arbitrates 'all requests' to access DRAM 116." *Id*. at 40 (citing Ex. 1005, 6:29–31, 6:52–53, 7:39–48). "Thus," Petitioner concludes, "DRAM arbiter 120 ('arbitration logic') arbitrates between host computer 101 ('system bus master') and SCSI controllers 112A-E ('first memory controller') for access to DRAM 116 ('second memory')." *Id*. We agree with Petitioner that Callison teaches the claimed "arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory."

Patent Owner argues that Callison is deficient because its system bus master and first memory controller do not access the second memory directly, but instead do so through intermediary components. *See* PO Resp. 40, 42, 43. According to Patent Owner, because all access to Callison's DRAM must go through the DRAM interface, DRAM arbiter 120 arbitrates only requests from requestors in DRAM interface 118 (second memory controller), rather than requests from the system bus master and the first memory controller. *See id*. at 38 (citing Ex. 1005, 6:28–30). Patent Owner's argument is premised largely on its arbitration logic claim construction, which we decline to adopt for the reasons explained above.

Patent Owner repeatedly cites Callison's teaching that "DRAM arbiter 120 . . . arbitrates requests for the DRAM 116 from the various possible requestors in the DRAM interface 118." Ex. 1005, 6:28–30; *see* PO Resp. 25 (quoting Ex. 1005, 6:28–30); *id*. at 38 (same); *id*. at 46 (same); Sur-reply 2 (same); *id*. at 6 (same); *id*. at 7 (same). But the requests and data that access Callison's DRAM 116 (second memory) do not originate within DRAM interface 118 (second memory controller). Rather, they originate

from host computer 101 (system bus master) and SCSI controllers 112A–E (first memory controllers), as the disputed limitation requires. *See* Ex. 1005, 2:32–34, 5:35–37, 4:36–51, 6:59–67, 10:4–20. In other words, Callison's host computer 101 and SCSI controllers 112A–E access DRAM 116 even if they use intermediary components in the process to do so.

Patent Owner does not dispute Callison teaches host computer 101 (system bus master) initiates write operations to DRAM 116 (second memory) in which data is written from host computer 101 (system bus master) to DRAM 116 (second memory). *See* PO Resp. 40–41, 42; Sur-reply 9–10; Tr. 30:22–23. Patent Owner also does not dispute Callison discloses moving data from SCSI controllers 112A–E (first memory controllers) to DRAM 116 (second memory). *See* PO Resp. 44; Sur-reply 13–14. Because Callison further teaches "the DRAM arbiter 120 [arbitration logic] controls all requests to the DRAM 116 [second memory]," Ex. 1005, 6:52–53, we agree with Petitioner that Callison discloses "arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory."

b. Claim 17

Claim 17 depends from claim 15 and recites "wherein the first memory type comprises block accessible memory." Petitioner explains, with relevant support from the prior art and its expert, Dr. Mazumder, that Callison's hard disk drives include block accessible memory. *See* Pet. 44 (citing Ex. 1008, 1 (describing "block-access memory devices like hard disks"); Ex. 1003, A29, G4). Patent Owner does not dispute Petitioner's

assertion in this regard. We find Callison teaches "the first memory type comprises block accessible memory."

c. Claim 18

Claim 18 depends from claim 15 and recites "wherein the second memory comprises random accessible memory." Petitioner, with relevant support from its expert, explains that Callison's DRAM (Dynamic Random-Access Memory) by definition includes random accessible memory. *Id*. at 45 (citing Ex. 1003, G4, A29). Patent Owner does not dispute Petitioner's assertion in this regard. We find Callison teaches "the second memory comprises random accessible memory."

2. Obviousness of Claims 16 and 19 Based on Callison and Shanley

a. Claim 16

Claim 16 depends from claim 15 and recites "direct memory access (DMA) circuitry coupled to the system bus" and "a processor coupled to the system bus." Petitioner explains that, "[t]o the extent that Callison does not expressly disclose any DMA circuitry coupled to EISA bus 100 ('system bus'), Shanley discloses a DMA controller ('DMA circuitry') that is coupled to an EISA bus (*e.g.*, EISA bus 100 in Callison, 'system bus')." *Id*. at 45–46. Petitioner further explains, "[t]o the extent that Callison does not expressly disclose a processor coupled to EISA bus 100 ('system bus'), Shanley discloses that a microprocessor or host CPU ('processor') is coupled to an EISA bus (*e.g.*, EISA bus 100 in Callison), as shown in Figure 2-1." *Id*. at 47 (citing Ex. 1007, 28–31).

Petitioner asserts that it would have been obvious to one skilled in the art to include Shanley's DMA circuitry coupled to the system bus because "Callison . . . does not provide extensive detail on how to implement an EISA bus and associated components," whereas "Shanley provides that

detailed information, that is, the architecture of an EISA system that includes an EISA bus and other associated components in a computer system." *Id.* at 55. Petitioner explains further that one skilled in the art would also have been motivated to use Shanley's EISA system (including DMA circuitry) for Callison's host computer to achieve the benefits Shanley describes, including "parallel processing," which is "extremely efficient" and "a low-cost alternative to intelligent bus master cards." *Id.* at 56 (quoting Ex. 1007, 22, 29).

Patent Owner does not separately contest Callison's and Shanley's teachings related to claim 16. We agree with Petitioner that Shanley teaches both "direct memory access (DMA) circuitry coupled to the system bus" and "a processor coupled to the system bus." In addition, Petitioner has articulated persuasive reasoning with rational underpinning that supports the legal conclusion that its proffered combination—i.e., adapting Callison's host computer in view of Shanley's teachings on EISA systems—would have been obvious to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

b. Claim 19

Independent claim 19 largely parallels the limitations in claims 15 and 16. Claim 19 further recites "system bus arbitration logic, coupled to the system bus, said system bus arbitration logic performing arbitration on the system bus." Petitioner explains that, although "Callison discloses host computer 101 that includes EISA bus 100 ('system bus')," it "does not expressly disclose any arbitration logic that performs arbitration on EISA bus 100." Pet. 49–50. To account for Callison's deficiency, Petitioner explains Shanley "discloses Central Arbitration Control . . . that is coupled

to an EISA bus and performs arbitration on the EISA bus." *Id*. at 50. As explained above, Petitioner asserts one skilled in the art would have been motivated to include Shanley's Central Arbitration Control (CAC) in Callison's EISA bus 100 because Shanley provides implementation details missing in Callison and to achieve the benefits (e.g., parallel processing) described in Shanley. *Id*. at 55–57.

Patent Owner does not separately contest Callison's and Shanley's teachings related to claim 19. We agree with Petitioner that Shanley teaches "system bus arbitration logic, coupled to the system bus, said system bus arbitration logic performing arbitration on the system bus." In addition, Petitioner has articulated persuasive reasoning with rational underpinning that supports the legal conclusion that its proffered combination of Callison and Shanley would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 418.

III. CONCLUSION

As indicated in the table below, Petitioner has shown by a preponderance of the evidence that claims 15–19 are unpatentable over the asserted prior art.[7]

[7] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s)	Claims Shown Unpatentable	Claims Not Shown Unpatentable
15, 17, and 18	103(a)	Callison	15, 17, and 18	None
16 and 19	103(a)	Callison and Shanley	16 and 19	None
Overall Outcome			15–19	

Certain documents have been sealed in this proceeding, but have not been relied upon in this Final Written Decision. *See* Paper 13. The record will be maintained undisturbed pending the outcome of any appeal taken from this decision. At the conclusion of any appeal proceeding, or if no appeal is taken, the documents may be made public. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,760–61 (Aug. 14, 2012). Either party may file a motion to expunge the sealed documents from the record pursuant to 37 C.F.R. § 42.56. Any such motion will be decided after the conclusion of any appeal proceeding or the expiration of the time period for appealing.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown by a preponderance of the evidence that claims 15–19 of the '526 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Jeremy Jason Lang
WEIL, GOTSHAL & MANGES LLP
jason.lang@weil.com

PATENT OWNER:

Philip E. Levy
Robert W. Morris
ECKERT SEAMANS CHERIN & MELLOTT, LLC
plevy@eckertseamans.com
rwmorris@eckertseamans.com