UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.
Patent Owner.

Case IPR. No. 2018-00998
U.S. Patent No. 6,127,875

Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and STEVEN M. AMUNDSON, *Administrative Patent Judges*.

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a), Patent Owner North Star Innovations, Inc. ("North Star" or "Patent Owner") hereby respectfully gives notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Patent Trial and Appeal Board's ("Board") Final Written Decision entered on October 22, 2019 (Paper No. 29), as well as from all other underlying orders, decisions, rulings, and opinions that are adverse to Patent Owner regarding U.S. Patent No. 6,127,875 in IPR 2018-00998.

For the limited purpose of providing the Director with the information requested in 37 C.F.R. § 90.2(a)(3)(ii), the issues on Patent Owner's appeal may include, but are not limited to:

(1) the Board's determination of unpatentability of Claims 1-3;

(2) any and all findings or determinations supporting or related to the aforementioned issues, as well as other issues decided adversely to Patent Owner in any orders, decisions, rulings, or opinions; and

(3) the unconstitutional appointment of the panel of administrative patent judges under the appointments clause. See *Arthrex, Inc., v. Smith & Nephew, Inc., Arthrocare Corp.*, Case No. 2018-2140 (Fed. Cir. Oct. 31, 2019).

Simultaneous with this submission, a copy of the Notice of Appeal is being filed electronically with the Patent Trial and Appeal Board. In addition, a copy of

this Notice of Appeal, along with the required docketing fees, is being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit.

Dated: December 23, 2019

Respectfully Submitted,

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Certificate of Service

I hereby certify that, in addition to being electronically filed through the Board's E2E System, a true and correct copy of the Patent Owner's Notice of Appeal was mailed via United States Postal Service Priority Express Mail on December 23, 2019 to the Director of the United States Patent and Trademark Office at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel
PO Box 1450
Alexandria, VA 22313-1450

I hereby certify that on December 23, 2019, a true and correct copy of the foregoing Patent Owner's Notice of Appeal, and the filing fee, were filed with the Clerk's Office of the United States Court of Appeals for the Federal Circuit, via CM/ECF.

I also hereby certify that a true and correct copy of the foregoing Patent Owner's Notice of Appeal was served by electronic mail on December 23, 2019 to the Petitioner by serving Petitioner's counsel of record at the e-mail address set forth below for IPR2018-00998.

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EXHIBIT 1

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
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v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

IPR2018-00998
Patent 6,127,875

Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and STEVEN M. AMUNDSON, *Administrative Patent Judges*.

WORMMEESTER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting *inter partes* review of claims 1–3 of U.S. Patent No. 6,127,875 (Ex. 1001, "the '875 patent"). North Star Innovations, Inc. ("Patent Owner") did not file a Preliminary Response. *See* Paper 7 (Waiver of Patent Owner's Preliminary Response). Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of challenged claims 1–3 based on the sole ground presented in the Petition. Paper 9 ("Inst. Dec."). Patent Owner filed a Response (Paper 16, "PO Resp."), and Petitioner filed a Reply (Paper 23, "Pet. Reply"). Patent Owner subsequently filed a Sur-Reply (Paper 25, "PO Sur-Reply").

On July 17, 2019, we conducted an oral hearing. A copy of the transcript (Paper 28, "Tr.") is included in the record.

We have jurisdiction under 35 U.S.C. § 6(b). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–3 of the '875 patent are unpatentable. This final written decision is issued pursuant to 35 U.S.C. § 318(a).

II. BACKGROUND

A. Related Proceedings

The parties identify two related district court cases. Pet. 2–3; Paper 4, 1. The parties also identify several related petitions for *inter partes* review. Pet. 3; Paper 4, 1.

B. The '875 Patent

The '875 patent describes a voltage-boosting circuit, which provides an output voltage that is greater than the supplied input voltage. Ex. 1001, 1:5–9. Figure 3, which is reproduced below, illustrates an example of a boosting circuit according to the '875 patent. *Id.* at 2:3–4, 2:18–20.

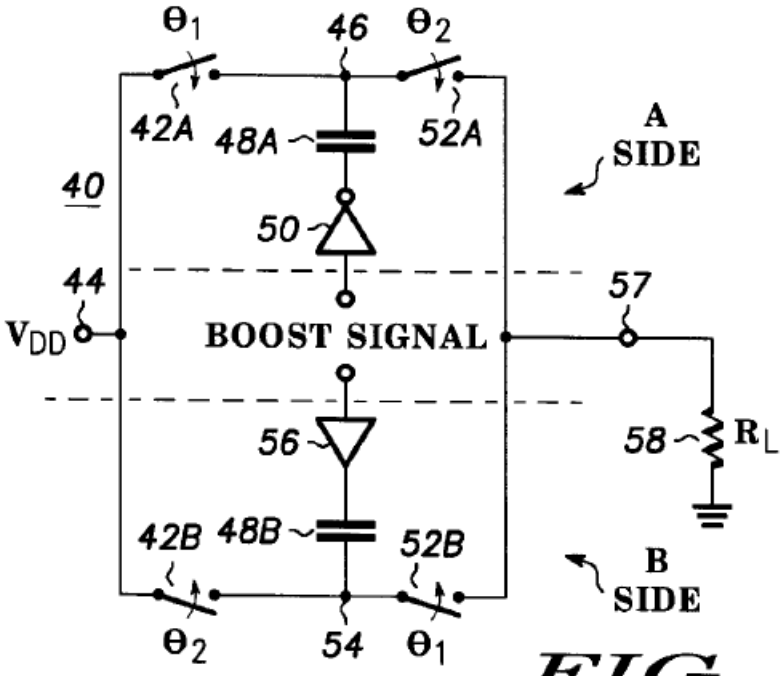

FIG. 3

In particular, Figure 3 shows double-pumping voltage-boosting circuit 40, which has an A side and a B side. *Id.* at 2:20–23. Supply voltage V_{DD} is applied to terminal 44. *Id.* at 2:25–26. Switches 42A and 42B connect supply voltage V_{DD} to respective terminals 46 and 54 when closed, and disconnect terminal 44 from terminals 46 and 54 when opened. *Id.* at 2:24–28. The A side of circuit 40 additionally includes capacitor 48A, which is connected between terminal 46 and the output of inverting buffer driver 50. *Id.* at 2:28–30. Similarly, the B side of circuit 40 includes capacitor 48B, which is connected between terminal 54 and non-inverting buffer driver 56.

Id. at 2:31–33. Terminals 46 and 54 are connected via respective switches 52A and 52B to output 57 of circuit 40, which is connected to load 58. *Id.* at 2:33–36. A voltage boost signal is applied to the inputs of buffer drivers 50 and 56. *Id.* at 2:36–37.

To help explain how circuit 40 operates, Figure 2A also is reproduced below. *Id.* at 2:1–2.

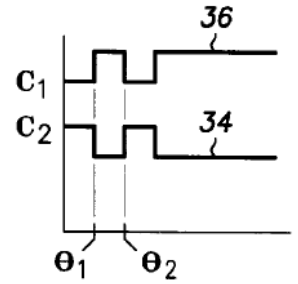

FIG. 2A

Figure 2A shows non-overlapping clock signals C1 and C2 (or clocking signals 34 and 36) that are 180 degrees out of phase with each other. *Id.* at 1:32–34, 2:39.

During first half cycle Θ_1 of clocking signals 34 and 36, switches 42A and 52B are closed, while switches 42B and 52A are opened. *Id.* at 2:38–40. Assuming that capacitor 48B has already been charged to V_{DD} during a previous half cycle, when switch 52B is closed, the boost signal changes to a high-level state, boosting the voltage across capacitor 48B to nearly $2V_{DD}$ to drive into load 58. *Id.* at 2:40–46. As current from capacitor 48B flows into load 58, the charge across capacitor 48B starts to decrease. *Id.* at 2:46–57. At the same time, capacitor 48A is being charged to V_{DD}. *Id.* at 2:54–56. Conversely, during second half cycle Θ_2, switches 42B and 52A are closed, while switches 42A and 52B are opened. *Id.* at 2:56–58. The boost signal also changes from the high-level state to a low-level state, boosting the voltage across capacitor 48A. *Id.* at 2:58–59. As the voltage across

capacitor 48A is boosted, the A side of circuit 40 drives load 58 with a voltage nearly equal to $2V_{DD}$, while V_{DD} is applied across capacitor 48B. *Id.* at 2:59–63. Thus, during the initiation of both half cycles, the voltage drive into load 58 is raised to nearly $2V_{DD}$. *Id.* at 2:63–65.

C. Illustrative Claim

Petitioner challenges claims 1–3 of the '875 patent. Claim 1 is independent and illustrative of the challenged claims:

> 1. A boost circuit having an input terminal and an output terminal, comprising:
>
> a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;
>
> a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;
>
> a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and
>
> a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.

D. Asserted Ground of Unpatentability

Petitioner challenges claims 1–3 of the '875 patent on a single ground based on anticipation under 35 U.S.C. § 102.[1] Pet. 3, 32–54. We instituted *inter partes* review of that ground. Inst. Dec. 21. The instituted ground is as follows.

Claims Challenged	35 U.S.C. §	Reference
1–3	102	Hsieh[2]

In support of this instituted ground, Petitioner relies on a Declaration (Ex. 1003) as well as a Reply Declaration (Ex. 1019) of Jacob Baker, Ph.D., P.E. With its Response, Patent Owner submits a Declaration of Sunil Khatri, Ph.D. (Ex. 2001). The transcripts of the depositions of Dr. Baker and Dr. Khatri are entered in the record as Exhibit 2005 and Exhibit 1021, respectively.

III. ANALYSIS

A. Claim Construction

The '875 patent expired on August 13, 2018, twenty years from its filing date of August 13, 1998. Ex. 1001, code (22); *see also* Pet. 19; PO Resp. 19. For claims of an expired patent, the Board applies the claim interpretation standard applied by district courts. *See Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1376 (Fed. Cir. 2019). "[T]he words of a claim 'are generally given their ordinary and customary meaning'

[1] The Leahy-Smith America Invents Act ("AIA") amended 35 U.S.C. § 102. *See* Pub. L. No. 112-29, 125 Stat. 284, 285–87 (2011). Because the application that issued as the '875 patent was filed before the effective date of the relevant amendment, the pre-AIA version of § 102 applies.
[2] Hsieh, U.S. Patent No. 5,801,997, issued Sept. 1, 1998 (Ex. 1005).

. . . that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp*., 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). "[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which [it] appears, but in the context of the entire patent, including the specification." *Id.* at 1313. A "claim construction that excludes [a] preferred embodiment [described in the specification] is rarely, if ever, correct and would require highly persuasive evidentiary support." *Adams Respiratory Therapeutics, Inc. v. Perrigo Co.*, 616 F.3d 1283, 1290 (Fed. Cir. 2010) (citation omitted). But "a claim construction must not import limitations from the specification into the claims." *Douglas Dynamics, LLC v. Buyers Prods. Co.*, 717 F.3d 1336, 1342 (Fed. Cir. 2013).

Petitioner and Patent Owner propose constructions for various claim terms. Pet. 20–25; PO Resp. 21–35. For purposes of this Decision, we address the claim terms "boost signal," "coupled for receiving," and "non-inverting buffer." *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that "we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999))).

1. "boost signal"

The term "boost signal" appears in claims 1 and 2. Patent Owner argues that "'boost signal' is not a common term of art in the field of electrical and computer engineering," and that an ordinarily skilled artisan's "understanding of the meaning of this claim term at the time of the invention

of the '875 patent would be the meaning as informed by the specification of the '875 patent," namely, "a voltage signal provided to the voltage boosting circuit such that either a non-inverted or inverted version of that signal is received by the second terminal of a capacitor, thereby causing the voltage of the first terminal to be increased." PO Resp. 21–23 (emphasis omitted). As support, Patent Owner contends that the '875 patent teaches that a "BOOST SIGNAL is provided to both the input of the inverting buffer 50 and the input of the non-inverting buffer 56 of the voltage boosting circuit." *Id.* at 22; *see* Ex. 1001, Fig. 3. Patent Owner further contends,

> [D]uring operation of the voltage boosting circuit of the '875 patent, in each side (A or B) of the circuit, the capacitor (48A or 48B, respectively) in that side is first charged to V_{DD} during one half cycle, while its associated switch (42A or 42B, respectively) is closed. Also, during that same half cycle, the signal that is applied to the second terminal of the capacitor in that side (which will either always be a non-inverted or always be an inverted version of BOOST SIGNAL, depending on the side) will be in a low state. Then, during the following half cycle, the signal that is applied to the second terminal of the capacitor in that side (which again will always be either a non-inverted or inverted version of BOOST SIGNAL) will change to a high state. That high state will cause the voltage of the first terminal of the capacitor in that side to be increased (or "boosted") from V_{DD} to nearly $2V_{DD}$.

PO Resp. 22 (citing Ex. 1001, 2:38–65 (describing Figure 3)).

In its Reply, Petitioner counters that "boost signal" does carry "a plain and ordinary meaning," which an ordinarily skilled artisan would have understood to be "a signal that is input to a voltage boosting circuit and that is used to generate a boosted voltage." Pet. Reply 2–3. Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (citing Ex. 1019 ¶ 5).

Petitioner further characterizes Patent Owner's proposed construction as "unduly narrow." *Id.* at 10. As support, Petitioner contends that Patent Owner's proposed construction "reads in a specific embodiment from the specification." *Id.* at 8. According to Petitioner, importing limitations from the specification is improper "even when a specification describes very specific embodiments of the invention or even describes only a single embodiment, unless the specification makes clear that 'the patentee . . . intends for the claims and the embodiments in the specification to be strictly coextensive.'" *Id.* at 9 (quoting *JVW Enters., Inc. v. Interact Accessories, Inc.*, 424 F.3d 1324, 1335 (Fed. Cir. 2005)).

Petitioner additionally contends that Patent Owner's proposed construction "is at odds with the other language of the claims." *Id.* at 7. In particular, Petitioner points us to where claim 1 recites "a second terminal [of a capacitor] coupled for receiving [the] boost signal," and asserts that, "[i]f 'boost signal' would have been understood to require that it be received by a second terminal of a capacitor, this additional claim language would be superfluous." *Id.*

Patent Owner responds that Petitioner "ignores the '875 specification and instead reaches for the broadest construction that, in the absence of any context whatsoever, could apply to virtually *any* signal input to voltage boosting circuit." PO Sur-Reply 6. According to Patent Owner, "[a]ny signal input to the voltage boosting circuit can be said to be *used* to generate a boosted voltage," including Hsieh's power supply voltage source V_{CC}. *Id.* (citing Ex. 1005, Fig. 7).

Based on the record before us, we agree with Petitioner that Patent Owner's proposed construction is overly narrow. Claim 1 recites two

capacitors, namely, "a first capacitor having . . . a second terminal coupled for receiving a boost signal" and "a second capacitor having . . . a second terminal coupled for receiving the boost signal." Construing "boost signal" to mean, in part, that the signal "is received by the second terminal of a capacitor" would render the claim language "a second terminal coupled for receiving" in these instances redundant and superfluous. *See Dig.-Vending Servs. Int'l, LLC v. Univ. of Phx., Inc.*, 672 F.3d 1270, 1275 (Fed. Cir. 2012) (noting "the importance of construing claim terms in light of the surrounding claim language, such that words in a claim are not rendered superfluous").

Further, Patent Owner's proposed construction improperly requires the second terminal of a capacitor to receive the *non-inverted or inverted version* of the boost signal. *See* Tr. 43:3–7 (Patent Owner's counsel stating with respect to claim construction that "we felt like we needed to bring in this notion of that operation that I described in connection with Figure 3"). Even if "*every* embodiment describes the 'boost signal' of the voltage boosting circuit in the same way, *i.e.*, that the second terminal of a capacitor receives either a non-inverted or inverted version of the boost signal, thereby causing the voltage of the first terminal of the capacitor to be increased," as Patent Owner argues, the specification "is not a substitute for, nor can it be used to rewrite, the chosen claim language." PO Sur-Reply 5; *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004); *see Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (expressly rejecting "the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment"). We recognize that "understanding the claim language may be aided by the explanations contained in the written description," but

"it is important not to import into a claim limitations that are not a part of the claim." *SuperGuide*, 358 F.3d at 875. Thus, "a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." *Id.*

Here, the claim language itself recites nothing about the non-inverted or inverted version of the boost signal. As our reviewing court has explained, "it is the *claims*, not the written description, which define the scope of the patent right." *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1347 (Fed. Cir. 1998). Although the '875 patent specification discloses an embodiment in Figure 3 where the second terminal of a capacitor receives the non-inverted or inverted version of the boost signal, nowhere does the specification limit "boost signal" to that embodiment, which we note is described in terms of preference. For example, the '875 patent states that Figure 3 shows "double pumping voltage boosting converter 40 of the *preferred* embodiment of the present invention." Ex. 1001, 2:18–20 (emphasis added). Our reviewing court has "cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1346–47 (Fed. Cir. 2015) (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1328 (Fed. Cir. 2002)).

Turning now to Petitioner's proposed construction of "boost signal" (i.e., "a signal that is input to a voltage boosting circuit and that is used to generate a boosted voltage"), we note Patent Owner's contention that it is overly broad "in the *absence of any context* whatsoever," and that it "could apply to virtually *any* signal input to voltage boosting circuit," including a power supply voltage source. PO Sur-Reply 6 (first emphasis added). As

discussed above, an ordinarily skilled artisan "is deemed to read the claim term not only *in the context of the particular claim in which [it] appears*, but *in the context of the entire patent*, including the specification." *Phillips*, 415 F.3d at 1313 (emphases added). Here, the '875 patent states that "[t]he present invention relates to voltage boosting converters and, more particularly to a double pumping voltage boosting circuit for providing an output voltage greater than a supplied input voltage." Ex. 1001, 1:5–8. As to Figure 3, the '875 patent also describes two distinct signals applied to the voltage boosting circuit, namely, a voltage boost signal and supply voltage V_{DD}. *Id.* at 2:23–28, 2:36–37. Read in the context of the '875 patent, the claim term "boost signal" would not encompass a supplied input voltage.

For purposes of clarification, we construe "boost signal" to mean "a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage." This construction, consistent with the '875 patent, distinguishes between a boost signal and a supplied input voltage. Additionally, our construction of "boost signal" encompasses, but is not limited to, Patent Owner's proposed construction of the term (i.e., "a voltage signal provided to the voltage boosting circuit such that either a non-inverted or inverted version of that signal is received by the second terminal of a capacitor, thereby causing the voltage of the first terminal to be increased"), which corresponds to the embodiment in Figure 3 of the '875 patent.

2. "coupled for receiving"

As discussed above, claim 1 recites "a first capacitor having . . . a second terminal coupled for receiving a boost signal" and "a second

capacitor having . . . a second terminal coupled for receiving the boost signal." With respect to the claim term "coupled for receiving" in particular, Petitioner asserts that the "term 'A "coupled for receiving" D' would not have been understood to mean that A must receive the exact voltage signal of D," or "that A must directly receive D," or "that A always receives (directly or indirectly) the logical value of D or an inversion of the logical value of D." Pet. 24–25. Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (citing Ex. 1003 ¶¶ 74–76).

Patent Owner argues that "[t]he claim language 'terminal coupled for receiving . . . signal' is not a common term of art in the field of electrical and computer engineering," and that an ordinarily skilled artisan's "understanding of the meaning of this claim language at the time of the invention of the '875 patent would be the meaning as informed by the '875 specification," namely, "terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal." PO Resp. 23, 26 (emphasis omitted). As support, Patent Owner directs our attention to Figure 3 of the '875 patent and contends,

> BOOST SIGNAL is applied to the inputs of non-inverting buffer 56 and inverting buffer 50. A non-inverted version of BOOST SIGNAL is output by the non-inverting buffer 56, and an inverted version of BOOST SIGNAL is output by the inverting buffer 50. As a result, the signal that is received by 'second terminal' of the capacitor 48B is *always* a non-inverted version of BOOST SIGNAL, and the signal that is received by the 'second terminal' of capacitor 48A is *always* an inverted version of BOOST SIGNAL.

Id. at 25 (citing Ex. 1001, Fig. 3). Patent Owner adds that "[t]here is no disclosure in the '875 patent of any signal received by the second terminal of

either the first or second capacitors that is not either always a non-inverted version of BOOST SIGNAL or always an inverted version of BOOST SIGNAL." *Id.* at 26.

In its Reply, Petitioner counters that "[t]he plain English meaning of 'for' indicates purpose," and that the claim term "coupled for receiving" therefore has the plain and ordinary meaning "capable of receiving." Pet. Reply 15 (citing Ex. 1026); *see also* Ex. 1026, 709 (dictionary entry defining "for" as "[u]sed to indicate the object, aim, or purpose of an action or activity"). To illustrate, Petitioner asserts that "'X coupled for receiving Y' means that there is a direct/indirect connection between X and Y (at least some of the time) **in order for X to receive Y**." *Id.* Petitioner further asserts that "nothing about the term 'coupled for receiving' indicates the frequency . . . with which the boost signal is received," that is, "[t]his plain and ordinary meaning does not mean that X **always receives** Y." *Id.* Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (Ex. 1019 ¶ 20).

Patent Owner responds that "'[c]oupled for receiving' the specified boost signal, as informed by the entirety of the '875 specification, means that the capacitor actually receives that boost signal, and none other." PO Sur-Reply 15.

As an initial matter, we note Petitioner's apparent misunderstanding of Patent Owner's contention that "the signal that is received by 'second terminal' of the capacitor 48B is *always* a non-inverted version of BOOST SIGNAL, and the signal that is received by the 'second terminal' of capacitor 48A is *always* an inverted version of BOOST SIGNAL." *See* PO Resp. 25. Petitioner treats Patent Owner's use of the term "always" as

referring to frequency, meaning the signal is constantly being received. *See* Pet. Reply 15. During oral argument, however, Patent Owner's counsel clarified that Patent Owner's use of "always" was intended to convey the meaning "only." Tr. 45:8–12, 46:1–24. This is consistent with arguments presented in Patent Owner's Response as well as its Sur-Reply. *See* PO Resp. 25 ("[T]he **signal** that is received by 'second terminal' of the capacitor 48B **is *always* a non-inverted version** of BOOST SIGNAL, and the **signal** that is received by the 'second terminal' of capacitor 48A **is *always* an inverted version** of BOOST SIGNAL.") (emphasis in bold added); PO Sur-Reply 15 ("[T]he capacitor actually receives that boost signal, and none other."). Accordingly, we treat Patent Owner's use of "always" as referring to "only" for purposes of construing "coupled for receiving."

Based on the record before us, we determine that Patent Owner's proposed construction is overly narrow. In particular, it improperly requires that the signal received is either always a *non-inverted version* of the boost signal or always an *inverted version* of the boost signal. *See* Tr. 43:3–7 (Patent Owner's counsel stating with respect to claim construction that "we felt like we needed to bring in this notion of that operation that I described in connection with Figure 3"). The claim language recites nothing about the non-inverted version or the inverted version of the boost signal. Although the '875 patent specification discloses an embodiment in Figure 3 where the second terminal of a capacitor is connected so that the signal it receives is either always a non-inverted version of the boost signal or the inverted version of the boost signal, nowhere does the specification limit "coupled for receiving" the boost signal to that embodiment. Indeed, the '875 patent describes the embodiment of Figure 3 in terms of preference, stating that

Figure 3 shows "double pumping voltage boosting converter 40 of the *preferred* embodiment of the present invention." Ex. 1001, 2:18–20 (emphasis added). As discussed above, our reviewing court has "cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification." *Williamson*, 792 F.3d at 1346–47.

As for Petitioner's proposed construction of "coupled for receiving," we agree that "for" conveys purpose. *See* Ex. 1026, 709. Petitioner does not dispute Patent Owner's contention that "coupled" means "connected." *See* Pet. Reply 15 ("Thus, 'X coupled for receiving Y' means that there is a direct/indirect connection between X and Y (at least some of the time) in order for X to receive Y.) (emphasis omitted); *see also* PO Resp. 26 ("[T]he term 'second terminal of the first capacitor coupled for receiving a boost signal' would have been understood by a [person of ordinary skill in the art] to mean 'the second terminal of the first capacitor is connected in a manner such that the signal received by that second terminal is either always an non-inverted version of the boost signal or always an inverted version of the boost signal.'") (emphasis omitted). Accordingly, we construe "coupled for receiving" to mean "connected in order to receive." Thus, "a first capacitor having . . . a second terminal coupled for receiving a boost signal" refers to a first capacitor having a second terminal that is connected in order to receive a boost signal. Similarly, "a second capacitor having . . . a second terminal coupled for receiving the boost signal" refers to a second capacitor having a second terminal that is connected in order to receive the boost signal.

Based on our construction of "coupled for receiving," we further note that "terminal coupled for receiving . . . signal" encompasses, but is not limited to, Patent Owner's proposed construction of the latter term (i.e.,

"terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal"), which corresponds to the embodiment in Figure 3 of the '875 patent.

3. "non-inverting buffer"

This term appears in claim 2. Petitioner asserts that the '875 patent does not define the claim term "non-inverting buffer." Pet. 21. According to Petitioner, "non-inverting buffer" means "a circuit that isolates or decouples its output from its input, and when enabled, generates an output that is not inverted from its input (*i.e.*, when the input is high, the output is high, and when the input is low, the output is low)." *Id.* at 21–22; *see also id.* at 20 (construing "buffer") (citing Ex. 1011, 112). To support this construction, Petitioner contends that an ordinarily skilled artisan "would have understood that a non-inverting buffer refers to a buffer circuit whose output is not inverted from its input." *Id.* at 21. Petitioner also contends that "a non-inverting buffer can be a tri-state non-inverting buffer that behaves as a non-inverter only when it is enabled (*i.e.*, when its enabling signal is a certain value)." *Id.* Petitioner relies on the declaration testimony of Dr. Baker. *Id.* at 21–22 (citing Ex. 1003 ¶¶ 43, 88, 89).

By contrast, Patent Owner argues that "the term 'non-inverting buffer' would have been understood by a [person of ordinary skill in the art] to mean 'a circuit with a single input and a single output, where the output is always a non-inverted version of the input.'" PO Resp. 33. As support, Patent Owner contends that "[t]he '875 patent, when referencing non-inverting buffer 56, uses the common electrical symbol of a buffer gate,"

and that "a buffer gate is a single input, single output circuit whose output is always 1 if the input is 1, and whose output is always 0 if the input is 0." *Id.* at 32–33; *see also id.* at 34 ("[T]he '875 patent only discloses a single input, single output circuit, where the single output is always a non-inverted version of the single input."). Patent Owner adds that "nothing in the '875 patent suggests that the recited non-inverting buffer would have multiple inputs or that it would need to be selectively enabled." *Id.* at 34.

In its Reply, Petitioner contends that Patent Owner reads into the claim a specific embodiment from the specification, namely, the embodiment shown in Figure 3 of the '875 patent. Pet. Reply. 28. Petitioner further points us to a reference showing "methods of using AND gates as simple buffers" (i.e., non-inverting buffers). *Id.* at 24 (citing Ex. 1027, Fig. 3.27); *see also* Ex. 1027, 462 ("Note that AND gates can be converted into non-inverting buffers . . . as shown in *Figure 3.27*."). These AND gates have multiple inputs. *See* Ex. 1027, Fig. 3.27.

On this record, we agree with Petitioner. Patent Owner's proposed construction improperly imports limitations from the specification into the claims. The claim language recites nothing about a single input and a single output. Although Figure 3 of the '875 patent discloses an embodiment including a non-inverting buffer with a single input and a single output, nowhere does the specification limit "non-inverting buffer" to that embodiment, which is described in terms of preference. Ex. 1001, 2:18–20, Fig. 3. Moreover, the record—specifically, a manual published two years before the filing date of the '875 patent—shows that non-inverting buffers may have more than one input. *See* Ex. 1027, Fig. 3.27.

Additionally, the claim language recites nothing about the output *always* being a non-inverted version of the input. Again, Figure 3 may disclose an embodiment with that feature, but nowhere does the specification limit "non-inverting buffer" to that embodiment. Ex. 1001, Fig. 3.

As noted above, "we need only construe terms . . . to the extent necessary to resolve the controversy." *Nidec*, 868 F.3d at 1017. For purposes of this Decision, we do not construe the entire scope of "non-inverting buffer." Instead, we determine based on the record before us that "non-inverting buffer" is not limited to a circuit with a single input and a single output. For example, a circuit with multiple inputs may be a "non-inverting buffer." Additionally, we determine that the term "non-inverting buffer" also is not limited to a circuit whose output is *always* a non-inverted version of the input. That is, a circuit may be a "non-inverting buffer" if its output is a non-inverted version of the input at any time.

B. Anticipation by Hsieh

Petitioner asserts that Hsieh anticipates claims 1–3 of the '875 patent. Pet. 32–54. Patent Owner responds that Hsieh does not anticipate these claims because Hsieh does not disclose the following claim limitations: "a boost signal," "a second terminal [of a first capacitor] coupled for receiving a boost signal," "a second terminal [of a second capacitor] coupled for receiving the boost signal," and "a non-inverting buffer." PO Resp. 35–48. For the reasons explained below, we determine that Petitioner has demonstrated by a preponderance of the evidence that Hsieh anticipates claims 1–3.

1. Hsieh

Hsieh relates to voltage boosting circuits. Ex. 1005, code (57) (Abstract). Figure 7, which is reproduced below, illustrates an example of Hsieh's circuit. *Id.* at 3:33–34.

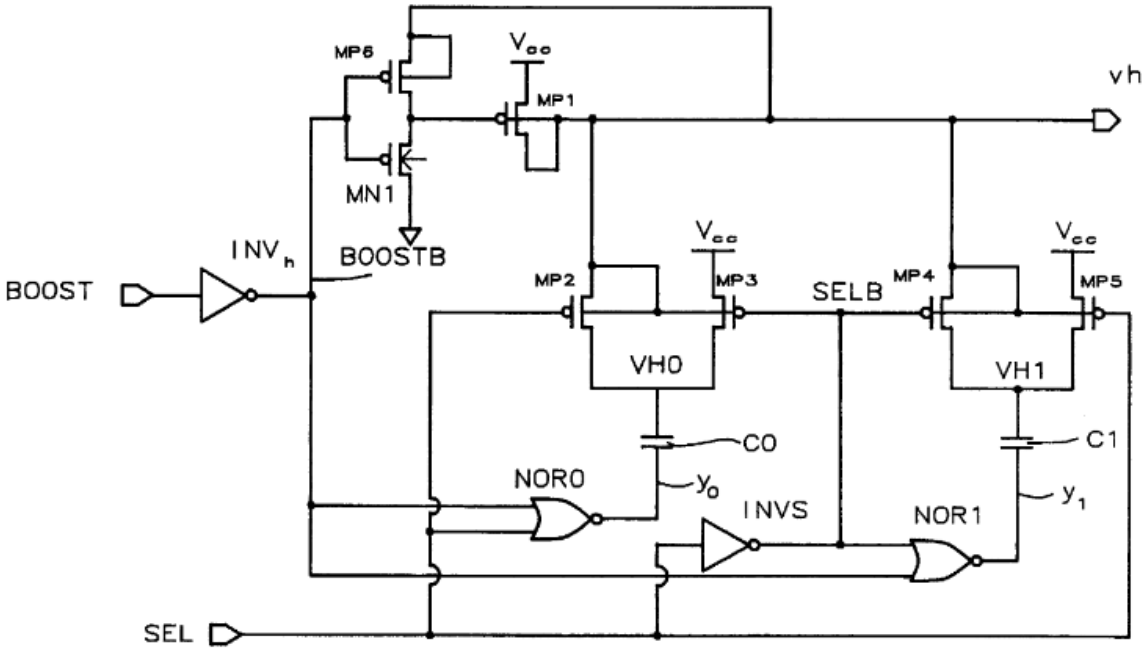

FIG. 7

In particular, Figure 7 shows a ping-pong boost circuit, which comprises two boost circuits BC0 and BC1. *Id.* at 4:50–51, 5:9–11, 5:26–28. First boost circuit BC0 includes transistors Mp2 and Mp3, first capacitor C0, and logical switching circuit NOR0. *Id.* at 5:9–11. Capacitor C0 is connected to logical switching circuit NOR0, which has inputs connected to boost signal BOOSTB (the inverted form of boost signal BOOST) as well as to select signal SEL. *Id.* at 5:5–9. Second boost circuit BC1 includes transistors Mp4 and Mp5, second capacitor C1, and logical switching circuit NOR1. *Id.* at 5:26–28. Capacitor C1 is connected to logical switching circuit NOR1,

whose inputs are connected to signal BOOSTB and signal SELB (the inverted form of select signal SEL). *Id.* at 5:22–26.

If boost signal BOOST and select signal SEL are each at a logical 0, then the outputs of both logical switching circuits NOR0 and NOR1 will each be at a logical 0. *Id.* at 5:36–40. According to these logical states, transistor Mp1 will conduct, and the voltage across output terminal V_h will be the value of power supply voltage source V_{CC}. *Id.* at 5:40–43. Additionally, transistors Mp2 and Mp5 also will conduct, while transistors Mp3 and Mp4 will not conduct. *Id.* at 5:43–44. Thus, both capacitors C0 and C1 will be charged to the level of power supply voltage source V_{CC}. *Id.* at 5:43–47.

If boost signal BOOST changes to a logical 1, while select signal SEL remains at a logical 0, then transistor Mp1 will no longer conduct, and the output of logical switching circuit NOR0 will be at the level of power supply voltage source V_{CC}. *Id.* at 5:53–57. As a result, the charge across capacitor C0 will increase to VH, which will approach 2 X V_{CC}, thereby increasing the voltage across output terminal V_h to VH. *Id.* at 5:57–61.

If boost signal BOOST changes back to a logical 0, while select signal SEL changes to a logical 1, then the outputs of both logical switching circuits NOR0 and NOR1 will each be at a logical 0. *Id.* at 5:62–66. According to these logical states, transistor Mp1 will conduct, and the voltage across output terminal V_h will be the value of power supply voltage source V_{CC}. *Id.* at 5:66–6:2. Additionally, transistors Mp3 and Mp4 also will conduct, while transistors Mp2 and Mp5 will not conduct, causing both capacitors C0 and C1 to be charged to the level of power supply voltage source V_{CC}. *Id.* at 6:2–6.

If the boost signal BOOST changes to a logical 1, while the select signal SEL remains at a logical 1, then transistor Mp1 will stop conducting, and the output of logical switching circuit NOR1 will be at the level of power voltage source V_{CC}. *Id.* at 6:11–15. This will raise the voltage across capacitor C1 to VH, which will approach 2 X V_{CC}, thereby raising the voltage across output terminal V_h again to VH. *Id.* at 6:15–19.

Thus, while first boost circuit BC0 is generating voltage level VH across output terminal V_h, second boost circuit BC1 is restoring the charge to capacitor C1. *Id.* at 6:20–23. Conversely, while second boost circuit BC1 is generating voltage level VH across output terminal V_h, first boost circuit BC0 is restoring the charge to capacitor C0. *Id.* at 6:23–27.

2. Petitioner's Arguments

Petitioner addresses claims 1–3 separately. Accordingly, we address these claims in turn.

a. Claim 1

The preamble of claim 1 recites a "boost circuit" with an "input terminal" and an "output terminal." Petitioner identifies Hsieh's ping-pong boost circuit as a "boost circuit." Pet. 32. As discussed above, Hsieh's ping-pong boost circuit includes transistors Mp1, Mp3, and Mp5. Ex. 1005, Fig. 7. Petitioner notes that transistor Mp1 has a source connected to power supply voltage source V_{CC} as well as a drain and a bulk connected to output terminal V_h, which Petitioner identifies as an "output terminal." Pet. 32–33 (citing Ex. 1005, 4:50–53, Fig. 7). As for the recited "input terminal," Petitioner further notes that each of the sources of transistors Mp1, Mp3, and

Mp5 is connected to power supply voltage source V_{CC}, and contends that an ordinarily skilled artisan "would have understood that the sources of those transistors are essentially connected to a common input terminal that receives the power supply voltage source V_{CC}." *Id.* at 32 (citing Ex. 1005, 4:66–67, 5:16–17, Fig. 7). To support this contention, Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (citing Ex. 1003 ¶ 134). Based on the entire trial record before us, we find that Petitioner has established that Hsieh discloses the preamble.[3]

Claim 1 further recites "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal." For this limitation, Petitioner identifies Hsieh's transistor Mp5 as a "first switch," explaining that transistor Mp5 is positioned between power supply voltage source V_{CC} and output terminal V_h. *Id.* at 34–35. Petitioner further directs us to Figure 7 of Hsieh, which shows that transistor Mp5 is connected directly to supply voltage source V_{CC} and connected to output terminal V_h via transistor Mp4. *Id.* at 35; Ex. 1005, Fig. 7.

Petitioner also identifies Hsieh's select signal SEL as a "first phase signal." Pet. 34. Petitioner points out that "Hsieh discloses that transistor Mp5's gate is connected to select signal SEL," and contends that the "conducting of transistor Mp5 is controlled by select signal SEL." *Id.* (citing Ex. 1005, 5:18–19, 5:36–47, 5:62–6:6, Fig. 7). As support, Petitioner directs us to where Hsieh teaches that transistor Mp5 will conduct when select signal SEL is a logical 0, but will not conduct when select signal SEL is a logical 1. *Id.* (citing Ex. 1005, 5:36–47, 5:62–6:6). Additionally,

[3] We need not decide whether the preamble is limiting because Petitioner shows that Hsieh discloses the preamble.

Petitioner explains that Hsieh's select signal SEL "is a 'phase signal' because it has phases in which it is logical 0 and logical 1." *Id.* at 34 n.12.

Based on the entire trial record before us, we find that Petitioner has established that Hsieh discloses the recited "first switch."

Claim 1 further recites "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal." For this limitation, Petitioner identifies Hsieh's transistor Mp3 as a "second switch," explaining that Figure 7 of Hsieh shows transistor Mp3 being positioned between power supply voltage source V_{CC} and output terminal V_h. *Id.* at 38. In particular, Petitioner explains, transistor Mp3 is connected directly to power supply voltage source V_{CC} and connected to output terminal V_h via transistor Mp2. *Id.* (citing Ex. 1005, Fig. 7).

Petitioner also identifies Hsieh's signal SELB as a "second phase signal." *Id.* at 36. Claim 1 requires the "second switch" to be operated by the "second phase signal." For this aspect of the limitation, Petitioner notes that "Hsieh discloses that transistor Mp3's gate is connected to signal SELB," and contends that "signal SELB controls when transistor Mp3 is conducting." *Id.* at 36–37 (citing Ex. 1005, 5:1–3, 5:36–47, 5:62–6:6, Fig. 7). As support, Petitioner directs us to where Hsieh teaches that transistor Mp3 will conduct when signal SELB is at a logical 0, but will not conduct when signal SELB is at a logical 1. *Id.* at 37 (citing Ex. 1005, 5:36–47, 5:62–6:6).

Claim 1 also requires the "second phase signal" to be opposite to the "first phase signal." For this aspect of the limitation, Petitioner explains that "Hsieh describes that signal SELB is inverted from select signal SEL by

inverter INVS." *Id.* at 36 (citing Ex. 1005, 5:31–33). Petitioner further explains that "Hsieh also describes that the two signals [SEL and SELB] take opposite logical values at the same time (i.e., when one is logical 1, the other is logical 0, and vice versa)." *Id.* (emphasis omitted) (citing Ex. 1005, 5:36–39, 5:62–65). Additionally, Petitioner contends that an ordinarily skilled artisan "would have understood that 'SELB' means SEL 'bar' which, by convention, is the opposite of SEL." *Id.* at 37. Petitioner also contends that an ordinarily skilled artisan "would have understood that . . . the first and second phase signals are opposite to each other even though the signal paths for SEL and SELB are not identical," noting that the '875 patent "treats the two clock signals as being opposite . . . even though the signal paths for Θ_1 and Θ_2 in the ['']875 Patent are not identical." *Id.* at 37 & n.13. Petitioner relies on the declaration testimony of Dr. Baker. *Id.* at 36–37 & n.13 (citing Ex. 1003 ¶¶ 144–146).

Based on the entire trial record before us, we find that Petitioner has established that Hsieh discloses the recited "second switch."

Claim 1 further recites "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal." For this limitation, Petitioner identifies Hsieh's capacitor C1 as a "first capacitor." *Id.* at 39. Referring to Figure 7 of Hsieh, Petitioner points out that "top terminal VH1 of capacitor C1 is connected to output terminal V_h via transistor Mp4." *Id.* (citing Ex. 1005, 5:12–15, Fig. 7). Thus, Petitioner contends, top terminal VH1 of Hsieh's capacitor C1 corresponds to the recited "first terminal." *Id.*

Petitioner further contends that the bottom terminal of Hsieh's capacitor C1 corresponds to the recited "second terminal," and identifies

Hsieh's signal BOOST as a "boost signal." *Id.* at 40 & n.14. As discussed above, we construe "boost signal" to mean "a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage." *See supra* Part III.A.1. With this in mind, we note Petitioner's assertion that "signal BOOST is used to boost the voltage of capacitors C0, C1 to generate a boosted voltage for the ping-pong boost circuit." Pet. 40 n.14 (citing Ex. 1005, 5:36–6:19, Fig. 7). Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (citing Ex. 1003 ¶ 155).

Petitioner also asserts that Hsieh's logical switching circuit NOR1 "receives signal BOOST as an input and outputs the signal y1 to the bottom terminal of capacitor C1." *Id.* at 41 (Ex. 1005, 5:22–29, Fig. 7). To illustrate, Petitioner refers to an annotated version of Figure 7 of Hsieh, which is reproduced below. *Id.* at 40.

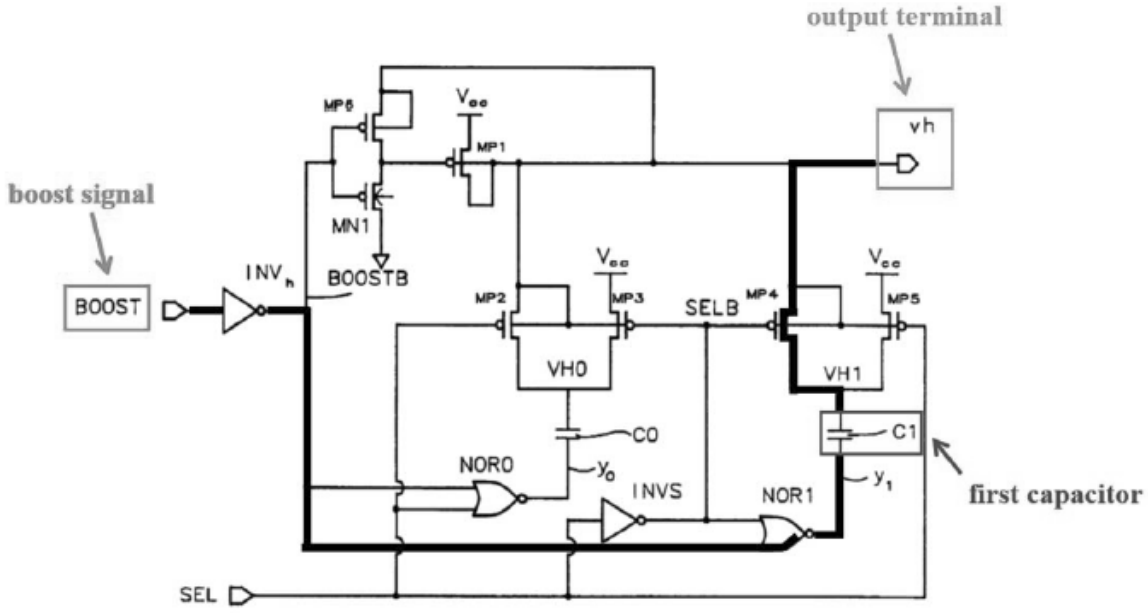

FIG. 7

Petitioner's annotated version of Hsieh's Figure 7 shows a ping-pong boost circuit according to Hsieh. *See* Ex. 1005, 3:33–34; Pet. 40. Petitioner contends:

> Hsieh discloses a circuit, including inverter INVB,[4] inverter INVS, and NOR gate NOR1 . . . . A [person of ordinary skill in the art] would have understood that this circuit is a non-inverting buffer . . . (i.e., with select signal SEL serving as an enabling signal). Specifically, when SEL is logical 1, this non-inverting buffer is enabled, and output y1 is the logical value of the input BOOST. When SEL is logical 0, this non-inverting buffer is disabled, and output y1 is always logical 0 regardless of the value of its input BOOST. Thus, when the non-inverting buffer is enabled, the output signal y1 is the logical value of the input BOOST. Thus, the bottom terminal of capacitor C1 is coupled for receiving signal BOOST.

Pet. 40–41 (internal citations omitted). As discussed above, "coupled for receiving" means "connected in order to receive." *See supra* Part III.A.2. Petitioner relies on the declaration testimony of Dr. Baker. Pet. 41 (citing Ex. 1003 ¶¶ 152–154).

Having considered the trial record before us, including Patent Owner's arguments regarding the claim terms "boost signal" and "coupled for receiving," which we address in detail below, we find that Petitioner has shown that Hsieh discloses the recited "first capacitor." *See infra* Part III.B.3.

Lastly, claim 1 recites "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal." For this limitation, Petitioner identifies Hsieh's capacitor

[4] Petitioner notes that "[t]his inverter is described in the specification of Hsieh as 'INVB' while mistakenly labeled as 'INVh' in FIG. 7." Pet. 41 n.15 (citing Ex. 1005, 5:30–35). We agree with Petitioner in this regard.

C0 as a "second capacitor." Pet. 42. Petitioner also identifies top terminal VH0 of Hsieh's capacitor C0 as a "first terminal." As support, Petitioner directs us to where Hsieh teaches that "top terminal VH0 of capacitor C0 is connected to output terminal V_h via transistor Mp2." *Id.* (citing Ex. 1005, 4:61–65, Fig. 7).

Petitioner further identifies the bottom terminal of Hsieh's capacitor C0 as a "second terminal." *Id.* at 43. Directing us to another annotated version of Figure 7 of Hsieh, which is reproduced below, Petitioner presents an argument similar to the one discussed above with respect to the recited "first capacitor." *Id.* at 43.

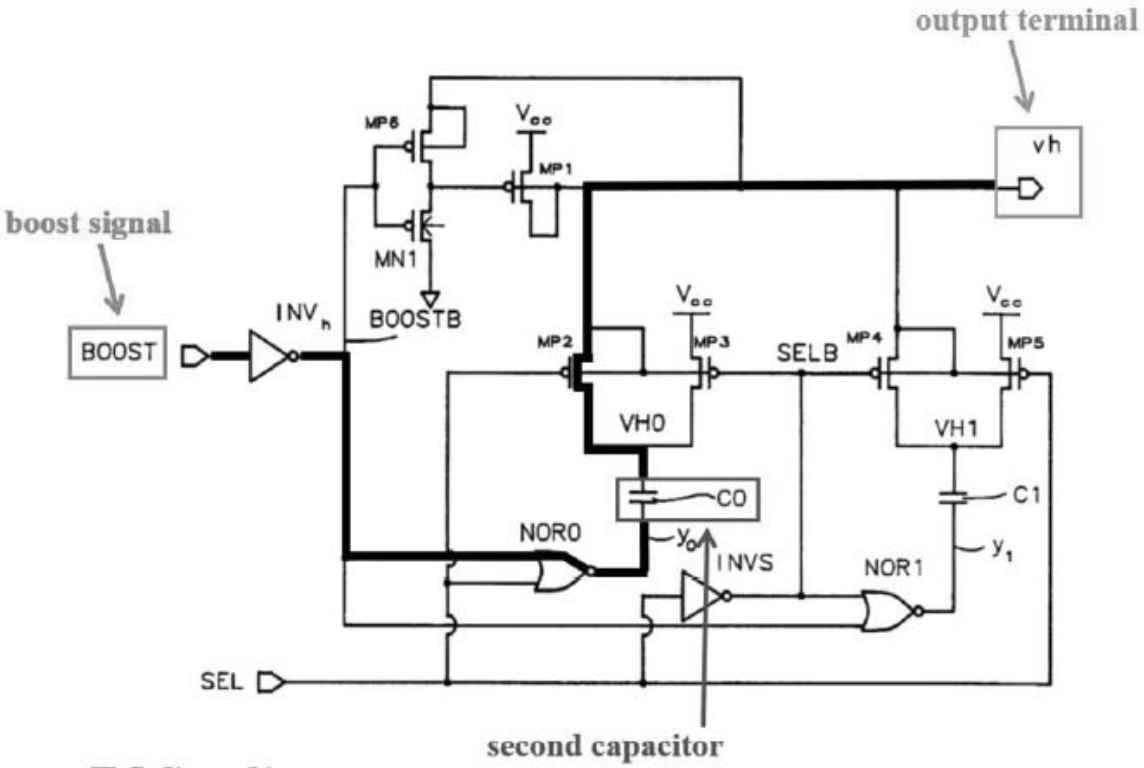

FIG. 7

Petitioner's annotated version of Hsieh's Figure 7 shows a ping-pong boost circuit according to Hsieh. *See* Ex. 1005, 3:33–34; Pet. 43. According to Petitioner, an ordinarily skilled artisan would have understood that the

circuit comprising "inverter INVB and NOR gate NOR0, which receives signal BOOST as an input and outputs signal y0 to the bottom terminal of capacitor C0 . . . is a non-inverting buffer" that operates like the non-inverting buffer discussed above with respect to the recited "first capacitor." Pet. 43. That is, "when SEL is logical 0, this non-inverting buffer is enabled, and output y0 is the logical value of input BOOST," and "[w]hen SEL is logical 1, this non-inverting buffer is disabled, and output y0 is always logical 0 regardless of the value of its input BOOST." *Id.* at 44. Accordingly, Petitioner contends, "when the non-inverting buffer is enabled, the output signal y0 is the logical value of input BOOST," and "the bottom terminal of capacitor C0 is coupled for receiving signal BOOST." *Id.* Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (citing Ex. 1003 ¶¶ 159, 161); *see also* Ex. 1003 ¶ 160.

Having considered the trial record before us, including Patent Owner's arguments regarding the claim terms "boost signal" and "coupled for receiving," which we address in detail below, we find that Petitioner has established that Hsieh discloses the recited "second capacitor." *See infra* Part III.B.3.

b. Claim 2

Claim 2 depends from claim 1 and recites "an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor." For this limitation, Petitioner identifies Hsieh's inverter INVB as an "inverting buffer." As support, Petitioner directs us to where Hsieh teaches that "inverter INVB forms the inverted boost signals BOOSTB from the input BOOST." Pet. 45 (citing

Ex. 1005, 5:30–31). Referring to Figure 7 of Hsieh, Petitioner also points out that "inverter INVB ('inverting buffer') has an input coupled for receiving signal BOOST ('boost signal')," and that "the output of inverter INVB is connected to the bottom terminal of capacitor C1 via NOR gate NOR1." *Id.* at 46. As discussed above with respect to claim 1, Petitioner identifies Hsieh's capacitor C1 as a "first capacitor" and the bottom terminal of capacitor C1 as the capacitor's "second terminal." Having considered the trial record before us, including Patent Owner's arguments regarding the claim terms "boost signal" and "coupled for receiving," which we address in detail below, we find that Petitioner has shown that Hsieh discloses the recited "inverting buffer." *See infra* Part III.B.3.

Claim 2 further recites "a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor." For this limitation, Petitioner identifies Hsieh's inverter INVB and logical switching circuit NOR0 together as comprising a "non-inverting buffer." Pet. 47. To illustrate, Petitioner provides an annotated version of Figure 7 of Hsieh, which is reproduced below.

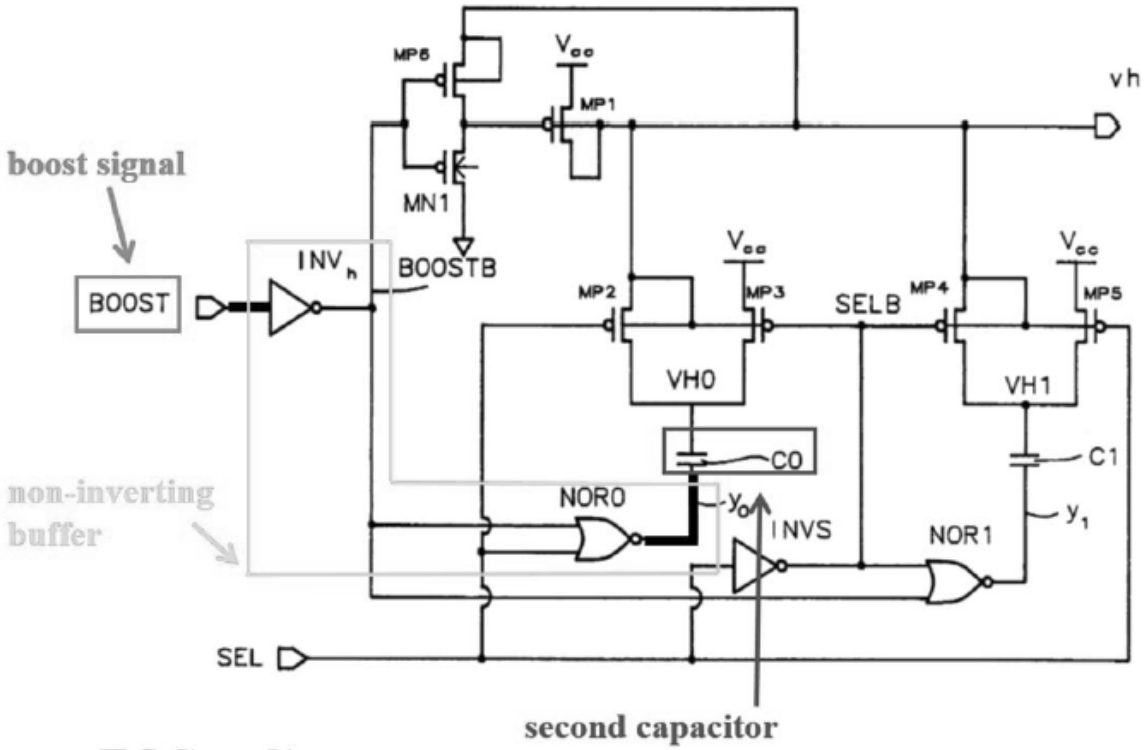

FIG. 7

Petitioner's annotated version of Hsieh's Figure 7 shows a ping-pong boost circuit described in Hsieh (*see* Ex. 1005, 3:33–34), where the circuit components enclosed in green are what Petitioner identifies as comprising a "non-inverting buffer" (Pet. 48). As shown in the figure, the non-inverting buffer receives boost signal BOOST as its input at inverter INVB. Pet. 49. Additionally, the non-inverting buffer has an output at logical switching circuit NOR0 directly connected to the bottom terminal of capacitor C0. *Id.* at 50. As discussed above, Petitioner identifies Hsieh's capacitor C0 as a "second capacitor" and the bottom terminal of capacitor C0 as the capacitor's "second terminal."

According to Petitioner, an ordinarily skilled artisan would have understood that the non-inverting buffer circuit (enclosed in green) operates similarly to the non-inverting buffer discussed above with respect to claim 1.

Id. at 48. In particular, Petitioner explains that "select signal SEL is an 'enabling signal,'" enabling the circuit when it is at a logical 0 and disabling the circuit when it is at a logical 1. *Id.* at 48–49. Petitioner further explains that output y0 depends on boost signal BOOST while the circuit is enabled, but does not depend on boost signal BOOST while the circuit is disabled. *Id.* at 49. To illustrate, Petitioner provides a truth table, which is reproduced below. *Id.*

<table>
<tr><th>BOOST</th><th>y0</th><th>SEL</th></tr>
<tr><td>1</td><td>1</td><td rowspan="2">0 (enabled)</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td rowspan="2">0</td><td rowspan="2">1 (disabled)</td></tr>
<tr><td>0</td></tr>
</table>

Petitioner's truth table shows the relationship between the input signal (i.e., Hsieh's boost signal BOOST), the output signal (i.e., Hsieh's output y0), and the enabling signal (i.e., Hsieh's select signal SEL) of the non-inverting buffer circuit. *Id.* When the circuit is enabled (i.e., when select signal SEL is at a logical 0), its output is not inverted from its input. *Id.* Petitioner relies on the declaration testimony of Dr. Baker. *Id.* at 48–49 (citing Ex. 1003 ¶¶ 171–173).

Having considered the trial record before us, including Patent Owner's arguments regarding the claim terms "boost signal," "coupled for receiving," and "non-inverting buffer," which we address in detail below, we find that Petitioner has established that Hsieh discloses the recited "non-inverting buffer." *See infra* Part III.B.3.

c. Claim 3

Claim 3, which also depends from claim 1, recites "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal." For this limitation, Petitioner identifies Hsieh's transistor Mp4 as a "third switch," explaining that transistor Mp4 is positioned between top terminal VH1 of capacitor C1 and output terminal V_h. Pet. 52 (citing Ex. 1005, Fig. 7). As discussed above with respect to claim 1, Petitioner identifies Hsieh's capacitor C1 as a "first capacitor," top terminal VH1 as the capacitor's "first terminal," and output terminal V_h as an "output terminal."

Petitioner further contends that Hsieh's transistor Mp4 is operated by signal SELB (which Petitioner identifies as a "second phase signal," as discussed above with respect to claim 1). *Id.* at 51. As support, Petitioner directs us to Hsieh's teaching that the gate of transistor Mp4 is connected to signal SELB. *Id.* (citing Ex. 1005, Fig. 7). Petitioner also directs us to where Hsieh teaches that transistor Mp4 does not conduct when signal SELB is at a logical 1, but does conduct when signal SELB is at a logical 0. *Id.* (citing Ex. 1005, 5:36–47, 5:62–6:6). Petitioner relies on the declaration testimony of Dr. Baker. *Id.* (citing Ex. 1003 ¶ 178).

Based on the entire trial record before us, we find that Petitioner has established that Hsieh discloses the recited "third switch."

Claim 3 also recites "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal." For this limitation, Petitioner identifies Hsieh's transistor Mp2 as a "fourth switch," explaining that transistor Mp2 is located between top terminal VH0 of capacitor C0 and output terminal V_h. *Id.* at 53. As

discussed above with respect to claim 1, Petitioner identifies Hsieh's capacitor C0 as a "second capacitor," top terminal VH0 as the capacitor's "first terminal," and output terminal V_h as an "output terminal."

Petitioner further contends that Hsieh's transistor Mp2 is operated by signal SEL (which Petitioner identifies as a "first phase signal," as discussed above with respect to claim 1). *Id.* at 52. As support, Petitioner points to Hsieh's teaching that the gate of transistor Mp2 is connected to select signal SEL. *Id.* (citing Ex. 1005, 4:62–63, Fig. 7). Petitioner additionally directs us to where Hsieh teaches that transistor Mp2 conducts when select signal SEL is at a logical 0, but does not conduct when select signal SEL is at a logical 1. *Id.* (citing Ex. 1005, 5:36–47, 5:62–6:6). Petitioner relies on the declaration testimony of Dr. Baker. *Id.* at 53 (citing Ex. 1003 ¶ 182).

Based on the entire trial record before us, we find that Petitioner has established that Hsieh discloses the recited "fourth switch."

3. Patent Owner's Arguments

Patent Owner argues that Hsieh does not disclose three claim limitations: "boost signal," "second terminal coupled for receiving" the boost signal, and "non-inverting buffer." PO Resp. 35–48. We address these limitations in turn.

a. "boost signal"

As discussed above, claims 1 and 2 recite the term "boost signal." Patent Owner argues that Hsieh's BOOST signal is not a "boost signal" because "y0 and y1 are not non-inverted or inverted versions of the signal

designated BOOST in Hsieh." PO Resp. 38. As support, Patent Owner contends,

> [T]here are only two time intervals during which the voltage at the top terminal of the capacitors (C0 or C1) is increased or boosted. . . . [D]uring the first time interval, ... [t]he signal y0 is received by the bottom terminal ("second terminal") of C0, which was previously charged to Vcc. As a result, the voltage at VH0 (the top terminal ("first terminal") of C0) is increased from Vcc to nearly 2Vcc. During the second time interval, ... [t]he signal y[1][5] is received by the bottom terminal ("second terminal") of C1, which was previously charged to Vcc. As a result, the voltage at VH1 (the top terminal ("first terminal") of C1) is increased from Vcc to nearly 2Vcc.

Id. at 37 (internal citations omitted). According to Patent Owner, "[s]ignals y0 and y1 that are output by NOR0 and NOR1, respectively, and received by the bottom terminals ('second terminals') of C0 and C1, respectively, are not either non-inverted or inverted versions of the signal designated BOOST in Hsieh." *Id.*

We disagree with Patent Owner's argument, which relies on Patent Owner's proposed construction of "boost signal" (i.e., "a voltage signal provided to the voltage boosting circuit such that either a non-inverted or inverted version of that signal is received by the second terminal of a capacitor, thereby causing the voltage of the first terminal to be increased"). As discussed above, that construction is overly narrow and improperly requires a non-inverted or inverted version of the boost signal. *See supra* Part III.A.1.

[5] Patent Owner specifies "y0," but we believe Patent Owner intended to specify "y1." *See* Ex. 1005, Fig. 7 (showing capacitor C1 receiving signal y1, not signal y0).

The proper construction of "boost signal" is "a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage." *Id.* Under that construction, we find that Hsieh's BOOST signal is a "boost signal," as recited in claim 1. Hsieh teaches that its "boost signals will cause the [output] voltage Vh to be clamped . . . to the level of the power supply voltage source Vcc and then boosted to the voltage VH." Ex. 1005, 4:37–39. Referring to Figure 7, Hsieh teaches specifically that "[i]f the BOOST signal now changes to a logical 1 and the SELECT signal remains at a logical 0, . . . the output y0 of the logical switching circuit NOR0 will be placed at the level of the *power supply voltage source Vcc*," and "[t]he first plate VH0 of the first capacitor C0 will now be raised to the level of *VH, which will approach the level of 2XVcc*." *Id.* at 5:53–59 (emphases added) (cited by Pet. 40 n.14). We note that Hsieh's capacitor C1 corresponds to the recited "first capacitor." Hsieh also teaches that "[i]f the BOOST signal now changes to a logical 1 and the SELECT signal remains at a logical 1, . . . the output y1 of the logical switching circuit NOR1 will be placed at the level of the *power supply voltage source Vcc*," and "[t]he first plate VH1 of the second capacitor C1 will now be raised to the level of *VH, which will approach the level of 2XVcc*." *Id.* at 6:11–17 (emphases added) (cited by Pet. 40 n.14). Hsieh's capacitor C0 corresponds to the recited "second capacitor." For both scenarios, Hsieh states that "[t]his voltage doubling action will *raise the voltage level of the output terminal [Vh] to the level of VH*." *Id.* at 5:59–61, 6:17–19 (emphasis added) (cited by Pet. 40 n.14). In light of these teachings, we find that Patent Owner's argument does not undermine Petitioner's showing that Hsieh discloses the recited "boost signal."

b. "coupled for receiving"

As discussed above, claim 1 recites "a first capacitor having . . . a second terminal coupled for receiving a boost signal" and "a second capacitor having . . . a second terminal coupled for receiving the boost signal." Patent Owner argues that "the second terminals of capacitors C0 and C1 in Hsieh are not coupled for receiving the signal designated BOOST in Hsieh" because "the signals y0 and y1 are not either always non-inverted or inverted versions of BOOST." PO Resp. 39, 41; *see also id.* at 43 ("[U]nder the proper construction of these claim terms, for the second terminals of C0 and C1 to be coupled for receiving the signal designated BOOST in Hsieh, y0 and y1 must either always be the non-inverted version of BOOST or always be the inverted version of BOOST."). As support, Patent Owner points out that "the bottom terminal of the capacitor C0 receives the signal y0 that is output by NOR0," and "the bottom terminal of the capacitor C1 receives the signal y1 that is output by NOR1." *Id.* at 40–41 (citing Ex. 1005, 5:5–11, 5:22–29, Fig. 7). Patent Owner contends that signals y0 and y1 are "entirely different signal[s] than the signal designated BOOST in Hsieh." *Id.* at 41. In particular, Patent Owner contends, "[S]ignals y0 and y1 are entirely new signals generated by the logic functions that include NOR0 and NOR1, respectively, of which BOOST is only one of two inputs." *Id.*

Patent Owner additionally contends that "the signal received by the second terminal of the first and second capacitors must be non-inverted or inverted versions of each other." *Id.* at 44. According to Patent Owner, Hsieh's signals "y0 and y1 are not either always non-inverted versions of

each other or always inverted versions of each other," but they are instead "different logic signals generated by different logic functions." *Id.* at 45.

We disagree with Patent Owner's argument. Patent Owner relies on its proposed construction of "terminal coupled for receiving . . . signal" (i.e., "terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal"). For the reasons given above, Patent Owner's proposed construction improperly requires a non-inverted version or inverted version of the boost signal. *See supra* Part III.A.2.

As explained above, the proper construction of "coupled for receiving" is "connected in order to receive." *Id.* Thus, "a first capacitor having . . . a second terminal coupled for receiving a boost signal" refers to a first capacitor having a second terminal that is connected in order to receive a boost signal. Similarly, "a second capacitor having . . . a second terminal coupled for receiving the boost signal" refers to a second capacitor having a second terminal that is connected in order to receive the boost signal.

Based on our construction, we find that the terminals of Hsieh's capacitors C0 and C1 are coupled for receiving a boost signal, namely, Hsieh's BOOST signal. Figure 7 of Hsieh shows that BOOST signal follows a path leading to capacitor C0 as well as a path leading to capacitor C1. Ex. 1005, Fig. 7. In particular, Figure 7 shows that BOOST signal passes through inverter INVB and logical switching circuit NOR0 before reaching capacitor C0, and that BOOST signal also passes through inverter INVB and logical switching circuit NOR1 before reaching capacitor C1. *Id.* Because BOOST signal passes through inverter INVB and logical switching circuits NOR0, NOR1, the capacitors receive signals y0

and y1, which are functions of BOOST signal. *See* Tr. 61:23–62:7 (Patent Owner's counsel conceding that Hsieh's signal y0 is "a function of the Boost signal"). Nothing in the '875 patent precludes the recited "boost signal" from passing through intervening circuit elements, such as Hsieh's inverter INVB and logical switching circuits NOR0, NOR1, before reaching a capacitor. Indeed, the embodiment in Figure 3 of the '875 patent includes intervening circuit elements, namely, inverting buffer driver 50 and non-inverting buffer driver 56. Ex. 1001, Fig. 3. The outputs of these drivers are functions of the boost signal. Accordingly, Patent Owner's argument does not undermine Petitioner's showing that Hsieh discloses "a first capacitor having . . . a second terminal coupled for receiving a boost signal" and "a second capacitor having . . . a second terminal coupled for receiving the boost signal."

c. "non-inverting buffer"

As discussed above with respect to claim 2, Petitioner contends, and we agree, that the circuit including Hsieh's inverter INVB and logical switching circuit NOR0 comprises a "non-inverting buffer," as recited in the claim. Pet. 47. Patent Owner counters that the circuit including these two elements of Hsieh "is not a non-inverting buffer" because it "has two inputs, namely BOOST and SEL, and one output, namely y0." PO Resp. 46, 48. Patent Owner also contends that the circuit is not a non-inverting buffer because it "only *sometimes* generates an output that is a non-inverted version of the input." *Id.* at 47. According to Patent Owner, the recited "non-inverting buffer" requires "a circuit with a single input and a single output,

where the output is always a non-inverted version of the input." *Id.* at 46 (emphasis omitted).

We disagree. Patent Owner relies on its proposed construction of "non-inverting buffer" (i.e., "a circuit with a single input and a single output, where the output is always a non-inverted version of the input"). As discussed above, Patent Owner's proposed construction improperly requires a *single input* and a *single output* as well as an output that is *always* a non-inverted version of the input. *See supra* Part III.A.3. Accordingly, that Hsieh's circuit comprising inverter INVB and logical switching circuit NOR0 may have multiple outputs and may sometimes generate an output that is a non-inverted version of the input does not undermine Petitioner's showing that Hsieh discloses the recited "non-inverting buffer." *See also* Ex. 1027, Fig. 3.6 ("Any two elements from an inverter IC can be used to make a non-inverting buffer element.") (cited by Pet. Reply 24), Fig. 3.15 ("Any NAND or NOR gate can be used as an inverting buffer element.") (cited by Pet. Reply 24).

In view of the foregoing, we determine that Petitioner has demonstrated by a preponderance of the evidence that Hsieh anticipates claims 1–3.

IV. CONCLUSION[6]

In summary:

Claims	Basis	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3	§ 102	Hsieh	1–3	

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–3 of the '875 patent are held *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

[6] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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