UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.,
Petitioner,

v.

Qualcomm Incorporated,
Patent Owner

Case IPR2018-01249
U.S. Patent No. 7,693,002

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 37 C.F.R § 90.2(a), Patent Owner Qualcomm Incorporated ("Qualcomm" or "Patent Owner"), hereby appeals to the United States Court of Appeals for the Federal Circuit the Patent Trial and Appeal Board's Final Written Decision in IPR2018-01249, entered on January 6, 2020 (Paper No. 27) and from all underlying orders, decisions, rulings and opinions that are adverse to Qualcomm, including, without limitation, those within the Decision on Institution of *Inter Partes* Review, entered January 15, 2019 (Paper No. 6).

In accordance with 37 C.F.R § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal include, but are not limited to, constitutionality of the appointment of the Administrative Patent Judges who presided over this *inter partes* review; determination of unpatentability of claims 1-28 and 31-37 of U.S. Patent No. 7,693,002 under 35 U.S.C. § 103(a); any finding or determination supporting or related to those issues; as well as all other issues decided adversely to Patent Owner in any orders, decisions, rulings, and opinions.

Simultaneous with this submission, a copy of this Notice of Appeal is being filed with the United States Patent and Trademark Office by way of hand delivery to the Office of General Counsel to:

Office of the General Counsel
United States Patent and Trademark Office
Madison Building East, Room 10B20
600 Dulany Street
Alexandria, Virginia 22314

In addition, this Notice of Appeal, along with a copy of the Final Written Decision, is being filed electronically with the United States Court of Appeals for the Federal Circuit along with the required docketing fees, and one paper copy of the Notice of Appeal is being provided to the Clerk's Office:

Clerk of Court
United States Court of Appeals for the Federal Circuit
717 Madison Place, NW, Room 401
Washington, DC 20439

Respectfully submitted,

Date: March 4, 2020

/ Joshua R. Nightingale /

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Counsel for Patent Owner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that on March 4, 2020, a complete and entire copy of this **PATENT OWNER'S NOTICE OF APPEAL** has been served in its entirety by e-mail on the following counsel of record for petitioner:

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Paper 27
Entered: January 6, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

IPR2018-01249
Patent 7,693,002 B2

Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and SCOTT B. HOWARD, *Administrative Patent Judges.*

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Granting Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Apple Inc. ("Petitioner") challenges the patentability of claims 1–28 and 31–37 of U.S. Patent No. 7,693,002 B2 ("the '002 patent," Ex. 1001), which is assigned to Qualcomm Incorporated ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–28 and 31–37 of the '002 patent are unpatentable. *See* 35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

On June 18, 2018, Petitioner requested *inter partes* review of claims 1–28 and 31–37 of the '002 patent on the following grounds:

Claims Challenged	35 U.S.C. §[1]	Reference(s)
1–28, 31–37	103(a)	Sato[2]
1–17, 20–28, 31–36	103(a)	Asano,[3] Itoh[4]

[1] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 103 and 112 that became effective after the filing of the application for the '002 patent. Therefore, we apply the pre-AIA versions of these sections.
[2] US 4,951,259, issued Aug. 21, 1990 (Ex. 1005).
[3] US 2006/0098520 A1, published May 11, 2006 (Ex. 1006).
[4] Kiyoo Itoh, *VLSI Memory Chip Design*, (2001) (Ex. 1007).

Paper 2 ("Pet."). Patent Owner did not file a Preliminary Response. We instituted trial on all grounds of unpatentability. Paper 6 ("Dec. on Inst."), 18.

During the trial, Patent Owner filed a Response (Paper 11, "PO Resp."), Petitioner filed a Reply (Paper 15, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 17, "PO Sur-reply").

Petitioner filed a Motion to Exclude Exhibit 2004 (Paper 19), to which Patent Owner filed an Opposition (Paper 21), and in support of which Petitioner filed a Reply (Paper 23).

An oral hearing was held on October 10, 2019, a transcript of which appears in the record. Paper 26 ("Tr.").

B. The '002 Patent and Illustrative Claim

The '002 patent generally relates to wordline drivers and decoders for memory arrays. Ex. 1001, code (57), 1:7–9. Figure 1 of the '002 patent is reproduced below.

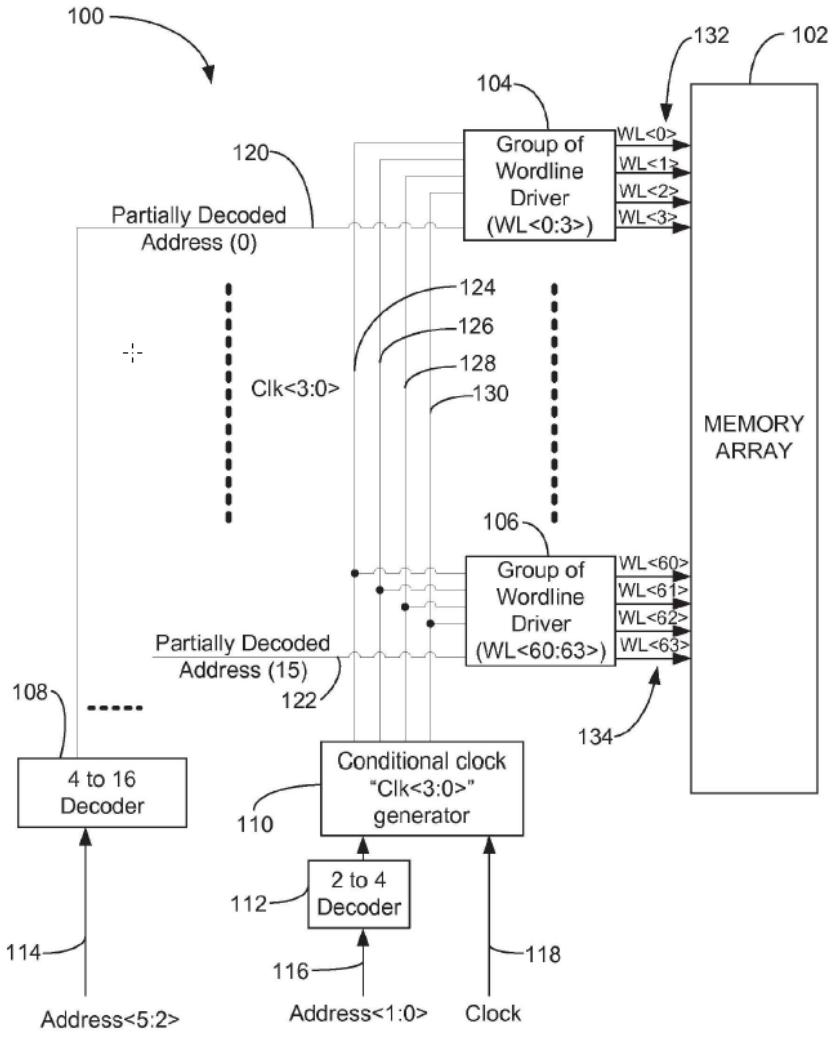


FIG. 1

Figure 1 is a block diagram of an embodiment of a wordline driver system 100. Ex. 1001, 2:31–34. Figure 1 shows groups of wordline drivers 104 and 106 that control particular wordlines in memory array 102. *Id.* at 2:53–3:8. Group of wordline drivers 104 drives wordlines WL<0> through WL<3>, and group of wordline drivers 106 drives wordlines WL<60> through WL<63>. *Id.* Additional wordline drivers that are not shown control the wordlines between WL<3> and WL<60>. *Id.* at 3:4–8.

In operation, two-to-four bit decoder 112 decodes the first portion (such as bits 0 and 1) of a six-bit memory address, and four-to-sixteen bit decoder decodes the remaining portion of the address (bits 2 through 5). Ex. 1001, 3:9–25. Based on the decoded first portion of the address received from decoder 112, conditional clock generator 110 "selectively applies the clock signal to a selected one of the clock outputs 124, 126, 128 and 130," each of which is coupled to a particular wordline driver in each group of wordline drivers. *Id.* at 3:26–34. "The four-to-sixteen bit memory address decoder 108 decodes the remainder of the six-bit memory address (e.g. bits two to five) and applies a partial address input to the wordlines that are related to the decoded memory address." *Id.* at 3:37–40. For example, if the partially-decoded address indicates that the first group of wordlines is addressed (WL<0> through WL<3>), decoder 108 applies a signal to address line 120, which, as shown in Figure 1, connects to group of wordline drivers 104. Ex. 1001, 3:41–67. The '002 patent explains that "the decoded output of the two-to-four decoder 112 with clock generator 110 and the decoded output of the four-to-sixteen bit memory address decoder 108 may be utilized via a logical AND operation to selectively activate a wordline driver of the group of wordline drivers 104." *Id.* at 4:3–8.

Of the challenged claims, claims 1, 7, 11, 17, 21, and 23–27 are independent. Claim 1, reproduced below, is illustrative.

> 1. A circuit device comprising:
>
> first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array; and

> second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Robert Horst, Petitioner offers the following assessment as to the level of ordinary skill in the art:

> A person of ordinary skill in the art ("POSITA") as of October 10, 2006 would have had at least an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. Alternatively, a person of ordinary skill with less than the amount of experience noted above would have had a correspondingly greater amount of educational training such a graduate degree in a related field.

Pet. 2 (citing Ex. 1003 ¶¶ 27–29). In the Institution Decision, we stated that, "[t]o the extent necessary, and for purposes of this Decision, we accept the assessment offered by Petitioner, with the exception of the language 'at least,' because this assessment is consistent with the '002 patent, the asserted prior art, and the evidence of record." Dec. on Inst. 6 (citing Ex. 1003 ¶ 27). In its Response, Patent Owner states that it "accepts Petitioner's proposed education and experience level of one of ordinary skill in the art, as modified by the Board's institution decision." PO Resp. 15 (citing Pet. 2; Dec. on Inst. 6).

Based on the evidence of record, we determine, consistent with our assessment in the Institution Decision, that the skill level of a person of ordinary skill in the art would have been that of a person with an undergraduate degree in electrical engineering, or a related field, and three

years of experience in the design of memory systems and circuits. Alternatively, a person of ordinary skill with less than the amount of experience noted above would have had a correspondingly greater amount of educational training such as a graduate degree in a related field. *See* Ex. 1003 ¶ 27; *see also* Ex. 2001 (Patent Owner's declarant Dr. Pedram testifying that he "do[es] not dispute Petitioner's proposed level of ordinary skill in the art as modified by the Board").

B. Claim Interpretation

In an *inter partes* review for a petition filed before November 13, 2018, a claim in an unexpired patent shall be given its broadest reasonable construction in light of the Specification of the patent in which it appears. 37 C.F.R. § 42.100(b) (2018); *see* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)). The Petition was accorded a filing date of June 18, 2018, and, therefore, the broadest reasonable interpretation standard for claim interpretation applies. *See* Paper 5 (Notice of Filing Date Accorded to Petition).

In applying a broadest reasonable interpretation, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). This presumption may be rebutted when a patentee, acting as a lexicographer, sets forth an alternate definition of a term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480

(Fed. Cir. 1994). Furthermore, only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

1. Clock Signal

Patent Owner argues that the term "clock signal" should be construed as "a periodic signal used for synchronization" and that, under this interpretation, Petitioner's obviousness challenge based on Sato fails because Sato does not teach such a signal. PO Resp. 11–15, 30–45.

Patent Owner relies on the absence of disclosure in the '002 patent to show that its construction is proper rather than on intrinsic evidence that affirmatively supports its construction. For example, Patent Owner argues that "[t]he '002 patent *does not* describe an asynchronous memory system that uses multiple, non-periodic timing signals." PO Resp. 12 (citing Ex. 2001 ¶ 54). This is true insofar as the '002 patent is completely silent on the issue. Notably absent from the Specification of the '002 patent is any mention of the clock signal as "periodic" or used for "synchronization." The words "period," "frequency," and "synchronous," and derivatives therefrom, appear nowhere in the Specification of the '002 patent. In its Response, Patent Owner does not cite a single passage of the '002 patent to support its proposed construction. *See* PO Resp. 11–15. In its Sur-reply, Patent Owner argues the following:

> [T]he invention of the '002 patent is specifically intended to address problems that arise from the use of a periodic clock signal. Such a clock signal periodically switches between logic-level high and low states, thus resulting in high power

> consumption, and because the periodic clock signal is distributed to many different components of the memory system to synchronize them, a heavy load is placed on the clock signal. *See* Ex. 1001 at 1:11-25. The invention of the '002 patent is intended to address the problems of power consumption and loading that result from the use of a periodic, synchronizing clock signal. *See id.*

PO Sur-reply 3–4. The cited passage is from the "Description of Related Art" section in the "BACKGROUND" of the '002 patent and does not mention periodicity or synchronization. Ex. 1001, 1:11–25.

Patent Owner's declarant Dr. Pedram similarly focuses on the absence of disclosure in the '002 patent as supporting the limiting construction advocated by Patent Owner. *See* Ex. 2001 ¶¶ 53–70. Much of this testimony is a description of the operation of asynchronous memories and an explanation that the '002 patent *does not* disclose various components allegedly necessary for an asynchronous memory. *See* Ex. 2001 ¶¶ 55–60, 65–66. The few passages of the '002 patent cited by Dr. Pedram mention a "clock" or "clock signal" but do not support the construction proposed by Patent Owner. Ex. 1001, 1:11–16, 1:64–66, 2:2–12. Thus, we are not persuaded that the intrinsic record's *lack of disclosure* supports Patent Owner's proposed interpretation.

Because the '002 patent is silent on the nature of its "clock signal," Patent Owner relies on the IEEE Dictionary's definition of "clock signal" as "[a] periodic signal used for synchronizing events." PO Resp. 12 (citing Ex. 2002, 9). As Petitioner notes, however, the IEEE Dictionary states that "clock pulse" and "timing pulse" are synonyms for "clock signal." Pet. Reply 6–7 (citing Ex. 2002, 9). This is significant because of the parties' dispute over whether Sato's disclosure of a "timing signal" teaches a "clock

signal." The IEEE Dictionary at least suggests an equivalence between the two terms.

Whether or not the IEEE Dictionary supports Patent Owner's proposed definition of "clock signal," we determine that it is not necessary to construe the term "clock signal" in light of Sato's disclosure. In particular, Sato discloses that "[t]he present invention can be applied widely to semiconductor memory devices having at least a *clocked static type address decoder* and semiconductor devices with built-in semiconductor memory devices of the type described above." Ex. 1005, 12:4–8 (emphasis added). Sato also states that "[t]his invention relates to semiconductor memory devices and to a technique which will be effective when applied, for example, to CMOS (Complementary MOS) static RAMs (Random Access Memories)" and further that "CMOS static RAMs including *clocked static decoders* are known in the art." Ex. 1005, 1:6–11 (emphasis added). Thus, as explained further below, Patent Owner's attempt to narrow the recited "clock signal" to data having certain characteristics so as to avoid Sato's disclosure of a "timing signal" that is allegedly asynchronous fails to differentiate over Sato in any event.

Thus, we determine that it is not necessary to construe the term "clock signal."

2. Means-Plus-Function Limitations

In accordance with 37 C.F.R. § 42.104(b)(3), Petitioner proposes constructions for the following limitations it contends are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6: "means for decoding a first portion of a memory address of a memory array" in claim 11; "means for selectively providing a clock signal to a selected group of wordline

drivers based on the first portion of the memory address [of a memory array]"[5] in claims 11, 27; "means for decoding a second portion of the memory address" in claims 11, 14; "means for activating a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address" in claims 11, 27; and "means for applying the second portion of the memory address to a shared address line" in claim 14. Pet. 5–7.

Patent Owner does not offer its own constructions for any of these limitations, nor does it address Petitioner's proposed constructions. *See* PO Resp. 11–15 (discussing claim construction).

Each of the limitations reproduced above recites "means" and further recites a function, thus creating a presumption that 35 U.S.C. § 112, ¶ 6 applies. *See* 35 U.S.C. § 112, ¶ 6 ("An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."); *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (en banc in relevant part) (holding that "use of the word 'means' creates a presumption that § 112, ¶ 6 applies" (quoting *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 703 (Fed. Cir. 1998))).

We agree with Petitioner that these limitations are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6. We have reviewed the portions of the Specification of the '002 patent cited by Petitioner, and we

[5] Claim 27 includes "of a memory array."

adopt Petitioner's proposals for the structure corresponding to the recited functions. *See* Pet. 5–7.

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Obviousness over Sato (Claims 1–28, 31–37)

Petitioner contends claims 1–28 and 31–37 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Sato. Pet. 2, 9–32, 51–52, 54, 55, 58–60, 63–81.

1. Sato

Like the '002 patent, Sato is directed to wordline drivers for memory. Ex. 1005, codes (54), (57). Figure 3 of Sato is reproduced below.

FIG. 3

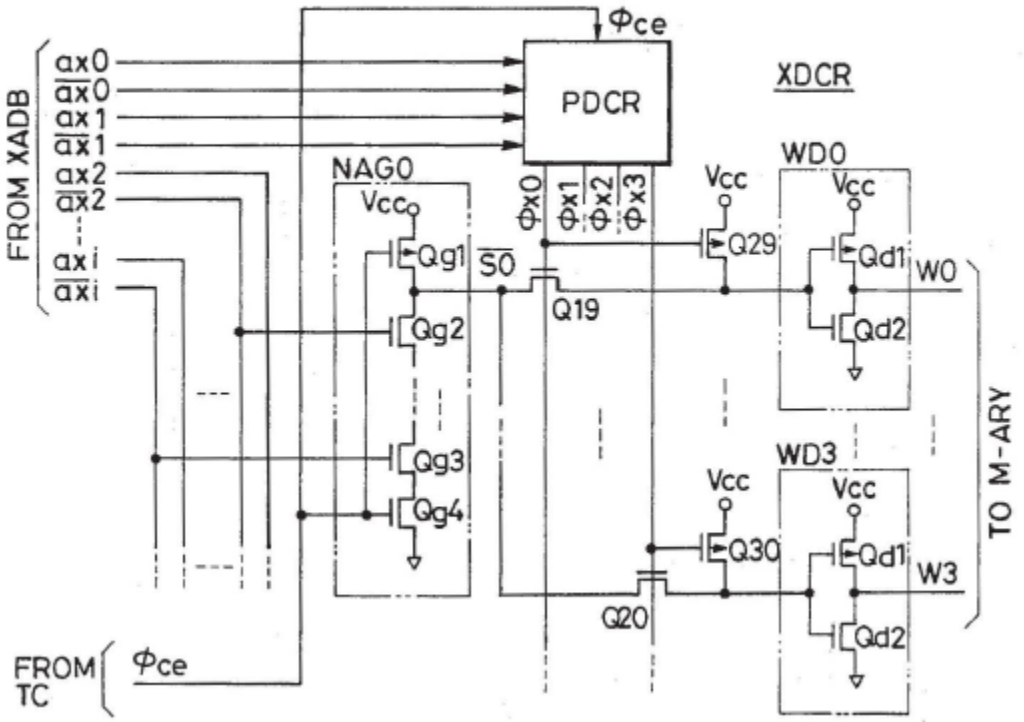


Figure 3 is a diagram of an address decoder in one embodiment. Ex. 1005, 2:57–59. Sato explains that pre-decoder PDCR receives and decodes the lower 2-bit complementary address signals ax0 and ax1. Ex. 1005, 5:16–28. Furthermore, "timing signal ϕce described above is supplied to the pre-decoder PDCR and its output signal, that is, the selection signal ϕx0 ~ ϕx3, is generated in accordance with this timing signal ϕce." Ex. 1005, 10:36–39. Decoding NAND gate circuits, of which only one, NAG0, is shown in Figure 3, are used to decode the remaining address bits to select the appropriate wordline drive circuit. Ex. 1005, 5:43–6:59.

2. Alleged Deficiency of Sato Ground

Patent Owner argues that Petitioner has not set forth a *prima facie* case of obviousness because it has not identified any differences between the claimed subject matter and the prior art and, thus, has not complied with

Graham. PO Resp. 28–30. We disagree. In *Graham*, the Supreme Court stated the following:

> Under § 103, the scope and content of the prior art are to be determined; *differences between the prior art and the claims at issue are to be ascertained*; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy.

383 U.S. at 17–18 (emphasis added).

Petitioner asserts that Sato's "[t]iming signal ϕce represents or renders obvious a clock signal" and explains why a person of ordinary skill in the art would have "viewed the function of the timing signal ϕce as similar to or equivalent to that of a clock signal." Pet. 14–17 (quoting Ex. 1003 ¶ 64). Petitioner presents over two pages of argument explaining how Sato's disclosures relating to its timing signal ϕce teach the recited subject matter pertaining to the "clock signal." *See* Pet. 14–17. The trial record shows that the wording difference between Sato ("timing signal") and the '002 patent ("clock signal") is the pivotal issue raised by Patent Owner in its challenge to the Sato ground. *See* PO Resp. 30–45. Thus, Petitioner's explanation addressing this *difference* in terminology between the prior art and the claims shows that its analysis follows *Graham*.

3. Claim 1

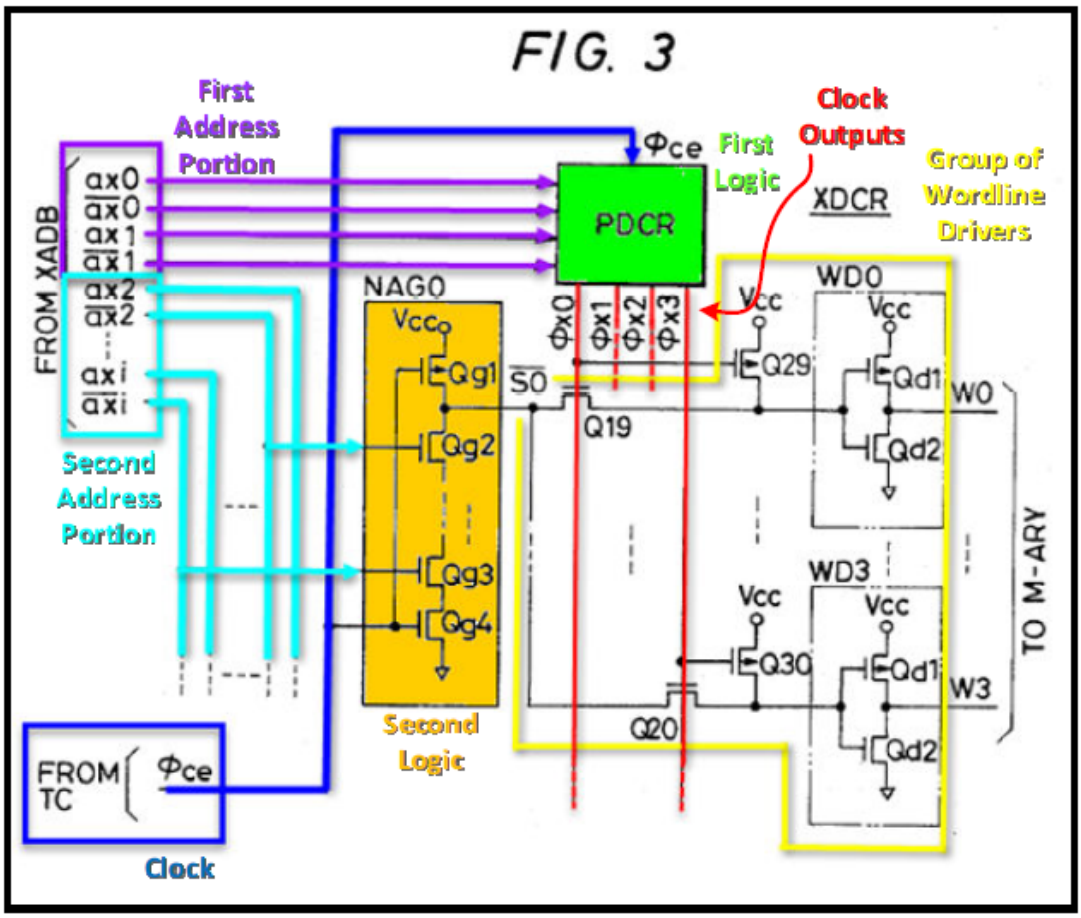
a) First logic

i. Petitioner's contentions

Independent claim 1 is reproduced above and is directed to "[a] circuit device" having

> first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array.

With its obviousness contentions, Petitioner provides the following annotated version of Sato's Figure 3:



Pet. 10. In the annotated version of Sato's Figure 3, Petitioner identifies with color annotations particular components that it contends teach various limitations recited in claim 1. Pet. 10.

Petitioner contends Sato's disclosure of pre-decoder PDCR receiving timing signal ϕce and address signals ax0 and ax1, along with their complements, teaches "first logic to receive a clock signal and a first portion of a memory address of a memory array," as recited in claim 1. Pet. 14 (citing Ex. 1005, 3:9–15, 3:50–59, 4:6–11, 5:16–24, 9:44–54, Fig. 3). Petitioner contends (Pet. 18) Sato teaches "the first logic to decode the first portion of the memory address" because Sato discloses that "pre-decoder PDCR decodes the lower 2-bit complementary internal address signals ax0 and ax1" (Ex. 1005, 5:25–26). Petitioner also contends Sato teaches the first logic "to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array" through its disclosure of PDCR generating selection signals ϕx0 through ϕx3 based on input timing signal ϕce. Pet. 18–23 (citing, *inter alia*, Ex. 1005, 5:25–31, 6:40–55, 9:30–51, 9:52–65, 10:36–39, claim 1, Fig. 3).

ii. Patent Owner's arguments and our analysis

Patent Owner argues Sato does not teach the recited "clock signal" because Sato's timing signal is not "a periodic signal used for synchronization," as Patent Owner proposes to construe the term. PO Resp. 30–44. According to Patent Owner, Sato discloses an asynchronous system whereas the '002 patent discloses a synchronous system. Patent Owner acknowledges that "Sato does not expressly refer to its memory system as being asynchronous" but argues that a person of ordinary skill in

the art "would understand it as such because it is an exact match of the asynchronous systems" Patent Owner describes in its Response. PO Resp. 34 (citing Ex. 2001 ¶ 102). Patent Owner argues that "Sato *does not* suggest that any of the signals ϕce, ϕwe, ϕsa, and ϕoe are periodic, which is consistent with asynchronous systems' use of multiple, non-periodic internal timing signals." PO Resp. 34 (citing Ex. 2001 ¶ 103).

Although Sato may not say that its timing signal is periodic, the '002 patent does not say that the recited "clock signal" is periodic. Rather, Patent Owner attempts to take advantage of the lack of disclosure in its own Specification to support an alleged distinction over the prior art based on a difference in terminology – "timing signal" as opposed to "clock signal."

Regardless of the differences in terminology, Patent Owner's attempted distinction over Sato fails because Sato discloses that its circuit operates with a clock signal as well. In particular, as Petitioner points out (Pet. 15), Sato discloses that "[t]he present invention can be applied widely to semiconductor memory devices having at least a *clocked static type address decoder* and semiconductor devices with built-in semiconductor memory devices of the type described above." Ex. 1005, 12:4–8 (emphasis added); *see also* Pet. 15 (quoting Ex. 1005, 12:4–6). Sato also states that "[t]his invention relates to semiconductor memory devices and to a technique which will be effective when applied, for example, to CMOS (Complementary MOS) static RAMs (Random Access Memories)" and further that "CMOS static RAMs including *clocked static decoders* are known in the art." Ex. 1005, 1:6–11 (emphasis added); *see also* Pet. 15 (quoting Ex. 1005, 1:10–11).

Patent Owner responds to Sato's disclosure of "clocked" circuits as follows:

> The portion of Sato cited by Petitioner merely provides Sato's unexplained, unsupported opinion that his invention can be applied to devices having a clocked static type address decoder in the same way that Sato opines that his invention can also be applied to dynamic RAMs and other semiconductor memory devices.

PO Resp. 43 (citing Ex. 2001 ¶ 118; Ex. 1005, 11:66–12:3). We disagree with Patent Owner. The cited portion of Sato not "unsupported opinion." It is the express disclosure of the prior art, and it moots Patent Owner's argument, which is based entirely on the difference in terminology between "clock signal" and "timing signal." As discussed above, nowhere does the '002 patent describe the nature of its clock signal. Thus, Patent Owner's argument depends solely on the use of the term "clock signal." Sato's disclosure of "a clocked static type address decoder" refutes Patent Owner's attempted semantic distinction. Ex. 1005, 12:4–8.

Patent Owner further argues that "Sato's vague statement about potential uses for its invention does not transform the reference's non-periodic timing signal ϕce into a periodic clock signal." PO Resp. 43–44. As noted above, however, the '002 patent never says that its "clock signal" is periodic. Rather, Patent Owner bases its argument on extrinsic evidence—the IEEE Dictionary—to which Patent Owner resorts based on the word "clock signal" and the *lack of disclosure* in the '002 patent of the nature of that signal. *See* PO Resp. 11–15. Sato's disclosure of "a clocked static type address decoder" demonstrates that Sato teaches a circuit having logic "to receive a clock signal." Whether or not the received clock signal is periodic does not negate Sato's teaching of logic to receive a clock signal.

Patent Owner also argues that Sato does not teach the "clock output" of the claims. PO Resp. 45–47. In particular, Patent Owner argues that "the predecoder PDCR is a black box—Sato provides no disclosure on its internal circuitry" and that, "even if the input signal ϕce to the predecoder PDCR is considered a clock signal, the outputs of the predecoder PDCR are not necessarily clock signals." PO Resp. 47 (citing Ex. 2001 ¶ 76). The evidence, however, shows that Sato's predecoder is not a black box. Referring to the predecoder of Figure 1, which does not receive timing signal ϕce as an input, Sato discloses the following:

> The pre-decoder PDCR decodes the lower 2-bit complementary internal address signals ax0 and axl supplied thereto from the X address buffer XADB and generates selection signals ϕx0 ~ ϕx3. These selection signals ϕx0 ~ ϕx3 are formed selectively in accordance with the complementary internal address signals ax0 and ax1. In other words, the selection signal ϕx0 is set to the high logic level when both the inversed internal address signals $\overline{\text{ax0}}$ and $\overline{\text{ax1}}$ are at the high logic level. Similarly, the selection signals ϕx1, ϕx2 and ϕx3 are set to the high logic level when both the non-inversed internal address signal ax0 and the inversed internal address signal $\overline{\text{ax1}}$ are at the high logic level, when both the inversed internal address signal $\overline{\text{ax0}}$ and non-inversed internal address signal ax1 are at the high logic level and when both the non-inversed internal address signals ax0 and ax1 are at the high logic level, respectively.

Ex. 1005, 5:25–42. For the predecoder of Figure 3, upon which Petitioner relies in its contentions of obviousness, Sato discloses that "[t]he timing signal ϕce described above is supplied to the pre-decoder PDCR and its output signal, that is, the selection signal ϕx0 ~ ϕx3, is generated in accordance with this timing signal ϕce." Ex. 1005, 10:36–39. Thus, Sato

explains how the predecoder works without timing signal ϕce and additionally with timing signal ϕce.

Patent Owner does not dispute that Sato's description of predecoder PDCR in column 5, lines 25–42 applies to the predecoder of Figure 3 as well. Indeed, Patent Owner's declarant, Dr. Pedram, relies on this disclosure to explain the operation of predecoder PDCR of Figure 3. Ex. 2001 ¶¶ 75–76. Dr. Horst, Petitioner's declarant, testifies that "Sato does not provide a diagram the internals of XDCR in Fig. 3, but the text description above [(Ex. 1005, 5:25–42, 9:44–59)] provides enough detail for a [person of ordinary skill in the art] to understand that it performs a function equivalent to four AND gates." Ex. 1003 ¶ 62. Dr. Horst provides the following figure:

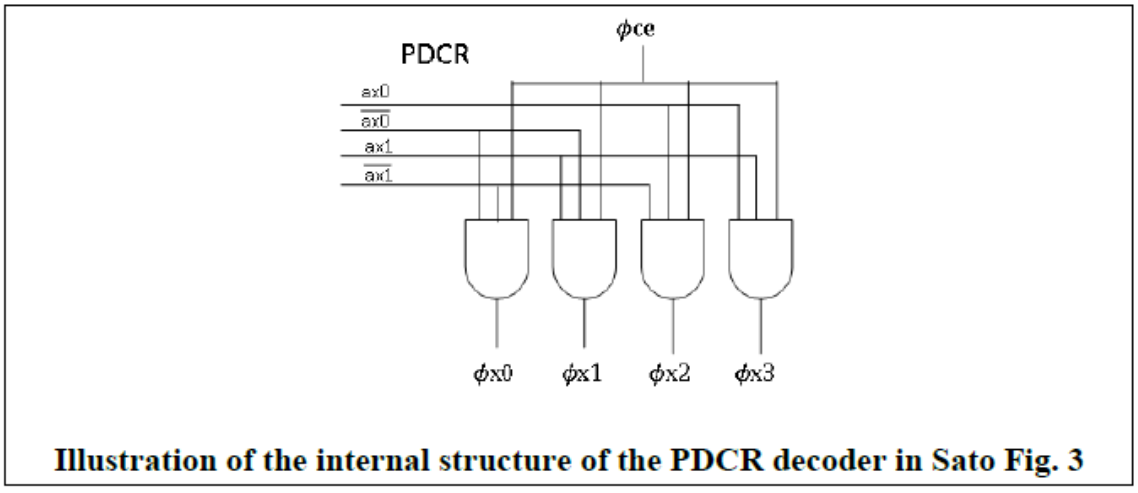


Illustration of the internal structure of the PDCR decoder in Sato Fig. 3

Ex. 1003 ¶ 62. The figure reproduced above is captioned "Illustration of the internal structure of the PDCR decoder in Sato Fig. 3." Ex. 1003 ¶ 62. In support of his testimony, Dr. Horst cites a textbook titled *Fundamentals of Digital Logic with Verilog Design* (Ex. 1009) that shows how a truth table for a decoder is implemented using AND gates and inverters. Ex. 1003 ¶ 63 (citing Ex. 1009, 312 (Fig. 6.16), 315).

In its Sur-reply, Patent Owner again asserts that "Sato's predecoder PDCR is a black box" and argues "that Petitioner's arguments about what the [person of ordinary skill in the art] 'would understand' are based purely on speculation." PO Sur-reply 20 (citing PO Resp. 45–47). We disagree. Dr. Horst's testimony as to how a person of ordinary skill in the art would have understood Sato's predecoder PDCR in Figure 3 is not based on speculation. Rather, it is based on a detailed explanation, and we credit this explanation. *See* Ex. 1003 ¶¶ 60–63. Sato's disclosure at column 5, lines 25–42 lists the address inputs that will result in each of ϕx0, ϕx1, ϕx2, and ϕx3 being at a high logic level, thus providing, in its written description, a truth table. Sato then discloses that "[t]he timing signal ϕce described above is supplied to the pre-decoder PDCR and its output signal, that is, the selection signal ϕx0 ~ ϕx3, is generated in accordance with this timing signal ϕce." Ex. 1005, 10:36–39. Dr. Horst explains that this means that "the value of timing signal ϕce is passed through to the selected output." Ex. 1003 ¶ 63. Based on Sato's disclosure and Dr. Horst's detailed explanation, we find that a person of ordinary skill in the art—a person with an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits—would have readily recognized how Sato's predecoder operates based on Sato's detailed description.

iii. Our findings as to "first logic"

We are persuaded by Petitioner's contentions that Sato teaches the "first logic" recited in claim 1. *See* Pet. 14–23. In particular, we find Sato teaches "first logic to receive a clock signal and a first portion of a memory address of a memory array" because it discloses, with reference to Figure 3,

that predecoder PDCR receives timing signal ϕce and address signals ax0 and ax1, along with their complements, as inputs. Ex. 1005, Fig. 3; *see* Ex. 1005, 5:16–24 (disclosing that PDCR "receives the lower 2-bit complementary internal address signals ax0 and ax1"), 10:36–39 (disclosing that "timing signal ϕce described above is supplied to the pre-decoder PDCR"). More particularly, we find Sato discloses "logic to receive a clock signal" because it discloses that "[t]he present invention can be applied widely to semiconductor memory devices having at least a *clocked static type address decoder*," as discussed in detail above. Ex. 1005, 12:4–8 (emphasis added).

We find Sato teaches "the first logic to decode the first portion of the memory address" by its disclosure that "pre-decoder PDCR decodes the lower 2-bit complementary internal address signals ax0 and ax1." Ex. 1005, 5:25–28, *cited in* Pet. 18. We also find Sato teaches "the first logic . . . to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array." Sato discloses that "[t]he timing signal ϕce described above is supplied to the pre-decoder PDCR and its output signal, that is, the selection signal ϕx0 ~ ϕx3, is generated in accordance with this timing signal ϕce." Ex. 10:36–39. As discussed above, we credit Dr. Horst's detailed explanation of how a person of ordinary skill in the art would have understood the operation of Sato's predecoder PDCR in Figure 3. *See* Ex. 1003 ¶¶ 60–63. Dr. Horst explains that "the values of Sato's address signals (ax0 and ax1) select one of four outputs (ϕx0-ϕx3) and force the non-selected outputs low" and, therefore, that "the value of timing signal ϕce is passed through to the selected

output." Ex. 1003 ¶ 63; *see also* Ex. 2001 ¶ 78 (Patent Owner's declarant Dr. Pedram confirming that "[e]xactly one of the selection signals ϕx0-ϕx3 is active at any time").

We also are persuaded by Petitioner's explanation that Sato's selection signals ϕx0 – ϕx3 are associated with wordline drive circuits WD0 – WD3 associated with the memory array. Pet. 23 (citing Ex. 1005, 6:40–55, 7:32–36; Ex. 1003 ¶¶ 58, 76–78). In particular, Sato discloses that each of selections signals ϕx0 – ϕx3 connects to the gate of one transistor controlling a wordline driver in each group of wordline driver circuits. Ex. 1005, 6:40–55. Sato discloses that "selection signal ϕx0 is supplied in common from the pre-decoder PDCR to the gate of the first MOSFET represented by MOSFETs Q13 and Q15, and the selection signal ϕx3 is supplied in common to the gate of the fourth MOSFET represented by MOSFETs Q14 and Q16" and that, "[s]imilarly, the selection signals ϕx1 and ϕx2 are supplied in common from the pre-decoder PDCR to the gates of the second and third MOSFETs among the four capacitance cut MOSFETs of each set, respectively." Ex. 1005, 6:45–55; *see also* Ex. 1005, 9:60–65 (explaining, with reference to Figure 3, that selections signals ϕx0 – ϕx3 are coupled through transistors to "the corresponding four sets of word line drive circuits WD0 ~ WD3"). Furthermore, Sato discloses that "[w]ord line drive circuits WD ~ WDm are also disposed in such a manner as to correspond to the word lines WD ~ Wm of the memory array M-ARY, respectively." Ex. 1005, 9:48–51.

Based on the foregoing, we find Sato teaches "[a] circuit device" having

> first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array,

as recited in claim 1.

b) Second logic

Claim 1 further recites "second logic to decode a second portion of the memory address, the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address."

Petitioner contends Sato discloses that NAND gate circuits, such as NAG0 in Figure 3, decode the address bits other than those decoded by pre-decoder PDCR, thereby teaching "second logic to decode a second portion of the memory address." Pet. 24–27 (citing, *inter alia*, Ex. 1005, 5:19–22, 5:53–58, 5:66–6:21, 9:44–48, Fig. 3). We are persuaded by this argument, and we find Sato teaches this subject matter because it discloses that its RAM has "k+1 *decoding* NAND gate circuits NAG0 ~ NAGk to which the complementary internal address signals ax2 ~ axi *other than the lower two bits* in respective combinations are supplied." Ex. 1005, 5:19–22 (emphases added); *see also id.* at 9:45–48 (explaining that the Figure 3 "embodiment includes one pre-decoder PDCR and k+1 decoding NAND gate circuits NAG0-NAGk in the same way as in the foregoing embodiments").

Petitioner also contends that Sato teaches "selectively activat[ing] a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address" through its disclosure of activating a particular wordline based on the address signal.

Pet. 27–32 (citing, *inter alia*, Ex. 1005, 5:66–6:21, 6:40–44, 6:55–59, 8:27–32, 9:31–51, 9:60–10:13, 10:36–39, claim 1, Fig. 3). We are persuaded by this argument, and we find Sato teaches this subject matter because Sato discloses that, based on address decoding by the NAND gates in combination with the operation of the PDCR, a selection signal "is transmitted to only the word line drive circuit corresponding to one word line that is designated by the X address signal Ax0 ~ Axi." Ex. 1005, 6:55–59.

c) Determination of unpatentability of claim 1

As discussed above, we find Sato teaches the subject matter recited in claim 1. Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that claim 1 of the '002 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Sato.

4. Dependent Claims 2–6

Claims 2 and 4–6 depend directly from claim 1, and claim 3 depends from claim 2. Petitioner presents persuasive arguments and evidence showing how Sato teaches the subject matter recited in these claims. *See* Pet. 51–52 (claim 2), 54 (claim 3), 55 (claim 4), 58–59 (claim 5), 60–61 and 63–64 (claim 6).

Claim 2 recites "wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output," and claim 3 recites "wherein the conditional clock generator selectively applies the clock signal to the selected clock

output according to the first portion of the memory address." Claim 5 recites "wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output." Petitioner contends Sato's description of PDCR receiving timing signal ϕce and address signals ax0 and ax1 and generating one selection signal ϕx0 – ϕx3, as discussed above with respect to claim 1, teaches the subject matter recited in claims 2, 3, and 5. Pet. 51–52, 54, 58–59; *see* Ex. 1005, 5:28–31, 9:52–59, 10:36–39.

Claim 4 recites "wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address." Petitioner contends that Sato teaches this subject matter through its disclosure that "pre-decoder PDCR decodes the lower 2-bit complementary internal address signals ax0 and ax1" (Ex. 1005, 5:25–26). Pet. 55.

Claim 6 recites "wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input." Petitioner contends Sato discloses four wordline drivers per group, as evidenced by Sato's description of "four sets of word line drive circuits WD0 ~ WD3" (Ex. 1005, 9:60–65). Pet. 60; *see also* Ex. 1005, 6:22–45 (disclosing "(m+l) word line drive circuits WD0~WDm" corresponding to "word lines W0~Wm of the memory array M-ARY" and denoting sets of four word line drive circuits as "WDm-3~WDm"). Petitioner argues that each wordline driver in a group of

wordline drivers shares a common address input based on the selection signal $\overline{S0}$ output from decoding NAND gate NAG0. Pet. 63–64.

Patent Owner does not separately address the additional limitations recited in claims 2–6. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 2–6 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Sato.

5. Independent Claims 7, 11, and 17

Independent claim 7 is directed to "[a] method of selecting a particular wordline of a memory array," and it recites subject matter similar to that recited in claim 1. Petitioner argues Sato teaches the subject matter of claim 7 by referring to its contentions for claim 1. *See* Pet. 65–66. Independent claim 11 is directed to "[a] circuit device" comprising various limitations recited in means-plus-function format, the functions of which correspond to steps recited in method claim 7. Petitioner contends Sato teaches the structure corresponding to the means-plus-function limitations. *See* Pet. 67–70. Independent claim 17 is also directed to "[a] circuit device," and it also recites subject matter similar to that recited in claim 1. Petitioner argues Sato teaches the subject matter of claim 17 by referring to its contentions for claim 1. *See* Pet. 73–78.

Patent Owner does not raise additional arguments concerning these claims but, rather, argues that Petitioner's contentions fail for the reasons addressed above with respect to claim 1. *See generally* PO Resp. 27–47.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that independent claims 7, 11, and 17 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Sato.

6. Dependent Claims 8–10, 12–16, 18, and 19

Claims 8–10 depend from independent claim 7, claims 12–16 depend ultimately from independent claim 11, and claims 18 and 19 depend ultimately from independent claim 17. Petitioner presents persuasive arguments and evidence showing how Sato teaches the subject matter recited in these claims, referring where applicable to previous discussions of similar subject matter recited in other claims. *See* Pet. 66–67 (claims 8–10, referring to discussions of claims 1, 2, 3, and 6), 71–73 (claims 12–16, referring to discussions of claims 1, 2, 3, 6, 7), 78–80 (claims 18 and 19). Below we highlight limitations that are not found in claims previously discussed.

Claim 15 depends from claim 12, which depends from independent claim 11, and recites "wherein the circuit device comprises an integrated circuit." Claim 16 depends from claim 15 and recites "wherein the integrated circuit includes the memory array." Petitioner argues "Sato discloses that the entire RAM circuit of Figure 4, which includes the X address decoder and memory array, is 'formed on one semiconductor substrate such as single crystal silicon by known fabrication technique of CMOS integrated circuits.'" Pet. 72–73 (quoting Ex. 1005, 3:1–6).

Claim 18 depends from independent claim 17 and recites "wherein the selected wordline driver of the group of wordline drivers is in an active

evaluation state wherein other wordline drivers of the group of wordline drivers are in a static precharge state." Claim 19 depends from claim 18 and recites "wherein a state of the wordline driver is determined by the selective application of the clock signal." As to claim 18, Petitioner contends that, in Sato, when "a particular one of the wordline drivers (e.g., WD0) is selected and activated, the selected wordline driver is placed in an active evaluation state by asserting its associated wordline" and that "the non-selected wordline drivers are held at a high precharge voltage (i.e., precharge state)." Pet. 78–79 (citing Ex. 1003 ¶¶ 103–106). As to claim 19, Petitioner contends that, in Sato, "the selective application of input clock signal ϕce to a particular one of PDCR outputs ϕx0-ϕx3 determines which one of the wordline drivers is activated by the active selection signal ($\overline{S0}$ - $\overline{Sk}$)." Pet. 80 (citing Ex. 1003 ¶¶ 72, 103–106).

Patent Owner does not separately address the additional limitations recited in claims 8–10, 12–16, 18, and 19. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 8–10, 12–16, 18, and 19 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Sato.

7. Claims 20–28 and 31–37

Petitioner argues that claims 20–28 and 31–36 recite subject matter addressed with respect to claims 1–7 and 10–14 and that claim 37 recites subject matter addressed in claims 2 and 18, and, therefore, Petitioner contends claims 20–28 and 31–37 are unpatentable for the reasons given for the previously-discussed claims. *See* Pet. 80–81. We have reviewed the

subject matter recited in claims 20–28 and 31–37, and we agree with Petitioner's characterization that these claims recite subject matter found in other claims, which we address above. Patent Owner does not challenge Petitioner's characterization of these claims, nor does Patent Owner separately address these claims. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 20–28 and 31–37 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Sato.

E. Obviousness over Asano and Itoh (Claims 1–17, 20–28, and 31–36)

Petitioner contends claims 1–17, 20–28, and 31–36 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Asano and Itoh. Pet. 2, 33–59, 61–62, 64–78, 80–81.

1. Asano

Like the '002 patent, Asano is directed to wordline drivers for memory. Ex. 1005, codes (54), (57). Figure 2 of Asano is reproduced below.

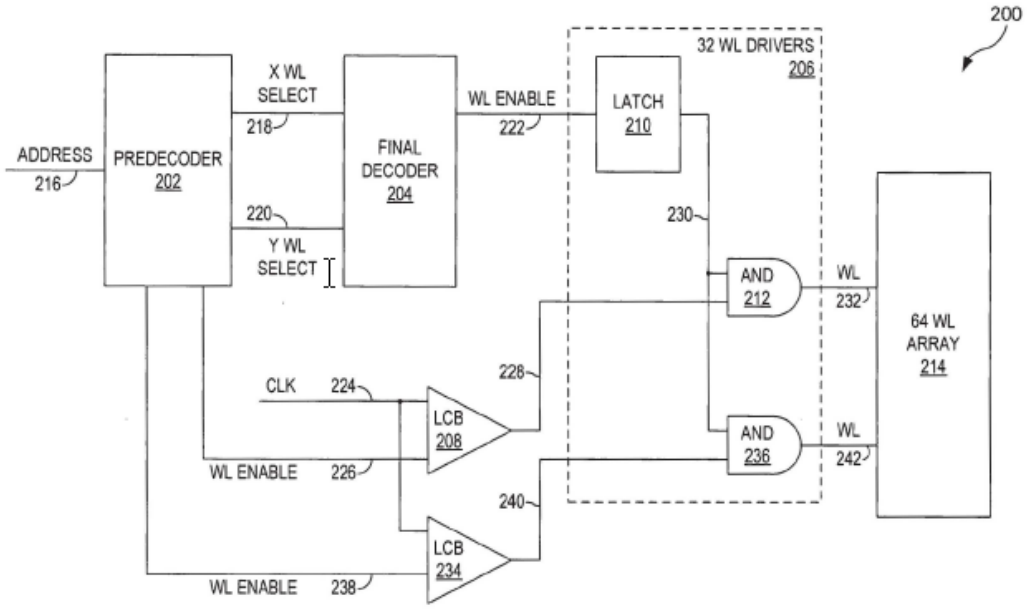


FIG. 2

Figure 2 is a diagram of memory 200 having predecoder 202, final decoder 204, 32 wordline drivers 206, first local clock buffer (LCB) 208, second LCB 234, and 64 wordline array 214. Ex. 1006 ¶ 15. Asano explains that final decoder 204 "determines which of the 32 wordline drivers 206 are to be enabled" and also that predecoder 202 provides a selection signal either to first LCB 208 or second LCB 234 based on the most significant bit of the address. Ex. 1006 ¶¶ 17–19. "By providing selection signals to the LCBs, the last decoding can be delayed until the wordline driver stage." Ex. 1006 ¶ 18. Thus, one of the 32 wordline drivers is selected, and, within each wordline driver, one of the two AND gates 212 and 236 is selected by virtue of the selection of either LCB 208 or LCB 234 based on the most significant bit of the address. Asano explains, therefore, that "[o]ne of the respective AND gates 212 and 236 can then output a

wordline signal in step 318 to a wordline within the 64 wordline array 214." Ex. 1006 ¶ 19.

2. Itoh

Itoh is a textbook on memory design, and, in a chapter on DRAM circuits, it provides examples of predecoding circuits in Figure 3.46, reproduced below.

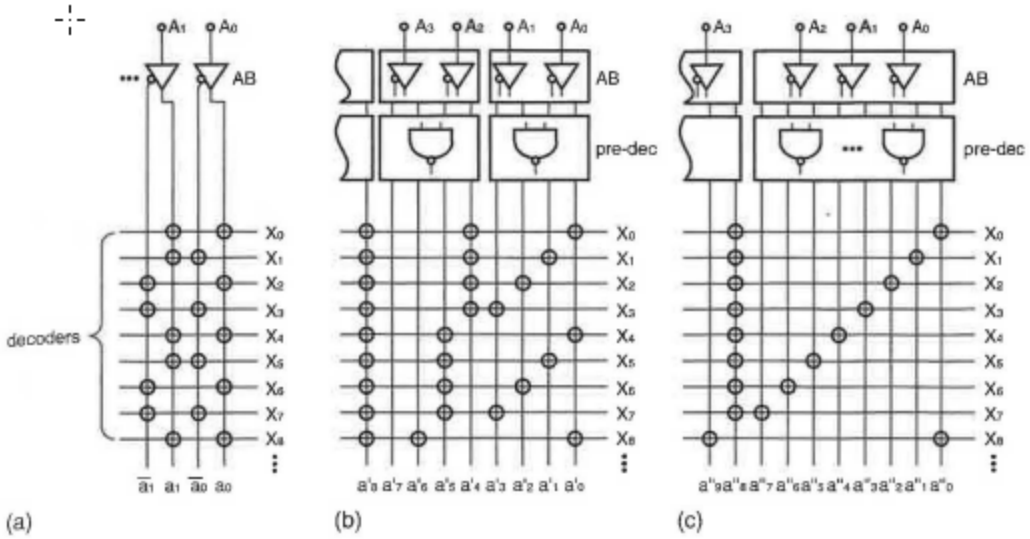


Fig. 3.46. Predecoding [3.4]. (**a**) no predecoding; (**b**) 2-bit predecoding; (**c**) 3-bit predecoding

Figure 3.46 illustrates a 2-bit predecoding circuit and a 3-bit predecoding circuit in (b) and (c), respectively. Ex. 1007, 146–47.

3. Independent Claim 1

a) Petitioner's contentions

With its obviousness contentions, Petitioner provides the following annotated version of Asano's Figure 2:

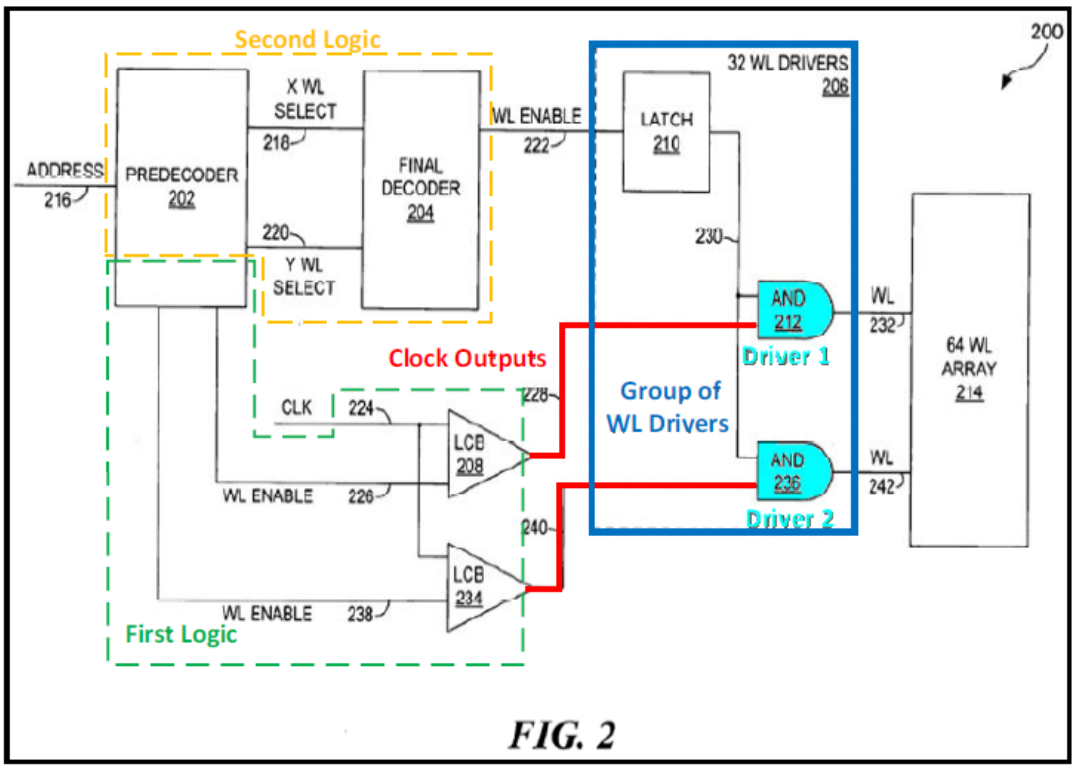


FIG. 2

Pet. 34. In the annotated version of Asano's Figure 2, Petitioner identifies particular components that it contends teach various limitations recited in claim 1. Pet. 34.

Petitioner notes that "Asano represents the predecoder 202 simply using a block element in a block diagram," and Petitioner argues that a person of ordinary skill in the art "would have looked to Itoh's textbook circuits in determining how the internal structure of the predecoder 202 would be built as separate logic sections for decoding different portions of the 6-bit memory address." Pet. 35. Petitioner contends a person of ordinary skill in the art "designing Asano's memory circuit would have naturally turned to a textbook such as Itoh's for details on memory design techniques for a predecoder" and "would have understood that Itoh's individual predecoder circuits would merely perform their intended

functions when implemented in Asano's predecoder 202." Pet. 35 (citing Ex. 1003 ¶¶ 121–123).

Petitioner contends that, in combination with Itoh, Asano's disclosure of LCB 208 and LCB 234, each with a clock input and a selection signal input from predecoder 202 based on the most significant bit of the address, teaches "first logic to receive a clock signal and a first portion of a memory address of a memory array." Pet. 41 (citing Ex. 1006 ¶¶ 16, 19, 21, Fig. 2; Ex. 1003 ¶¶ 117–120, 131). Petitioner contends that, in combination with Itoh, Asano's disclosure that predecoder 202 provides wordline enable signals (or "selection signals," as stated in paragraph 18) to LCB 208 and LCB 234 based on the most significant bit of the address teaches "the first logic to decode the first portion of the memory address." Pet. 42–44 (citing Ex. 1006 ¶¶ 16, 18–21, Fig. 2; Ex. 1003 ¶¶ 115, 117–120, 123). Petitioner contends that providing the clock outputs from either LCB 208 or LCB 234 based on the most significant bit of the address teaches "apply[ing] the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array." Pet. 45–48 (citing, *inter alia*, Ex. 1006 ¶¶ 16–21, Fig. 2; Ex. 1003 ¶¶ 14, 113–118, 132–133).

As to the claimed "second logic," Petitioner contends "Asano's predecoder 202 and final decoder 204 decode five of six address bits (e.g., the second portion) of memory address 216" to produce an 8-bit X wordline select signal and a 4-bit Y wordline select signal. Pet. 48 (citing Ex. 1006 ¶ 16; Ex. 1003 ¶¶ 110–111, 118).

Petitioner argues that "it would have been an obvious design choice for a [person of ordinary skill in the art] to implement Asano's predecoder

using Itoh's three-bit and two-bit predecoders to generate the X and Y wordline select signals," and Petitioner provides an annotated figure showing Asano's predecoder implemented with Itoh's predecoder circuitry. Pet. 48–49 (citing Ex. 1003 ¶¶ 110–111, 118, 122–124). Petitioner contends that Asano's "final decoder decodes the X and Y wordline select signals to determine which of the 32 wordline groups to enable." Pet. 49 (citing Ex. 1006 ¶ 17; Ex. 1003 ¶ 112).

b) Patent Owner's arguments

Patent Owner makes two arguments in response to Petitioner's contentions of obviousness based on the combined teachings of Asano and Itoh. First, Patent Owner argues that Asano does not teach distinct and separate first and second logics. PO Resp. 48–52. Second, Patent Owner argues that Petitioner does not provide a sufficient reason to combine the teachings of Asano and Itoh. PO Resp. 53–57; PO Sur-reply 21–25. We address these arguments below.

i. Separate first and second logics

Patent Owner argues that "[t]he splitting of the memory address into multiple portions and the decoding of the two portions at separate first and second logics are fundamental features of the '002 patent invention." PO Resp. 48. According to Patent Owner, Asano "does not disclose splitting a memory address into first and second portions, nor does it disclose decoding the first and second portions using distinct first and second logics, respectively." PO Resp. 48 (citing Ex. 2001 ¶ 127 (Dr. Pedram testifying similarly)). Patent Owner argues that Asano discloses predecoder 202 as "a single predecoder, not separate first and second decoding logics" and that "Asano contains no teaching or suggestion that the predecoder can or should

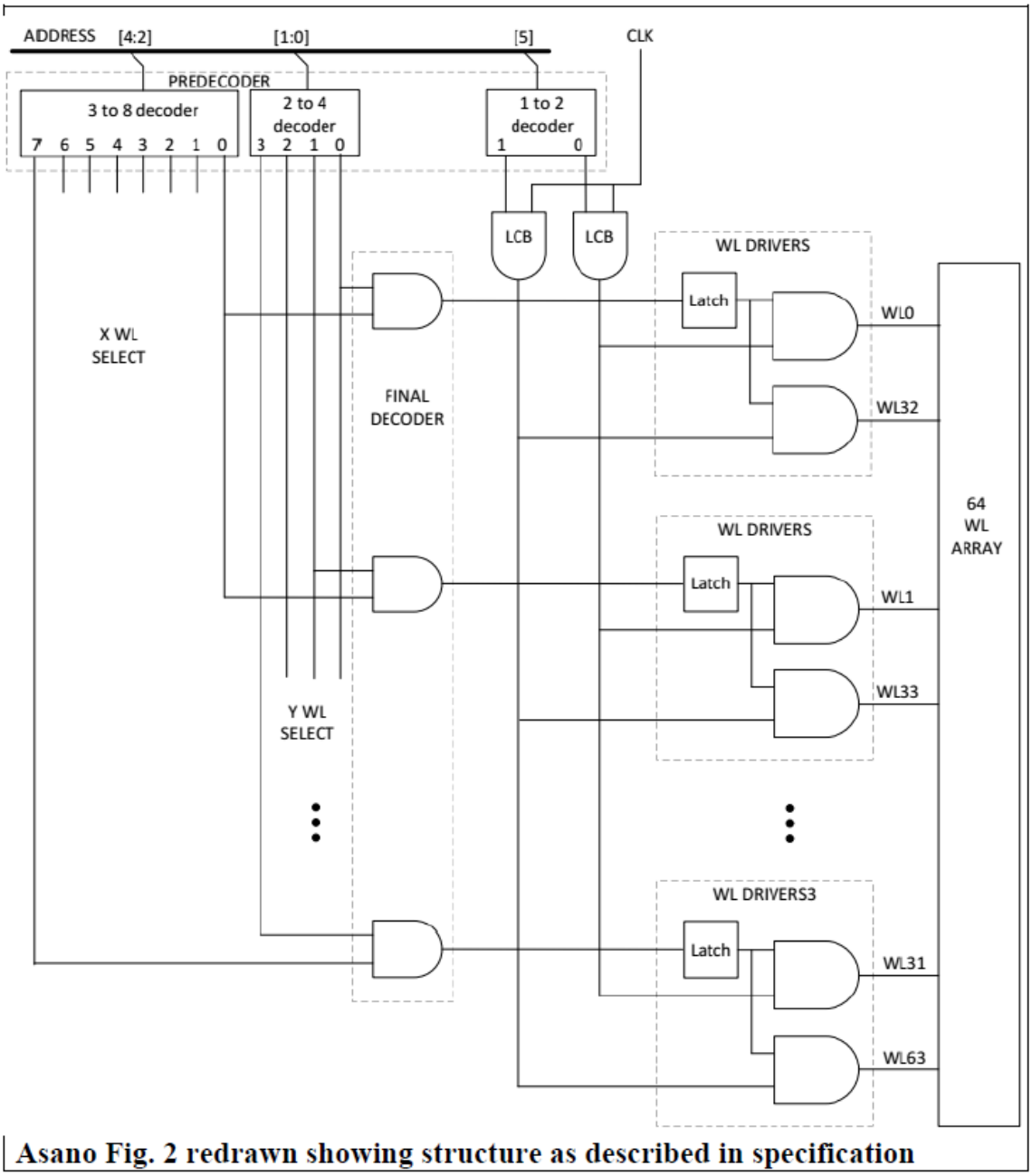
be split into multiple, different decoding logics." PO Resp. 50–51 (citing Ex. 2001 ¶ 127 (Dr. Pedram testifying similarly)). Patent Owner argues that "there is nothing in Asano to suggest that predecoder 202 can or should be implemented using multiple predecoders or multiple decoding logics, as opposed to a single predecoder, as the reference expressly teaches." PO Resp. 52 (citing Ex. 2001 ¶ 129 (Dr. Pedram testifying similarly)).

We disagree with Patent Owner's assertions. Although Asano's Figure 2 shows predecoder 202 as one box, the following passage from Asano's written description details the operation of that predecoder:

> To begin the access cycle for the memory 200, an address is first received in step 302 at the predecoder 202 through a first communication channel 216. Typically, the address is 6 bits long, and from those 6 bits, the predecoder derives a wordline enable signal and two wordline select signals in step 304, an X wordline select signal and a Y wordline select signal. The X wordline select signal is 8 bits long and is output to the final decoder 204 through a second communication channel 218. The Y wordline select signal is output to the final decoder 204 through a third communication channel 220 and is 4 bits long.

Ex. 1006 ¶ 16.

Petitioner's declarant, Dr. Horst, provides the following illustration explaining Asano's Figure 2:



Asano Fig. 2 redrawn showing structure as described in specification

Ex. 1003 ¶ 108. The figure reproduced above is captioned "Asano Fig. 2 redrawn showing structure as described in specification." Ex. 1003 ¶ 108. Citing Asano's disclosure at paragraph 16, Dr. Horst explains that a person of ordinary skill in the art

> would have understood that if the decoded X wordline select signal is 8 bits long, it would come from decoding three bits of

> the address field (e.g. bits 4:2) with a 3-to-8 decoder as shown in the predecoder of redrawn Fig. 2. Similarly, if the Y wordline select signal is 4 bits long, it would come from a 2-to-4 decoder connected to two address bits (e.g. bits 1:0) as shown in the diagram.

Ex. 1008 ¶ 111.

We credit Dr. Horst's testimony because it explains how a person of ordinary skill in the art would have understood Asano's Figure 2 not just from the figure itself but from the accompanying written description as well. *See* Ex. 1003 ¶ 108 ("While Fig. 2 of Asano shows key elements of the '002 patent, there is more information disclosed in the text of Asano. Below, I have redrawn Asano Fig. 2 with added details from the Asano specification."). Contrary to Patent Owner's assertion that Asano "does not disclose splitting a memory address into first and second portions" (PO Resp. 48), Asano discloses that a 6-bit address is used to derive a wordline enable signal, an 8-bit X wordline select signal, and a 4-bit Y wordline select signal (Ex. 1006 ¶ 16). We credit Dr. Horst's testimony that three bits of the 6-bit address would be decoded to derive an 8-bit wordline select signal because 2^3 is 8. *See* Ex. 1003 ¶ 111. Similarly two bits would be decoded to derive a 4-bit wordline select signal because 2^2 is 4. *See* Ex. 1003 ¶ 111. Dr. Horst explains that the remaining bit of the 6-bit address would go to a 1-to-2 decoder to supply the selection signals to the local clock buffers (LCBs) 208 and 234. Ex. 1003 ¶ 115. Asano discloses that "[a] selection signal for the first LCB 208 and for the second LCB 234 are provided by the predecoder 202 through an eighth communication channel 226 and a ninth communication channel 238, respectively." Ex. 1006 ¶ 18.

Based on the foregoing, we disagree with Patent Owner's argument that Asano does not teach first logic and second logic. Rather, the evidence

shows that a person of ordinary skill in the art would have understood that Asano's predecoder 202 takes a 6-bit address and breaks that address into constituent parts, as described in Asano, using different decoders, thus teaching different first and second logics. *See* Ex. 1003 ¶¶ 107–115.

ii. Reason to combine

Patent Owner also argues that Petitioner does not provide a sufficient reason to combine the teachings of Asano and Itoh. PO Resp. 53–57; PO Sur-reply 21–25. Patent Owner argues that "Petitioner has provided no reasons *why* the POSA allegedly would have looked specifically to Itoh." PO Resp. 54 (citing Ex. 2001 ¶ 133 (Dr. Pedram testifying similarly)). Patent Owner argues that, because Itoh discloses "just one of multiple different ways that Asano's predecoder 202 could possibly be implemented," "Petitioner must provide reasons *why* the POSA allegedly would have selected the specific arrangement of three circuits from Itoh instead of the other possible implementations." PO Resp. 54. Patent Owner's arguments, therefore, take issue with Petitioner's selection of particular decoder implementations in Itoh to use in combination with Asano. *See* PO Resp. 56–57.

As discussed above, the evidence shows that a person of ordinary skill in the art would have understood Asano as disclosing the use of separate decoders to take the 6-bit address and break it up into the constituent parts taught in Asano, namely a wordline enable signal and two wordline select signals. Ex. 1006 ¶ 16; Ex. 1003 ¶¶ 107–115. Thus, Asano itself teaches, to a person of ordinary skill in the art, first logic that decodes a first portion of the address and second logic that decodes a second portion of the address. If anything, Petitioner's reliance on Itoh for supplying details on how decoders

would be implemented at the gate level goes beyond what is required. The Supreme Court has stated that "[w]hat matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR*, 550 U.S. at 419. Claim 1 requires "first logic" and "second logic," but it does not specify a particular arrangement of gates necessary to achieve that logic.

Petitioner argues that "Itoh discloses well-known circuits that illustrate a possible implementation of the internal structure for the predecoder 202." Pet. 35 (citing Ex. 1003 ¶¶ 121–122). Patent Owner cites this statement as problematic because it shows that there are many possible ways to implement the claimed logic. PO Resp. 54; *see also* PO Resp. 56 ("Petitioner has provided no explanation or evidence as to why the POSA would have looked to *Itoh's decoding circuits*, specifically, instead of other circuits described in various other textbooks and sources."). We disagree with Patent Owner. Rather, all of this shows that decoding circuits were well-known to and well-understood by persons of ordinary skill in the art at the relevant time. Furthermore, as discussed above, the parties agree that a person of ordinary skill in the art would have had an undergraduate degree in electrical engineering, or a related field, and three years of experience in the design of memory systems and circuits. It is from the standpoint of a person of ordinary skill in the art that the question of obviousness is evaluated. *See* 35 U.S.C. § 103(a).

The Supreme Court has stated that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 416. Petitioner asserts that "the petition sets forth the judicially recognized motivation for

combining the teaching of two references by combining known prior art elements according to known methods to achieve predictable results." Pet. Reply 24 (citing *KSR*, 550 U.S. at 416). We are persuaded that Petitioner has set forth sufficient evidence to support this rationale. As discussed above, Petitioner is relying on Itoh to supply well-known and well-understood circuitry at a level of granularity not even required by the claims. Patent Owner does not dispute that applying Itoh's decoder teachings to Asano would have been within the ability of a person of ordinary skill in the art. *See* Tr. 27:18–21 (Counsel for Patent Owner acknowledging that it is not "beyond the knowledge of a person of ordinary skill in the art to be able to turn to a textbook, a core textbook in the field, and apply it to Asano"). Citing the testimony of Dr. Pedram, Patent Owner argues that "Itoh discloses a specific type of decoder—known as a 'one-hot decoder'—but there are many other ways to implement the decoding functions of Asano's predecoder 202," such as "zero-hot decoders, balanced decoders, and constant-weight decoders are alternative ways of implementing Asano's predecoder 202." PO Resp. 56–57 (citing Ex. 2001 ¶ 136). If anything, this argument and the cited evidence support Petitioner's rationale by showing that Itoh's disclosed decoders are some of the many options a person of ordinary skill in the art would have had for implementing the first and second logic decoding functions. As noted above, the claims do not require any particular implementation for the "first logic" and the "second logic." Nor does the Specification of the '002 patent disclose any particular gate configuration to implement the described decoders. Rather, the '002 patent explains that, "[t]o clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, configurations, modules,

circuits, and steps have been described above generally in terms of their functionality." Ex. 1001, 10:42–45.

c) Findings and conclusions as to claim 1

We are persuaded by Petitioner's contentions that the combination of Asano and Itoh teaches a "circuit device" having

> first logic to receive a clock signal and a first portion of a memory address of a memory array, the first logic to decode the first portion of the memory address and to apply the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array.

See Pet. 36–48. We find Asano's disclosure that "[e]ach of the LCBs 208 and 234 receive a clocking signal through a seventh communication channel 224" (Ex. 1006 ¶ 18) teaches "first logic to receive a clock signal." Asano also discloses that, "[d]epending on the most significant bit of the address signal that is input into the predecoder 202, either the first AND gate 212 or the second AND gate 236 is selected." Ex. 1006 ¶ 19. Dr. Horst testifies that the "'most significant bit' of the memory address . . . selects one LCB when that bit is low and the other LCB when it is high" and that "[d]riving one of two outputs high based on an input bit is the well-known function of a 1-to-2 decoder." Ex. 1003 ¶ 115. Based on this evidence, we find Asano teaches "first logic to receive . . . a first portion of a memory address of a memory array [and] . . . to decode the first portion of the memory address," namely the most significant bit of the address.

Petitioner also notes that Asano discloses using more than one bit for LCB selections. *See* Pet. 43–44 (citing Ex. 1006 ¶ 21; Ex. 1003 ¶¶ 117–120). Asano discloses the following: "Additionally, for the purposes of illustration, 1 bit has been utilized for LCB selections. It is possible to have

2 or more LCB selections up to N bits. In each case, there will be 2^N LCBs each with a reduced load of 2^{-N}." Ex. 1006 ¶ 21. Dr. Horst provides detailed testimony explaining that a 2-to-4 decoder would be used if two bits of the address were used for LCB selections. Ex. 1003 ¶¶ 117–119. We credit this testimony because it is consistent with Asano's disclosure that 2^N LCBs are required for N bits (Ex. 1006 ¶ 21), and, therefore, setting N equal to 2 would mean that 4 (2^2) LCBs would be required, which itself would require a 2-to-4 decoder to select each of the 4 LCBs. Although claim 1 does not require the first portion of the address to be longer than one bit, dependent claim 4 and independent claim 23 recite "decod[ing] at least two address bits to determine the first portion of the memory address."

Petitioner contends that providing the clock outputs from either LCB 208 or LCB 234 based on the most significant bit of the address teaches "apply[ing] the clock signal to a selected clock output of a plurality of clock outputs associated with a selected group of a plurality of wordline drivers that are associated with the memory array." Pet. 45–48 (citing, *inter alia*, Ex. 1006 ¶¶ 16–21, Fig. 2; Ex. 1003 ¶¶ 14, 113–118, 132–133). We are persuaded by Petitioner's argument and evidence. Referring to Figure 2, Asano discloses that there are 32 wordline drivers 206, each of which drives two wordlines. Ex. 1006 ¶¶ 15, 19. Asano discloses that, "for the 64 wordline array 214, there are 32 drivers" such that "every two of the wordlines within the array 214 has an associated driver." Ex. 1006 ¶ 19. Figure 2 depicts one instance of the 32 wordline drivers. *See* Ex. 1006 ¶ 19 ("For the sake of illustration, a single latch 210, first AND gate 212, and a second AND gate 236 are depicted."). Asano further discloses that, "[d]epending on the most significant bit of the address signal that is input

into the predecoder 202, either the first AND gate 212 or the second AND gate 236 is selected, wherein the clocking signal is ANDed with the output of the latch 210 in steps 314 and 316." Ex. 1006 ¶ 19. Asano also discloses that "[t]he first AND gate 212 receives a clocking signal from the first LCB 208 through the fifth communication channel 228, while the second AND gate 236 receives a clocking signal from the second LCB 234 through the sixth communication channel 240." Ex. 1006 ¶ 19. Dr. Horst explains that Asano's LCBs "perform an AND function by passing the clock signal through (when the enable is high) and forcing the output low (when the enable is low)." Ex. 1003 ¶ 113. Thus, Asano teaches that the clock signal is applied to a selected one of the clock outputs by disclosing that one of the two AND gates 212 and 236 will be selected from the output of LCBs 208 and 234 at any given time based on the most significant bit of the address. Furthermore, the clock outputs from LCBs 208 and 234 are associated with the group of two wordline drivers depicted as 206 in Figure 2, and Asano discloses that there are 32 such groups of wordline drivers. *See* Ex. 1006 ¶ 19 ("Within the modified memory 200, every two of the wordlines within the array 214 has an associated driver."). Therefore, we find Asano teaches that the "plurality of clock outputs [are] associated with a selected group of a plurality of wordline drivers that are associated with the memory array."

As to the claimed "second logic," Petitioner contends "Asano's predecoder 202 and final decoder 204 decode five of six address bits (e.g., the second portion) of memory address 216" to produce an 8-bit X wordline select signal and a 4-bit Y wordline select signal. Pet. 48 (citing Ex. 1006 ¶ 16; Ex. 1003 ¶¶ 110–111, 118). We are persuaded by this contention because, as discussed above, Asano discloses this in paragraph 16. *See*

Ex. 1003 ¶¶ 108–111 (explaining how paragraph 16 of Asano discloses deriving X and Y wordline enable signals by decoding 5 of the 6 address bits). Thus, we find that Asano teaches "second logic to decode a second portion of the memory address."

As to the limitation of claim 1 reciting "the second logic to selectively activate a particular wordline driver of the selected group of wordline drivers according to the second portion of the memory address," Petitioner argues the following:

> Asano discloses that the final decoder (part of the second logic–orange below) "determines which of the 32 wordline drivers 206 are to be enabled" and communicates the WL enable signal (orange line) to the appropriate group of wordline drivers (blue outline). APPLE-1006, [0017]; APPLE-1003, ¶¶119, 134. The WL enable signal is latched and output to both AND gate wordline drivers (light blue) in the group. APPLE-1006, [0019]. "Either the first AND gate 212 or the second AND gate 236" wordline driver "is selected [when] the clocking signal is ANDed with the output of the latch." APPLE-1006, [0019]. The output of the latch is the WL enable signal. Finally, the selected AND gate wordline driver can then "output a wordline signal in step 318 to a wordline within the 64 wordline array." APPLE-1006, [0019].

Pet. 50; *see also* Pet. 51 (annotated version of Asano's Figure 2). We are persuaded by this explanation because it is supported by the disclosure of Asano. As discussed above, Asano discloses deriving X and Y wordline enable signals from 5 of the 6 address bits. Ex. 1006 ¶ 16. Asano discloses that, "[o]nce the X wordline select signal and the Y wordline select signal have been transmitted to the final decoder 204, the final decoder 204 in step 306 determines which of the 32 wordline drivers 206 are to be enabled." Ex. 1006 ¶ 17. Asano further discloses the following:

> Depending on the most significant bit of the address signal that is input into the predecoder 202, either the first AND gate 212 or the second AND gate 236 is selected, wherein the clocking signal is ANDed with the output of the latch 210 in steps 314 and 316. One of the respective AND gates 212 and 236 can then output a wordline signal in step 318 to a wordline within the 64 wordline array 214 through an eleventh communication channel 232 or a twelfth communication channel 242, respectively.

Ex. 1006 ¶ 19. Thus, Asano discloses that one of the 32 groups of wordline drivers is selected based on five of the address bits ($2^5 = 32$) and then, within the selected group, the particular wordline is activated based on the clock signal applied by the "first logic" discussed above.

Petitioner relies on Itoh for details on a particular gate implementation for the decoding logic in Asano. *See* Pet. 35, 37–41, 42–44, 48–49. As discussed above, the claims do not require any particular implementation for the "first logic" and the "second logic." As also discussed above, we are persuaded Petitioner has demonstrated that implementing the decoding logic of Asano using the particular gate implementations of Itoh would have been nothing more than "combining the teaching of two references by combining known prior art elements according to known methods to achieve predictable results." *See* Pet. Reply 24.

In sum, we find the combination of Asano and Itoh teaches the subject matter recited in claim 1, and we find Petitioner has set forth articulated reasoning underpinned by evidence in the record to support the combination. As noted above, Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims. Having considered the full record developed during trial, we determine that Petitioner has proven by a preponderance of the evidence that

claim 1 of the ’002 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Asano and Itoh.

4. Dependent Claims 2–6

Claims 2 and 4–6 depend directly from claim 1, and claim 3 depends from claim 2. Petitioner presents persuasive arguments and evidence showing how the combination of Asano and Itoh teaches the subject matter recited in these claims. *See* Pet. 52–54 (claim 2), 55 (claim 3), 55–57 (claim 4), 58–59 (claim 5), 61–62 and 64–65 (claim 6).

Claim 2 recites “wherein the first logic comprises a conditional clock generator to receive the clock signal and to selectively apply the clock signal to the selected clock output,” and claim 3 recites “wherein the conditional clock generator selectively applies the clock signal to the selected clock output according to the first portion of the memory address.” Petitioner contends “Asano’s LCBs work to [sic] together to generate a conditional clock, and thus represent a conditional clock generator like conditional clock generator 110 described in the ’002 patent.” Pet. 52 (citing Ex. 1006 ¶¶ 18–20, claims 7, 11, Fig. 2; Ex. 1003 ¶¶ 131, 135).

Claim 4 recites “wherein the first logic comprises a decoder to decode at least two address bits to determine the first portion of the memory address.” Claim 5 recites “wherein the first logic generates four conditional clock outputs, wherein one of the four conditional clock outputs is active at a time, the first logic to apply the one conditional clock output as the selected clock output.” Claim 6 recites “wherein the selected group of wordline drivers comprises four wordline drivers, each of the four wordline drivers is associated with a respective wordline of the memory array, wherein the four wordline drivers share a common address input.” For these claims,

Petitioner relies on Asano's disclosure of using additional bits, such as two bits, for LCB selection. Pet. 55 (citing Ex. 1006 ¶ 21), 58, 61–62. As noted above, Asano discloses the following: "Additionally, for the purposes of illustration, 1 bit has been utilized for LCB selections. It is possible to have 2 or more LCB selections up to N bits. In each case, there will be 2^N LCBs each with a reduced load of 2^{-N}." Ex. 1006 ¶ 21. Petitioner explains how the combination of Asano and Itoh teaches the subject matter of these claims when N is set to 2 such that there are 4 (2^2) LCBs. Pet. 55–59, 61–62, 64–65.

Patent Owner does not separately address the additional limitations recited in claims 2–6. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 2–6 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Asano and Itoh.

5. Independent Claims 7, 11, and 17

Independent claim 7 is directed to "[a] method of selecting a particular wordline of a memory array," and it recites subject matter similar to that recited in claim 1. Petitioner argues the combination of Asano and Itoh teaches the subject matter of claim 7 by referring to its contentions for claim 1. *See* Pet. 66. Independent claim 11 is directed to "[a] circuit device" comprising various limitations recited in means-plus-function format, the functions of which correspond to steps recited in method claim 7. Petitioner contends the combination of Asano and Itoh teaches the structure corresponding to the means-plus-function limitations. *See* Pet. 67–70.

Independent claim 17 is also directed to "[a] circuit device," and it also recites subject matter similar to that recited in claim 1. Petitioner argues the combination of Asano and Itoh teaches the subject matter of claim 17 by referring to its contentions for claim 1. *See* Pet. 73–78.

Patent Owner does not raise additional arguments concerning these claims but, rather, argues that Petitioner's contentions fail for the reasons addressed above with respect to claim 1. *See generally* PO Resp. 47–57.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that independent claims 7, 11, and 17 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Asano and Itoh.

6. Dependent Claims 8–10 and 12–16

Claims 8–10 depend from independent claim 7, and claims 12–16 depend ultimately from independent claim 11. Petitioner presents persuasive arguments and evidence showing how the combination of Asano and Itoh teaches the subject matter recited in these claims, referring where applicable to previous discussions of similar subject matter recited in other claims. *See* Pet. 66–67 (claims 8–10, referring to discussions of claims 1, 2, 3, and 6), 71–73 (claims 12–16, referring to discussions of claims 1, 2, 3, 6, 10). Below we highlight limitations that are not found in claims previously discussed.

Claim 15 depends from claim 12, which depends from independent claim 11, and recites "wherein the circuit device comprises an integrated circuit." Claim 16 depends from claim 15 and recites "wherein the integrated circuit includes the memory array." Petitioner argues "Asano

states that 'all functions described herein may be performed in either hardware or software' including by 'integrated circuits.'" Pet. 73 (quoting Ex. 1006 ¶ 14).

Patent Owner does not separately address the additional limitations recited in claims 8–10 and 12–16. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 8–10 and 12–16 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Asano and Itoh.

7. Claims 20–28 and 31–36

Petitioner argues that claims 20–28 and 31–36 recite subject matter addressed with respect to claims 1–7 and 10–14, and, therefore, Petitioner contends claims 20–28 and 31–36 are unpatentable for the reasons given for the previously-discussed claims. *See* Pet. 81. We have reviewed the subject matter recited in claims 20–28 and 31–36, and we agree with Petitioner's characterization that these claims recite subject matter found in other claims, which we address above. Patent Owner does not challenge Petitioner's characterization of these claims, nor does Patent Owner separately address these claims. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 20–28 and 31–36 of the '002 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Asano and Itoh.

III. PETITIONER'S MOTION TO EXCLUDE EXHIBIT 2004

Federal Rule of Evidence 801(c) provides the following: "'Hearsay' means a statement that: (1) the declarant does not make while testifying at the current trial or hearing; and (2) a party offers in evidence to prove the truth of the matter asserted in the statement." Federal Rule of Evidence 802 states that "[h]earsay is not admissible unless" allowed by "a federal statute," the Federal Rules of Evidence, or "other rules prescribed by the Supreme Court." The Federal Rules of Evidence apply to this proceeding. 37 C.F.R. § 42.62.

Exhibit 2004 is a declaration of Dr. Donald Alpert from IPR2015-00148 submitted by the petitioner Xilinx, Inc. in that proceeding. Petitioner moved to exclude Exhibit 2004 as inadmissible hearsay, among other reasons. Paper 19, 5–7. Petitioner argues that "Exhibit 2004 should be excluded under Rule 802 as hearsay because Exhibit 2004 is a statement made outside of this proceeding and relied upon by Patent Owner to prove the truth of the matter asserted in Exhibit 2004" and, in particular, that "Patent Owner relies on portions of Exhibit 2004 to support its construction of the term 'clock signal.'" Paper 19, 5.

Patent Owner responds that it offers the testimony in Exhibit 2004, not "for what it describes" or "for the truth of its disclosures," but as "evidence that [Patent Owner's] reliance on the IEEE dictionary definition would not be unreasonable to a POSA, as Dr. Alpert relied on the same definition for a similar term." Paper 21, 2. In its Response, however, Patent Owner argues the following:

> Petitioner's expert in the related ITC proceeding involving the '002 patent, Dr. Donald Alpert, previously provided relevant testimony. Specifically, in another IPR proceeding not directed

> to the '002 patent, but addressing the meaning of the claim term "clock," Dr. Alpert told the Board that the term "clock" should be interpreted as "a periodic signal used for synchronization." Ex. 2004 at 3–4. Dr. Alpert stated that the "definition ['a periodic signal used for synchronization'] is consistent with the broadest reasonable interpretation of the term ['clock']." *Id.* Dr. Alpert's statement provides further support for Qualcomm's proposed construction.

PO Resp. 14–15. This passage shows that Patent Owner is relying on Dr. Alpert's testimony for the truth of the matter asserted, namely Dr. Alpert's definition of "clock." Thus, this testimony is hearsay because Dr. Alpert does not offer the testimony while testifying at the current trial or hearing. *See* FED. R. EVID. 801(c). Patent Owner does not argue that this testimony falls under an exception to the rule against hearsay.

Based on the foregoing, we exclude Exhibit 2004 as hearsay. We further note that we discuss the IEEE dictionary definition of "clock signal" in our claim construction discussion above. Therefore, there is no need for Dr. Alpert's testimony to show the propriety of relying on the IEEE dictionary, as Patent Owner argues in its opposition to the motion. *See* Paper 21, 2. Indeed, Petitioner cites the IEEE dictionary definition of "clock signal" as well. Pet. Reply 6–7.

IV. CONCLUSION[6]

For the reasons discussed above, we determine Petitioner has proven, by a preponderance of the evidence, that the challenged claims are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	Reference(s)	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–28, 31–37	103(a)	Sato	1–28, 31–37	
1–17, 20–28, 31–36	103(a)	Asano, Itoh	1–17, 20–28, 31–36	
Overall Outcome			1–28, 31–37	

[6] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–28 and 31–37 of the ’002 patent have been shown to be unpatentable;

FURTHERED ORDERED that Exhibit 2004 is excluded; and

FURTHERED ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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