UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION

Petitioner,

v.

QUALCOMM INCORPORATED

Patent Owner.

IPR2018-01334[1]
U.S. Patent No. 8,838,949

PETITIONER'S NOTICE OF APPEAL

[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

Pursuant to 35 U.S.C. §§ 141-144 and 319, and 37 C.F.R. § 90.2-90.3, notice is hereby given that Petitioner Intel Corporation appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered March 16, 2020 (Paper 30) in IPR2018-01334, attached as Exhibit A, and all prior and interlocutory rulings related thereto or subsumed therein.

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Petitioner indicates that the issues for appeal include the holding that claims 1-9, 12, 16, and 17 are not unpatentable, the construction of "hardware buffer," the Board's decision not to evaluate the obviousness of claims 16 and 17 in view of the asserted prior art, any finding or determination supporting or related to those issues, and all other issues decided adversely to Petitioner in any orders, decisions, rulings, and opinions.

Pursuant to 37 C.F.R. § 90.3, this Notice of Appeal is timely, having been duly filed within 63 days after the date of the Final Written Decision.

A copy of this Notice of Appeal is being filed simultaneously with the Patent Trial and Appeal Board, the Clerk's Office for the United States Court of Appeals for the Federal Circuit, and the Director of the U.S. Patent and Trademark Office.

Respectfully submitted,

Dated: May 15, 2020

/Thomas E. Anderson/
Thomas E. Anderson
Registration No. 37,063

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 90.2(a)(1) and 104.2(a), I hereby certify that, in addition to being filed electronically through the Patent Trial and Appeal Board's End to End (PTAB E2E) system, a true and correct original version of the foregoing PETITIONER'S NOTICE OF APPEAL is being filed by Express Mail on this 15th day of May, 2020, with the Director of the United States Patent and Trademark Office, at the following address:

> Office of the General Counsel
> United States Patent and Trademark Office
> P.O. Box 1450
> Alexandria, VA 22313-1450

Pursuant to 37 C.F.R. § 90.2(a)(2) and Federal Circuit Rule 15(a)(1), and Rule 52(a),(e), I hereby certify that a true and correct copy of the foregoing PETITIONER'S NOTICE OF APPEAL is being filed in the United States Court of Appeals for the Federal Circuit using the Court's CM/ECF filing system on this 15th day of May, 2020, and the filing fee is being paid electronically using pay.gov.

I hereby certify that on May 15, 2020, I caused a true and correct copy of the PETITIONER'S NOTICE OF APPEAL to be served via electronic mail, as previously agreed by the parties, on the following counsel for Patent Owner:

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Exhibit A

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

———————————

INTEL CORPORATION,
Petitioner,

v.

QUALCOMM INCORPORATED,
Patent Owner.

———————————

IPR2018-01334[1]
Patent 8,838,949 B2

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Before TREVOR M. JEFFERSON, DANIEL J. GALLIGAN, and
AARON W. MOORE, *Administrative Patent Judges.*

GALLIGAN, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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[1] IPR2018-01335 and IPR2018-01336 have been consolidated with the instant proceeding.

I. INTRODUCTION

In this *inter partes* review, Intel Corporation ("Petitioner") challenges the patentability of all claims (1–23) of U.S. Patent No. 8,838,949 B2 ("the '949 patent," Ex. 1001), which is assigned to Qualcomm Incorporated ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 10, 11, 13–15, and 18–23 are unpatentable but that Petitioner has not proven by a preponderance of the evidence that claims 1–9, 12, 16, and 17 are unpatentable. *See* 35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. *Procedural History*

On July 3, 2018, Petitioner filed three petitions challenging claims of the '949 patent as follows: IPR2018-01334 (claims 1–9, 22, and 23), IPR2018-01335 (claims 10–17), and IPR2018-01336 (claims 18–21). In each proceeding, Patent Owner filed a Preliminary Response. Paper 7 (in each proceeding). We instituted review in each case on all grounds presented, which are as follows:

Claims Challenged	35 U.S.C. §[2]	References
1–15, 22, 23	103(a)	Bauer,[3] Svensson,[4] Kim[5]
16, 17	103(a)	Bauer, Svensson, Kim, Zhao[6]
18–21	103(a)	Bauer, Svensson, Kim, Lim[7]

IPR2018-01334, Paper 10 ("Dec. on Inst."), 29; IPR2018-01335, Paper 10 ("1335 Dec. on Inst."),[8] 38; IPR2018-01336, Paper 10 ("1336 Dec. on Inst."), 32.

After institution, we consolidated IPR2018-01335 and IPR2018-01336 with IPR2018-01334 and terminated IPR2018-01335 and IPR2018-01336. Paper 12.

During the trial, Patent Owner filed a Response (Paper 16, "PO Resp."), Petitioner filed a Reply (Paper 21, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 25, "PO Sur-reply").

An oral hearing was held on December 12, 2019, a transcript of which appears in the record. Paper 29 ("Tr.").

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[2] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 103 and 112 that became effective after the filing of the application for the '949 patent. Therefore, we apply the pre-AIA versions of these sections.

[3] US 2006/0288019, published Dec. 21, 2006 (Ex. 1009).

[4] US 7,356,680 B2, issued Apr. 8, 2008 (Ex. 1010).

[5] Korean Patent Application Publication No. 10-2002-0036354, published May 16, 2002 (Ex. 1011). References to Kim in this Decision are to the English translation provided by Petitioner as Exhibit 1012.

[6] US 2007/0140199 A1, published June 21, 2007 (Ex. 1013).

[7] US 7,203,829 B2, published Apr. 10, 2007 (Ex. 1014).

[8] We use prefixes "1335" and "1336" to denote papers from IPR2018-01335 and IPR2018-01336, respectively. We do not use a prefix for papers from IPR2018-01334.

B. Real Parties in Interest

Petitioner identifies itself and Apple Inc. as real parties in interest. Pet. 2. Patent Owner identifies itself as the real party in interest. Paper 4, 2.

C. The '949 Patent and Illustrative Claim

The '949 patent generally relates to loading software from one processor to another in a multi-processor system. Ex. 1001, code (57). One example disclosed in the '949 patent involves loading modem image executable data by first retrieving and processing an image header, which "includes information used to identify where the modem image executable data is to be eventually placed into the system memory of the secondary processor." Ex. 1001, 8:9–21. Figure 3 of the '949 patent is reproduced below.
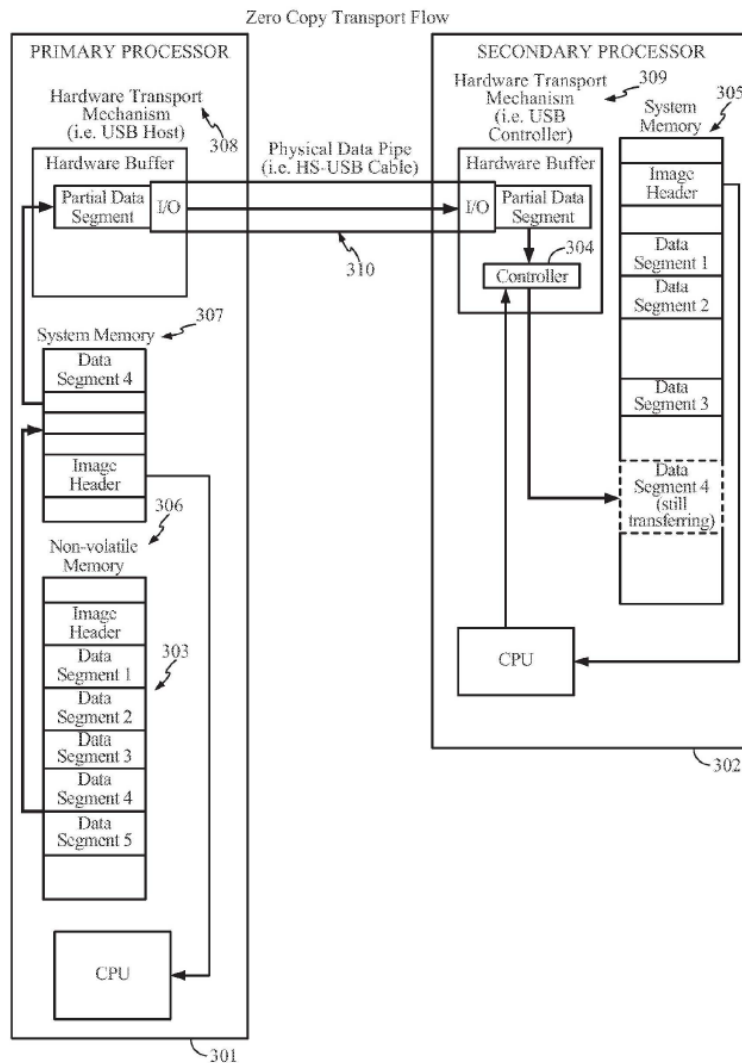
FIG. 3

Figure 3 shows "operational flow for an exemplary loading process for loading an executable image from a primary processor to a secondary processor according to one aspect of the present disclosure." Ex. 1001, 4:10–13. Referring to various components depicted in Figure 3, the '949 patent discloses the following:

> The header information is used by the secondary processor 302 to program the scatter loader/direct memory access controller 304 receive address when receiving the actual executable data. Data segments are then sent from system memory 307 to the primary hardware transport mechanism 308. The segments are

then sent from the hardware transport mechanism 308 of the primary processor 301 to a hardware transport mechanism 309 of the secondary processor 302 over an inter-chip communication bus 310 (e.g., a HS-USB cable.) The first segment transferred may be the image header, which contains information used by the secondary processor to locate the data segments into target locations in the system memory of the secondary processor 305. The image header may include information used to determine the target location information for the data.

Ex. 1001, 8:21–35.

Claims 1, 10, 16, 18, 20, and 22 are independent claims. Claims 1, 10, and 16 are reproduced below.

1. A multi-processor system comprising:
    a secondary processor comprising:
        system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image, the image header and each data segment being received separately, and
            a scatter loader controller configured:
                to load the image header; and
                to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory;
    a primary processor coupled with a memory, the memory storing the executable software image for the secondary processor; and
        an interface communicatively coupling the primary processor and the secondary processor, the executable software image being received by the secondary processor via the interface.

10. A method comprising:
        receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor

that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;

processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment;

receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment; and

scatter loading, by the secondary processor, each data segment [directly[9]] to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header.

16. An apparatus comprising:

means for receiving at a secondary processor, from a primary processor via an inter-chip communication bus, an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment, the image header and each data segment being received separately;

means for processing, by the secondary processor, the image header to determine at least one location within system memory to which the secondary processor is coupled to store each data segment;

means for receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment; and

means for scatter loading, by the secondary processor, each data segment directly to the determined at least one location

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[9] The issued patent recites "reedy," which appears to be a printing error. The April 30, 2014 claim listing submitted by the applicants during prosecution states "directly."

within the system memory, and each data segment being scatter
loaded based at least in part on the processed image header.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner offers the following assessment as to the level of ordinary
skill in the art:

> A person of ordinary skill in the art (POSITA) of the '949
> patent would have had a Master's degree in Electrical
> Engineering, Computer Engineering or Computer Science plus
> at least two years of experience in mobile device architecture and
> multi-processor systems, or a Bachelor's degree in one of those
> fields plus at least four years of experience in mobile device
> architecture and multiprocessor systems.

Pet. 16 (citing Ex. 1002 ¶ 74; Ex. 1007, 11–13). Patent Owner states that it
"accepts Petitioner's proposed education and experience level of one of
ordinary skill in the art." PO Resp. 21.

We determine that the parties' agreed level of skill in the art is
appropriate in view of the evidence of record, with the exception of the
language "at least," which is vague because it expands the range indefinitely
without an upper bound. Thus, we determine that a person of ordinary skill
in the art would have had a Master's degree in Electrical Engineering,
Computer Engineering, or Computer Science plus two years of experience in
mobile device architecture and multi-processor systems, or a Bachelor's
degree in one of those fields plus four years of experience in mobile device
architecture and multiprocessor systems.

B. Claim Interpretation

In an *inter partes* review for a petition filed before November 13,
2018, a claim in an unexpired patent shall be given its broadest reasonable

construction in light of the Specification of the patent in which it appears. 37 C.F.R. § 42.100(b) (2018); *see* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)). The Petition was accorded a filing date of July 3, 2018, and, therefore, the broadest reasonable interpretation standard applies. *See* Paper 6 (Notice of Filing Date Accorded to Petition).

In applying a broadest reasonable interpretation, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). This presumption may be rebutted when a patentee, acting as a lexicographer, sets forth an alternate definition of a term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Furthermore, only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

1. Image Header

Petitioner argues the term "image header" means "a header associated with the entire image that specifies where the data segments are to be placed in the system memory." Pet. 17 (citing Ex. 1001, 7:50–52, 8:18–21, 9:23–24, 10:6, claim 10; Ex. 1008, 3; Ex. 1002 ¶ 77). When we instituted trial, we did not adopt Petitioner's proposed construction as the broadest

reasonable interpretation for reasons explained in the Decision on Institution, including that the proposed construction requires plural "data segments" while the claim recites "at least one data segment." Dec. on Inst. 6–8. Nonetheless, "we determine[d] that Petitioner's proposed construction falls within the broadest reasonable interpretation of 'image header.'" Dec. on Inst. 6–8. Thus, we applied Petitioner's proposed construction in determining whether the asserted prior art teaches the subject matter claimed. Dec. on Inst. 24–26.

In its Response, Patent Owner agrees with Petitioner's proposed construction. PO Resp. 12–13. Because the concerns with Petitioner's proposed construction that we highlighted in the Decision on Institution do not impact our analysis in this Decision, we apply the parties' agreed construction of "image header" as "a header associated with the entire image that specifies where the data segments are to be placed in the system memory."

2. *Hardware Buffer*

The term "hardware buffer" appears in independent claim 1, and claims 2 and 8, which depend from claim 1, and in claim 12, which depends from independent claim 10. Claim 1 recites, in part, "a secondary processor comprising: system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image" and "a scatter loader controller configured: to load the image header; and to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory." Claim 12 recites, "The method of claim 10 further comprising loading the executable software image directly from a hardware buffer to the system

memory of the secondary processor without copying data between system memory locations."

Although the Petition does not set forth an express construction for "hardware buffer," Petitioner contends that the claimed "hardware buffer" is taught by the prior art's (Svensson's and Bauer's) disclosure of a block of random access memory (RAM) that is reserved when needed to create an intermediate storage area for temporarily storing information being sent to system memory. Pet. 27 (citing Ex. 1009 ¶¶ 35–36, Fig. 2; Ex. 1010, 3:54–58, 3:64–4:5, Fig. 1; Ex. 1002 ¶ 110); Pet. Reply. 34–35. In its Preliminary Response, Patent Owner argued that "[t]he 'intermediate storage area' in Svensson is a temporary buffer within *system* memory – it is not a 'hardware buffer' as alleged by Petitioner." Prelim. Resp. 34.

In the Decision on Institution, we stated that, "[o]n the evidence before us, we are persuaded that Svensson and Bauer's intermediate storage area teaches a 'hardware buffer'" because "[t]he intermediate storage area of Bauer and Svensson is a buffer used to store data destined for another memory, and the intermediate storage area is in hardware inasmuch as SARAM and DARAM [of Bauer and Svensson] are hardware." Dec. on Inst. 27.

During the trial, Patent Owner maintains that the disclosure of a temporary buffer in RAM, such as in Bauer and Svensson, does not teach the claimed "hardware buffer." PO Resp. 70–71. Patent Owner argues that the term "hardware buffer" means "a buffer within a hardware transport mechanism that receives data sent from the primary processor to the secondary processor." PO Resp. 14. In its Reply, Petitioner argues that Patent Owner's proposed construction should be rejected, and Petitioner

argues that "the term 'hardware buffer' should be given its ordinary meaning of 'a buffer implemented in hardware.'" Pet. Reply 8–11 (citing Ex. 1023 ¶ 25). In response, Patent Owner disputes Petitioner's proposed construction, arguing that "a buffer cannot exist absent some piece of hardware, such that all buffers must ultimately be 'implemented in hardware.'" PO Sur-reply 11. Patent Owner offers an alternative proposed construction in the following discussion:

> [T]o the extent the Board determines that Qualcomm's proposed construction of "hardware buffer" is too narrow, Qualcomm alternatively proposes that the term be construed as "a buffer that is not allocated by the secondary processor." In the '949 patent, the hardware buffer is a *permanent* buffer within the hardware transport mechanism (Ex. 1001 at 2:58-61, 8:24-30, Fig. 3; Ex. 2007 at ¶¶69-71), in contrast to a *temporary* buffer in system memory that is allocated by the secondary processor at run time for this purpose (Ex. 1001 at 2:14-34; Ex. 2007 at ¶¶52-53). Qualcomm's alternative construction of "hardware buffer" captures this distinction between the system memory and the hardware buffer, whereas Petitioner's overly broad construction does not.

PO Sur-reply 13.

We begin our analysis with the claim language. Independent claim 1 does not recite any particular configuration for the "hardware buffer." As noted above, claim 1 recites, in part, "a secondary processor comprising: system memory and a hardware buffer for receiving an image header and at least one data segment of an executable software image" and "a scatter loader controller configured: to load the image header; and to scatter load each received data segment based at least in part on the loaded image header, directly from the hardware buffer to the system memory." Thus, claim 1 recites that the hardware buffer is "for receiving an image header

12

and at least one data segment of an executable software image," but it does
not define what implementation the hardware buffer must take or what type
of storage device the hardware buffer is. Claim 1 separately recites a
"system memory," but that recitation of a separate system memory, by itself,
does not foreclose the possibility of implementing a buffer in some other
system memory.

Turning next to the Specification of the '949 patent, Figure 3 depicts a
"Hardware Buffer" as part of the "Hardware Transport Mechanism" in each
of the primary processor and the secondary processor. Ex. 1001, Fig. 3.
Patent Owner relies on this disclosure in support of its proposed construction
that a hardware buffer be "within a hardware transport mechanism." PO
Resp. 14–15. We find Patent Owner's position problematic for two reasons.
First, as Petitioner points out (Pet. Reply 10), the Specification of the '949
patent describes Figure 3 as "exemplary." Ex. 1001, 4:10–13, 7:60–62; *see
also* Ex. 1001, 4:22–25 ("The word 'exemplary' is used herein to mean
'serving as an example, instance, or illustration.' Any aspect described
herein as 'exemplary' is not necessarily to be construed as preferred or
advantageous over other aspects."). We are not persuaded that importing
this limitation from the Specification into the claims is warranted under the
broadest reasonable interpretation. *See Phillips v. AWH Corp.*, 415 F.3d
1303, 1323 (Fed. Cir. 2005) (en banc) ("[A]lthough the specification often
describes very specific embodiments of the invention, we have repeatedly
warned against confining the claims to those embodiments.").

Second, even if we were persuaded that adding the qualifier "within a
hardware transport mechanism" were appropriate, that language does not
provide a very helpful definition to a person of ordinary skill in the art. The

'949 patent states that "[s]econdary processor 302 includes a hardware transport mechanism 309 (e.g., a USB controller)." Ex. 1001, 8:60–62; *see also* Ex. 1001, Fig. 3 (labeling box 309 as "Hardware Transport Mechanism (i.e. USB Controller)"). Thus, the '949 patent gives an example of a hardware transport mechanism, but the '949 patent does not indicate that the term "hardware transport mechanism" is limited to this example. *See* Tr. 64:4–9 (Patent Owner's counsel stating that "hardware transport mechanism" "refers to a broad variety of hardware"), 46:11–14 (Patent Owner's counsel stating that "hardware transport mechanism" is "a generic term if you look at the specification. That's a generic term for a USB controller, a PCIU controller. It's some kind of serial bus controller that exists in both the secondary processor and the primary processor."). Thus, the phrase "hardware transport mechanism" itself lacks the kind of specificity that would help a person of ordinary skill at the time of patenting understand the term "hardware buffer" or that would help us resolve the obviousness inquiry from the perspective of a person of ordinary skill in the art.

As noted above, Petitioner asserts that the term "hardware buffer" means "a buffer implemented in hardware." Pet. Reply 11 (citing Ex. 1023 ¶ 25). This proposed construction is similar to our preliminary determination at institution that Svensson and Bauer's intermediate storage area teaches the claimed "hardware buffer" because the intermediate storage area is a buffer and it is in hardware. Dec. on Inst. 27. Having considered the full trial record, we agree with Patent Owner that Petitioner's proposed construction and our preliminary determination fail to give meaning to the term "hardware." In particular, Patent Owner correctly points out that "a

buffer cannot exist absent some piece of hardware, such that all buffers must ultimately be 'implemented in hardware.'" PO Sur-reply 11; *see Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

The written description of the '949 patent, which uses the term "hardware buffer" only three times (Ex. 1001, 2:58–63, 9:37–41), does not provide much, if any, guidance on what a "hardware buffer" must be. As Patent Owner points out, however, the '949 patent does differentiate disclosed loading techniques from known prior art techniques that use temporary buffers to receive data from a primary processor for loading. *See* PO Sur-reply 5–6. For example, the "Background" section of the '949 patent describes a conventional loading process as follows:

> In a system in [w]hich the software image is loaded onto a target "secondary" processor from a first "primary" processor, *one way of performing such loading is to allocate a temporary buffer* into which each packet is received, and each packet would have an associated packet header information along with the payload. The payload in this case would be the actual image data. From the temporary buffer, some of the processing may be done over the payload, and then the payload would get copied over to the final destination. The temporary buffer would be some place in system memory, such as in internal random-access-memory (RAM) or double data rate (DDR) memory, for example.

Ex. 1001, 2:23–34 (emphasis added). The '949 patent contrasts its disclosure with the prior art's use of a temporary buffer, stating that "[i]n one exemplary aspect a direct scatter load technique is disclosed for loading a segmented image from a primary processor's non-volatile memory to a secondary processor's volatile memory. As discussed further below, the

direct scatter load technique avoids use of a temporary buffer." Ex. 1001, 4:43–47. Furthermore, in describing a disclosed loading technique with reference to the exemplary device of Figure 1, the '949 patent discloses that "[t]he modem processor 110 stores the modem executable image 132 directly into the modem processor RAM (Random Access Memory) 112 to the final destination *without copying the data into a temporary buffer* in the modem processor RAM 112." Ex. 1001, 5:31–35 (emphasis added).

Patent Owner likens the '949 patent's distinction over using temporary buffers to the situation in *SciMed Life Systems, Inc. v. Advanced Cardiovascular Systems, Inc.*, 242 F.3d 1337 (Fed. Cir. 2001). PO Sur-reply 5–6. In that case, the Court of Appeals for the Federal Circuit noted that the written description of the patents at issue described several disadvantages of certain prior art catheters. *Id.* at 1342–43. The court stated that

> the SciMed patents distinguish the prior art on the basis of the use of dual lumens and point out the advantages of the coaxial lumens used in the catheters that are the subjects of the SciMed patents. That discussion in the written description supports the district court's conclusion that the claims should not be read so broadly as to encompass the distinguished prior art structure.

Id. at 1343. We find this reasoning applicable to the claims that recite the use of a hardware buffer because those claims have affirmatively recited a distinct term—"hardware buffer"—to differentiate from prior art techniques described in the '949 patent that use a "temporary buffer." For those claims, therefore, we agree with Patent Owner that the '949 patent distinguishes over prior art techniques that use a temporary buffer, based on the passages discussed above. Ex. 1001, 2:23–34, 4:43–47, 5:31–35.

For the above reasons, we conclude that the "hardware buffer" limitations of independent claim 1 and its dependent claims (2–9) and dependent claim 12 "should not be read so broadly as to encompass" the use of a temporary buffer. *See SciMed*, 242 F.3d at 1343. No further interpretation of "hardware buffer" is necessary to resolve the obviousness inquiry before us. *See Nidec*, 868 F.3d at 1017.

3. Means-Plus-Function Limitations

The 1335 Petition sets forth proposed constructions for several limitations of independent claim 16 that Petitioner contends are means-plus-function limitations governed by 35 U.S.C. § 112, ¶ 6. IPR2018-01335 Paper 3 ("1335 Pet."), 17–22 (addressing "means for receiving . . . an image header," "means for processing . . . the image header," "means for receiving . . . each data segment," and "means for scatter loading"). In the 1335 Decision on Institution, we agreed with Petitioner that the identified limitations of claim 16 are means-plus-function limitations subject to 35 U.S.C. § 112, ¶ 6, and we agreed with Petitioner's identification of the claimed functions. 1335 Dec. on Inst. 13. We stated, however, that "we have questions as to the sufficiency of Petitioner's identified structures," and we discussed the "means for processing . . . the image header" and "means for scatter loading" limitations. 1335 Dec. on Inst. 13–15.

In its Response, Patent Owner addresses the "means for processing . . . the image header" and "means for scatter loading" limitations and identifies the same corresponding structure identified in the 1335 Petition. PO Resp. 18–21. Patent Owner also argues that "these terms do not need to be construed in order for the Board to reach its Final Written Decision" because "[n]one of the arguments Qualcomm makes below to

distinguish the prior art requires construction of these limitations." PO Resp. 17. In its Reply, Petitioner states that, "[u]pon consideration of the Board's articulated concerns, Petitioner agrees that the '949 specification fails to disclose sufficient structure to perform the recited functions." Pet. Reply 14. Petitioner, however, also agrees with Patent Owner's position that we still "can address in this proceeding whether claim 16 is invalid in view of the asserted prior art." Pet. Reply 14 (citing PO Resp. 17).

Under our Rules, for a means-plus-function limitation, a petition "must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function." 37 C.F.R. § 42.104(b). Therefore, it is Petitioner's burden to identify corresponding structure. Because Petitioner asserts during the trial that the Specification of the '949 patent fails to disclose sufficient corresponding structure for the "means for processing . . . the image header" and "means for scatter loading" limitations (Pet. Reply 14), Petitioner has not met this burden. Furthermore, in the absence of the requisite showing by Petitioner of sufficient corresponding structure for the means-plus-function limitations, we need not further address the construction of these claim terms to determine whether Petitioner has met its burden to prove, by a preponderance of the evidence, unpatentability of independent claim 16 and dependent claim 17.

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence.[10] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Obviousness over Bauer, Svensson, and Kim
(Claims 1–15, 22, 23)

Petitioner contends claims 1–15, 22, and 23 of the '949 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, and Kim. Pet. 23–75; 1335 Pet. 29–67.

1. Svensson

Svensson describes a multi-processor system in which data are sent from a host processor to a client processor. Ex. 1010, code (57). Figure 1 of Svensson is reproduced below.

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[10] Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.
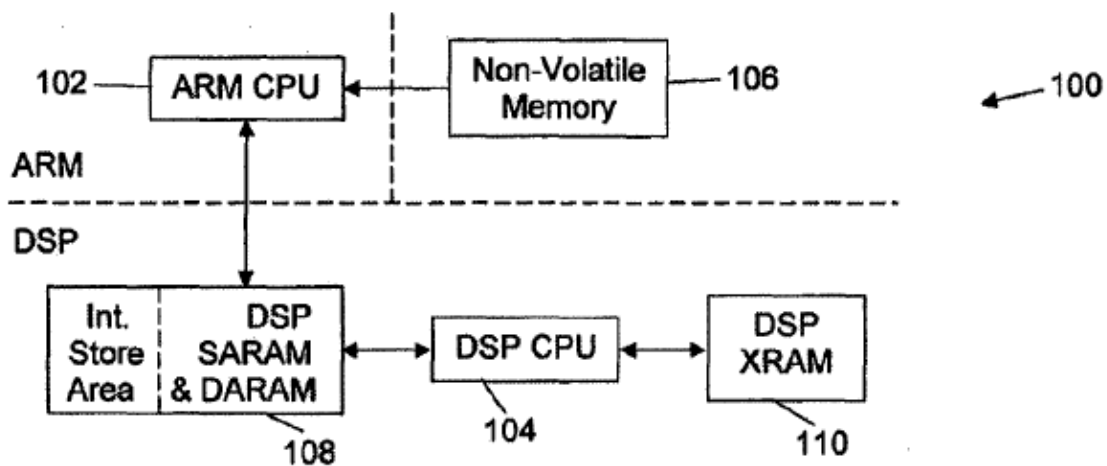
FIG. 1

Figure 1 depicts multi-processor system 100 having host processor 102 and client processor 104. Ex. 1010, 3:49–50. Client processor 104 is the processor for a digital signal processor (DSP) device. Ex. 1010, 3:54–58. As Svensson explains, "[m]ost commercially available DSP devices include on-chip memories, and as indicated in FIG. 1, the DSP includes 'internal' single-access RAM (SARAM) and dual-access RAM (DARAM) 108, as well as an 'external' RAM (XRAM) 110." Ex. 1010, 3:64–4:1. Svensson explains that "XRAM 110 is invisible to, i.e., not accessible by, the CPU 102," whereas CPU 102 can access "internal" SARAM and DARAM 108. Ex. 1010, 4:5–8, 4:13–14. DSP processor 104 can access both RAMs 108 and 110. Ex. 1010, 4:7–8.

Because host processor 102 cannot access XRAM 110, Svensson discloses a technique for sending data from host processor 102 to be stored in XRAM 110. Ex. 1010, Fig. 2, 4:15–6:11, 7:7–8. Svensson's Figure 2 is reproduced below.
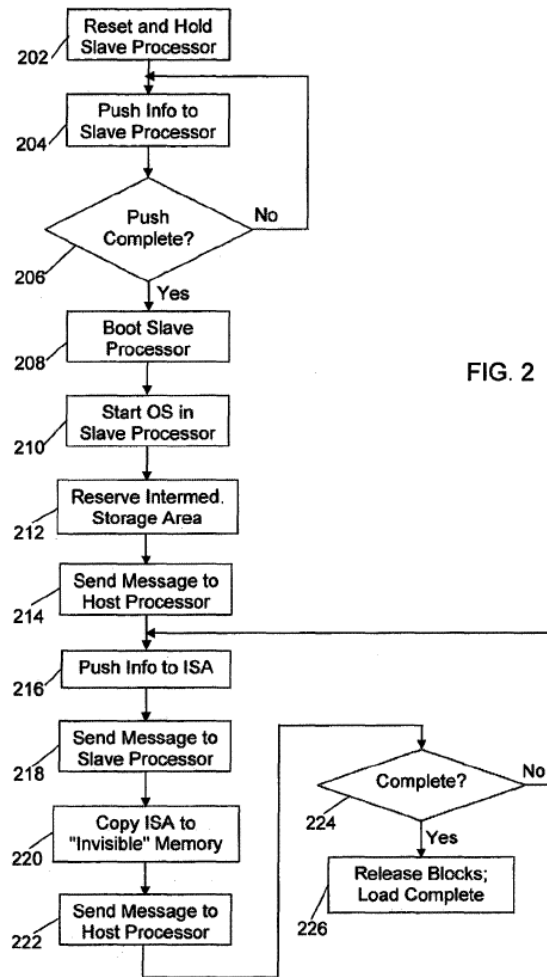
Figure 2 is a flow chart of Svensson's bootloader operation. Ex. 1010, 3:34, 4:15–19. In step 212, a block of memory in "internal" memory 108 is reserved as an intermediate storage area (ISA) for data that are being sent from the host to the invisible memory of the client processor. Ex. 1010, 5:21–28. After the host transfers data to the ISA (step 216), the host tells the client the ISA has been loaded and indicates whether more data are coming (step 218). Ex. 1010, 5:53–63. The client then copies the data from the ISA to its "invisible" memory (step 220) and responds to the host when copying is finished (step 222). Ex. 1010, 5:63–6:3. "If there is more code and/or data to load (Step 224), this cycle of copying and messaging (Steps 216–224) can be repeated as many times as required." Ex. 1010, 6:4–6.

21

2. *Bauer*

Bauer discloses the file format depicted in Figures 1A, 1B, and 1C, which are reproduced below.

FIG. 1A

Header 102	Section Information 104	Section Data 106

100

FIG. 1B

102

Size [32 bits] 102-1	Number of sections [16 bits] 102-2

Section 1 Length [16 bits] 108-1	Extra 1 [16 bits] 112-1	Section 2 Length [16 bits] 108-2	Extra 2 [16 bits] 112-2
Load Address 1 [32 bits] 110-1		Load Address 2 [32 bits] 110-2	

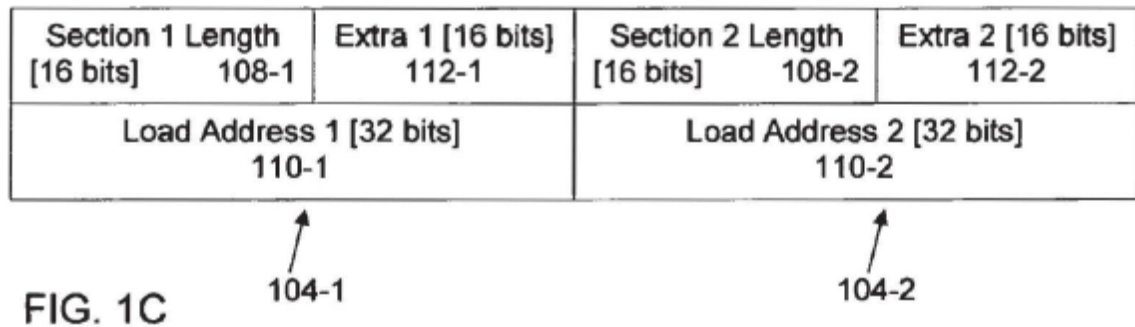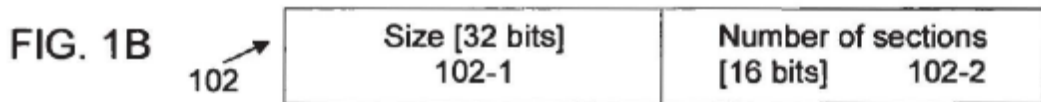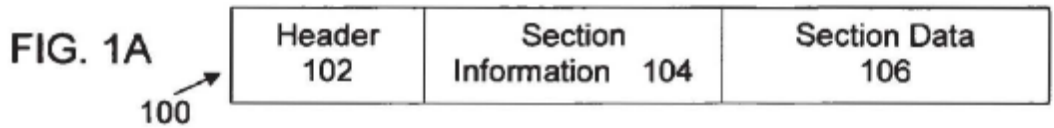104-1   104-2

FIG. 1C

Figure 1A shows the format for a data image, Figure 1B shows the header of the data image, and Figure 1C shows the section information of the data image. Ex. 1009 ¶¶ 21–23. As shown in Figure 1A, binary data image 100 has header 102, section information 104, and section data 106. Ex. 1009 ¶ 32. Each section of data in section data 106 has a section information entry in section information 104, two of which are depicted in Figure 1C as entries 104-1 and 104-2. Ex. 1009 ¶ 34. Each section information entry indicates the length (108) and load address (110) for its respective section data. Ex. 1009 ¶ 34. Additional information about a section may be included in extra information element 112. Ex. 1009 ¶ 34.

According to Bauer, "[h]aving all section information entries 104 collected together in the image 100 advantageously simplifies system navigation through the image, and having all section data arranged in a sequence makes it possible to optimize loading of the sections." Ex. 1009 ¶ 38. Bauer explains that "[t]here are many possible applications of this format and its individually coded sections," including "[o]bject code and data . . . with a program loader reading the stored information and processing stored sections accordingly." Ex. 1009 ¶ 31. "One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for 'Operating-System-Friendly Bootloader'." Ex. 1009 ¶ 31. This is the application that issued as Svensson. Svensson's Figure 1 depicts the same multi-processor system as Bauer's Figure 2, which Bauer says "can advantageously use a binary image 100 having the format depicted in FIGS. 1A, 1B, 1C." Ex. 1009 ¶ 35; *compare* Ex. 1010, Fig. 1, *with* Ex. 1009, Fig. 2.

3.   Kim

Kim discloses a system in which a system startup loader in a system management processor provides program blocks to multiple other processors in a system. Ex. 1012, 4:8–21, Fig. 1. Figure 3 of Kim is reproduced below.
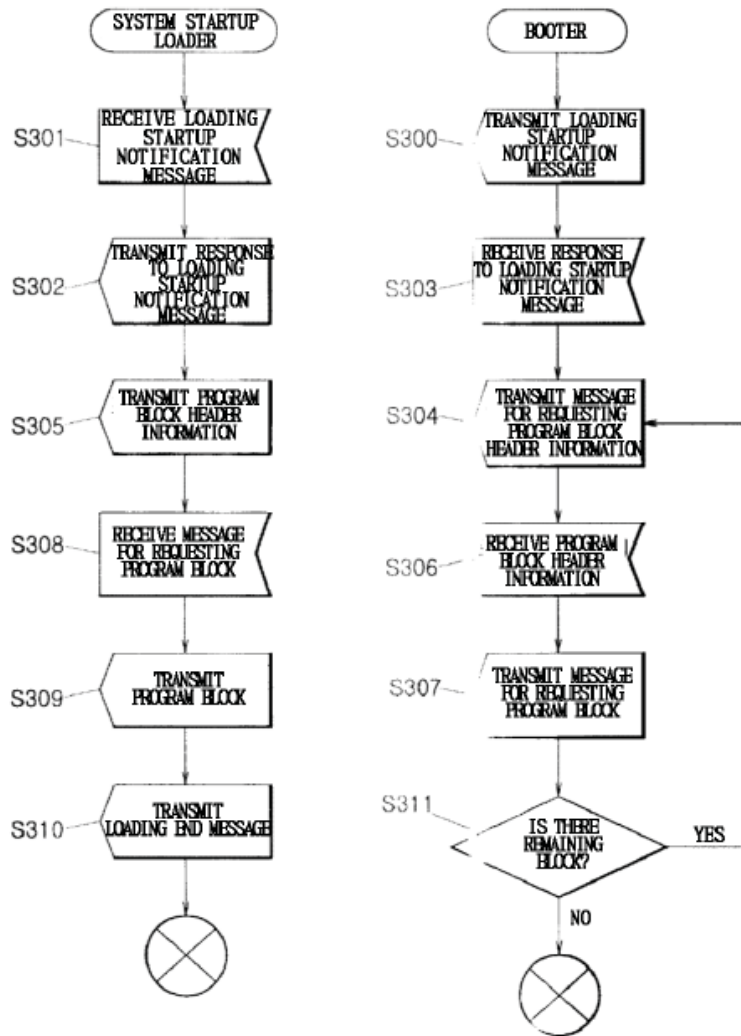
FIG. 3

Figure 3 is a flowchart showing a procedure for loading program blocks from the system startup loader to other processors in the system. Ex. 1012, 5:9–11. In step S304, the booter in a processor requests program block header information, which the system startup loader provides in step S305. Ex. 1012, 5:18–21. When the header is received, the booter requests a program block in step S307, which the system startup loader provides in step S309. Ex. 1012, 5:21–24. If there are more blocks to be received, the booter returns to step S304. Ex. 1012, 6:2–4.

24

4. *Petitioner's Use of "Bauer and Svensson combined"*

As noted above, Bauer expressly cites Svensson's program loader as an example of a program loader that can use the file format disclosed in Bauer. Ex. 1009 ¶ 31 ("One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for 'Operating-System-Friendly Bootloader'."). Based on the interrelatedness of Bauer and Svensson, Petitioner refers to "'Bauer and Svensson combined' to illustrate what Bauer alone, or Bauer in combination with Svensson, teaches to a" person of ordinary skill in the art. Pet. 23–25. Petitioner further explains:

> Although it is readily apparent that the file format of Bauer can be used in the multiprocessor system of Svensson, Bauer does not describe the multiprocessor system with the same level of detail as Svensson. Because of that, this Petition refers to "Bauer and Svensson combined," but is clear in identifying the relevant disclosures from each reference in its citations.

Pet. 24–25.

Patent Owner argues that "Petitioner's reliance on 'Bauer and Svensson combined' is ambiguous and does not identify which claim limitations are missing from either of the particular references" and, therefore, that Petitioner has not set forth a *prima facie* case of obviousness in compliance with *Graham*. PO Resp. 35–37; *see* PO Sur-reply 15–16.

We disagree with Patent Owner's assertion that Petitioner has not set forth a *prima facie* case by using "Bauer and Svensson combined" in its contentions. As discussed more fully below, the Petitions set forth how Bauer and Svensson teach the claimed subject matter, including citations to the disclosures of the references, as required by our Rules. *See, e.g.,* 37 C.F.R. § 42.104(b)(4) ("The petition must specify where each element of

the claim is found in the prior art patents or printed publications relied

upon . . . ."). As also discussed below, the Petitions explain how the asserted

references allegedly render obvious the claimed subject matter, accounting

for differences between the references and the claims, as required by

Graham. We further note that Patent Owner and its declarant, Dr. Rinard,

use the phrase "Bauer and Svensson combined," undermining Patent

Owner's assertion that this phrase is ambiguous. PO Resp. 44, 65, 67, 68,

72; Ex. 2007 ¶¶ 157, 162, 163.

5. Independent Claim 10[11]

a) Receiving an image header

Claim 10 is a method claim and recites

> receiving at a secondary processor, from a primary processor via
> an inter-chip communication bus, an image header for an
> executable software image for the secondary processor that is
> stored in memory coupled to the primary processor, the
> executable software image comprising the image header and at
> least one data segment, the image header and each data segment
> being received separately.

Ex. 1001, 13:47–55 ("first receiving limitation").

For the structural elements of claim 10, Petitioner identifies particular

components in Bauer's Figure 2 and in Svensson's Figure 1, both of which

depict the same multi-processor system, as noted above. Petitioner argues a

person of ordinary skill in the art would have been motivated to combine the

teachings of Bauer and Svensson because, among other reasons, Bauer

expressly cites Svensson's program loader as an example of a program

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[11] Petitioner challenged independent claim 10 in IPR2018-01335, which was
consolidated into IPR2018-01334. Therefore, citations to the Petition in
IPR2018-01335 are preceded by "1335."

loader that can use the file format disclosed in Bauer. 1335 Pet. 31 (citing Ex. 1009 ¶ 31; Ex. 1020[12] ¶¶ 109–110); *see* Ex. 1009 ¶ 31 ("One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for 'Operating-System-Friendly Bootloader'.").
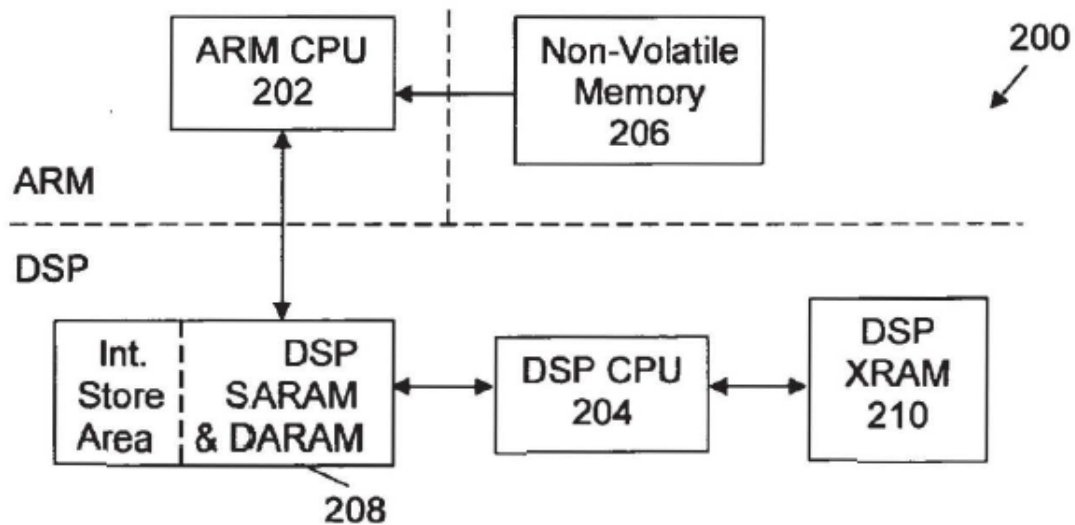
Figure 2 of Bauer is reproduced below.

FIG. 2

Figure 2 of Bauer depicts multi-processor system 200 having host processor 202 and client processor 204. Ex. 1009 ¶ 35. In Figure 2, host processor 202 is an advanced RISC (reduced instruction set computer) machine (ARM) central processing unit (CPU), and client processor 204 is a DSP CPU. Ex. 1009 ¶ 35.

Referring to Bauer's Figure 2, which depicts the same multi-processor system as Svensson's Figure 1, Petitioner contends the DSP device teaches

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[12] This exhibit was originally filed as Exhibit 1102 in IPR2018-01335. After consolidation, it was filed as Exhibit 1020. *See* Paper 15 (Joint Identification of Exhibits).

the claimed "secondary processor" and the ARM device teaches the claimed "primary processor." 1335 Pet. 32–33. Petitioner further argues Figure 2 of Bauer and Figure 1 of Svensson show these two processors coupled by a bus and that the combination of Bauer and Svensson, therefore, teaches "an inter-chip communication bus." 1335 Pet. 32–33 (citing Ex. 1009 ¶¶ 35–36, Fig. 2; Ex. 1010, 3:49–63, 4:3–8, Fig. 1; Ex. 1020 ¶ 115); *see* Ex. 1009 ¶ 36 ("The arrows in FIG. 2 indicate access paths, e.g., busses and direct memory access (DMA) paths, between the CPUs and the memories . . . ."). Patent Owner does not dispute these contentions. We are persuaded by Petitioner's contentions and evidence, summarized above, and we find that the combination of Bauer and Svensson teaches this subject matter.

As to the claimed "image header," Petitioner notes that, in Bauer, section information 104, rather than header 102, specifies the destination addresses for each section of data. 1335 Pet. 43 (citing Ex. 1009 ¶¶ 32–34, Figs. 1A–1C; Ex. 1020 ¶ 132). To meet the "image header" limitation under its proposed construction ("a header associated with the entire image that specifies where the data segments are to be placed in the system memory"), Petitioner argues that including section information in Bauer's header would have been obvious to a person of ordinary skill in the art. 1335 Pet. 43–45. In the Decision on Institution, we agreed with Petitioner, and we noted that "the only difference between Bauer's section information and Petitioner's proposed construction of 'image header' is the label applied, namely whether it is a 'header' or not." 1335 Dec. on Inst. 25; Dec. on Inst. 18. We further noted that "Petitioner's proposed modification appears to involve little more than applying the label 'header' to Bauer's header 102 and section information 104 collectively," and we cited instances in which Bauer

"effectively treats these two data segments as one entity." 1335 Dec. on Inst. 25–26 (citing Ex. 1009 ¶¶ 29, 30); Dec. on Inst. 19. During the trial, Patent Owner does not dispute Petitioner's contention that the claimed "image header" would have been obvious based on Bauer's disclosure of header and section information. *See* Tr. 55:21–56:13. Based on the full trial record, we are persuaded by Petitioner's evidence and argument, and we conclude that "a header associated with the entire image that specifies where the data segments are to be placed in the system memory," as the parties construe "image header," would have been obvious based on Bauer's disclosure of header and section information that contains the required information. Ex. 1009 ¶¶ 29, 30, 32–34, 38, Figs. 1A–1C; *see* Dec. on Inst. 24–26.

Petitioner further contends the combination of Bauer and Svensson teaches "an image header for an executable software image for the secondary processor that is stored in memory coupled to the primary processor, the executable software image comprising the image header and at least one data segment." 1335 Pet. 35–38. In particular, Petitioner contends Bauer discloses that its file format can hold executable data and object code, thereby teaching "an executable software image." 1335 Pet. 35–36 (citing Ex. 1009 ¶¶ 30–32; Ex. 1020 ¶ 121); *see* Ex. 1009 ¶ 31 ("There are many possible applications of this format and its individually coded sections. . . . It can also be used as a file format in which executable files are stored . . . ."). Bauer's file format stores data in section data 106. Ex. 1009 ¶ 32 ("The section data 106 includes the data of the one or more sections included in the image 100."), Fig. 1A.

Petitioner argues that, in Bauer and Svensson, the non-volatile memory coupled to the ARM CPU stores executable software for the DSP device and, therefore, that the combination of Bauer and Svensson teaches "an executable software image for the secondary processor that is stored in memory coupled to the primary processor." 1335 Pet. 37–38 (citing Ex. 1009 ¶¶ 11, 31, 35–36, Fig. 2; Ex. 1110, 4:9–14, 6:12–15, Figs. 1, 3; Ex. 1020 ¶ 124). For example, Svensson discloses that "[t]he SARAM and DARAM 108 [of the DSP device] can be loaded from the non-volatile memory 106 [of the ARM device] by the trivial 'push' method." Ex. 1010, 4:9–10. Patent Owner does not dispute these contentions. We are persuaded by Petitioner's contentions and evidence, summarized above, and we find that the combination of Bauer and Svensson teaches this subject matter.

For this limitation of claim 10, the dispute between the parties is whether the subject matter reciting "the image header and each data segment being received separately" would have been obvious based on Bauer, Svensson, and Kim. We address this next.

i. Receiving image header and each data segment separately

Claim 10 recites "the image header and each data segment being received separately." As noted above, Bauer's file format stores data in section data 106. Ex. 1009 ¶ 32. As discussed above, we are persuaded the combination of Bauer and Svensson renders obvious an "image header" under the parties' agreed construction.

Petitioner contends that the subject matter of receiving the image header and each data segment separately at the secondary processor would have been obvious to a person of ordinary skill in the art based on the

combined teachings of Bauer and Svensson. 1335 Pet. 45–47. In particular, Petitioner relies on Bauer's disclosure that "[i]nformation about the sections is located in a header and section information at, for example, the beginning of the image, and so the information about the sections *can be retrieved before the sections are read*." Ex. 1009 ¶ 30 (emphasis added), *cited in* 1335 Pet. 46. Citing the testimony of its declarant, Dr. Lin, Petitioner argues that a person of ordinary skill in the art

> would understand from Bauer and Svensson combined that "retrieving" the header and section information before the data segments are read and processed means that the secondary processor's hardware buffer (intermediate storage area) receives the header and section information **separately** from (and before) the data segments are transferred.

1335 Pet. 46 (citing Ex. 1020 ¶ 140). Petitioner additionally cites Bauer and Svensson's disclosure of transferring data between processors in blocks in support of its argument that receiving header and data segments separately would have been obvious. 1335 Pet. 46 (citing Ex. 1010, 5:28–36, 5:53–6:33, 6:67–7:2, Fig. 2; Ex. 1009 ¶¶ 27, 43, Figs. 1A–1C; Ex. 1020 ¶ 141).

As discussed above, Petitioner argues a person of ordinary skill in the art would have been motivated to combine the teachings of Bauer and Svensson because, among other reasons, Bauer expressly cites Svensson's program loader as an example of a program loader that can use the file format disclosed in Bauer. 1335 Pet. 31 (citing Ex. 1009 ¶ 31; Ex. 1020 ¶¶ 109–110); *see* Ex. 1009 ¶ 31 ("One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for 'Operating-System-Friendly Bootloader'.").

Patent Owner does not dispute that a person of ordinary skill in the art would have combined Bauer and Svensson; rather, Patent Owner challenges

Petitioner's contentions as to how the combined system would operate. *See*
Tr. 65:2–8 (Patent Owner: "And we are not, were not arguing that the
person of skill in the art wouldn't combine Bauer and Svensson and I think
they would. That's not the question. The question is when you combine
Bauer and Svensson . . . how would the system work."). According to
Patent Owner, in the combined system, the host processor ("primary
processor") would store data in Bauer's format but convert that data to
Svensson's format for transmission to the secondary processor. *See* PO
Resp. 43–46.

Patent Owner produces the annotated figure below in its Response.
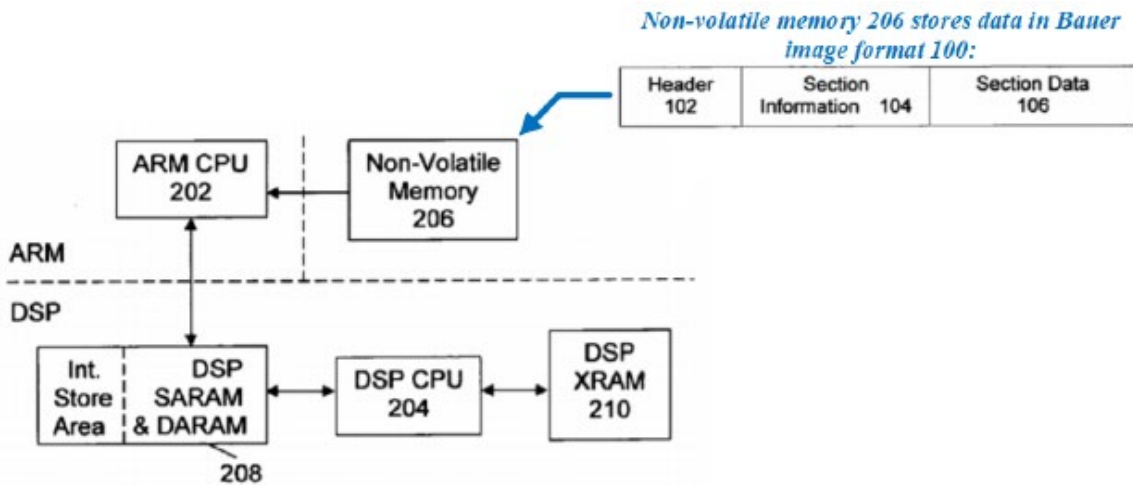
PO Resp. 43. The figure reproduced above shows binary data image 100
from Bauer's Figure 1A with an arrow to non-volatile memory 206 in
Bauer's Figure 2 and contains the following annotation: "Non-volatile
memory 206 stores data in Bauer image format 100." PO Resp. 43. Patent
Owner argues that, "to the extent the [person of ordinary skill in the art]
would combine Bauer and Svensson, the [person of ordinary skill in the art]
would be motivated to store a binary data image in the format of Bauer
Figs. 1A-1C within the non-volatile memory of the host processor." PO

Resp. 43 (citing Ex. 2007 ¶¶ 118–119). As Patent Owner correctly notes,
"[t]his is consistent with Bauer's express disclosure that the non-volatile
memory can store 'an image in the format depicted in Figs. 1A-1C.'" PO
Resp. 43 (quoting Ex. 1009 ¶ 36). This is also consistent with Petitioner's
contentions that a person of ordinary skill in the art would have been
motivated to use Bauer's file format in the system of Svensson based on
Bauer's express teaching. *See* 1335 Pet. 40–41 (citing, *inter alia*, Ex. 1009
¶ 31).

The parties, however, disagree as to how, in the combined system of
Bauer and Svensson, the image data stored in the non-volatile memory of the
primary processor would be sent to the secondary processor. Petitioner
argues that a person of ordinary skill in the art would have been motivated to
transfer an image from a primary processor to a secondary processor using
Bauer's file format based on Bauer's disclosure. 1335 Pet. 40–41. Patent
Owner, on the other hand, argues that the host processor would read the
section information and "would use the offset, length, and load address
information to generate headers for individual blocks, with each header
including a length and destination address for a respective block, as shown
in Fig. 3 of Svensson." PO Resp. 44 (citing Ex. 1009, Fig. 1C; Ex. 2007
¶¶ 121–122). Patent Owner argues that "[t]he host processor would further
use the section information 104 to process the section data of the data image,
specifically to locate and copy each section in the section data into the
intermediate storage area in the format of the transfer block disclosed in
Fig. 3 of Svensson." PO Resp. 44 (citing Ex. 2007 ¶¶ 122–123). According
to Patent Owner, therefore, "the [person of ordinary skill in the art] would
arrange information in the intermediate storage area using the format of

Svensson Fig. 3, where information is stored in blocks and each block has its own respective header." PO Resp. 45 (citing Ex. 2007 ¶ 124). Thus, Patent Owner's argument is that, in the combined system, the host processor would store data in Bauer's format but convert that data to Svensson's format for transmission to the secondary processor according to Svensson's teachings. *See* PO Resp. 43–46.

Patent Owner's proposal is certainly one way a person of ordinary skill in the art could implement the combined teachings of Bauer and Svensson, but Petitioner proposes a different manner of implementation that we find is supported by the record evidence. In particular, Bauer discloses the following:

> There are many possible applications of this format and its individually coded sections. For example, an operating system memory manager can load and unload sections of memory according to images in this format. It can also be used as a file format in which executable files are stored, and linkers and *program loaders can be readily adapted to support (read, write, and interpret) the format.* Object code and data can also be stored in this file format, with *a program loader reading the stored information and processing stored sections accordingly. One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for "Operating-System-Friendly Bootloader".*

Ex. 1009 ¶ 31 (emphases added). Thus, Bauer expressly teaches its file format being used with Svensson's program loader "reading the stored information and processing stored sections *accordingly*." Ex. 1009 ¶ 31 (emphasis added). Patent Owner's argument that a person of ordinary skill in the art would have used Svensson's format for loading data, while a possibility, ignores the proposed combination and Bauer's express disclosure.

Patent Owner also argues that "the *only* format disclosed in either Svensson or Bauer for storing data in the intermediate storage area and transferring data to the XRAM is the block format shown in Svensson Fig. 3, and neither reference suggests any disadvantages or drawbacks to using this format." PO Resp. 46. Similarly, Patent Owner argues that "neither reference suggests that this format [(Bauer's file format)] should be used to store data in the intermediate storage unit." PO Resp. 46. We disagree. In addition to Bauer's teaching of using its format in the program loader of Svensson, Bauer discloses the following:

> Most commercially available DSP devices include on-chip memories, and as indicated in FIG. 2, the DSP includes "internal" single-access RAM (SARAM) and dual-access RAM (DARAM) 208, as well as an "external" RAM (XRAM) 210. An *intermediate storage area*, indicated by the dashed line, may be defined within the memory 208. The arrows in FIG. 2 indicate access paths, e.g., busses and direct memory access (DMA) paths, between the CPUs and the memories, *any one or more of which may store an image in the format depicted in FIGS. 1A-1C.*

Ex. 1009 ¶ 36 (emphases added). Thus, as Petitioner correctly points out (Pet. Reply 24–25), Bauer teaches using its file format in any memory, including the intermediate storage area.

Patent Owner also cites Svensson's disclosures of the benefits of large data transfers to keep the intermediate storage area filled as evidence that a person of ordinary skill in the art "would not be motivated to have the secondary processor receive the image header and each data segment separately as required by the claims." PO Resp. 63–64 (citing Ex. 1010, 6:32–37, 6:49–7:2; Ex. 2007 ¶¶ 155–156). Citing the testimony of Dr. Rinard, Petitioner argues that a person of ordinary skill in the art "would

be motivated to keep the intermediate storage area full and send information to the intermediate storage area in fewer large transfers rather than more small transfers, consistent with the express teachings of Svensson." PO Resp. 64 (citing Ex. 2007 ¶¶ 155–156). According to Patent Owner, "[t]o achieve this, the header 102, section information 104, and as much of the section data 106 as would fit in the intermediate storage area would all be transferred together to the intermediate storage area." PO Resp. 64 (citing Ex. 2007 ¶ 156).

Patent Owner is correct that Svensson discloses benefits to filling its intermediate storage area. For example, Svensson discloses that "it should be understood that the system will operate more efficiently when the intermediate storage area is always filled. This means that if the blocks to be loaded are smaller than this area, a transfer of several (smaller) blocks should be done at the same time." Ex. 1010, 6:32–37. Svensson also discloses that "fewer large transfers are typically preferable to more small transfers" and that "[a] kept-full intermediate storage area can make the most efficient use of the available bandwidth by advantageously minimizing overhead on the communications channel." Ex. 1010, 6:50–57. As Petitioner points out, however, "Svensson describes transferring data in the context of its disclosed file format." Pet. Reply 44. Petitioner's obviousness contentions are based on Bauer's file format, as discussed above.

Petitioner argues that "Bauer teaches that this approach 'simplifies optimization' and 'makes memory loading efficient.'" 1335 Pet. 25 (quoting Ex. 1009 ¶ 43; citing Ex. 1009 ¶¶ 16, 27). Bauer discloses the following:

> Having information about the sections collected in the header 102 and section information 104 simplifies optimization in a number of circumstances, for instance, if sections are to be

loaded into memory. The block 104 lists all sections, preferably in order of memory location, and *this makes memory loading efficient as there is no need to search through an image for section headers when loading*.

Ex. 1009 ¶ 43 (emphasis added). Under Patent Owner's theory, Svensson's file format would be used for transferring data from the primary processor to the secondary processor. PO Resp. 42 (citing Ex. 1010, 6:15–18, 6:20–24, Fig. 3; Ex. 2007 ¶¶ 114–115). For this procedure, Svensson discloses the following:

> As described above, the host fills the intermediate storage area in the memory 108 with code and data that the slave further copies to end destinations in the slave-private memory 110. Perhaps the simplest way of doing this is to precede all code and data in the intermediate storage area with a tag that contains the destination address and length of the block to be loaded. FIG. 3 depicts one example of such an organization of the intermediate storage area. A block of code and/or data to be transferred into the intermediate storage area includes a header that indicates the length of the block and where it is to be loaded in the slave memory, i.e., the destination address. As indicated by the dashed lines in FIG. 3, several such blocks may be concatenated in the intermediate storage area

Ex. 1010, 6:12–25. Thus, according to the teachings of Svensson upon which Patent Owner relies, multiple blocks are put into the intermediate storage area, and each block has a header containing loading information. *See* PO Resp. 44 ("The host processor would use the offset, length, and load address information to generate headers for individual blocks, with each header including a length and destination address for a respective block, as shown in Fig. 3 of Svensson."). This, however, runs counter to Bauer, which discloses that "[t]he section information contains the information for all sections, *which is more advantageous than having each section include*

37

its own information, i.e., the information is concentrated rather than distributed across the sections." Ex. 1009 ¶ 27 (emphasis added). Thus, Bauer teaches that it is advantageous to have section information in one place, rather than spread out among different sections or blocks, as taught in Svensson's file format. In this context, Bauer discloses that "[i]nformation about the sections is located in a header and section information at, for example, the beginning of the image, and so the information about the sections can be retrieved before the sections are read." Ex. 1009 ¶ 30. Thus, although a person of ordinary skill in the art could use Svensson's file format for loading, this ignores Petitioner's proposed combination, which is that a person of ordinary skill in the art would have been motivated to use Bauer's file format, and we agree with Petitioner based on Bauer's teachings of certain advantages to using its file format for memory loading. Ex. 1009 ¶¶ 16, 27, 43.

Patent Owner also argues that Petitioner misunderstands Bauer's disclosure of retrieving section information before reading the sections. PO Resp. 65–66. According to Patent Owner, Bauer's disclosure that "the information about the sections can be retrieved before the sections are read" (Ex. 1009 ¶ 30) does not mean that the intermediate storage area in the secondary processor receives the header and section information separately from and before the data segments. PO Resp. 65. Rather, citing the testimony of Dr. Rinard, Patent Owner argues that a person of ordinary skill in the art "would understand that the header 102 and section information 104 of the image are retrieved before the data sections 106 at two steps in Svensson's bootloading process"—(1) when the primary processor reads the header and section information to determine the size of the image to transfer

and (2) when the secondary processor reads the header and section information before loading the data sections from the intermediate storage area to the destinations in memory. PO Resp. 66 (citing Ex. 2007 ¶¶ 157–158). According to these arguments, data would be reformatted to Svensson's format for transmission from the primary processor to the secondary processor. As discussed above, however, this ignores the proposed combination and Bauer's express teachings of a file format used for program loading "with a program loader reading the stored information and processing stored sections *accordingly*," i.e., according to Bauer's file format. Ex. 1009 ¶ 31 (emphasis added).

*ii. Findings and conclusions for
the first receiving limitation*

Having considered the full trial record, we are persuaded by Petitioner's contention that receiving the image header and each data segment separately at the secondary processor would have been obvious to a person of ordinary skill in the art based on the combined teachings of Bauer and Svensson. We find that paragraph 31 of Bauer provides an express teaching to use Bauer's file format in the program loader of Svensson. Ex. 1009 ¶ 31 ("One example of such a program loader is described in U.S. patent application Ser. No. 11/040,798 filed on Jan. 22, 2005, by M. Svensson et al. for 'Operating-System-Friendly Bootloader'."). We further find that a person of ordinary skill in the art would have been motivated to transfer an image from a primary processor to a secondary processor using Bauer's file format based on Bauer's disclosure. *See* 1335 Pet. 40–41 (citing Ex. 1009 ¶¶ 16, 27, 31, 43; Ex. 1020 ¶ 129). As discussed above, Bauer discloses that "[o]bject code and data can also be stored in this file format,

with a program loader reading the stored information and processing stored

sections accordingly," and Bauer identifies the program loader of Svensson

as "[o]ne example of such a program loader." Ex. 1009 ¶ 31.

Furthermore, we are persuaded that receiving the image header and

each data segment separately at the secondary processor would have been

obvious to a person of ordinary skill in the art. *See* 1335 Pet. 45–47 (citing

Ex. 1009, code (57), ¶¶ 28–30, 43, 47, Figs. 1A–1C; Ex. 1010, 5:28–36,

5:53–6:33, 6:67–7:2; Ex. 1020 ¶¶ 139–142). Bauer discloses that

"[i]nformation about the sections is located in a header and section

information at, for example, the beginning of the image, and so the

information about the sections *can be retrieved before the sections are*

read." Ex. 1009 ¶ 30 (emphasis added). Referring to this disclosure of

Bauer, Dr. Lin testifies as follows:

> A person of ordinary skill in the art would understand from
> Bauer and Svensson combined that "retrieving" the header and
> section information before the data segments are read and
> processed means that the secondary processor's hardware buffer
> (intermediate storage area) receives the header and section
> information **separately** from (and before) the data segments are
> transferred.

Ex. 1020 ¶ 140. We credit this testimony because it is consistent with

Bauer's disclosure of the benefits of having section information collected in

one place rather than scattered throughout the intermediate storage area. In

particular, Bauer explains that "[t]he section information contains the

information for all sections, *which is more advantageous than having each*

section include its own information, i.e., the information is concentrated

rather than distributed across the sections." Ex. 1009 ¶ 27 (emphasis added).

Bauer further discloses that "this makes memory loading efficient as there is

no need to search through an image for section headers when loading."
Ex. 1009 ¶ 43.

As discussed in the previous section, we are persuaded by Petitioner's
contentions and evidence, and we find that the combination of Bauer and
Svensson teaches the remaining subject matter in this limitation. Having
considered the full trial record, we conclude that the following subject
matter recited claim 10 would have been obvious based on the combined
teachings of Bauer and Svensson:

> receiving at a secondary processor, from a primary processor via
> an inter-chip communication bus, an image header for an
> executable software image for the secondary processor that is
> stored in memory coupled to the primary processor, the
> executable software image comprising the image header and at
> least one data segment, the image header and each data segment
> being received separately.

Petitioner further argues that receiving the image header and each data
segment separately at the secondary processor would have been obvious to a
person of ordinary skill in the art based on the combined teachings of Bauer,
Svensson, and Kim. 1335 Pet. 47–52. Petitioner argues Kim discloses a
loading process in which the secondary processor receives program block
header information before and separate from a program block. 1335 Pet.
48–50 (citing Ex. 1012, 5:9–6:5, Fig. 3). Patent Owner argues that "Kim
does not disclose an image header associated with the entire image" and that
"Kim only discloses blocks of data, with each block having its own header,"
similar to Svensson. PO Resp. 49 (citing Ex. 1012, 4:13–21; Ex. 2007
¶ 128). Petitioner, however, relies on Bauer to teach the image header, as
discussed above. Petitioner relies on Kim to teach receiving a header
separately from the data "[t]o the extent the Patent Owner contends that

Bauer and Svensson combined does not teach this claim feature."

1335 Pet. 47. We are persuaded by Petitioner's contention that Kim teaches

a secondary processor receiving a header separately from a program block

based on Kim's disclosure that

> the booter transmits a message for requesting program block
> header information needed for the loading to the system startup
> loader (S304). When the message is received, the system startup
> loader transmits the program block header information to the
> booter (S305). When the header information is received, the
> booter requests a program block corresponding to actual program
> content from the system startup loader (S307). The system
> startup loader receives the request from the booter (S308). The
> system startup loader transmits the program block to the booter
> (S309) . . . .

Ex. 1012, 5:16–6:2. Thus, Kim teaches receiving header information at a

secondary processor separately from the corresponding data. We have

already concluded that this subject matter would have been obvious based on

the combined teachings of Bauer and Svensson, and we conclude likewise

that it would have been obvious based on the combined teachings of Bauer

and Svensson additionally in view of Kim, which provides additional record

evidence supporting Petitioner's contention that it was known in the prior art

to receive header information separately from the corresponding data.

b) *Processing the image header and receiving each data segment*

Claim 10 further recites "processing, by the secondary processor, the

image header to determine at least one location within system memory to

which the secondary processor is coupled to store each data segment" and

"receiving at the secondary processor, from the primary processor via the

inter-chip communication bus, each data segment."

Citing Bauer's teachings of section information with load addresses for data segments and Svensson's teachings of loading data to a secondary processor's memory, Petitioner argues a person of ordinary skill in the art would have understood that the secondary processor processes the image header to determine the location in system memory at which to store each data segment. 1335 Pet. 53–55 (citing Ex. 1009, code (57), ¶¶ 28–30, 32, 34–36, 47, Figs. 1A–1C, 2; Ex. 1010, 3:49–4:8, 5:21–28, 5:65–67, 6:12–15, Figs. 1, 2; Ex. 1020 ¶¶ 152–156). Patent Owner does not dispute Petitioner's contentions for this limitation.

We are persuaded by Petitioner's contentions and evidence, and we find that the combination of Bauer and Svensson teaches processing the image header, as recited in claim 10. In particular, Bauer discloses a file format with section information having load addresses for data segments, and Bauer explains that "an operating system memory manager can load and unload sections of memory according to images in this format." Ex. 1009 ¶¶ 31, 34.

Referring to its discussion of receiving header and data segments separately, Petitioner argues the combination of Bauer and Svensson teaches "receiving at the secondary processor, from the primary processor via the inter-chip communication bus, each data segment." 1335 Pet. 55 (citing Ex. 1020 ¶ 157). Patent Owner does not dispute Petitioner's contentions for this limitation. We are persuaded by Petitioner's contentions and evidence, and we find that the combination of Bauer and Svensson teaches this limitation because, as discussed above, Svensson discloses a program loader for loading data from a host processor to a client processor and Bauer

discloses a file format that can be used in the program loader of Svensson. *See*, *e.g.*, Ex. 1010, Fig. 2; Ex. 1009 ¶ 31.

> *c) Scatter loading each data segment directly to system memory*

Claim 10 further recites "scatter loading, by the secondary processor, each data segment [directly] to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header." Petitioner argues the combination of Bauer and Svensson teaches such scatter loading based on Bauer's disclosure that each data section has an associated destination address and that these sections can be in any order, including an arbitrary order. 1335 Pet. 56–57 (citing Ex. 1009 ¶¶ 36–37, Figs. 1A–1C; Ex. 1010, 5:21–28, 5:65–67, 6:12–15, Figs. 2, 3; Ex. 1020 ¶¶ 158–160).

Patent Owner makes two arguments for this limitation: (1) that the combination of Bauer and Svensson does not teach direct loading (PO Resp. 50–58), and (2) that Petitioner has not shown that the combination of Bauer and Svensson teaches scatter loading (PO Resp. 58–61).

> *i. Direct loading*

Patent Owner argues that the '949 patent distinguishes its loading technique from those that use a temporary buffer, and, citing the testimony of Dr. Rinard, Patent Owner argues that "avoiding use of the temporary buffer makes the scatter loading 'direct.'" PO Resp. 50–51 (citing Ex. 1001, 4:43–47; Ex. 2007 ¶¶ 132–133). Much of Patent Owner's argument here is based on a distinction between a "hardware buffer" and a "temporary buffer" in memory. *See* PO Resp. 51–56. As we discuss above in section addressing claim construction, we agree with Patent Owner that the '949 patent distinguishes a "hardware buffer" from a "temporary buffer" in

memory. Claim 10, however, does not recite a "hardware buffer." Patent Owner argues that the '949 patent "seeks to avoid" an "intermediate buffering step." PO Resp. 53. To the contrary, Figure 3 of the '949 patent, upon which Patent Owner relies, shows buffering in a "hardware buffer."

Patent Owner further argues that, in Figure 1 of Svensson, "there is no access path for directly transferring data from the host processor to target memory locations in the DSP XRAM." PO Resp. 57 (citing Ex. 1010, Fig. 1; Ex. 2007 ¶ 135). The '949 patent, however, does not show any such direct path from host processor to system memory either; rather, Figure 3 of the '949 patent shows data going through a "hardware buffer" in the secondary processor before being put into system memory. Ex. 1001, Fig. 3.

We note that, during prosecution, the applicants distinguished the subject matter of claim 1 from Svensson's disclosure based in part on the recitation of a "hardware buffer." Ex. 1005, 9. The applicants further stated:

> Applicants have demonstrated above that Svensson fails to teach or suggest various elements recited in claim 1. Therefore, claim 1 is believed to be allowable over the cited reference. Furthermore, the independent claims 11, 17, 19, 21, and 23 also recite separately receiving the image header and each data segment and scatter loading each received data segment *directly from the hardware buffer to the system memory*.

Ex. 1005, 9 (emphasis added). Independent claims 11, 17, 19, 21, and 23 during prosecution correspond, respectively, to issued independent claims 10, 16, 18, 20, and 22. These claims, however, did not during prosecution, and do not now, recite a "hardware buffer." *See* Ex. 1005, 4–7 (listing of claims).

Svensson discloses that "the host fills the intermediate storage area in the memory 108 with code and data that the slave further copies to end destinations in the slave-private memory 110." Ex. 1010, 6:12–15. This loading is as "direct" as the '949 patent's description of going through a buffer, albeit a "hardware buffer," which is not required in claim 10. Stated differently, in both the '949 patent and in Svensson, data are received at some location in the secondary processor first before they are directly loaded, and claim 10 does not specify that that location must be a hardware buffer. Furthermore, Patent Owner's argument that the prior art teaches copying from one system memory location to another, even if true, implies that this is prohibited by the claims. *See* PO Resp. 56 (distinguishing Bauer and Svensson where "data is first loaded into one part of system memory and then copied to another part of system memory"). Claim 10 does not limit the claims to exclude such loading. Claim 12, however, depends from claim 10 and recites "further comprising loading the executable software image directly from a hardware buffer to the system memory of the secondary processor *without copying data between system memory locations*" (emphasis added). Thus, claim 12, not claim 10, limits the claim to exclude such copying.

Therefore, we are persuaded by Petitioner's contentions and evidence, and we find that the combination of Bauer and Svensson teaches direct loading.

ii. Scatter loading

Petitioner argues that the combination of Bauer and Svensson teaches "scatter loading" because

> Bauer discloses that each data segment (section) (1) has its own load (or destination) address in the section information specifying where the data segment is to be placed in the system memory and (2) can be arranged in the image in any suitable order (*e.g.,* "in order of the section load addresses" or in "an arbitrary order").

1335 Pet. 56–57 (citing Ex. 1009 ¶ 37). According to Petitioner, a person of ordinary skill in the art "would understand from this disclosure that Bauer teaches that the data segments can be loaded in contiguous or non-contiguous locations of the system memory, and thus the data segments are 'scatter loaded.'" 1335 Pet. 57 (citing Ex. 1020 ¶ 60; Ex. 1001, 9:12–15, 9:21–41).

Patent Owner argues that Petitioner has not shown that scatter loading would have been obvious based on the combination of Bauer and Svensson. PO Resp. 58–60; *see also* Tr. 70:5–8 (Patent Owner stating that, for "scatter loading," "[t]he argument that we are making here is essentially a failure of proof in the petition"). According to Patent Owner, "Bauer merely discloses that data sections may be arbitrarily placed in the binary data image 100 of Figs. 1A-1C" but does not disclose "how data sections are loaded or placed in the XRAM (*i.e.*, the purported 'system memory')." PO Resp. 60 (citing Ex. 2007 ¶¶ 147–149).

Having considered the entire trial record, we are persuaded Petitioner has met its burden to show that scatter loading would have been obvious based on the combined teachings of Bauer and Svensson. As discussed above, Bauer discloses a file format in which all section information, including load addresses, "is collected together in the image" and "precede[s] the data 106 of the section(s) in the image 100." Ex. 1009 ¶¶ 37–38, Figs. 1A–1C. Bauer further discloses:

> Having information about the sections collected in the header 102 and section information 104 simplifies optimization in a number of circumstances, for instance, if sections are to be loaded into memory. The block 104 lists all sections, preferably in order of memory location, and *this makes memory loading efficient as there is no need to search through an image for section headers when loading.*

Ex. 1009 ¶ 43 (emphasis added). Thus, Bauer discloses having load addresses for each section to know where the section should be loaded into memory. As Petitioner points out (1335 Pet. 56–57), Bauer discloses that its "sections may be in an arbitrary order." Ex. 1009 ¶ 37. Patent Owner argues that this disclosure describes how data sections are arranged in an image, rather than in memory. PO Resp. 59–60. Bauer, however, further discloses that, "[a]s each section has a respective load address, the sections can appear in any order (e.g., by size, coding type, or whatever is suitable)." Ex. 1009 ¶ 37. And, according to Bauer, having all section information, including load addresses, collected in one place "makes memory loading efficient as there is no need to search through an image for section headers when loading." Ex. 1009 ¶ 43. This disclosure of Bauer is consistent with the applicants' characterization of "scatter loading" during prosecution, in which the applicants distinguished claim 1 from Svensson's disclosure by arguing the following:

> [C]laim 1 recites that each data segment is scatter loaded based at least in part on the loaded image header. That is, the individual data segments of claim 1 are not concatenated with the header files. Rather, the image header file is loaded into memory to scatter load *each data segment directly* from the hardware buffer to the system memory.

Ex. 1005, 9. Consistent with this characterization of "scatter loading," Bauer discloses collecting all section information together for many sections

in an image, rather than having a separate header with load information for each data section, for the purpose of loading the sections to memory.

Based on the foregoing, we are persuaded by Petitioner's contentions and evidence, and we conclude that "scatter loading" would have been obvious to a person of ordinary skill in the art based on the combined teachings of Bauer and Svensson.

Furthermore, Petitioner notes that "[t]he '949 patent admits that scatter loading is prior art." 1335 Pet. 56 n.19 (citing Ex. 1001, 2:35–41). The '949 patent discloses the following in its "Background" section:

> Thus, where an intermediate buffer is used, the data being downloaded from a primary processor to a secondary processor is copied into the intermediate buffer. In this way, the buffer is used to receive part of the image data from the primary processor, and from the buffer the image data may be scattered into the memory (e.g., volatile memory) of the secondary processor.

Ex. 1001, 2:35–41. During deposition, Patent Owner's declarant, Dr. Rinard, testified, "I think the general concept of scatter loading was known prior to the '949 patent, yes." Ex. 1022, 37:3–5, *quoted in* Pet. Reply 41–42. Patent Owner argues that "whether a claim limitation was supposedly known at the time of the invention is irrelevant. What matters is whether the limitation is taught or suggested by the *prior art cited in the petition*." PO Sur-reply 30. Contrary to Patent Owner's position, however, the Federal Circuit has stated that "[a]lthough the prior art that can be considered in inter partes reviews is limited to patents and printed publications, it does not follow that we ignore the skilled artisan's knowledge when determining whether it would have been obvious to modify the prior art." *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020). Rather, "the inquiry into whether any 'differences' between the invention and the

prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan's knowledge." *Id.* The record shows that scatter loading was within the knowledge of a person of ordinary skill in the art at the relevant time, further supporting Petitioner's contention, and our conclusion, that the claimed subject matter would have been obvious.

iii. Conclusion as to the scatter loading limitation

Based on the foregoing discussions and having considered the full trial record, we are persuaded by Petitioner's contentions and evidence, and we conclude that "scatter loading, by the secondary processor, each data segment [directly] to the determined at least one location within the system memory, and each data segment being scatter loaded based at least in part on the processed image header" would have been obvious to a person of ordinary skill in the art based on the combined teachings of Bauer and Svensson.

d) Determination of unpatentability of independent claim 10

Having considered the full record developed during trial and for the reasons discussed above, Petitioner has demonstrated by a preponderance of the evidence that claim 10 of the '949 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, and Kim.

6. Dependent Claims 11 and 13–15

Claims 11 and 13–15 depend from independent claim 10. Petitioner presents persuasive arguments and evidence showing how the combination of Bauer, Svensson, and Kim teaches the subject matter recited in these claims. *See* 1335 Pet. 57–60, 63–67.

Claim 11 recites, "The method of claim 10 further comprising booting the secondary processor using the executable software image." Petitioner contends the subject matter of claim 11 would have been obvious based on Svensson's disclosure of loading "boot code" to the memory of the secondary processor and Bauer's disclosure of using Svensson's program loader to load an executable image in Bauer's file format. 1335 Pet. 58–60 (citing Ex. 1010, 4:9–14, 4:20–6:11, 8:12–16, Fig. 2; Ex. 1009 ¶ 31; Ex. 1020 ¶¶ 162–165). Petitioner contends a person of ordinary skill in the art "would have understood that the loaded 'boot code' would execute as part of the booting process of the secondary processor." 1335 Pet. 60 (citing Ex. 1020 ¶ 164).

Claim 13 recites, "The method of claim 10 in which the processing occurs prior to the loading." Referring to its contentions for claim 10 that it would have been obvious to receive the image header separately from and before the data, Petitioner argues that processing the header prior to loading would have been obvious so as to determine the destination address for each data segment. 1335 Pet. 63–64.

Claim 14 recites, "The method of claim 10 in which the primary and secondary processors are located on different chips." Referring to its contentions for claim 10, Petitioner contends that the combination of Bauer and Svensson teaches that the ARM device (primary processor) and DSP device (secondary processor) are on different chips. 1335 Pet. 65; *see* 1335 Pet. 33–35 (providing detailed explanation as to how the combination of Bauer and Svensson teaches or renders obvious separate chips).

Claim 15 recites,

> The method of claim 10 further comprising performing the receiving, processing, and loading, in at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

Petitioner contends this subject matter would have been obvious to a person of ordinary skill in the art, citing various disclosures in Bauer and Svensson of using the disclosed techniques in computers and mobile phones. 1335 Pet. 66–67 (citing Ex. 1009 ¶¶ 15, 16, 26; Ex. 1010, 7:61–63, 8:26–29).

Patent Owner does not separately address the additional limitations recited in claims 11 and 13–15. *See generally* PO Resp.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 11 and 13–15 of the '949 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, and Kim.

7. Claims 22 and 23

Independent claim 22 recites the following:

A method comprising:

> sending, from a memory coupled to a primary processor, an executable software image for a secondary processor, via an interface communicatively coupling the primary processor and secondary processor, the executable software image comprising an image header and at least one data segment;

> receiving, at the secondary processor, the image header and each data segment of the executable software image, the image header and each data segment being received separately,

52

and the image header being used to scatter load each received data segment directly to a system memory of the secondary processor; and

executing, at the secondary processor, the executable software image.

The sending and receiving limitations of claim 22 recite subject matter similar to claim 10. Although claim 10 does not recite sending from a memory coupled to a primary processor, claim 10 recites receiving the same information from the primary processor. Petitioner argues that a person of ordinary skill in the art "would understand from the teaching of a secondary processor receiving an image from a primary processor, that this means that the primary processor is sending the image to the secondary processor." Pet. 72 (citing Ex. 1010, 6:12–15).

The sending limitation of claim 10 also recites sending the data from the primary processor to the secondary processor "via an interface communicatively coupling the primary processor and secondary processor," rather than "via an inter-chip communication bus," as recited in claim 10. Petitioner identifies the same disclosures of Bauer and Svensson to teach the "interface" for claim 22 that it identifies for the "inter-chip communication bus" in claim 10. Pet. 51–52, 72.

The "receiving" limitation of claim 22 recites subject matter similar to subject matter recited in claim 10 and discussed above, including several disputed limitations—receiving image header and data segments separately, direct loading, and scatter loading. Petitioner relies on the same prior art and arguments for its contentions for the "receiving" limitation of claim 22 as it relies on for similar subject matter in claim 10. Pet. 73–74. We have

addressed Petitioner's contentions and Patent Owner's arguments as to this subject matter with respect to claim 10.

Claim 22 further recites "executing, at the secondary processor, the executable software image." This limitation is not recited in claim 10. Petitioner contends that a person of ordinary skill in the art "would understand from the teachings of Bauer and Svensson combined that the point of sending an executable software image to a secondary processor is so that the secondary processor can execute the executable software image. Svensson further teaches executing an executable software image at the secondary processor (DSP device)." Pet. 74 (citing Ex. 1010, 6:6–11, 8:12–16; Ex. 1002 ¶ 201).

Claim 23 recites,

> The method of claim 22 further comprising performing the sending, receiving, and executing, in at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

This claim recites subject matter similar to claim 15, and Petitioner's contentions are similar to those for claim 15, which we discuss above. Pet. 70–71, 75.

Patent Owner does not raise additional arguments concerning claims 22 and 23 but, rather, argues that Petitioner's contentions fail for the reasons addressed above with respect to claim 10. *See generally* PO Resp. 33–69. We are persuaded by Petitioner's contentions for claims 22 and 23 for the reasons discussed in this section and with respect to claims 10 and 15.

Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 22 and 23 of the '949 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, and Kim.

8. Claims 1–9 and 12

Independent claim 1 and its dependent claims 2–9 and claim 12, which depends from claim 10, are the remaining claims that Petitioner challenges based on the combination of Bauer, Svensson, and Kim. Independent claim 1 recites "[a] multi-processor system comprising: a secondary processor comprising: system memory and *a hardware buffer* for receiving an image header and at least one data segment of an executable software image," and it further recites a scatter loader controller "to scatter load each received data segment based at least in part on the loaded image header, *directly from the hardware buffer to the system memory*" (emphases added). Claim 12 recites "loading the executable software image directly from a hardware buffer to the system memory of the secondary processor without copying data between system memory locations." Thus, claim 1, claims 2–9 by virtue of their dependency from claim 1, and claim 12 all require a "hardware buffer."

Petitioner argues that the intermediate storage area of Bauer and Svensson teaches the claimed "hardware buffer." Pet. 27; 1335 Pet. 61. Patent Owner argues that the intermediate storage area of Bauer and Svensson is a temporary buffer and, therefore, does not teach the claimed "hardware buffer." PO Resp. 41–42, 55. We agree with Patent Owner.

Svensson discloses that the intermediate storage area is reserved at runtime of the program loader in the following passage:

> The idle process reserves a block of memory in the slave's heap of memory that is located in the memory visible to the host, such as "internal" memory 108 (Step 212). As described in more detail below, this reserved block of memory is used for intermediate storage of information (code and/or data) to be transferred to the slave-private memory, i.e., the memory that is invisible to the host, such as "external" XRAM 110.

Ex. 1010, 5:21–29; s*ee* Tr. 19:19–25 (Petitioner agreeing that "the intermediate storage area in Svensson and Bauer is allocated by the secondary processor at the time that the program loader is operating"). Thus, we find that the intermediate storage area of Bauer and Svensson is a temporary buffer.

As discussed above in addressing the broadest reasonable interpretation of "hardware buffer," we conclude that the "hardware buffer" limitations of claims 1–9 and 12 do not encompass the use of a temporary buffer. Because Petitioner relies on a temporary buffer to teach the claimed "hardware buffer," we determine Petitioner has not proven unpatentability of claims 1–9 and 12 by a preponderance of the evidence.

E. Obviousness over Bauer, Svensson, Kim, and Lim (Claims 18–21)

Petitioner contends claims 18–21 of the '949 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, Kim, and Lim. 1336 Pet. 26–75.

1. Lim

Lim is directed to initializing a coprocessor in a system having a main processor and a coprocessor. Ex. 1014, code (57), 1:21–25. Lim discloses various memories coupled to the main processor and the coprocessor that

56

can store boot programs and file systems. *See, e.g.*, Ex. 1014, 5:47–58, 6:2–7, 6:39–42, Figs. 1, 3.

2. Claims 18–21

Much of the subject matter recited in independent claims 18 and 20 is recited in independent claims 10 and 22, which we have discussed above. Patent Owner does not raise additional arguments concerning claims 18–21 but, rather, argues that Petitioner's contentions fail for the reasons addressed above with respect to claim 10. *See generally* PO Resp. 33–69. Below we address subject matter recited in independent claims 18 and 20 that is not present in independent claims 10 and 22.

Claim 18 recites "a first non-volatile memory coupled to the primary processor and *storing a file system for the primary processor* and executable images for the primary processor and secondary processor" (emphasis added). Bauer and Svensson disclose a "non-volatile memory" coupled to the "ARM CPU" (primary processor). Ex. 1009, Fig. 2; Ex. 1010, Fig. 1. Citing various teachings from Bauer and Svensson and the testimony of Dr. Lin, Petitioner contends that a person of ordinary skill in the art "would understand that Bauer and Svensson combined teaches a file system for the primary processor (ARM device) that would be stored in the first non-volatile memory." 1336 Pet. 30–31 (citing Ex. 1009 ¶ 3; Ex. 1010, 7:47–51; Ex. 1021[13] ¶ 109). Petitioner additionally asserts that Lim teaches storing a file system for the primary processor in non-volatile memory. 1336 Pet. 33–36. For example, Lim discloses a flash memory for "storing a

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[13] This exhibit was originally filed as Exhibit 1202 in IPR2018-01336. After consolidation, it was filed as Exhibit 1021. *See* Paper 15 (Joint Identification of Exhibits).

boot module, a loader module, a flash file system, and other execution program modules of the main processor 100." Ex. 1014, 6:39–42, *cited in* 1336 Pet. 35. Petitioner provides various reasons that a person of ordinary skill in the art would have been motivated to combine these teachings of Lim with the teachings of Bauer and Svensson and supports its reasoning with testimony from Dr. Lin. 1336 Pet. 36–39 (citing Ex. 1021 ¶¶ 120–124).

Independent claim 18 further recites "a secondary processor coupled with a second non-volatile memory, the second non-volatile memory coupled to the secondary processor and storing configuration parameters and file system for the secondary processor." Petitioner acknowledges that Bauer and Svensson do not teach the second non-volatile memory. 1336 Pet. 39. Citing Lim's disclosure of storing initialization information, including a boot program and a file system, for a coprocessor in a flash memory, Petitioner argues Lim teaches a "second non-volatile memory coupled to the secondary processor and storing configuration parameters and file system for the secondary processor." 1336 Pet. 39–41 (citing Ex. 1014, 1:42–47, 2:3–13, 5:23–25, 5:43–6:7, 6:28–30, 7:27–33, 7:41–47, 7:53–55, 10:12–18, 11:10–16, Figs. 1, 3; Ex. 1021 ¶¶ 125–127). For example, Lim discloses the following:

> The embodiments of the present invention remove a flash memory for storing initialization information of a coprocessor from a system, the system including a main processor and the coprocessor, and stores initialization information of the coprocessor in either *another memory of the coprocessor*, or a memory of the main processor, such that the system initialization is established. The memory can be either one of a ROM, a RAM, first and second flash memories, and similar devices. The initialization information can be either one of a *boot program*

> *module, a loader program, a boot loader program, and a tiny*
> *flash file system of the coprocessor.*

Ex. 1014, 5:47–58 (emphases added). Lim further discloses that

"[i]nitialization information of the auxiliary device, for example, a boot

program, a loader program, a boot-loader program, and tiny flash file

systems, can be stored in an internal ROM of the coprocessor." Ex. 1014,

6:2–5. Dr. Lin testifies as follows:

> A person of ordinary skill in the art would understand from
> Lim's teaching that the initialization information includes, in
> addition to a file system, "configuration parameters" for the
> secondary processor (coprocessor). In particular, the person of
> ordinary skill in the art would understand that the initialization
> information, such as the boot, loader and boot-loader programs,
> includes data needed to configure and initialize the secondary
> processor during the boot process. The person of ordinary skill
> in the art would understand this well-known type of data to be
> "configuration parameters."

Ex. 1021 ¶ 128.

Petitioner argues a person of ordinary skill in the art would have been

motivated to combine the teachings of Bauer and Svensson with Lim's

teachings of storing configuration parameters and a file system for a

secondary processor in a non-volatile memory coupled to the secondary

processor because the person of ordinary skill in the art

> would . . . have understood that (1) configuration parameters
> were necessary to configure and initialize a processor during the
> boot process as taught by Lim, and (2) file systems were
> necessary to control how file formats such as COFF [(Common
> Object File Format)] and ELF [(Executable and Linking
> Format)] are stored and retrieved from memory as taught by
> Bauer and Svensson combined.

1336 Pet. 44 (citing Ex. 1021 ¶ 133).

The remaining limitations of claim 18 recite subject matter that is substantively the same as limitations discussed with respect to claims 10 and 22.

Independent claim 20 recites "a first non-volatile memory coupled to the primary processor and storing executable images and file systems for the primary and secondary processors." This differs slightly from the "first non-volatile memory" of claim 18 in requiring the memory to store file systems for both the primary processor and the secondary processor. Petitioner argues that "Lim discloses that the initialization information of the secondary processor (co-processor), which includes 'tiny flash file systems,' can alternatively be stored at the memories of the primary processor (main processor)—internal ROM, the first flash memory, or the second flash memory—instead of in the ROM of the coprocessor." 1336 Pet. 69 (citing Ex. 1014, 5:47–6:7, 7:27–33, 7:53–55, 10:12–18, 11:10–16). For example, Lim discloses that "[i]nitialization information of the auxiliary device, for example, a boot program, a loader program, a boot-loader program, and tiny flash file systems, can be stored in an internal ROM of the coprocessor, an internal ROM of the main processor, the first flash memory or the second flash memory." Ex. 1014, 6:2–7. Petitioner provides reasons to combine this teaching with the teachings of Bauer and Svensson similar to its reasons for claim 18. 1336 Pet. 70–71 (citing Ex. 1021 ¶¶ 181–183).

Independent claim 20 also recites "a secondary processor *not directly coupled* to the first non-volatile memory" (emphasis added). Petitioner argues that non-volatile memory 206 in Bauer's Figure 2 is directly coupled to the primary processor but not directly coupled to the secondary processor

because there is no access path from the secondary processor directly to non-volatile memory 206. 1336 Pet. 71–72.

Claims 19 and 21 depend, respectively, from claims 18 and 20 and recite,

> The multi-processor system of claim [18, 20] integrated into at least one of a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and a fixed location data unit.

This recites subject matter similar to claim 15, and Petitioner's contentions are similar to those for claim 15, which we discuss above. 1336 Pet. 66–68, 74–75.

As noted above, Patent Owner does not raise additional arguments concerning claims 18–21 but, rather, argues that Petitioner's contentions fail for the reasons addressed above with respect to claim 10. *See generally* PO Resp. 33–69.

We are persuaded by Petitioner's contentions and evidence, discussed above, showing how the combination of Bauer, Svensson, Kim, and Lim teaches the subject matter recited in these claims and showing why a person of ordinary skill in the art would have combined the teachings of the references in the manner asserted. Having considered the full record developed during trial, we are persuaded by Petitioner's contentions and evidence, and we determine that Petitioner has proven by a preponderance of the evidence that claims 18–21 of the '949 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, Kim, and Lim.

F. Obviousness over Bauer, Svensson, Kim, and Zhao
(Claims 16 and 17)

Petitioner contends claims 16 and 17 of the '949 patent are unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Bauer, Svensson, Kim, and Zhao. 1335 Pet. 67–77.

As discussed above in the section addressing claim construction, independent claim 16 recites several limitations in means-plus-function format, and Petitioner takes the position during trial "that the '949 specification fails to disclose sufficient structure to perform the recited functions" for two of the means-plus-function limitations. Pet. Reply 14. To assess Petitioner's obviousness contentions as to claim 16, which recites means-plus-function limitations, we must "engage[] in a comparison of the asserted prior art's disclosure to the 'structure' disclosed in the" specification of the '949 patent. *IPCom GmbH & Co. v. HTC Corp.*, 861 F.3d 1362, 1371 (Fed. Cir. 2017) (citing *In re Donaldson Co., Inc.*, 16 F.3d 1189, 1195 (Fed. Cir. 1994) (en banc)). Thus, we disagree with the parties' contentions (PO Resp. 17; Pet. Reply 14) that we should proceed to evaluate obviousness of claims 16 and 17 in view of the asserted prior art.

Because Petitioner has not met its burden under our Rules to show structure corresponding to the claimed function to which we can compare the prior art's disclosure, we determine Petitioner has not shown, by a preponderance of the evidence, that claim 16 and, by virtue of its dependency, claim 17 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combined teachings of Bauer, Svensson, Kim, and Zhao.

III. CONCLUSION[14]

For the reasons discussed above, we determine Petitioner has proven, by a preponderance of the evidence, that certain of the challenged claims are unpatentable but has not proven, by a preponderance of the evidence, that other claims are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–15, 22, 23	103(a)	Bauer, Svensson, Kim	10, 11, 13–15, 22, 23	1–9, 12
16, 17	103(a)	Bauer, Svensson, Kim, Zhao		16, 17
18–21	103(a)	Bauer, Svensson, Kim, Lim	18–21	
Overall Outcome			10, 11, 13–15, 18–23	1–9, 12, 16, 17

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[14] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

Accordingly, it is:

ORDERED that claims 10, 11, 13–15, and 18–23 of the '949 patent have been shown to be unpatentable;

ORDERED that claims 1–9, 12, 16, and 17 of the '949 patent have not been shown to be unpatentable; and

FURTHERED ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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