UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner

Case IPR2019-00102
U.S. Patent No. 5,943,274

PETITIONER KINGSTON TECHNOLOGY COMPANY, INC.'S NOTICE OF APPEAL

Pursuant to 35 U.S.C §§ 141(c) and 142 and in accordance with 37 C.F.R. § 90.2(a), Petitioner Kingston Technology Company, Inc. ("Petitioner") appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision (attached hereto as Exhibit 1) entered by the Patent Trial and Appeal Board ("the Board") on April 1, 2020.

Petitioner indicates that the issues on appeal include:

- The Board's determination that Petitioner did not show claim 1 of U.S. Patent No. 5,943,274 to be unpatentable by a preponderance of the evidence; and
- Any and all findings or determinations supporting or related to the Board's determination with respect to claim 1.

Simultaneous with this filing and in accordance with 37 C.F.R. § 90.2(a)(1), this Notice of Appeal is (1) filed with the Director of the United States Patent and Trademark Office; (2) filed with the Board; and (3) served upon the Patent Owner in accordance with 37 C.F.R. § 1.248.

Dated: June 3, 2020

Respectfully submitted,

/Robert C.F. Perez/

Robert C.F. Pérez (Reg. No. 39,328)
Christopher Kao (*Pro hac vice*)
Brock S. Weber (*Pro hac vice*)

Attorneys for Petitioner
Kingston Technology Company, Inc.

PILLSBURY WINTHROP SHAW PITTMAN LLP
1650 Tysons Boulevard, 14th Floor
McLean, VA 22102
Telephone: 703.770.7900
Facsimile: 703.770.7901

CERTIFICATE OF SERVICE

I hereby certify that, in addition to being filed and served electronically through the Patent Trial and Appeal Board's E2E System, the original version of the foregoing "**PETITIONER KINGSTON TECHNOLOGY COMPANY INC.'S NOTICE OF APPEAL**" was filed on this 3rd day of June, 2020, with the Director of the United States Patent and Trademark Office, via hand delivery at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22313-1450

I also certify that on this 3rd day of June, 2020, the foregoing "**PETITIONER KINGSTON TECHNOLOGY COMPANY INC.'S NOTICE OF APPEAL**," and the filing fee, were filed with the Clerk's Office of the United States Court of Appeals for the Federal Circuit, via CM/ECF.

The undersigned also hereby certifies that a true copy of the foregoing "**PETITIONER KINGSTON TECHNOLOGY COMPANY INC.'S NOTICE OF APPEAL**" has been served in its entirety this 3rd day of June, 2020, on the counsel of record for the Patent Owner of IPR2019-00102 by filing these

documents through the Patent Trial and Appeal Board's E2E System as well as delivering copies via electronic mail to the following addresses:

Philip E. Levy
Edward C. Flynn
Eckert Seamans Cherin & Mellott, LLC
600 Grant Street, 44th Floor
Pittsburgh, PA 15219
plevy@eckertseamans.com
eflynn@eckertseamans.com

Robert W. Morris
Eckert Seamans Cherin & Mellott, LLC
10 Bank Street, Suite 700
White Plains, NY 10606
rwmorris@eckertseamans.com

/Robert C.F. Perez/
Robert C.F. Pérez (Reg. No. 39,328)

EXHIBIT 1

Trials@uspto.gov
Tel: 571-272-7822

Paper 32
Entered: April 1, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

IPR2019-00102
Patent 5,943,274

Before MICHELLE N. WORMMEESTER, GARTH D. BAER, and STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claim 1 of U.S. Patent No. 5,943,274 (Ex. 1001, "the '274 patent") under 35 U.S.C. §§ 311–319. Under 37 C.F.R. § 42.107(b), North Star Innovations, Inc. ("Patent Owner") waived its Preliminary Response (Paper 6).

In our Institution Decision (Paper 7, "Inst. Dec."), we instituted review based on all challenged claims and all grounds advanced in the Petition. We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner has not shown by a preponderance of the evidence that claim 1 of the '274 patent is unpatentable. *See* 35 U.S.C. § 316(e) (2012).

II. BACKGROUND

A. Procedural History

After we instituted review, Patent Owner filed a Response (Paper 12, "Resp."), Petitioner filed a Reply (Paper 25, "Reply"), and Patent Owner filed a Sur-reply (Paper 30, "Sur-reply"). On January 16, 2020, we held an oral hearing. *See* Paper 31 ("Tr.").

B. Related Proceedings

Petitioner and Patent Owner identify the following civil action where Patent Owner has asserted the '274 patent against Petitioner: *North Star Innovations, Inc. v. Kingston Technology Co.*, No. 8:17-cv-1833 (C.D. Cal. filed Oct. 20, 2017). Pet. 2; Paper 4, 1.

Petitioner and Patent Owner identify other petitions challenging the patentability of claims in other patents asserted by Patent Owner against

Petitioner in the above-identified civil action: IPR2018-01784 (U.S. Patent No. 6,101,145), IPR2018-01794 (U.S. Patent No. 6,917,555), and IPR2019-00104 (U.S. Patent No. 6,127,875). Pet. 2–3; Paper 4, 1.

C. The '274 Patent (Ex. 1001)

The '274 patent, titled "Method and Apparatus for Amplifying a Signal to Produce a Latched Digital Signal," issued on August 24, 1999 from an application filed on February 2, 1998. Ex. 1001, codes (22), (45), (54). The patent has expired. *See* Pet. 32; Resp. 23.

The '274 patent discloses a semiconductor memory with an output stage including a differential amplifier, a level converter, a timing circuit, a clock-free latch, an impedance-control circuit, and an output driver. Ex. 1001, code (57), 2:50–4:13, Fig. 2; *see* Pet. 13. Figure 2 of the '274 patent is reproduced below:

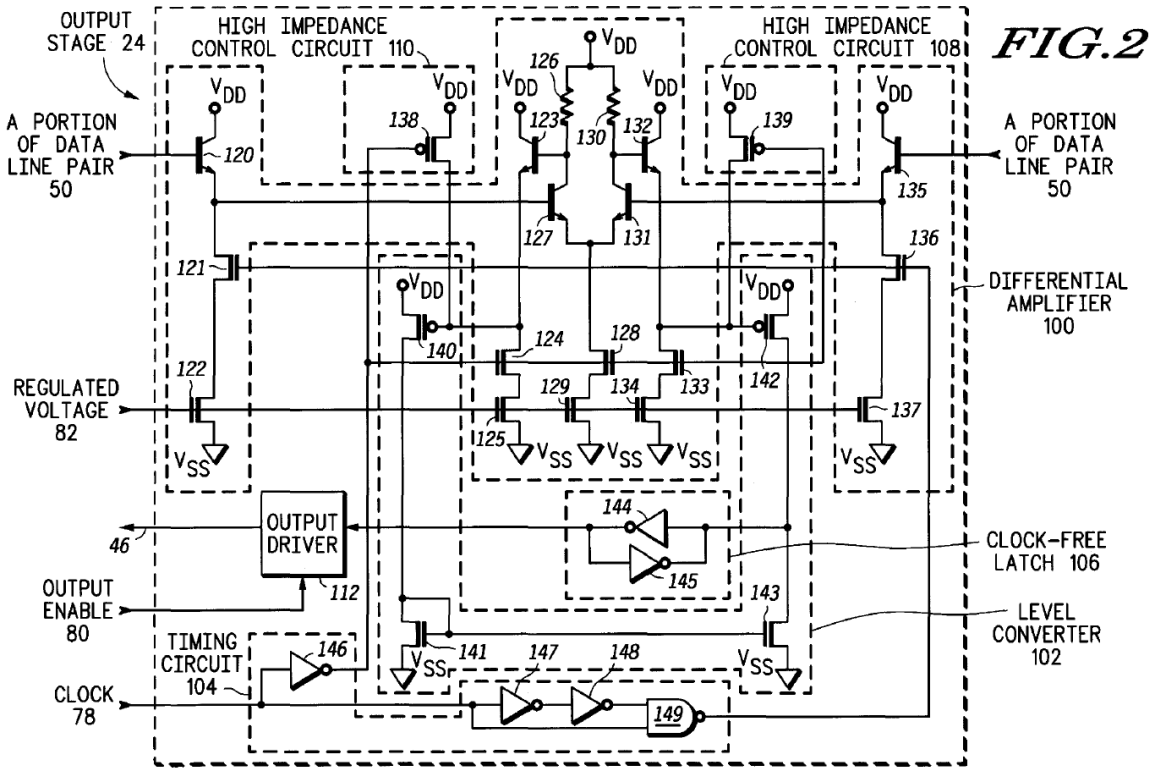


FIG.2

Figure 2 "illustrates in partial block diagram form and partial schematic diagram form" an output stage for a semiconductor memory "in accordance with one embodiment" of the invention. *Id.* at 1:51–53; *see id.* at 2:50–52, 4:48–49.

In Figure 2, the output stage includes the following circuit elements: differential amplifier 100, level converter 102, timing circuit 104, clock-free latch 106, impedance-control circuits 108 and 110, and output driver 112. Ex. 1001, 2:50–57, Fig. 2. Timing circuit 104 receives clock signal 78 as an input. *Id.* at 3:63–4:1, Fig. 2.

The '274 patent contemplates other embodiments of an output stage and other embodiments of the circuit elements illustrated in Figure 2, i.e., circuit elements 100–112. Ex. 1001, code (57), 2:50–3:13, 4:48–51, 5:18–20. For instance, the patent states that Figure 2 "illustrates one embodiment of" an output stage as shown Figure 1. *Id.* at 2:50–52, 4:48–49; *see id.* at 4:49–51. The patent also states that "alternate embodiments of the present invention may use different circuit elements than those illustrated in" Figure 2. *Id.* at 3:11–13. As an example, the patent identifies timing circuit 104 in Figure 2 as "one embodiment" of a timing circuit. *Id.* at 3:4–5.

The '274 patent instructs that semiconductor memories commonly use a differential amplifier and latch as follows. A differential amplifier located "between the bit cell array and the data output signals" detects "a small voltage difference and amplifies that small voltage difference into a larger voltage difference." Ex. 1001, 1:23–29. A latch located "between the differential amplifier and the data I/O pad" latches the data output signals "to provide a consistent logic level one or logic level zero at the data I/O pad

while the differential amplifier is detecting the next data value." *Id.* at 1:29–33.

The '274 patent explains that prior-art circuits "use[d] two clock signals," i.e., "one clock signal to clock the differential amplifier portion, and one clock signal to clock the latch portion of the memory output stage." Ex. 1001, 1:33–37. The patent also explains that using "two clock signals" caused problems because "the timing relationship between the two clocks cannot be consistently controlled due to manufacturing process variations, temperature variations, power supply voltage variations, etc." *Id.* at 1:37–40. The patent purports to solve those problems by providing an output stage "that does not require two or more clocks, and thus does not require that a precise timing relationship between two or more clocks be maintained." *Id.* at 1:40–44.

In particular, the '274 patent instructs that "clock 78 and timing circuit 104" may in "one embodiment" provide two versions of clock signal 78 to differential amplifier 100. Ex. 1001, 5:20–23, 5:26–29; *see id.* at code (57). The two versions selectively enable and disable differential amplifier 100 "to reduce power [consumption] and to increase speed." *Id.* at 5:23–25; *see id.* at code (57), 5:18–20. The two versions "are not separate clock signal[s] as used by the prior art, but are merely different versions of the same clock." *Id.* at 5:34–36.

In addition, the '274 patent explains that in "one embodiment" the two versions "have approximately simultaneous rising [or enabling] edges" and "a delay between their [falling or] disabling edges," i.e., "purposely skewed" disabling edges. Ex. 1001, 5:26–37; *see id.* at code (57). The patent

describes the two versions as "slightly different versions" of the input clock signal. *Id.* at 5:43–44.

But the '274 patent explains that "some embodiments of the present invention may use clock 78 directly as the only clock, without using timing circuit 104 to create two slightly different versions." Ex. 1001, 5:41–44. Further, the patent expressly states that "[t]he present invention merely requires a single clock signal." *Id.* at 5:25–26; *see id.* at code (57).

D. The Challenged Claim

Petitioner challenges claim 1. Pet. 4, 45–67. Claim 1 reads as follows:

> 1. An apparatus for use as an output stage of a memory device, the apparatus comprising:
>
> a timing circuit;
>
> a differential amplifier responsive to the timing circuit;
>
> an impedance control circuit;
>
> a level converter responsive to the differential amplifier and the impedance control circuit; and
>
> a clock-free latch responsive to the level converter.

Ex. 1001, 6:62–7:3.

E. The Asserted Prior Art

For its challenges, Petitioner relies on U.S. Patent No. 5,245,223 to Lim et al., titled "CMOS Latching Comparator," filed on March 17, 1992, and issued on September 14, 1993 (Ex. 1005, "Lim").

F. Testimonial Evidence

To support its challenges, Petitioner relies on two declarations of Bruce Jacob, Ph.D. (Ex. 1003, "Jacob Decl."; Ex. 1020, "Jacob Reply Decl."). Patent Owner relies on the declaration of Sunil P. Khatri, Ph.D.

(Ex. 2001, "Khatri Decl."). The record includes a transcript of Dr. Khatri's deposition (Ex. 1019, "Khatri Dep.") and a transcript of Dr. Jacob's deposition (Ex. 2003, "Jacob Dep.").

G. Asserted Grounds of Unpatentability

We instituted an *inter partes* review of claim 1 on the following grounds:

Claim Challenged	35 U.S.C. §	Reference
1	102(b)[1]	Lim
1	103(a)	Lim

Inst. Dec. 22.

H. Burden

Petitioner bears "the burden of proving . . . unpatentability by a preponderance of the evidence." 35 U.S.C. § 316(e); *see* 37 C.F.R. § 42.1(d) (2018).

III. PATENTABILITY ANALYSIS

A. Level of Ordinary Skill in the Art

Factors pertinent to determining the level of ordinary skill in the art include (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of workers active in the field. *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir.

[1] On September 16, 2012, the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), took effect and amended 35 U.S.C. §§ 102 and 103. Because the '274 patent's filing date predates the AIA's amendments to §§ 102 and 103, this decision refers to the pre-AIA versions of §§ 102 and 103.

1983). Evidence for these factors may not exist in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, these factors are not exhaustive, but are merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). Further, the prior art itself may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Here, Petitioner asserts that a person of ordinary skill in the art would have had "either an undergraduate degree in electrical engineering (or equivalent subject), with at least two years of post-graduate experience designing memory arrays, or a master's degree in electrical engineering (or equivalent subject), with at least one year of post-graduate experience in designing memory arrays." Pet. 33–34 (citing Ex. 1003 ¶ 22); *see* Ex. 1003 ¶ 22. Petitioner also asserts that "a higher level of education could make up for less experience, and vice versa." Pet. 34; *see* Ex. 1003 ¶ 23. Patent Owner states that "[f]or purposes of this proceeding," it "is not challenging Petitioner's proposed definition of" a person of ordinary skill in the art. Resp. 26; *see* Ex. 2001 ¶ 26. Thus, we adopt Petitioner's proposed definition as consistent with the '274 patent and the asserted prior art.

B. Claim Construction

As noted above, the '274 patent has expired. *See* Pet. 32; Resp. 23. Because the '274 patent has expired, we construe disputed claim terms according to the principles articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1279 (Fed. Cir. 2017). Further, the parties agree

that we should construe disputed claim terms according to *Phillips*. *See* Pet. 32; Resp. 23.

According to *Phillips*, claim terms "are generally given their ordinary and customary meaning" as understood by "a person of ordinary skill in the art." *Phillips*, 415 F.3d at 1312–13. "[T]he person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent," including the other claims ("both asserted and unasserted") and the written description. *Id.* at 1313–14, 1321. Further, "the prosecution history can often inform the meaning of the claim language by demonstrating how" an inventor or an examiner understood the claim language. *Id.* at 1317. Thus, the meaning of a disputed claim term may be determined by "look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

To the extent that the parties raise patentability issues requiring claim construction, we address claim construction in our patentability analysis when considering the particular patentability issue. *See infra* § III.C.3(b). We do so to provide better context to explain the dispute about claim construction and our resolution of the dispute.

C. Anticipation by Lim: Claim 1

1. ANTICIPATION UNDER 35 U.S.C. § 102

"[T]o demonstrate anticipation, the proponent must show 'that the four corners of a single, prior art document describe every element of the claimed invention.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359,

1369 (Fed. Cir. 2008) (quoting *Xerox Corp. v. 3Com Corp.*, 458 F.3d 1310, 1322 (Fed. Cir. 2006)). The prior-art document "must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Hence, a patent challenger cannot rely on portions from different embodiments in a prior-art document to demonstrate anticipation. *See id.* at 1369, 1371.

We analyze the anticipation issues according to these principles.

2. OVERVIEW OF LIM (EX. 1005)

Lim discloses a CMOS latching comparator circuit. Ex. 1005, 1:1–10, 3:5–7, 4:6–8, 7:38–39, 7:52–8:6 (claim 1), codes (54) and (57), Figs. 2–3. The acronym CMOS refers to complementary metal-oxide semiconductor. Ex. 1001, 1:28–29. A comparator circuit (1) compares two voltages, often an unknown input voltage and a known reference voltage, and (2) outputs "a digital/binary yes/no decision whether one input is less than or greater than the other." Ex. 1003 ¶ 79. Lim's comparator circuit includes latching capability because the circuit stores a logic state at its output "indefinitely" until an enable or unlatch command occurs. *See* Ex. 1005, 1:25–32, 5:65–6:5, 6:17–25, 6:65–67.

Lim states that the "invention includes a two-stage CMOS latching comparator circuit" with an input stage and a latching stage. Ex. 1005, 1:56–2:25, 7:52–8:6 (claim 1); *see id.* at code (57). Lim describes the latching comparator circuit as useful for, among other things, data-acquisition applications, including analog-to-digital conversion (ADC) applications. *Id.* at 1:5–10, 1:48–51, 2:47–51, 7:38–43.

The latching comparator circuit's input stage includes "a first differential pair of transistors arranged to receive an input voltage VIN and a reference voltage VREF." Ex. 1005, 1:59–62. The input stage also includes "a [first] cross-coupled pair of transistors," with each cross-coupled transistor "coupled between a respective one of the input differential [transistor] pair" and voltage VSS. *Id.* at 1:62–68. The input stage additionally includes "a [first] pair of diode-connected transistors," with each diode-connected transistor "coupled in parallel to a respective one of the first cross-coupled transistors to control gain in the first cross-coupled pair." *Id.* at 1:68–2:3.

The latching comparator circuit's latching stage includes "a second differential pair of transistors, coupled to [voltage] VSS and having input or gate terminals coupled to outputs of the input stage." Ex. 1005, 2:7–10. The latching stage also includes "a second cross-coupled pair of transistors," with each cross-coupled transistor "coupled between a respective one of the second differential [transistor] pair" and voltage VDD. *Id.* at 2:13–15. The latching stage additionally includes "a second pair of diode-connected transistors," with each diode-connected transistor "disposed between a respective one of the second cross-coupled [transistor] pair and a common switch node." *Id.* at 2:16–20.

A digital switch "disposed between the switch node" and voltage VDD selectively couples "the switch node to [voltage] VDD responsive to a binary latch clock signal," i.e., the CLK signal. Ex. 1005, 2:21–25; *see id.* at code (57), Fig. 2. Lim discloses that a "single transistor may be used" as the digital switch. *Id.* at 5:56–57; *see id.* at 7:17–18. Although a "single transistor may be used," Lim explains that a digital switch comprising a

"pair of transistors in parallel" offers advantages, such as "smaller individual device size and layout symmetry." *Id.* at 5:57–59. When using a "pair of transistors in parallel" as the digital switch, the "transistor gates are connected together to receive the latch clock signal," i.e., the CLK signal. *Id.* at 2:21–27, 5:54–56.

Lim's Figures 2 and 3 depict a preferred embodiment comprising various transistors. Ex. 1005, 3:5–7, 4:6–8. In these figures, transistors identified as MP# denote p-channel metal-oxide semiconductor (PMOS) devices, and transistors identified as MN# denote n-channel metal-oxide semiconductor (NMOS) devices. Ex. 1003 ¶¶ 83, 115, 142.

Lim's Figure 2 is reproduced below:

Figure 2

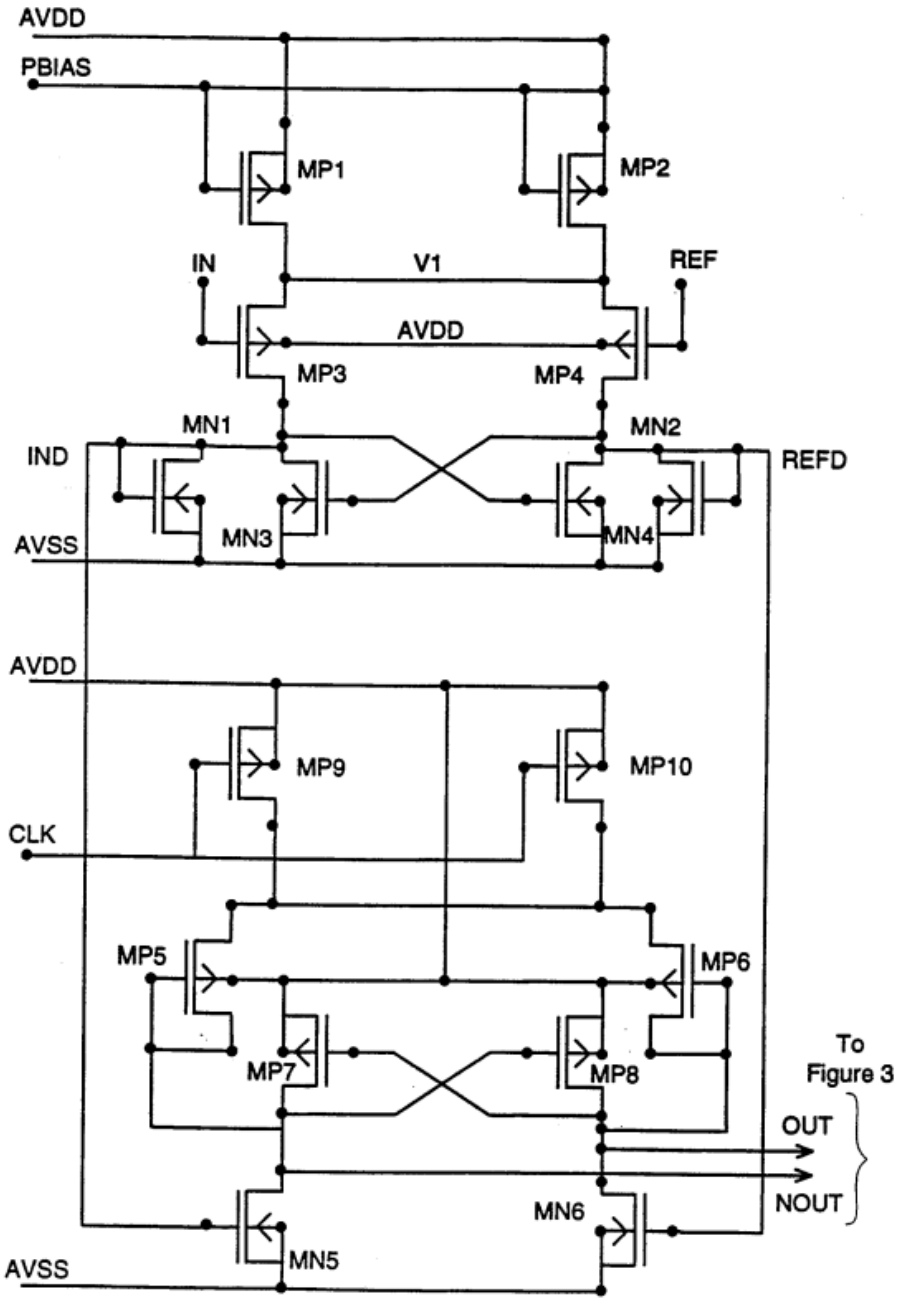


Figure 2 shows a partial "schematic diagram of a CMOS latching comparator circuit." Ex. 1005, 3:5–6, Fig. 2.

In Figure 2, bias transistors MP1 and MP2 couple to voltage AVDD and "provide a suitable bias current" for the latching comparator circuit's

input stage. Ex. 1005, 4:8–12. "A first differential pair of transistors, MP3 and MP4, are coupled to" bias transistors MP1 and MP2 and "connected together at node V1." *Id.* at 4:15–17. "A first cross-coupled pair of transistors, MN3 and MN4, are disposed between the source terminals of the first differential pair" and voltage AVSS. *Id.* at 4:31–34. A first pair of diode-connected transistors MN1 and MN2 are coupled in parallel to transistors MN3 and MN4, respectively. *Id.* at 4:42–44, 4:56–57.

The meeting point for transistor MP3's source, transistor MN3's drain, and transistor MN4's gate defines the input stage's IND node. Ex. 1005, 4:34–38, Fig. 2. The meeting point for transistor MP4's source, transistor MN4's drain, and transistor MN3's gate defines the input stage's REFD node. *Id.* The IND and REFD nodes supply the input stage's output signals to the latching stage. *Id.* at 5:32–34.

The latching stage includes a "second differential pair of transistors" MN5 and MN6 that "are common source coupled to" voltage AVSS. Ex. 1005, 5:34–37. Transistor MN5's gate receives an input signal from the input stage's IND node. *Id.* at 5:37–38, 6:6–9, Fig. 2. Transistor MN6's gate receives an input signal from the input stage's REFD node. *Id.*

The latching stage also includes a "second cross-coupled pair of transistors MP7 and MP8," with each transistor "coupled between a respective one of the second differential pair" of transistors MN5 and MN6 and voltage AVDD. Ex. 1005, 5:42–45. Transistor MP7's gate connects to the latching stage's OUT node. *Id.* at 5:45–46, Fig. 2. Transistor MP8's gate connects to the latching stage's NOUT node. *Id.* at 5:46–47, Fig. 2.

The meeting point for transistor MN6's drain, transistor MP7's gate, and transistor MP8's drain defines the latching stage's OUT node. Ex. 1005,

5:38–45, Fig. 2. The meeting point for transistor MN5's drain, transistor MP7's drain, and transistor MP8's gate defines the latching stage's NOUT node. *Id.* The OUT and NOUT nodes supply the latching stage's output signals to inverters shown in Figure 3. *Id.* at 5:60–65, Figs. 2–3.

The latching stage additionally includes a "second pair of diode-connected transistors" MP5 and MP6, with each transistor "coupled between a respective one of the second cross-coupled pair [MP7, MP8] and a switch node" in the latching stage. Ex. 1005, 5:48–50, Fig. 2. Transistor MP5 is coupled between the switch node and the meeting point for transistor MN5's drain, transistor MP7's drain, and transistor MP8's gate, i.e., the latching stage's NOUT node. *Id.* at 5:46–47, 5:51, Fig. 2. Transistor MP6 is coupled between the switch node and the meeting point for transistor MN6's drain, transistor MP7's gate, and transistor MP8's drain, i.e., the latching stage's OUT node. *Id.* at 5:45–46, 5:52, Fig. 2.

The switch node couples to voltage AVDD "through a pair of digital switch transistors MP9 and MP10, connected in parallel." Ex. 1005, 5:52–55; *see id.* at 2:21–25. "The gates of MP9, MP10 are coupled to receive the latch clock signal," i.e., the CLK signal. *Id.* at 5:55–56, Fig. 2; *see id.* at code (57), 2:26–27.

When turned on by a low CLK signal, transistors MP9 and MP10 act together to connect the switch node to voltage AVDD. Ex. 1005, 5:48–56, 6:6–18, Fig. 2; *see id.* at 2:21–31. Connecting the switch node to voltage AVDD couples diode-connected transistors MP5 and MP6 in parallel with transistors MP7 and MP8, respectively, thus regulating the gain of transistors MP7 and MP8. *Id.* at 2:27–31, 6:9–18, Fig. 2; *see id.* at code (57), 4:50–55, 4:58–60.

When turned off by a high CLK signal, transistors MP9 and MP10 act together to disconnect the switch node from voltage AVDD. Ex. 1005, 5:48–56, 6:6–25, 6:65–7:2, Fig. 2; *see id.* at 2:21–38. Disconnecting the switch node from voltage AVDD effectively removes diode-connected transistors MP5 and MP6 from the circuit, thus permitting transistors MP7 and MP8 "to form a very high gain positive feedback amplifier for latching." *Id.* at 6:19–25; *see id.* at 2:31–38. The "amplifier operates at maximum gain during latching." *Id.* at code (57).

Lim's Figure 3 is reproduced below:

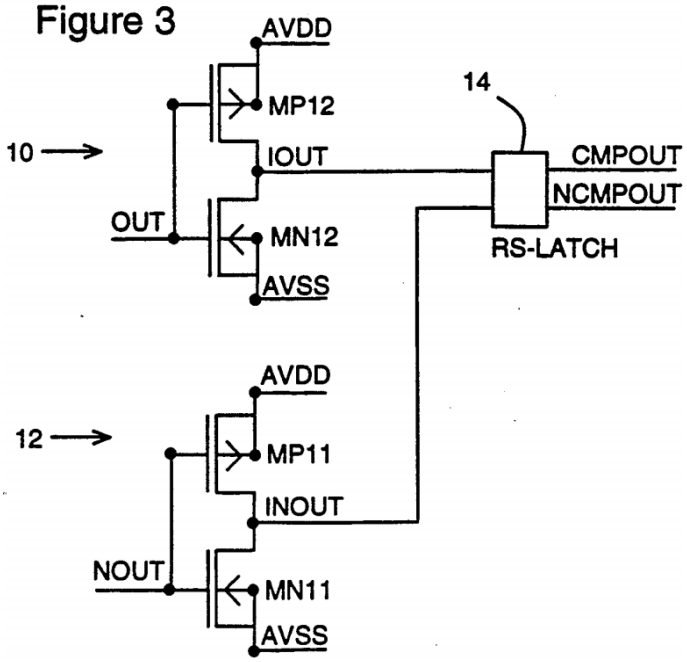


Figure 3 shows a partial "schematic diagram of a CMOS latching comparator circuit." Ex. 1005, 3:5–6, Fig. 3.

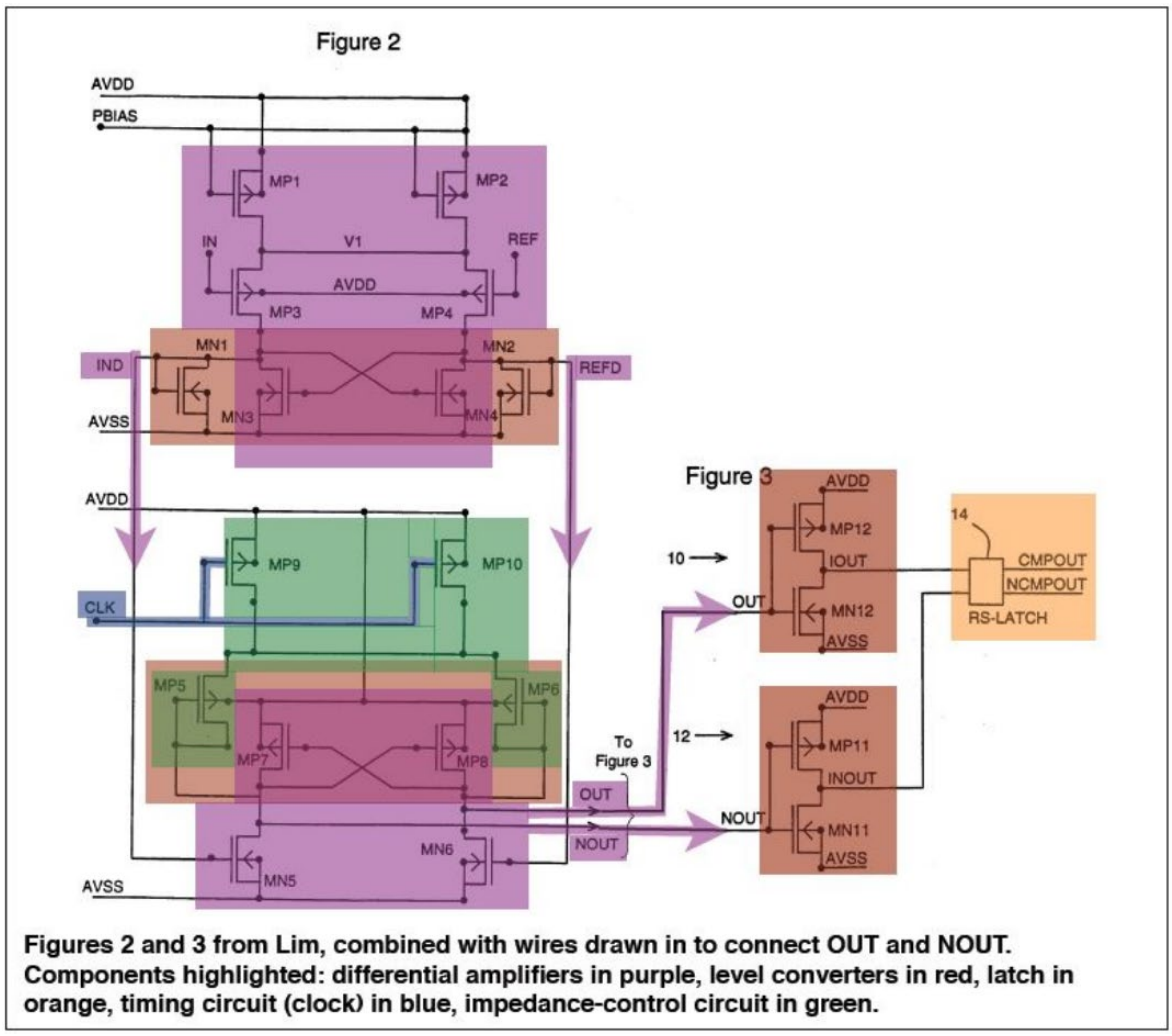
In Figure 3, inverter circuit 10 receives an input signal from the latching stage's OUT node and "provides an inverted output signal IOUT at appropriate CMOS logic voltage levels." Ex. 1005, 5:60–63. Similarly, inverter circuit 12 receives an input signal from the latching stage's NOUT node and "provides an inverted output signal INOUT." *Id.* at 5:63–65. "The

output signals IOUT and INOUT are connected to" RS-latch circuit 14. *Id.* at 5:65–67.

RS-latch circuit 14 "provides the final comparator output signals CMPOUT and its complement NCMPOUT." Ex. 1005, 6:1–3. Hence, "when IN is higher than REF, CMPOUT is a logic low, and when IN is less than REF, CMPOUT is a logic high." *Id.* at 6:3–5.

3. WHETHER LIM ANTICIPATES CLAIM 1

Petitioner argues that the latching comparator circuit illustrated in Lim's Figures 2 and 3 anticipates claim 1. *See* Pet. 45–57. To support its argument, Petitioner presents the highlighted version of Lim's Figures 2 and 3 (as combined by Petitioner) reproduced below:



Figures 2 and 3 from Lim, combined with wires drawn in to connect OUT and NOUT. Components highlighted: differential amplifiers in purple, level converters in red, latch in orange, timing circuit (clock) in blue, impedance-control circuit in green.

According to Petitioner, this highlighted version of Figures 2 and 3 shows:

(1) a timing circuit (clock) "highlighted in blue,"

(2) differential amplifiers "highlighted in purple,"

(3) an impedance-control circuit "highlighted in green,"

(4) level converters "highlighted in red," and

(5) a clock-free latch "highlighted in orange."

Pet. 36–37 (citing Ex. 1003 ¶ 115); *see* Ex. 1003 ¶¶ 114–115.

(a) Preamble

Claim 1's preamble recites "[a]n apparatus for use as an output stage of a memory device." Ex. 1001, 6:62–63. Petitioner asserts that Lim

satisfies claim 1's preamble because (1) Lim discloses a latching comparator circuit with an input stage and a latching stage and (2) the latching stage constitutes an output stage of a memory device. Pet. 45 (citing Ex. 1003 ¶¶ 134–136; Ex. 1005, code (57), 1:5–10); *see* Ex. 1003 ¶¶ 134–136. Petitioner also asserts that Lim's latching comparator circuit stores a logic state at its output "indefinitely" until an enable or unlatch command occurs. Pet. 45 (citing Ex. 1005, 1:25–31).

To support Petitioner's assertions, Dr. Jacob stated that "Lim describes the inventive circuit" as an analog-to-digital conversion (ADC) circuit. Ex. 1003 ¶ 134; *see id.* ¶ 111. He also stated that an ordinarily skilled artisan would have known that an ADC circuit "is a necessary component of modern resistive memory devices" for "reading the cell's analog output signal, converting it to a digital number, and producing as the memory's output the corresponding digital value representing the cell's analog output." *Id.* ¶ 134; *see id.* ¶¶ 26, 38–43. Further, Dr. Jacob described Lim's latching comparator circuit as suitable for use in "modern resistive memory devices" having memory cells that "store analog values" requiring conversion "to digital by an ADC circuit" before use by a digital circuit. *Id.* ¶ 136.

Patent Owner does not make any arguments specific to claim 1's preamble. *See, e.g.*, Resp. 30–36.

Generally, a preamble does not limit a claim. *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002). Here, we need not decide whether claim 1's preamble limits the claim because we agree with Petitioner that Lim satisfies claim 1's preamble.

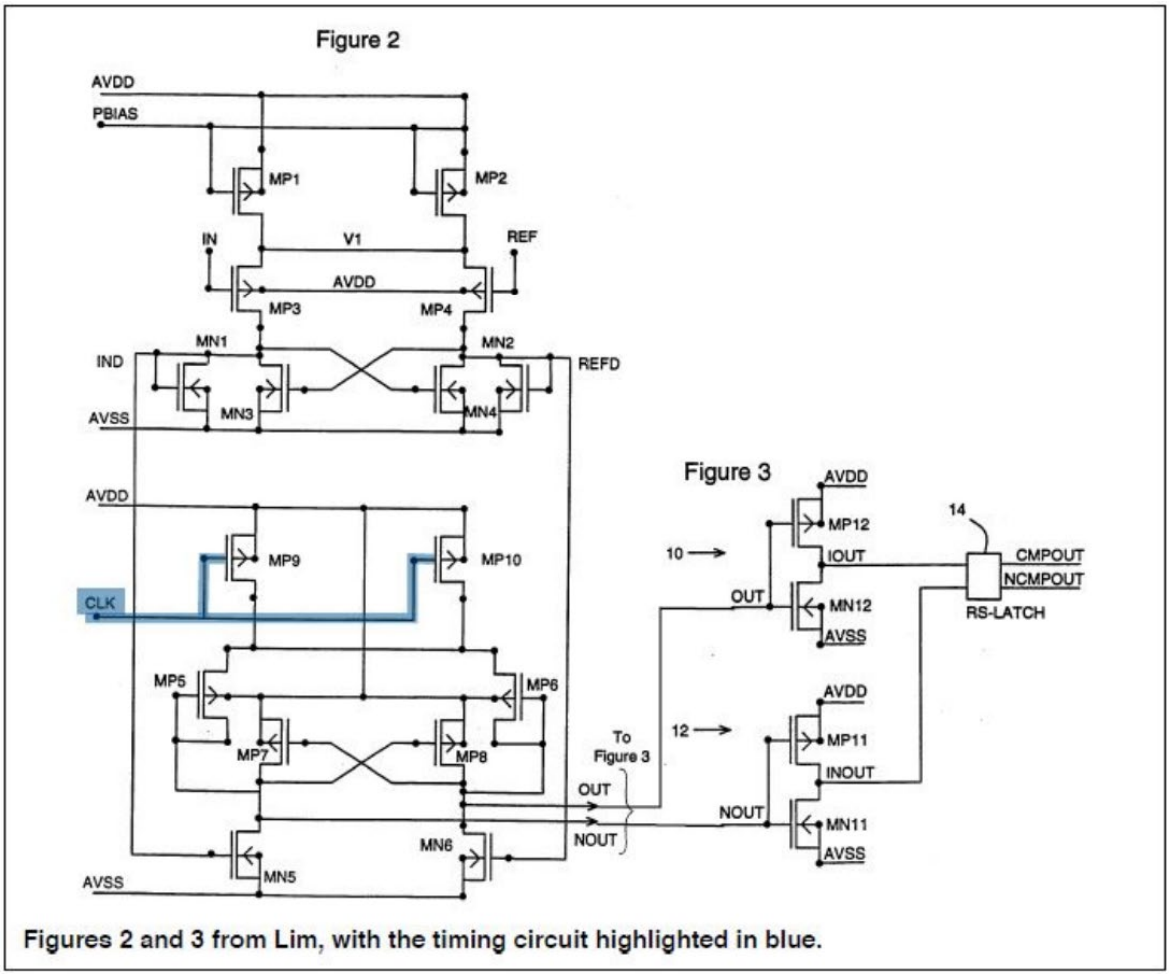
Specifically, Lim's latching comparator circuit may operate as an analog-to-digital conversion (ADC) circuit. Ex. 1005, 1:5–10, 1:48–51, 2:47–51, 7:38–43; *see* Ex. 1003 ¶¶ 111, 116, 134–136. As Dr. Jacob stated, an ordinarily skilled artisan would have known that an ADC circuit "is a necessary component of modern resistive memory devices" for "reading the cell's analog output signal, converting it to a digital number, and producing as the memory's output the corresponding digital value representing the cell's analog output." Ex. 1003 ¶ 134. And, as Petitioner asserts, Lim's latching comparator circuit stores a logic state at its output "indefinitely" until an enable or unlatch command occurs. *See* Ex. 1005, 1:25–32, 5:65–6:5, 6:17–25, 6:65–67; Ex. 2001 ¶ 62; Pet. 45.

Based on Lim's disclosure and Dr. Jacob's testimony, Lim's latching comparator circuit constitutes "[a]n apparatus for use as an output stage of a memory device." Hence, Lim satisfies claim 1's preamble.

(b) The "Timing Circuit" Limitation

(i) Petitioner's Arguments in the Petition

Claim 1 recites "a timing circuit." Ex. 1001, 6:65. For the claimed "timing circuit," Petitioner identifies in Lim's Figure 2 the CLK signal and the wires connected to the gates of transistors MP9 and MP10. Pet. 46–47; *see* Ex. 1003 ¶¶ 137–138. To support its position, Petitioner presents another highlighted version of Lim's Figures 2 and 3 (as combined by Petitioner) reproduced below:



Figures 2 and 3 from Lim, with the timing circuit highlighted in blue.

According to Petitioner, this highlighted version of Figures 2 and 3 shows "a timing circuit, CLK, highlighted in blue." Pet. 46–47; *see* Ex. 1003 ¶ 137.

Petitioner asserts that "timing circuit, CLK, has input nodes" at the gates of transistors MP9 and MP10. Pet. 47; *see* Ex. 1003 ¶ 138. Petitioner also asserts that "timing circuit, CLK, drives the 'digital switch' in Lim" to control a differential amplifier's operating mode. Pet. 47–48; *see* Ex. 1003 ¶ 138.

(ii) Patent Owner's Arguments in the Response

Patent Owner disputes that Lim's latching comparator circuit includes "a timing circuit" according to claim 1. *See* Resp. 30–36. In particular,

Patent Owner contends that the term "timing circuit" means "an electrical circuit that generates and outputs a plurality of different versions of a clock signal." Resp. 30, 33 (emphasis omitted); Sur-reply 2, 12 n.2. Patent Owner also contends that a "timing circuit" does not encompass "a single clock signal provided directly to an output stage as the only clock." Resp. 30; *see id.* at 32; Sur-reply 2. Patent Owner then asserts that the CLK signal is not a "timing circuit" because the CLK signal "does not generate and output a plurality of different versions of a clock signal," but instead connects directly to the gates of transistors MP9 and MP10. Resp. 31–32; *see* Ex. 2001 ¶¶ 87–88.

(iii) Petitioner's Arguments in the Reply

Petitioner disagrees that the term "timing circuit" requires construction. *See* Reply 2–14. Petitioner argues that the plain and ordinary meaning of "timing circuit" controls because the '274 patent does not redefine that term or narrow it by disavowal. *Id.* at 2–3, 13–14. Petitioner asserts that the plain and ordinary meaning of "timing circuit" is "a circuit for timing." *Id.* at 2–3, 12; *see* Ex. 1020 ¶ 9. Petitioner contends that Dr. Khatri "agreed during cross-examination that 'a timing circuit is a very broad category of circuit' and that '[i]t's **a circuit that provides timing in some manner**.'" Reply 2 (alteration and emphasis by Petitioner) (quoting Ex. 1019, 13:22–14:2).

Additionally, Petitioner criticizes Patent Owner's proposed construction of "timing circuit" for three reasons. *See* Reply 3–14. First, Petitioner asserts that Patent Owner's proposed construction improperly attempts to limit "timing circuit" to "the embodiment of timing circuit 104" in the '274 patent's Figure 2. *Id.* at 3–4, 11. Petitioner contends that timing

circuit 104 "outputs two versions of a clock signal (clock 78)," i.e., a first control/clock signal output by inverter 146 and a second control/clock signal output by NAND gate 149. *Id.* at 4 (citing Resp. 27). Petitioner also contends that the '274 patent "explicitly calls this just 'one embodiment' of the present invention." *Id.* at 4–5 (citing Ex. 1001, 5:18–29).

Second, Petitioner asserts that Patent Owner's proposed construction "violates principles of claim differentiation." Reply 7–12. In particular, Petitioner argues that Patent Owner's proposed construction "requires that the 'plurality of different versions of a clock signal' differ by some amount of delay." *Id.* at 7–9, 12. Petitioner notes that claim 2 depends from claim 1 and specifies that "the timing circuit is a clock delay circuit." *Id.* at 10. Petitioner also notes that in IPR2018-00989 the Board construed "clock delay circuit" in claim 2 to mean "a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version." *Id.* at 11–12 (citing *Micron Tech., Inc. v. N. Star Innovations, Inc.*, IPR2018-00989, Paper 35 at 42 (PTAB Oct. 22, 2019) (Final Written Decision)). Petitioner then contends that "Patent Owner's construction of 'timing circuit' in Claim 1 is coextensive with the Board's construction of 'clock delay circuit' in Claim 2 and therefore cannot be correct." *Id.* at 12.

Third, Petitioner asserts that Patent Owner's proposed construction renders claim 1 "impermissibly vague" because "there is no objective standard provided to determine how much delay or difference is required between two versions of a clock signal" to produce "different" versions. Reply 12–13. Petitioner contends that Dr. Khatri "testified during cross-examination that he could not provide an objective measure of how much

delay was required to make two versions of clock signals 'different' under Patent Owner's proposed construction" except to say that it would depend on the "context" and the "circuit that is driven by the timing circuit." *Id.* (citing Ex. 1019, 34:5–8, 34:20–35:3, 36:14–37:9).

Toward the same end, Petitioner quotes Dr. Khatri's statement that "[i]n this context, you know, I could look at the circuit and say that from **my intuition it would be at least a handful of gate delays** that would be required." Reply 13 (emphasis by Petitioner) (quoting Ex. 1019, 37:5–9). Petitioner then contends that Patent Owner's proposed construction contains a subjective "term of degree" whose interpretation "depends on the 'unpredictable vagaries of any one person's opinion.'" *Id.* (quoting *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014)).

(iv) Patent Owner's Arguments in the Sur-reply

Patent Owner responds by explaining that different versions of a clock signal may result from differences other than delay, for example, differences in amplitude, frequency, or duty cycle. Sur-reply 4–5 (citing Ex. 1019, 39:4–40:14; Ex. 2003, 17:12–18:23); *see id.* at 6–7. Patent Owner then contends that (1) claim 1's "timing circuit" encompasses "a multitude of differences between multiple versions of a clock signal" and (2) claim 2's "clock delay circuit" requires a difference based on delay. *Id.* at 8. Patent Owner also contends that claim 2's "clock delay circuit" narrows claim 1's "timing circuit" by adding a limitation, and therefore claims 1 and 2 differ in scope. *Id.* at 8.

Regarding Petitioner's assertion that Patent Owner's proposed construction renders claim 1 "impermissibly vague," Patent Owner argues that Petitioner focuses on different versions of a clock signal that differ due

to delay alone, without considering that versions of a clock signal may diverge in amplitude, frequency, or duty cycle. Sur-reply 9.

Further, in "the specific context of differences" due to delay, Patent Owner contends that "Petitioner mischaracterizes Dr. Khatri's testimony" because he mentioned his "intuition" about a "handful of gates" when (1) considering the specific output stage in the '274 patent's Figure 2 and (2) describing the delay needed to cause "a delayed disablement of the differential amplifier" in that output stage. Sur-reply 9–10 (citing Ex. 1019, 33:16–35:3, 35:4–19, 37:5–38:20). Patent Owner also contends that Dr. Khatri "was not referring to the amount of delay that would be required generally to make two versions of a clock signal different." *Id.* at 10. Moreover, Patent Owner asserts that Dr. Khatri identified "an entirely objective measure of the amount of delay that would be required to make two different versions of a clock signal," i.e., a one-gate delay. *Id.* at 10–11 (citing Ex. 1019, 58:6–14, 59:2–5).

(v) Construction of "Timing Circuit"

For the reasons explained below, we agree with Patent Owner that the term "timing circuit" means "an electrical circuit that generates and outputs a plurality of different versions of a clock signal."

Patent applicants typically present "a set of claims, each differing in scope, one from the other, and usually running from the broadest permissible definition of the invention to a very specific definition of the invention." *Westwood Chem., Inc. v. United States*, 525 F.2d 1367, 1371–72 (Ct. Cl. 1975). Hence, "[d]ifferences among claims can also be a useful guide in understanding the meaning of particular claim terms." *Phillips*, 415 F.3d at 1314.

Here, claim 1 differs from the other independent claims because claim 1 requires a circuit element "responsive" to a "timing circuit," while the other independent claims require circuit elements "responsive" to a "clock signal." In particular, claim 1 recites "a timing circuit" and "a differential amplifier responsive to the timing circuit." Ex. 1001, 6:65–66. In contrast to claim 1, independent claim 21 recites "a differential amplifier responsive to a clock signal." *Id.* at 8:42. Similar to claim 21, independent claim 14 recites "amplifying a differential input to produce a differential output in response to a clock signal." *Id.* at 8:1–2. And similar to claim 14, independent claim 20 recites "amplifying and level converting a differential input to produce a level converted signal in response to a clock signal." *Id.* at 8:29–31.

By using different language, the independent claims indicate that claim 1's "timing circuit" does something more than the "clock signal" required by claims 14, 20, and 21. The dependent claims indicate that claim 1's "timing circuit" provides different versions of a clock signal that may differ due to delay or some other characteristic.

In particular, claim 2 depends directly from and narrows claim 1. Ex. 1001, 7:4–5. Claim 2 specifies that "the timing circuit is a clock delay circuit." *Id.* As Petitioner notes, in IPR2018-00989 the Board construed "clock delay circuit" in claim 2 to mean "a circuit that receives a clock signal as an input and provides different versions of the input clock signal, with one version delayed compared to the other version." *Micron Tech., Inc. v. N. Star Innovations, Inc.*, IPR2018-00989, Paper 35 at 33–34, 42 (PTAB Oct. 22, 2019) (Final Written Decision); *see* Reply 11–12. Under that construction, claim 2's "clock delay circuit" provides different versions of a

clock signal that differ due to delay. And under claim-differentiation principles, claim 1's "timing circuit" should differ from claim 2's "clock delay circuit" by not requiring delay.

Setting aside the construction from IPR2018-00989, claim 2 expressly requires delay, i.e., a "clock delay circuit." Again, claim 1's "timing circuit" should differ from claim 2's "clock delay circuit" by not requiring delay. Dr. Khatri and Dr. Jacob agreed that different versions of a clock signal may result from differences in amplitude, frequency, or duty cycle as well as differences in delay. Ex. 1019, 33:16–34:4, 39:4–40:9, 53:5–15; Ex. 2003, 17:12–21, 18:13–23. Construing "timing circuit" to mean "an electrical circuit that generates and outputs a plurality of different versions of a clock signal" comports with claim-differentiation principles for claims 1 and 2.

That construction also comports with claim-differentiation principles for claims 1 and 13. Claim 13 depends directly from and narrows claim 1. Ex. 1001, 7:35–55. Claim 13 recites particular circuit components and specifies that "the timing circuit includes a first inverter to produce a first clock signal, a second inverter, a third inverter, and a NAND gate to produce a second clock signal." *Id.* at 7:36–38.

The particular circuit components in claim 13's "timing circuit" correspond to the circuit components in Figure 2's timing circuit 104, i.e., "a first inverter [146] to produce a first clock signal, a second inverter [147], a third inverter [148], and a NAND gate [149] to produce a second clock signal." Ex. 1001, 3:4–5, 3:63–4:1, 5:18–23, 5:26–37, 7:36–38, Fig. 2; *see* Ex. 2001 ¶¶ 51–59, 77–78. The particular circuit components in claim 13's "timing circuit" provide different versions of a clock signal that differ due to delay, i.e., versions having "approximately simultaneous rising [or enabling]

edges" and "a delay between their [falling or] disabling edges," i.e., "purposely skewed" disabling edges. Ex. 1001, 5:26–37; *see id.* at code (57); Ex. 2001 ¶¶ 51–59.

Thus, the particular circuit components in claim 13's "timing circuit" produce a particular response, i.e., signals with simultaneous enabling edges and "purposely skewed" disabling edges. But claim 1's "timing circuit" does not require those particular circuit components and encompasses other components producing other responses.

Because the particular circuit components in claim 13's "timing circuit" correspond to the circuit components in Figure 2's timing circuit 104 and because claim 1's "timing circuit" encompasses other components, we disagree with Petitioner that Patent Owner improperly attempts to limit claim 1's "timing circuit" to "the embodiment of timing circuit 104" in Figure 2. *See* Reply 3–4, 11.

The '274 patent's specification supports the conclusion that "timing circuit" means "an electrical circuit that generates and outputs a plurality of different versions of a clock signal." *See* Ex. 1001, code (57), 2:50–3:13, 4:48–51, 5:18–44. The Federal Circuit has described a patent's specification as "highly relevant" to claim construction and "the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

Here, the '274 patent's specification contemplates other embodiments of an output stage as well as other embodiments of the circuit elements comprising an output stage, e.g., Figure 2's timing circuit 104. Ex. 1001, 2:50–3:13, 4:48–51, 5:18–20; *see id.* at code (57). For instance, the specification states that Figure 2 "illustrates one embodiment of" an output

stage as shown in Figure 1. *Id.* at 2:50–52, 4:48–49; *see id.* at 4:49–51. The specification also states that "alternate embodiments of the present invention may use different circuit elements than those illustrated in" Figure 2. *Id.* at 3:11–13. As an example, the specification identifies Figure 2's timing circuit 104 as "one embodiment" of a timing circuit. *Id.* at 3:4–5. The specification's discussion of other embodiments of an output stage as well as other embodiments of the circuit elements comprising an output stage parallels how claims 1, 2, and 13 differ in scope.

Moreover, the specification discloses multiple embodiments of a timing circuit. For instance, when discussing Figure 2, the specification states that "[i]n one embodiment, timing circuit 104 is used to provide two versions of clock signal 78," i.e., versions having "approximately simultaneous rising [or enabling] edges" and "a delay between their [falling or] disabling edges," i.e., "purposely skewed" disabling edges. Ex. 1001, 5:26–37; *see id.* at code (57); Ex. 2001 ¶¶ 51–59. In that embodiment, "clock 78 and timing circuit 104 provide two clock signals to differential amplifier 100" to selectively enable and disable differential amplifier 100, thus reducing power and increasing speed. Ex. 1001, 5:20–25; *see id.* at code (57).

But the specification makes clear that an output stage "requires one clock signal to function" and that "[t]he present invention merely requires a single clock signal." Ex. 1001, code (57), 5:25–26. Referencing Figure 2's timing circuit 104, the specification explains that "some embodiments of the present invention may use clock 78 directly as the only clock, without using timing circuit 104 to create two slightly different versions." *Id.* at 5:41–44.

Thus, the specification distinguishes a "timing circuit," e.g., timing circuit 104, from a "single clock signal," e.g., clock signal 78. Ex. 1001, 2:44–46, 3:4–5, 3:63–4:1, 5:18–44; *see id.* at code (57). In addition, the specification consistently describes a "timing circuit" as providing different versions of a clock signal. *Id.* at 5:18–44. By distinguishing a "timing circuit" from a "single clock signal" and consistently describing a "timing circuit" as providing different versions of a clock signal, the specification indicates that a "timing circuit" provides different versions of a clock signal that may differ in various ways.

Petitioner asserts that "the **only** type of difference disclosed in the '274 Patent between versions of a clock signal is **delay**." Reply 9 (emphasis by Petitioner) (citing Ex. 1001, 5:18–44); *see* Tr. 10:22–11:2. But a patent need not "explain every detail" since it speaks to "those skilled in the art." *In re Howarth*, 654 F.2d 103, 105 (CCPA 1981). For similar reasons, a patent need not "spell out every possible iteration of every claim." *Trs. of Bos. Univ. v. Everlight Elecs. Co.*, 896 F.3d 1357, 1364 (Fed. Cir. 2018).

For instance, those skilled in the art would appreciate that certain circuit elements may differ in construction and, therefore, may require enabling or disabling signals that differ in amplitude, e.g., differ in voltage. As Dr. Jacob explained, digital systems often have different sections "driven by different power-supply voltage levels," and "[w]hen signals cross between these different power-supply domains one must translate from one domain to the other by converting/shifting from the level supplied by one domain to the level supplied by the other." Ex. 1003 ¶ 87.

A claim construction should comport with the purposes of the invention. *See OSRAM GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358

(Fed. Cir. 2007). Here, construing "timing circuit" as "a circuit for timing" according to the asserted plain and ordinary meaning does not comport with the purposes of the invention. For example, "a circuit for timing" would not avoid the timing-relationship problem with "separate clock signal[s] as used by the prior art." *See* Ex. 1001, 1:33–44, 5:34–37 (discussing the timing-relationship problem). But "an electrical circuit that generates and outputs a plurality of different versions of a clock signal" would avoid the timing-relationship problem with separate clock signals.

The '274 patent's prosecution history sheds no light on the meaning of "timing circuit." In the first Office action, the Examiner issued a Notice of Allowability and made minor amendments to application claims 7, 10, and 19 that have no bearing on the patentability issues here. Ex. 1002, 30–34; *see id.* at 17–20. In the Notice of Allowability, the Examiner included the following statement of reasons for allowance:

> The prior art of record fails to show an apparatus and a method for use as an output stage of a memory device, utilizing a timing circuit, a differential amplifier responsive to the timing circuit, an impedance control circuit, a level converter responsive to the differential amplifier and the impedance control circuit, and a clock-free latch responsive to a level converter, as represented in claims 1, 14, 20, and 21.

Id. at 31. Application claims 1–24 then issued as patent claims 1–24 without further commentary from the Examiner or the Applicants. *See, e.g.*, *id.* at 135.

Nevertheless, an analysis of the '274 patent in its entirety leads us to conclude that "timing circuit" means "an electrical circuit that generates and outputs a plurality of different versions of a clock signal." That construction comports with the purposes of the invention because the "timing circuit"

outputs "different versions of a clock signal" instead of "separate clock signal[s] as used by the prior art." *See* Ex. 1001, 1:33–44, 5:34–37.

We note that claim 4 depends from claim 1 and specifies that "the timing circuit receives a clock signal." Ex. 1001, 7:8–9. The construction of "timing circuit" we adopt does not render claim 4 superfluous, however, because claim 1's "timing circuit" may generate different versions of a clock signal in at least two ways. That "timing circuit" may generate different versions internally without receiving a clock signal. Alternatively, that "timing circuit" may generate different versions responsive to receiving a clock signal.

As for Dr. Khatri's statements that "a timing circuit is a very broad category of circuit" and that "[i]t's a circuit that provides timing in some manner," he explained that the statements concerned a general context, not the context of the '274 patent. *See* Ex. 1019, 13:5–14:21. When asked, "Before this case had you heard of the term timing circuit before," he answered, "In general for sure, yes." *Id.* at 13:5–7. And when asked, "[I]n what context in general did you hear of that term," he answered, "I mean, timing circuits are a very broad category of circuits so, you know, they're in every context in chip design. So you hear about them in many, many different sort of contexts in a chip." *Id.* at 13:8–14.

Dr. Khatri's statements about timing circuits in a general context provide little aid in determining the meaning of "timing circuit" in the context of the '274 patent. "The only meaning that matters in claim construction is the meaning in the context of the patent." *Trs. of Columbia Univ. v. Symantec Corp.*, 811 F.3d 1359, 1363 (Fed. Cir. 2016) ("*Columbia Univ.*").

We disagree with Petitioner that the plain and ordinary meaning of "timing circuit" controls because the '274 patent does not redefine that term or narrow it by disavowal. *See* Reply 2–3, 13–14. Federal Circuit case law "does not require explicit redefinition or disavowal" because a "specification may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent." *Columbia Univ.*, 811 F.3d at 1363–64 (citing *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012); *Phillips*, 415 F.3d at 1320–21).

Further, we disagree with Petitioner that the construction of "timing circuit" we adopt renders claim 1 "impermissibly vague." *See* Reply 12–13. Based on the '274 patent's repeated references to different versions of a clock signal, an ordinarily skilled artisan would recognize the amount of dissimilarity needed for "different" versions. Ex. 1001, 5:18–44; *see id.* at code (57). Also, as Patent Owner argues, Petitioner focuses on different versions of a clock signal that differ due to delay alone, without considering that versions of a clock signal may diverge in amplitude, frequency, or duty cycle. *See* Sur-reply 9; *see also* Ex. 1019, 33:16–34:4, 39:4–40:9, 53:5–15; Ex. 2003, 17:12–21. Moreover, for different versions of a clock signal that differ due to delay, Dr. Khatri identified an objective measure of the amount of delay needed for "different" versions, i.e., a one-gate delay. Ex. 1019, 58:6–14, 59:2–5.

In addition, we agree with Patent Owner that Dr. Khatri mentioned his "intuition" about a "handful of gates" when (1) considering the specific output stage in the '274 patent's Figure 2 and (2) describing the delay needed to cause "a delayed disablement of the differential amplifier" in that output stage. Ex. 1019, 35:4–38:20. For instance, he said, "[I]n the context

of the '274 patent the amount of phase shift that would be needed . . . causes a delayed disablement of the differential amplifier." *Id.* at 35:9–14. He also said, "[I]n the case of the '274 patent and the circuit that we see on figure 2, my intuition would have said that this would be, you know, a handful of gate delays." *Id.* at 38:17–20. Similarly, he noted that "a handful of gate delays . . . would be required that the disablement edge is delayed by." *Id.* at 37:5–9.

For the reasons discussed above, we construe "timing circuit" to mean "an electrical circuit that generates and outputs a plurality of different versions of a clock signal."

(vi) Whether Lim Includes the Claimed "Timing Circuit"

Next, we consider whether Lim's latching comparator circuit includes the claimed "timing circuit." For the reasons explained below, it does not.

Referencing Lim's Figure 2, Petitioner asserts that "the timing circuit in Lim, CLK, outputs two versions of the inputted clock signal," i.e., a first version received at transistor MP9's gate and a second version received at transistor MP10's gate. Reply 15. Petitioner argues that "Lim inherently discloses" that "the two versions of the clock signal differ in terms of one being delayed compared to the other." *Id.* at 16. Petitioner similarly argues that "Lim discloses two clock signals that will necessarily have different phase delays" at the gates of transistors MP9 and MP10. *Id.* at 17. To support its arguments, Petitioner relies on Dr. Jacob's testimony. *Id.* at 16–18 (citing Ex. 1020 ¶¶ 36–42).

Dr. Jacob stated that the CLK signal in Lim's Figure 2 "is provided to two different PMOS transistors MP9 and MP10" and that the signals received by those transistors at their respective gates are "different versions

of a clock signal." Ex. 1020 ¶ 40. He explained that "[t]hose signals are not the same signal" because "they travel down different wires, and therefore each experiences a different phase delay." *Id.* ¶ 41 (footnote omitted).

Patent Owner disputes that transistors MP9 and MP10 receive signals that inherently differ because they travel down different wires. *See* Sur-reply 14–17; Ex. 2001 ¶¶ 71, 94–97. Patent Owner contends that "nothing in Lim discloses that there is any delay in the signals" received by transistors MP9 and MP10 at their respective gates. Sur-reply 15. Patent Owner asserts that "Lim does not want delay in those signals" because transistors MP9 and MP10 "are intended to function as one switch" since "they are connected in parallel" and "laid out symmetrically." *Id.* (citing Ex. 1019, 60:5–16, 61:4–12). Patent Owner also asserts that Lim's disclosure that a "single transistor may be used" as a digital switch instead of transistors MP9 and MP10 further evidences Lim's intent that they function as one switch. *Id.* (citing Ex. 1005, 5:56–57).

In addition, Patent Owner contends that Dr. Jacob conceded that Lim's Figure 2 is "not meant to show the implementation, as fabricated." Sur-reply 14 (citing Ex. 2003, 21:8–19). Patent Owner also contends that Dr. Jacob said that he was "not sure" if anything in Lim's disclosure indicated that the wires connected to the gates of transistors MP9 and MP10 have different lengths. *Id.* (citing Ex. 2003, 27:12–16).

We agree with Patent Owner that transistors MP9 and MP10 do not receive signals that inherently differ because they travel down different wires. *See* Ex. 1003 ¶¶ 113, 138, 144; Ex. 1005, code (57), 2:21–38, 5:48–59, 6:6–25, 6:65–7:2, 7:17–18, 7:28–30, Fig. 2; Ex. 1019, 51:9–15, 59:2–12, 60:5–16, 61:4–12; Ex. 2001 ¶¶ 71, 94–97; Ex. 2003, 21:8–19,

23:24–24:3, 27:12–28:11. Lim repeatedly describes transistors MP9 and MP10 collectively as a "digital switch." Ex. 1005, code (57), 2:21–27, 5:52–55, 6:12–25, 6:65–7:2, 7:28–30; *see* Ex. 1003 ¶ 113; Ex. 2001 ¶¶ 71, 94. As an example, the Abstract states that "[t]he latch clock signal is provided to a digital switch (MP9, MP10)." Ex. 1005, code (57); *see* Ex. 1003 ¶ 113. As another example, the Summary of the Invention states that "[a] digital switch, comprising a pair of switch transistors, is disposed between" a switch node and a voltage source. Ex. 1005, 2:21–25; *see* Ex. 1003 ¶¶ 138, 144.

Additionally, Lim describes how transistors MP9 and MP10 act together as a single switch. First, transistors MP9 and MP10 are "connected in parallel" in the latching comparator circuit. Ex. 1005, 5:54–55, Fig. 2; *see* Ex. 1003 ¶¶ 138, 144; Ex. 2001 ¶¶ 71, 96. Second, "[t]he gates of MP9, MP10 are coupled to receive the latch clock signal," i.e., the CLK signal. Ex. 1005, 5:55–56, Fig. 2; *see id.* at code (57), 2:26–27; Ex. 1003 ¶¶ 138, 144; Ex. 2001 ¶¶ 71, 96. Third, responsive to the CLK signal, transistors MP9 and MP10 turn on or off together to alternately connect and disconnect two nodes, i.e., the switch node and voltage AVDD. Ex. 1005, 5:48–56, 6:6–25, 6:65–7:2, Fig. 2; *see id.* at 2:21–38; Ex. 1003 ¶¶ 121–122, 143–144; Ex. 2001 ¶¶ 71, 94.

Lim confirms that transistors MP9 and MP10 act together as a single switch by disclosing that a "single transistor may be used" as the digital switch. Ex. 1005, 5:56–57; *see id.* at 7:17–18; Ex. 2001 ¶ 96. Although a "single transistor may be used," Lim explains that a digital switch comprising a "pair of transistors in parallel" offers advantages, such as

"smaller individual device size and layout symmetry." Ex. 1005, 5:57–59; *see* Ex. 1019, 61:4–12; *see also* Ex. 1003 ¶¶ 138, 144; Ex. 2001 ¶ 96.

Because transistors MP9 and MP10 act together as a single switch, a circuit designer would "take pains to make" the wires connected to their respective gates equal in length. Ex. 1019, 51:9–15, 59:2–12, 60:5–16, 61:4–12. As Dr. Khatri explained, "it is essential that MP9 and MP10 receive[] and are controlled by the same signal" in the latching comparator circuit. Ex. 2001 ¶ 95. Moreover, Lim contemplates "layout symmetry" for a digital switch comprising a "pair of transistors in parallel." Ex. 1005, 5:57–59. As Dr. Khatri also explained, "Lim says that those transistors would be implemented symmetrically," and "when it says that, that means that we take pains to make the transistors match in terms of wire lengths and such." Ex. 1019, 61:4–12. Dr. Jacob admitted that Lim does not discuss an intent to create delay due to the wire lengths. Ex. 2003, 23:24–24:3, 27:17–28:11.

Although Lim's Figure 2 illustrates wires with different lengths connected to the gates of transistors MP9 and MP10, "figures in a patent are not drawn to scale unless otherwise indicated." *See Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000). Nothing in Lim's disclosure indicates that the figures are drawn to scale. Consistent with that, Dr. Jacob conceded that Lim's Figure 2 is "not meant to show the implementation, as fabricated." Ex. 2003, 21:8–19.

After weighing the evidence, we determine that Petitioner has not shown that the wires connected to the gates of transistors MP9 and MP10 have equal lengths. Because Petitioner has not shown that the wires have equal lengths, Petitioner has not shown that the gate signals received by

transistors MP9 and MP10 have different phase delays. In addition, Petitioner identifies no evidence indicating that the gate signals received by transistors MP9 and MP10 have different amplitudes, frequencies, or duty cycles or that the gate signals differ in some other way. *See* Pet. 46–48; Reply 15–18; Ex. 1003 ¶¶ 137–138; Ex. 1020 ¶¶ 36–42. Hence, Petitioner has not shown that the CLK signal and the wires connected to the gates of transistors MP9 and MP10 generate and output a plurality of different versions of a clock signal. Thus, Petitioner fails to establish that the CLK signal and the wires connected to the gates of transistors MP9 and MP10 satisfy claim 1's requirement for "a timing circuit."

At best, Petitioner raises a possibility that the wires connected to the gates of transistors MP9 and MP10 have different lengths. But possibilities or even probabilities do not establish inherency. *See Bettcher Indus., Inc. v. Bunzl USA, Inc.*, 661 F.3d 629, 639 (Fed. Cir. 2011).

For the reasons discussed above, Lim's latching comparator circuit lacks "a timing circuit" according to claim 1.

(c) The "Differential Amplifier" Limitation

Claim 1 recites "a differential amplifier responsive to the timing circuit." Ex. 1001, 6:66. For the claimed "differential amplifier," Petitioner identifies in Lim's Figure 2 transistors MN5, MN6, MP7, and MP8. Pet. 48–49; *see* Ex. 1003 ¶¶ 139–142. Petitioner contends that these components form a "cross-coupled differential amplifier" that "is responsive to [the] CLK signal and digital switch transistors MP9 and MP10." Pet. 48; *see* Ex. 1003 ¶¶ 139–140.

To support Petitioner's contention, Dr. Jacob stated that the "cross-coupled differential amplifier" formed by transistors MN5, MN6, MP7, and

MP8 operates in different modes depending on the CLK signal. Ex. 1003 ¶ 140. In particular, he explained that the amplifier operates in (1) a "regulated-gain mode" when the CLK signal is low and (2) an "unregulated" mode when the CLK signal is high, "behaving like a differential sense amplifier" with a high gain. *Id.* ¶¶ 140, 143; *see id.* ¶¶ 120–125, 138. He further explained that transistors MP7 and MP8 "form a very high gain positive feedback amplifier for latching" when digital switch transistors MP9 and MP10 turn off due to a high CLK signal. *Id.* ¶ 140 (citing Ex. 1005, 6:23–24); *see id.* ¶¶ 116, 122–123, 125.

Because the "cross-coupled differential amplifier" formed by transistors MN5, MN6, MP7, and MP8 operates in different modes depending on the CLK signal, Petitioner asserts that the differential amplifier "is clearly responsive to the timing circuit, CLK." Pet. 49–50; *see* Ex. 1003 ¶¶ 140, 144.

Patent Owner does not make any arguments specific to claim 1's "differential amplifier" limitation. *See, e.g.*, Resp. 30–36.

We agree with Petitioner that transistors MN5, MN6, MP7, and MP8 act as "a differential amplifier" according to claim 1. *See* Ex. 1003 ¶¶ 139–142. In Lim's latching comparator circuit, the latching stage includes transistors MN5, MN6, MP7, and MP8. Ex. 1005, 5:34–47, 6:9–12, Fig. 2; *see* Ex. 1003 ¶¶ 119–120, 124; Ex. 2001 ¶¶ 61–62, 70. Transistors MN5 and MN6 receive input signals from the latching comparator circuit's input stage, i.e., from nodes IND and REFD, respectively. Ex. 1005, 5:31–38, 6:6–9, Fig. 2; *see* Ex. 1003 ¶¶ 119–120; Ex. 2001 ¶ 68.

The meeting point for transistor MN6's drain, transistor MP7's gate, and transistor MP8's drain defines the latching stage's OUT node. Ex. 1005, 5:38–45, Fig. 2; *see* Ex. 2001 ¶¶ 69–70. The meeting point for transistor MN5's drain, transistor MP7's drain, and transistor MP8's gate defines the latching stage's NOUT node. Ex. 1005, 5:38–45, Fig. 2; *see* Ex. 2001 ¶¶ 69–70. The OUT and NOUT nodes supply the latching stage's output signals to inverter circuits connected to a latch circuit. Ex. 1005, 5:60–67, Figs. 2–3; *see* Ex. 1003 ¶¶ 116, 126–128; Ex. 2001 ¶¶ 70, 72.

Further, when digital switch transistors MP9 and MP10 turn off due to a high CLK signal, transistors MP7 and MP8 "form a very high gain positive feedback amplifier for latching." Ex. 1005, 6:19–25; *see id.* at 2:31–38; *see* Ex. 1003 ¶¶ 116, 122–123, 125, 140. The "amplifier operates at maximum gain during latching." Ex. 1005, code (57).

For the reasons discussed above, Lim's latching comparator circuit includes "a differential amplifier" according to claim 1. But that differential amplifier is not "responsive to the timing circuit" as required by claim 1 because, as discussed above in Section III.C.3(b), Lim's latching comparator circuit lacks "a timing circuit" according to claim 1.

(d) The "Impedance Control Circuit" Limitation

Claim 1 recites "an impedance control circuit." Ex. 1001, 6:67. For the claimed "impedance control circuit," Petitioner identifies in Lim's Figure 2 transistors MP5, MP6, MP9, and MP10, i.e., diode-connected transistors MP5 and MP6 and digital switch transistors MP9 and MP10. Pet. 51–52; *see* Ex. 1003 ¶¶ 113, 121–122, 138, 143–144. Petitioner contends that these components control impedance responsive to the CLK signal. *See* Pet. 52–53.

First, Petitioner asserts that when the CLK signal is low, digital switch transistors MP9 and MP10 turn on and transmit voltage AVDD "to the differential amplifier" via diode-connected transistors MP5 and MP6, thus regulating the differential amplifier's gain. Pet. 52; *see* Ex. 1003 ¶¶ 121, 143. Second, Petitioner asserts that when the CLK signal is high, digital switch transistors MP9 and MP10 turn off and "produce a high-impedance output." Pet. 52 (emphasis omitted); *see* Ex. 1003 ¶¶ 122, 143. Petitioner contends that this high-impedance output deprives diode-connected transistors MP5 and MP6 of voltage AVDD, thus allowing the differential amplifier "to operate unregulated, behaving like a differential sense amplifier" with a high gain. Pet. 52–53; *see* Ex. 1003 ¶¶ 122–123, 138, 140, 143.

To support Petitioner's assertions, Dr. Jacob explained that digital switch transistors MP9 and MP10 turn on or off to alternately connect and disconnect diode-connected transistors MP5 and MP6 to the differential amplifier, thus "changing the amplifier's behavior from regulated-gain to unregulated-gain." Ex. 1003 ¶¶ 125, 143–144 (citing Ex. 1005, 2:8–46, 4:50–55, 5:48–59, 6:6–25); *see id.* ¶¶ 116, 121–124, 138.

Patent Owner does not make any arguments specific to claim 1's "impedance control circuit" limitation. *See, e.g.*, Resp. 30–36.

We agree with Petitioner that transistors MP5, MP6, MP9, and MP10 act as "an impedance control circuit" according to claim 1. *See* Ex. 1003 ¶¶ 120–125, 143–144. As Dr. Jacob explained, digital switch transistors MP9 and MP10 turn on or off to alternately connect and disconnect diode-connected transistors MP5 and MP6 to the differential amplifier, thus "changing the amplifier's behavior from regulated-gain to unregulated-

gain." Ex. 1003 ¶¶ 125, 143–144; *see id.* ¶¶ 116, 120–124, 138; Ex. 1005, 2:8–46, 4:50–55, 5:48–59, 6:6–25. Turning digital switch transistors MP9 and MP10 on or off changes their impedance. Ex. 1003 ¶¶ 122, 140, 143.

Specifically, with digital switch transistors MP9 and MP10 turned off, they "produce as output a high impedance value" and disconnect diode-connected transistors MP5 and MP6 from voltage AVDD. Ex. 1003 ¶ 122. In that state, "no voltage at all comes through transistors MP9 and MP10," and diode-connected transistors MP5 and MP6 "are cut off and therefore nonfunctional." *Id.*

For the reasons discussed above, Lim's latching comparator circuit includes "an impedance control circuit" according to claim 1.

(e) The "Level Converter" Limitation

Claim 1 also recites "a level converter responsive to the differential amplifier and the impedance control circuit." Ex. 1001, 7:1–2. For the claimed "level converter," Petitioner identifies in Lim's Figure 3 the following components: inverter circuit 10 (including transistor MP12 and transistor MN12) and inverter circuit 12 (including transistor MP11 and transistor MN11). Pet. 53–54; *see* Ex. 1003 ¶¶ 145–148.

Petitioner contends that "Lim discloses that the function of the inverters [10 and 12] is to provide an output signal 'at appropriate CMOS logic voltage levels,' which is the definition of a level converter." Pet. 54 (quoting Ex. 1005, 5:62–63); *see* Ex. 1003 ¶ 146. Petitioner asserts that inverter circuits 10 and 12 are responsive to the differential amplifier because they receive as input signals the differential amplifier's output signals. Pet. 55; *see* Ex. 1003 ¶¶ 116, 145–148. Petitioner also asserts that inverter circuits 10 and 12 are responsive to the impedance-control circuit

because it changes the differential amplifier's operating mode depending on the CLK signal. Pet. 55; *see* Ex. 1003 ¶¶ 120–125, 138, 143–144, 147–148.

Patent Owner does not make any arguments specific to claim 1's "level converter" limitation. *See, e.g.*, Resp. 30–36.

We agree with Petitioner that inverter circuits 10 and 12 act as "a level converter responsive to the differential amplifier and the impedance control circuit" according to claim 1 for three reasons. *See* Ex. 1003 ¶¶ 116, 120–125, 131, 138, 143–144, 147–148. First, inverter circuits 10 and 12 are responsive to the differential amplifier because they receive as input signals the differential amplifier's output signals. *See* Ex. 1003 ¶¶ 116, 145–148. Specifically, inverter circuit 10 receives an input signal from the latching stage's OUT node defined by transistors MN6, MP7, and MP8 in the differential amplifier. Ex. 1005, 5:60–61, Figs. 2–3; *see* Ex. 1003 ¶¶ 116, 123, 128; Ex. 2001 ¶ 72. Similarly, inverter circuit 12 receives an input signal from the latching stage's NOUT node defined by transistors MN5, MP7, and MP8 in the differential amplifier. Ex. 1005, 5:63–64, Figs. 2–3; *see* Ex. 1003 ¶¶ 116, 123, 128; Ex. 2001 ¶ 72.

Second, inverter circuits 10 and 12 are responsive to the impedance-control circuit because it changes the differential amplifier's operating mode depending on the CLK signal. *See* Ex. 1003 ¶¶ 120–125, 138, 143–144, 147–148.

Third, inverter circuits 10 and 12 level convert the input signals received from the differential amplifier. Ex. 1003 ¶¶ 116, 126–128, 131, 146–147. Specifically, inverter circuit 10 "provides an inverted output signal IOUT at appropriate CMOS logic voltage levels." Ex. 1005, 5:61–63, Fig. 3; *see* Ex. 1003 ¶¶ 116, 126–127, 146; Ex. 2001 ¶ 72. Similarly,

inverter circuit 12 "provides an inverted output signal INOUT." Ex. 1005, 5:63–65, Fig. 3; *see* Ex. 1003 ¶¶ 116, 126–127, 146; Ex. 2001 ¶ 72. Inverter circuits 10 and 12 "ensure that any less-than-fully-digital output from" the differential amplifier increases to a suitable digital level. Ex. 1003 ¶¶ 116, 131, 146.

For the reasons discussed above, Lim's latching comparator circuit includes "a level converter responsive to the differential amplifier and the impedance control circuit" according to claim 1.

(f) The "Clock-Free Latch" Limitation

Claim 1 further recites "a clock-free latch responsive to the level converter." Ex. 1001, 7:3. For the claimed "clock-free latch," Petitioner identifies in Lim's Figure 3 RS-latch circuit 14. Pet. 55–56; *see* Ex. 1003 ¶¶ 149–150. Petitioner asserts that RS-latch circuit 14 is responsive to the level converter because RS-latch 14 receives as input signals "the fully digital output signal[s] of the level converters," i.e., inverter circuits 10 and 12. Pet. 55–56; *see* Ex. 1003 ¶ 149.

Patent Owner does not make any arguments specific to claim 1's "clock-free latch" limitation. *See, e.g.*, Resp. 30–36.

We agree with Petitioner that RS-latch circuit 14 acts as "a clock-free latch responsive to the level converter" according to claim 1. *See* Ex. 1003 ¶¶ 116, 128, 149–150. Inverter circuit 10 "provides an inverted output signal IOUT" to RS-latch circuit 14. Ex. 1005, 5:61–66, Fig. 3; *see id.* at code (57); Ex. 1003 ¶ 150; Ex. 2001 ¶ 73. Inverter circuit 12 "provides an inverted output signal INOUT" to RS-latch circuit 14. Ex. 1005, 5:61–66, Fig. 3; *see id.* at code (57); Ex. 1003 ¶ 150; Ex. 2001 ¶ 73. The signals IOUT and INOUT "set the state of the RS latch to either 0/1 or 1/0," and the

"latch stores this state." Ex. 1003 ¶ 116. Hence, RS-latch circuit 14 is responsive to the level converter because that latch circuit receives as input signals the level converter's output signals. *See id.* ¶¶ 116, 128, 149–150.

Further, RS-latch circuit 14 "provides the final comparator output signals CMPOUT and its complement NCMPOUT." Ex. 1005, 6:1–3; *see* Ex. 1003 ¶ 150; Ex. 2001 ¶ 73. Hence, "when IN is higher than REF, CMPOUT is a logic low, and when IN is less than REF, CMPOUT is a logic high." Ex. 1005, 6:3–5; *see* Ex. 1003 ¶ 150; Ex. 2001 ¶ 73. RS-latch circuit 14 stores a logic state at its output "indefinitely" until an enable or unlatch command occurs. *See* Ex. 1005, 1:25–32, 5:65–6:5, 6:17–25, 6:65–67; Ex. 2001 ¶ 62.

For the reasons discussed above, Lim's latching comparator circuit includes "a clock-free latch responsive to the level converter" according to claim 1.

(g) Whether Lim Anticipates Claim 1

For the reasons discussed above, Petitioner has not shown by a preponderance of the evidence that Lim's latching comparator circuit includes every element of claim 1 arranged as required by the claim, i.e., because Lim's circuit lacks the claimed "timing circuit" and a differential amplifier "responsive to the timing circuit." Hence, Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable under § 102(b) as anticipated by Lim.

D. Obviousness over Lim: Claim 1

1. OBVIOUSNESS UNDER 35 U.S.C. § 103

A patent may not be obtained "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter

as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). An obviousness analysis involves underlying factual inquiries including (1) the scope and content of the prior art; (2) differences between the claimed invention and the prior art; (3) the level of ordinary skill in the art; and (4) where in evidence, objective evidence of nonobviousness, such as commercial success, long-felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 35–36 (1966); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047–48 (Fed. Cir. 2016) (en banc).

"An obviousness determination requires finding that a person of ordinary skill in the art would have been motivated to combine or modify the teachings in the prior art and would have had a reasonable expectation of success in doing so." *Regents of Univ. of Cal. v. Broad Inst., Inc.*, 903 F.3d 1286, 1291 (Fed. Cir. 2018); *In re Stepan Co.*, 868 F.3d 1342, 1345–46, 1346 n.1 (Fed. Cir. 2017). Thus, an obviousness analysis should address "whether there was an apparent reason" to combine or modify "known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Moreover, "mere conclusory statements" do not suffice for an apparent reason to combine or modify. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Crediting conclusory statements "risks allowing the challenger to use the challenged patent as a roadmap to reconstruct the claimed invention using disparate elements from the prior art—i.e., the impermissible *ex post* reasoning and hindsight bias that *KSR* warned

against." *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019).

We analyze the obviousness issues according to these principles.

2. WHETHER THE SUBJECT MATTER OF CLAIM 1 WOULD HAVE BEEN OBVIOUS OVER LIM

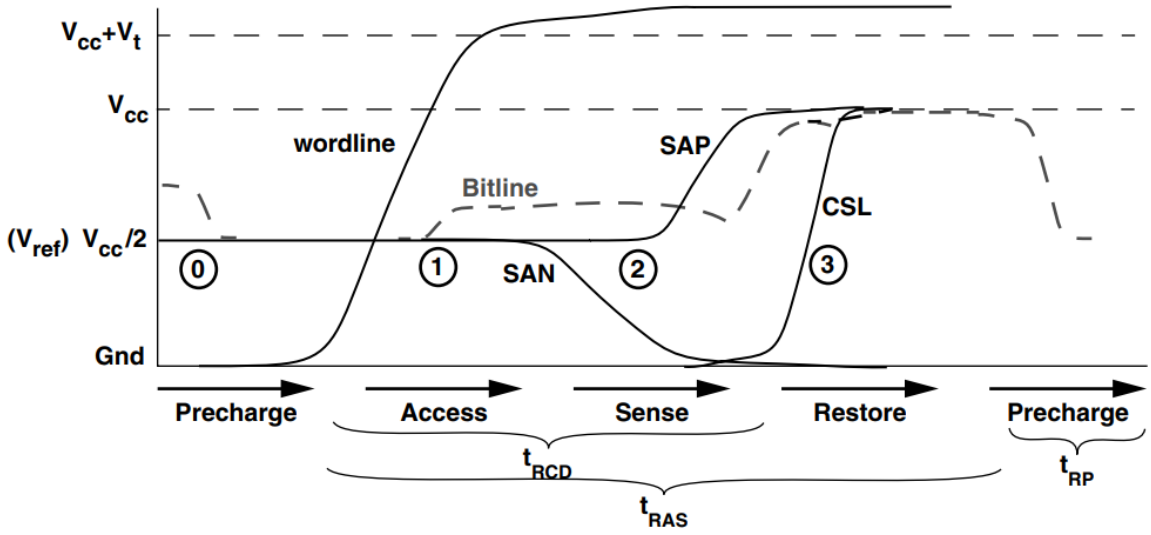
As discussed above for the anticipation ground, claim 1 differs from Lim's latching comparator circuit because Lim's circuit lacks the claimed "timing circuit" and a differential amplifier "responsive to the timing circuit." *See supra* §§ III.C.3(b)–(c).

Petitioner asserts that to "the extent that Lim does not disclose a timing circuit and a differential amplifier responsive to that circuit," it "would have been an obvious modification to make to Lim" for an ordinarily skilled artisan. Pet. 60; *see* Ex. 1003 ¶¶ 154–157. Petitioner also asserts that an ordinarily skilled artisan "would have known that memory devices have sense amplifiers, and the sense-amplifier timing mechanisms are all driven by timing circuits." Pet. 60; *see* Ex. 1003 ¶ 154.

Specifically, Petitioner identifies the SAN and SAP control signals for sense amplifiers. Pet. 60; *see id.* at 16–18; Ex. 1003 ¶¶ 53–60, 154–156. SAN refers to "Sense-Amplifier N-Fet Control," and SAP refers to "Sense-Amplifier P-Fet Control." Ex. 1006, 362.[2] "The SAN signal controls activation of the NFets in the sensing circuit, and the SAP signal controls the activation of the PFets in the sensing circuit." *Id.*

[2] For this publication, a page number in the citation references a page number in the publication itself rather than a page number added by Petitioner, e.g., 1006-1, 1006-2, 1006-3, etc.

Petitioner provides the timing diagram for a sense amplifier reproduced below. Pet. 17; *see* Ex. 1003 ¶¶ 56, 156; Ex. 1006, 365.



This timing diagram depicts four phases: a precharge phase shown as phase 0; an access phase shown as phase 1; a sense phase shown as phase 2; and a restore phase shown as phase 3. Ex. 1003 ¶¶ 57–60; *see* Ex. 1006, 363–65. In phase 2, the SAN and SAP control signals "are activated in quick succession and drive the voltage on the bitline to the full voltage." Ex. 1006, 365; *see* Ex. 1003 ¶¶ 59, 156.

Petitioner contends that this "timing diagram of the known SAN and SAP control signals for a sense amplifier clearly indicate[s] that the two signals have a different phase delay, as the SAN signal is falling while the SAP signal is rising." Reply 19.

To support Petitioner's contention, Dr. Jacob stated that an ordinarily skilled artisan would have been familiar with "the timing of the SAN and SAP control circuits." Ex. 1003 ¶¶ 156–157; *see* Pet. 62. He also stated that "this is simply how these circuits operate: memory arrays have sense amplifiers, and those sense amplifiers are controlled by timing circuits," and

therefore a skilled artisan "would have found it obvious to include these mechanisms in the memory device." Ex. 1003 ¶ 157; *see* Pet. 62.

In addition, Dr. Jacob identified three reasons why an ordinarily skilled artisan "would have been motivated to use a more complex timing circuit in Lim." Ex. 1020 ¶ 45; *see* Reply 20–22. According to Dr. Jacob, the resulting "modifications would have been trivial changes and well within the skill set of a person of ordinary skill in the art." Ex. 1020 ¶ 46; *see* Reply 22.

As one reason, Dr. Jacob stated that if "for reasons of die-area efficiency" a skilled artisan "desired to use NMOS devices instead of PMOS devices for the impedance-control circuit (for instance, replacing MP9 and MP10 with NMOS devices)," the skilled artisan "would have inserted an inverter in the CLK signal path, thereby changing high to low and low to high, as appropriate for NMOS devices." Ex. 1020 ¶ 45; *see* Reply 21.

As another reason, Dr. Jacob stated that if "the on/off period of the CLK signal were 180° out of phase with the operation of the rest of the circuit (if it shut off the impedance-control circuit when it should turn it on, and vice versa)," the skilled artisan "would have inserted an inverter in the CLK signal path, to change the phase 180°, thereby changing high to low and low to high, and also changing the on/off orientation of the impedance-control circuit." Ex. 1020 ¶ 45; *see* Reply 21.

As yet another reason, Dr. Jacob stated that if "the period of the CLK signal did not perfectly match the desired on/off behavior of the claimed impedance-control circuit (which includes PMOS devices MP9 and MP10)—for instance, if it turned on or off slightly early or slightly late," the skilled artisan "would have desired to alter the duty cycle and/or phase offset

of the CLK signal, which would have required additional logic such as delays inserted in the signal path." Ex. 1020 ¶ 45; *see* Reply 21–22.

Patent Owner disputes that an ordinarily skilled artisan would have been motivated to modify Lim's latching comparator circuit to include the claimed "timing circuit," i.e., "an electrical circuit that generates and outputs a plurality of different versions of a clock signal." *See* Resp. 33–36; Sur-reply 17–26; Ex. 2001 ¶¶ 93–98.

In particular, Patent Owner argues that Lim's latching comparator circuit requires that digital switch transistors MP9 and MP10 "receive and be controlled by the same, single signal, CLK, and not different versions of a clock signal." Resp. 34 (emphasis omitted); *see* Ex. 2001 ¶¶ 94–95. Patent Owner asserts that transistors MP9 and MP10 function as "a single switch" and, therefore, "must be controlled by the same single clock signal, not signals that are delayed with respect to one another," such as the SAN and SAP control signals. Sur-reply 19–20. Patent Owner contends that connecting "two different versions of a clock signal" to the gates of transistors MP9 and MP10 would "make no sense" because Lim describes the transistors as "connected in parallel." Resp. 35; *see* Ex. 2001 ¶¶ 96–97.

In addition, Patent Owner notes that Lim discloses that a "single transistor may be used" as the digital switch. Resp. 35 (citing Ex. 1005, 5:56–59); *see* Sur-reply 19; Ex. 2001 ¶ 96. Patent Owner then contends that connecting "two different versions of a clock signal" to a single transistor would "not even be feasible." Resp. 35; *see* Ex. 2001 ¶ 98.

Regarding Dr. Jacob's three reasons for using "a more complex timing circuit in Lim," Patent Owner asserts that he offered "puzzling solutions" to "non-existent problems" and "solutions that result in the

transistors in Lim still not receiving different versions of the clock signal as required by claim 1." Sur-reply 21. Patent Owner also asserts that Dr. Jacob relied on "assumptions that have no support." *Id.* at 23.

For the reasons explained below, we agree with Patent Owner that an ordinarily skilled artisan would not have been motivated to modify Lim's latching comparator circuit to include the claimed "timing circuit," i.e., "an electrical circuit that generates and outputs a plurality of different versions of a clock signal."

As discussed above for the anticipation ground, digital switch transistors MP9 and MP10 act together as a single switch. Ex. 1005, code (57), 5:48–59, 6:6–25, 6:65–7:2, Fig. 2; *see id.* at 2:21–38, 7:17–18; Ex. 1003 ¶¶ 138, 144; Ex. 2001 ¶¶ 71, 93–98; *supra* § III.C.3(b)(vi). When turned on by a low CLK signal, transistors MP9 and MP10 act together to connect the switch node to voltage AVDD. Ex. 1005, 5:48–56, 6:6–18, Fig. 2; *see id.* at 2:21–31; Ex. 1003 ¶¶ 121, 143; Ex. 2001 ¶¶ 71, 94. When turned off by a high CLK signal, transistors MP9 and MP10 act together to disconnect the switch node from voltage AVDD. Ex. 1005, 5:48–56, 6:6–25, 6:65–7:2, Fig. 2; *see id.* at 2:21–38; Ex. 1003 ¶¶ 122, 143; Ex. 2001 ¶¶ 71, 94.

Transistors MP9 and MP10 turn on or off together to control the gain of transistors MP7 and MP8 via diode-connected transistors MP5 and MP6 coupled to the switch node. Ex. 1005, 2:27–38, 6:9–25, Fig. 2; *see id.* at code (57), 4:50–55, 4:58–60; Ex. 1003 ¶¶ 116, 120–125, 140, 143–144; Ex. 2001 ¶ 94. Accordingly, as Dr. Khatri explained, "it is essential that MP9 and MP10 receive[] and are controlled by the same signal, CLK, not different versions of a clock signal." Ex. 2001 ¶ 95.

Because digital switch transistors MP9 and MP10 act together as a single switch, an ordinarily skilled artisan would have had "no reason and no motivation" to modify Lim's latching comparator circuit to provide different versions of a clock signal to the gates of transistors MP9 and MP10. Ex. 2001 ¶¶ 71, 93–95; *see id.* ¶¶ 96–98. Providing different versions of a clock signal to the gates of transistors MP9 and MP10 would cause them to turn on and off at different times. *See* Ex. 1005, 5:52–56, Fig. 2; Ex. 2001 ¶¶ 71, 96. If transistors MP9 and MP10 turned on and off at different times, only the on transistor would connect the switch node to voltage AVDD. *See* Ex. 1005, 2:21–27, 5:52–56, Fig. 2. Petitioner offers no reason why an ordinarily skilled artisan would have wanted to do that, i.e., have only one of two transistors connect the switch node to voltage AVDD. *See* Pet. 60–62; Reply 18–22; Ex. 1003 ¶¶ 154–157; Ex. 1020 ¶¶ 45–47.

That a skilled artisan would have (1) been familiar with "the timing of the SAN and SAP control circuits" and (2) known that "sense amplifiers are controlled by timing circuits" does not amount to a reason that would have prompted the skilled artisan to modify Lim's latching comparator circuit to supply the SAN and SAP control signals to the gates of transistors MP9 and MP10. *See* Pet. 60–62; Ex. 1003 ¶¶ 156–157. Also, Petitioner fails to explain why a skilled artisan would have selected the SAN control signal for NMOS devices for use with Lim's digital switch, which includes two PMOS devices and lacks NMOS devices. *See* Pet. 60–62; Reply 18–19; Ex. 1006, 362–65.

Further, Dr. Jacob's three reasons for using "a more complex timing circuit in Lim" fail to withstand scrutiny. As explained in more detail below, "a more complex timing circuit" does not equate to the claimed

"timing circuit," i.e., "an electrical circuit that generates and outputs a plurality of different versions of a clock signal."

Regarding Dr. Jacob's first reason discussed above, he stated that if "for reasons of die-area efficiency" a skilled artisan "desired to use NMOS devices instead of PMOS devices for the impedance-control circuit (for instance, replacing MP9 and MP10 with NMOS devices)," the skilled artisan "would have inserted an inverter in the CLK signal path, thereby changing high to low and low to high, as appropriate for NMOS devices." Ex. 1020 ¶ 45; *see* Reply 21. But Lim cautions against replacing a PMOS device with an NMOS device. Ex. 1005, 7:28–32. Specifically, when discussing an advantage of the latching comparator circuit in Figures 2 and 3, Lim explains that "since only P-type transistors (MP9 and MP10) are used as the digital switch, there is no need to derive an inverted latch clock signal," and "[t]his eliminates another source of tricky timing problems." *Id.* Dr. Jacob failed to explain why a skilled artisan would have disregarded that disclosure. *See* Ex. 1020 ¶¶ 45–47; *see also* Ex. 1003 ¶¶ 154–157.

Further, Dr. Jacob identified no evidence that (1) replacing PMOS devices MP9 and MP10 with NMOS devices and (2) adding an extra component, i.e., "an inverter in the CLK signal path," would have reduced the required die area. *See* Ex. 1020 ¶¶ 45–47; *see also* Ex. 1003 ¶¶ 154–157. An extra component would seem to require more die area, not less.

In any event, inserting "an inverter in the CLK signal path" to two NMOS devices used as the digital switch would not have provided different versions of a clock signal to the two NMOS devices. In that proposed arrangement, the two NMOS devices would receive at their respective gates the same inverted CLK signal.

Regarding Dr. Jacob's second reason discussed above, he stated that if "the on/off period of the CLK signal were 180° out of phase with the operation of the rest of the circuit (if it shut off the impedance-control circuit when it should turn it on, and vice versa)," the skilled artisan "would have inserted an inverter in the CLK signal path, to change the phase 180°, thereby changing high to low and low to high, and also changing the on/off orientation of the impedance-control circuit." Ex. 1020 ¶ 45; *see* Reply 21. But Dr. Jacob identified no evidence of any actual or potential 180°-out-of-phase signal problem. *See* Ex. 1020 ¶¶ 45–47; *see also* Ex. 1003 ¶¶ 154–157. In addition, inserting "an inverter in the CLK signal path" to PMOS devices MP9 and MP10 would not have provided different versions of a clock signal to the two PMOS devices. In that proposed arrangement, the two PMOS devices would receive at their respective gates the same inverted CLK signal.

Regarding Dr. Jacob's third reason discussed above, he stated that if "the period of the CLK signal did not perfectly match the desired on/off behavior of the claimed impedance-control circuit (which includes PMOS devices MP9 and MP10)—for instance, if it turned on or off slightly early or slightly late," the skilled artisan "would have desired to alter the duty cycle and/or phase offset of the CLK signal, which would have required additional logic such as delays inserted in the signal path." Ex. 1020 ¶ 45; *see* Reply 21–22. But Dr. Jacob identified no evidence of any actual or potential mismatch problem between the CLK signal and digital switch transistors MP9 and MP10. *See* Ex. 1020 ¶¶ 45–47; *see also* Ex. 1003 ¶¶ 154–157. Moreover, including additional logic in the signal path to transistors MP9 and MP10 would not have provided different versions of a clock signal to

the two transistors. In that proposed arrangement, the two transistors would receive at their respective gates the same logic signal.

As discussed above, digital switch transistors MP9 and MP10 turn on or off together to alternately connect and disconnect the switch node and voltage AVDD for gain-control purposes. Ex. 1005, 5:48–56, 6:6–25, 6:65–7:2, Fig. 2; *see id.* at code (57), 2:21–38, 4:50–55, 4:58–60; Ex. 1003 ¶¶ 116, 120–125, 140, 143–144; Ex. 2001 ¶¶ 71, 94. Dr. Jacob offered no reason why an ordinarily skilled artisan would have wanted to separately control the digital switch's two transistors with different versions of a clock signal. *See* Ex. 1020 ¶¶ 45–47; *see also* Ex. 1003 ¶¶ 154–157.

For the reasons discussed above, Petitioner fails to present evidence that an ordinarily skilled artisan would have been motivated to modify Lim's latching comparator circuit to include "a timing circuit" according to claim 1. Hence, Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable under § 103(a) as obvious over Lim.

IV. CONCLUSION

Based on the evidence presented with the Petition, the evidence introduced during the trial, and the parties' respective arguments, Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable under § 102(b) as anticipated by Lim or unpatentable under § 103(a) as obvious over Lim.

In summary:

Claim	35 U.S.C. §	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1	102(b)	Lim		1
1	103(a)	Lim		1

Claim	35 U.S.C. §	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
Overall Outcome				1

V. ORDER

Accordingly, it is

ORDERED that claim 1 of the '274 patent is not determined to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Robert C.F. Pérez
Christopher Kao
Brock S. Weber
PILLSBURY WINTHROP SHAW PITTMAN LLP
robert.perez@pillsburylaw.com
christopher.kao@pillsburylaw.com
brock.weber@pillsburylaw.com

PATENT OWNER:

Philip E. Levy
Robert W. Morris
ECKERT SEAMANS CHERIN & MELLOTT, LLC
plevy@eckertseamans.com
rwmorris@eckertseamans.com