UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RENESAS ELECTRONICS CORPORATION,
Petitioner,

v.

BROADCOM CORPORATION,
Patent Owner.

Case IPR2019-01041

Patent 7,512,752

PATENT OWNER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141(c) and 142 and 37 C.F.R. §§ 90.2(a) and 90.3, Patent Owner Broadcom Corporation hereby appeals to the United States Court of Appeals for the Federal Circuit from the Patent Trial and Appeal Board's ("Board") Final Written Decision, entered on October 30, 2020 (Paper No. 30), and from all underlying and related factual findings, orders, decisions, rulings and opinions regarding U.S. Patent No. 7,512,752 ("'752 patent").

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner further indicates that the issues on appeal may include, but are not limited to: Whether the Board erred in concluding that: claims 1, 2, 5, 7 and 8 of the '752 patent are unpatentable under 35 U.S.C. §103 as obvious based on Foster; claim 5 of the '752 patent is unpatentable under 35 U.S.C. §103 as obvious based on the combination of Foster and Sih.

Patent Owner further reserves the right to challenge any finding or determination supporting or relating to the issues above, and to challenge other issues decided adversely to Patent Owner.

Simultaneous with this submission, Patent Owner is electronically filing a copy of this Notice of Appeal and its Exhibit A with the Patent Trial and Appeal Board. In addition, Patent Owner is electronically filing a copy of this Notice of Appeal, including attachment, with the Clerk's Office for the United States Court of Appeals for the Federal Circuit, together with the required fees.

Respectfully submitted,

Date: December 29, 2020

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EXHIBIT A

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Paper 30
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RENESAS ELECTRONICS CORPORATION,
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IPR2019-01041
Patent 7,512,752 B2

Before THOMAS L. GIANNETTI, DANIEL J. GALLIGAN, and NORMAN H. BEAMER, *Administrative Patent Judges.*

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Renesas Electronics Corporation ("Petitioner") challenges the patentability of claims 1, 2, 5, 7, and 8[1] of U.S. Patent No. 7,512,752 B2 ("the '752 patent," Ex. 1001), which is assigned to Broadcom Corporation ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1, 2, 5, 7, and 8 of the '752 patent are unpatentable. *See* 35 U.S.C. § 316(e) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

On May 7, 2019, Petitioner requested *inter partes* review of claims 1, 2, 5, 7, and 8 of the '752 patent on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 5, 7, 8	103(a)[2]	Foster[3]
1, 2, 5, 7, 8	103(a)	Foster, Sih[4]
1, 2, 5, 7, 8	103(a)	Foster, Rovati[5]

[1] Although the first paragraph of the Petition identifies claims 1–10 as being challenged, the Petition's listing of grounds and its arguments are directed only to claims 1, 2, 5, 7, and 8. Pet. 1, 17.

[2] The Leahy-Smith America Invents Act ("AIA") included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the filing of the application for the '752 patent. Therefore, we apply the pre-AIA versions of these sections.

[3] Foster, US 6,240,492 B1, issued May 29, 2001 (Ex. 1007).

[4] Sih, US 2003/0106053 A1, published June 5, 2003 (Ex. 1005).

[5] Rovati, US 2002/0031179 A1, published Mar. 14, 2002 (Ex. 1004).

Paper 2 ("Pet."), 17. Patent Owner filed a Preliminary Response. Paper 6; *see also* Papers 7 (Petitioner's Reply to Patent Owner Preliminary Response), 8 (Patent Owner's Sur-reply to Petitioner's Reply). We instituted trial on all grounds of unpatentability. Paper 9, 16.

During the trial, Patent Owner filed a Response (Paper 18, "PO Resp."), Petitioner filed a Reply (Paper 22, "Reply"), and Patent Owner filed a Sur-reply (Paper 23, "Sur-reply").

An oral hearing was held on August 6, 2020, a transcript of which appears in the record. Paper 29 ("Tr.").

B. Related Matters

The parties state that the '752 patent is at issue in the following investigation at the International Trade Commission: *Certain Infotainment Systems, Components Thereof, and Automobiles Containing the Same*, Inv. No. 337-TA-1119. Pet. 64; Paper 5, 2. The parties state that the '752 patent is also at issue in *Broadcom Corporation v. Toyota Motor Corporation et al.*, No. 2-18-cv-00190-JRG (E.D. Tex.). Pet. 64; Paper 5, 2.

C. Real Parties in Interest

Petitioner identifies itself and Renesas Electronics America, Inc. as real parties in interest. Pet. 64. Patent Owner identifies itself as the real party in interest. Paper 5, 2.

D. The '752 Patent and Illustrative Claim

The '752 patent discloses a "memory access unit compris[ing] an output port for providing access requests for lists of addresses in a memory over a link to a memory controller." Ex. 1001, code (57). The '752 patent discloses that the memory access unit may have a queue that "queues the access requests for the lists of addresses." Ex. 1001, 3:20–23.

Challenged independent claim 1 recites the following:

> A memory access unit for accessing data for a module, said memory access unit comprising:
>
> an output port for providing access requests for lists of addresses in a memory over a link to a memory controller; and
>
> a queue for queuing the access requests for the lists of addresses.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner's declarant, Dr. Vivek Subramanian, testifies that "a person of ordinary skill in the art at the time of the alleged invention would have had a Bachelor's Degree in Electrical Engineering, Computer Science, or a similar discipline, with at least two years of experience working with memory access and digital video processing." Ex. 1003 ¶ 47. Citing the testimony of its declarant, Dr. Marilyn Wolf, Patent Owner proposes a similar definition, arguing that a person of ordinary skill in the art "would have had a Bachelor's Degree in Electrical Engineering, Computer Science, or a similar discipline, with one to two years of experience in this or a related field. The [person of ordinary skill in the art] would also have been familiar with memory access and digital video processing." PO Resp. 11 (citing Ex. 2005 ¶ 16).

The parties, therefore, differ on the amount of experience that is required with memory access and digital video processing technologies, and both parties' definitions are somewhat imprecise. Patent Owner's definition requires some familiarity without defining how much is enough, while Petitioner's definition requires *at least* two years of experience, which is open-ended and would include a person whose experience far exceeds that

of a person of ordinary skill in the art. Neither party explains how its recited level of skill impacts the obviousness analysis such that application of one proposal versus the other would lead to different ultimate outcomes.

Based on the record before us, including the types of problems and solutions described in the '752 patent and the cited prior art, we determine that a person of ordinary skill in the art would have had a bachelor's degree in electrical engineering, computer science, or a similar discipline, with two years of experience working with memory access and digital video processing. We further note that our analysis would be the same under either party's definition.

B. Claim Interpretation

The Petition was accorded a filing date of May 7, 2019. Paper 3, 1. In an *inter partes* review for a petition filed on or after November 13, 2018, a claim "shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018) (now codified at 37 C.F.R. § 42.100(b) (2019)).

Petitioner proposes express constructions for two phrases that appear in claim 1. Pet. 8–16. First, Petitioner argues that the phrase "access requests for lists of addresses in a memory" means "memory access requests, each of which is a request that includes a list of multiple memory addresses." Pet. 8–11. Thus, according to Petitioner, a list must have more than one address. Pet. 8–11. Patent Owner argues that this phrase means

"memory access requests for data stored in memory at one or more addresses" and that a list can have a single address. PO Resp. 13–16. Second, Petitioner argues that the phrase "a link to a memory controller" means "a non-shared bus from the memory access unit to a memory controller." Pet. 11–16. Patent Owner argues that this phrase means "a connection to a memory controller." PO Resp. 16–22.

During the oral argument, Petitioner stated that "Petitioner is prepared to accept Patent Owner's constructions for the purpose of this proceeding." Tr. 7:3–4. Thus, there are now no terms whose meanings are in controversy, and we do not find it necessary to construe expressly any claim terms. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy' . . . ." (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary

considerations, if in evidence.[6] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Obviousness over Foster (Claims 1, 2, 5, 7, and 8)

Petitioner asserts that claims 1, 2, 5, 7, and 8 of the '752 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Foster. Pet. 17–48, 62–63.

1. Foster

Foster discloses a memory interface for accessing multiple memories in the context of a video decoder. Ex. 1007, code (57), 6:19–47. Figure 2 of Foster is reproduced below.

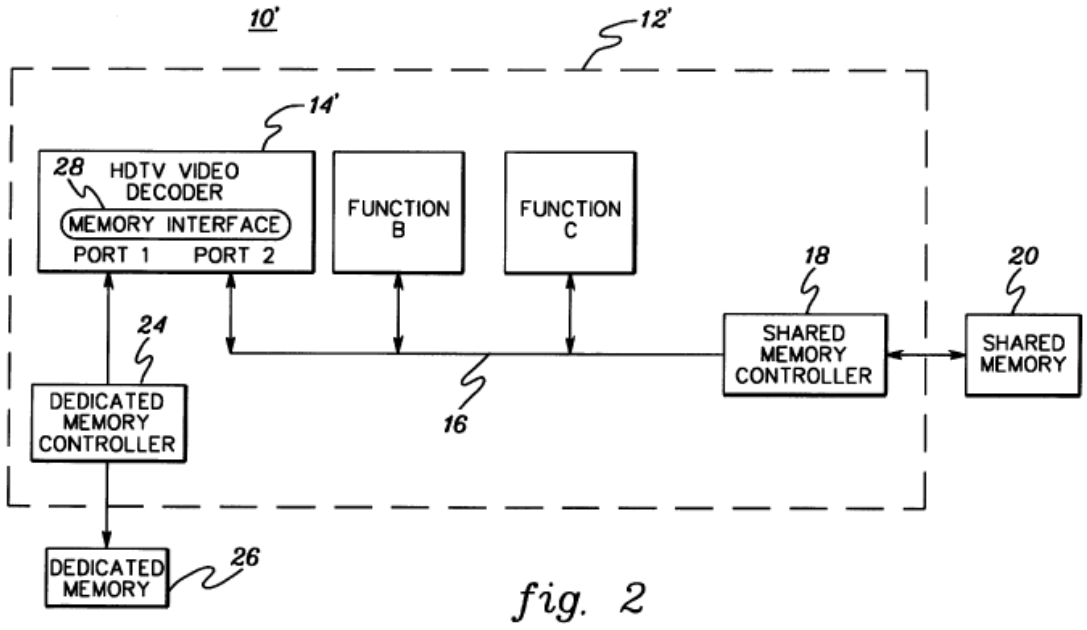

fig. 2

Figure 2 of Foster, reproduced above, shows integrated circuit chip 12' having video decoder 14' with memory interface 28 and two memory ports, labeled "PORT 1" and "PORT 2." Ex. 1007, 6:19–47. Foster discloses that

[6] Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

"port 1 [is] coupled to dedicated bus 22 for accessing dedicated memory 26 through dedicated memory controller 24." Ex. 1007, 6:28–34.

Figure 4 of Foster is reproduced below.

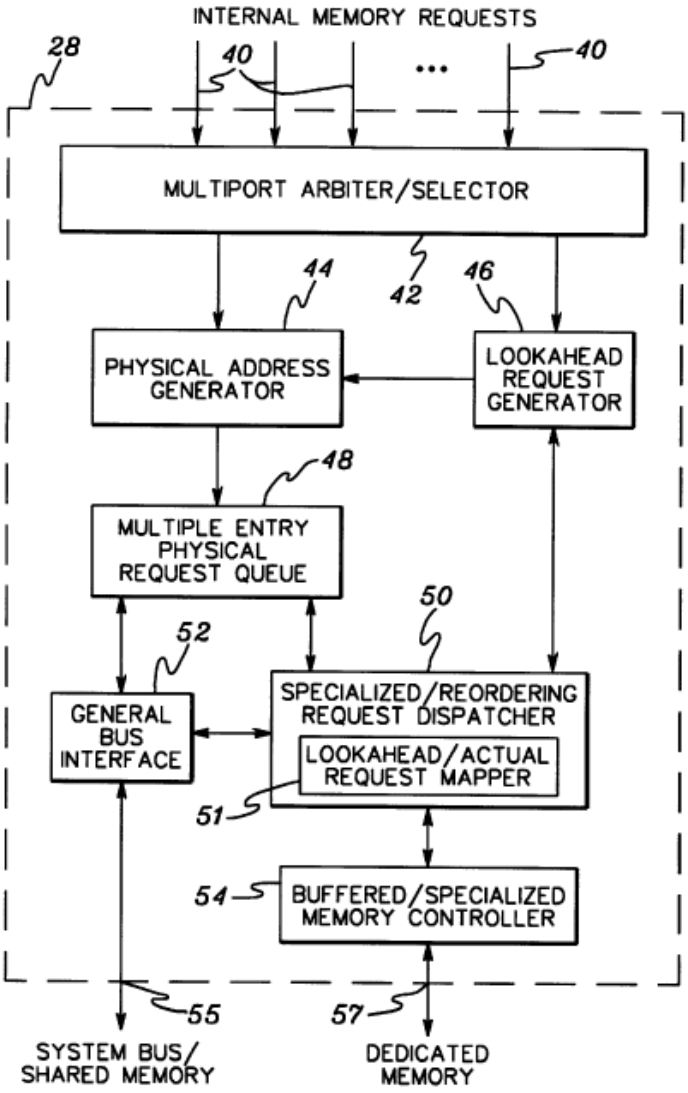

fig. 4

Figure 4 depicts an embodiment of memory interface 28. Ex. 1007, 7:54–58. Figure 4 shows that memory interface 28 has multiple entry physical request queue 48, and Foster discloses that "physical address requests are then pooled logically in multiple queues, (each queue corresponding to one

memory port) in a multi-entry physical request queue 48." Ex. 1007, 8:11–14.

2. Independent Claim 1

As noted above, independent claim 1 recites the following:

> A memory access unit for accessing data for a module, said memory access unit comprising:
>
> an output port for providing access requests for lists of addresses in a memory over a link to a memory controller; and
>
> a queue for queuing the access requests for the lists of addresses.

Petitioner contends that Foster's disclosure of memory interface 28 in video decoder 14' teaches "[a] memory access unit for accessing data for a module," as recited in the preamble of claim 1. Pet. 22–23 (citing Ex. 1007, 6:22–34, Fig. 2; Ex. 1003 ¶¶ 62–63). In particular, Foster discloses that video decoder 14' has "requesting units," such as "a motion compensation unit." Ex. 1007, 6:25–28. Memory interface 28 accesses data for the requesting units. Ex. 1007, 2:50–54 ("The memory interface further includes a receiver for receiving memory fetch requests from at least one requesting unit within the functional unit and a controller for controlling forwarding of each memory fetch request to either the dedicated memory or the shared memory.").

Patent Owner does not dispute Petitioner's contentions as to the subject matter recited in the preamble. We are persuaded by Petitioner's contentions and evidence, summarized above, and we find that Foster teaches the subject matter recited in the preamble.[7]

[7] Because we find that Petitioner has shown that Foster teaches this subject matter, we need not decide whether the preamble of claim 1 is limiting.

Petitioner contends that Foster discloses an output port, such as "PORT 1" in Figure 2, and thereby teaches "an output port for providing access requests for lists of addresses in a memory over a link to a memory controller." Pet. 23–24, 30–31 (citing Ex. 1007, 2:50–54, 2:65–67, 5:35–37, 5:63–6:1, 6:28–34, Fig. 2; Ex. 1003 ¶¶ 64, 76), 62–63 (citing Ex. 1007, 7:61–65, 8:11–14, 9:32–35; Ex. 1003 ¶¶ 151–152). For example, Foster discloses that "port 1 [is] coupled to dedicated bus 22 for accessing dedicated memory 26 through dedicated memory controller 24." Ex. 1007, 6:28–34. Foster further discloses that, "[d]uring operation, the memory interface directs accesses to the appropriate memory port based on logical addressing contained within the memory fetch requests received from the requesting units." Ex. 1007, 7:1–4.

Petitioner further contends that "Foster discloses that the motion compensation unit typically sends eight memory access requests, each including a 'list' of one address, which are then processed by the memory interface to generate requests the memory can understand." Pet. 63 (citing Ex. 1007, 7:61–65, 9:32–35; Ex. 1003 ¶ 152). For example, Foster discloses that "a motion compensation unit may be generating requests for a block of data it is processing" and that "[t]his processing typically generates a series of eight requests with each address separated by a fixed value." Ex. 1007, 9:32–35.

Petitioner further contends that Foster's multiple entry physical request queue 48, shown in Figure 4, teaches a queue for queuing the access requests. Pet. 31–34 (citing Ex. 1007, 5:43–48, 7:41–44, 7:54–65, 8:11–14, 9:52–55, 9:65–10:2; Ex. 1003 ¶¶ 78, 82–84). As noted above, Foster discloses that "physical address requests are then pooled logically in

multiple queues, (each queue corresponding to one memory port) in a multi-entry physical request queue 48." Ex. 1007, 8:11–14.

Patent Owner does not dispute that Foster discloses "an output port" and "a queue," but Patent Owner argues that the disclosures of each are in different embodiments that cannot be combined. PO Resp. 22–26. More particularly, Patent Owner argues that "Foster discloses distinct embodiments that include either an external memory controller (Figures 1 and 2) or an internal memory controller (Figure 4), but not both." PO Resp. 23–24 (citing Ex. 1007, 5:67–6:1). Patent Owner argues that a person of ordinary skill in the art "would consider these two embodiments to be distinct, incompatible devices . . . that cannot and would not be combined together." PO Resp. 24 (citing Ex. 2005 ¶ 37). According to Patent Owner, therefore, Petitioner's contentions fail because the internal memory controller configuration of Figure 4 does not have an output port going to a memory controller, while the external memory controller configurations of Figures 1 and 2 "do not disclose a [memory access unit (MAU)] that output[]s 'access requests for lists of addresses' or a MAU that includes 'a queue for queuing the access requests for the lists of addresses.'" PO Resp. 25–26 (citing Ex. 2005 ¶¶ 39–40).

We agree with Petitioner that Patent Owner's arguments reflect "an overly narrow reading of Foster." *See* Reply 4. Foster gives the following introduction to its disclosed invention:

> Generally stated, this invention is targeted to integrated systems having several functions on a single chip wherein the functions access multiple memories. Conventionally, the multiple memories comprise off-chip memories, however, one or more of the memories described herein may alternatively comprise on-chip memory space. *Pursuant to one aspect of the*

> *present invention, a functional unit is provided with multiple memory ports, each memory port coupling to a different type of memory.* For example, one port couples via a dedicated bus to dedicated memory, while another port couples via a general system bus to shared memory. *In another aspect, this invention comprises a lookahead request generator implemented within a memory interface of a functional unit.* The lookahead request generator intelligently generates speculative memory requests based on actual memory requests received from the requesting units and based on predefined information, such as known memory request patterns. Further, this invention preferably employs an automated reordering of memory requests at a request dispatcher in order to optimize bandwidth on the communications link coupling the memory interface to dedicated memory, as well as the internal memory banks of the dedicated memory. *FIGS. 1–3 depict examples of the multi-port aspect, while FIGS. 4–7 depict the lookahead request generator and reordering concepts of the present invention*.

Ex. 1007, 5:27–52 (emphases added). Therefore, Foster describes Figure 4 as directed to the same invention as Figures 1 and 2 but as illustrating different aspects of that invention. Contrary to Patent Owner's arguments, Foster's Figure 4 is in fact complementary to, not incompatible with, Figures 1 and 2.

Patent Owner argues that Foster's "Figure 4, which depicts a MAU with an internal memory controller," "does not disclose an 'output port' that provides the alleged access requests 'over a link to a memory controller' as required by Claim 1." PO Resp. 25–26 (citing Ex. 2005 ¶ 39; Ex. 1007, 9:11–13, Figs. 4, 7). We disagree. Foster explains the following:

> Significant to this invention is the presentation of functional unit A with multiple memory ports. A first memory port is coupled to the general system bus 16, while (in this example) *a second memory port connects to a dedicated bus 22 coupled to dedicated memory 26 directly through a dedicated memory controller 24 (shown in phantom) which can be external*

> *or internal to functional unit A*. Memory requests are directed by a memory interface 28 in accordance with this invention to either the first memory port or the second memory port.

Ex. 1007, 5:62–6:4 (emphasis added). Thus, Foster is not concerned with whether the memory controller is internal or external. *See* Ex. 1016 ¶ 4 (Dr. Subramanian testifying that "[t]o a POSITA, something is shown 'in phantom,' usually indicated by a dotted line, when it could be in alternative positions" (citing Appx. A (*Engineering Drawing and Design*))). Rather, Foster discloses that, whether the memory controller is internal or external, memory requests are output from the "memory port" to the memory controller. Ex. 1007, 5:62–6:4.

Furthermore, we disagree with Patent Owner's argument that Foster does not show "a link to a memory controller" when the memory controller is internal to the MAU. *See* PO Resp. 25–26. As noted above, Foster discloses that "a second memory port connects to a dedicated bus 22 coupled to dedicated memory 26 directly through a dedicated memory controller 24 (shown in phantom) which can be external or internal to functional unit A." Ex. 1007, 5:63–6:1. Thus, Foster discloses that, even when the memory controller is internal to the MAU, the memory port connects to memory controller 24 over dedicated bus 22. We are persuaded, and we find, that Foster's dedicated bus 22 teaches "a connection to a memory controller" under the parties' agreed construction of "a link to a memory controller."

As noted above, Petitioner contends that Foster discloses generating eight memory access requests, each of which has one address, thus teaching "access requests for lists of addresses" under the parties' agreed construction that a list may comprise a single address. Pet. 63 (citing Ex. 1007, 7:61–65, 9:32–35; Ex. 1003 ¶ 152). Patent Owner does not dispute this contention,

apart from its dispute about "output port," discussed above. We are persuaded, and we find, that Foster describes "access requests for lists of addresses" because Foster discloses that "a motion compensation unit may be generating requests for a block of data it is processing" and that "[t]his processing typically generates a series of eight requests with each address separated by a fixed value." Ex. 1007, 9:32–35.

Based on the foregoing, we are persuaded, and we find, that Foster's disclosure of providing memory requests from a memory port through a dedicated memory controller to a dedicated memory teaches "an output port for providing access requests for lists of addresses in a memory over a link to a memory controller," as recited in claim 1.

As noted above, Petitioner contends that Foster's multiple entry physical request queue 48, shown in Figure 4, teaches a queue for queuing the access requests. Pet. 31–34 (citing Ex. 1007, 5:43–48, 7:41–44, 7:54–65, 8:11–14, 9:52–55, 9:65–10:2; Ex. 1003 ¶¶ 78, 82–84). Patent Owner does not dispute that Foster discloses a queue but argues that Figure 4's disclosure is incompatible with the configurations of Figures 1 and 2. PO Resp. 22–26. As discussed above, we disagree with Patent Owner's argument. We are persuaded, and we find, that Foster teaches "a queue for queuing the access requests for the lists of addresses," as recited in claim 1, because Foster discloses that "physical address requests are then pooled logically in multiple queues, (each queue corresponding to one memory port) in a multi-entry physical request queue 48." Ex. 1007, 8:11–14.

For the reasons discussed above, we find that Foster teaches the subject matter recited in claim 1, and, therefore, Petitioner has proven by a

preponderance of the evidence that claim 1 of the '752 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Foster.

3. Claim 2

Claim 2 recites the following:

> The memory access unit of claim 1, further comprising:
> an input port for receiving requests for blocks of pixels from a motion prediction processing unit; and
> logic for generating the lists of addresses from the requests for blocks of pixels, wherein the lists of addresses correspond to addresses in a memory that store pixels in the blocks of pixels.

Petitioner contends that Foster's "memory interface 28 receives requests from a motion compensation unit for fetching pixel data" and, therefore, that Foster teaches "an input port for receiving requests for blocks of pixels from a motion prediction processing unit." Pet. 34 (citing Ex. 1007, 8:60–63, 9:32–33; Ex. 1003 ¶¶ 87–88). Petitioner contends Foster's physical address generator 44 teaches "logic for generating the lists of addresses from the requests for blocks of pixels." Pet. 36 (citing Ex. 1007, 7:38–41, 7:61–65, 9:32–33, 10:16–20; Ex. 1003 ¶¶ 92–93). Petitioner contends that "Foster's addresses correspond to blocks or macroblocks to be used in motion compensation" and that "[t]o access a block of pixels, a request for a block of pixels must correspond to the multiple addresses in a memory where the data for each of those pixels is stored," and, therefore, Petitioner contends that Foster teaches that "the lists of addresses correspond to addresses in a memory that store pixels in the blocks of pixels." Pet. 37 (citing Ex. 1003 ¶ 95).

Patent Owner argues that Foster refers to requesting and processing "blocks of data," not "blocks of pixels" as recited in claim 2. PO Resp. 33–34 (citing Ex. 1007, 9:32–33; Ex. 2005 ¶ 52). Patent Owner argues, and

Dr. Wolf testifies, that Foster does not describe "[w]hat this data may or may not be . . . and Petitioner does not describe how this is an explicit or inherent disclosure of requests for 'blocks of pixels.'" PO Resp. 34; Ex. 2005 ¶ 52. Thus, Patent Owner argues that Petitioner has not shown that the memory access requests are for retrieving a particular type of data—pixels.

We disagree with Patent Owner. Foster discloses that the requests are for "blocks of data" that a motion compensation unit is processing. Ex. 1007, 9:32–33. Dr. Subramanian testifies that "[t]he purpose of a 'motion compensation unit' is to predict a frame in a video, taking into account the previous and/or future frames by accounting for motion of the camera and/or objects in the video." Ex. 1003 ¶ 89. Dr. Subramanian further testifies that "a [person of ordinary skill in the art] would know that 'block of data' [in Foster] refers to a block of pixels, because pixels are the most basic information the system must access in order to perform motion compensation." Ex. 1016 ¶ 11.

This testimony is consistent with Dr. Wolf's testimony that a person of ordinary skill in the art "would understand that a motion compensation unit does work on blocks of pixels." Ex. 2005 ¶ 53; *see also* PO Resp. 35 (argument based on this testimony). Dr. Wolf, however, testifies that the motion compensation unit "does not necessarily need to request those blocks of pixels from external memory. Foster's reference to 'requests' could be requests for any information involved in motion compensation processing." Ex. 2005 ¶ 53; *see also* PO Resp. 35 (Patent Owner's argument based on this testimony). This testimony from Dr. Wolf actually supports Petitioner's contention of unpatentability because claim 2 is directed to a "memory access unit" having "an input port for receiving requests for blocks of pixels

from a motion prediction processing unit." Dr. Wolf's testimony, therefore, shows that Foster's device has the capability to receive requests "for any information involved in motion compensation processing" including pixels. Similarly, we are not persuaded by Patent Owner's argument that Foster discloses that the "block of data" is being processed and, therefore, is not "what is being requested" (*see* PO Resp. 34–35 (citing Ex. 2005 ¶ 53)). Even if a particular block of data does not represent pixels, Foster still discloses an input port for receiving requests "for any information involved in motion compensation processing" including pixels. *See* Ex. 2005 ¶ 53.

Patent Owner also argues that Foster discloses requests for lines of data, not blocks of data. PO Resp. 35–36 (citing Ex. 1007, 9:33–41; Ex. 2005 ¶ 55). According to Patent Owner, Foster's "processing typically generates eight requests because the typical block of pixel data being processed would have been an 8 x 8 block of pixels and each request would have been for one row or column of pixel data." PO Resp. 36 (citing Ex. 2005 ¶ 55; Ex. 1001, 4:36–44). Patent Owner's argument is premised on its assertion that "[t]he language of the claim is clear, each received request must be for a block of pixels." Sur-reply 11. We disagree that there must be a one-to-one correspondence between a request and a block because claim 2 recites "an input port for receiving requests for blocks of pixels from a motion prediction processing unit." Thus, even if Foster discloses requests for lines of data, as asserted by Patent Owner, there would simply be multiple requests for a block of data, and for multiple blocks, there would be multiple requests, which is within the scope of "requests for blocks," as recited in claim 2.

Based on Petitioner's persuasive evidence and argument, we find that Foster teaches "an input port for receiving requests for blocks of pixels from a motion prediction processing unit." Patent Owner does not dispute Petitioner's contentions for the remaining subject matter recited in claim 2. We are persuaded, and we find, that Foster's physical address generator 44 teaches "logic for generating the lists of addresses from the requests for blocks of pixels, wherein the lists of addresses correspond to addresses in a memory that store pixels in the blocks of pixels." Pet. 36–37 (citing Ex. 1007, 7:38–41, 7:61–65, 9:32–33, 10:16–20; Ex. 1003 ¶¶ 92–93, 95). In particular, Foster discloses that "[e]ach selected request is forwarded to a physical address generator 44 where the logical address associated with the request is converted to a physical address for accessing memory space in one of the memories coupled to the memory interface." Ex. 1007, 7:61–65.

For the reasons discussed above, we find that Foster teaches the subject matter recited in claim 2, and, therefore, Petitioner has proven by a preponderance of the evidence that claim 2 of the '752 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Foster.

4. Claim 5

Claim 5 recites, "The memory access unit of claim 2, wherein the logic generates the access requests based on the list of addresses and based on sizes of each of the requests for blocks of pixels from the motion prediction processing unit."

For the recited "logic," Petitioner refers to its contentions for claim 2's "logic for generating the lists of addresses." Pet. 37. Petitioner argues that Foster teaches "generat[ing] the access requests based on the list of addresses and based on sizes of each of the requests for blocks of pixels

from the motion prediction processing unit" in two ways. Pet. 37–40. First, Petitioner relies on Foster's disclosure of generating addresses for lookahead requests. Pet. 37–38 (citing Ex. 1007, 8:56–63, 9:5–7, 9:27–29, 9:32–33, Fig. 5; Ex. 1003 ¶¶ 98–99). Patent Owner argues that Foster's lookahead request generator predicts "requests for data that the system anticipates needing in the future and, thus, are not for the data that was requested." PO Resp. 40 (citing Ex. 1007, 7:66–8:7, 8:56–9:31). We agree with Patent Owner on this point. Foster discloses that "lookahead request generator 46 receives requesting unit/burst information," which includes "the size of the request, as well as the logical address. . . . A burst analyzer 60 analyzes the access patterns of the actual requests. This analysis is then used to generate speculative lookahead requests via a logical address generator 62." Ex. 1007, 8:56–66. Because Foster's speculative lookahead requests deal with predicted accesses, we are not persuaded that Petitioner has shown how this disclosure of Foster teaches generating requests "based on the list of addresses," which "correspond to addresses in a memory that store pixels in the blocks of pixels" that were requested, as recited in claim 2, from which claim 5 depends.

Alternatively, Petitioner argues that "Foster also explains that the size of requests is taken into account when generating access requests, depending on whether the requests are seeking to access the shared or dedicated memory." Pet. 39–40 (citing Ex. 1007, 12:1–13; Ex. 1003 ¶ 100). Foster discloses the following:

> For shared memory, the data requests must be compliant with the established system bus protocol, and are optimized for short bursts to avoid dominating the bus (and preventing other devices from accessing memory). For dedicated memory, data requests

> can be re-ordered or even pre-fetched on speculation, and must be optimized for long bursts in alternating banks to fully utilize all available access time and minimize overhead.

Ex. 1007, 12:7–13.

Patent Owner argues that this contention fails because "Foster only describes adjusting the size of bursts based on the destination for the requests, while Claim 5 requires generating access requests based on the size of the requests." PO Resp. 42. Petitioner argues, however, that "both destination and size are taken into account to determine whether a request must be optimized." Pet. Reply 17. This position is supported by Dr. Subramanian's unrebutted testimony that

> a [person of ordinary skill in the art] would understand that an adjustment would only be necessary if the request seeks data in a specific memory *and* is the wrong size for that memory. A short burst, directed at shared memory, would not need further optimization. But if a request to shared memory is too long of a burst, it must be optimized. Thus a [person of ordinary skill in the art] would understand this to be an adjustment "based on the size of the requests for blocks of pixels."

Ex. 1016 ¶ 13. We credit this testimony because it is consistent with Foster's disclosure that data requests have to be compliant with the destination memory such that the size of the request is considered to make sure that the size is appropriate for the destination memory. Ex. 1007, 12:7–13. Thus, in Foster, the size of the destination memory is taken into account in relation to the size of the request, and, therefore, we find that Foster discloses generating access requests based on the sizes of the requests for blocks of pixels.

Patent Owner also argues the following:

> Petitioner provides no evidence that Foster discloses using ***the size of the block of pixel*** in generating its alleged access requests.

> Petitioner only argues that the sizes of the alleged access requests are adjusted if the alleged access requests are "too long," which would be using ***the size of the access request*** in generating the alleged access requests. Even if this were true, it is not what claim 5 requires, *i.e.*, it is not using ***the size of the block of pixel*** as a basis for generating access requests.

Sur-reply 12–13. We disagree with Patent Owner's reading of the claim. Claim 5 recites "wherein the logic generates the access requests based on the list of addresses and *based on sizes of each of the requests for blocks of pixels* from the motion prediction processing unit" (emphasis added). Although the size of the requested block of pixels may influence or even dictate the size of the request, the claim does not recite using the size of the block of pixels but, rather, recites using the sizes of the *requests* for the blocks of pixels.

Patent Owner also argues that "Petitioner does not identify logic that generates '***the*** access requests based on ***the*** list of addresses,'" as recited in claim 5. PO Resp. 39 (citing Ex. 2005 ¶ 59). We disagree because Foster discloses generating "data requests" (Ex. 1007, 12:7–13), as discussed above, and Petitioner relies on this to show that Foster teaches the recited "logic." Pet. 39–40.

For the reasons discussed above, we are persuaded by Petitioner's contentions and evidence, and we find that Foster teaches the subject matter recited in claim 5. Therefore, Petitioner has proven by a preponderance of the evidence that claim 5 of the '752 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Foster.

5. Claim 7

Claim 7 recites, "The memory access unit of claim 1, wherein the addresses are non-contiguous." Petitioner cites the following disclosure of Foster:

> The dedicated memory requests are preferably sent through a specialized/reordering request dispatcher 50 in accordance with this invention. Dispatcher 50 includes a lookahead/actual request mapper 51 where actual requests are mapped to previously generated speculative or lookahead requests to ensure that an actual request is not dispatched which may already have been executed as a lookahead request.

Ex. 1007, 8:19–26, *quoted in* Pet. 43. Petitioner argues that, "[b]ecause certain access requests are removed, this cache miss/hit event makes the addresses sent to the memory controller 24 'non-contiguous.'" Pet. 43 (citing Ex. 1003 ¶ 108). Patent Owner does not dispute Petitioner's contentions as to claim 7. *See generally* PO Resp.

We are persuaded by Petitioner's contentions, and we find that Foster teaches that "the addresses are non-contiguous." Thus, we determine that Petitioner has proven by a preponderance of the evidence that claim 7 of the '752 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Foster.

6. Claim 8

Claim 8 recites, "The memory access unit of claim 1, wherein the memory access unit receives data stored at the addresses in the memory from the lists of addresses in the memory over said link." Petitioner argues that "Foster's memory access unit 28 receives data from the dedicated memory via the dedicated bus 22," thereby teaching the subject matter of

claim 8. Pet. 47–48 (citing Ex. 1007, 5:6–8, 6:16–18, Fig. 3; Ex. 1003 ¶¶ 115–116).

Patent Owner argues Petitioner's contentions fail for two reasons. PO Resp. 49–51. First, Patent Owner argues that Figure 3 shows a data path between memory 26 and HDTV video decoder 14' and that Petitioner "fails to establish that any data going from dedicated memory 26 goes to Foster's MAU, memory interface 28." PO Resp. 49–50 (citing Ex. 2005 ¶ 72). We disagree because Foster discloses that, in Figure 3, "an HDTV video decoder 14' includes the memory interface 28 in accordance with the invention for accessing both dedicated memory 26 and shared memory 20." Ex. 1007, 6:49–52, *quoted in* Reply 24–25. Thus, Foster expressly states that memory interface 28 accesses the memory.

Second, Patent Owner argues that Petitioner fails to show that the data path in Figure 3 teaches "said link" in claim 8, which refers back to "a link to a memory controller" in claim 1. PO Resp. 50–51 (citing Ex. 2005 ¶ 73). According to Patent Owner, "[w]hile Figure 2 shows a memory controller, Figure 3's operational data paths do[] not go through a memory controller." PO Resp. 50 (citing Ex. 2005 ¶ 73). We disagree. Although Figure 3 does not illustrate a memory controller, Foster explains that "FIG.3 depicts the operational data paths shown in FIGS. 1 & 2." Ex. 1007, 6:48–49, *quoted in* Reply 25. Patent Owner's arguments ignore that Foster presents Figure 3 in the context of Figures 1 and 2, which both depict a memory controller through which the memory interface accesses the memory. Further, Foster explains that "the depicted data buses in practice may each comprise an associated read data bus and write data bus." Ex. 1007, 6:16–18, *quoted in* Pet. 47–48. Dr. Subramanian testifies that "data is both sent and received by

the memory interface via the dedicated bus 22." Ex. 1003 ¶ 116. We credit this testimony because it is consistent with Foster's disclosure that the memory interface accesses the memory via a memory controller and, therefore, over the bus that connects the memory interface to the memory controller. *See* Ex. 1007, 6:49–52.

In its Sur-reply, Patent Owner argues that Petitioner set forth improper reply arguments. Sur-reply 17–18, 20–21. First, Patent Owner argues that Petitioner relies on inherency for the first time in reply by arguing that "the dedicated bus 22 *must be* used for both sending requests and receiving the resulting data." Sur-reply 17 (quoting Reply 24). Notwithstanding Petitioner's use of "must," we do not view Petitioner's argument as relying on inherency. Rather, in context, we understand Petitioner's argument to be that Foster expressly discloses that the received data travel over dedicated bus 22 because that is the only path Foster discloses. *See* Reply 24. In any event, we find Foster teaches the claimed subject matter, and we do not rely on inherency.

Second, Patent Owner argues that, "for the first time in their Reply, Petitioner is arguing that Figures 1 and 2 'independently' disclose Claim 8's limitations." Sur-reply 21 (citing Reply 25). We do not rely on Figures 1 and 2 independent of Figure 3 because, as discussed above, Foster presents Figure 3 in the context of Figures 1 and 2. Ex. 1007, 6:48–49. Thus, Patent Owner's concern is moot.

Based on the foregoing, we are persuaded by Petitioner's contentions, and we find that Foster teaches that "the memory access unit receives data stored at the addresses in the memory from the lists of addresses in the memory over said link" and that Petitioner has proven by a preponderance of

the evidence that claim 8 of the '752 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over the teachings of Foster.

E. Obviousness over the Combination of Foster and Sih

Petitioner also argues that claims 1, 2, 5, 7, and 8 are unpatentable as obvious over the combined teachings of Foster and Sih. Pet. 17–48.

1. Sih

Like Foster, Sih discloses memory access in the context of video coding. Ex. 1005, code (57). Sih discloses "issu[ing] VDMA controller 26 access commands specifying multidimensional blocks of video data." Ex. 1005 ¶ 33. Sih further discloses that, "[i]n response to a command from DSP 28, for example, VDMA controller 26 may copy one or more blocks of video data from video memory 15 to motion estimation unit 24." Ex. 1005 ¶ 33.

2. Claims 1, 2, 7, and 8

For claim 1, Petitioner relies on Sih only to show access requests that include a list of more than one address under a construction of the claim Petitioner proposed in the Petition. Pet. 25–27. As discussed in § II.B above addressing claim construction, Petitioner no longer advocates this claim interpretation in this case, and, as discussed above in § II.D.2, Patent Owner does not dispute that Foster teaches "lists of addresses," and we find Foster teaches this subject matter. Thus, our discussion of claim 1 in § II.D.2 of obviousness based on Foster alone resolves all of the parties' disputes for that claim.

For dependent claim 2, Petitioner states that it "did not rely on Sih . . . for the features recited in claim 2." Reply 16.

For dependent claim 7, Petitioner relies on Sih in the alternative to show non-contiguous addresses, but Patent Owner does not dispute that Foster teaches this subject matter, and we find Foster teaches this subject matter. *See* § II.D.5 above.

For dependent claim 8, Petitioner does not rely on Sih. Pet. 47–48.

Because we determine Petitioner has demonstrated unpatentability of claims 1, 2, 7, and 8 based on Foster alone and because, for claims 1, 2, 7, and 8, Petitioner does not rely on Sih for any teaching that Patent Owner contends is missing from Foster, we decline to address Petitioner's additional arguments of unpatentability for claims 1, 2, 7, and 8 based on the combination of Foster and Sih. 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d).").

3. Claim 5

As discussed above in § II.D.4, we conclude the subject matter of claim 5 would have been obvious over the teachings of Foster alone based on the arguments and evidence presented. Petitioner also asserts that the subject matter of claim 5 would have been obvious based on the combined teachings of Foster and Sih, arguing that Sih discloses generating access requests based on sizes of the requests. Pet. 40–42. Because of the disputes between the parties as to Foster's teachings in relation to claim 5 (*see* § II.D.4 above), we address Petitioner's contentions for claim 5 based on Foster in combination with Sih.

Petitioner argues that Sih's disclosure of access commands for multidimensional blocks of data teaches generating access requests based on sizes of the requests. Pet. 40–42 (citing Ex. 1005 ¶¶ 24, 33, 44; Ex. 1003 ¶¶ 101–104). Sih discloses that "processor 30 and DSP 28 issue VDMA controller access commands specifying multidimensional blocks of video data, which VDMA controller 26 translates into single dimensional storage addresses." Ex. 1005 ¶ 33. Sih further discloses that the access commands "include a set of parameters specifying the block to transfer," including video block width and video block length, and that "the video block width and video block length are used to define the dimensions of the desired rectangular block in bytes." Ex. 1005 ¶¶ 35–37, 44.

Patent Owner counters that "[s]imply because the size information is provided as input does not mean that the information is used as a basis for generating the access requests." PO Resp. 43 (citing Ex. 2005 ¶ 64). We do not agree with this reading of Sih because, as Dr. Subramanian credibly testifies, "Sih describes eight parameters included in each access command, and specifically states that it is the length and width that are 'used to define the dimension of the desired rectangular block in bytes.'" Ex. 1016 ¶ 14. Thus, we agree with Petitioner and find that Sih teaches generating access requests based on sizes of the requests. *See* Pet. 40–42.

Petitioner contends a person of ordinary skill in the art would have understood that Sih's approach of "us[ing] a single memory access request to access multiple blocks of data" would be preferable to Foster's approach of "generating an individual request for each address within a single block." Pet. 29 (citing Ex. 1003 ¶ 72). Petitioner contends that "[a] person of ordinary skill would therefore have modified each of Foster's memory

access requests to be directed to two or more addresses (or every address needed for a single block), in order to improve memory access efficiency in the video decoding function common to both Foster and Sih." Pet. 29 (citing Ex. 1003 ¶ 73).

Patent Owner argues that Petitioner's characterization of Sih's disclosure is incorrect and that Sih actually discloses that each request is for a single row of memory or a single word of memory. PO Resp. 27–28 (citing Ex. 2005 ¶¶ 43–44; Ex. 1005 ¶¶ 33, 34, 44). We disagree. As Petitioner correctly points out (Reply 9–10), Sih's disclosure of reading a "single row of memory" is referring to "conventional DMA controllers," which Sih expressly contrasts with the operation of its VDMA controller. Ex. 1005 ¶ 33 ("Unlike conventional DMA controllers that read a single row of memory at a time, VDMA controller 26 fetches multidimensional video blocks of a frame without having to be reprogrammed between rows."). Sih further discloses the following:

> The command [specifying a multidimensional block of video data] may, for example, specify a number of rows and a number of columns for the block of video data, and a jump parameter indicating a number of storage units between each row of the video block. In this manner, the VDMA controller is capable of fetching an entire block of video data having multiple non-contiguous rows in response to a single direct memory access (DMA) command.

Ex. 1005 ¶ 6, *quoted in* Reply 9–10.

Patent Owner also argues that the proposed combination would not necessarily result in improved efficiency, citing a disclosure in Foster of how to improve efficiency, and, therefore, that Petitioner's rationale to combine is insufficient. PO Resp. 28–29 (citing Ex. 2005 ¶ 44 (citing Ex. 1007, 9:65–10:2, 10:11–65)). Even assuming Foster discloses some ways to

improve efficiency, Petitioner's rationale to combine is persuasive and supported by Sih's disclosed improvement of not "having to perform the high number of address calculations that is typically required to access video data due to the non-sequential manner in which video data is typically stored." Ex. 1005 ¶ 21, *quoted in* Pet. 28; *see also* Ex. 1005 ¶ 6 ("Accordingly, the microprocessor can access a block of video data with a reduced number of address calculations."). Thus, we credit Dr. Subramanian's testimony that "Sih explains that its invention increases the efficiency of memory access for a video encoding or decoding function" (Ex. 1003 ¶ 71) because it is consistent with Sih's own disclosure. We find that a person of ordinary skill in the art would have been motivated to combine Sih's disclosure of using one request to access multiple blocks of data with the teachings of Foster.

Patent Owner also argues that Petitioner has not provided any evidence that a person of ordinary skill in the art would have had a reasonable expectation of success in combining the teachings of Foster and Sih and that the proposed combination "would potential[ly] destroy the alternating bank nature of the requests" in Foster. PO Resp. 29–30 (citing Ex. 2005 ¶ 45), 45–46 (citing Ex. 2005 ¶ 66). For this assertion Patent Owner relies on the following testimony from Dr. Wolf:

> Foster is specifically designed to allegedly transmit single address requests to alternating memory banks. Any modification to that addressing scheme would potential[ly] destroy the alternating bank nature of the requests. Thus, a [person of ordinary skill in the art] would not have a reasonable expectation of success in making the modification that Petitioner proposed.

Ex. 2005 ¶ 45; *see also* Ex. 2005 ¶ 66 (same testimony).

Dr. Wolf does not explain why applying Sih's teachings would "destroy" this aspect of Foster's disclosure, and we do not see how it would. Foster discloses that "a characteristic of physical memory chips is that sequential accesses to the same memory bank are slower than sequential accesses to alternate banks." Ex. 1007, 10:10–12. Foster discloses requesting data "in alternating banks to fully utilize all available access time and minimize overhead." Ex. 1007, 12:10–13. Thus, Foster's disclosure of accessing alternating banks simply takes advantage of a known characteristic of physical memory. Patent Owner's and Dr. Wolf's position suggests that a person of ordinary skill in the art (a person with a bachelor's degree in electrical engineering, computer science, or a similar discipline, with two years of experience working with memory access and digital video processing) would not be capable of working within the technical constraints of known physical memory chips. We do not agree with this. Rather, we credit Dr. Subramanian's testimony that a person of ordinary skill in the art "would understand that it would be straightforward to perform Foster's reordering with requests that each include multiple addresses." Ex. 1016 ¶ 8 (citing Ex. 1003 ¶¶ 72–73).

Based on the foregoing, we find that the combination of Foster and Sih teaches the subject matter recited in claim 5 and that a person of ordinary skill in the art would have been motivated to combine the references and would have had a reasonable expectation of success in doing so. Accordingly, we conclude that the subject matter of claim 5 would have been obvious based on the combined teachings of Foster and Sih.

F. Obviousness over the Combination of Foster and Rovati

In view of our determination that claims 1, 2, 5, 7, and 8 are unpatentable as discussed above, we need not address Petitioner's additional arguments of unpatentability based on Foster in combination with Rovati. 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d).").

III. CONCLUSION[8]

For the reasons discussed above, we determine Petitioner has proven, by a preponderance of the evidence, that the challenged claims are unpatentable, as summarized in the following table:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 5, 7, 8	103(a)	Foster	1, 2, 5, 7, 8	
1, 2, 5, 7, 8	103(a)	Foster, Sih[9]	5	
1, 2, 5, 7, 8	103(a)	Foster, Rovati[10]		
Overall Outcome			1, 2, 5, 7, 8	

[8] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[9] As explained above, because we determine that the challenged claims are unpatentable based on Foster alone, we decline to address this ground for claims 1, 2, 7, and 8.

[10] As explained above, because we determine that the challenged claims are unpatentable based on Foster alone, we decline to address this ground.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1, 2, 5, 7, and 8 of the ’752 patent have been shown to be unpatentable; and

FURTHERED ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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CERTIFICATE OF SERVICE

Per 37 C.F.R. § 90.2(a)(1), on December 29, 2020 the foregoing **PATENT OWNER'S NOTICE OF APPEAL** was filed electronically with the Board in accordance with 37 C.F.R. § 42.6(b)(1), and mailed to the Director via Priority Mail Express in accordance with 37 C.F.R. §§ 1.10 and 104.2 at the following address:

Director of the U.S. Patent & Trademark Office
c/o Office of the General Counsel
P.O. Box 1450
Alexandria, VA 22313-1450

Per 37 C.F.R. § 90.2(a)(2), Fed. R. App. P. 15 and Fed. Cir. Rules 15, 24 and 52 on December 29, 2020 the foregoing notice of appeal was electronically filed with the Court of Appeals for the Federal Circuit via CM/ECF with appropriate fees paid through pay.gov.

Per 37 C.F.R. § 42.6(e) on December 29, 2020 the foregoing notice of appeal was served to the following email address:

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Dated: December 29, 2020

/John Caracappa/
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