IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC,	**Civil Action No. 11-CV-1025-SLR**
Plaintiffs,	**JURY TRIAL DEMANDED**
v.	
NIKON CORPORATION, NIKON AMERICAS INC., and NIKON INC.,	
Defendants.	

SECOND AMENDED COMPLAINT

Plaintiffs Intellectual Ventures I LLC ("Intellectual Ventures I") and Intellectual Ventures II LLC ("Intellectual Ventures II") (collectively, "Intellectual Ventures I and II") for their Complaint against Defendants Nikon Corporation, Nikon Americas Inc., and Nikon Inc. (collectively, "Nikon"), hereby allege as follows:

PARTIES

1. Intellectual Ventures I is a Delaware limited liability company with its principal place of business located in Bellevue, Washington.

2. Intellectual Ventures II is a Delaware limited liability company with its principal place of business located in Bellevue, Washington.

3. Defendant Nikon Corporation is a corporation organized under the laws of Japan having a principal place of business at Shin-Yurakucho Bldg., 12-1, Yurakucho 1-chome, Chiyoda-ku, Tokyo, 100-8331, Japan.

4. Defendant Nikon Americas Inc. is a corporation organized under the laws of Delaware, having a principal place of business at 1300 Walt Whitman Road, Melville, New

York, 11747-3064. Nikon Americas Inc. may be served with process through Corporation Service Company, 2711 Centerville Road, Suite 400, Wilmington, Delaware, 19808.

5. Defendant Nikon Inc. is a corporation organized under the laws of New York, having a principal place of business at 1300 Walt Whitman Road, Melville, New York, 11747-3064. Nikon Inc. may be served with process through the New York Department of State's office at One Commerce Plaza, 6th Floor, 99 Washington Avenue, Albany, NY 12231.

NATURE OF THE ACTION

6. This is a civil action for the infringement of United States Patent No. 5,712,870, United States Patent No. 6,121,960, United States Patent No. 6,221,686, United States Patent No. 6,754,195, United States Patent No. 6,977,944, United States Patent No. 6,979,587, United States Patent No. 7,365,298 and United States Reissued Patent No. RE43,700 (collectively, the "Patents-in-Suit") under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq.*

JURISDICTION AND VENUE

7. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patent laws of the United States, including 35 U.S.C. § 271 *et seq*.

8. This Court has personal jurisdiction over Defendants because Defendants have committed acts of infringement in violation of 35 U.S.C. § 271 and have placed infringing products into the stream of commerce with the knowledge and/or understanding that such products are used and sold in this District. Defendant Nikon Corporation maintains a website in English that is available in the United States offering information and user manuals concerning infringing products, including but not limited to, Coolpix AW100, AW110, L610, L820, P310, P330, P510, P520, P7700, S800, S4100, S5200, S6100, S6300, S6400, S6500, S9050, S9200,

S9300, S9400, and S9500 cameras, Nikon's D3s, D4, D600, D3100, D3200 cameras, and WU-1a/b Wireless Mobile Adapters. These acts have caused and continue to cause injury to Intellectual Ventures I and II within the District. Defendants derive substantial revenue from the sale of infringing products distributed within the District, and/or expect or should reasonably expect their actions to have consequences within the District, and derive substantial revenue from interstate and international commerce. In addition, Defendants knowingly induce infringement within this District by contracting with others to market and sell infringing products with the knowledge and intent to facilitate infringing sales of the products by others within this District and by creating and/or disseminating instructions and other materials for the products with like mind and intent.

9. Venue is proper in this judicial district as to Defendants pursuant to 28 U.S.C. §§ 1391 and 1400(b).

THE PATENTS-IN-SUIT

10. Paragraphs 1-9 are reincorporated by reference as if fully set forth herein.

11. On September 19, 2000, United States Patent No. 6,121,960 ("the '960 Patent"), titled "Touch Screen Systems And Methods," was duly and lawfully issued by the United States Patent and Trademark Office ("PTO"). The '960 Patent is attached hereto as Exhibit A.

12. Intellectual Ventures II owns the '960 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

13. On October 2, 2012, United States Reissued Patent No. RE43,700 ("the RE'700 Patent"), titled "Virtual Reality Camera," was duly and lawfully issued by the PTO. The RE'700 Patent is attached hereto as Exhibit B.

14. Intellectual Ventures I owns the RE'700 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

15. On April 24, 2001, United States Patent No. 6,221,686 ("the '686 Patent"), titled "Method Of Making A Semiconductor Image Sensor," was duly and lawfully issued by the PTO. The '686 Patent is attached hereto as Exhibit C.

16. Intellectual Ventures II owns the '686 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

17. On December 27, 2005, United States Patent No. 6,979,587 ("the '587 Patent"), titled "Image Sensor And Method For Fabricating The Same," was duly and lawfully issued by the PTO. The '587 Patent is attached hereto as Exhibit D.

18. Intellectual Ventures II owns the '587 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

19. On April 29, 2008, United States Patent No. 7,365,298 ("the '298 Patent"), titled "Image Sensor And Method For Manufacturing The Same," was duly and lawfully issued by the PTO. The'298 Patent is attached hereto as Exhibit E.

20. Intellectual Ventures II owns the '298 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

21. On June 22, 2004, United States Patent No. 6,754,195 ("the '195 Patent"), titled "Wireless Communication System Configured To Communicate Using A Mixed Waveform Configuration," was duly and lawfully issued by the PTO. The '195 Patent is attached hereto as Exhibit F.

22. Intellectual Ventures I owns the '195 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

23. On January 27, 1998, United States Patent No. 5,712,870 ("the '870 Patent"), titled "Packet Header Generation And Detection Circuitry," was duly and lawfully issued by the PTO. The '870 Patent is attached hereto as Exhibit G.

24. Intellectual Ventures I owns the '870 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

25. On December 20, 2005, United States Patent No. 6,977,944 ("the '944 Patent"), titled "Transmission Protection For Communications Networks Having Stations Operating With Different Modulation Formats," was duly and lawfully issued by the PTO. The '944 Patent is attached hereto as Exhibit H.

26. Intellectual Ventures I owns the '944 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

FACTUAL BACKGROUND

27. Intellectual Ventures Management, LLC ("Intellectual Ventures") was founded in 2000. Since its founding, Intellectual Ventures has been deeply involved in the business of invention. Intellectual Ventures creates inventions and files patent applications for those inventions; collaborates with others to develop and patent inventions; and acquires and licenses patents from individual inventors, universities, and other institutions. A significant aspect of Intellectual Ventures' business is managing the plaintiffs in this case, Plaintiffs Intellectual Ventures I and Intellectual Ventures II.

28. Intellectual Ventures' business includes purchasing important inventions from individual inventors and institutions and then licensing the inventions to those who need them. Through this business, Intellectual Ventures allows inventors to reap a financial reward from their innovations, a frequently difficult task for individual inventors. To date, Intellectual

Ventures has built a portfolio of more than 35,000 assets and more than 3,000 of those patents and patent applications are the result of Intellectual Ventures' own invention efforts, both in-house and with Intellectual Ventures' inventor network. Intellectual Ventures has paid individual inventors more than $400 million for their inventions. Intellectual Ventures, in turn, has earned more than $2 billion by licensing these patents to some of the world's most innovative and successful technology companies who continue to use them to make computer equipment, software, semiconductor devices, consumer products, and a host of other products.

29. Intellectual Ventures also develops its own inventions. Intellectual Ventures has a staff of scientists and engineers who develop ideas in a broad range of fields, including agriculture, computer hardware, life sciences, medical devices, semiconductors, and software. Intellectual Ventures has invested millions of dollars developing such ideas and has filed hundreds of patent applications on its inventions every year, making it one of the top patent filers in the world. Intellectual Ventures also has invested in laboratory facilities to assist with the development and testing of new ideas.

30. Intellectual Ventures also develops inventions by collaborating with inventors and research institutions around the world. For example, Intellectual Ventures has developed inventions by selecting a technical challenge, requesting proposals for inventions to solve the challenge from inventors and institutions, selecting the most promising ideas, rewarding the inventors and institutions for their contributions, and filing patent applications on the ideas. Intellectual Ventures has invested millions of dollars in this way and has created a network of more than 3000 inventors worldwide.

31. Nikon is a global company that designs, manufactures, and/or markets consumer electronics, including digital single-lens reflex ("DSLR") cameras, compact digital cameras, and imaging software.

32. Beginning in 2008, Intellectual Ventures approached Nikon about taking a license to Intellectual Ventures' patents. Over the next several months, Intellectual Ventures attempted to meet and negotiate license terms with Nikon; however, Nikon declined to meet with Intellectual Ventures. In 2011, Intellectual Ventures again attempted to contact Nikon and negotiate license terms. However, Intellectual Ventures' attempts were unsuccessful and discussions stalled. Despite Intellectual Ventures' good-faith efforts to negotiate a business solution, Nikon has failed and refused to license Intellectual Ventures' patents on reasonable terms, and continues to use those inventions without permission.

COUNT I

(Nikon's Infringement of the '960 Patent)

33. Paragraphs 1-32 are incorporated by reference as if fully restated herein.

34. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the '960 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Nikon's Coolpix S4100 and S6100 cameras) without authority and in violation of 35 U.S.C. § 271.

35. Nikon has had knowledge of and notice of the '960 Patent and its infringement since at least October 26, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Nikon of the filing of the Complaint on October 26,

2011. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’960 patent.

36. Intellectual Ventures II has suffered damage as a result of Nikon’s infringement of the ’960 Patent.

COUNT II

(Nikon’s Infringement of the ’870 Patent)

37. Paragraphs 1-36 are incorporated by reference as if fully restated herein.

38. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others includes its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’870 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital camera and adapters capable of wireless file transfer (including but not limited to Coolpix S9500 equipped with WiFi connectivity and Nikon’s D-3200 or D600 digital cameras in combination with the WU-1a/b Wireless Mobile Adapter) without authority and in violation of 35 U.S.C. § 271.

39. Nikon has had knowledge of and notice of the ’870 Patent and its infringement since at least the filing of this Second Amended Complaint. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’870 patent.

40. Intellectual Ventures I has suffered damage as a result of Nikon’s infringement of the ’870 Patent.

COUNT III

(Nikon’s Infringement of the ’686 Patent)

41. Paragraphs 1-40 are incorporated by reference as if fully restated herein.

42. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’686 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Nikon’s D3s DSLR camera) without authority and in violation of 35 U.S.C. § 271.

43. Nikon has had knowledge of and notice of the ’686 Patent and its infringement since at least October 26, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Nikon of the filing of the Complaint on October 26, 2011. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’686 patent.

44. Intellectual Ventures II has suffered damage as a result of Nikon’s infringement of the ’686 Patent.

COUNT IV

(Nikon’s Infringement of the ’587 Patent)

45. Paragraphs 1-44 are incorporated by reference as if fully restated herein.

46. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’587 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Nikon’s D3100 camera) without authority and in violation of 35 U.S.C. § 271.

47. Nikon has had knowledge of and notice of the ’587 Patent and its infringement since at least October 26, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Nikon of the filing of the Complaint on October 26,

2011. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’587 patent.

48. Intellectual Ventures II has suffered damage as a result of Nikon’s infringement of the ’587 Patent.

COUNT V

(Nikon’s Infringement of the ’195 Patent)

49. Paragraphs 1-48 are incorporated by reference as if fully restated herein.

50. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’195 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products containing Wi-Fi connectivity (including but not limited to Coolpix S9500 equipped with WiFi connectivity and Nikon’s D-3200 or D600 digital cameras in combination with the WU-1a/b Wireless Mobile Adapter) without authority and in violation of 35 U.S.C. § 271.

51. Nikon has had knowledge of and notice of the ’195 Patent and its infringement since at least the filing of this Second Amended Complaint. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’195 patent.

52. Intellectual Ventures I has suffered damage as a result of Nikon’s infringement of the ’195 Patent.

COUNT VI

(Nikon’s Infringement of the ’944 Patent)

53. Paragraphs 1-52 are incorporated by reference as if fully restated herein.

54. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’944 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products containing Wi-Fi connectivity (including but not limited to Coolpix S9500 equipped with WiFi connectivity and Nikon’s D-3200 or D600 digital cameras in combination with the WU-1a/b Wireless Mobile Adapter) without authority and in violation of 35 U.S.C. § 271.

55. Nikon has had knowledge of and notice of the ’944 Patent and its infringement since at least the filing of this Second Amended Complaint. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’944 patent.

56. Intellectual Ventures I has suffered damage as a result of Nikon’s infringement of the ’944 Patent.

COUNT VII

(Nikon’s Infringement of the ’298 Patent)

57. Paragraphs 1-56 are incorporated by reference as if fully restated herein.

58. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’298 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Nikon’s D4 camera) without authority and in violation of 35 U.S.C. § 271.

59. Nikon has had knowledge of and notice of the ’298 Patent and its infringement since at least the filing of this Second Amended Complaint. Nikon possessed, and continues to

possess, the specific intent to encourage others, including its customers, to infringe the ’298 patent.

60. Intellectual Ventures II has suffered damage as a result of Nikon’s infringement of the ’298 Patent.

COUNT VIII

(Nikon’s Infringement of the RE’700 Patent)

61. Paragraphs 1-60 are incorporated by reference as if fully restated herein.

62. Nikon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the RE’700 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Nikon’s cameras that include the “Easy Panorama” mode, such as the S9200, S9300, S9400, S9500, AW100, AW110, L610, L820, P310, P330, P510, P520, P7700, S800, S5200, S6300, S6400, S6500, and S9050 cameras) without authority and in violation of 35 U.S.C. § 271.

63. Nikon has had knowledge of and notice of the RE’700 Patent and its infringement since at least the filing of this Second Amended Complaint. Nikon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the RE’700 patent.

64. Intellectual Ventures I has suffered damage as a result of Nikon’s infringement of the RE’700 Patent.

PRAYER FOR RELIEF

WHEREFORE, Intellectual Ventures I and II respectfully request the following relief:

a) A judgment that Nikon has infringed the ’960 Patent;

b) A judgment that Nikon has infringe the RE’700 Patent;

c) A judgment that Nikon has infringed the ’686 Patent;

d) A judgment that Nikon has infringed the ’587 Patent;

e) A judgment that Nikon has infringed the ‘298 Patent;

f) A judgment that Nikon has infringed the ‘195 Patent;

g) A judgment that Nikon has infringed the ’870 Patent;

h) A judgment that Nikon has infringed the ’944 Patent;

i) A judgment that Intellectual Ventures I be awarded all appropriate damages under 35 U.S.C. § 284 for Nikon’s past infringement and any continuing or future infringement of the’195, ’870, RE’700 and ’944 Patents up until the date such judgment is entered, including pre and post judgment interest, costs, and disbursements as justified under 35 U.S.C. § 284 and, if necessary, to adequately compensate Intellectual Ventures I for Nikon’s infringement, an accounting:

a. that Intellectual Ventures I be awarded the attorney fees, costs, and expenses that it incurs in prosecuting this action; and

b. that Intellectual Ventures I be awarded such further relief at law or in equity as the Court deems just and proper.

j) A judgment that Intellectual Ventures II be awarded all appropriate damages under 35 U.S.C. § 284 for Nikon’s past infringement and any continuing or future infringement

of the ’960, ’686, ’298 and ’587 Patents up until the date such judgment is entered, including pre and post judgment interest, costs, and disbursements as justified under 35 U.S.C. § 284 and, if necessary, to adequately compensate Intellectual Ventures II for Nikon’s infringement, an accounting:

a. that Intellectual Ventures II be awarded the attorney fees, costs, and expenses that it incurs in prosecuting this action; and

b. that Intellectual Ventures II be awarded such further relief at law or in equity as the Court deems just and proper.

DEMAND FOR JURY TRIAL

Intellectual Ventures I and Intellectual Ventures II hereby demand trial by jury on all claims and issues so triable.

DATED: December __, 2013

Respectfully submitted,

FARNAN LLP

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Counsel for Plaintiffs

EXHIBIT A

US006121960A

United States Patent [19]

Carroll et al.

[11] Patent Number: 6,121,960

[45] Date of Patent: Sep. 19, 2000

[54] **TOUCH SCREEN SYSTEMS AND METHODS**

[75] Inventors: **David W. Carroll**; **James L. Carroll**; **Steven V. Case**, all of Northfield, Minn.

[73] Assignee: **ViA, Inc.**, Burnsville, Minn.

[21] Appl. No.: **08/919,527**

[22] Filed: **Aug. 28, 1997**

Related U.S. Application Data

[60] Provisional application No. 60/024,780, Aug. 28, 1996, provisional application No. 60/028,028, Oct. 9, 1996, and provisional application No. 60/036,195, Jan. 21, 1997.

[51] **Int. Cl.**[7] **G09G 5/00**

[52] **U.S. Cl.** **345/173**; 345/172; 345/169

[58] **Field of Search** 345/173, 172, 345/168, 169, 429, 113; 361/683

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,725,694	2/1988	Auer et al. .	
4,763,356	8/1988	Day, Jr. et al. .	
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5,379,057	1/1995	Clough et al. .	
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5,615,384	3/1997	Allard et al. .	
5,627,567	5/1997	Davidson .	
5,675,362	10/1997	Clough .	
5,798,907	8/1998	Janik	361/683
5,870,100	2/1999	DeFreitas	345/429

FOREIGN PATENT DOCUMENTS

2-155029	6/1990	Japan .

Primary Examiner—Steven J. Saras
Assistant Examiner—Alecia D. Nelson
Attorney, Agent, or Firm—Patterson, Thuente & Skaar, P.A.

[57] **ABSTRACT**

A screen peripheral system according to an embodiment of the invention includes a computing device for producing a main image and a touch-activated input device for generating and displaying a composite image visible to a user. The composite image simultaneously includes a representation of at least one key, for example a QWERTY keyboard, for activating an input function, and the main image provided by the computing device. The keyboard representation preferably is laid over the main image. According to one embodiment, the main image is an output image generated by an application being executed by the computing device. Other touch screen systems and methods are also disclosed.

30 Claims, 9 Drawing Sheets

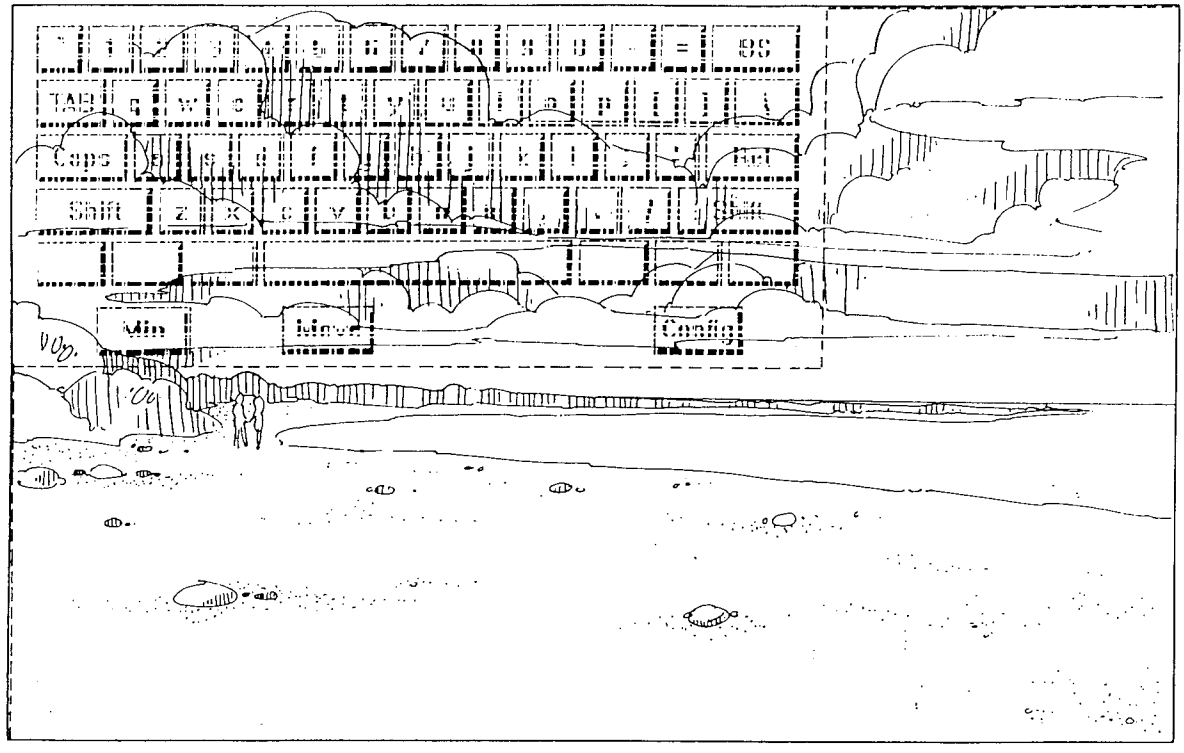
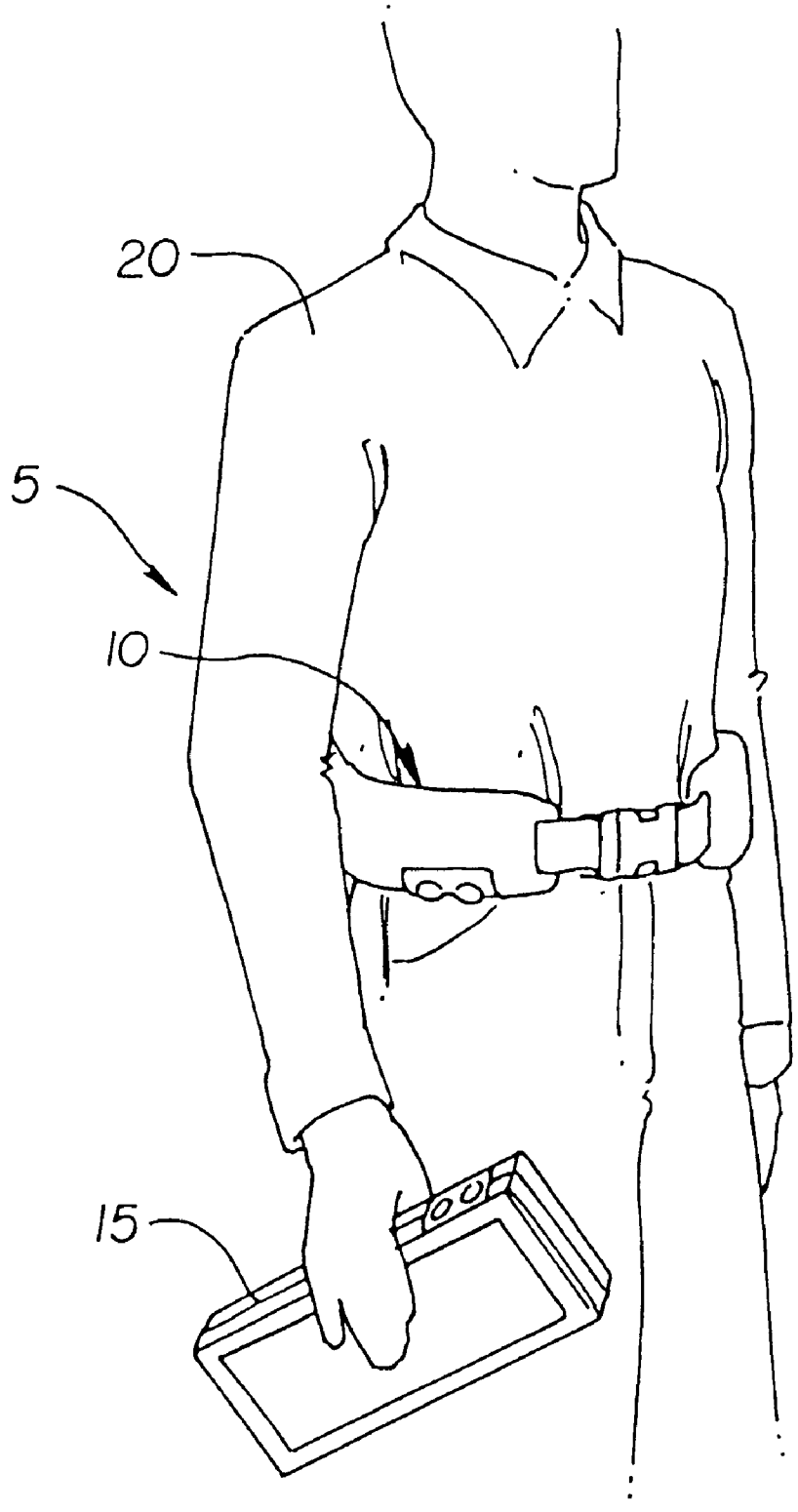


FIG. 1



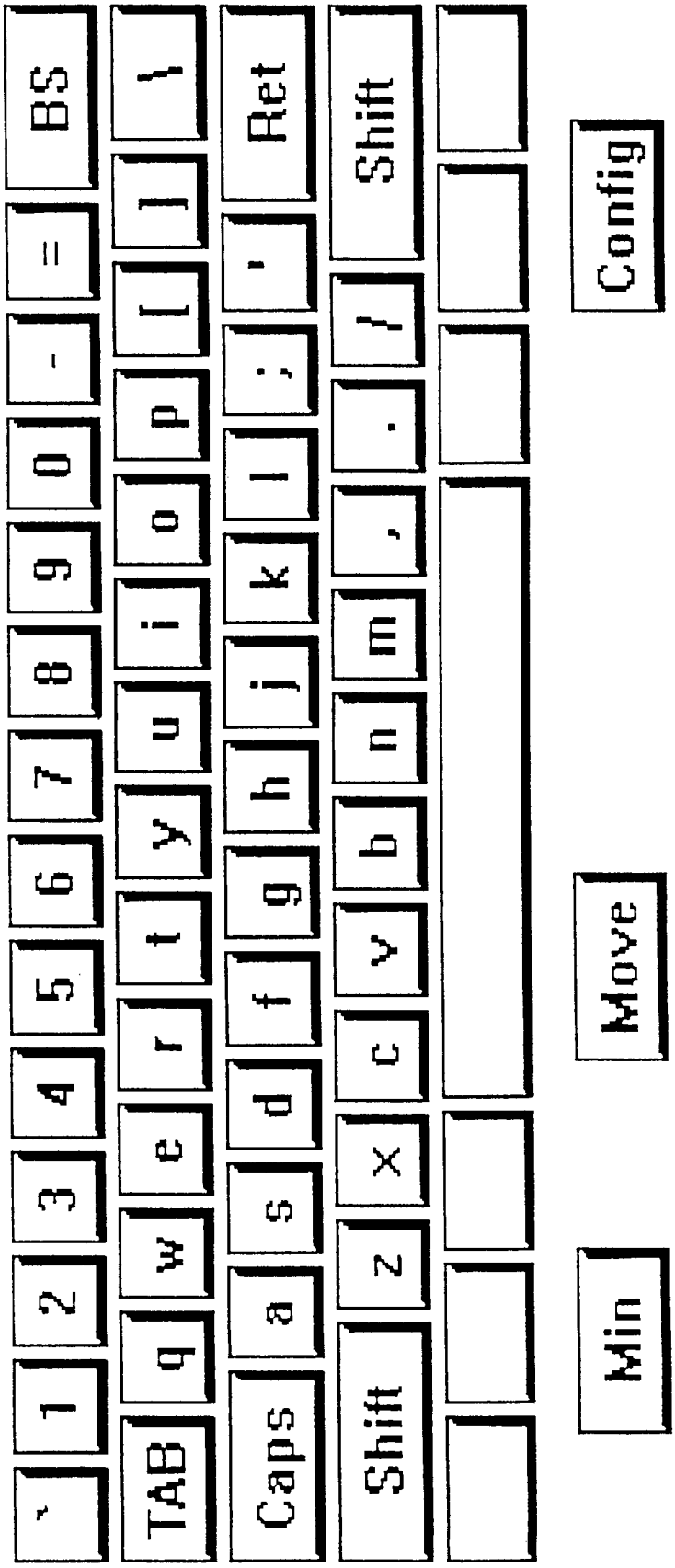

` 1 2 3 4 5 6 7 8 9 0 - = BS
TAB q w e r t y u i o p [ ] \
Caps a s d f g h j k l ; ' Ret
Shift z x c v b n m , . / Shift
Min
Move
Config

FIG. 2

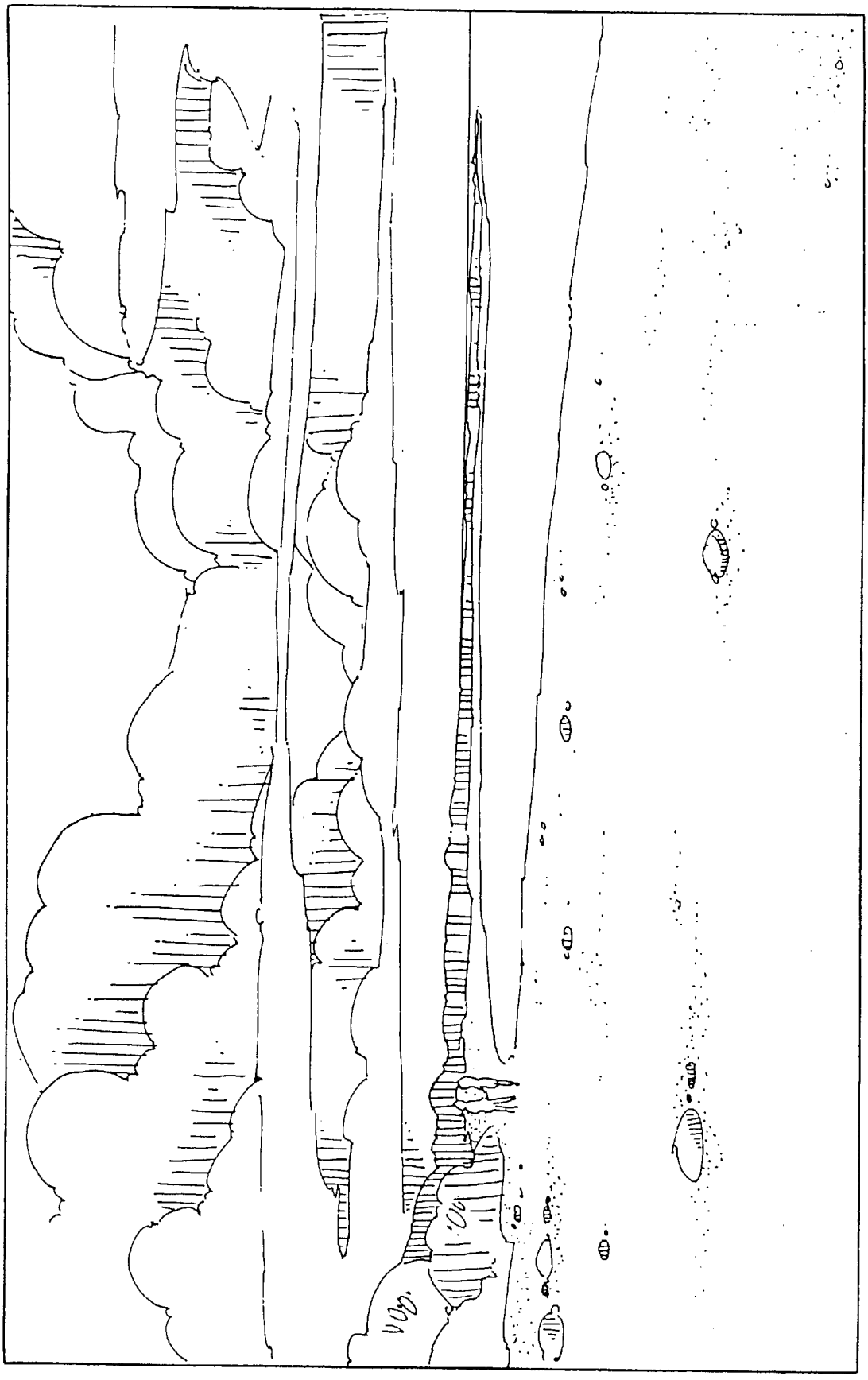


FIG. 3

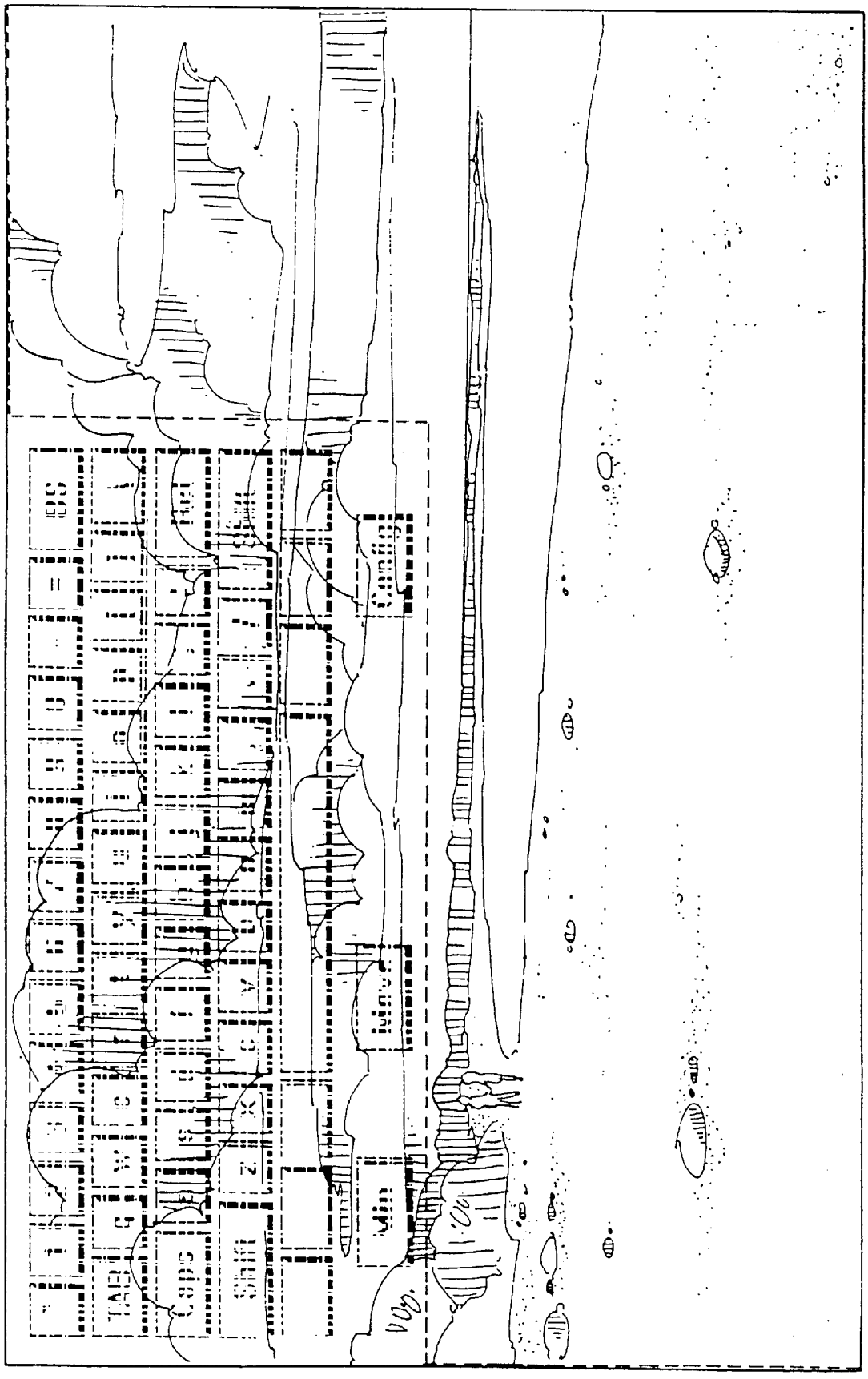


FIG. 4

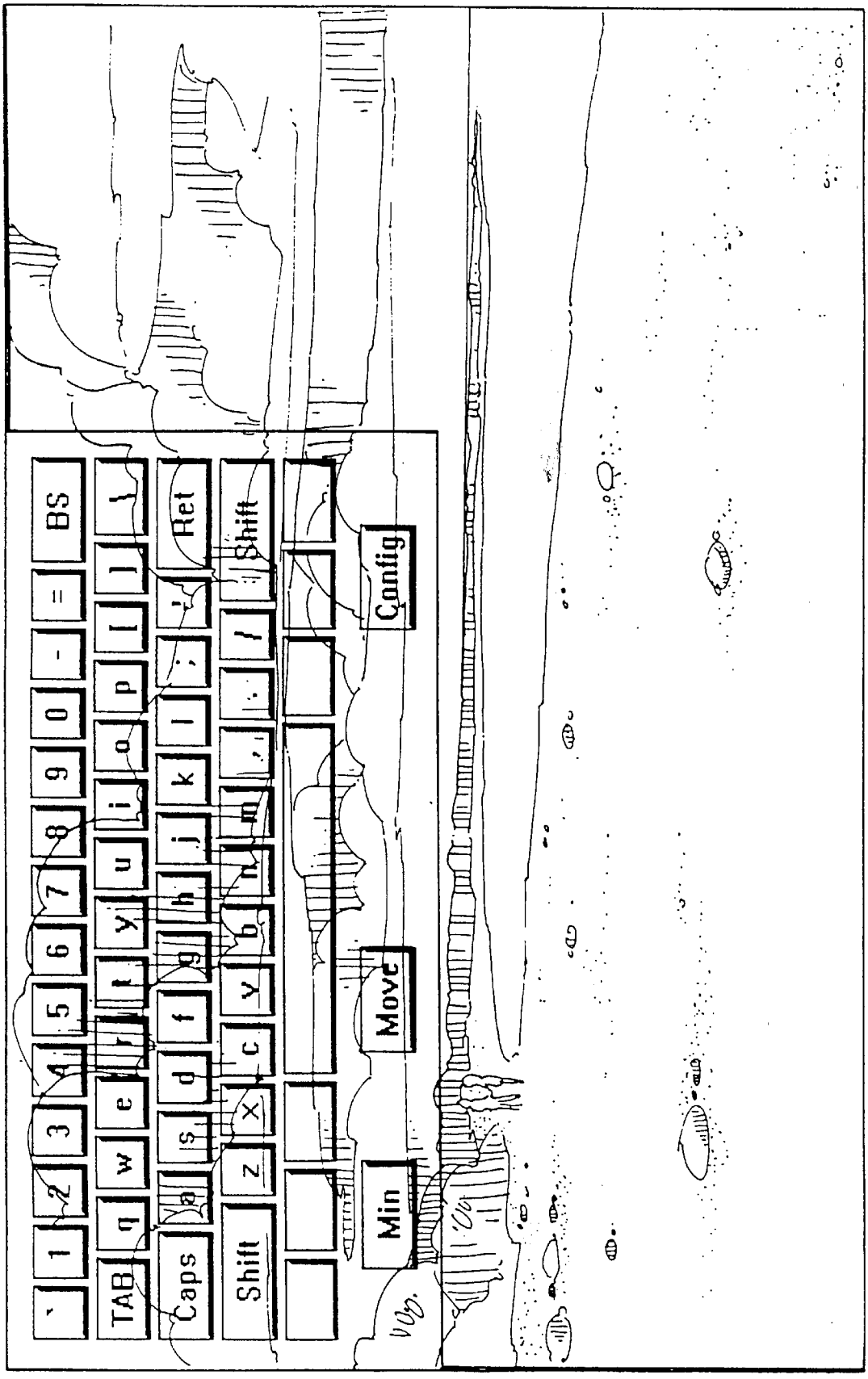


FIG. 5

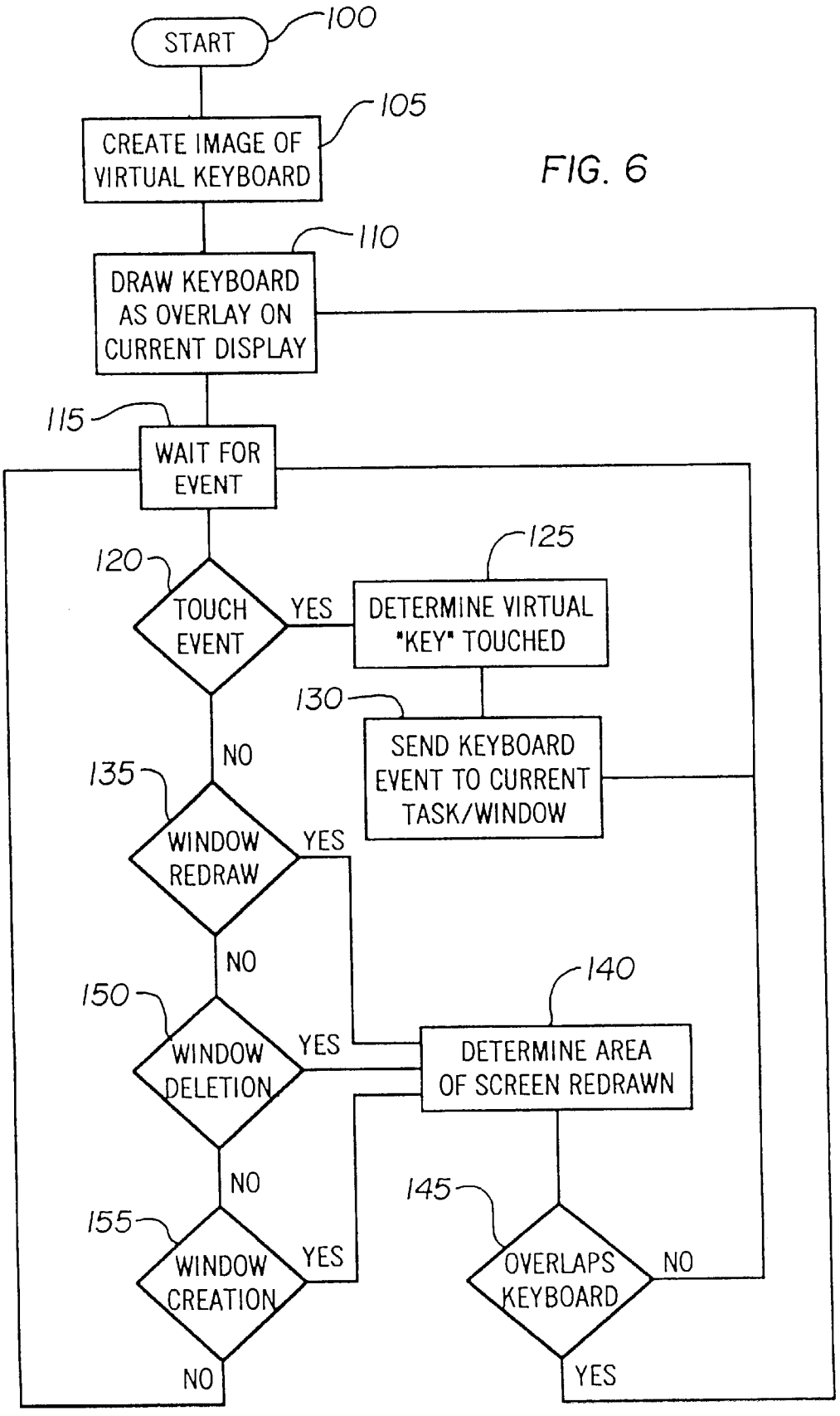

START
100
CREATE IMAGE OF VIRTUAL KEYBOARD
105
DRAW KEYBOARD AS OVERLAY ON CURRENT DISPLAY
110
WAIT FOR EVENT
115
TOUCH EVENT
120
YES
DETERMINE VIRTUAL "KEY" TOUCHED
125
SEND KEYBOARD EVENT TO CURRENT TASK/WINDOW
130
NO
WINDOW REDRAW
135
YES
NO
WINDOW DELETION
150
YES
DETERMINE AREA OF SCREEN REDRAWN
140
NO
WINDOW CREATION
155
YES
NO
OVERLAPS KEYBOARD
145
NO
YES

FIG. 6

FIG. 7

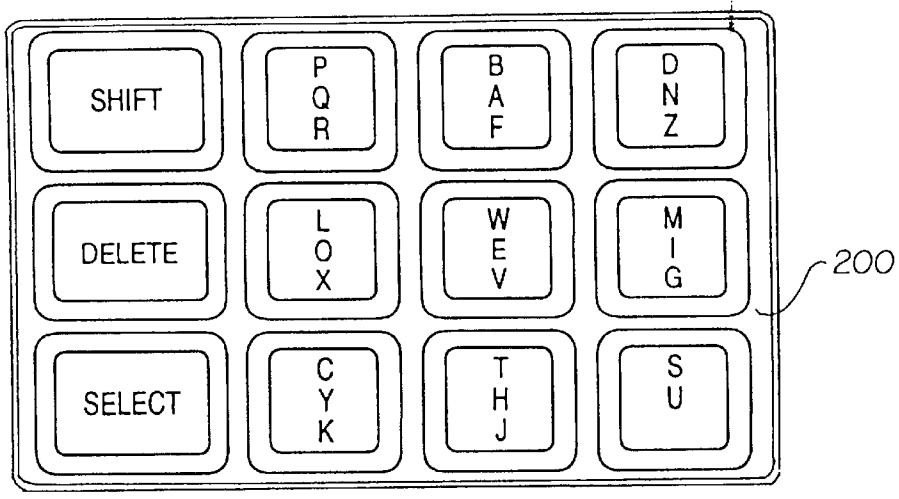

SHIFT
P Q R
B A F
D N Z
DELETE
L O X
W E V
M I G
SELECT
C Y K
T H J
S U
200

FIG. 8

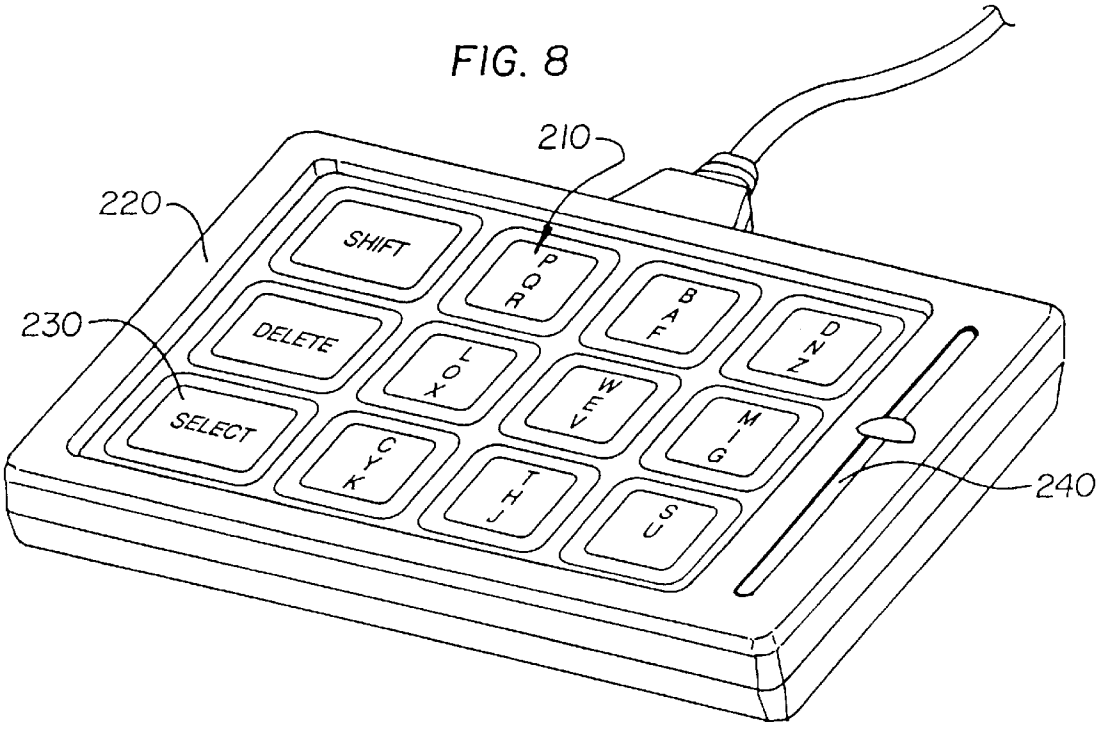

210
220
230
240
SHIFT
DELETE
SELECT

FIG. 9

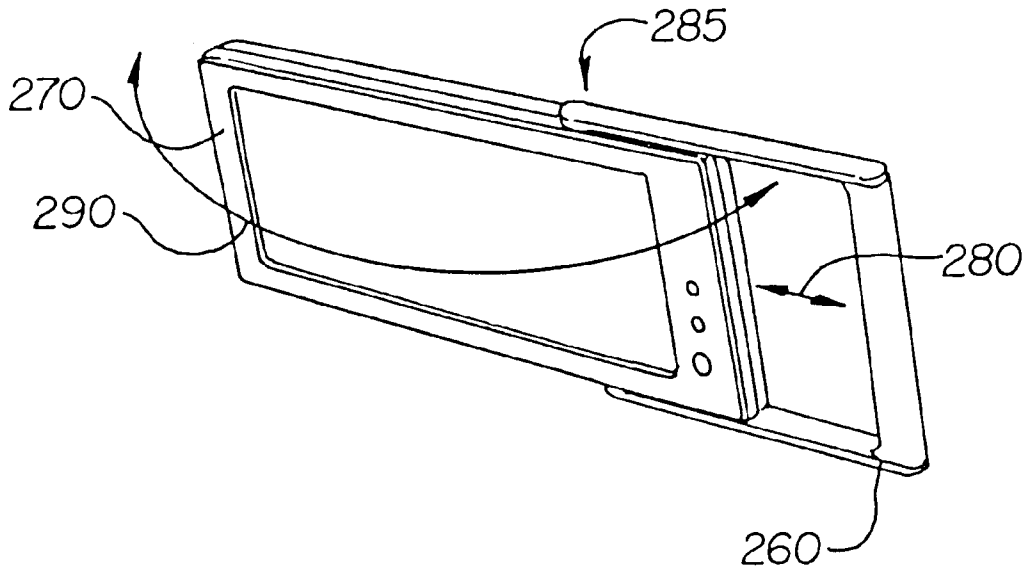


FIG. 10

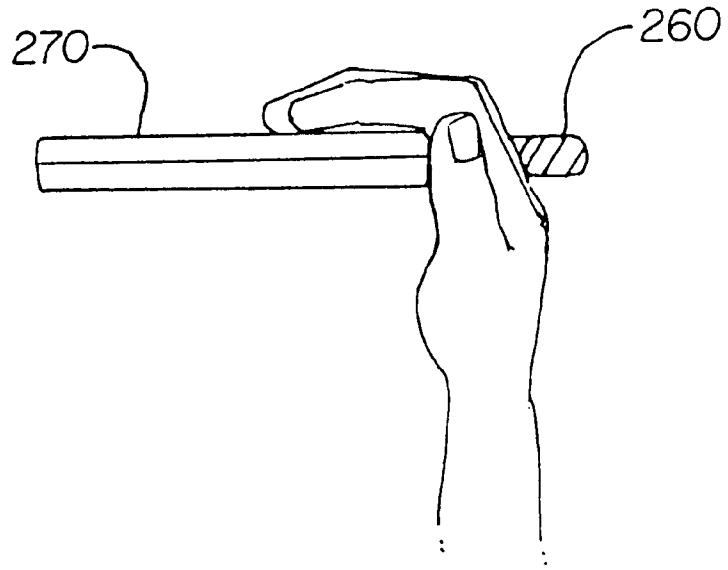


FIG. 11

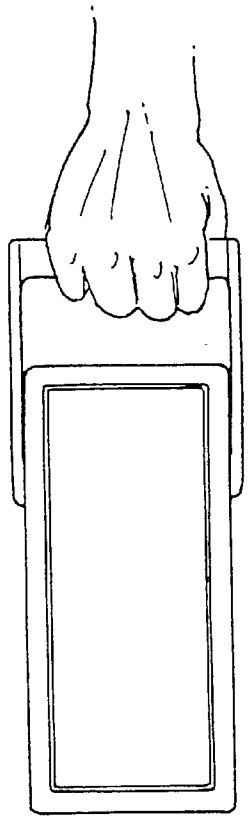


FIG. 12

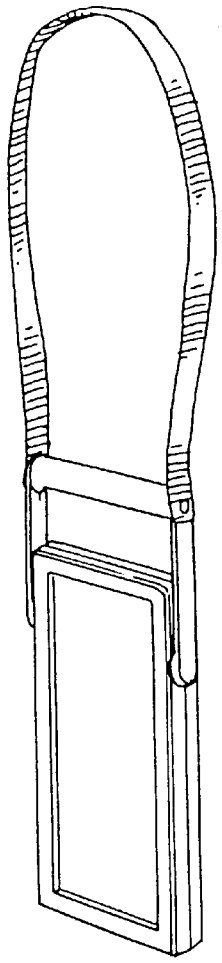
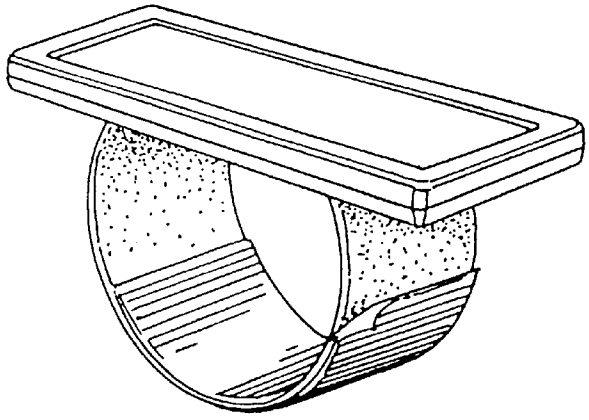


FIG. 13



TOUCH SCREEN SYSTEMS AND METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

The subject matter of this application is related to the subject matter of commonly assigned U.S. Provisional Applications Ser. No. 60/024,780, filed Aug. 28, 1996, Ser. No. 60/028,028, filed Oct. 9, 1996, and Ser. No. 60/036,195, filed Jan. 21, 1997, all of which provisional applications are incorporated by reference herein and priority to which is claimed under 35 U.S.C. §119(e).

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to touch-sensitive input and output devices, and more particularly, to touch screens that simultaneously can display a keyboard-type image superimposed on a background image. The invention also relates to other features of touch-sensitive i/o devices. Embodiments of the invention have particular application to wearable-computing devices and environments, although non-wearable embodiments are also contemplated.

2. Description of Related Art

It is known in the art to superimpose a keyboard over an image that is output by an application being executed on a computer, i.e. to form a "phantom" keyboard, on a touch-sensitive input display device. U.S. Pat. No. 5,581,243 to Ouellette et al., for example, which is incorporated by reference herein in its entirety, describes a system for displaying a simulated keyboard on a touch-sensitive display, without occluding from view an underlying application output image. An output image is generated and displayed for a first period of time at a first luminous radiation intensity having a predetermined persistence. A simulated keyboard image is generated and displayed for a second, shorter period of time at a second, lower luminous radiation intensity having the predetermined persistence. The keyboard and output images are generated in alternation, and the amount of time each is displayed is controlled, to try to create the illusion that both images are being displayed continuously.

The system described in Ouellette et al., however, is believed to suffer a number of disadvantages. First, it is believed that flashing between application and keyboard screens, as the reference discloses, would significantly reduce the refresh rate achievable relative to a continuously displayed application output (or a keyboard) image. This reduction could cause considerable detriment to the viewer and potentially could confuse the displayed interpretive features. Second, it is believed that displaying the keyboard and the application output in alternation requires additional hardware features for proper functioning, for example a second frame buffer for switching back and forth between the screens. Additionally, although this feature is not disclosed or apparently contemplated in Ouellette, using the Ouellette device in a wireless-transmission (e.g. RF) environment, for example in a wearable-computing context, would require e.g. twice as much information to wirelessly be transmitted and therefore would greatly increase the required bandwidth.

SUMMARY OF THE INVENTION

To overcome the above and other disadvantages, a screen peripheral system according to an embodiment of the invention includes a computing device for producing a main image and a touch-activated input device for generating and displaying a composite image visible to a user. The composite image simultaneously includes a representation of at least one key, for example a QWERTY keyboard, for activating an input function, and the main image provided by the computing device. The keyboard representation preferably is laid over the main image.

The system implements variable-pixel control to form the keyboard representation and to form the main image, causing the pixels selected to form the keyboard representation and selected to form the main image to be dependent on each other. In other words, the keyboard-representation pixels are not independent of the main-image pixels. According to one embodiment, the main image is an output image generated by an application being executed by the computing device.

Various image-adjustment, mode-switching, zoom-up/zoom-down and other embodiments associated with invention are also described, as are corresponding methods.

Embodiments of the invention have particular application to wearable computing devices, such as those available from ViA, Inc., Northfield, Minn. Attention also is directed to the following U.S. patents, each of which is incorporated by reference herein: U.S. Pat. Nos. 5,581,492; 5,572,401; 5,555,490; 5,491,651 and 5,285,398, all of which are owned by ViA, Inc.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be described with respect to the figures, in which like reference numerals denote like elements, and in which:

FIG. **1** is a perspective view of a wearable computing environment according to an embodiment of the invention;

FIG. **2** shows a keyboard representation according to an embodiment of the invention;

FIG. **3** shows a main image according to an embodiment of the invention;

FIG. **4** shows a composite image according to an embodiment of the invention;

FIG. **5** shows a second composite image according to an embodiment of the invention;

FIG. **6** is a flow chart showing operational steps according to an embodiment of the invention;

FIG. **7** shows a reduced-key keyboard;

FIG. **8** shows a touch screen according to an embodiment of the invention; and

FIGS. **9–13** show touch screens having a handle, according to embodiments of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the invention have wide application in a number of computing environments. The invention is particularly applicable to wearable computing environments, as discussed above, in which portability and compactness are fundamental considerations. The invention is also applicable to a number of different input/output devices. For example, embodiments of the invention contemplate i/o devices with full, partial, reduced-key, alphanumeric or non-alphanumeric keyboards comprising one or more "keys," "buttons," "contact zones" or the like. The invention also contemplates a number of input schemes in which a user manually or audibly directs certain keys to be activated, not just screens requiring direct manual contact with e.g. a user's finger. Proximity-based, pen-based and voice-based

inputs are among the functionalities encompassed by embodiments of the invention. In fact, any display with any "pointing" device, i.e. a device that designates a particular point or zone on the display, is contemplated for use with embodiments of the invention. Therefore, although particular embodiments will be described with respect to touch screens, keyboards and touch input, the invention is intended to be broadly interpreted as needed and not necessarily limited to those particular embodiments.

Additionally, various images can be combined/superimposed according to embodiments of the invention. In primary embodiments, the superimposed image is that of at least one key, e.g. a keyboard. The background image is that output by an application executed by a computing device, for example a graphics, spreadsheet, word-processing, etc. application for use in private, commercial, military, public-service fields or other fields. However, either the background image or the superimposed image can be of other types; for example the background image, or both images, can be provided by a processor or storage device associated with the system, instead of by an application program per se. Either or both image can be the subject of an enlargement or reduction process, to provide composite images having elements of different sizes. More than two images can be combined according to the invention as well; any combination of application, keyboard, or other images can be combined in a composite image. Therefore, although particular embodiments will be described herein with reference to application-output images, keyboards, etc., the invention is intended to be broadly interpreted as needed and not necessarily limited to those particular embodiments.

Touch screen keyboard overlays according to embodiments of the invention can be selectively turned on and off by a user of an associated personal computing device, for example a wearable personal computer. A representation of a keyboard, as will be described, lies over a main image on the touch screen, the main image preferably being formed in connection with a main software application. A keyboard overlay according to the invention eliminates a physical keyboard or the necessity of having a split screen with a touch keyboard on a lower portion and a main screen squeezed into the remaining upper portion, for example. A keyboard overlay according to the invention also reduces and/or eliminates the space-conflict problems that can arise when a superimposed keyboard occupies the same portion of the display screen as a critical portion of the application output image.

Keyboard overlays according to the invention are especially advantageous for very small screens, because of the relatively large and accessible overlay "buttons" (keys) that are provided, along with the ability to see all of the data behind the keyboard at the same time.

Embodiments of the invention are especially advantageous in situations where voice-based input is undesirable. Although voice-recognition technology is making significant advances, it still requires verbal input, which can be disruptive to a meeting, for example. Verbal input also potentially announces to all within earshot of the speaker the exact notes, etc. that are being entered. According to embodiments of the invention, therefore, the user inputs directly to the machine in complete silence. Still, voice-based input may be desirable in many cases, so optional switching between voice input and keyboard-overlay input is also contemplated. This can be activated by a physical button or key on the side or other surface of the touchscreen or associated device, or by a virtual button or key on the touch-sensitive portion of the screen itself, or by voice.

Keyboard overlays according to embodiments of the invention can take a number of forms. For example, a solid-line or dashed/dotted-line overlay is contemplated, providing outlines of each key. Alternatively, and selectively as chosen by a user, each key can be represented by a dot, or as a letter-area zone between intervening markers such as x's, dots, etc. Ideally, the representation of the keyboard is provided faintly on the standard screen, so that it and data/images from the main program can be seen simultaneously. Variable-pixel controls, described in more detail below, can be provided to change the thickness, brightness, and/or dotted-ness of the keyboard representation. In many cases the keyboard overlay can be extremely faint. Additionally, a color difference can be imparted to the pixels of either the keyboard overlay or the underlying image, or both, to highlight the difference between the two.

The characters of the keyboard themselves, e.g. the letters associated with each key or zone, can be turned off if the user has memorized the keyboard layout, for example. The keyboard can be active without being visible at all, for the user who can type effectively without even seeing representations of the keys/zones themselves.

Contrast adjustment buttons are contemplated, preferably represented on the touch screen itself but possibly on a housing of the touch screen, to adjust contrast between the keyboard and the main screen. A keyboard on-off button is also contemplated. Alternatively, these features can be controlled by voice.

Variable-pixel controls

In accordance with embodiments of the invention, software-based variable-pixel controls are provided to determine and control which pixels of the touch screen will be used for displaying the keyboard representation and which pixels for displaying the main image. In some cases, each pixel of the screen is 100% dedicated to either the keyboard or the main image. In other cases, touch screen pixels may be dedicated to both the keyboard and the main image, producing a "blended" effect as will be described.

Merging the image of the virtual keyboard with the normal output image on the display according to the invention can occur by a variety of methods and programming schemes. Using most current video graphics controllers, however, it is believed a highly efficient method available to perform the merging of images is to use bit-block or bit-block-type transfer operations, i.e. BitBlt operations.

BitBlt operations provide an efficient method of performing logical combination of up to three sets of pixels on raster-based display devices. According to embodiments of the invention, BitBlt operations are used with the following three sets of pixels:

(1) The original pixels on the display, i.e. the image that would be presented in the absence of the virtual keyboard.

(2) The pixels representing the image of the virtual keyboard.

(3) An image mask, allowing control of which pixels within the virtual keyboard will be merged with the original display pixels.

Using BitBlt operations, the virtual keyboard can be combined with the display using a variety of effects. The following table summarizes the typical operations that can be performed:

Source (S)	1 1 0 0 1 1 0 0		
Destination (D)	1 0 1 0 1 0 1 0	Boolean	
Mask (M)	1 1 1 1 0 0 0 0	Operation	Operation
Result	0 0 0 0 0 0 0 0	0	Blackness
	0 0 0 1 0 0 0 1	~(S|D)	Not source erase
	0 0 1 1 0 0 1 1	~S	Not source copy
	0 1 0 0 0 1 0 0	S & ~D	Source erase
	0 1 0 1 0 1 0 1	~D	Destination invert
	0 1 0 1 1 0 1 0	M ^ D	Mask invert
	0 1 1 0 0 1 1 0	S ^ D	Source invert
	1 0 0 0 1 0 0 0	S & D	Source and
	1 0 1 1 1 0 1 1	~S|D	Merge paint
	1 1 0 0 0 0 0 0	M & S	Merge copy
	1 1 0 0 1 1 0 0	S	Source copy
	1 1 1 0 1 1 1 0	S|D	Source paint
	1 1 1 1 0 0 0 0	M	Mask copy
	1 1 1 1 1 0 1 1	M|~S|D	Mask paint
	1 1 1 1 1 1 1 1	1	Whiteness

Additionally, those of skill in the art upon reading this disclosure will comprehend that similar logic functions can be applied to the color-differentiation capability described earlier; such functions are not limited to black/white/grey capabilities.

The logical operations described herein each preferably have a different blending or merging effect. Although some of them do not have substantive effect, e.g. they just copy the source in to the destination or just fill it with zeros or ones and are ignorant of what the source and destination have, the large majority of these operations can be used to create a number of different effects to determine how to mesh the keyboard image and the application output image together. Additionally, the various logical operations can be combined as needed to produce an even greater variety of visual effects, e.g. harshness/intensity of one image with respect to the other.

Two examples of the myriad of meshing possibilities contemplated according to the invention will now be described. In the first example, the keyboard is blended with the original display application-output image by using 25% of the pixels to represent the keyboard and 75% of the pixels to represent the original display image. In the second example, the two images are more truly blended together, with each pixel of the final composite display image receiving a contribution from both images. For the second example, the composite realized image can appear as e.g. a blended shadow from the original images. For both examples, it is assumed according to one embodiment that the graphics controller of the computer system is using an 8-bit bit plane, which is typical of most personal computers supporting 256 colors per pixel. Of course, those of ordinary skill will readily be able to adapt these examples for use in other current and future graphics controllers, bit planes, etc.

In the first example, where the keyboard is blended with the display by using 25% of the pixels to represent the keyboard and 75% of the pixels to represent the original display image, each display update preferably is performed in three steps. The first step removes that portion of the keyboard image that is not to be seen, i.e. it eliminates 75% of the keyboard image. The second step removes that portion of the main display image that is not to be seen, i.e. it eliminates 25% of the main display image. The third step merges these two images. The following pseudocode represents one embodiment of the associated processing used according to this example:

```
reduced_kbd := BitBlt     (source      => keyboard image,
                           destination => keyboard image,
                           mask        => [0xFF, 0x00, 0x00, 0x00,
                                           0xFF, 0x00, 0x00, 0x00,
                                           . . . ],
                           operation   => merge copy);
reduced_display := BitBlt (source      => original display image,
                           destination => original display image,
                           mask        => [0x00, 0xFF, 0xFF, 0xFF,
                                           0x00, 0xFF, 0xFF, 0xFF,
                                           . . . ],
                           operation   => merge copy);
display := BitBlt          (source      => reduced_kbd,
                           destination => reduced_display,
                           mask        => null,
                           operation   => source paint);
```

With the first example, for performance reasons the first BitBlt can be performed once at initialization and then stored for reuse in future display updates. Essentially, the process eliminates from the two images those pixels that are not desired for the single, final composite image that is displayed to the user. In this way, neither image contains overlapping pixels. In the combined image, therefore, each pixel is contributed 100% by either the keyboard or the display, but 0% from the alternate.

With the second example, the two images are logically combined using a single BitBlt, according to one embodiment. The following pseudocode represents one embodiment of the associated processing used according to this example:

```
display := BitBlt          (source      => keyboard image,
                           destination => original display image,
                           mask        => null,
                           operation   => source paint);
```

Current embodiments of the invention employ the following assumptions for performance reasons. It is contemplated that embodiments of the invention are for typically available operating systems, ones that support multi-tasking, with each application having its own thread of control, and a graphical user interface using windows as the visual representation of each task. Examples of such operating systems are Microsoft Windows 95, Microsoft Windows NT, SCO Unix, and Sun's Solaris operating system. Embodiments of the invention are also for typical video graphics controllers, ones that support bit-block transfer (BitBlt) operations and DMA between processor memory and video memory. Graphics controllers from Chips and Technologies, S3, NeoMagic, Trident, and other companies all support these operations, for example.

Embodiments of the invention should be useable without necessarily relying on these assumptions, as hardware and software technologies evolve, for example (such as with multiprocessors used in one device, for example). Even currently, implementation in environments other than those described above is contemplated according to the invention, even though implementation in at least some of those environments may be more complex and subject to slower operation.

Thus, according to embodiments of the invention, and as shown in e.g. FIGS. **1–5**, screen peripheral system **5** according to an embodiment of the invention includes computing device **10** for e.g. executing a software application, and touch-activated input device **15** for generating and display-

ing a composite image visible to a user **20** of screen peripheral system **5**. The composite image includes, according to one embodiment, a representation of at least one key for activating an input function, e.g. a keyboard-input function. The composite image also includes a main display image, for example the output image produced by the software application being executed by computing device **10**. The representation of at least one key is laid over the main image produced by the software application.

FIG. **1** shows screen peripheral system **5** in a wearable-computing environment, which as described earlier is especially well-suited to embodiments of the invention. Embodiments of the invention can also be used in connection with a miniature, low-power, spread-spectrum "bodyLAN"-type system allowing selective control based on proximity to a user. With such a system, touch-activated input device **15** can be in either wired or wireless communication with computing device **10** and/or other devices/systems, for example LANs, WANs, etc. Wired and wireless communication embodiments are also contemplated for use with non-wearable computing devices as well. Fiber optic, electrical, infrared, RF and other data-transmission schemes between e.g. the disclosed input device and the wearable or other computer, or between any other elements of the system, are contemplated. For example, RF transmission to keyboard or a wearable, desktop, laptop or other computer. Embodiments of the invention are especially useful with tablet-type touch screens and other small, readily portable/pocketable input/output devices.

Embodiments of the invention also can be used in connection with heads-up and/or body-worn display devices, e.g. dual-screen stereo displays. A keyboard overlay according to the invention, preferably a voice-activated and/or voice-controlled overlay, appears on the display, allowing the user to input data without looking down. Automatic typing features with voice-recognition can be provided, whereby the user sees individual keys of the keyboard being activated as the user speaks. Voice can thus be used as an intuitive keyboard approach for the spoken words/letters in a hands-free environment.

Screen peripheral system **5** implements variable-pixel control to form the representation of at least one key and to form the output image, for example in the manner described above. The variable-pixel control causes the pixels used to form the representation of at least one key and the pixels used to form the output image to be directly dependent on each other, in a manner that for example is also described above. In other words, unlike the Ouellette reference disclosed above, the pixels chosen to represent the images are not independent.

The variable-pixel control can provide contrast adjustment between the representation of at least one key and the output image produced by the software application. The contrast adjustment can include changing at least one of the thickness, brightness, color and dotted-ness of the representation of at least one key.

As referenced above, according to one example computing device **5** eliminates X% of the pixels of a full representation of at least one key, X% representing that portion of the keyboard that is not to be seen in the composite image. In the first example described above, X=75, although X can have a variety of different values to suit a particular display or purpose. Computing device **5** also eliminates (100-X)%, e.g. 25% as described above, of the pixels of a full application output image. Here, (100-X)% represents that portion of the application output image that is not to be seen in the composite image. Computing device **5** merges the pixel-eliminated key representation with the pixel-eliminated main image to form the composite image. Alternatively and/or additionally, as in the second example described above, the composite image can include a blended shadow of the representation of at least one key and the main image. Computing device **5** can control the lightness/darkness of the blended shadow by controlling the blending of pixels of the at least one key representation and the main image, according to one embodiment. By changing the darkness of the pixels of the composite image, for example the keyboard portion of the composite image, the keyboard can be made to appear to "bleed through" the other image. Thus, the keyboard "steals away" appropriate pixels from the main image, and/or shades them differently in a selected manner, to produce the keyboard image.

As will be appreciated by those of ordinary skill in the art upon reading this disclosure, methods corresponding to the above-described apparatus and systems are also contemplated according to the invention.

FIGS. **2–5** illustrate sample images and composite screens according to embodiments of the invention. FIG. **2** illustrates a representation of at least one key—in this example a full QWERTY keyboard with several function/option keys/buttons. FIG. **3** illustrates a main image generated by a computing device. FIG. **3** should also be interpreted to cover the situation where the main image is an output image or images of an application or applications being executed by a processor or other element of the computing device. FIG. **4** shows a composite image formed in accordance with Example 1 above, and FIG. **5** shows a composite image formed in accordance with Example 2 above.

FIG. **6** illustrates a flow chart according to an embodiment of the invention, identifying the generalized processing that occurs to allow a virtual keyboard to be overlayed upon a normal display. This processing maintains consistency of the virtual keyboard image with the rest of the information being displayed.

After start step **100**, a virtual keyboard image is created, at step **105**. The keyboard is drawn as an overlay on the current display in step **110**, and then an event is awaited at step **115**. When a touch event occurs at step **120**, the virtual key touched is determined at step **125** and the keyboard event is sent to the current task/window at step **130**. The next event is then awaited at step **115**.

If there is no touch event at step **120**, it is determined whether a pertinent window has been redrawn, at step **135**. If so, the area of screen redrawn is determined at step **140**, and then it is determined at step **145** whether the area of screen redrawn overlaps the keyboard image. If not, the next event is simply awaited at step **115**. If so, the keyboard is (re)drawn as an overlay on the current display at step **110**. It is also determined whether a window is deleted at step **150**, and whether a window is created, at step **155**. If the answer is yes, steps **140**, **145** and **110** or **115** occur as described above. If the answer is no, the next event is (still) awaited at step **115**.

Mode-switching

According to one embodiment, if a representation of a key or button is held "down" for a set time, for example one second, a cursor appears at the point of the depressed key and the remainder of the keyboard (optionally) disappears. By dragging a finger along the touch screen, the user can move the cursor to a desired location. According to one embodiment, upon entering the cursor mode a number of new keys/buttons (or representations thereof, as above) appear on a side of the screen, for example, cut, paste, copy, delete and/or hold buttons. An appropriately placed mouse

button is also contemplated on the screen, e.g. in a corner of the screen, to be accessed by a user's thumb. A convenient holding mechanism for the screen, allowing easy access by the user's thumb, is described below.

In use, a user types on the keyboard overlay for a desired time, and then holds one finger down for a set period of time to exit the keyboard mode and enter the cursor mode. Selected text can be highlighted using the above-described mouse button in e.g. a corner or on a side of the touch screen, and then the cursor can be dragged to hover over a cut button or other desired button. Movement of the user's finger becomes equivalent to movement of the mouse when the finger is held down, and the touch button for the mouse is in the corner of the screen so that it is accessible by the thumb. Upon exiting the cursor mode, the user's fingers are again used for typing.

Reduced-key embodiments

According to one keyboard overlay embodiment, the number of keys of a virtual QWERTY keyboard is reduced to e.g. twelve, nine of which are letter keys and the other three of which are shift, delete and select keys, for example. Note FIG. **7**, showing one type of reduced-key keyboard **200**. Each letter key represents multiple letters, for example three letters or letter combinations. A word-recognition program discerns the word intended to be typed by hitting the letter keys, e.g. upon depressing the select (or space) keys. Reduced-key keyboard patterns enhance miniaturization achievable according to the invention and provide other advantages.

According to one embodiment of the invention, a reduced-key keyboard is incorporated as a virtual or physical touch layout **210** on a standard touch screen/slidepad mouse **220**, as shown in FIG. **8**. A program monitors the touch screen **220** continually, detecting when a virtual option button **230** or physical option button **240** is selected to change the mode of operation from a standard touchpad mouse ("relative" mode) to a keyboard-input touchpad ("absolute" mode). Upon entering the keyboard mode, a key pattern overlay (e.g. a letter keyboard, number pad, and/or individual keys) according to the invention appears on the touchscreen directly and/or on an associated screen. It is then detected which key of the keyboard the finger of the user is tapping on to generate letter/word or other input. Using a reduced-key keyboard in connection with a standard touchpad mouse, with mode-switching as described above, provides significant display-miniaturization and key-enlargement advantages, as well as other advantages such as an increase in one-finger typing speed.

According to another embodiment, the virtual or physical select or other buttons **230**, **240**, or another area on the touch screen itself, can be depressed multiple times, or held down for a longer period of time, to enter and/or exit various submodes of operation. The first touch can cause a change from a relative mode to an absolute mode, and subsequent touches to absolute submodes such as alphabet, numeric, punctuation and/or other sub-modes. For example, if a user desires to input e.g. punctuation while in a standard relative mouse mode, the user taps the appropriate button or buttons twice, first to enter the absolute mode and then to enter the punctuation input sub-mode, enters the appropriate punctuation, and then taps the button or buttons twice again to return to an absolute keypad mode. One or a plurality of buttons can be used to switch between relative and absolute modes, and, within e.g. the absolute mode, to choose a keyboard, number pad, punctuation input sub-mode or other option.

It is also known in the art to reduce the size of a full keyboard, with alphabetic, numeric and function sub-keyboards, by superimposing the keys of the sub-keyboards on top of each other. According to one example, the alphabetic sub-keyboard is superimposed on the numeric and function sub-keyboards. For numeric input, the numbers are printed not at the top of each key but where multiple adjacent letter keys meet, at the interstices between the keys. Four "quarter" keys thus operate together to register the desired number, but each virtual number key is full-sized. Beneath the four letter keys associated with each number are sensing areas, i.e. points or elements or regions, with activation of a sufficient number of sensing areas by the user's finger registering the desired number. This technology reduces the overall size of the keyboard, for example to credit-card size. Examples of these types of key layouts are shown in U.S. Pat. No. 5,612,690, among others. U.S. Pat. No. 5,612,690 is incorporated herein by reference.

Superimposing the keys of various sub-keyboards on top of each other, such as an alphabetic sub-keyboard superimposed on a numeric and/or function sub-keyboard, can be combined with the reduced-key concepts disclosed above with respect to FIGS. **7–8**, to further reduce the size of a keyboard or keyboard overlay according to the invention. With the layout of the FIG. **7** embodiment, for example, number and/or function keys would be placed at the physical or virtual "interstices" between the three-letter keys shown. The resulting composite image would then be superimposed over an application output in a manner described previously, for example.

Zoom embodiments

According to other embodiments, zoom-up/zoom-down capabilities are incorporated through a touch screen or other touch-sensitive input device, for example in a manner compatible with the above-described technologies. Once an appropriate zoom mode is activated, e.g. by virtual or physical keys, contact of one, two, three or more of a user's fingers with the touch-sensitive surface causes activation of an appropriate number of sensing areas and/or "zones" thereon to control screen size and/or the amount of magnification displayed. According to one example embodiment, one-finger contact causes normal screen size and/or magnification, two-finger contact causes a zoom-up to double size/magnification, three-finger contact causes triple size/magnification, and so on. Zoom-down capabilities function can be configured similarly. Sequential step-up or step-down is not required; for example triple-size/magnification can be reduced to normal size/magnification merely with the touch of one finger, without entering a double-size/magnification mode.

Thus, the user is spared the burden of going to a file menu, pulling down to the zoom feature and then selecting zoom-in and zoom-out functions using e.g. the mouse. A virtual, physical, or voice-activated zoom function select button is activated, and, simultaneously or thereafter, the touchscreen/slidepad itself determines how much of the touchscreen is covered at any one time by the user's fingers (or other pointing device), providing a specific screen size/magnification related to the number of fingers being used. According to a more specific embodiment, appropriate zoom functionality occurs based on the number of sensing areas or contact zones activated on the touch-sensitive input device. A particular area of a screen chosen can "zoom up" at the user as that area is touched.

These features have special relevance to portable, wearable computing, in which miniaturized screens are used, for example on the wrist, and generally are not full-sized. To use existing software, a user may want to see screen features in larger, zoomed-in format at certain times and, at other times,

in a zoomed-out format in refer ence to how items look on an overall page. Flip and rotate commands, either voice-based or touch-based, can also be implemented to improve/augment the user's view of the displayed information.

Other hardware embodiments

One problem with prior touch screens is that for miniature computers and miniature screens, the user's hand is often bigger than the screen itself. According to the embodiments of the invention, therefore, retractable handle **260** (FIGS. **9–10**) slides relative to touch screen **270** between extended and retracted positions, as shown at **280**, to provide a convenient holding mechanism at either the left or right side of touch screen **270**. To shift handle **260** from the left side to the right side, or vice versa, pivot **285** is provided to swing the handle over the touch screen, as shown at **290**. In the retracted position, the handle catches on the back side of the touch screen, permitting the pivoting motion. Upon traveling to or remaining in an extended position, a ball or similar projection snaps into a lateral groove or equivalent mechanism to prevent pivoting. Thus, embodiments of the invention are significantly advantageous for use by both left-handed and right-handed individuals, as shown in FIG. **10**, as well as those who need to use alternative hands for different tasks. Handle **260** can also be used as a carrying handle (FIG. **11**), as part of a necklace embodiment (FIG. **12**), or in a wristband embodiment (FIG. **13**) using e.g. a VELCRO strap. Additionally, according to another embodiment, a double-sided touch screen is provided, with the capability of flipping the screen by voice or by touch to accommodate left-handed or right-handed gripping of the touch screen by the handle without pivoting the handle from one side to the other. Multiple screen bleedthroughs, e.g. from one screen to another, on multiple screens, are also contemplated. A person with a folding screen or two displays can have them on more than one screen.

As indicated earlier, embodiments of the invention have application in voice-recognition and/or hands-free embodiments. A microphone/speaker can be built in the face of the touch-sensitive input device, permitting a user to look at and talk to the device without having a separate microphone/speaker. Voice commands can be used to change turn keyboard overlays and/or voice-input modes on and off, and to change contrast, keyboard representation types, keyboard/cursor modes, etc. Voice commands also can be used to activate the touch screen itself, so that it doesn't turn on by e.g. being depressed in a user's pocket, for example.

Other features

Sound and flashing can also be used in connection with an area to highlight where and when a user has touched the input device. Merging program use can be incorporated to highlight certain program outputs that are active and/or de-emphasize those that are inactive, for example by using a 25% pixel ratio for de-emphasis. As a user switches from one active program to another, their bleed-through intensities can shift and change accordingly. Multiprocessing be incorporated, wherein separate screens are run by separate processors, one for each screen. Keyboards can be moved, and percentage areas changed, by dragging. Although preferred embodiments have been described with respect to two images, any number of images can be combined/blended according to embodiments of the invention as long as their visual distinctions are preserved to the user's eye.

It is contemplated that features disclosed in this application, as well as those described in the above applications incorporated by reference, can be mixed and matched to suit particular circumstances. Various other modifications and changes will be apparent to those of ordinary skill.

What is claimed is:

1. A screen peripheral system, comprising:

a computing device for providing a main image; and

a touch-activated input device for generating and displaying a composite image visible to a user of the screen peripheral system, the touch-activated input device comprising a plurality of pixels, the composite image simultaneously including:

a representation of at least one key, the representation of at least one key activating an input function; and

the main image provided by the computing device, the representation of at least one key being laid over the main image;

wherein the screen peripheral system implements variable-pixel control to form the representation of at least one key and to form the main image, the variable-pixel control causing pixels selected to form the representation of at least one key in the composite image to depend on and be activated simultaneously with pixels selected to form the main image, such that the main image and the representation of at least one key are displayed simultaneously to form the composite image;

further wherein the variable-pixel control includes logical operators to provide different blending/merging effects such that individual pixels of the touch-activated input device can be dedicated simultaneously to both the main image and the representation of at least one key.

2. The screen peripheral system of claim **1**, wherein the variable-pixel control provides contrast adjustment between the representation of at least one key and the main image produced by the computing device.

3. The screen peripheral system of claim **2**, wherein the contrast adjustment includes changing at least one of the thickness, brightness, and dotted-ness of the representation of at least one key.

4. The screen peripheral system of claim **1**, wherein the representation of at least one key is a dotted-line representation.

5. The screen peripheral system of claim **1**, wherein the representation of at least one key includes a representation of a full keyboard.

6. The screen peripheral system of claim **1**, wherein the touch-activated input device operates in two modes, the first mode being a keyboard mode in which a user activates input functions by intermittently touching the input device, and the second mode being a cursor mode in which the user moves a cursor associated with the touch-activated input device, the second mode being entered from the first mode and/or the first mode being entered from the second by continuously touching the input device for a set time.

7. The screen peripheral system of claim **1**, wherein the computing device forms the composite image by merging the representation of at least one key with the main image.

8. The screen peripheral system of claim **7**, wherein the computing device merges the representation of at least one key with the main image by using a bit-block-type transfer operation.

9. The screen peripheral system of claim **8**, wherein the bit-block-type transfer operation performs logical combinations of three sets of pixels:

(a) the pixels of the main image;

(b) the pixels of the representation of at least one key; and

(c) optionally, an image mask for controlling which pixels of the main image will be merged with which pixels of the representation of at least one key.

10. The screen peripheral system of claim 1, wherein each pixel of the touch-activated input device is contributed 100% by either the pixels of the main image or the pixels of the representation of the at least one key to form the composite image.

11. The screen peripheral system of claim 1:

wherein the computing device eliminates X% of the pixels of a full representation of at least one key, X% representing that portion of the keyboard that is not to be seen in the composite image;

further wherein the computing device eliminates (100-X)% of the pixels of a full main image, (100-X)% representing that portion of the main image that is not to be seen in the composite image;

further wherein the computing device merges the pixel-eliminated key representation with the pixel-eliminated main image to form the composite image.

12. The screen peripheral system of claim 1, wherein the composite image includes a blended shadow of the representation of at least one key and the main image, or a clear space around a blended area to highlight the area of blending.

13. The screen peripheral system of claim 12, wherein the computing device controls the lightness/darkness of the blended shadow by controlling the blending of pixels of the at least one key representation and the main image.

14. The screen peripheral system of claim 1, wherein the computing device executes a software application, the main image being an output image produced by the software application executed by the computing device.

15. The screen peripheral system of claim 1, wherein the touch-activated input device provides zoom-up/zoom-down capability dependent on the number of the user's fingers in contact with the touch-activated input device.

16. The screen peripheral system of claim 1, wherein the touch-activated input device allows switching between relative and absolute input modes depending on the number of times or amount of time a user contacts a selected area of the touch-activated input device.

17. The screen peripheral system of claim 1, wherein the touch-activated input device allows switching between keyboards/alphanumeric sets depending on the number of times a user contacts a selected area of the touch-activated input device.

18. A wearable computing system comprising the screen peripheral system of claim 1.

19. A method of superimposing a representation of at least one key over a main image provided by a computing device, the method comprising:

(a) using variable-pixel control to form a representation of at least one key, the representation of at least one key activating an input function, and to form the main image, the variable-pixel control causing pixels selected to form the representation of at least one key to be activated simultaneously with pixels selected to form the main image; and

(b) generating and displaying a composite image visible to a user of the screen peripheral system, the composite image simultaneously including the representation of at least one key and the main image produced by the computing device, the representation of at least one key being superimposed on the main image;

wherein the variable-pixel control allows individual pixels to be dedicated simultaneously to both the main image and the representation of at least one key.

20. The method of claim 19, wherein the step of (b) includes the step of merging the representation of at least one key with the main image.

21. The method of claim 20, wherein said merging includes using a bit-block-type transfer operation.

22. The method of claim 21, wherein (b) further includes combining three sets of pixels:

(aa) the pixels of the main image;

(bb) the pixels of the representation of at least one key; and

(cc) optionally, an image mask for controlling which pixels of the main image will be merged with which pixels of the representation of at least one key.

23. The method of claim 21, wherein (b) further includes:

(c) eliminating X% of the pixels of a full representation of at least one key, X% representing that portion of the keyboard that is not to be seen in the composite image;

(d) eliminating (100-X)% of the pixels of a full main image, (100-X)% representing that portion of the main image that is not to be seen in the composite image; and

(e) merging the pixel-eliminated key representation with the pixel-eliminated main image to form the composite image.

24. The method of claim 19, wherein the composite image includes a blended shadow of the representation of at least one key and the main image.

25. The method of claim 24, wherein (b) includes controlling the lightness/darkness of the blended shadow by controlling the blending of pixels of the at least one key representation and the main image.

26. A screen peripheral system, comprising:

means for computing, the means for computing providing a main image;

means for displaying a composite image visible to a user of the screen peripheral system, the means for displaying also being for input to the means for computing, wherein the means for displaying comprises a plurality of pixels, the composite image simultaneously including:

a representation of at least one input zone, the representation of at least one input zone activating an input function; and

the main image provided by the means for computing, the representation of at least one input zone being laid over the main image;

wherein pixels selected to form the representation of at least one input zone are activated simultaneously with pixels selected to form the main image, such that the main image and the representation of at least one input zone are displayed simultaneously to form the composite image;

further wherein individual pixels of the means for displaying can be dedicated simultaneously to both the main image and the representation of at least one input zone.

27. The system of claim 26, wherein the representation of at least one input zone comprises at least one key of a keyboard.

28. The system of claim 26, wherein the representation of at least one input zone comprises a contact zone.

29. The system of claim 26, wherein the representation of at least one input zone comprises a button.

30. The system of claim 26, wherein the means for displaying a composite image comprises a touch screen.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,121,960
DATED : September 19, 2000
INVENTOR(S) : David W. Carroll et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the front page of the patent, in the "References Cited" section, the following U.S. Patent has been added:

--5,148,155 9/1992 Martin, et al.--

Signed and Sealed this

Twelfth Day of June, 2001

Nicholas P. Godici

Attest:

Attesting Officer

NICHOLAS P. GODICI
Acting Director of the United States Patent and Trademark Office

EXHIBIT B

US00RE43700E

(19) **United States**

(12) **Reissued Patent**
Chen

(10) **Patent Number: US RE43,700 E**

(45) **Date of Reissued Patent: Oct. 2, 2012**

(54) **VIRTUAL REALITY CAMERA**

(75) Inventor: **Shenchang Eric Chen**, Los Gatos, CA (US)

(73) Assignee: **Intellectual Ventures I LLC**, Wilmington, DE (US)

(21) Appl. No.: **11/113,455**

(22) Filed: **Apr. 22, 2005**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **6,552,744**
Issued: **Apr. 22, 2003**
Appl. No.: **08/938,366**
Filed: **Sep. 26, 1997**

(51) **Int. Cl.**
H04N 5/225 (2006.01)

(52) **U.S. Cl.** **348/218.1**; 348/207.99; 348/36; 348/239

(58) **Field of Classification Search** 348/143, 348/36, 39, 218.1, 222.1, 239, 333.01, 281.1, 348/207.99
See application file for complete search history.

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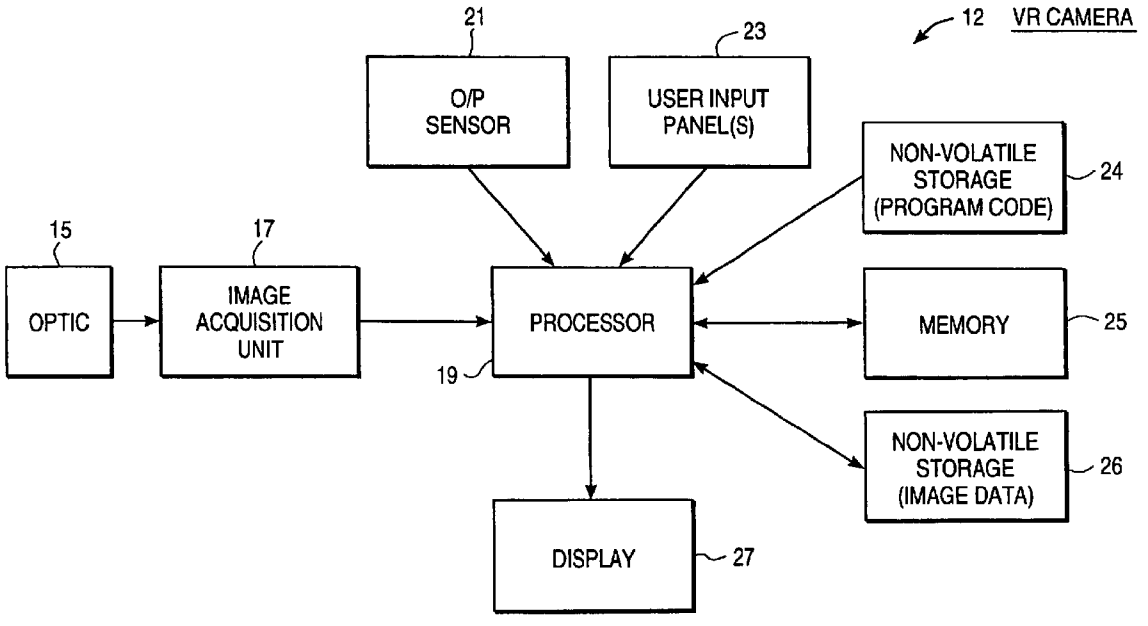
Primary Examiner — Tuan Ho
(74) *Attorney, Agent, or Firm* — Perkins Coie LLP

(57) **ABSTRACT**

A method and apparatus for creating and rendering multiple-view images. A camera includes an image sensor to receive images, sampling logic to digitize the images and a processor programmed to combine the images based upon a spatial relationship between the images.

108 Claims, 9 Drawing Sheets



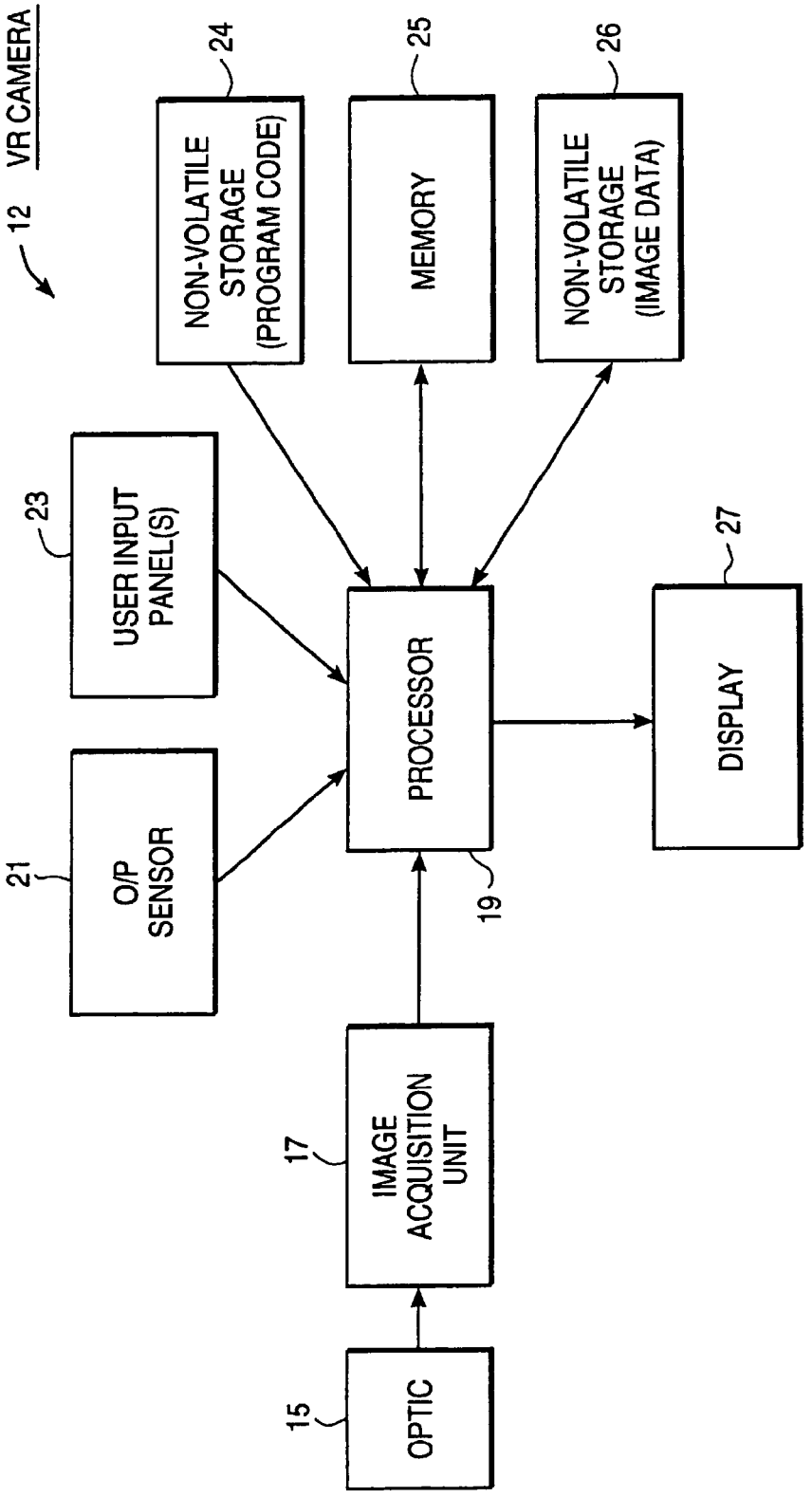

12 VR CAMERA
24
NON-VOLATILE STORAGE (PROGRAM CODE)
25
MEMORY
26
NON-VOLATILE STORAGE (IMAGE DATA)
23
USER INPUT PANEL(S)
27
DISPLAY
PROCESSOR
21
O/P SENSOR
19
17
IMAGE ACQUISITION UNIT
15
OPTIC

FIG. 1

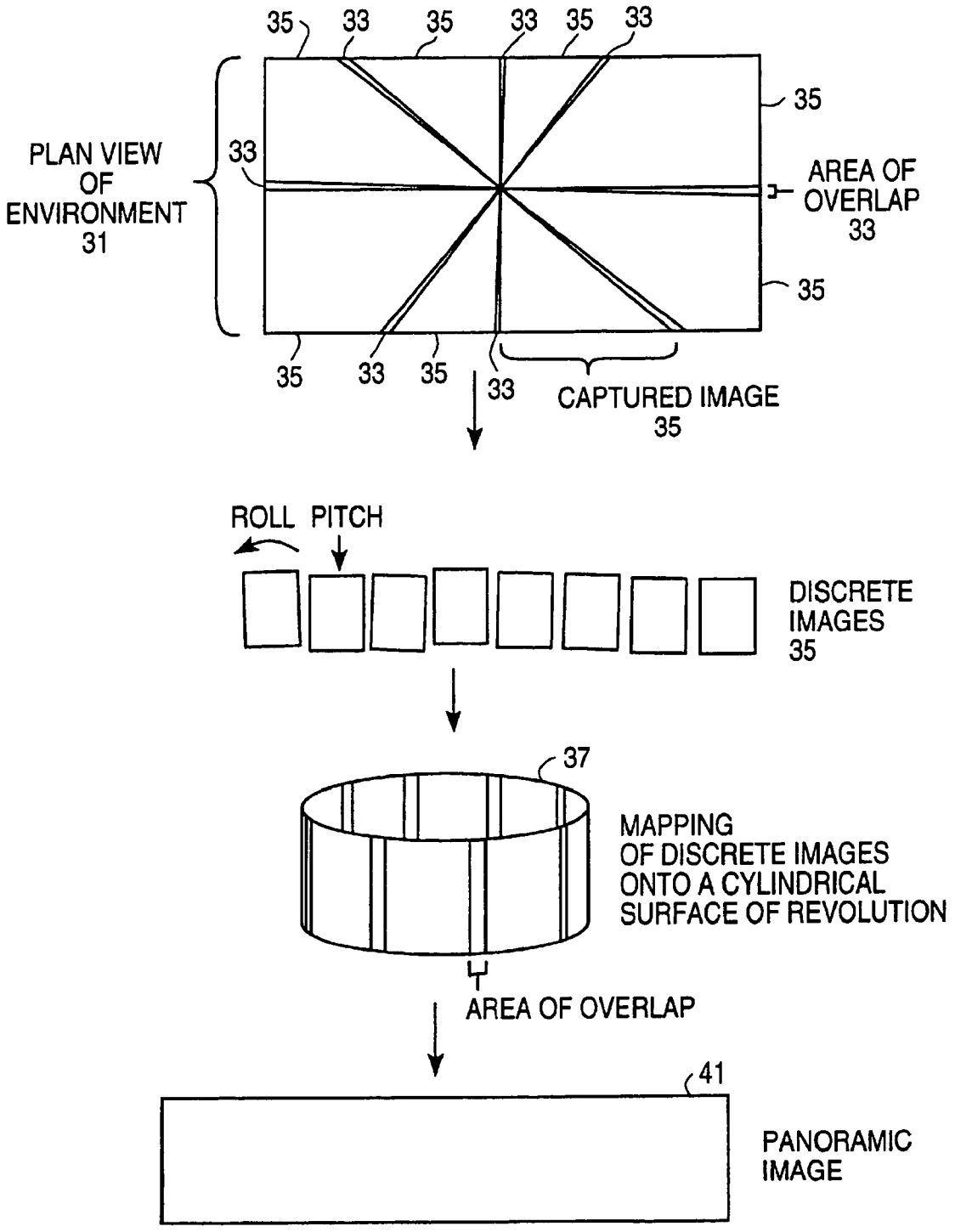

35
33
35
33
35
33
35
PLAN VIEW OF ENVIRONMENT 31
33
AREA OF OVERLAP 33
35
35
33
35
33
CAPTURED IMAGE 35
ROLL
PITCH
DISCRETE IMAGES 35
37
MAPPING OF DISCRETE IMAGES ONTO A CYLINDRICAL SURFACE OF REVOLUTION
AREA OF OVERLAP
41
PANORAMIC IMAGE

FIG. 2

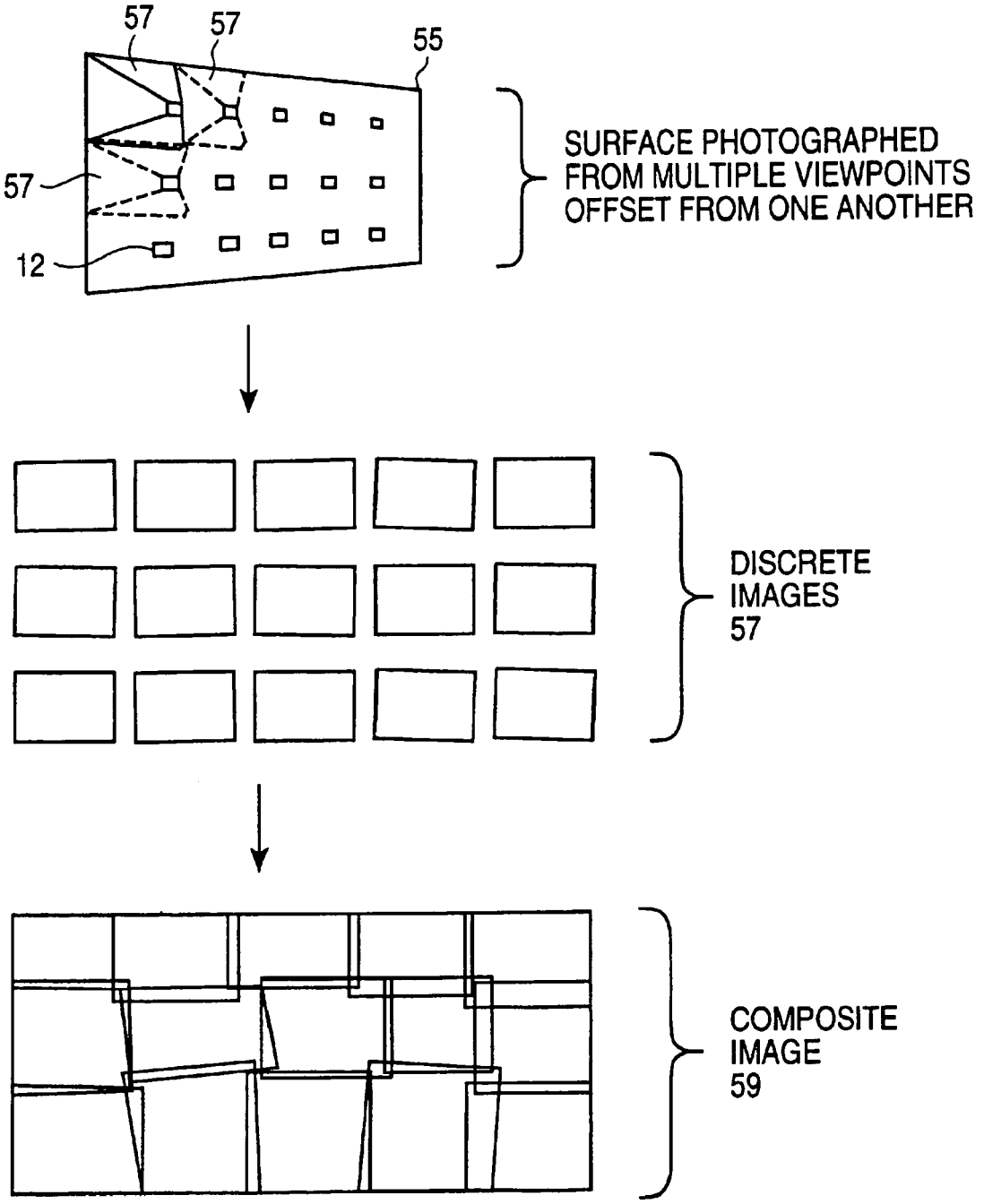

57
57
55
57
12
SURFACE PHOTOGRAPHED FROM MULTIPLE VIEWPOINTS OFFSET FROM ONE ANOTHER
DISCRETE IMAGES 57
COMPOSITE IMAGE 59

FIG. 3

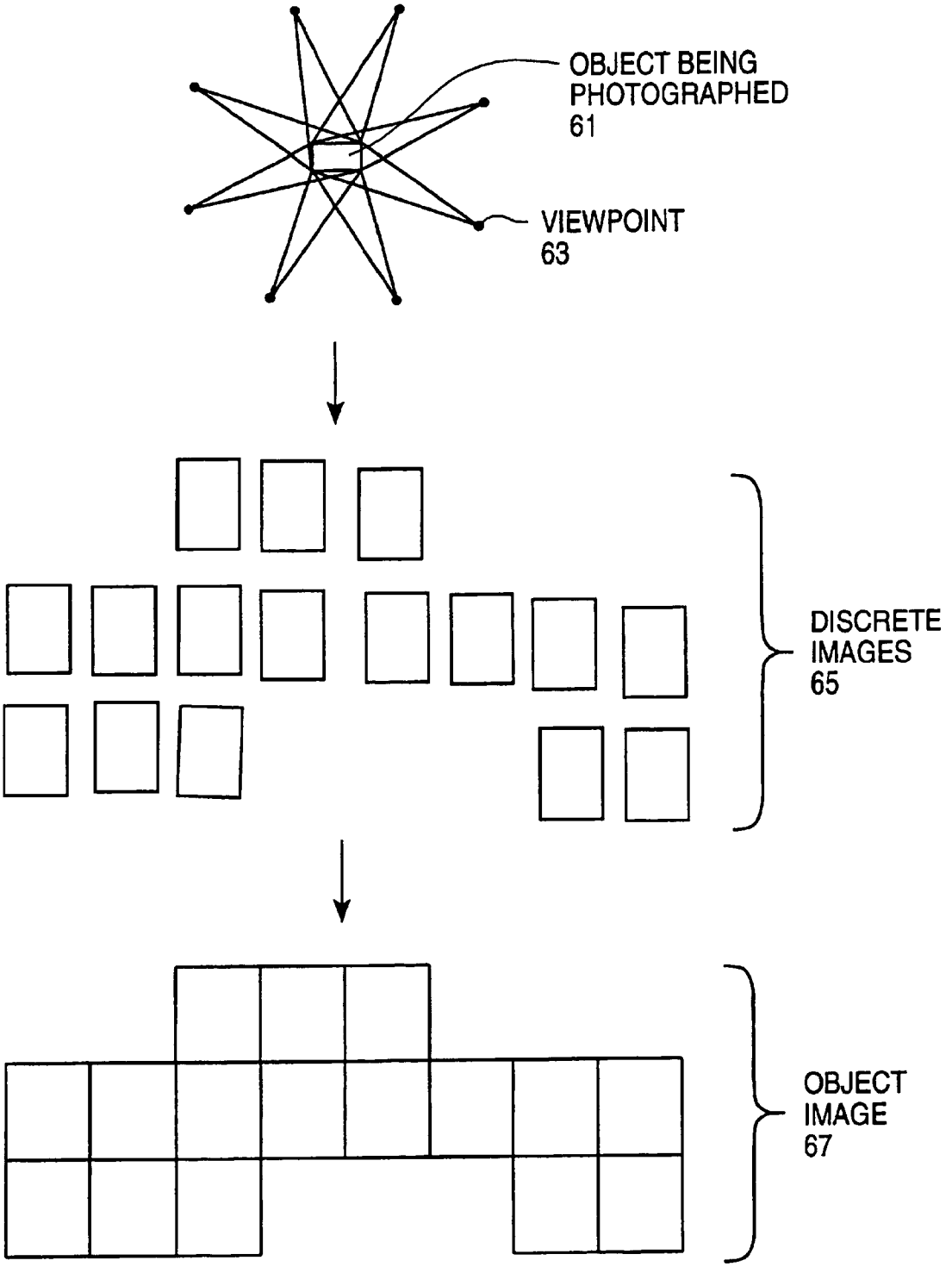

OBJECT BEING PHOTOGRAPHED 61
VIEWPOINT 63
DISCRETE IMAGES 65
OBJECT IMAGE 67

FIG. 4

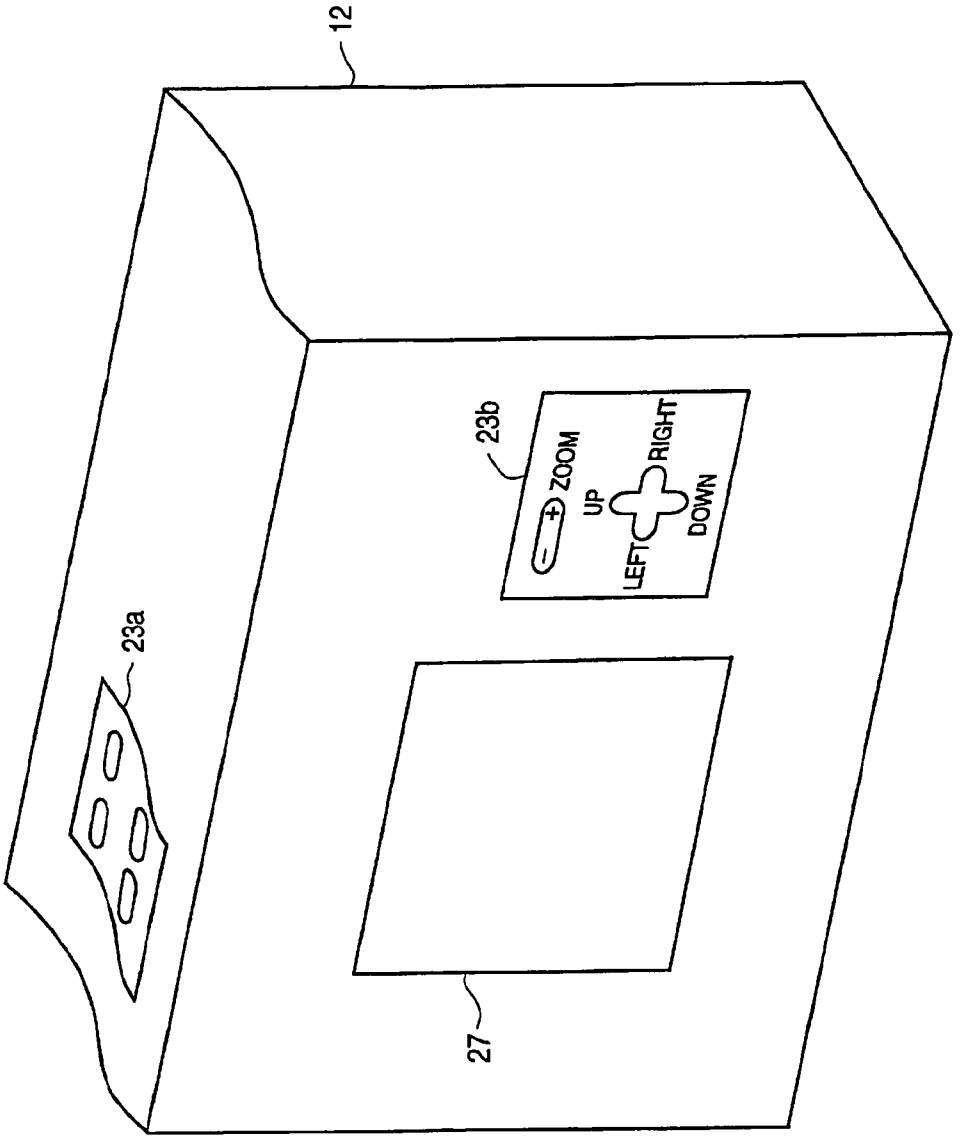


FIG. 5

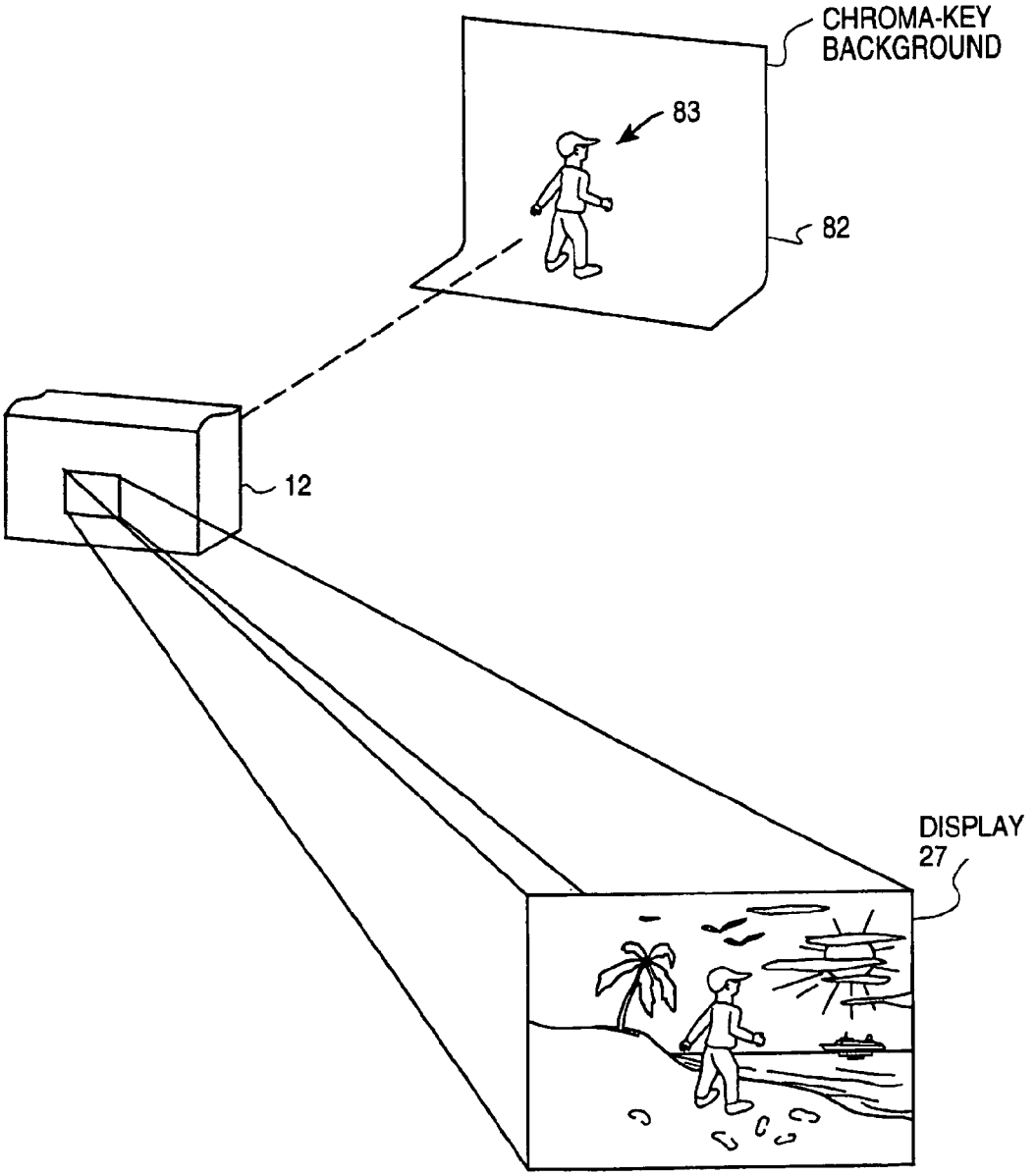


FIG. 6

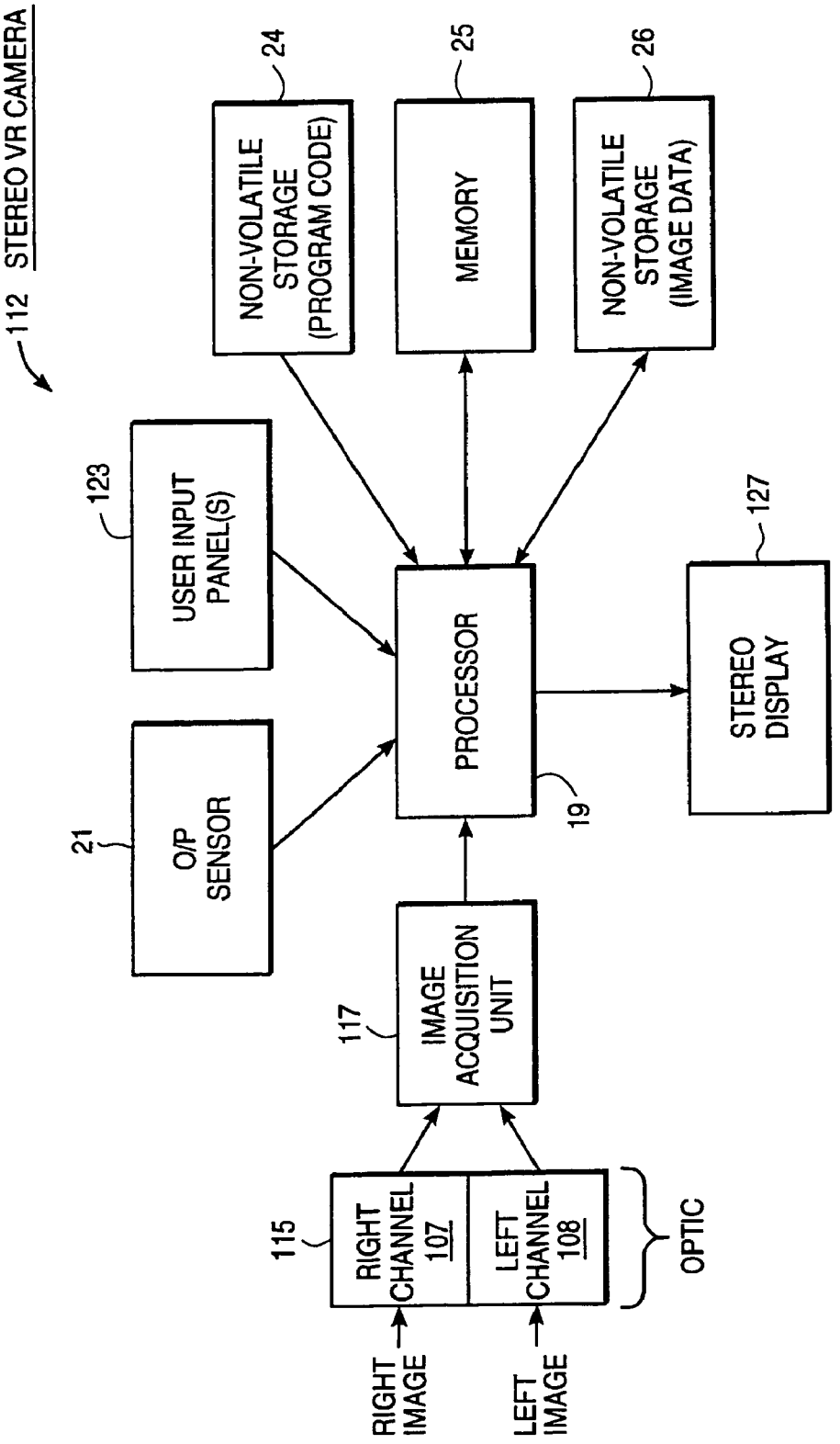

112 STEREO VR CAMERA
24
NON-VOLATILE STORAGE (PROGRAM CODE)
25
MEMORY
26
NON-VOLATILE STORAGE (IMAGE DATA)
123
USER INPUT PANEL(S)
127
STEREO DISPLAY
PROCESSOR
19
21
O/P SENSOR
117
IMAGE ACQUISITION UNIT
115
RIGHT CHANNEL 107
LEFT CHANNEL 108
OPTIC
RIGHT IMAGE
LEFT IMAGE

FIG. 7

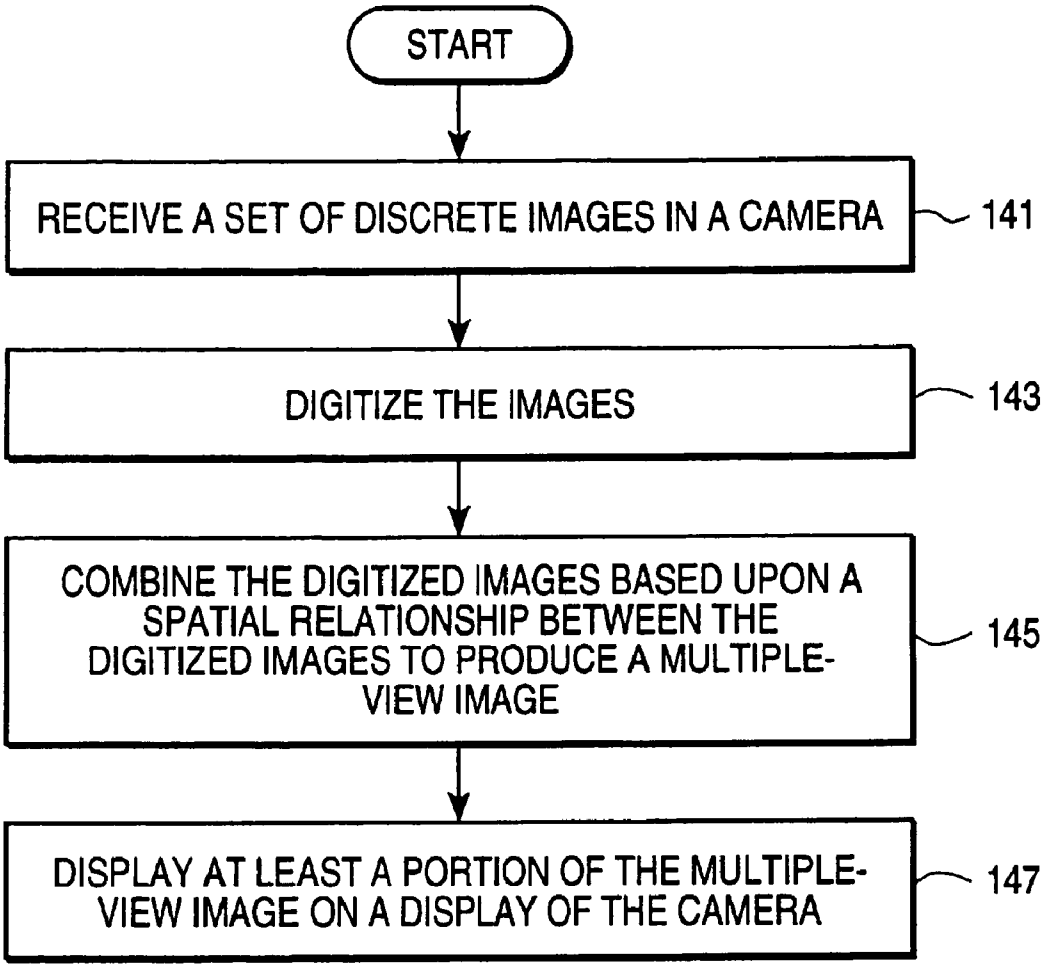

START
RECEIVE A SET OF DISCRETE IMAGES IN A CAMERA
141
DIGITIZE THE IMAGES
143
COMBINE THE DIGITIZED IMAGES BASED UPON A SPATIAL RELATIONSHIP BETWEEN THE DIGITIZED IMAGES TO PRODUCE A MULTIPLE-VIEW IMAGE
145
DISPLAY AT LEAST A PORTION OF THE MULTIPLE-VIEW IMAGE ON A DISPLAY OF THE CAMERA
147

FIG. 8

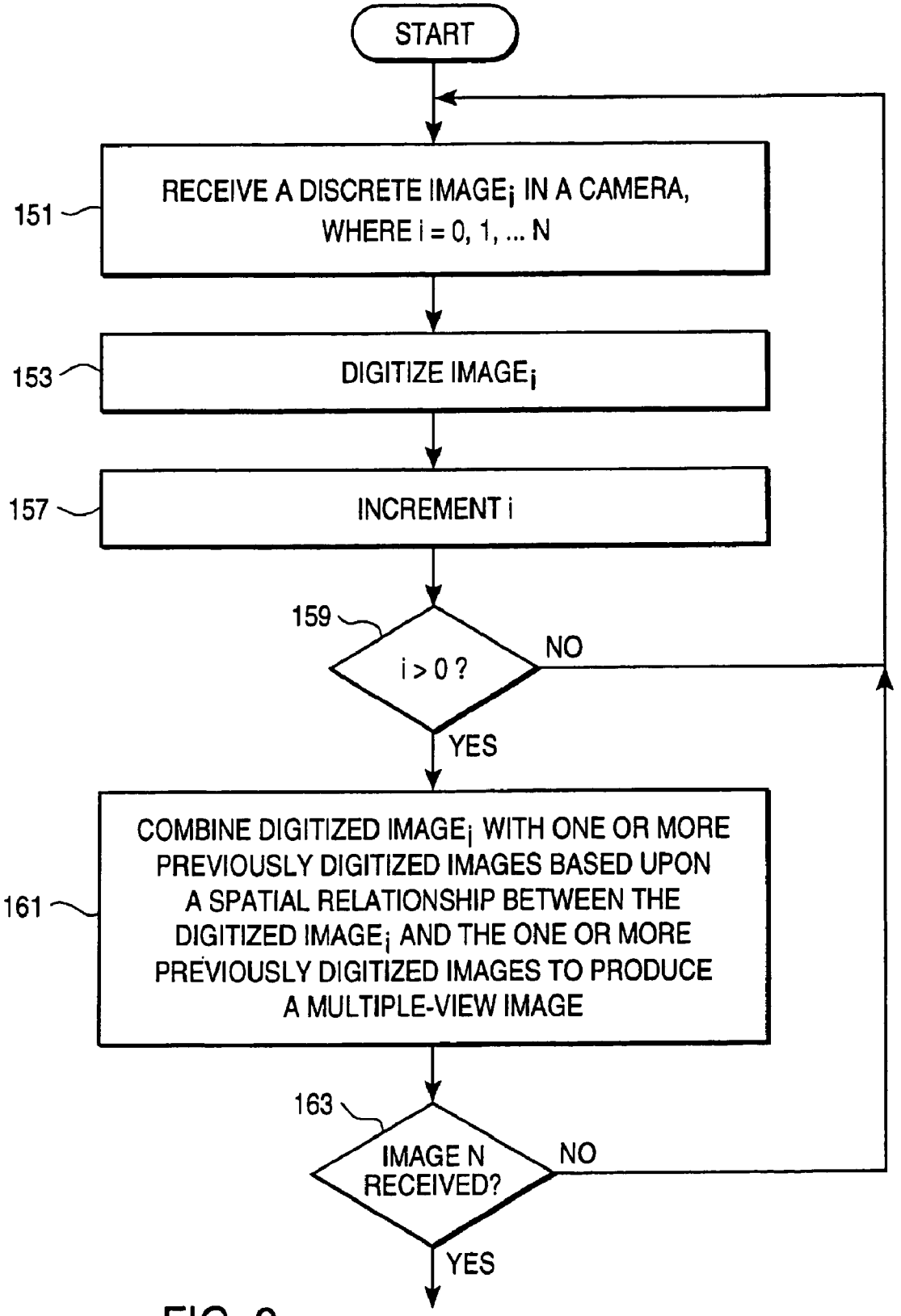

START
RECEIVE A DISCRETE IMAGE$_i$ IN A CAMERA, WHERE i = 0, 1, ... N
151
DIGITIZE IMAGE$_i$
153
INCREMENT i
157
i > 0 ?
159
NO
YES
COMBINE DIGITIZED IMAGE$_i$ WITH ONE OR MORE PREVIOUSLY DIGITIZED IMAGES BASED UPON A SPATIAL RELATIONSHIP BETWEEN THE DIGITIZED IMAGE$_i$ AND THE ONE OR MORE PREVIOUSLY DIGITIZED IMAGES TO PRODUCE A MULTIPLE-VIEW IMAGE
161
IMAGE N RECEIVED?
163
NO
YES

FIG. 9

VIRTUAL REALITY CAMERA

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS-REFERENCE TO RELATED APPLICATION

This patent application is a reissue application for U.S. Pat. No. 6,552,744, issued from U.S. patent application Ser. No. 08/938,366, filed on Sep. 26, 1997.

FIELD OF THE INVENTION

The present invention relates to the field of photography, and more particularly to a camera that combines images based on a spatial relationship between the images.

BACKGROUND OF THE INVENTION

A panoramic image of a scene has traditionally been created by rotating a vertical slit camera about an optical center. Using this technique, film at the optical center is continuously exposed to create a wide field of view (e.g., a 360° field of view). Because of their specialized design, however, vertical slit cameras are relatively expensive. Further, because the panoramic image is captured in a continuous rotation of the camera, it is difficult to adjust the camera to account for changes in the scene, such as lighting or focal depth, as the camera is rotated.

In a more modern technique for creating panoramic images, called "image stitching", a scene is photographed from different camera orientations to obtain a set of discrete images. The discrete images of the scene are then transferred to a computer which executes application software to blend the discrete images into a panoramic image.

After the panoramic image is created, application software may be executed to render user-specified portions of the panoramic image onto a display. The effect is to create a virtual environment that can be navigated by a user. Using a mouse, keyboard, headset or other input device, the user can pan about the virtual environment and zoom in or out to view objects of interest.

One disadvantage of existing image stitching techniques is that photographed images must be transferred from the camera to the computer before they can be stitched together to create a navigable panoramic image. For example, with a conventional exposed-film camera, film must be exposed, developed, printed and digitized (e.g., using a digital scanner) to obtain a set of images that can be stitched into a panoramic image. In a digital camera, the process is less cumbersome, but images must still be transferred to a computer to be stitched into a panoramic view.

Another disadvantage of existing image stitching techniques is that the orientation of the camera used to photograph each discrete image is typically unknown. This makes it more difficult to stitch the discrete images into a panoramic image because the spatial relationship between the constituent images of the panoramic image are determined, at least partly, based on the respective orientations of the camera at which they were captured. In order to determine the spatial relationship between a set of images that are to be stitched into a panoramic image, application software must be executed to prompt the user for assistance, hunt for common features in the images, or both.

Yet another disadvantage of existing image stitching techniques is that it is usually not possible to determine whether there are missing views in the set of images used to create the panoramic image until after the images have been transferred to the computer and stitched. Depending on the subject of the panoramic image, it may be inconvenient or impossible to recreate the scene necessary to obtain the missing view. Because of the difficulty determining whether a complete set of images has been captured, images to be combined into a panoramic image are typically photographed with conservative overlap to avoid gaps in the panoramic image. Because there is more redundancy in the captured images, however, a greater number of images must be obtained to produce the panoramic view. For conventional film cameras, this means that more film must be exposed, developed, printed and scanned to produce a panoramic image than if less conservative image overlap were possible. For digital cameras, more memory must typically be provided to hold the larger number of images that must be captured than if less conservative image overlap were possible.

SUMMARY OF THE INVENTION

A method and apparatus for creating and rendering multiple-view images are disclosed. Images are received on the image sensor of a camera and digitized by sampling logic in the camera. The digitized images are combined by a programmed processor in the camera based upon a spatial relationship between the images.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

FIG. **1** is a block diagram of a virtual reality (VR) camera.

FIG. **2** illustrates the use of a VR camera to generate a panoramic image.

FIG. **3** illustrates the use of a VR camera to generate a composite image of a surface.

FIG. **4** illustrates the use of a VR camera to generate an object image.

FIG. **5** illustrates control inputs on a VR camera according

FIG. **6** illustrates the use of a VR camera to overlay a video feed over a previously recorded scene.

FIG. **7** is a block diagram of a stereo VR camera.

FIG. **8** is a diagram of a method according to one embodiment of the present invention.

FIG. **9** is a diagram of a method according to an alternate embodiment of the present invention.

DETAILED DESCRIPTION

According to the present invention, a virtual reality (VR) camera is provided to create and render panoramic images and other multiple-view images. In one embodiment, the VR camera includes a sensor to detect the camera orientation at which images in a scene are captured. A computer within the VR camera combines the images of the scene into a panoramic image based, at least partly, on the respective camera orientations at which the images were captured. A display in the VR camera is used to view the panoramic image. In one embodiment of the present invention, the orientation of the VR camera is used to select which portion of the panoramic

image is displayed so that a user can effectively pan about the panoramic image by changing the orientation of the camera.

FIG. **1** is a block diagram of a VR camera **12** according to one embodiment of the present invention. VR camera **12** may be either a video camera or a still-image camera and includes an optic **15**, an image acquisition unit (IAU) **17**, an orientation/position sensor (O/P sensor) **21**, one or more user input panels **23**, a processor **19**, a non-volatile program code storage **24**, a memory **25**, a non-volatile data storage **26** and a display **27**.

The optic **15** generally includes an automatically or manually focused lens and an aperture having a diameter that is adjustable to allow more or less light to pass. The lens projects a focused image through the aperture and onto an image sensor in the IAU **17**. The image sensor is typically a charge-coupled device (CCD) that is sampled by sampling logic in the IAU **17** to develop a digitized version of the image. The digitized image may then be read directly by the processor **19** or transferred from the IAU **17** to the memory **25** for later access by the processor **19**. Although a CCD sensor has been described, any type of image sensor that can be sampled to generate digitized images may be used without departing from the scope of the present invention.

In one embodiment of the present invention, the processor **19** fetches and executes program code stored in the code storage **24** to implement a logic unit capable of obtaining the image from the IAU **17** (which may include sampling the image sensor), receiving orientation and position information from the O/P sensor **21**, receiving input from the one or more user input panels **23** and outputting image data to the display **27**. It will be appreciated that multiple processors, or hard-wired logic may alternatively be used to perform these functions. The memory **25** is provided for temporary storage of program variables and image data, and the non-volatile image storage **26** is provided for more permanent storage of image data. The non-volatile storage **26** may include a removable storage element, such as a magnetic disk or tape, to allow panoramic and other multiple-view images created using the VR camera **12** to be stored indefinitely.

The O/P sensor **21** is used to detect the orientation and position of the VR camera **12**. The orientation of the VR camera **12** (i.e., pitch, yaw and roll) may be determined relative to an arbitrary starting orientation or relative to a fixed reference (e.g., earth's gravitational and magnetic fields). For example, an electronic level of the type commonly used in virtual reality headsets can be used to detect camera pitch and roll (rotation about horizontal axes), and an electronic compass can be used to detect camera yaw (rotation about a vertical axis). As discussed below, by recording the orientation of the VR camera **12** at which each of a set of discrete images is captured, the VR camera **12** can automatically determine the spatial relationship between the discrete images and combine the images into a panoramic image, planar composite image, object image or any other type of multiple-view image.

Still referring to FIG. **1**, when a panoramic image (or other multiple-view image) is displayed on display **27**, changes in camera orientation are detected via the O/P sensor **21** and interpreted by the processor **19** as requests to pan about the panoramic image. Thus, by rotating the VR camera **12** in different directions, a user can view different portions of the previously generated panoramic image on the display **27**. The VR camera's display **27** becomes, in effect, a window into a virtual environment that has been created in the VR camera **12**.

In one embodiment of the present invention, the position of the VR camera **12** in a three-dimensional (3D) space is determined relative to an arbitrary or absolute reference. This is accomplished, for example, by including in the O/P sensor **21** accelerometers or other devices to detect translation of VR the camera **12** relative to an arbitrary starting point. As another example, the absolute position of the VR camera **12** may be determined including in the O/P sensor **21** a sensor that communicates with a global positioning system (GPS). GPS is well known to those of ordinary skill in the positioning and tracking arts. As discussed below, the ability to detect translation of the VR camera **12** between image capture positions is useful for combining discrete images to produce a composite image of a surface.

It will be appreciated from the foregoing discussion that the O/P sensor **21** need not include both an orientation sensor and a position sensor, depending on the application of the VR camera **12**. For example, to create and render a panoramic image, it is usually necessary to change the angular orientation of the VR camera **12** only. Consequently, in one embodiment of the present invention, the O/P sensor **21** is an orientation sensor only. Other combinations of sensors may be used without departing from the scope of the to present invention.

Still referring to FIG. **1**, the one or more user input panels **23** may be used to provide user control over such conventional camera functions as focus and zoom (and, at least in the case of a still camera, aperture size, shutter speed, etc.). As discussed below, the input panels **23** may also be used to receive user requests to pan about or zoom in and out on a panoramic image or other multiple-view image. Further, the input panels **23** may be used to receive user requests to set certain image capture parameters, including parameters that indicate the type of composite image to be produced, whether certain features are enabled, and so forth. It will be appreciated that focus and other camera settings may be adjusted using a traditional lens dial instead of an input panel **23**. Similarly, other types of user input devices and techniques, including, but not limited to, user rotation and translation of the VR camera **12**, may be used to receive requests to pan about or zoom in or out on an image.

The display **27** is typically a liquid crystal display (LCD) but may be any type of display that can be included in the VR camera **12**, including a cathode-ray tube display. Further, as discussed below, the display **27** may be a stereo display designed to present left and right stereo images to the left and right eyes, respectively, of the user.

FIG. **2** illustrates use of the VR camera **12** of FIG. **1** to generate a panoramic image **41**. A panoramic image is an image that represents a wide-angle view of a scene and is one of a class of images referred to herein as multiple-view images. A multiple-view image is an image or collection of images that is displayed in user-selected portions.

To create panoramic image **41**, a set of discrete images **35** is first obtained by capturing images of an environment **31** at different camera orientations. With a still camera, capturing images means taking photographs. With a video camera, capturing image refers to generating one or more video frames of each of the discrete images.

For ease of understanding, the environment **31** is depicted in FIG. **2** as being an enclosed space but this is not necessary. In order to avoid gaps in the panoramic image, the camera is oriented such that each captured image overlaps the preceding captured image. This is indicated by the overlapped regions **33**. The orientation of the VR camera is detected via the O/P sensor (e.g., element **21** of FIG. **1**) and recorded for each of the discrete images **35**.

In one still-image camera embodiment of the present invention, as the user pans the camera about the environment

31, the orientation sensor is monitored by the processor (e.g., element 19 of FIG. 1) to determine when the next photograph should be snapped. That is, the VR camera assists the photographer in determining the camera orientation at which each new discrete image 35 is to be snapped by signaling the photographer (e.g., by turning on a beeper or a light) when region of overlap 33 is within a target size. Note that the VR camera may be programmed to determine when the region of overlap 33 is within a target size not only for camera yaw, but also for camera pitch or roll. In another embodiment of the present invention, the VR camera may be user-configured (e.g., via a control panel 23 input) to automatically snap a photograph whenever it detects sufficient change in orientation. In both manual and automatic image acquisition modes, the difference between camera orientations at which successive photographs are acquired may be input by the user or automatically determined by the VR camera based upon the camera's angle of view and the distance between the camera and subject.

In a video camera embodiment of the present invention, the orientation sensor may be used to control the rate at which video frames are generated so that frames are generated only when the O/P sensor indicates sufficient change in orientation (much like the automatic image acquisition mode of the still camera discussed above), or video frames may be generated at standard rates with redundant frames being combined or discarded during the stitching process.

As stated above, the overlapping discrete images 35 can be combined based on their spatial relationship to form a panoramic image 41. Although the discrete images 35 are shown as being a single row of images (indicating that the images were all captured at approximately same pitch angle), additional rows of images at higher or lower pitch angles could also have been obtained. Further, because the VR camera will typically be hand held (although a tripod may be used), a certain amount of angular error is incurred when the scene is recorded. This angular error is indicated in FIG. 2 by the slightly different pitch and roll orientation of the discrete images 35 relative to one another, and must be accounted for when the images are combined to form the panoramic image 41.

After the discrete images 35 have been captured and stored in the memory of the camera (or at least two of the discrete image have been captured and stored), program code is executed in the VR camera to combine the discrete images 35 into the panoramic image 41. This is accomplished by determining a spatial relationship between the discrete images 35 based on the camera orientation information recorded for each image 35, or based on common features in the overlapping regions of the images 35, or based on a combination of the two techniques.

One technique for determining a spatial relationship between images based on common features in the images is to "cross-correlate" the images. Consider, for example, two images having an unknown translational offset relative to one another. The images can be cross-correlated by "sliding" one image over the other image one step (e.g., one pixel) at a time and generating a cross-correlation value at each sliding step. Each cross-correlation value is generated by performing a combination of arithmetic operations on the pixel values within the overlapping regions of the two images. The offset that corresponds to the sliding step providing the highest correlation value is found to be the offset of the two images. Cross-correlation can be applied to finding offsets in more than one direction or to determine other unknown transformational parameters, such as rotation or scaling. Techniques other than cross-correlation, such as pattern matching, can also be used to find unknown image offsets and other transformational parameters.

Based on the spatial relationship between the discrete images 35, the images 35 are mapped onto respective regions of a smooth surface such as a sphere or cylinder. The regions of overlap 33 are blended in the surface mapping. Depending on the geometry of the surface used, pixels in the discrete images 35 must be repositioned relative to one another in order to produce a two-dimensional pixel-map of the panoramic image 41. For example, if the discrete images 35 are mapped onto a cylinder 37 to produce the panoramic image 41, then horizontal lines in the discrete images 35 will become curved when mapped onto the cylinder 37 with the degree of curvature being determined by latitude of the horizontal lines above the cylindrical equator. Thus, stitching the discrete images 35 together to generate a panoramic image 41 typically involves mathematical transformation of pixels to produce a panoramic image 41 that can be rendered without distortion.

FIG. 3 illustrates the use of the VR camera 12 to generate a composite image of a surface 55 that is too detailed to be adequately represented in a single photograph. Examples of such surfaces include a white-board having notes on it, a painting, an inscribed monument (e.g., the Viet Nam War Memorial), and so forth.

As indicated in FIG. 3, multiple discrete images 57 of the surface 55 are obtained by translating the VR camera 12 between a series of positions and capturing a portion of the surface 55 at each position. According to one embodiment of the present invention, the position of the VR camera 12 is obtained from the position sensing portion of the O/P sensor (element 21 of FIG. 1) and recorded for each discrete image 57. This allows the spatial relationship between the discrete images 57 to be determined no matter the order in which the images 57 are obtained. Consequently, the VR camera is able to generate an accurate composite image 59 of the complete surface 55 regardless of the order in which the discrete images 57 are captured. In the case of a still image camera, the position sensor can be used to signal the user when the VR camera 12 has been sufficiently translated to take a new photograph. Alternatively, the VR camera may be user-configured to automatically snap photographs as the VR camera 12 is swept across the surface 55. In the case of a video camera, the position sensor can be used to control when each new video frame is generated, or video frames may be generated at the standard rate and then blended or discarded based on position information associated with each.

After two or more of the discrete images 57 have been stored in the memory of the VR camera 12, program code can be executed to combine the images into a composite image 59 based on the position information recorded for each discrete image 57, or based on common features in overlapping regions of the discrete images 57, or both. After the discrete images 57 have been combined into a composite image 59, the user may view different portions of the composite image 59 on the VR camera's display by changing the orientation of the VR camera 12 or by using controls on a user input panel. By zooming in at a selected portion of the image, text on a white-board, artwork detail, inscriptions on a monument, etc. may be easily viewed. Thus, the VR camera 12 provides a simple and powerful way to digitize and render high resolution surfaces with a lower resolution camera. Composite images of such surfaces are referred to herein as "planar composite images", to distinguish them from panoramic images.

FIG. **4** illustrates yet another application of the VR camera. In this case the VR camera is used to combine images into an object image **67**. An object image is a set of discrete images that are spatially related to one another, but which have not been stitched together to form a composite image. The combination of images into an object image is accomplished by providing information indicating the location of the discrete images relative to one another and not by creating a separate composite image.

As shown in FIG. **4**, images of an object **61** are captured from surrounding points of view **63**. Though not shown in the plan view of the object **61**, the VR camera may also be moved over or under the object **61**, or may be raised or tilted to capture images of the object **61** at different heights. For example, the first floor of a multiple-story building could be captured in one sequence of video frames (or photographs), the second floor in a second sequence of video frames, and so forth. If the VR camera is maintained at an approximately fixed distance from the object **61**, the orientation of the VR camera alone may be recorded to establish the spatial relationship between the discrete images **65**. If the object is filmed (or photographed) from positions that are not equidistant to the object **61**, it may be necessary to record both the position and orientation of the VR camera for each discrete image **65** in order to produce a coherent objec image **67**.

After two or more discrete images **65** of object **61** have been obtained, they can be combined based upon the spatial relationship between them to form an object image **67**. As stated above, combining the discrete images **65** to form an object image **67** typically does not involve stitching the discrete images **65** and is instead accomplished by associating with each of the discrete images **65** information that indicates the image's spatial location in the object image **67** relative to other images in the object image **67**. This can be accomplished, for example, by generating a data structure having one member for each discrete image **65** and which indicates neighboring images and their angular or positional proximity. Once the object image **67** is created, the user can pan through the images **65** by changing the orientation of the camera. Incremental changes in orientation can be used to select an image in the object image **67** that neighbors a previously displayed image. To the user, rendering of the object image **67** in this manner provides a sense of moving around, over and under the object of interest.

According to another embodiment of the present invention, the relative spatial location of each image in the object image **67** an object image is provided by creating a data structure containing the camera orientation information recorded for each discrete image **65**. To select a particular image in the object image **67**, the user orients the VR camera in the direction that was used to capture the image. The VR camera's processor detects the orientation via the orientation sensor, and then searches the data structure to identify the discrete image **65** having a recorded orientation most nearly matching the input orientation. The identified image **65** is then displayed on the VR camera's display.

FIG. **5** depicts a VR camera **12** that is equipped with a number of control buttons that are included in user input panels **23**a and **23**b. The buttons provided in user-input panel **23**a vary depending on whether VR camera **12** is a video camera or a still-image camera. For example, in a still-image camera, panel **23**a may include shutter speed and aperture control buttons, among others, to manage the quality of the photographed image. In a video camera, user input panel **23**a may include, for example, zoom and focus control. User input panel **23**a may also include mode control buttons to allow a user to select certain modes and options associated with creating and rendering virtual reality images. In one embodiment, for example, mode control buttons may be used to select a panoramic image capture mode, planar composite image capture mode or object image capture mode. Generally, any feature of the VR camera that can be selected, enabled or disabled may be controlled using the mode control buttons.

According to one embodiment of the present invention, view control buttons Right/Left, Up/Down and Zoom are provided in user input panel **23**b to allow the user to select which portion of a panoramic image, planar composite image, object image or other multiple-view image is presented on display **27**. When the user presses the Right button, for example, view control logic in the camera detects the input and causes the displayed view of a composite image or object image to pan right. When the user presses the Zoom+button, the view control logic causes the displayed image to be magnified. The view control logic may be implemented by a programmed processor (e.g., element **19** of FIG. **1**), or by dedicated hardware. In one embodiment of the present invention, the view control logic will respond either to user input via panel **23**b or to changes in camera orientation. Alternatively, the camera may be configured such that in one mode, view control is achieved by changing the VR camera orientation, and in another mode, view control is achieved via the user input panel **23**b. In both cases, the user is provided with alternate ways to select a view of a multiple-view image.

FIG. **6** illustrates yet another application of the VR camera **12** of the present invention. In this application, a video signal captured via the IAU (element **17** of FIG. **1**) a is superimposed on a previously recorded scene using a chroma-key color replacement technique. For example, an individual **83** standing in front of a blue background **82** may be recorded using the VR camera **12** to generate a live video signal. Program code in the VR camera **12** may then be executed to implement an overlay function that replaces pixels in a displayed scene with non-blue pixels from the live video. The effect is to place the subject **83** of the live video in the previously generated scene. According to one embodiment of the present invention, the user may pan about a panoramic image on display **27** to locate a portion of the image into which the live video is to be inserted, then snap the overlaid subject of the video image into the scene. In effect, the later received image is made part of the earlier recorded panoramic image (or other multiple-view image) and the combined images can be permanently stored as a single recorded video or still image.

FIG. **7** is a block diagram of a VR camera **112** that is used to receive and process stereo images. As shown, the optic **115** includes both left and right channels (**108**, **107**) for receiving respective left and right images. Typically the left and right images are of the same subject but from spatially differentiated viewpoints. This way a 3D view of the subject is captured. According to one embodiment of the present invention, the left and right images **108** and **107** are projected onto opposing halves of an image sensor in the IAU **117** where they are sampled by the processor **19** and stored in memory **25**. Alternatively, multiple image sensors and associated sampling circuitry may be provided in the IAU **117**. In either case, the left and right images are associated with orientation/position information obtained from the O/P sensor **21** in the manner described above, and stored in the memory **25**. After two or more discrete images have been obtained, the processor may execute program code in the non-volatile code storage **24** to combine the left images into a left composite image and the right images into a right composite image. In an object image application, the processor combines the right and left images into respective right and left object images.

As shown in FIG. **7**, a stereo display **127** is provided to allow a 3D view of a scene to be displayed. For example, a polarized LCD display that relies on the different viewing angles of the left and right eyes of an observer may be used. The different viewing angles of the observer's left and right eyes causes different images to be perceived by the left and right eyes. Consequently, based on an orientation/position of the camera, or a view select input from the user, a selected portion of the left composite image (or object image) is presented to the left eye and a selected portion of the right composite image (or object image) is presented to the right eye.

As with the VR camera **12** described above, live stereo video received in the IAU **117** of the stereo VR camera **112** may be overlaid on a previously generated composite image or object image. The left and right video components of the live stereo video may be superimposed over the left and right composite or object images, respectively. Consequently, the user may view live video subjects in 3D as though they were present in the previously recorded 3D scene. A stereo photograph may also be overlaid on an earlier recorded composite image or object image.

FIG. **8** is a diagram of a method according to one embodiment of the present invention. At step **141**, a set of discrete images are received in the camera. The images are digitized at step **143**. Based upon a spatial relationship between the digitized images, the digitized images are combined to produce a multiple-view image at step **143**. Then, at step **145**, at least a portion of the multiple-view image is displayed on a display of the camera.

It will be appreciated from the foregoing description of the present invention that the steps of receiving (**141**), digitizing (**143**) and combining (**145**) may be performed on an image by image basis so that each image is received, digitized and combined with one or more previously received and digitized images before a next image is received and digitized.

A method of generating of a multiple-view image on a discrete image by discrete image basis shown in FIG. **9**. At step **151**, a discrete $image_i$ is received, where i ranges from 0 to N. At step **153**, image, is digitized, and i is incremented at step **157**. If i is determined to be less than or equal to one at step **159**, execution loops back to step **151** to receive the next discrete $image_i$. If i is greater than one, then at step **161** digitized $image_i$ is combined with one or more previously digitized images based on a spatial relationship between the digitized $image_i$ and the one or more previously digitized images to produce a multiple-view image. If it is determined that a final image has been received and digitized, (arbitrarily shown as N in step **163**) the method is exited. It will be appreciated that the determination as to whether a final image has been received may be made in a number of ways, including: detecting that a predetermined number of images have been received, digitized and combined; or receiving a signal from the user or an internally generated signal indicating that a desired or threshold number of images have been received, digitized and combined into the multiple-view image. Also, according to one embodiment of the present invention, the user may select a portion of the multiple-view image for viewing any time after an initial combining step **159** has been performed.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A hand-held camera comprising:

a camera housing;

a camera lens mounted on said *camera* housing;

image acquisition circuitry located within said camera housing for acquiring images of fields of view via said camera lens at various orientations of said camera housing;

at least one user input panel for receiving a user request to select a panoramic or non-panoramic image capture mode; and

image processing circuitry located within said camera housing; responsive to the panoramic image capture mode selection, for at least partially combining each successively acquired image of a field of a view with previously acquired images of fields of view, on an image by image basis in real time, by determining spatial relationships between the images of fields of view, and by mapping the images of fields of view onto regions of a cylindrical surface, based on the spatial relationships.

2. The hand-held camera of claim **1** wherein said image processing circuitry determines spatial relationships between the images based on at least one feature in images that at least partially overlap.

3. The hand-held camera of claim **1** wherein said image processing circuitry determines spatial relationships between the images based on cross-correlations of images that at least partially overlap.

4. The hand-held camera of claim **1** wherein said image processing circuitry determines spatial relationships between the images based on the orientations of said camera housing during image acquisition.

5. The hand-held **[**cameral**]** *camera* of claim **4** further comprising a sensor for detecting the orientations of said camera housing.

6. The hand-held camera of claim **5** wherein said image acquisition circuitry uses orientation information from said sensor to automatically determine fields of view for which to acquire images thereof.

7. The hand-held camera of claim **1** wherein the camera is a video camera and wherein sampling logic digitizes the images at a predetermined rate.

8. A hand-held camera comprising:

a camera housing;

a camera lens mounted on said *camera* housing;

a display mounted on said camera housing;

image acquisition circuitry located within said **[**cameral**]** *camera* housing for acquiring images of fields of view via said camera lens at various orientations of said camera housing;

image processing circuitry located within said camera housing for at least partially combining each successively acquired image of a field of view with previously acquired images of fields of view, on an image by image basis in real time, by determining spatial relationships between the images of fields of view, and by mapping the images of fields of view onto regions of a cylindrical surface, based on spatial relationships;

at least one user input panel to select a panoramic or non-panoramic image view mode, and to receive a user request to display a spatial region of the cylindrical panoramic image on said display; and

view control circuitry, located within said camera housing and responsive to the panoramic *image* view mode, to

display a spatial region of the cylindrical panoramic image on said display, wherein said view control circuitry selects the spatial region of the cylindrical panoramic image based upon the user request.

9. The hand-held camera of claim **8** wherein said view control circuitry selects the spatial region of the cylindrical panoramic image to be displayed on said display based upon an orientation of said housing.

10. The hand-held camera of claim **9** further comprising a sensor for detecting the orientation of said camera housing.

11. The hand-held camera of claim **8** further comprising a sensor for detecting the orientation of said camera housing.

12. The hand-held camera of claim **8** wherein said user input panel receives user requests to pan about a panoramic image.

13. The hand-held camera of claim **12** wherein said user input panel comprises left, right, up and down buttons.

14. The hand-held camera of claim **12** further comprising a sensor for detecting the orientation of said camera housing.

15. The hand-held camera of claim **8** wherein said user input panel receives user requests to zoom in and out of a panoramic image.

16. The hand-held camera of claim **15** wherein said user input panel comprises zoom in and zoom out buttons.

17. The hand-held camera of claim **15** further comprising a sensor for detecting the orientation of said camera housing.

18. A method for providing cylindrical panoramic images comprising:

selecting a panoramic or non-panoramic image capture mode;

acquiring images of fields of view at various orientations of a camera; and

when the panoramic image capture mode is selected, at least partially combining each successively acquired image of a field of view with previously acquired images of fields of view, on an image by image basis in real time, comprising:

determining spatial relationships between the image of fields of view; and

mapping the images of fields of view onto regions of a cylindrical surface, based on the spatial relationships.

19. The method of claim **18** wherein said determining is based on at least one feature in images that at least partially overlap.

20. The method of claim **18** wherein said determining is based on cross-correlations of images that at least partially overlap.

21. The method of claim **18** wherein said determining is based on the orientations of the **[**cameral**]** *camera* during image acquisitions.

22. The method of claim **21** further comprising detecting the orientation of said camera housing.

23. The method of claim **22** further comprising automatically determining fields of view for which to acquire images thereof, based on detected orientation information.

24. A method for providing cylindrical panoramic images comprising:

acquiring images of fields of view at various orientations of a camera;

at least partially combining each successively acquired image of a field**[**s**]** of view with previously acquired images of fields of view, on an image by image basis in real time, comprising:

determining spatial relationships between the images of fields of view; and

mapping the images of fields of view onto regions of a cylindrical surface, based on the spatial relationships;

selecting a panoramic or non-panoramic image view mode;

when the panoramic image view mode is selected, receiving a user request to display a spatial region of a cylindrical panoramic image; and

displaying the spatial region of the cylindrical panoramic image.

25. The method of claim **24** further comprising selecting the spatial region of the cylindrical panoramic image to be displayed based upon an orientation of the camera.

26. The method of claim **25** further comprising detecting the orientation of said camera housing.

27. A hand-held camera comprising:

a camera housing;

a camera lens mounted on said *camera* housing;

image acquisition circuitry located within said camera housing for acquiring images of fields of view via said camera lens at various orientations of said camera housing;

at least one user input panel for receiving a user request to select a panoramic or non-panoramic image capture mode; and

image processing circuitry located within said camera housing, responsive to the panoramic image capture mode selection, for at least partially combining each successively acquired image of a field of view with previously acquired images of fields of view, on an image by image basis in real time, by determining spatial relationships between the images of fields of view, and by mapping the images of fields of view onto regions of a spherical surface, based on the spatial relationships.

28. The hand-held camera of claim **27** **[**herein**]** *wherein* the camera is a video camera and wherein sampling logic digitizes the images at a predetermined rate.

29. A hand-held camera comprising:

a **[**careen**]** *camera* housing;

a camera lens mounted on said *camera* housing;

image acquisition circuitry located within said camera housing for acquiring images of fields of view via said camera lens at various orientations of said camera housing;

at least one user input panel for receiving a user request to select a panoramic or non-panoramic image capture mode; and

image processing circuitry located within said camera housing, responsive to the panoramic image capture mode selection, for at least partially combining each successively acquired images of a field of view with previously acquired images of fields of view, on an image by image basis in real time, by mapping the image**[**s**]** of fields of view onto regions of a cylindrical surface, based on spatial relationships between the images of fields of view.

30. The hand-held camera of claim **29** wherein the camera is a video camera and wherein sampling logic digitizes the images at a predetermined rate.

31. A hand-held camera comprising:

a camera housing;

a camera lens mounted on said *camera* housing;

image acquisition circuitry located within said camera housing for acquiring images of fields of view via said camera lens at various orientations of said camera housing;

at least one user input panel for receiving a user request to select a panoramic or non-panoramic image capture mode; and

image processing circuitry located within said camera housing, responsive to the panoramic image capture mode selection, for at least partially combining each successively acquired image of a field of view with previously acquired *images of* fields of view, on an image by image basis in real time, by [napping] *mapping* the images of fields of view onto regions of a spherical surface, based on spatial relationships between the images of fields of view.

32. The hand-held camera of claim **31** wherein the camera is a video camera and wherein sampling logic digitizes the images at a predetermined rate.

[**33**. A method for providing spherical panoramic images comprising:

selecting a panoramic or non-panoramic image capture mode;

acquiring images of fields of view at various orientations of a camera; and

when the panoramic image capture mode is selected, at least partially combining each successively acquired image of a field of view with previously acquired images of fields of view, on an image by image basis in real time, comprising:

determining spatial relationships between the images of fields of view; and

mapping the images of fields of view onto regions of a spherical surface, based on the spatial relationships.]

[**34**. A method for providing cylindrical panoramic images comprising:

selecting a panoramic or non-panoramic image capture mode;

acquiring images of fields of view at various orientations of a camera; and

when the panoramic image capture mode is selected, at least partially combining each successively acquired image of a field of view with previously acquired images of fields of view, on an image by image basis in real time, comprising mapping the images of fields of view onto regions of a cylindrical surface, based on spatial relationships between the images of fields of view.]

[**35**. A method for providing spherical panoramic images comprising:

selecting a panoramic or non-panoramic image capture mode;

acquiring images of fields of view at various orientations of a camera; and

when the panoramic image capture mode is selected, at least partially combining each successively acquired image of a field of view with previously acquired image of fields of view, on an image by image basis in real time, comprising mapping the images of fields of view onto regions of a spherical surface, based on spatial relationships between the images of fields of view.]

36. A camera comprising

a housing;

a lens mounted on said housing;

image acquisition circuitry located within said housing for acquiring images of fields of view via said lens at various orientations of said housing;

at least one input panel for receiving a request to select a panoramic or non-panoramic image capture mode; and

image processing circuitry located within said housing and responsive to the panoramic image capture mode selection, for at least partially combining each successively acquired image of a field of a view with previously acquired images of fields of view, on an image-by-image basis in real time, by determining spatial relationships between the images of fields of view, and by mapping the images of fields of view onto regions of a smooth surface, based on the spatial relationships.

37. A camera, comprising:

a housing;

a lens mounted on the housing;

image acquisition circuitry located within the housing for acquiring images of fields of view via the lens at various orientations of the housing;

at least one input panel for receiving a selection of a panoramic or a non-panoramic image capture mode; and

image processing circuitry located within the housing, responsive to the panoramic image capture mode selection for at least partially combining each successively acquired image of a field of a view with at least one previously acquired image of a field of view on an image-by-image basis in real time based at least in part on at least one spatial relationship between the images of fields of view, by mapping the images of fields of view onto regions of a surface based at least in part on at least one spatial relationship.

38. A camera according to claim 37, wherein the image processing circuitry is capable of determining at least one spatial relationship between the images based at least partially on at least one feature in the images that at least partially overlap.

39. The camera according to claim 37, wherein the image processing circuitry is capable of determining at least one spatial relationship between the images based at least partially on a cross-correlation of images that at least partially overlap.

40. The camera according to claim 37, wherein the image processing circuitry is capable of determining at least one spatial relationship between the images based at least partially on an orientation of the housing during image acquisition.

41. The camera according to claim 40, further comprising a sensor capable of detecting an orientation of the housing.

42. The camera according to claim 41, wherein the sensor is capable of detecting at least one of a pitch, yaw and roll orientation of the housing based at least in part on a fixed reference.

43. The camera according to claim 41, wherein the sensor is capable of detecting an orientation of the housing based at least in part on a gravitational field of the earth.

44. The camera according to claim 41, wherein the sensor is capable of detecting an orientation of the housing based at least in part on a magnetic field of the earth.

45. The camera according to claim 41, wherein the sensor is capable of generating orientation information corresponding to a detected orientation of the housing, and

wherein the image acquisition circuitry is capable of using orientation information to automatically determine fields of view for which to acquire images thereof.

46. The camera according to claim 37, wherein the camera comprises a video camera, and

wherein the camera comprises sampling logic capable of digitizing the images.

47. A camera, comprising:

a housing;

a lens mounted on the housing;

a display mounted on the housing;

image acquisition circuitry located within the housing capable of successively acquiring images of fields of view via the lens at various orientations of the camera housing;

image processing circuitry located within the housing capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of a field of view on an image-by-image basis in real time based at least in part on at least one spatial relationship between the images of fields of view by mapping the images of fields of view onto regions of a surface to form a panoramic image based at least in part on spatial relationships;

at least one input panel capable of receiving a panoramic-image view mode selection, and capable of receiving a request to display a selected spatial region of the panoramic image on the display; and

view-control circuitry, located within the housing, capable of displaying the selected spatial region of the panoramic image on the display in response to the panoramic-image view mode selection.

48. The camera according to claim 47, wherein the view control circuitry is capable of enabling a selection of the spatial region of the panoramic image to be displayed on the display based at least in part on an orientation of the housing.

49. The camera according to claim 48, wherein the input panel is capable of receiving a request to pan about a panoramic image.

50. The camera according to claim 49, wherein the input panel comprises left, right, up and down buttons.

51. The camera according to claim 49, wherein the input panel is capable of receiving requests to zoom in and out of a panoramic image.

52. The camera according to claim 51, wherein the input panel comprises zoom in and zoom out buttons.

53. The camera according to claim 47, further comprising a sensor capable of detecting an orientation of the housing.

54. The camera according to claim 53, wherein the sensor is capable of detecting at least one of a pitch, yaw and roll orientation of the housing based at least in part on a fixed reference.

55. The camera according to claim 53, wherein the sensor is capable of detecting the orientation of the housing based at least in part on a gravitational field of the earth.

56. The camera according to claim 53, wherein the sensor is capable of detecting the orientation of the housing based at least in part on a magnetic field of the earth.

57. The camera according to claim 53, wherein the sensor is capable of generating orientation information corresponding to detected orientations of the housing, and

wherein the image acquisition circuitry is capable of using the orientation information to automatically determine fields of view for which to acquire images thereof.

58. A camera, comprising:

a housing;

a lens mounted on the housing;

image acquisition circuitry located within the housing capable of acquiring images of fields of view via the lens at various orientations of the camera housing;

at least one input panel capable of receiving a panoramic-image capture mode selection; and

image processing circuitry located within the housing, responsive to the panoramic-image capture mode selection, capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of a field of view on an image-by-image basis in real time by determining at least one spatial relationship between the images of fields of view, and by mapping the images of fields of view onto regions of a smooth surface based at least in part on at least one spatial relationship.

59. The camera of claim 58, wherein the camera comprises a video camera, and wherein the camera further comprises sampling logic capable of digitizing the images.

60. A camera, comprising:

a housing;

a lens mounted on housing;

image acquisition circuitry located within the housing capable of acquiring images of fields of view via the lens at various orientations of the housing;

at least one input panel capable of receiving a panoramic-image capture mode selection; and

image processing circuitry located within the housing, responsive to the panoramic-image capture mode selection, capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of a field of view on an image-by-image basis in real time by mapping the images of fields of view onto regions of a surface based at least in part on at least one spatial relationship between the images of fields of view.

61. The camera of claim 60, wherein the camera comprises a video camera, and wherein the camera further comprises sampling logic capable of digitizing the images.

62. A camera, comprising:

a camera housing;

a camera lens mounted on the housing;

image acquisition circuitry located within the camera housing for acquiring images of fields of view via the camera lens at various orientations of the camera housing;

at least one input panel capable of receiving a panoramic-image capture mode selection; and

image processing circuitry located within the camera housing, responsive to the panoramic-image capture mode selection capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of a field of view on an image-by-image basis in real time by mapping the images of fields of view onto regions of a surface based at least in part on at least one spatial relationship between the images of fields of view.

63. The camera of claim 62, wherein the camera comprises a video camera, and

wherein the camera further comprises sampling logic capable of digitizing the images.

64. A camera, comprising:

a housing;

a lens mounted on the housing;

means for acquiring images of fields of view via the lens at various orientations of the housing, the means for acquiring the image being located within the housing;

means for receiving a selection of a panoramic or a non-panoramic image capture mode; and

means for processing images located within the housing, the means for processing images responsive to the panoramic image capture mode selection for at least partially combining each successively acquired image of a field of a view with at least one previously acquired image of a field of view on an image-by-image basis in real time based at least in part on at least one spatial relationship between the images of fields of view, and for mapping the images of fields of view onto regions of a surface based at least in part on at least one spatial relationship.

65. A camera according to claim 64, wherein the means for processing images is capable of determining at least one

spatial relationship between the images based at least partially on at least one feature in the images that at least partially overlap.

66. The camera according to claim 64, wherein the means for processing images is capable of determining at least one spatial relationship between the images based at least partially on a cross-correlation of images that at least partially overlap.

67. The camera according to claim 64, wherein the means for processing images is capable of determining at least one spatial relationship between the images based at least partially on an orientation of the housing during image acquisition.

68. The camera according to claim 67, further comprising means for detecting an orientation of the housing.

69. The camera according to claim 68, wherein the means for detecting is further capable of detecting at least one of a pitch, yaw and roll orientation of the housing based at least in part on a fixed reference.

70. The camera according to claim 68, wherein the means for detecting is further capable of detecting an orientation of the housing based at least in part on a gravitational field of the earth.

71. The camera according to claim 68, wherein the means for detecting is further capable of detecting an orientation of the housing based at least in part on a magnetic field of the earth.

72. The camera according to claim 68, wherein the means for detecting is further capable of generating orientation information corresponding to a detected orientation of the housing, and

wherein the means for processing images is further capable of using orientation information to automatically determine fields of view for which to acquire images thereof.

73. The camera according to claim 64, wherein the camera comprises a video camera, and

wherein the camera comprises means for digitizing the images.

74. A camera, comprising:

a housing;

a lens mounted on the housing;

a display mounted on the housing;

means for acquiring images of fields of view via the lens at various orientations of the housing, the means for acquiring images being located within the housing and being capable of successively acquiring images;

image processing circuitry located within the housing capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of a field of view on an image-by-image basis in real time based at least in part on at least one spatial relationship between the images of fields of view by mapping the images of fields of view onto regions of a surface to form a panoramic image based at least in part on spatial relationships;

means for receiving a panoramic-image view mode selection, and capable of receiving a request to display a selected spatial region of the panoramic image on the display; and

means for controlling a display, located within the housing, by displaying the selected spatial region of the panoramic image on the display in response to the panoramic-image view mode selection.

75. The camera according to claim 74, wherein the means for controlling a display is further capable of enabling a selection of the spatial region of the panoramic image to be displayed on the display based at least in part on an orientation of the housing.

76. The camera according to claim 75, wherein the means for receiving a panoramic-image view mode selection is further capable of receiving a request to pan about a panoramic image.

77. The camera according to claim 76, wherein the means for receiving a panoramic-image view mode selection comprises left, right, up and down buttons.

78. The camera according to claim 76, wherein the means for receiving a panoramic-image view mode selection is further capable of receiving requests to zoom in and out of a panoramic image.

79. The camera according to claim 78, wherein the means for receiving a panoramic-image view mode selection comprises zoom in and zoom out buttons.

80. The camera according to claim 74, further comprising means for detecting an orientation of the housing.

81. The camera according to claim 80, wherein the means for detecting an orientation is further capable of detecting at least one of a pitch, yaw and roll orientation of the housing based at least in part on a fixed reference.

82. The camera according to claim 80, wherein the means for detecting an orientation is further capable of detecting the orientation of the housing based at least in part on a gravitational field of the earth.

83. The camera according to claim 80, wherein the means for detecting an orientation is further capable of detecting the orientation of the housing based at least in part on a magnetic field of the earth.

84. The camera according to claim 80, wherein the means for detecting an orientation is further capable of generating orientation information corresponding to detected orientations of the housing, and

wherein the means for acquiring images of fields of view is further capable of using the orientation information to automatically determine fields of view for which to acquire images thereof.

85. A camera, comprising:

means for acquiring images of fields of view at various orientations of a camera;

means for at least partially combining each successively acquired image of fields of view with a previously acquired image of a field of view on an image-by-image basis in real time, comprising:

means for determining at least one spatial relationship between the images of fields of view; and

means for mapping the images of fields of view onto regions of a smooth surface based at least in part on at least one spatial relationship;

means for receiving a request to display a selected spatial region of a panoramic image; and

means for displaying the selected spatial region of the panoramic image.

86. The camera of claim 85, wherein the means for displaying comprises means for displaying the selected spatial region of the panoramic image based at least in part on an orientation of the camera.

87. The camera of claim 86, further comprising means for detecting an orientation of the camera.

88. A camera, comprising:

a housing;

a lens mounted on the housing;

means for acquiring images of fields of view via the lens at various orientations of the camera housing, the means for acquiring being located within the housing;

means for receiving a panoramic-image capture mode selection; and

means for processing images located within the housing, the means for processing images being responsive to the panoramic-image capture mode selection, being capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of a field of view on an image-by-image basis in real time by determining at least one spatial relationship between the images of fields of view, and for mapping the images of fields of view onto regions of a smooth surface based at least in part on at least one spatial relationship.

89. The camera of claim 88, wherein the camera comprises a video camera, and wherein the camera further comprises means for digitizing the images.

90. A camera, comprising:

a housing;

a lens mounted on housing;

means for acquiring images of fields of view via the lens at various orientations of the housing, the means for acquiring being located within the housing;

means for receiving a panoramic-image capture mode selection; and

means for processing images located within the housing, the means for processing images being responsive to the panoramic-image capture mode selection and being capable of at least partially combining each successively acquired image of a field of view with a previously acquired image of field of view on an image-by-image basis in real time by mapping the images of fields of view onto regions of a surface based at least in part on at least one spatial relationship between the images of fields of view.

91. The camera of claim 90, wherein the camera comprises a video camera, and

wherein the camera further comprises means for digitizing the images.

92. A camera, comprising:

a camera housing;

a camera lens mounted on the housing;

means for acquiring images of fields of view via the camera lens at various orientations of the camera housing, the means for acquiring images being located within the camera housing;

means for receiving a panoramic-image capture mode selection; and

means for processing images located within the camera housing, the means for processing images being responsive to the panoramic-image capture mode selection and being capable of at least partially combining each successively acquired image of a field of view with a previously acquired field of view on an image-by-image basis in real time by mapping the images of fields of view onto regions of a surface based at least in part on at least one spatial relationship between the images of fields of view.

93. The camera of claim 92, wherein the camera comprises a video camera, and wherein the camera further comprises means for digitizing the images.

94. A camera comprising:

a camera housing;

a camera lens mounted on said housing;

image acquisition circuitry located within said camera housing to acquire images via said camera lens at at least two orientations of said camera housing;

means for selecting a panoramic image capture mode;

image processing circuitry located within said camera housing, responsive to the selection of the panoramic image capture mode, to at least partially combine at least one successively acquired image with at least one previously acquired image by mapping the images onto regions of a cylindrical surface wherein the mapping is based, at least in part, on one or more spatial relationships between the images as determined on an image-by-image basis in real time; and

a sensing element adapted to determine when a next image in said panoramic image capture mode is to be acquired based in response to detection of at least an orientation of said camera.

95. The camera of claim 94, wherein said orientation of the camera includes at least one orientation selected from the group consisting of a pitch, roll and yaw, all of said camera.

96. The camera of claim 94, wherein said sensing element includes means for generating a signal to indicate that said next image is to be acquired.

97. The camera of claim 96, wherein said signal includes at least one of an audio signal or a visible signal.

98. The camera of claim 94 wherein said sensing element determining is further adapted to determine when said next image is to be acquired based at least in part on an angle of view of the camera and a distance between the camera and a subject in successive images.

99. The camera of claim 94, further including means for collecting image information for each acquired image and for associating said image information for each acquired image with that image, said image information including a spatial location of an acquired image at least relative to spatial locations of other acquired images.

100. The camera of claim 99, wherein the collecting means is further adapted to generate a data structure associated with acquired images of a panorama, the data structure including a data member for each acquired image in the panorama, and each data member identifying at least one neighboring image to the acquired image represented by the data member and said data member including information representing camera orientation.

101. The camera of claim 100, wherein the data member further includes a spatial location of said image in said panorama relative to other images acquired for said panorama.

102. The camera of claim 101, wherein said spatial location of said image is represented by at least an angular and positional proximity to at least one of said other acquired images.

103. A method for providing cylindrical panoramic images comprising:

sensing selection of a panoramic image capture mode;

acquiring images at various orientations of a camera;

responsive to said selection of said panoramic image capture mode, at least partially combining at least one successively acquired image with one or more previously acquired images, on an image-by-image basis in real time, comprising:

determining spatial relationships between the images; and

mapping the images onto regions of a cylindrical surface, based on the spatial relationships; and

sensing an orientation of said camera to determine when a next image in said panoramic image capture mode is to be acquired based at least in part on a camera orientation.

104. The method of claim 103, wherein said orientation of the camera includes at least one orientation selected from the group consisting of a pitch, roll and yaw, all of said camera.

105. The method of claim 103, further comprising generating a signal to indicate that said next image is to be acquired.

106. The method of claim 105, wherein said signal includes at least one of an audio signal or a visible signal.

107. The method of claim 103 wherein said sensing to determine is further based at least in part on an angle of view of the camera and a distance between the camera and a subject in successive images.

108. The method of claim 103, further comprising collecting image information for each acquired image, and associating said image information for each acquired image with that image, said image information including a spatial location of an acquired image at least relative to spatial locations of other acquired images.

109. The method of claim 108, further comprising generating a data structure associated with acquired images of a panorama, the data structure including a data member for each acquired image in the panorama, and each data member identifying at least one neighboring image to the acquired image represented by the data member and said data member including information representing camera orientation.

110. The method of claim 108, wherein the data member further includes a spatial location of said image in said panorama relative to other images acquired for said panorama.

111. The method of claim 110, wherein said spatial location of said image is represented by at least an angular and positional proximity to at least one of said other acquired images.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE43,700 E
APPLICATION NO. : 11/113455
DATED : October 2, 2012
INVENTOR(S) : Chen

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page, in Item (56), under "OTHER PUBLICATIONS", in Column 2, Line 1, delete "J." and insert -- J., --, therefor.

On the Title Page, in Item (56), under "OTHER PUBLICATIONS", in Column 2, Line 8, delete "B." and insert -- B., --, therefor.

In the Specification

In Column 2, Line 46, after "according", insert -- to a preferred embodiment of the present invention --.

In Column 4, Line 3, delete "VR the" and insert -- the VR --, therefor.

In Column 4, Line 6, after "determined", insert -- by --, therefor.

In Column 4, Line 21, delete "the to" and insert -- the --, therefor.

In Column 4, Line 28, delete "on" and insert -- of --, therefor.

In Column 4, Line 39, delete "on" and insert -- of --, therefor.

In Column 5, Line 33, after "approximately", insert -- the --.

In Column 5, Line 45, delete "image" and insert -- images --, therefor.

In Column 6, Line 16, delete "latitude" and insert -- the latitudes --, therefor.

In Column 7, Line 25, delete "objec" and insert -- object --, therefor.

Signed and Sealed this
Thirteenth Day of August, 2013

Teresa Stanek Rea

Teresa Stanek Rea
Acting Director of the United States Patent and Trademark Office

In the Specification (cont'd.)

In Column 7, Line 47, delete "an object image".

In Column 8, Line 30, after "FIG. 1)", delete "a".

In Column 8, Lines 39-46, delete "According to one embodiment of the present invention, the user may pan about a panoramic image on display 27 to locate a portion of the image into which the live video is to be inserted, then snap the overlaid subject of the video image into the scene. In effect, the later received image is made part of the earlier recorded panoramic image (or other multiple-view image) and the combined images can be permanently stored as a single recorded video or still image." and insert the same as a new paragraph at Line 40.

In Column 9, Line 29, delete "step 143." and insert -- step 145. --, therefor.

In Column 9, Line 29, delete "step 145," and insert -- step 147, --, therefor.

In Column 9, Line 40, after "basis", insert -- is --.

In Column 9, Line 43, delete "one" and insert -- zero --, therefor.

In Column 9, Line 45, delete "one," and insert -- zero, --, therefor.

In Column 9, Line 61, delete "step 159" and insert -- step 161 --, therefor.

In the Claims

In Column 13, Line 54, in Claim 36, delete "comprising" and insert -- comprising: --, therefor.

In Column 14, Line 23, in Claim 38, delete "A camera" and insert -- The camera --, therefor.

In Column 16, Line 36, in Claim 62, delete "selection" and insert -- selection, --, therefor.

In Column 16, Line 66, in Claim 65, delete "A camera" and insert -- The camera --, therefor.

EXHIBIT C

US006221686B1

(12) **United States Patent**
Drowley et al.

(10) **Patent No.: US 6,221,686 B1**
(45) **Date of Patent: Apr. 24, 2001**

(54) **METHOD OF MAKING A SEMICONDUCTOR IMAGE SENSOR**

(75) Inventors: **Clifford I. Drowley**, Phoenix; **Mark S. Swenson**, Higley; **Jennifer J. Patterson**, Mesa; **Shrinath Ramaswami**, Gilbert, all of AZ (US)

(73) Assignee: **Motorola, Inc.**, Schaumburg, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/493,366**

(22) Filed: **Jan. 28, 2000**

Related U.S. Application Data

(62) Division of application No. 08/970,720, filed on Nov. 14, 1997, now Pat. No. 6,023,081.

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/57**; 438/66; 438/69; 438/72; 438/73; 257/290; 257/292; 257/293

(58) **Field of Search** 438/57, 66, 69, 438/72, 73; 257/290, 292, 293, 233

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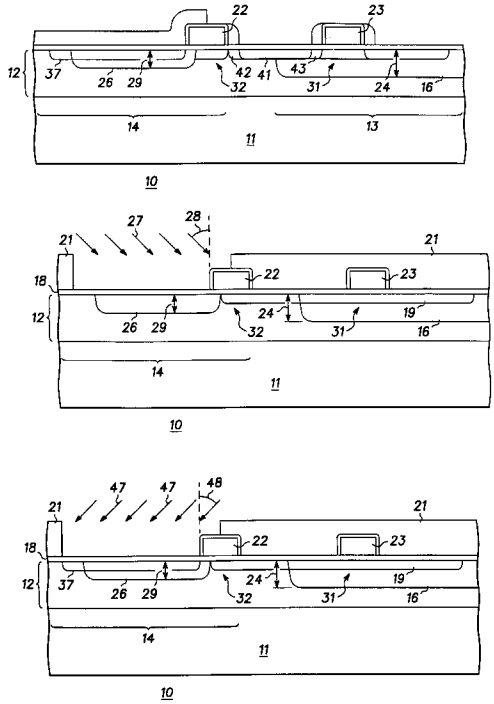
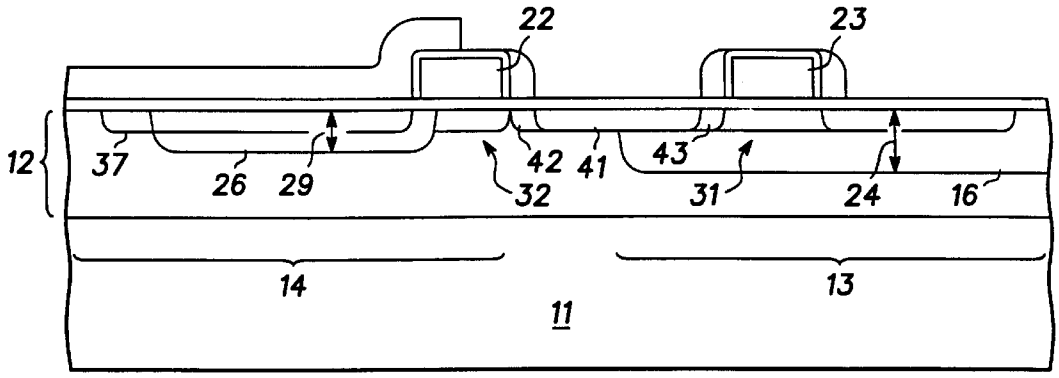
Primary Examiner—Charles Bowers
Assistant Examiner—Erik J. Kielin
(74) *Attorney, Agent, or Firm*—A. Kate Huffman

(57) **ABSTRACT**

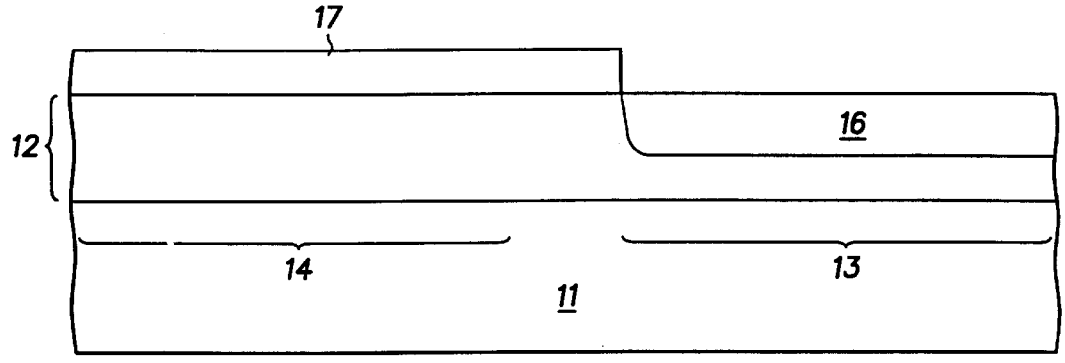
An image sensor **(10)** has an image sensing element that includes an N-type conducting region **(26)** and a P-type pinned layer **(37)**. The two regions form two P-N junctions at different depths that increase the efficiency of charge carrier collection at different frequencies of light. The conducting region **(26)** is formed by an angle implant that ensures that a portion of the conducting region **(26)** can function as a source of a MOS transistor **(32)**.

34 Claims, 3 Drawing Sheets

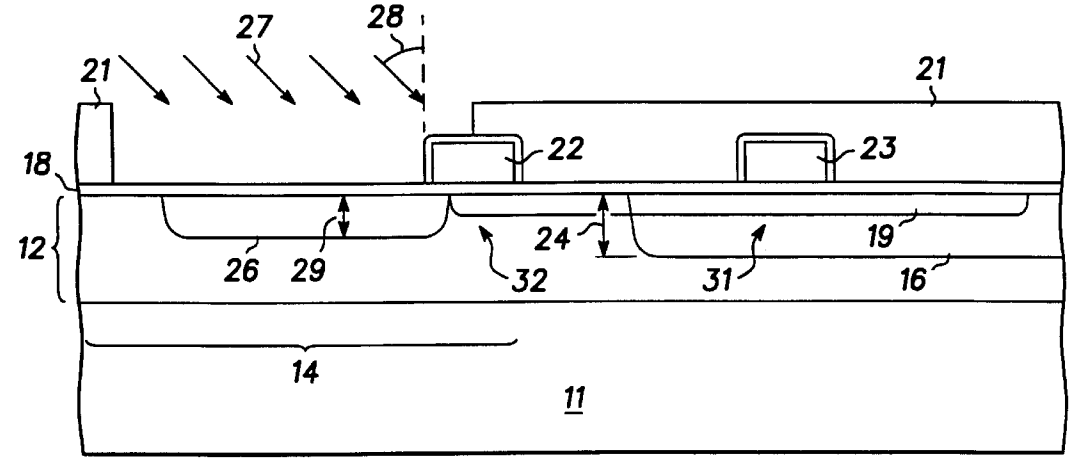




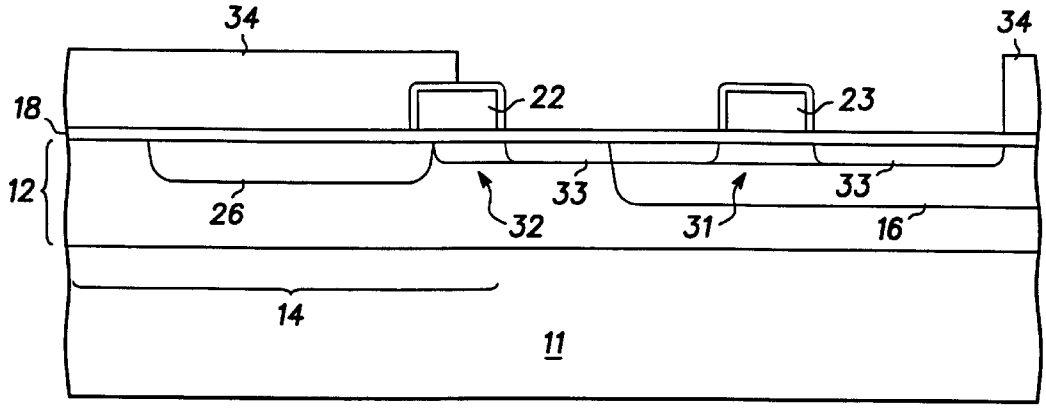
10 FIG. 1



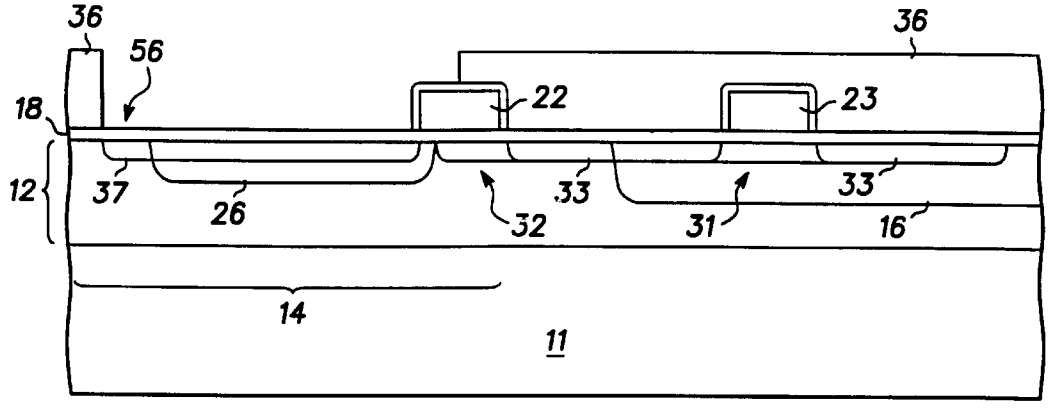
10 FIG. 2



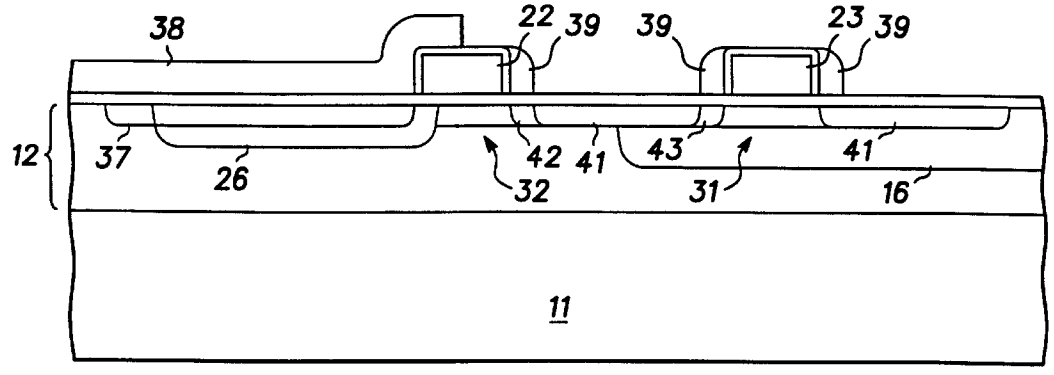
10 FIG. 3



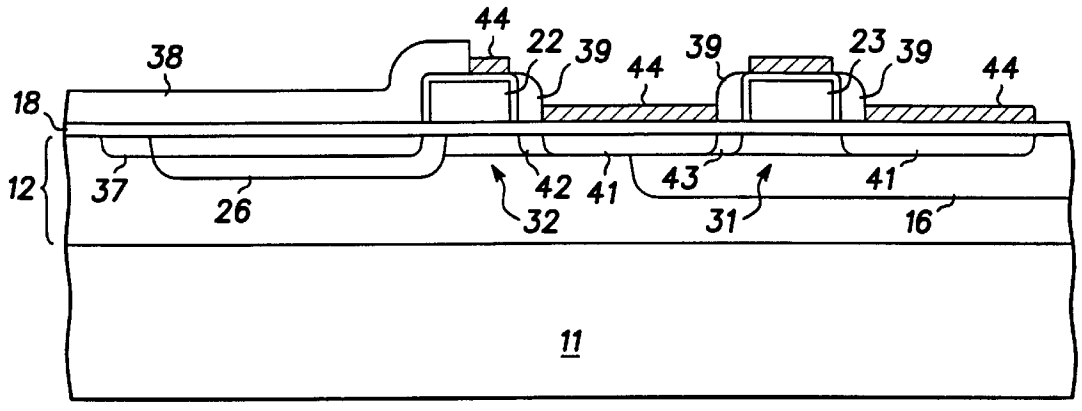
10 FIG. 4



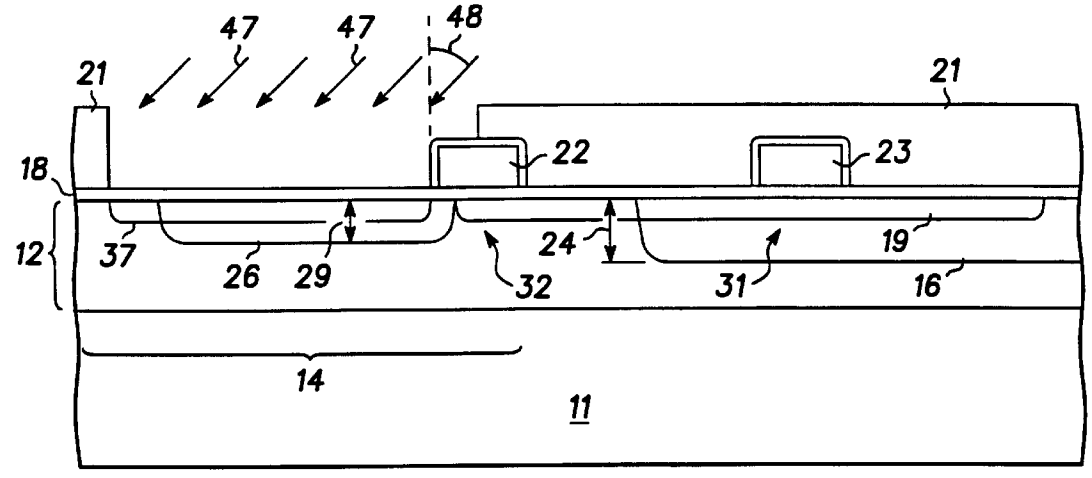
10 FIG. 5



10 FIG. 6



10 FIG. 7



10 FIG. 8

METHOD OF MAKING A SEMICONDUCTOR IMAGE SENSOR

This application is a division of application Ser. No. 08/970,720 filed Nov. 14, 1997, now U.S. Pat. No. 6,023,081.

BACKGROUND OF THE INVENTION

This application is related to an application entitled CMOS IMAGE SENSOR by Michael Guidash filed on the same day as the instant application, and an application entitled METHOD OF FORMING A SEMICONDUCTOR IMAGE SENSOR AND STRUCTURE by Drowley et al and filed concurrently herewith.

This invention relates, in general, to semiconductor devices, and more particularly to a semiconductor image sensor.

In the past, a variety of methods were used to form semiconductor image sensors on a substrate with complementary metal oxide semiconductor (CMOS) devices. Typically, the optical receiving portion of the sensor is formed either as a gate of a large area transistor, often referred to as a photo-gate, or as a source-drain junction of a metal oxide semiconductor (MOS) transistor. The photo-gate transistor implementation requires that light travel through the silicon gate of the transistor in order to convert light to electrical energy. Consequently, the photo-gate implementation has reduced sensitivity. Additionally, the depletion region generally is shallow (less than one micron) thereby reducing the collection efficiency of carriers induced by red light absorption. Also conventional photo-gate implementations are susceptible to noise created by surface recombination.

The source-drain junction implementation generally has a junction that is optimized for transistor operation and therefor also has a shallow junction that results in inefficient collection of carriers induced by red light. Another disadvantage of the source-drain junction implementation is that the junction typically is formed in a highly doped (greater than 10^{16} atoms/cm^3) region that limits the width of the junction depletion region thereby further reducing the collection efficiency of carriers induced by red light absorption. Furthermore, forming the junction in such a highly doped region results in a large capacitance that reduces the amount of charge that can be transferred from the photo sensing element to other electronics.

Traditional CMOS image sensor implementations often form a silicide layer over the image sensing element thereby further reducing sensitivity.

Accordingly, it is desirable to have an image sensor that does not utilize a photo-gate thereby resulting in higher efficiency, that does not have a shallow junction depth thereby increasing efficiency, that minimizes noise from surface recombination, that does not use a silicide overlying the light sensing area thereby further increasing efficiency, that has a wide depletion region for further increasing of carrier conversion for all wavelengths of light, and that does not have a large capacitance that minimizes the charge transferred from the image sensing element to other electronics.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an enlarged cross-sectional portion of an image sensor embodiment in accordance with the present invention;

FIG **2** illustrates an enlarged cross-sectional portion of the FIG. **1** embodiment at a manufacturing stage in accordance with the present invention;

FIGS. **3–7** illustrate enlarged cross-sectional portions of the FIG. **1** embodiment at a subsequent manufacturing stages in accordance with the present invention; and

FIG. **8** illustrates an enlarged cross-sectional portion of an alternate embodiment of an image sensor in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an enlarged cross-sectional portion of a semiconductor image sensor **10**. Sensor **10** includes an underlying P-type substrate formed by a semiconductor substrate **11** and an enhancement layer **12** formed thereon. Sensor **10** has a first well or P-type well **16** formed in a first portion **13** of the underlying substrate. Well **16** typically has a doping concentration that is higher than the doping concentration in a second portion **14** of the underlying substrate's layer **12**. Portions **13** and **14** of layer **12** are identified by a brackets shown below layer **12**. This second portion of layer **12** forms a second well within the underlying substrate. The surface doping concentration of well **16** typically is at least 1×10^{16} atoms/cm^3. A first depth or depth **24** of well **16** typically is less than the depth of layer **12** and typically is about two to four microns in order to facilitate forming other CMOS devices on substrate **11**.

The image capturing or light sensing element of sensor **10** includes an N-type conducting region **26** that is formed in the second well or second portion **14**. Conducting region **26** forms a first P-N junction with the P-type material of the underlying substrate. This first P-N junction is positioned at a second depth or depth **29** of conducting region **26** in order to readily sense light in the red wavelengths and typically is less than approximately 0.7 microns, and preferably about 0.5 microns, from the surface of the underlying substrate. A P-type pinning layer **37** is formed within region **26** and extends outward from region **26** into layer **12** of the underlying substrate in order to form an electrical connection with the underlying substrate. This electrical connection pins the potential applied to this element of the image sensor. Consequently, the resulting photodiode is often referred to as a pinned photodiode. A second P-N junction is formed along the intersection of layer **37** and region **26**. Typically layer **37** is formed simultaneously with the formation of lightly doped drain and source regions of other P-channel MOS transistors (not shown) on substrate **11**. The depth of the second P-N junction is less than that of the first P-N junction. This depth is selected to optimize the absorption or sensing of light in the blue wavelengths. A transfer transistor or first MOS transistor **32** is formed adjacent to conducting region **26** so that a portion of region **26** forms a source of transistor **32**. A second or reset MOS transistor **31** is formed within well **16**. Transistor **31** has a source that is electrically coupled to transistor **32** by a coupling region **41**.

Conducting region **26** is formed by applying a mask having an opening that exposes some of the surface of portion **14** extending up to and including a portion of a gate **22** of transistor **32**. Then dopants are implanted at an angle away from perpendicular to substrate **11** and toward gate **22** to ensure that region **26** extends under gate **22**, thereby saving masking and other processing operations in forming region **26** and the source of transistor **32**.

FIG. **2** illustrates an enlarged cross-sectional portion of a stage in an embodiment of manufacturing sensor **10** shown in FIG. **1**. Sensor **10** includes a heavily doped P-type

substrate **11** having a lightly doped P-type enhancement layer **12** formed thereon. Typically, substrate **11** has a first or P-type doping concentration of at least 1×10^{16}, and preferably 1×10^{18}, atoms/cm^3 and layer **12** has a P-type doping concentration no greater than approximately 1×10^{15} atoms/cm^3. Additionally, layer **12** includes first portion **13** in which first well or P-well **16** is formed, and second well or second portion **14** in which the light sensing element of sensor **10** will be formed. Forming the light sensing elements in lightly doped second portion **14** that overlies more heavily doped substrate **11** enhances carrier collection in the light sensing element.

P-type well **16** is formed by applying a mask **17** to expose the surface of first portion **13** of layer **12**. Dopants are formed within the exposed surface to form well **16**. After forming well **16**, mask **17** is removed.

FIG. **3** illustrates an enlarged cross-sectional portion of sensor **10** shown in FIGS. **1** and **2** at a subsequent formation stage. Like elements in FIGS. **1**, **2**, and **3** have the same element numbers. A gate oxide **18** is formed across the surface of sensor **10**. Thereafter, a channel doping region **19** is formed to facilitate creating channels for MOS transistors **31** and **32**. Gates **23** and **22** are formed on oxide **18** to facilitate the formation of transistors **31** and **32**, respectively.

Thereafter, a mask **21** is applied to expose the area of second portion **14** in which conducting region **26** is to be formed. Mask **21** has an opening that exposes a portion of the surface of gate oxide **18** in second portion **14** the exposed portion extends from an edge of gate **22** into second portion **14**, and also exposes a portion of gate **22**. Dopants, illustrated by arrows **27**, are implanted at an angle **28** toward gate **22**. Angle **28** is measured away from a line normal to the surface of sensor **10**. Angle **28** typically is greater than fifteen degrees, and preferably is at least twenty five degrees, from normal to the surface of sensor **10**. This angle implant is used to ensure that region **26** extends slightly under gate **22** to facilitate utilizing a portion of region **26** to function as the source of transistor **32**, thereby connecting the channel of transistor **32** to conducting region **26**. Subsequent to forming region **26**, mask **21** is removed.

Alternately, two different implants can be utilized to form region **26**. A high energy implant, for example 120–190 keV, can be used near normal to the surface of sensor **10** in order to form region **26** deep within layer **12**. Thereafter a lower energy implant, for example 90–130 keV, can be formed at an angle substantially equal to angle **28** and at a low energy to ensure that a portion of region **26** extends under gate **22**.

FIG. **4** represents a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, and **4** are represented by the same element numbers. A mask **34** is applied with an opening that exposes the areas for forming the drain of transistor **32**, and the source and drain of transistor **31**. Thereafter, source-drain dopants **33** are formed in layer **12** using the edges of gates **22** and **23** as masks to self-align the source and drain areas to gates **22** and **23**. Thereafter, mask **34** is removed.

FIG. **5** illustrates an enlarged cross-sectional portion of a subsequent stage in forming sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, **4**, and **5** are represented by the same element numbers. A mask **36** is applied having an opening that exposes an edge of gate **22**, the surface of conducting region **26**, and an area **56**, shown by an arrow, extending past region **26**. P-type dopants are formed in the exposed surface to form P-type pinning layer **37** within the exposed portion of region **26** and extending outward from region **26** into area **56** and away from transistor **32**. The depth and doping concentration of layer **37** are chosen to facilitate transferring all photo induced charge from region **26** to the drain of transistor **32**. Typically, layer **37** has a depth of approximately 0.2 to 0.3 microns and a surface doping concentration greater than approximately 5×10^{17} atoms/cm^3. Subsequent to forming layer **37**, mask **36** is removed.

FIG. **6** illustrates a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, **4**, **5**, and **6** are represented by the same element numbers. A dielectric material is applied to the surface of sensor **10** and is patterned to form spacers **39** on the sidewalls of gates **22** and **23**, and to form a dielectric covering **38** overlying the light sensing element of sensor **10**. Covering **38** typically extends onto gate **22** to form a mask for subsequent operations. The material used to form spacers **39** and covering **38** is chosen to have a dielectric constant between the dielectric constant of the underlying substrate and any material overlying covering **38**. The dielectric constant of covering **38** chosen in order to minimize reflections between the underlying semiconductor material and any other dielectric or material placed on top of covering **38**. For example, the material of covering **38** can be silicon nitride having a thickness of thirty to seventy nanometers in order to minimize reflections for light between the blue and red spectrums. Additionally, thickness of one hundred thirty to two hundred nanometers will also perform properly. Other materials such as aluminum oxide and aluminum nitride are also believed to be suitable materials for forming covering **38** and spacers **39**.

Subsequently, spacers **39** and covering **38** are used as masks to form N-type dopants in layer **12** that result in forming coupling region **41** electrically connecting drain **42** and source **43**.

FIG. **7** illustrates a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1–7** are represented by the same element numbers. A low resistance material is applied to minimize the resistance of contacts made to both coupling region **41** and gates **22** and **23**. Typically, titanium is blanket deposited across sensor **10** and then annealed to form titanium silicide with any exposed underlying silicon material. Consequently, layer **38** prevents forming a silicide overlying the photo-diode formed by region **26** and layer **37**. The remaining titanium that does not form titanium silicide is removed thereby leaving low resistance contact materials **44** on gates **22**, **23**, and coupling region **41**. Such formation techniques are well known to those skilled in the art. Generally, an interlayer dielectric, not shown, is formed over sensor **10** and contacts made to appropriate portions thereof.

FIG. **8** illustrates an alternate embodiment for forming pinned layer **37** of sensor **10**. Subsequent to forming conducting region **26** as discussed in FIG. **3**, layer **37** can be formed by performing an implant at an angle opposite to angle **28** shown in FIG. **3**. In this embodiment, dopants, represented by arrows **47**, are implanted away from gate **22** at an angle **48** from normal to the surface of sensor **10**. Typically, angle **48** is between ten and twenty five degrees to ensure that a portion of layer **37** extends outward from region **26** away from transistor **32**. This portion of layer **37** is utilized to form contact with enhancement layer **12**. For some processing sequences, this alternate embodiment can reduce the number of processing operations.

By now it should be appreciated that there has been provided a novel image sensor and method therefor. Forming the image sensor in a lightly doped region that overlies a more heavily doped region enhances carrier collection. Forming a deep conducting region and a shallower pinned layer forms two P-N junctions where one P-N junction, and

the associated depletion region, is deep to facilitate capturing light in the red wavelengths and a second P-N junction, and the associated depletion region, is shallow facilitating capturing blue wavelength light. This structure also minimizes surface recombination and maximizes charge transfer. Using an angled implant to form the conducting region ensures the conducting region can be used as a source of a charge transfer transistor thereby minimizing manufacturing operations. Utilizing a dielectric material having a dielectric constant between the dielectric constant of the underlying substrate and overlying material minimizes reflections and enhances efficiency of the sensor. Ensuring that the light sensing element is devoid of an overlying silicide material also improves the efficiency of the sensor.

What is claimed is:

1. A method of forming an image sensor comprising:

providing a semiconductor substrate of a first conductivity type;

forming an enhancement layer on the substrate, the enhancement layer having the first conductivity type and a first doping concentration;

forming a first well on a first portion of the enhancement layer, the first well having the first conductivity type and a second doping concentration that is greater than the first doping concentration wherein the first well has a first depth into the enhancement layer;

forming a conducting region of a second conductivity type in a second portion of the enhancement layer wherein a first portion of the conducting region forms a portion of a MOS transistor; and

forming a pinned layer of the first conductivity type in the second region of the enhancement layer by forming a first portion of the pinned layer within the conducting region and a second portion of the pinned layer extending laterally from the conducting region in a direction away from the MOS transistor.

2. The method of claim **1** wherein providing the substrate includes providing the substrate with a third doping concentration greater than the first and second doping concentrations.

3. The method of claim **1** wherein forming the conducting region includes implanting a first dopant at a first angle from normal to the substrate and angled toward the MOS transistor.

4. The method of claim **3** wherein implanting the first dopant at the first angle includes using an angle of at least fifteen degrees.

5. The method of claim **3** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

6. The method of claim **5** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

7. The method of claim **3** wherein the steps of forming the conducting region and forming the pinned layer of the first conductivity type includes implanting the conducting region by implanting the first dopant at the first angle away from normal to the substrate and toward the MOS transistor and implanting the pinned layer at a second angle away from normal to the substrate and away from the MOS transistor.

8. The method of claim **7** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

9. The method of claim **8** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

10. The method of claim **1** wherein forming the conducting region includes forming the conducting region to a depth less than 0.7 microns.

11. The method of claim **1** wherein forming the first well includes forming the first well to a first depth no greater than a depth of the enhancement layer.

12. The method of claim **1** further including forming a dielectric layer overlying the pinned layer, and forming a silicide layer on a portion of the image sensor wherein an area overlying the pinned layer is devoid of the silicide layer.

13. The method of claim **1** further including forming a dielectric layer overlying the pinned layer wherein the dielectric layer has a dielectric constant that is between a dielectric constant of any material overlying the dielectric layer and a dielectric constant of an underlying substrate on which the pinned layer is formed.

14. A method of forming an image sensor comprising:

using an implant at a first angle to form a conducting region of the image sensor; and forming a pinned layer at least partially within the conducting region.

15. The method of claim **14** further including using a substrate of a first doping concentration, and forming an enhancement layer on the substrate, the enhancement layer having a doping concentration that is less than the first doping concentration wherein the conducting region is formed in the enhancement layer.

16. The method of claim **14** further including forming the pinned layer by implanting at a second angle.

17. The method of claim **14** further including forming a dielectric layer overlying the pinned layer, and forming a silicide layer on a portion of the image sensor wherein an area overlying the pinned layer is devoid of the silicide layer.

18. The method of claim **14** further including forming a dielectric layer overlying the pinned layer wherein the dielectric layer has a dielectric constant that is between a dielectric constant of any material overlying the dielectric layer and a dielectric constant of an underlying substrate on which the pinned layer is formed.

19. A method of forming an active pixel sensor comprising:

providing a semiconductor substrate of a first conductivity type;

forming an enhancement layer on the substrate, the enhancement layer having the first conductivity type and a first doping concentration;

forming a first well on a first portion of the enhancement layer, the first well having the first conductivity type and a second doping concentration that is greater than the first doping concentration wherein the first well has a first depth into the enhancement layer;

forming at least one MOS transistor in the first well in the first portion; and

providing a pinned photodiode in a second portion of the enhancement layer, the pinned photodiode having a first P-N junction at a first depth from the surface, a second P-N junction at a second depth that is less than the first depth, and a conducting region of the second conductivity type between the first depth and the second depth; and

forming at least one MOS transistor in the second portion of the enhancement layer, such that the pinned photodiode forms a portion of the MOS transistor in the second portion, and a gate of the MOS transistor in the second portion is within the second portion and a drain of the MOS transistor is within the first portion and the second portion.

20. The method of claim **19** wherein the step of forming the portion of the MOS transistor in the second portion of the enhancement layer such that the portion of the MOS transistor formed from the pinned photodiode further comprises forming the photodiode portion such that the portion underlies the gate of the MOS transistor.

21. The method of claim **20** wherein forming the pinned photodiode includes forming a pinned layer of the first conductivity type in the second portion of the enhancement layer by forming a first portion of the pinned layer within the conducting region of the second conductivity type and a second portion of the pinned layer extending laterally from the conducting region of the second conductivity type in a direction away from the MOS transistor.

22. The method of claim **19** wherein providing the substrate includes providing the substrate with a third doping concentration greater than the first and second doping concentrations.

23. The method of claim **19** wherein forming the conducting region of the second conductivity type includes implanting a first dopant at a first angle from normal to the substrate and angled toward the MOS transistor.

24. The method of claim **23** wherein implanting the first dopant at the first angle includes using an angle of at least fifteen degrees.

25. The method of claim **23** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

26. The method of claim **25** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

27. The method of claim **23** wherein the steps of forming the conducting region and forming the pinned layer of the first conductivity type includes implanting the conducting region by implanting the first dopant at the first angle away from normal to the substrate and toward the MOS transistor and implanting the pinned layer at a second angle away from normal to the substrate and away from the MOS transistor.

28. The method of claim **27** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

29. The method of claim **28** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

30. The method of clam **19** wherein forming the conducting region includes forming the conducting region to a depth less than 0.7 microns.

31. The method of claim **19** wherein forming the first well includes forming the first well to a first depth no greater than a depth of the enhancement layer.

32. The method of claim **19** further including forming a dielectric layer overlying the pinned photodiode, and forming a silicide layer on a portion of the image sensor wherein an area overlying the pinned photodiode is devoid of the silicide layer.

33. The method of claim **19** further including forming a dielectric layer overlying the pinned photodiode wherein the dielectric layer has a dielectric constant that is between a dielectric constant of any material overlying the dielectric layer and a dielectric constant of an underlying substrate on which the pinned photodiode is formed.

34. The method of claim **19** further including forming the enhancement layer and first well such that the first well, the enhancement region and the substrate are connected by an ohmic conduction path below the surface of the semiconductor.

* * * * *

EXHIBIT D

US006979587B2

(12) **United States Patent**
Lee

(10) **Patent No.: US 6,979,587 B2**
(45) **Date of Patent: Dec. 27, 2005**

(54) **IMAGE SENSOR AND METHOD FOR FABRICATING THE SAME**

(75) Inventor: **Won-Ho Lee**, Ichon-shi (KR)

(73) Assignee: **Hynix Semiconductor Inc.**, Kyoungki-do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 224 days.

(21) Appl. No.: **10/330,287**

(22) Filed: **Dec. 30, 2002**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/57**; 438/451; 257/292; 257/446

(58) **Field of Search** 438/57, 73, 449, 438/451, 525, 527, 529; 257/291, 292, 446, 463

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Primary Examiner—Amir Zarabian
Assistant Examiner—Christy Novacek
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

The present invention provides an image sensor capable of suppressing the dark current due to crystalline defects occurring at an edge of a field oxide layer and a method for fabricating the same. The present invention provides an image sensor including: a semiconductor substrate; an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area; a field area for isolating electrically the active area; a field stop layer being formed beneath the field area by having a wider area than the field area through an expansion towards the active area with a first width; and a gate electrode formed on the substrate by covering the channel area and having one side superposed with a second width on one entire side of the photodiode contacted to the channel area.

10 Claims, 11 Drawing Sheets

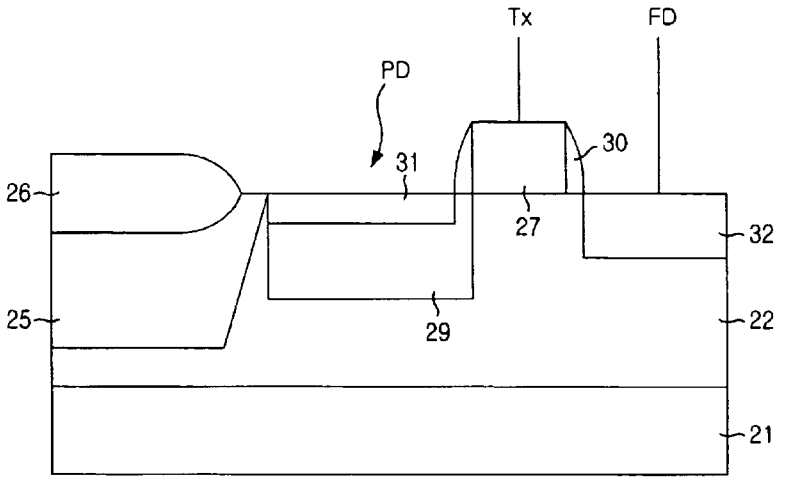

FIG. 1
(PRIOR ART)

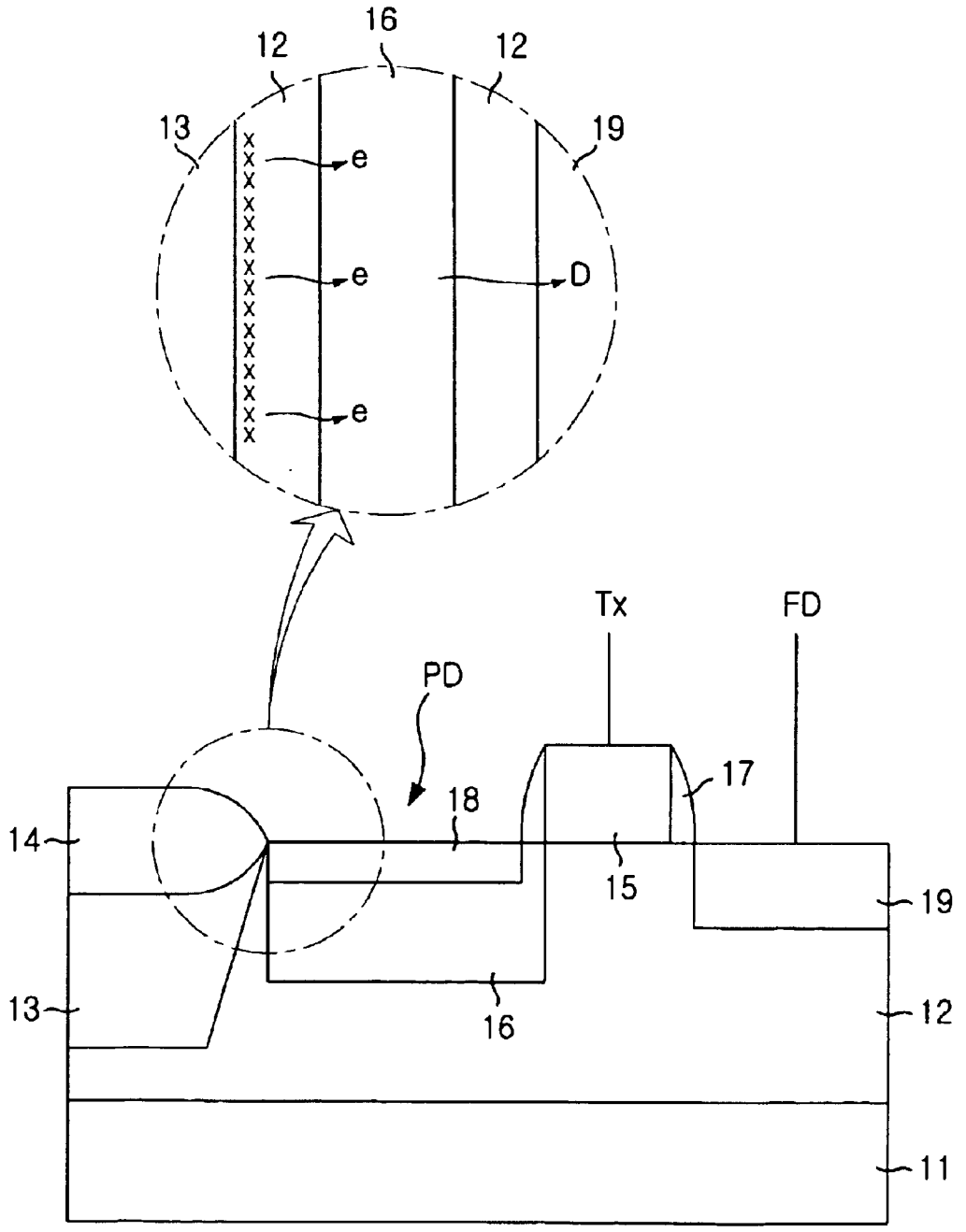

FIG. 2
(PRIOR ART)

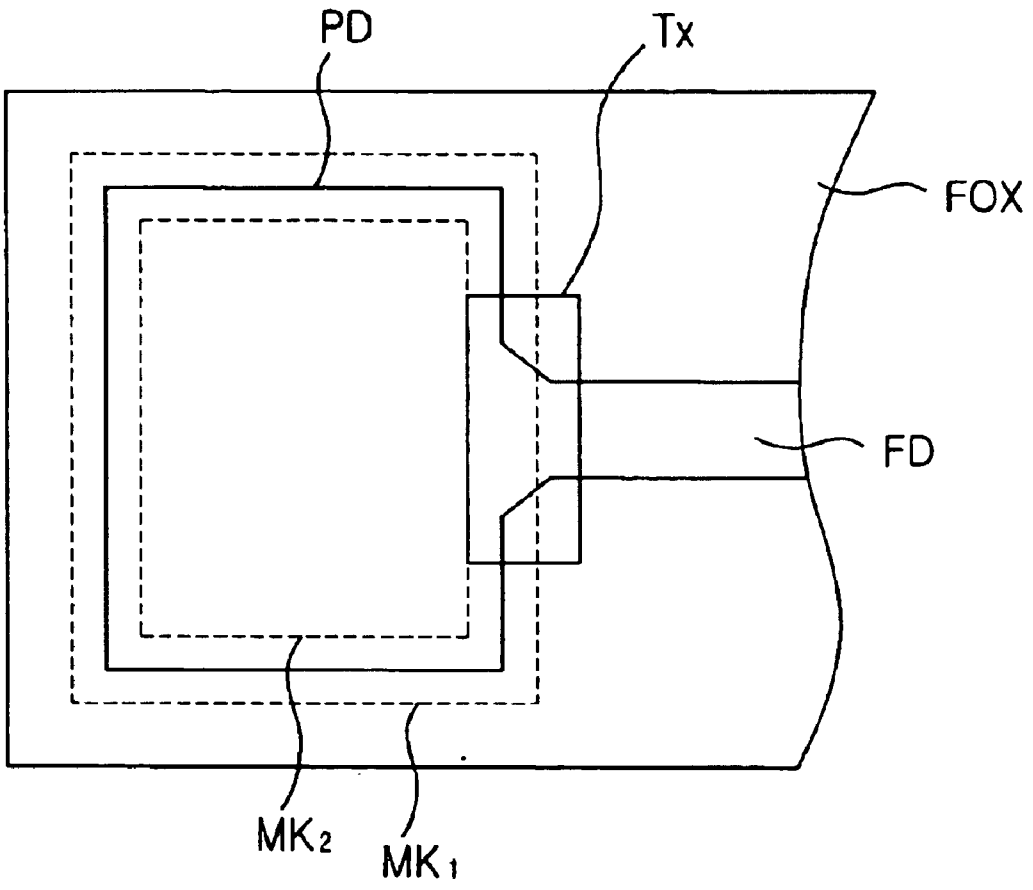

FIG. 3

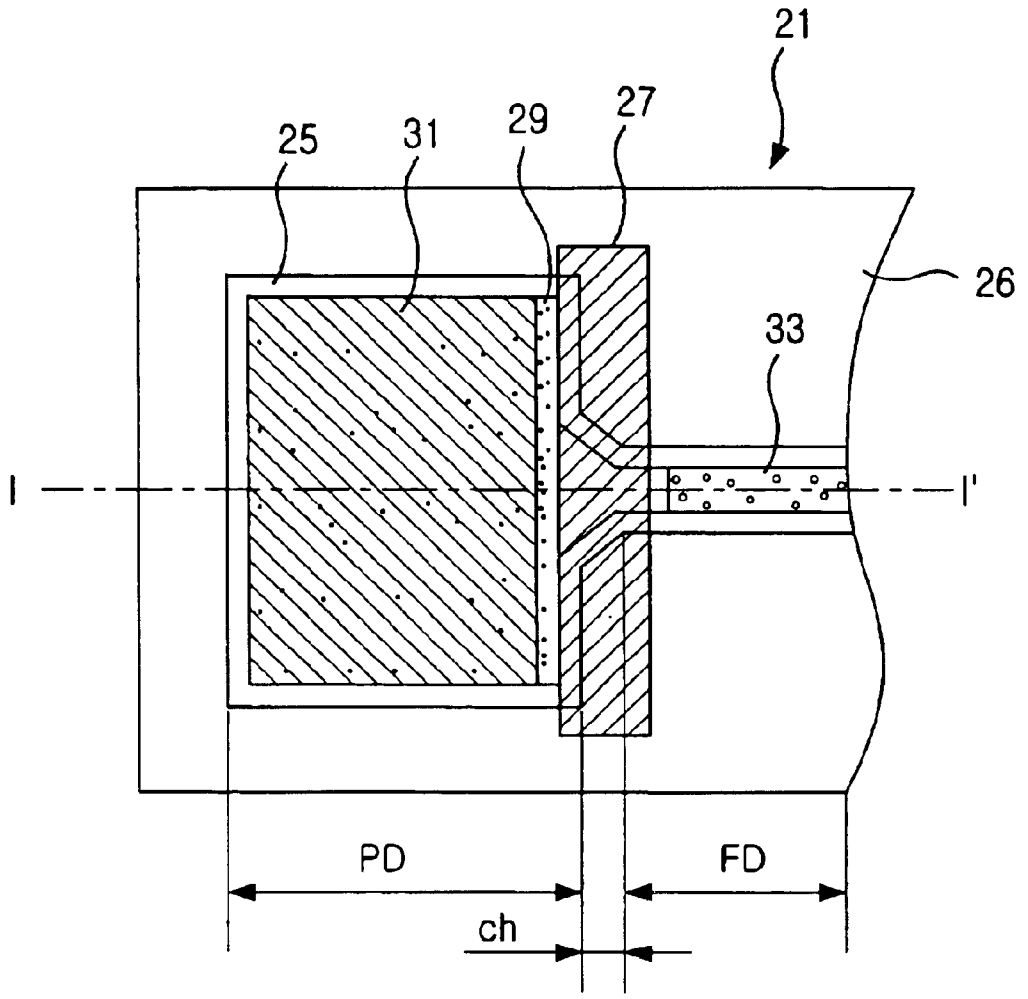

FIG. 4A

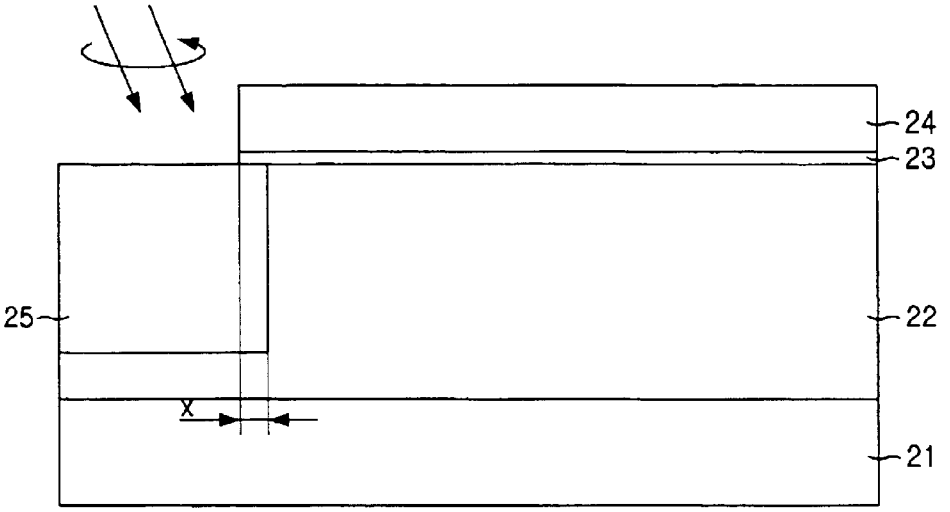

FIG. 4B

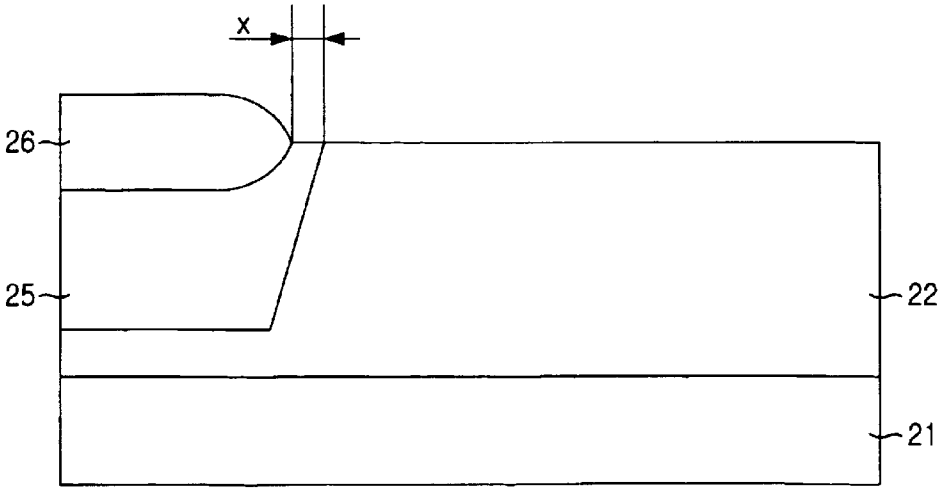

FIG. 4C

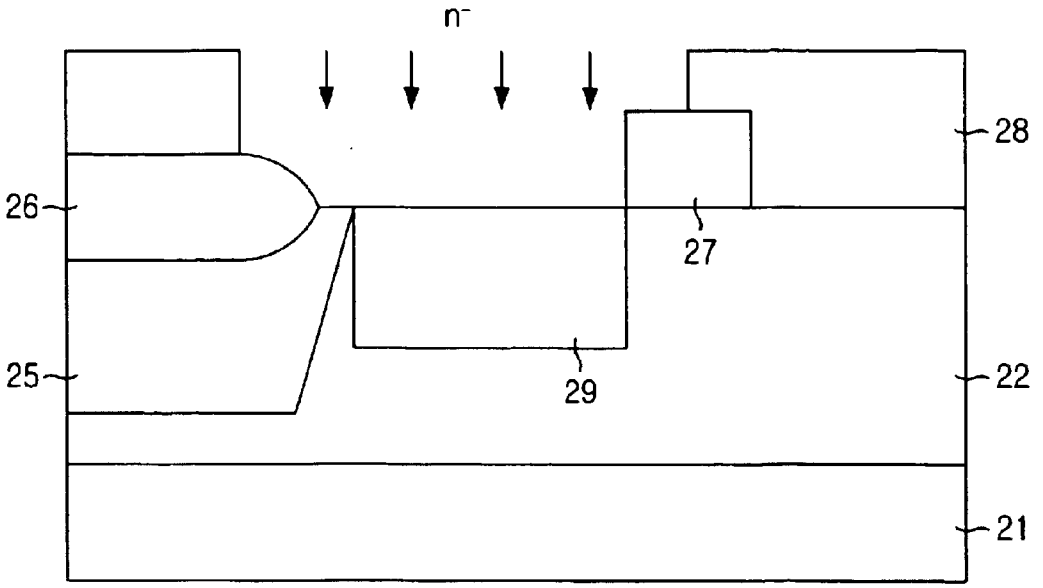

FIG. 4D

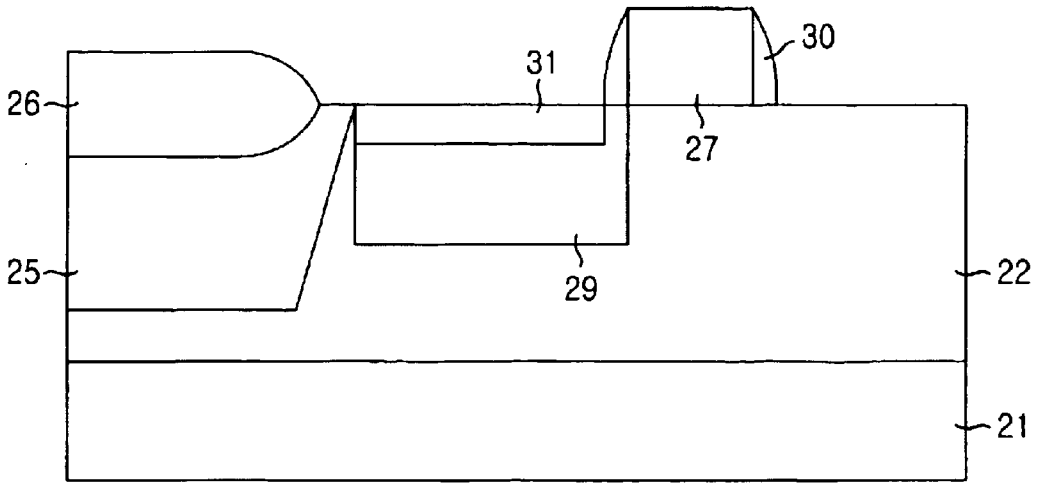

FIG. 4E

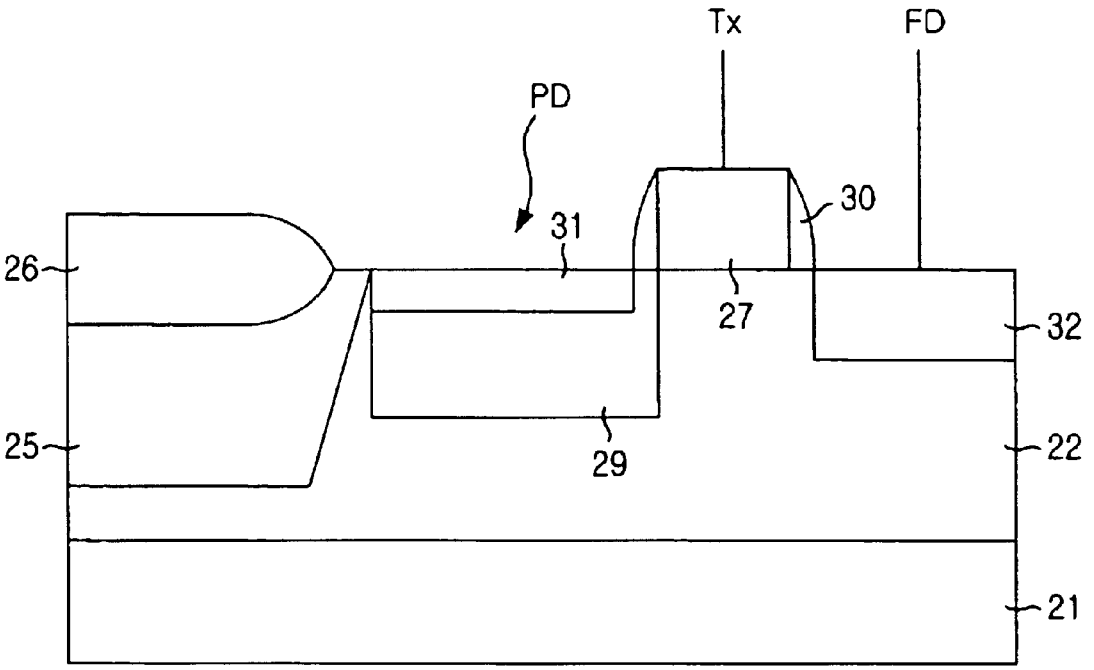

FIG. 5A

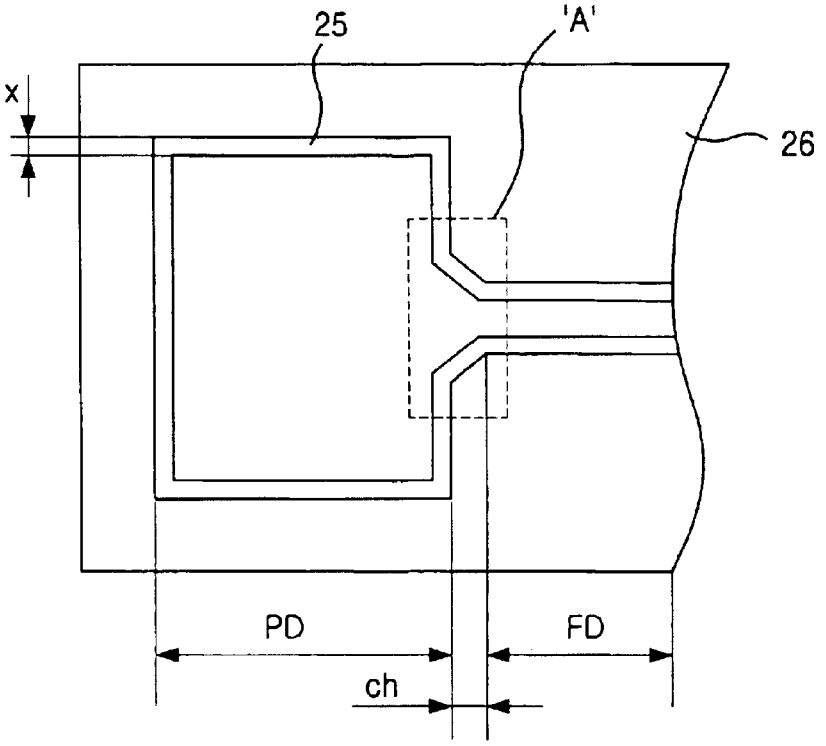

FIG. 5B

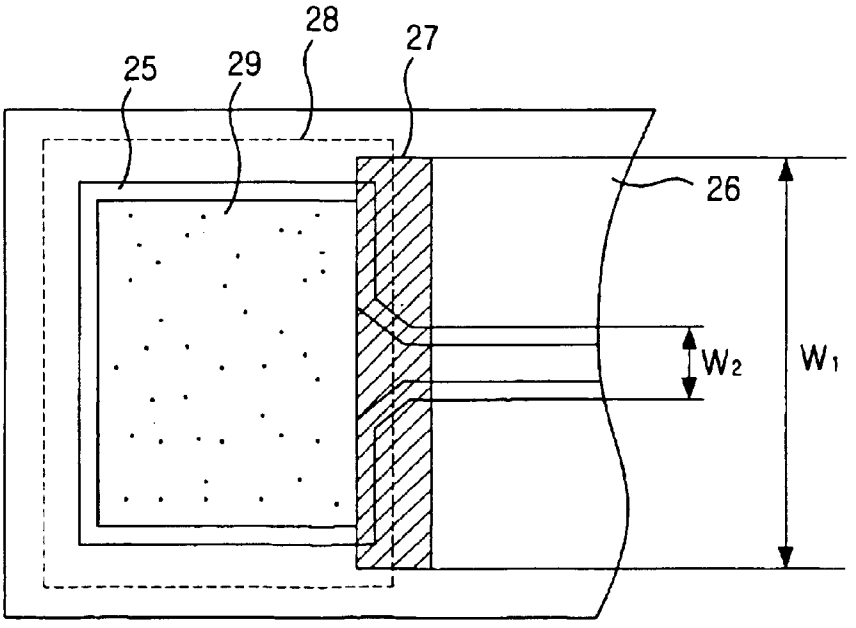

FIG. 5C

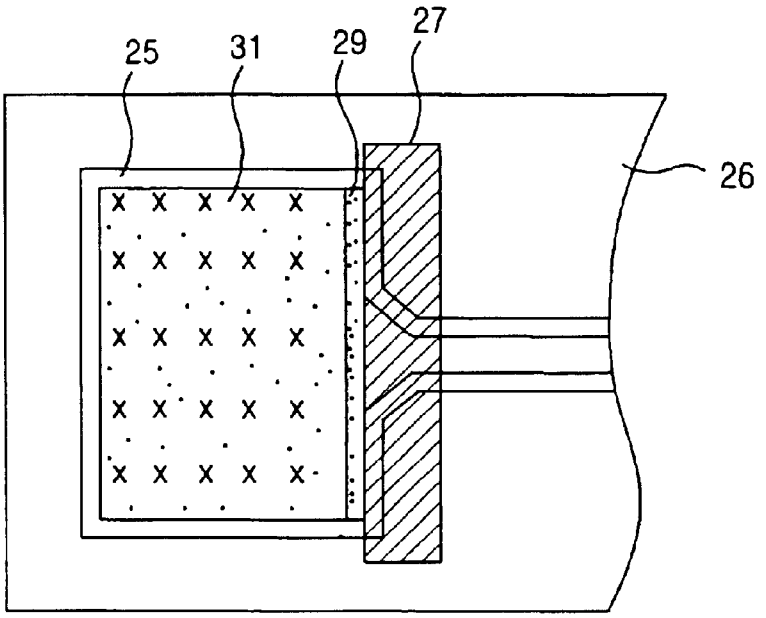

FIG. 5D

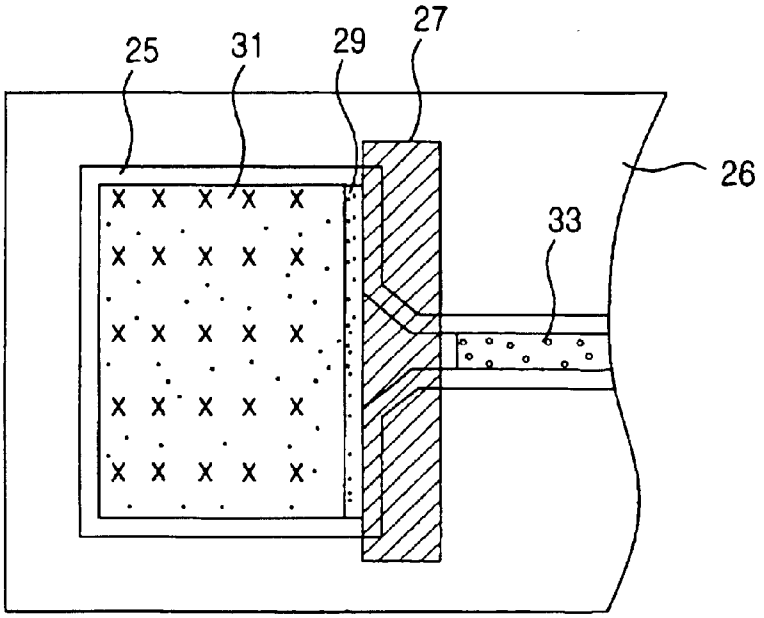

FIG. 6

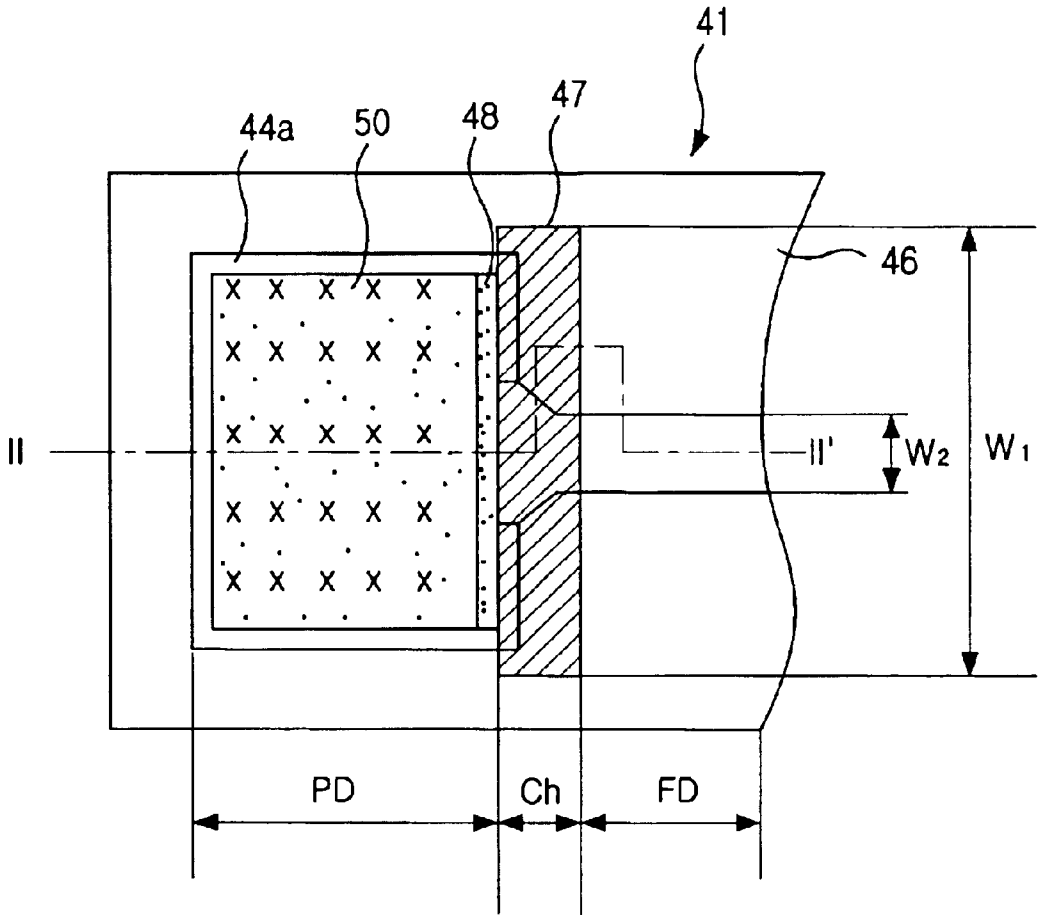

FIG. 7A

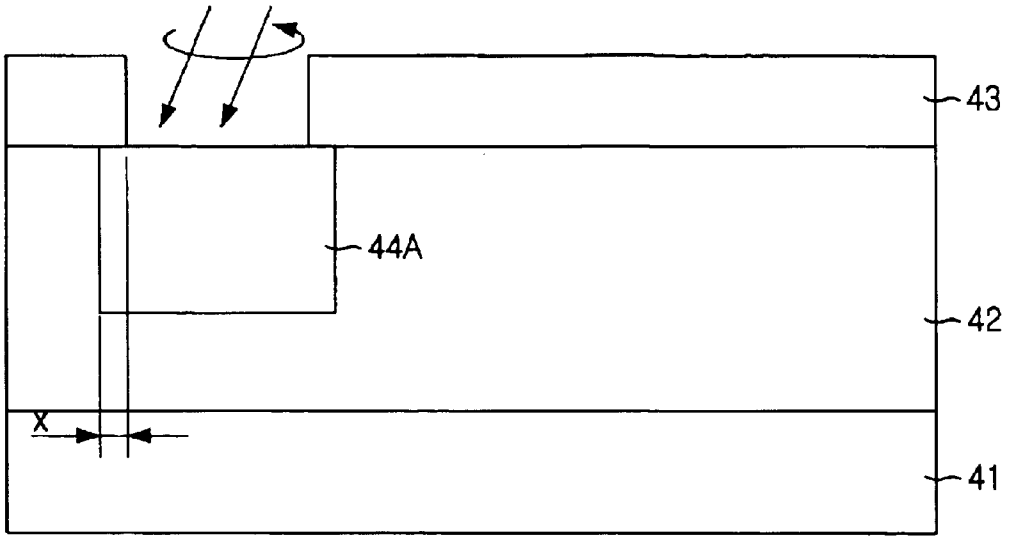

FIG. 7B

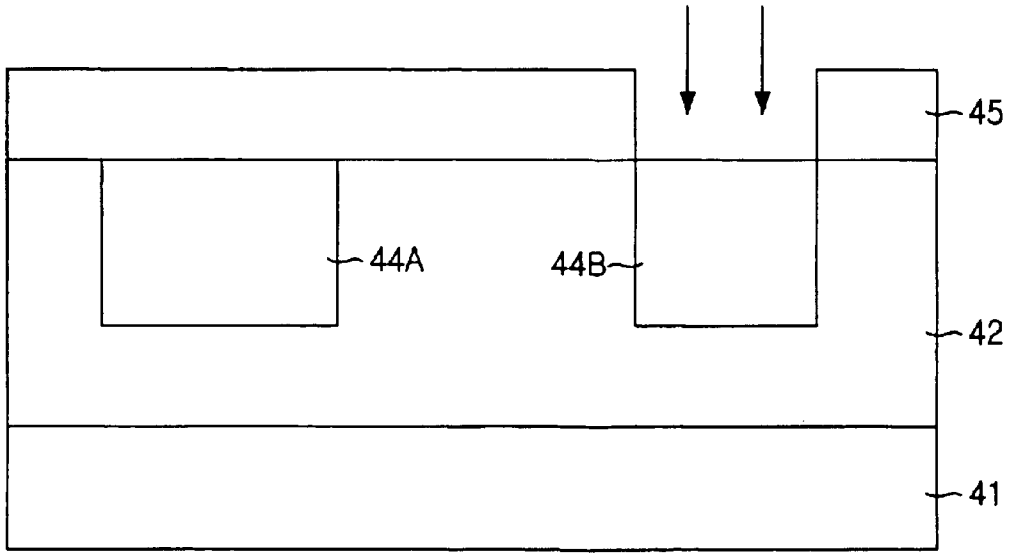

FIG. 7C

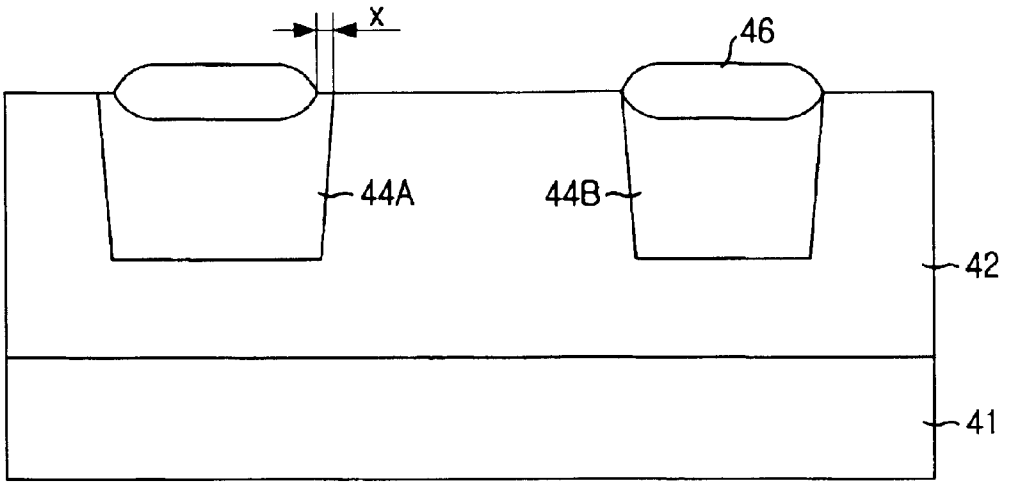

FIG. 7D

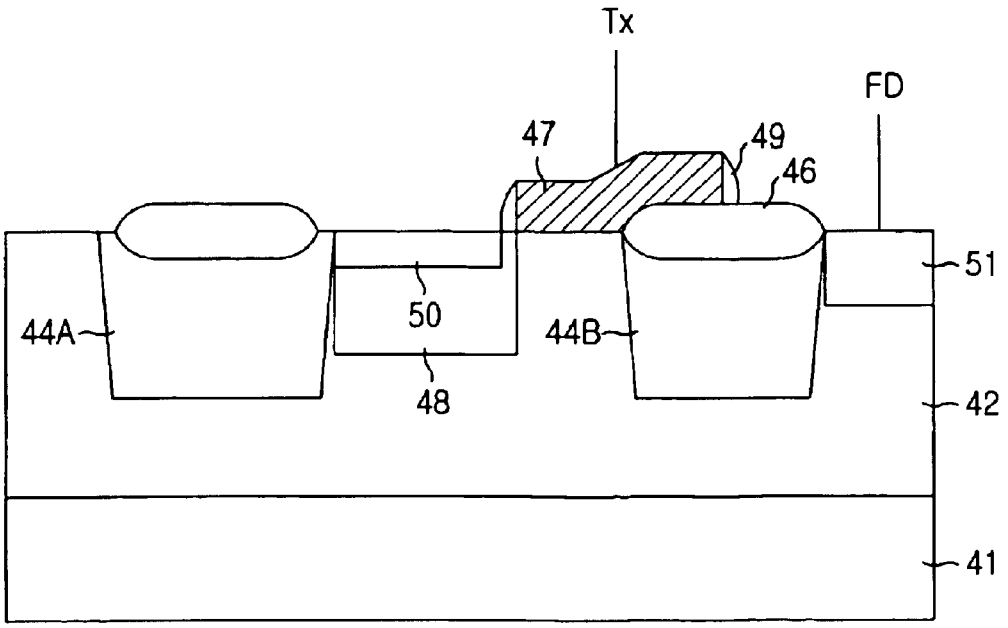

IMAGE SENSOR AND METHOD FOR FABRICATING THE SAME

This nonprovisional application claims priority under 35 U.S.C. §119(a) on Patent Application No. 2002-0001367 filed in KOREA on Jan. 10, 2002, which is herein incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to a method for fabricating a semiconductor device; and, more particularly, to an image sensor and a method for fabricating the same.

DESCRIPTION OF RELATED ARTS

Image sensor is a semiconductor device that converts an optical image into an electrical signal. Among the image sensors, a charge coupled device (CCD) is a device wherein an individual metal-oxide-silicon (CMOS) capacitor is closely allocated to each other, and carriers are stored and transferred to the MOS capacitor. A complementary metal-oxide semiconductor device (CMOS) image sensor employs CMOS technology using a control circuit and a signal processing circuit as peripheral circuits. In the CMOS image sensor, MOS transistors are formed as the same number of pixels in the peripheral circuit, and a switching mode is adopted for detecting sequentially outputs with use of the MOS transistors.

The CMOS image sensor includes a color filter arrayed on top of a light sensing element that generates and stores an optical charge after receiving light from an external source. The color filter array (CFA) can be classified with three colors of red (R), green (G) and blue (B) or those of yellow (Y), magenta (M) and cyan (C).

Also, the image sensor is constituted with a light sensing element for sensing light and a logic circuit component for processing the sensed light into an electrical signal, which is, in turn, systemized into data. There has been numerously attempted to improve a fill factor, which represents an areal ratio of the light sensing element with respect to the overall image sensor. However, these attempts are limited since the logic circuit component cannot be basically removed.

Accordingly, there introduced a light condensing technology for changing paths of incident lights that enter to areas other than the light sensing element and condensing the incident lights into the light sensing element so as to enhance a level of light sensing. To realize the light condensing technology, a method for forming a microlens on the color filter of the image sensor is particularly used.

A unit pixel of the typical CMOS image sensor has one photodiode area (hereinafter referred as to PD) and four N-channel metal-oxide semiconductor (NMOS) transistors, that are, a transfer transistor T_x, a reset transistor R_x, select transistor S_x and a drive transistor D_x. With respect to a specific function of each of the four NMOS transistors, the T_x is for transferring photo-generated charges collected at the PD to a floating diffusion area (hereinafter referred as to FD). The R_x is for resetting the FD by setting an electric potential of a node into a desired value and then releasing a charge (C_{pd}). Also, the D_x enacts as a source follower buffer amplifier, and the S_x is for providing a function of addressing with a switch.

Herein, the T_x and the R_x uses a native NMOS transistor, whereas the D_x and the S_x uses a normal NMOS transistor. Especially, the R_x is a transistor for a correlated double sampling (CDS).

The unit pixel of the above-described CMOS image sensor uses the native NMOS transistor so to sense rays in the visible wavelength bandwidth at the PD and then transfer detected photo-generated charges to the FD, i.e., an amount of the photo-generated charges transferred to a gate of the D_x is outputted in an electric signal from an output terminal V_{out}.

FIG. **1** is a cross-sectional view showing a typical CMOS image sensor in accordance with a prior art. Particularly, FIG. **1** shows merely a PD, a transfer transistor T_x and a FD.

Referring to FIG. **1**, a p-type epi layer **12** that is undergone with an epitaxial growth is formed on a P^+ substrate **11**. Also, a field oxide layer **14** for isolating devices is formed on the p-type epi layer **12**. A field stop layer **13** for an n-channel field stop layer is formed beneath the field oxide layer **14**.

Herein, the field stop layer **13** is allocated only beneath the field oxide layer **14** since ions are implanted without any tilts into the p-type epi layer **12** where the field oxide layer **14** is formed. Therefore, an n diffusion area **16** constituting the PD has only a boundary with an edge of the field oxide layer **14**, but does not affect an area of the n^- diffusion area **16**.

In addition, a gate electrode **15** of a T_x is formed on the p-type epi layer **12**. Also, a spacer **17** is then formed at lateral sides of the gate electrode **15**. The n^- diffusion area **16** is formed deeply in the p-type epi layer **12** by being aligned to an edge of one side of the gate electrode **15**. A shallow p^0 diffusion layer **18** is then formed on top of the n^- diffusion layer **16** as being aligned to one side of the spacer **17**.

Eventually, a PD including a deep n^- diffusion area **16** and a shallow p^0 diffusion area **18** is formed. A FD **19** is formed in the p-type epi layer **12** as being aligned to the spacer formed at the other side of the gate electrode **15**.

Meanwhile, one side of an ion implantation mask MK_1 (not shown) for forming the n^- diffusion area **16** is aligned to a center of the gate electrode of the T_x, while the other side of the ion implantation mask MK_1 is aligned to the field oxide layer **14**.

FIG. **2** is a plane view of FIG. **1** showing the typical CMOS image sensor in accordance with the prior art. One side of the gate electrode of the T_x is overlapped to an active area for providing the PD. The FD is formed below the other side of the gate electrode of the T_x.

Also, in the active area defined by the field oxide layer (FOX), the PD has a relatively larger area; however, an area between the PD and the FD becomes smaller. This effect is called a bottle-neck effect.

Meanwhile, as shown in FIG. **1**, when forming the n^- diffusion layer **16** constituting the PD, the n^- diffusion layer **16** is formed entirely on the active area except for a portion superposed on the gate electrode **15** of the T_x since the ion implantation mask MK_1 has a wide width compared to the actually formed n^- diffusion layer **16**. Therefore, the n^- diffusion area **16** is contacted to the field oxide layer FOX.

In the above-described prior art, if there exists a reverse bias between the n^- diffusion layer **16** and the p-area including the p^0 diffusion layer and the p-type epi layer, the n^- diffusion layer **16** becomes fully depleted when a concentration of impurities contained in the n^- diffusion layer **16** and the p-area is properly controlled. As a result of this full depletion, the depletion is also extended to the p-type epi layer **12** allocated beneath the n^- diffusion layer **16** and the p^0 diffusion layer **18** allocated above the n^- diffusion layer **16**. Especially, the depletion occurs in more extents in the p-type epi layer **12** having a relatively lower dopant concentration.

The image sensor having the above PD takes out electrons stored into the PD and obtains an electrical output signal, i.e., current or voltage. A maximum output signal is in a proportional relationship with the number of electrons that can be taken out from the PD, and thus, the number of electrons generated and stored in the PD due to inputs of light should be increased in order to increase the output signals.

The electrons generated at the depletion layer of the PD are converted to an electrical output signal such as a voltage or a current. Hence, the ion implantation is proceeded in such that a dopant concentration of the p^0 diffusion layer **18**, which is a surface layer, should be higher than that of the n^- diffusion layer **16** and the p-type epi layer **12**, which are a bottom layer.

Meanwhile, in the prior art, when incident lights are inputted, there occurs an electron hole pair (EHP) at the n^- diffusion layer **16**, which is the depletion layer. The hole (H) of the EHP is drained to the p^+ substrate **11**, and the electron (e) is accumulated and transferred to the FD **19** through the transfer transistor T_x so as to attain image data.

However, the prior art has a problem in that crystalline defects occur mainly at the edge of the field oxide layer **13** when applying an oxidation process to the field oxide layer **13**. A point defect, a line defect, an area defect and a volume defect are examples of the crystalline defects.

Eventually, electrons (e) are generated and stored due to the crystalline defects occurring at the edge of the field oxide layer **14** even when incident lights are not inputted. Therefore, there occurs dark current (D) flowing from the PD to the FD **19**.

In other words, the electrons should be generated and stored at the depletion layer, i.e., the n^- diffusion layer **16** of the PD only when the incident lights are inputted, and then, the stored electrons are transferred to the FD so to make current flow. However, the crystalline defects present at the edge of the field oxide layer **14** are in a state of generating electrons easily in a thermal aspect even without inputs of the incident lights. Thus, if there exists a plurality of defects even in a dark state without any light, the image sensor shows an abnormal state by acting as if there are inputs of the incident lights.

To solve the above problem, it is suggested to employ an ion implantation mask MK_2 of which linewidth is relatively smaller than the MK_1 for forming the deep n^- diffusion layer **16** (referred to FIG. **2**). However, this approach is sensitive to an overlay since there occurs no self-alignment during the ion implantation mask MK_2 process for forming the deep n^- diffusion layer **16**. Also, there is another problem in that the n^- diffusion layer **16** is extended near to an edge of the field oxide layer FOX due to a subsequent thermal process.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an image sensor capable of suppressing generation of dark current due to crystalline defects at an edge of a field oxide layer and a method for fabricating the same.

In accordance with an aspect of the present invention, there is provided an image sensor, comprising: a semiconductor substrate; an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area; a field area for isolating electrically the active area; a field stop layer being formed beneath the field area by having a wider area than the field area through an expansion towards the active area with a first width; and a gate electrode formed on the substrate by covering the channel area and having one side superposed with a second width on one entire side of the photodiode contacted to the channel area.

In accordance with another aspect of the present invention, there is also provided an image sensor, comprising: a substrate; an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area; a field area for isolating electrically the active area; a field stop layer being formed beneath the field area by having a wider area than the field area through an expansion towards the photodiode area with a first width; and a gate electrode formed on the substrate by covering the channel area and having one side superposed with a second width on one entire side of the photodiode contacted to the channel area.

In accordance with still another aspect of the present invention, there is also provided a method for fabricating an image sensor, comprising the steps of: forming an isolation mask that exposes partially a surface of the substrate; forming a first diffusion layer having a wider area than an exposed area of the isolation mask in the exposed substrate; forming a field oxide layer having a smaller area than the first diffusion layer on the first diffusion layer; forming a gate electrode on an active area of the substrate defined by the field oxide layer; forming a second diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and to the first diffusion layer; and forming a third diffusion layer being aligned with a predetermined distance from the edge of the one side of the gate electrode formed in the second diffusion layer.

In accordance with still another aspect of the present invention, there is also provided a method for forming an image sensor, comprising the steps of: forming on the substrate a first isolation mask that exposes a surface of one side of the substrate; forming a first diffusion layer having a wider area than an exposed area of the first isolation mask formed in the exposed substrate; forming on the substrate a second isolation mask that exposes the other side of the substrate; forming a second diffusion layer having an area identical to an exposed area of the second isolation mask formed in the exposed substrate; forming on the first diffusion layer a first field oxide layer having a smaller area than the first diffusion layer as simultaneously as forming on the second diffusion layer a second field oxide layer having an area identical to the second diffusion layer; forming a gate electrode extending on the active area of the substrate and simultaneously on the second field oxide layer; forming a third diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and the first diffusion layer; and forming a forth diffusion layer being aligned with a predetermined distance from the edge of the one side of the gate electrode in the third diffusion layer.

BRIEF DESCRIPTION OF THE DRAWING(S)

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

FIG. **1** is a cross-sectional view showing a complementary metal-oxide semiconductor (CMOS) image sensor in accordance with a prior art;

FIG. **2** is a plane view showing the CMOS image sensor in accordance with the prior art;

FIG. **3** is a plane view showing a CMOS image sensor in accordance with a first preferred embodiment of the present invention;

FIGS. **4**A to **4**E are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to a I-I' line of FIG. **3**;

FIGS. **5**A to **5**D are plane views illustrating a process for fabricating the CMOS image sensor with respect to the I-I' line of FIG. **3**;

FIG. **6** is a plane view showing a CMOS image sensor in accordance with a second preferred embodiment of the present invention; and

FIGS. **7**A to **7**D are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to a II-II' line of FIG. **6**.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **3** is a plane view showing a complementary metal-oxide semiconductor device (hereinafter referred as to CMOS) image sensor in accordance with a first preferred embodiment of the present invention. The-CMOS image sensor shown in FIG. **3** includes a photodiode area (hereinafter referred as to PD), a gate electrode of a transfer transistor T_x and a floating diffusion area (hereinafter referred as to FD).

On a predetermined place of a substrate **21**, an active area including the PD, the FD having a smaller area than the PD and a channel area ch having a bottle-neck structure that connects the PD and the FD is formed.

Then, a field oxide layer **26** for isolating electrically the active area is formed. A field stop layer **25** having a greater area than the field oxide layer **26** as being extended towards the active area with a first predetermined distance is formed beneath the field oxide layer **26**.

Also, a gate electrode **27** having one side superposed entirely on one side of the PD connected to the channel area ch with a second predetermined distance and the other side aligned to the FD is formed on the substrate **21**. Herein, the gate electrode also covers the channel area ch.

In the mean time, the PD includes an n^- diffusion area **29** formed by being self-aligned to the field stop layer **25** and the one side of the gate electrode **27** of the transfer transistor T_x and a p^0 diffusion area **31** formed in the n^- diffusion area **29** by being self-aligned to the field stop layer **25** with a predetermined distance from the one side of the gate electrode **27**.

Meanwhile, an n^+ diffusion layer **33** is formed at the other side of the gate electrode **27**.

FIGS. **4**A to **4**E are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to an I-I' line of FIG. **3**. Also, FIGS. **5**A to **5**D are plane views illustrating a process for fabricating the CMOS image sensor with respect to the I-I' line of FIG. **3**.

With reference to FIGS. **4**A to **4**E and FIGS. **5**A to **5**D, the process for forming the CMOS image sensor with respect to the I-I' line of FIG. **3** will be explained in more detail.

Referring to FIG. **4**A, a p-type epi layer **22** is grown on a p^+ substrate **21** doped with a high concentration of p-type impurities. On the p-type epi layer **22**, a pad oxide layer **23** and a pad nitride layer **24** are formed thereafter.

Herein, the reason for growing the p-type epi layer **22** is because a depth of a depletion layer of the PD can be increased due to the existence of the p-type epi layer **22** with a low dopant concentration. As a result, it is possible to obtain an excellent photosensitivity and to prevent the crosstalk phenomenon, which occurs between unit pixels of the CMOS image sensor due to irregular movements of optical charges that may be taken place at the deeper p^+-substrate **21**, by recombining the optical charges through the p^+-substrate **21** with the high dopant concentration.

Next, an isolation mask (not shown) is formed on the pad nitride layer **24**. Subsequently, the pad nitride layer **24** exposed by the isolation mask is firstly etched. After etching the pad nitride layer, the exposed pad nitride layer **23** is then etched so as to expose a surface of the p-type epi layer **22** where a field oxide layer will be formed.

Herein, the exposed p-type epi layer **22** has an area where the field oxide layer is formed and the unexposed p-type epi layer **22** is an active area.

After removing the isolation mask, impurities for an n-channel field stop layer **25** (hereinafter referred as to field stop layer) are ion implanted partially on the surface of the exposed p-type epi layer **22** by giving a tilt angle through rotation and twist. Herein, the pad nitride layer **24** exposed through the removal of the isolation mask is used as a mask.

At this time, the ion implantation for forming the field stop layer **25** is proceeded by giving a predetermined tilt angle α and rotating four times with 3.0×10^{13} cm of a dose quantity of boron (B_{11}) and 30 keV of ion implantation energy.

If the impurities are ion implanted with a tilted angle and rotations, the field stop layer **25** is expanded to the active area by distance X compared to the ion implantation without the tilt angle and the rotation. That is, the field stop layer formed through the ion implantation without the tilt angle and the rotation is merely allocated below the field oxide layer but is unable to penetrate to the active area.

Although an ion implantation mask for forming the field stop layer **25** uses the pad nitride layer **24**, it is also possible to use an additional ion implantation mask.

With reference to FIG. **5**A, the field stop layer **25** is formed and penetrated from the area where the field oxide layer will be formed to the exposed p-type epi layer **22** by a distance X.

Referring to FIG. **4**B, the surface of the p-type epi layer **22** where the field stop layer **25** is formed is oxidated so to grow the field oxide layer **26** on the field stop layer **25**. Thereafter, the pad nitride layer **24** and the pad oxide layer **23** are removed.

At this time, the active area defined by the field oxide layer **26** can be classified into a first active area ACT_1 having a wide area, a second active area ACT_2 having a relatively smaller area and width of an long and short axis and a third active area ACT_3 having a bottle-neck structure 'A' (referred to FIG. **5**A).

Herein, the first active area ACT_1 is an area for providing the PD, and the second active area ACT_2 is an area for providing the FD. The third active area ACT_3 is an area for providing a channel ch of the transfer transistor T_x.

Hereinafter, the first active area ACT_1, the second active area ACT_2 and the third active area ACT_3 are referred as to the PD, the FD and the channel area ch, respectively.

Meanwhile, before forming the field oxide layer **26**, a p-well (not shown) is formed in a predetermined area of the p-type epi layer **22** as to include a drive transistor D_x and a select transistor S_x through a lateral expansion due to a subsequent thermal process.

Next, after removing the pad oxide layer **23**, a general transistor fabrication process for forming the drive transistor D_x and the select transistor S_x among 4 transistors of the unit pixel.

Also, another ion implantation process (not shown) for a threshold voltage control ion that controls a threshold voltage of the transistor in the p-well and a deep ion implantation process (not shown) for p-type impurities that controls a punchthrough property are proceeded. However, these ion implantation processes are not proceeded at the active area where the PD will be formed and the area where a source/drain, i.e., the FD of the transfer transistor T_x.

Referring to FIG. **4**C, a conductive layer for forming the gate electrode **27** of the four transistors of the unit pixel is deposited. Then, a photosensitive film is coated and patterned through a photo-exposure process and a developing process so as to form a photosensitive pattern (not shown) for forming the gate electrode **27**.

At this time, since a doping profile of the PD at one side of the transfer transistor T_x determines charge transfer efficiency, the gate electrode **27** is formed to have a sufficient thickness so that ion implantations of high energy n-type impurities for forming the PD and low energy p-type impurities can be aligned at the one side of the transfer transistor T_x.

Afterwards, the conductive layer is etched by using the photosensitive pattern for forming the PD as an etch mask so as to form the gate electrode **27** of the four transistors of the unit pixel. Herein, the gate electrode **27** is the gate electrode of the transfer transistor T_x.

At this time, the gate electrode **27** can increase highly a width of long axis **W1** overlapped with the active area where the PD will be formed since the third activation area ACT_3 located at a bottom of the gate electrode **27** has the bottle-neck structure (referred to FIG. **5**B).

Accordingly, in the transfer transistor T_x of which channel area ch have the bottle-neck structure, a width W of the transistor that determines major parameters such as a drain current (I_{dsat}) and a threshold voltage V_t is the width **W2** of short axis of the FD not that **W1** of long axis of the gate electrode **27** that is overlapped with the FD.

For instance, in case that currents are flowing from a path having a wide width to a path having a narrow width, the path having the narrow width determines a speed of the current flow. In other words, the path having the wide width is not related to the speed of the current flow.

Next, a photosensitive film is coated entirely on the structure including the gate electrode **27** and patterned selectively so as to form a first mask **28** for ion implanting a low concentration of the n-type impurities n^- with high energy.

At this time, one side of the first mask **28** is aligned to a center of the gate electrode **27** while the other side of the first mask **28** is aligned to a predetermined portion of the field oxide layer **26** without having any portion penetrates into the PD (referring to FIG. **5**B).

Afterwards, an n^- diffusion layer **29** is formed through the ion implantation of the low concentration of the n-type impurities n^- with high energy by using the first mask **28** as an ion implantation mask.

At this time, one side of the n^- diffusion layer **29** is aligned to an edge of one side of the gate electrode **27** while the other side of the n^- diffusion layer **29** is aligned to an edge of one side of the field stop layer **25**. That is, even if the ion implantation mask that opens a partial portion of the field oxide layer **26** is used, the n^- diffusion layer **29** is not contacted to the field oxide layer **26** due to the field stop layer **25** penetrated into the active area with the predetermined distance X.

In the end, the n– diffusion layer **29** is self-aligned due to the gate electrode **27** and the field stop layer **25** as simultaneously as being isolated electrically from the edge of the field oxide layer **26** due to the field stop layer **25**.

Also, both ends of the gate electrode **27** are expanded to cover sufficiently one side of the PD. Since the n^- diffusion layer **29** is self-aligned due to the field stop layer **25**, it is possible to apply a reticle for forming a conventional n^- diffusion layer without any modification.

As described above, if the n^- diffusion layer **29** is formed by using the reticle without any modification, it is possible to reduce costs for forming a new reticle and freely control a distance between the field oxide layer **26** and the n^- diffusion layer **29**. It is also possible to obtain a mask overlay margin due to the self-alignment of the n^- diffusion layer **29**.

In case of using the new reticle for forming the n^- diffusion layer **29**, it is difficult to control the distance between the field oxide layer **23** and the n^- diffusion layer **29**.

Referring to FIG. **5**B, the n^- diffusion layer **29** is self-aligned to the one side of the gate electrode **27** of which long axis becomes elongated. Meanwhile, the rest of sides of the n^- diffusion layer **29** except for the portion self-aligned to the one side of the gate electrode **27** are also self-aligned due to the field stop layer **25** and formed in the PD.

Therefore, since the n– diffusion layer **29** is self-aligned only to the one side of the gate electrode **27** instead of aligning to both ends of the long axis of the gate electrode **27**, it is possible to minimize a contact between corners of the n– diffusion layer **29** and the field oxide layer **26**. This contact is a cause for the dark current.

After removing the first mask **28**, an ion implantation process for forming a lightly doped drain (LDD) structure of the four transistors of the unit pixel is proceed (not shown). Firstly, a photosensitive film is coated on entire structure and patterned through a photo-exposure process and a developing process so as to form a second mask (not shown) for forming the LDD structure.

Referring to FIG. **4**D, the second mask (not shown) is removed, and an insulating layer for a spacer is deposited on the entire structure. Then, the insulating layer is proceeded with an etch-back process so to form a spacer **30** at lateral sides of the gate electrode **27**.

With use of a blanket ion implantation technique, low energy p-type impurities p^0 are ion implanted so that a p^0 diffusion layer **31** is formed on the n^- diffusion layer **29** and at the other side of the gate electrode **27** as simultaneously as on the exposed p-type epi layer **22**. At this time, p^0 diffusion layer **31** formed in the n^- diffusion layer **29** is aligned to the spacer **30** with a distance as much as a thickness the spacer **30**.

Meanwhile, the p^0 diffusion layer **31** is also formed on the p-type epi layer **22** exposed at the other side of the gate electrode **27** through the blanket ion implantation technique. However, this p^0 diffusion layer **31** does not have any specific effect since it uses the identical p-type impurities used for the p-type epi layer **22**.

Through the ion implantation of the low energy p-type impurities p^0, a shallow pn junction including the p^0 diffusion layer **31** and the n^- diffusion layer **29** and a pnp-type PD including the p-type epi layer **22**, the n^- diffusion layer **29** and the p^0 diffusion layer **31** are formed.

With reference to FIG. **5**C, which showing a plane view of the p^0 diffusion layer **31**, one side of the p^0 diffusion layer **31** is aligned to the spacer (not shown) while the rest of sides are self-aligned to the field stop layer **25**.

As shown in FIG. **4**E, a photosensitive film is coated on the entire structure and patterned through a photo-exposure process and a developing process so to form a third mask (not shown) for forming a source/drain area. Then, n-type impurities n^+ with a high concentration are ion implanted by using the third mask as an ion implantation mask so as to form an n^+ diffusion layer **32**. Herein, the n^+ diffusion layer **32** is the source/drain area (not shown) of the drive transistor D_x and the select transistor S_x and that of the transfer transistor T_x and the reset transistor R_x, i.e., the FD of the unit pixel.

Referring to FIG. **5**D, the third mask exposes the other side of the gate electrode **27** of the transfer transistor T_x and the FD near to the other side of the gate electrode **27** but is aligned at a center of the gate electrode **27**. That is, the ion implantation of the n-type impurities n^+ with a high concentration does not occur at the area for providing the PD.

FIG. **6** is a plane view of a CMOS image sensor in accordance with a second preferred embodiment of the present invention.

With reference to FIG. **6**, an active area including a substrate **41**, a PD formed on a predetermined portion of the substrate **41**, a FD having a relatively smaller area than the PD, a channel area ch having a bottle-neck structure connecting the PD and the FD is formed.

Then, a field oxide layer **46** for isolating electrically the active area is formed, and then a field stop layer **44**A having a wider area than the field oxide layer **46** by extended towards the PD with a first predetermined width is formed below the field oxide layer **46**.

That is, the field stop layer **44**A is extended only to the active area where the PD will be formed, and formed below the channel area ch and the FD.

A gate electrode **47** having one side supposed with a second predetermined width with an entire area of one side of the PD and the other side is aligned to the FD as simultaneously as covering the channel area ch is formed on the substrate **41**. Herein, the PD is connected to the channel area ch.

Meanwhile, the PD includes an n^- diffusion layer **48** formed through a self-alignment to the one side of the gate electrode **47** and the field stop layer **44**A and a p^0 diffusion layer **50** formed in the n^- diffusion layer **48** by being self-aligned to the field stop layer **44**A with a predetermined distance from the one side of the gate electrode **47**.

On the other side of the gate electrode **47**, a n^+ diffusion layer **51** is formed.

In the following second preferred embodiment, a method for proceeding an ion implantation process for forming the field stop layer by classifying the channel area of the transfer transistor T_x sensitive to a tilt angle and other areas with each different mask will be described.

FIGS. **7**A to **7**D are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to an II-II' line of FIG. **6**.

Referring to FIG. **7**A, a p-type epi layer **42** is grown on a p^+ substrate **41** doped with a high concentration of p-type impurities. Subsequently, a first ion implantation mask **43** is formed on the p-type epi layer **42**.

At this time, the p-type epi layer **42** exposed by the first ion implantation mask **43** is an area where a field oxide layer allocated close to the PD is formed.

Next, impurities for forming a first field stop layer **44**A are ion implanted on the exposed p-type epi layer **42** by giving a tilt angle and rotations or twists.

At this time, the ion implantation for forming the first field stop layer **44**A is proceeded with a predetermined tilt angle α and 4 times of rotations by using 3.0×10^{13} cm^{-3} of a dose quantity of boron (B_{11}) and 30 keV of ion implantation energy.

As described above, if the impurities are ion implanted with the tilt angle and the rotations, the first field stop layer **44**A has an increased overlapping distance X with the active area compared to the ion implantation without any tilt angle and the rotation.

With reference to FIG. **6**, which is a plane view of the first field stop layer **44**A, the field stop layer **44**A is formed with a distance X penetrated into the PD from the area where the field oxide layer will be formed.

Referring to FIG. **7**B, after removing the first ion implantation mask **43**, a second ion implantation mask **45** is formed entirely on the above structure. At this time, the p-type epi layer **42** exposed by the second ion implantation mask **45** is an area where the field oxide layer near to the channel area ch of the transfer transistor T_x.

Next, impurities for forming a second field stop layer **44**B are ion implanted on the exposed p-type epi layer r**42** without any tilt angle.

At this time, the ion implantation for forming the second field stop layer **44**B is proceeded with 3.0×10^{13} cm^{-3} of a dose quantity of boron (B11) and 30 keV of ion implantation energy.

In case that the impurities are ion implanted without the tilt angle, the first field stop layer **44**A is not overlapped with the active area. Thus, this case does not appear in FIG. **6**.

Meanwhile, the first ion implantation mask **43** and the second ion implantation mask **45** uses the identical pad oxide layer and the pad nitride layer for a LOCOS process explained in the first preferred embodiment. However, the first and the second ion implantation masks **43** and **45** uses each different reticles.

In other words, the pad oxide layer and the pad nitride layer are simultaneously patterned to expose a portion of the p-type epi layer **42** where the first field stop layer **44**A will be formed. Subsequently, an ion implantation for forming the first field stop layer **44**A is proceeded. In continuous to the ion implantation for the first field stop layer **44**A, the rest of the p-type epi layer **42** except for the portion for the first field stop layer **44**A are exposed, and another ion implantation for forming the second field stop layer **44**B is proceeded.

With reference to FIG. **7**C, the surface of the p-type epi layer **42** for providing the first and the second field stop layers **44**A and **44**B are oxidated, and then grow the field oxide layer **46** on the first and the second field stop layer **44**A and **44**B.

Herein, the first field stop layer **44**A penetrated to the active area for providing the PD with a predetermined distance X isolates electrically the active area and the field oxide layer **46**. However, this first field stop layer **44**A does not isolate electrically the active area for providing the channel area ch of the transfer transistor T_x and a bottom part of the field oxide layer closed to the active area for the channel area ch.

All process for forming a subsequent gate electrode including an n^- diffusion layer and a p^0 diffusion layer are identical to the processes described in the first preferred embodiment.

Referring to FIG. **7**D, a gate electrode **47** of four transistors is formed on the p-type epi layer **42**. Herein, the gate electrode **47** shown in FIG. **7**D is the gate electrode of the transfer transistor T_x.

At this time, since the gate electrode **47** has a bottle-neck structure at a bottom part, it is possible to highly increase a width **W1** of a long axis superposed on the active area for providing the PD.

Therefore, with respect to the transfer transistor T_x of which channel area has the bottle-neck structure, a width of the transistor that determines major parameters such as a drain current (I_{dsat}) and a threshold voltage (V_t) is the width **W2** of a short axis of the FD not the width **W1** of the long axis of the gate electrode **47**.

Next, a low concentration of n-type impurities n^- are ion implanted by using an ion implantation mask of which one side is aligned to a center of the gate electrode **47** and the other side is aligned to a predetermined portion of the field oxide layer **46** without having portions penetrated into the PD so as to form an n^- diffusion layer **48**.

After forming a LDD structure, an insulating layer for a spacer is deposited on the above entire structure. The insulating layer is then proceeded with an etch-back process so to form a spacer **49** contacting to both lateral sides of the gate electrode **47**.

Through the blanket ion implantation technique, low energy p-type impurities p^0 are ion implanted so that a p^0 diffusion layer **50** is formed on the n^- diffusion layer **48** and simultaneously on the p-type epi layer **42** exposed at the other side of the gate electrode **47**. At this time, the p^0 diffusion layer **50** formed in the n^- diffusion layer **48** is aligned to the spacer **49** with a distance as same as a thickness of the spacer **49**.

A shallow pn junction including the p^0 diffusion layer **50** and the n^- diffusion layer **48** is formed through the ion implantation of the low energy p-type impurities p^0. Also, a pnp-type PD including the p-type epi layer **42**, the n^- diffusion layer **48** and the p^0 diffusion layer **50** is formed.

Next, a high concentration of n-type impurities n^+ are ion implanted through the use of an ion implantation mask that exposes the p-type epi layer **42** where an n^+ diffusion layer will be formed so as to form an n^+ diffusion layer **51**. The n^+ diffusion layer **51** is a source/drain area (not shown) of a drive transistor D_x and a select transistor S_x and a source/drain area of the transfer transistor T_x and a reset transistor R_x, i.e., the FD.

The first and the second preferred embodiments can be used not only in a process for fabricating the CMOS image sensor but also in other processes applicable for controlling the dark current of a charge coupled device (CCD).

The present invention provides an effect of fabricating the CMOS image sensor with high immunity against the dark current.

When proceeding the ion implantation process for forming the deep n^- diffusion layer constituting the PD, it is possible to improve a process margin since a dark current elimination structure capable of an self-alignment is applied.

Also, instead of fixing a distance between the n^- diffusion layer and the field oxide layer with a reticle, the distance is variable in accordance with a tilt angle during the formation of the n^- diffusion layer, thereby providing an effect of easily controlling optical characteristics of the CMOS image sensor.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.

What is claimed is:

1. An image sensor, comprising:

a semiconductor substrate;

an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area;

a field area for isolating electrically the active area;

a field stop layer being formed beneath the field area and being wider than the field area in a direction towards the active area; and

a gate electrode formed on the substrate by covering the channel area and a portion of the photodiode contacted to the channel area.

2. The image sensor as recited in claim **1**, wherein the photodiode area further includes:

a first diffusion layer formed in the photodiode area by being aligned to one side of the gate electrode and the field stop layer; and

a second diffusion layer formed in the first diffusion layer being aligned to the field stop layer with a predetermined distance from the one side of the gate electrode.

3. The image sensor as recited in claim **1**, wherein the gate electrode is aligned to the floating diffusion area.

4. An image sensor, comprising:

a substrate;

an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area;

a field area for isolating electrically the active area;

a field stop layer being formed beneath the field area and being wider than the field area in a direction towards the active area; and

a gate electrode formed on the substrate by covering the channel area and a portion of the photodiode contacted to the channel area.

5. A method for fabricating an image sensor, comprising the steps of:

forming an isolation mask that exposes partially a surface of a substrate;

forming a first diffusion layer having a wider area than an area of the partially exposed substrate;

forming a field oxide layer having a smaller area than the first diffusion layer on the first diffusion layer;

forming a gate electrode on an active area of the substrate defined by the, field oxide layer;

forming a second diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and to the first diffusion layer; and

forming a third diffusion layer being aligned with a predetermined distance from the edge of the one side of the gate electrode formed in the second diffusion layer.

6. The method as recited in claim **5**, wherein the step of forming the first diffusion layer is proceeded with an ion implantation that gives impurities a plurality of rotations or twists with a predetermined tilt angle.

7. The method as recited in claim **5**, wherein the active area of the substrate defined by the field oxide layer includes a photodiode area, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting the photodiode area and the floating diffusion area,

wherein the gate electrode has one entire side of the floating diffusion area.

8. A method for forming an image sensor, comprising the steps of:

forming a first isolation mask that exposes a portion of a surface of one side of a substrate;

forming a first diffusion layer having a wider area than an exposed area of the substrate;

forming on the substrate a second isolation mask that exposes the other side of the substrate;

forming a second diffusion layer having an area identical to an exposed area of the substrate;

forming on the first diffusion layer a first field oxide layer having a smaller area than the first diffusion layer, and simultaneously forming on the second diffusion layer a second field oxide layer having an area identical to the second diffusion layer;

forming a gate electrode extending on the active area of the substrate and simultaneously on the second field oxide layer;

forming a third diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and the first diffusion layer; and

forming a fourth diffusion layer being aligned with a predetermined distance from the edge of the one side of gate electrode in the third diffusion layer.

9. The method as recited in claim **8**, wherein the step of forming the first diffusion layer is proceeded with an ion implantation that gives impurities a plurality of rotations or twists with a predetermined tilt angle.

10. The method as recited in claim **8**, wherein the step of forming the second diffusion layer is proceeded with an ion implantation that implants impurities vertically.

* * * * *

EXHIBIT E

US007365298B2

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Ryu

(10) **Patent No.: US 7,365,298 B2**
(45) **Date of Patent: Apr. 29, 2008**

(54) **IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME**

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(73) Assignee: **Hynix Semiconductor Inc.**, Kyungki-do (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 219 days.

(21) Appl. No.: **10/945,182**

(22) Filed: **Sep. 20, 2004**

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(30) **Foreign Application Priority Data**

Sep. 29, 2003 (KR) 10-2003-0067561

(51) **Int. Cl.**
H01L 21/77 (2006.01)

(52) **U.S. Cl.** **250/208.1**; 250/226; 257/294; 438/70; 438/57

(58) **Field of Classification Search** 250/208.1, 250/226; 257/294, 223, 225, 215; 438/70, 438/57, 69, 73
See application file for complete search history.

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Assistant Examiner—Tony Ko
(74) *Attorney, Agent, or Firm*—Marshall Gerstein & Borun LLP

(57) **ABSTRACT**

The present invention discloses an image sensor and a method for manufacturing the same which is capable of increasing the light-collection efficiency of a photodiode. The image sensor comprises: at least one photodiode formed on a semiconductor substrate; multilayer interlayer insulating films formed on the photodiode and stacked in at least two layers so that the density of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multilayer interlayer insulating films proceed upward; a light shield layer and an element-protecting film sequentially stacked on the multilayer interlayer insulating film; color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and microlenses arranged on the positions corresponding to the color filters on the flattening layer. Therefore, the light-collection efficiency of the photodiode can be increased with an increased transmittance of a vertical light reaching to the photodiode by making the multilayer interlayer insulating films have a lower density as they proceed upward to decrease the refraction angle of the incident light penetrated through the microlenses and color filters.

12 Claims, 4 Drawing Sheets

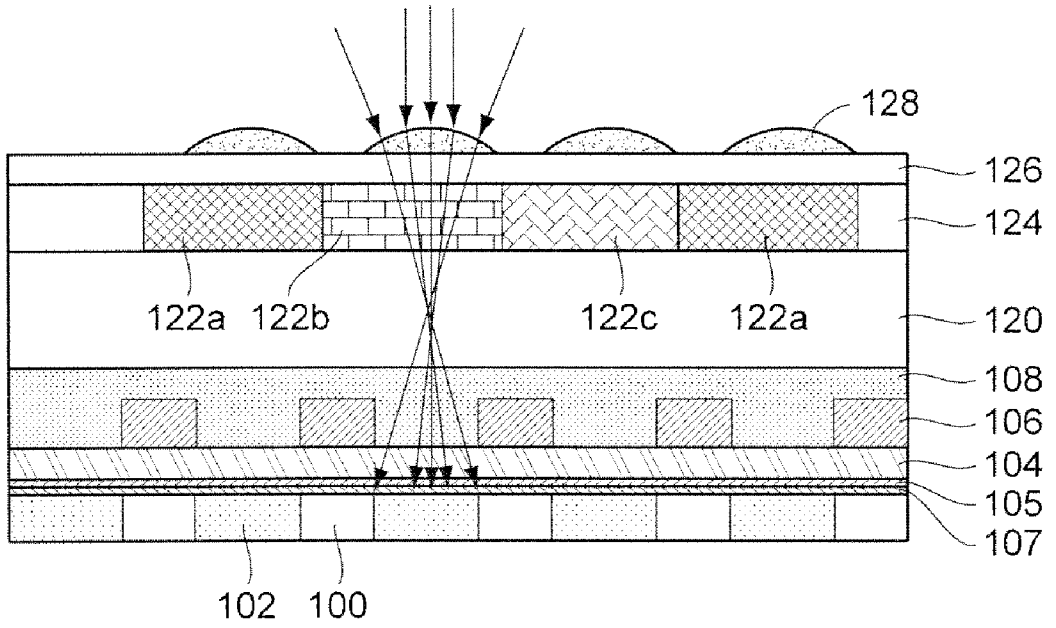


FIG. 1
(PRIOR ART)

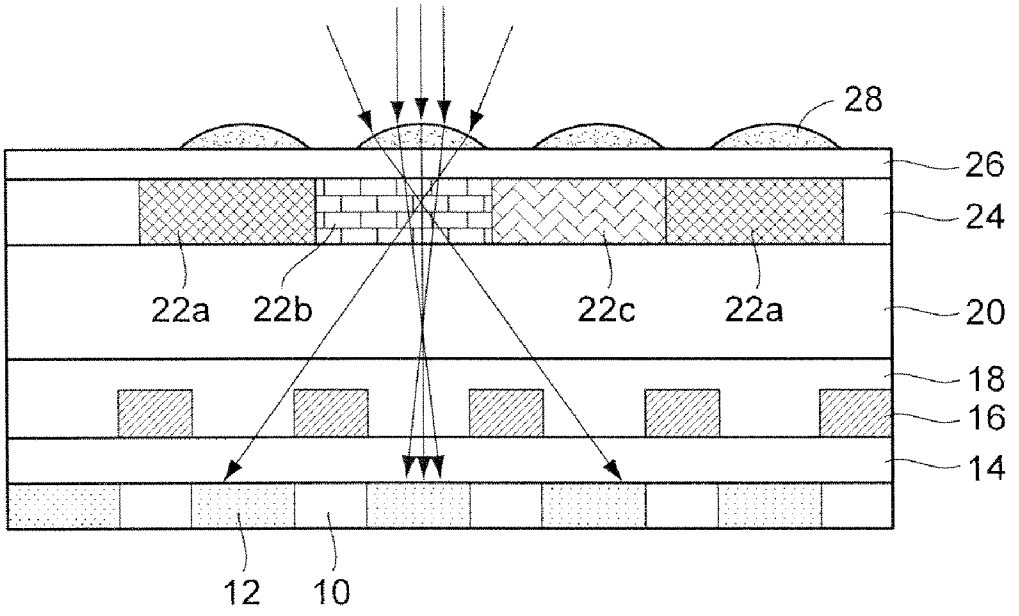


FIG. 2

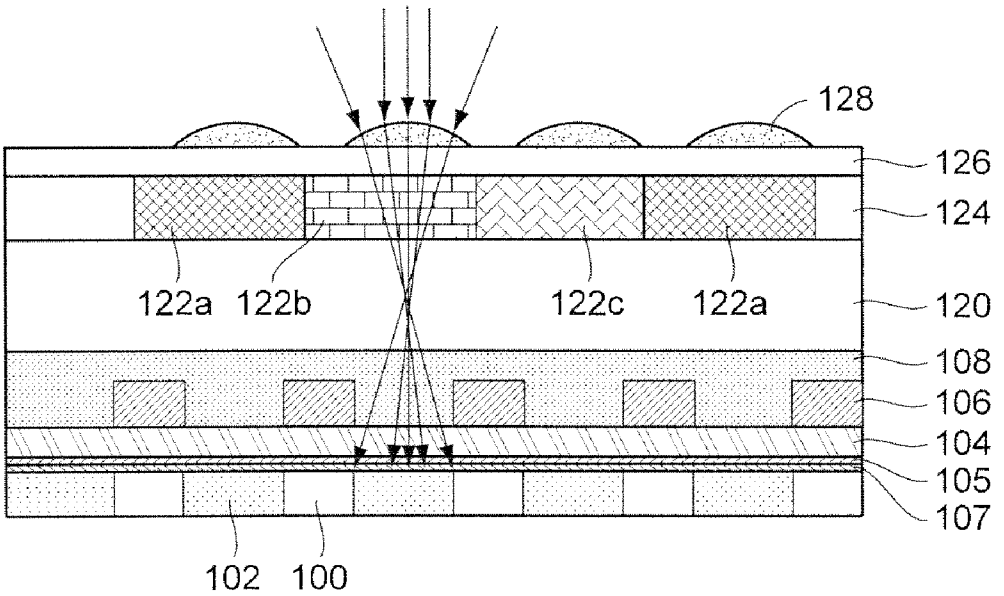


FIG. 3a

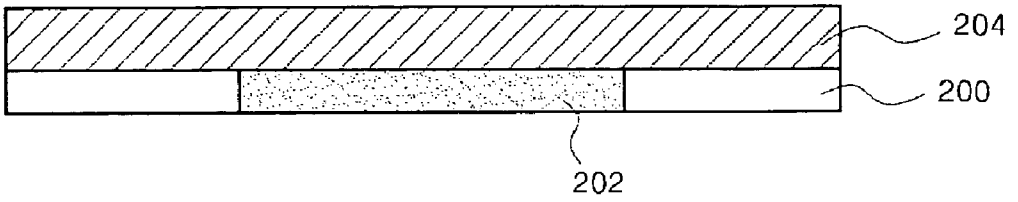


FIG. 3b

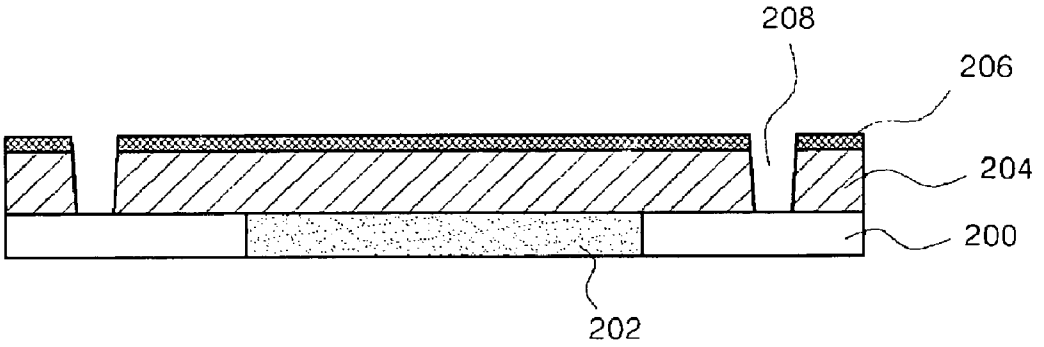


FIG. 3c

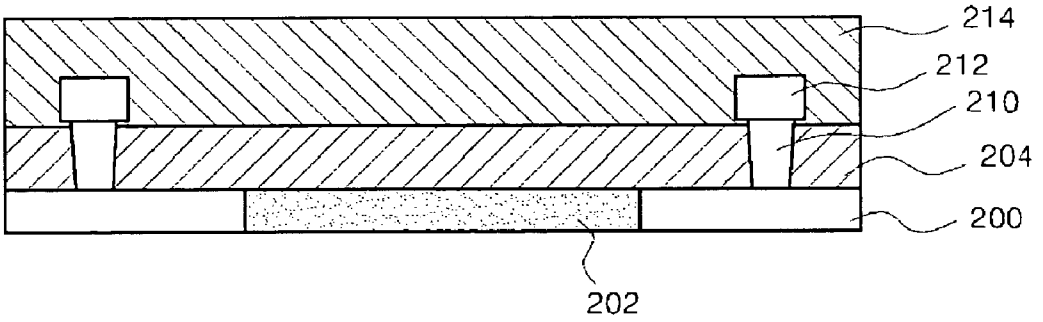


FIG. 3d

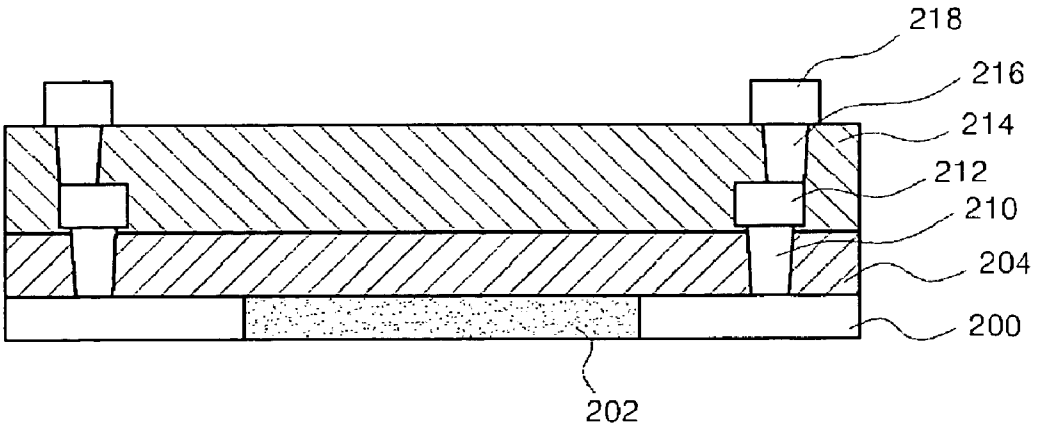
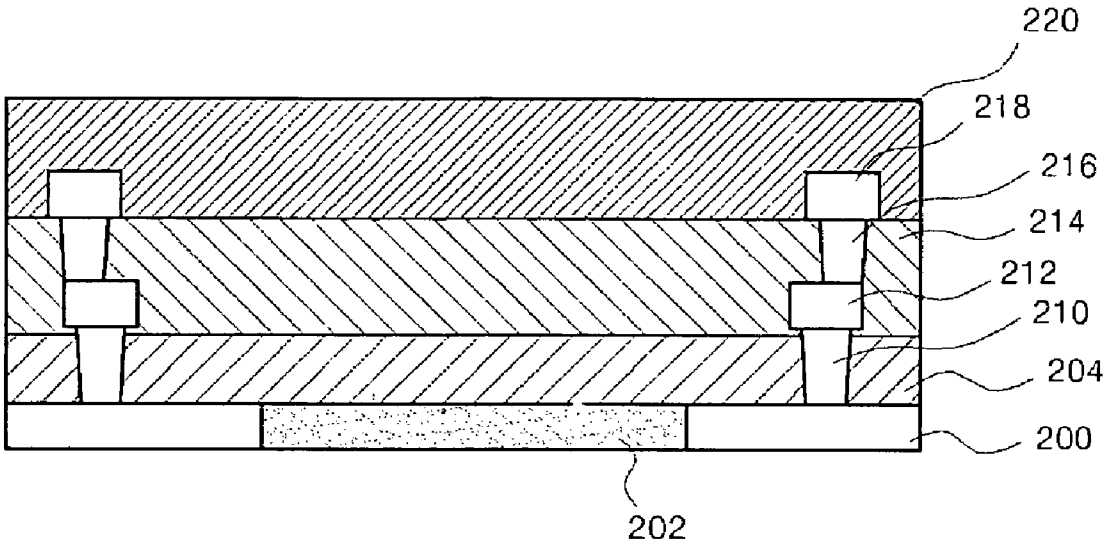


FIG.3e


220
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216
214
212
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FIG.3f

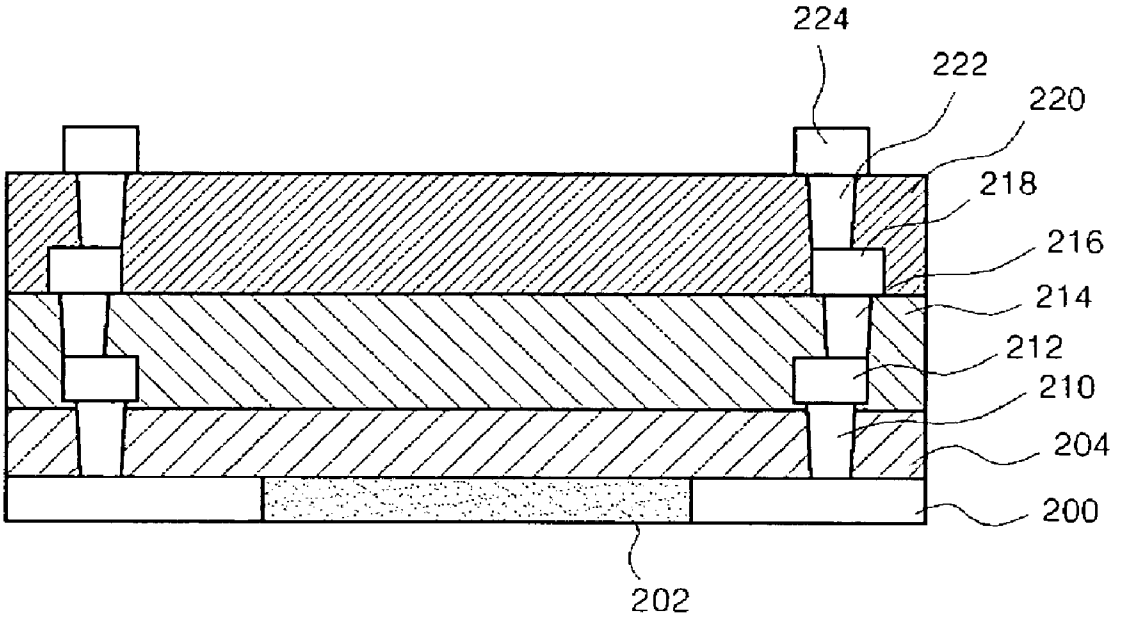
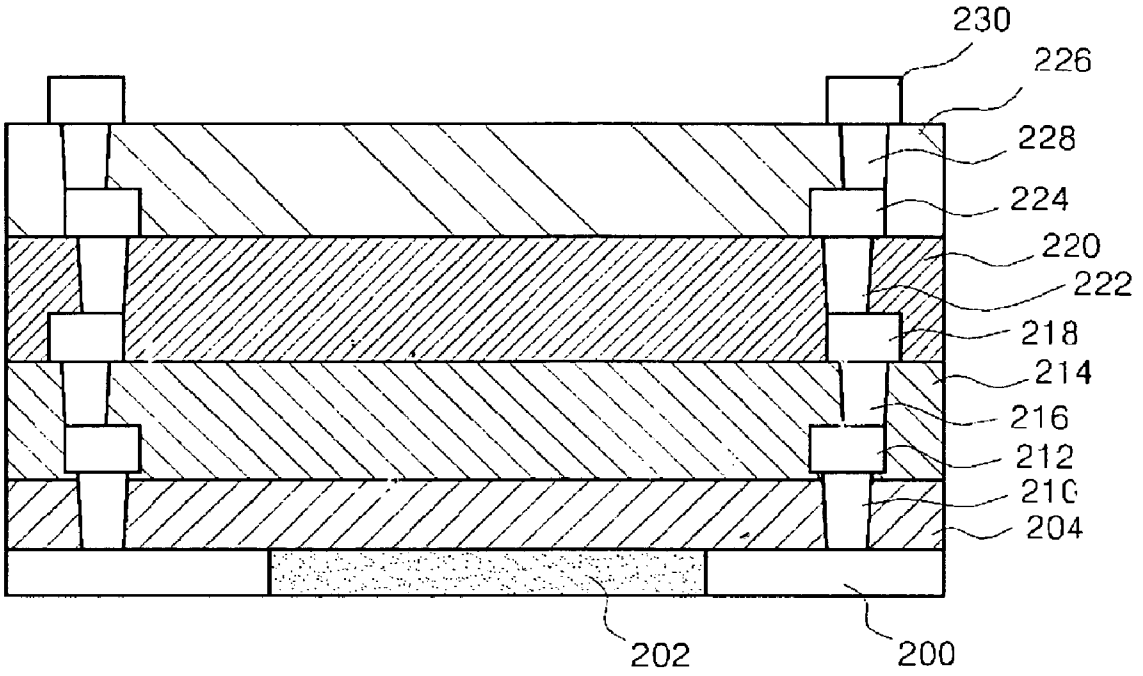

224
222
220
218
216
214
212
210
204
200
202

FIG.3g


230
226
228
224
220
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218
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FIG.4

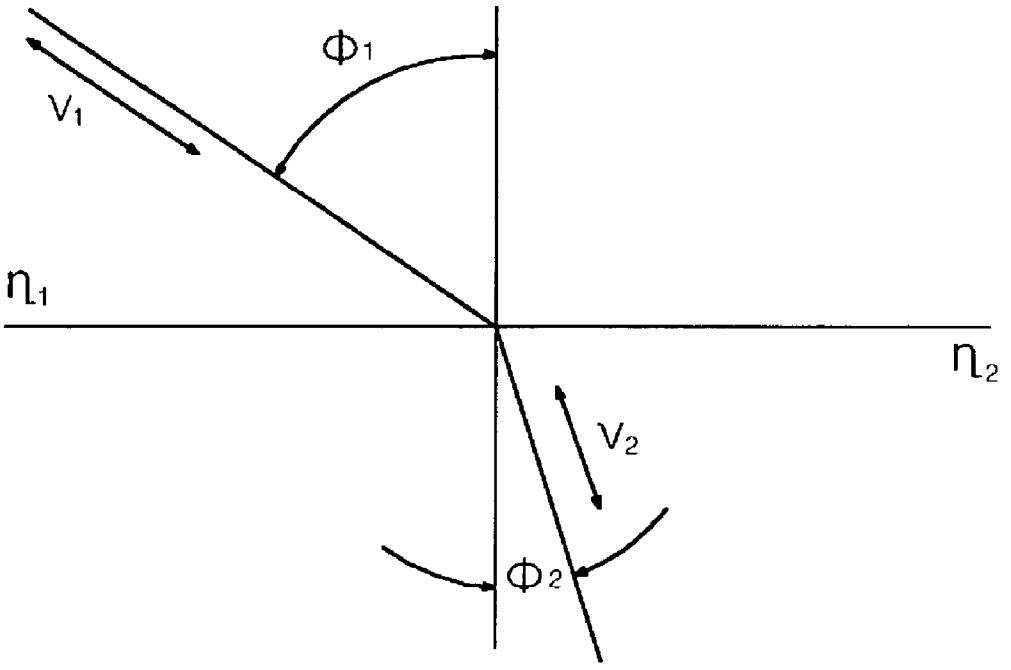

Φ1
V1
η1
η2
V2
Φ2

IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an image sensor and a method for manufacturing the same, and more particularly, to an image sensor, which is capable of increasing the light-collection efficiency of a photodiode, and a method for manufacturing the same.

2. Description of the Related Art

Generally, an image sensor is a semiconductor device that converts an optical image into an electric signal. Among the image sensors, a charge coupled device (CCD) is a device wherein each metal-oxide-silicon (hereinafter referred as to MOS) capacitor is closely located and charge carriers are stored into the MOS capacitor and transferred. A complementary metal oxide semiconductor (hereinafter referred as to CMOS) image sensor employs CMOS technology that uses a control circuit and a signal processing circuit as peripheral circuits to form as many arrays of MOS transistors as the number of pixels, and adopts a switching mode that detects outputs sequentially. MOS transistors formed in the peripheral circuit as the same number of pixels.

In manufacturing such a variety of image sensors, there have been many endeavors to increase the photosensitivity of the image sensor. Among those endeavors to increase the photosensitivity, a light-collecting technique is the most important technique.

The image sensor generally includes photosensitive circuit parts sensing light and CMOS logic circuit parts transforming the light into electric signals and generating data. Recently, there have been many studies of light-collecting techniques by which the pathways of the incident lights injecting to the regions other than the photosensitive circuit parts are changed and collected in photodiodes that are photosensitive elements.

FIG. **1** is a cross sectional view showing an image sensor in accordance with a prior art, in which the main components of a conventional CMOS image sensor are directly related to light-collection are illustrated.

Referring to FIG. **1**, the prior art image sensor includes a plurality of field insulating films **10** formed on a semiconductor substrate (not shown), at least one photodiode **12** which is an optical active region formed between these field insulating films **10**, multilayer interlayer insulating films **14** and **18** insulating between layers of the top parts of the field insulating films **10** and photodiode **12** and a light shield layer **16** formed of metal or the like in the interlayer insulating film **18** in order to prevent incident light from being focused onto the field insulating films **10**. An element-protecting film **20** is formed on the interlayer insulating film **18**, and an interlayer insulating film **24** is formed on the element-protecting film **20**. The color filter arrays **22***a*, **22***b* and **22***c* of red, green and blue are formed in the interlayer insulating film **24**. A flattening layer **26** is formed over these color filter arrays **22***a*, **22***b* and **22***c*. Microlenses **28** are formed at the positions corresponding to the color filters **22***a*, **22***b* and **22***c*.

As the materials of the color filters **22***a*, **22***b* and **22***c* of red, green and blue, mainly used are photoresists dyed in colors capable of absorbing only the light of a specific wavelength. As the materials of the microlenses **28**, mainly used are polymer type resins.

The interlayer insulating films **14**, **18** and **24** and the element-protecting film **20** are typically made by using silicon oxide films that are transparent insulating materials.

The flattening layer **26** is made by using a photoresist in order to compensate for the roughness of the color filters.

In the constructed conventional CMOS image sensor, the incident light received via the microlenses **28** is separated into corresponding red, green and blue light through the red color filter **22***a*, green color filter **22***b* and blue color filter **22***c*. The separated red, green and blue lights are focused on the photodiode **12** at the positions corresponding to the color filters through the element-protecting film **20** and the interlayer insulating films **14** and **18**, respectively. The light shield layer **16** arranged between the interlayer insulating films **14** and **18** plays the role of shielding the incident light so as not to deviate to other light pathways.

However, if the incident light on the photodiode through the microlenses **28** and the color filters **22***a*, **22***b* and **22***c* is not focused in parallel but focused to other light pathways, the photodiode **12** in the corresponding light pathway will be unable to sense the light or interference will occur with other adjacent photodiode **12**. Such a phenomenon acts as noise in embodying a high performance image in a CMOS image sensor.

SUMMARY OF THE INVENTION

The present invention is designed in consideration of the problems of the prior art, and therefore it is an object of the present invention to provide an image sensor which can improve the light-collection efficiency of the photodiode with an increased transmittance of vertical light reaching the photodiode by making the multi-layer interlayer insulating films have a lower density as they proceed upward to decrease the refraction angle of the incident light penetrated through the microlenses and color filters, and a method for manufacturing the same.

To achieve the above object, there is provided an image sensor in accordance with the present invention, comprising: at least one photodiode formed on a semiconductor substrate; multi-layer interlayer insulating films formed on the photodiode and stacked in at least two layers so that the density of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multi-layer interlayer insulating films proceed upward; a light shield layer and an element-protecting film sequentially stacked on the multi-layer interlayer insulating film; color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and microlenses arranged on the positions corresponding to the color filters on the flattening layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and aspects of the present invention will become apparent from the following description of embodiments with reference to the accompanying drawings in which:

FIG. **1** is a cross sectional view showing an image sensor in accordance with a prior art;

FIG. **2** is a cross sectional view showing the structure of an image sensor in accordance with the present invention;

FIGS. **3***a* to **3***g* are process views showing a process for manufacturing multi-layer wiring in multi-interlayer insulating films of the image sensor in accordance with the present invention; and

FIG. **4** is a view for explaining the difference of the index of refraction caused by a density difference in the multi-layer interlayer insulating film of the image sensor in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, a preferred embodiment of the present invention will be described in more detail referring to the drawings.

FIG. **2** is a cross sectional view showing the structure of an image sensor in accordance with the present invention, in which the main components of the CMOS image sensor of this invention directly related to light-collection are illustrated.

Referring to FIG. **2**, the CMOS image sensor of this invention includes a plurality of field insulating films **100** formed on a semiconductor substrate (not shown), at least one photodiode **102** which is an optical active region formed between these field insulating films **100**, multi-layer interlayer insulating films **104** and **108** insulating between layers of the top parts of the field insulating films **100** and photodiode **102** and being stacked in at least two layers so that the density is lower in upper parts than lower parts and a light shield layer **106** formed of metal or the like in the interlayer insulating film **108** in order to prevent an incident light from being focused onto the field insulating films **100**.

An element-protecting film **120** is formed on the interlayer insulating film **108**, and an interlayer insulating film **124** is formed on the element-protecting film **120**. The color filter arrays **122***a*, **122***b* and **122***c* of red, green and blue are formed in the interlayer insulating film **124**. A flattening layer **116** is formed over these color filter arrays **122***a*, **122***b* and **122***c*. Microlenses **128** are formed on the positions corresponding to the color filters **122***a*, **122***b* and **122***c*.

As the materials of the color filters **122***a*, **122***b* and **122***c* of red, green and blue, mainly used are photoresists dyed in colors capable of absorbing only the light of a specific wavelength. As the materials of the microlenses **128**, mainly used are polymer type resins. At this time, the interlayer insulating films **104** and **108** below the color filter arrays **122***a*, **122***b* and **122***c* are made so that the density of the interlayer insulating film in the upper side is lower than that of the interlayer insulating film in the lower side. For this, in the present invention, the density of an oxide film becomes higher in the order of PE-CVD<HDP-CVD<LP-CVD<thermal oxidation. Further, if the deposition temperature is lowered, the density of the oxide film is lowered. Accordingly, it is possible to carry out a density adjustment by this deposition process and by the adjustment of the deposition temperature. For example, in the manufacture of the interlayer insulating film **108** in the upper side, an oxide film is deposited by PE-CVD or HDP-CDP and in a low temperature range. On the contrary, in the manufacture of the interlayer insulating film **104** in the lower side, an oxide film is deposited by LP-CVD or a thermal oxidization process and deposited in the range of a higher temperature in comparison with the interlayer insulating film in the upper side. Also, it is possible to adjust the density of the upper interlayer insulating film **108** to be lower than that of the lower interlayer insulating film **104** by adjusting the deposition temperature while carrying out the same deposition process to all of the upper and lower interlayer insulating films **108** and **104**.

In the present invention, the interlayer insulating films **104** and **108** are transparent insulating materials and typically formed of silicon oxide films. At this time, the density can be lowered by increasing the concentration of impurities to be doped in the upper interlayer insulating film than in the lower interlayer insulating film. For example, if the interlayer insulating film **104** in the lower position is deposited with FSG, BPSG, PSG and BSG and the interlayer insulating film **108** in the upper position is deposited with USG, the density of the interlayer insulating film in the upper position becomes lower than that of the interlayer insulating film in the lower position.

The element-protecting film **120** is typically formed of a silicon oxide film that is a transparent insulating material, and the flattening layer **116** is formed of a photoresist in order to compensate for the roughness of the color filters.

In the CMOS image sensor of the above-described structure of the present invention, the incident light received via the microlenses **128** are separated into the corresponding red light, green light and blue light through the red color filter **122***a*, green color filter **122***b* and blue color filter **122***c*. The separated red, green and blue lights are focused on the photodiode **102** at the positions corresponding to the color filters through the element-protecting film **120** and the interlayer insulating films **108** and **104**. The light shield layer **106** arranged between the interlayer insulating films **104** and **108** plays a role of shielding the incident light so as not to deviate to other light pathways.

Further, according to the present invention, in the multi-layer interlayer insulating films **104** and **108** included in the CMOS image sensor, the density of the interlayer insulating film **108** in the upper position is lower than that of the interlayer insulating film **104** in the lower position. Due to this, the red, green and blue lights penetrated through the microlenses **128** and the color filters **122***a*, **122***b* and **122***c* are focused on the photodiode **102** in vertical light pathways without a light loss as the refraction angle on those interlayer insulating films **108** and **104** decreases until the incident lights are focused on the photodiode **102**. The light shield layer **106** arranged between the interlayer insulating films **108** and **104** plays a role of shielding the incident lights so as not to deviate to other light pathways.

As shown, in the present invention, a borderless contact or a photosensitivity adjusting film **105** is also formed of a silicon oxide film or the like below the multi-layer interlayer insulating films **104** and **108**. Also, a buffer insulating film **107** may be additionally formed of a silicon oxide film below the photosensitivity adjusting film.

Next, the process for manufacturing the thus constructed CMOS image sensor in accordance with the present invention will be described.

First, in order to insulate elements of the CMOS image sensor electrically, a field insulating film **100** is formed on a silicon substrate (not shown) and at least one photodiode **102** is formed in the gaps of the field insulating film **100**.

Next, an upper interlayer insulating film **104** having a large density is deposited on the entire surface of the field insulating film **100** and photodiode **102**, and a light shield layer **106** of metal or the like is formed thereon.

Continually, an upper interlayer insulating film **108** flattened and having a low density is formed over the entire surface of the lower interlayer insulating film **104** on which the light shield layer **106** is formed. Here, the adjusting processes of the deposition temperature and the impurity concentration in the deposition process for adjusting the density difference between the lower interlayer insulating film **104** and the upper interlayer insulating film **108** have been described above, the description thereof will be omitted.

Next, in order to protect the elements from moisture or scratching, a flattened element-protecting film **120** is formed on the entire surface of the upper interlayer insulating film **108**.

Then, a photoresist dyed in red, green and blue is applied onto the flattened element-protecting film **120** and developed, to form arrays of color filters **122***a*, **122***b* and **122***c* of red, green and blue, and then form a flattened interlayer insulating film **124** on the sides of the color filter arrays **122***a*, **122***b* and **122***c*. On the entire surface of the resultant material, a flattening layer **116** for flattening and adjusting the focal distance is formed. Next, microlenses **128** are formed on the flattening layer **116** at the positions corresponding to the red, green and blue color filters **122***a*, **122***b* and **122***c*.

FIGS. **3***a* to **3***g* are views showing a process for manufacturing multi-layer wiring in multi-layer interlayer insulating films of the image sensor in accordance with the present invention.

First, as shown in FIG. **3***a*, a field insulating film **200** for electrically insulating elements of a CMOS image sensor formed on a semiconductor substrate (not shown), and at least one photodiode **202** is formed in the gaps of the interlayer insulating film **200**. Next, a BPSG having a high rate of flow is deposited at 2000 to 15000 Å on the field insulating film **200** and photodiode **202**, and its surfaces are polished by chemical mechanical polishing (CMP) to thus forming a first interlayer insulating film **204** of 2000 to 9000 Å and then flatten it.

Next, as shown in FIG. **3***b*, HDP-USG is deposited at 300 to 9000 Å to form a second interlayer insulating film **206** having a high density. Then, the second and first interlayer insulating films **206** and **204** are etched to form contact holes **208**.

Continually, glue layer/barrier metal layer (not shown) such as Ti/TiN are deposited on the contact holes **208**. As shown in FIG. **3***c*, metal such as tungsten, etc. is buried and patterned to form first contacts **210** and metal wires **212**. Next, HDP-FSG is deposited at 9000 to 40000 Å to form a third interlayer insulating film **214** having a lower density than the second interlayer insulating film **206** and flatten the surface thereof by CMP.

Next, as shown in FIG. **3***d*, via holes are formed on the third interlayer insulating film **214** and tungsten plugs **216** and second metal wires **218** connected to the first metal wires **212** in the lower position are formed in the via holes.

Continually, as shown in FIG. **3***e*, PE-USG is deposited at 3000 to 8000 Å to form a fourth interlayer insulating film **220** having a lower density than the third interlayer insulating film **214** and flatten the surface thereof by CMP.

Continually, as shown in FIG. **3***f*, via holes are formed on the fourth interlayer insulating film **220** and tungsten plugs **222** and second metal wires **224** connected to the second metal wires **218** in the lower position are formed in the via holes.

Next, as shown in FIG. **3***g*, PE-FSG is deposited at 500 to 20000 Å to form a fifth interlayer insulating film **226** having a lower density than the fourth interlayer insulating film **220** and flatten the surface thereof by CMP. Afterwards, tungsten plugs **228** and fourth metal wires **230** connected to the third metal wires **224** in the upper position are formed in the fifth interlayer insulating film **226**.

As seen above, in the multi-layer interlayer insulating films of the CMOS image sensor of FIG. **2** and in the multi-layer interlayer insulating films having multi-layer metal wirings of FIGS. **3***a* to **3***g*, the density of the interlayer insulating film is lower in the upper position than in the lower position, thus making it possible to lower the refraction angle of an incident light.

FIG. **4** is a view for explaining the difference of the index of refraction caused by a density difference in the multi-layer interlayer insulating film of the image sensor in accordance with the present invention. In this drawing, the density is n**1**<n**2** and has a size of Φ**1**(incident angle)>Φ**2**(refraction angle). Herein, the incident light injected to a medium n**2** having a high density from a medium n**1** having a low density has a refraction angle Φ2 smaller than the incident angle Φ**1**.

Subsequently, in the multi-layer interlayer insulating film of the present invention, the density of the interlayer insulating film in the upper position is lower than that of the interlayer insulating film in the lower position. Resultantly, since the density of the interlayer insulating film in the upper position becomes lower than that of the interlayer insulating film in the lower position as the multi-layer interlayer insulating films proceed upward, the refraction angle of the incident light becomes smaller and smaller. Due to this, while the light penetrated through the microlenses and color filters reaches the photodiode in a lower position, the refraction angle becomes smaller and smaller by the multi-layer interlayer insulating film whose density difference gradually increases, and thereby the light is not refracted to other light pathways but reaches the photodiode at a right angle.

As described above, the present invention can improve the light-collection efficiency of the photodiode with an increased transmittance of a vertical light reaching to the photodiode by making the multi-layer interlayer insulating films have a lower density as they proceed upward to decrease the refraction angle of the incident light penetrated through the microlenses and color filters. Accordingly, the optical properties of the image sensor can be enhanced because the loss of the light as being refracted to other light pathways can be minimized.

While the present invention has been described with respect to certain preferred embodiment only, other modifications and variations may be made without departing from the spirit and scope of the present invention as set forth in the following claims

What is claimed is:

1. An image sensor, comprising:

at least one photodiode formed on a semiconductor substrate;

multi-layer interlayer insulating films formed on the photodiode and stacked in at least two layers of oxide film having different density and the refractive index so that the density and the refractive index of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multi-layer interlayer insulating films proceed upward;

a light shield layer and an element-protecting film sequentially stacked on the multi-layer interlayer insulating film;

color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and

microlenses arranged on the positions corresponding to the color filters on the flattening layer.

2. The image sensor of claim **1**, wherein the density of the oxide films becomes higher in the order of PE-CVD<HDP-CVD<LP-CVD<thermal oxidations.

3. The image sensor of claim **1**, multi-layer wiring is vertically formed on the multi-layer interlayer insulating films, the element-protecting film and the flattening layer.

4. The image sensor of claim **1**, further comprising a photosensitivity adjusting film formed below the multi-layer interlayer insulating films.

5. The image sensor of claim **4**, further comprising a buffer insulating film formed below the photosensitivity adjusting film.

6. A method for manufacturing an image sensor, comprising the steps of:

making at least one photodiode on a semiconductor substrate;

forming on the photodiode multi-layer interlayer insulating films stacked in at least two layers of oxide film having different density and the refractive index so that the density and the refractive index of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multi-layer interlayer insulating films proceed upward;

forming a light shield layer and an element-protecting film sequentially stacked on the multi-layer interlayer insulating film;

forming color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and

forming microlenses arranged on the positions corresponding to the color filters on the flattening layer.

7. The method of claim **6**, wherein the density of the oxide films becomes higher in the order of PE-CVD<HDP-CVD<LP-CVD<thermal oxidation.

8. The method of claim **7**, wherein the density of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film by adjusting the deposition process, the deposition temperature and the concentration of impurities doped on the interlayer insulating films.

9. The method of claim **6**, wherein the multi-layer interlayer insulating films are formed of oxides and the density is lowered by making the concentration of impurities to be doped higher in the upper interlayer insulating film than in the lower interlayer insulating film.

10. The method of claim **6**, further comprising the step of forming multi-layer wiring in the step of forming the multi-layer interlayer insulating films, the element-protecting film and the flattening layer.

11. The method of claim **6**, further comprising the step of forming a photosensitivity adjusting film below the multi-layer interlayer insulating films.

12. The method of claim **11**, further comprising the step of forming a buffer insulating film below the photosensitivity adjusting film.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

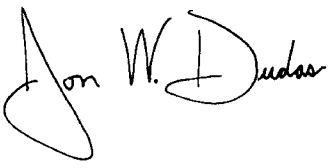
PATENT NO. : 7,365,298 B2
APPLICATION NO. : 10/945182
DATED : April 29, 2008
INVENTOR(S) : Sang Wook Ryu

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 6, line 58, "oxidations" should be -- oxidation --.

Signed and Sealed this

Second Day of September, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT F

US006754195B2

(12) **United States Patent**
Webster et al.

(10) **Patent No.: US 6,754,195 B2**
(45) **Date of Patent: Jun. 22, 2004**

(54) **WIRELESS COMMUNICATION SYSTEM CONFIGURED TO COMMUNICATE USING A MIXED WAVEFORM CONFIGURATION**

(75) Inventors: **Mark A. Webster**, Indian Harbour Beach, FL (US); **Michael J. Seals**, Melbourne, FL (US)

(73) Assignee: **Intersil Americas Inc.**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) bydays.days.

(21) Appl. No.: **10/143,134**

(22) Filed: **May 10, 2002**

(65) **Prior Publication Data**

US 2003/0012160 A1 Jan. 16, 2003

Related U.S. Application Data

(60) Provisional application No. 60/306,438, filed on Jul. 6, 2001.

(51) **Int. Cl.**[7] **H04B 7/216**; H04Q 7/24

(52) **U.S. Cl.** **370/335**; 370/338; 370/342

(58) **Field of Search** 370/204, 205, 370/206, 208, 480, 482, 486, 487, 503; 375/260, 340

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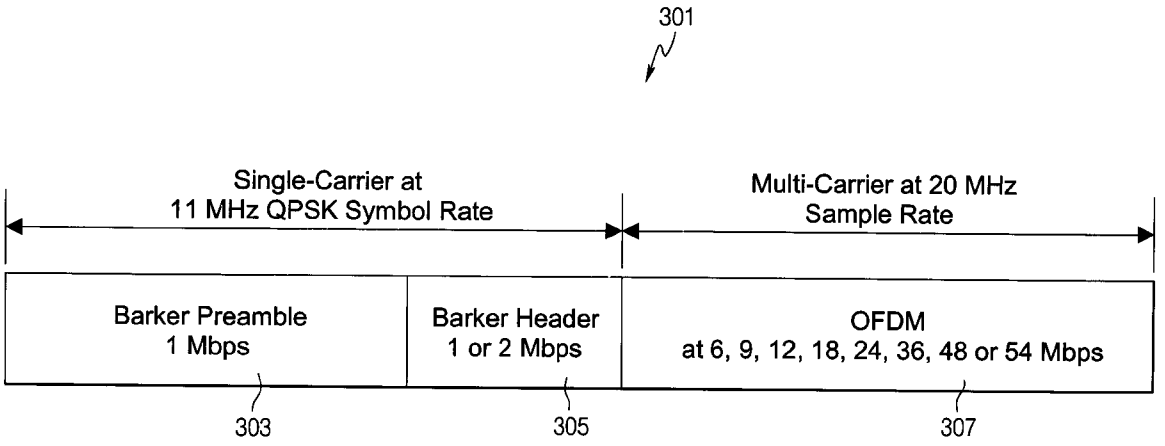
(List continued on next page.)

Primary Examiner—Wellington Chin
Assistant Examiner—William Schultz
(74) *Attorney, Agent, or Firm*—Gary R Stanford

(57) **ABSTRACT**

A wireless communication system configured to communicate using a mixed waveform configuration. The mixed waveform includes a first portion modulated according to a single-carrier scheme with a preamble and header and a second portion modulated according to a multi-carrier scheme. The waveform is specified so that a CIR estimate obtainable from the first portion is reusable for acquisition of the second portion by the receiver. The transmitter may include first and second kernels and a switch, where switch selects the first kernel for the first portion and the second kernel for the second portion to develop a transmit waveform. The receiver may include a single-carrier receiver, a multi-carrier receiver, and a switch that provides a first portion of a signal being received to the single-carrier receiver and a second portion of the signal being received to the multi-carrier receiver.

23 Claims, 18 Drawing Sheets



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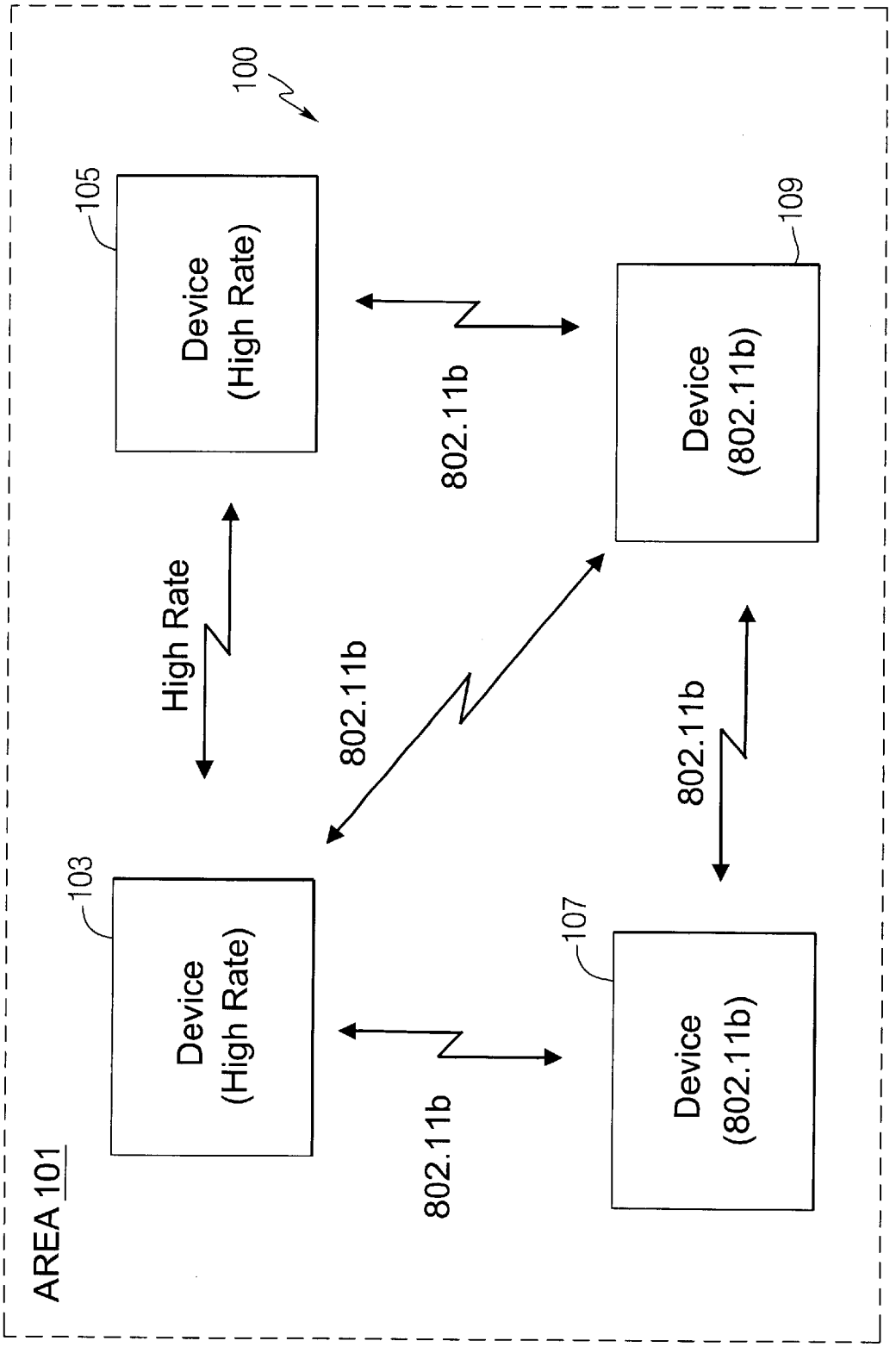

100
105
Device
(High Rate)
109
Device
(802.11b)
802.11b
High Rate
802.11b
802.11b
103
Device
(High Rate)
107
Device
(802.11b)
802.11b
AREA 101

FIG. 1

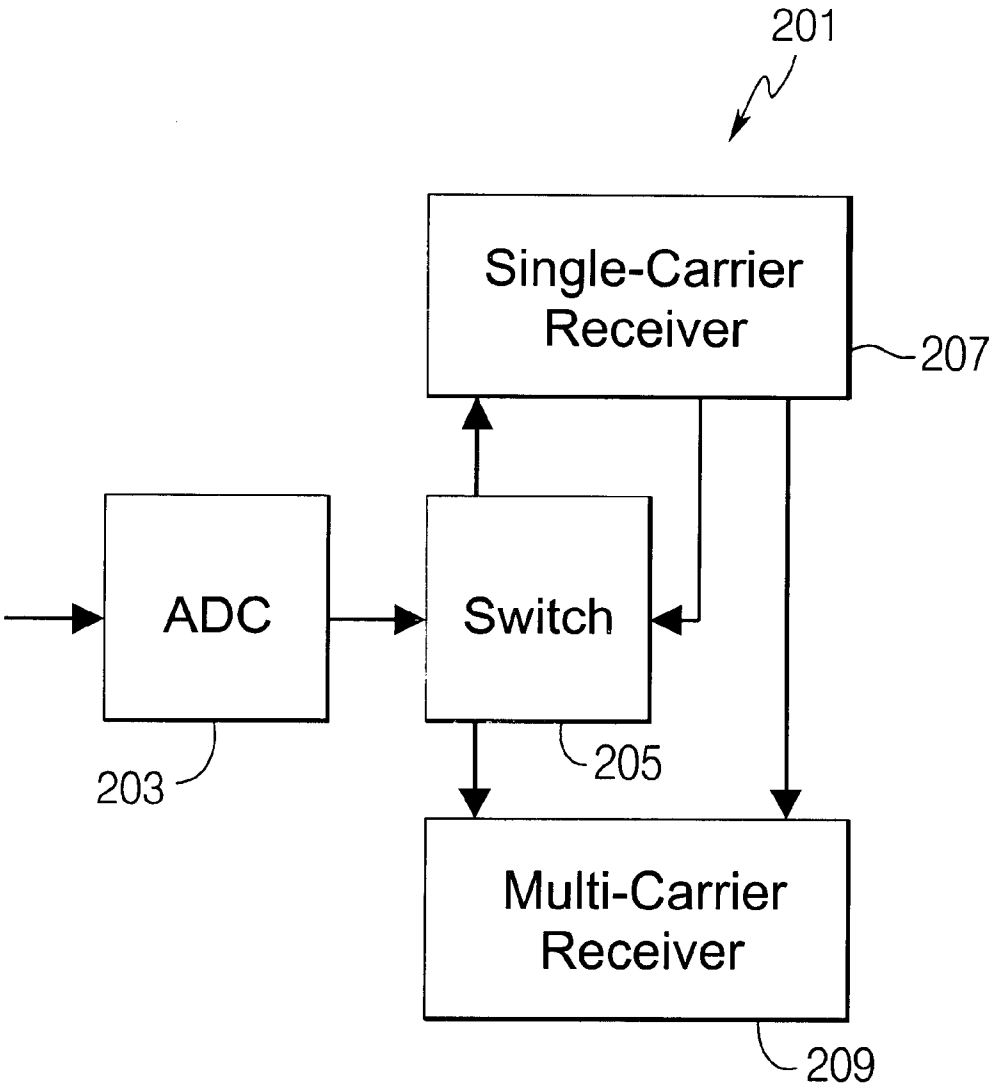

201
Single-Carrier Receiver
207
ADC
Switch
203
205
Multi-Carrier Receiver
209

FIG. 2

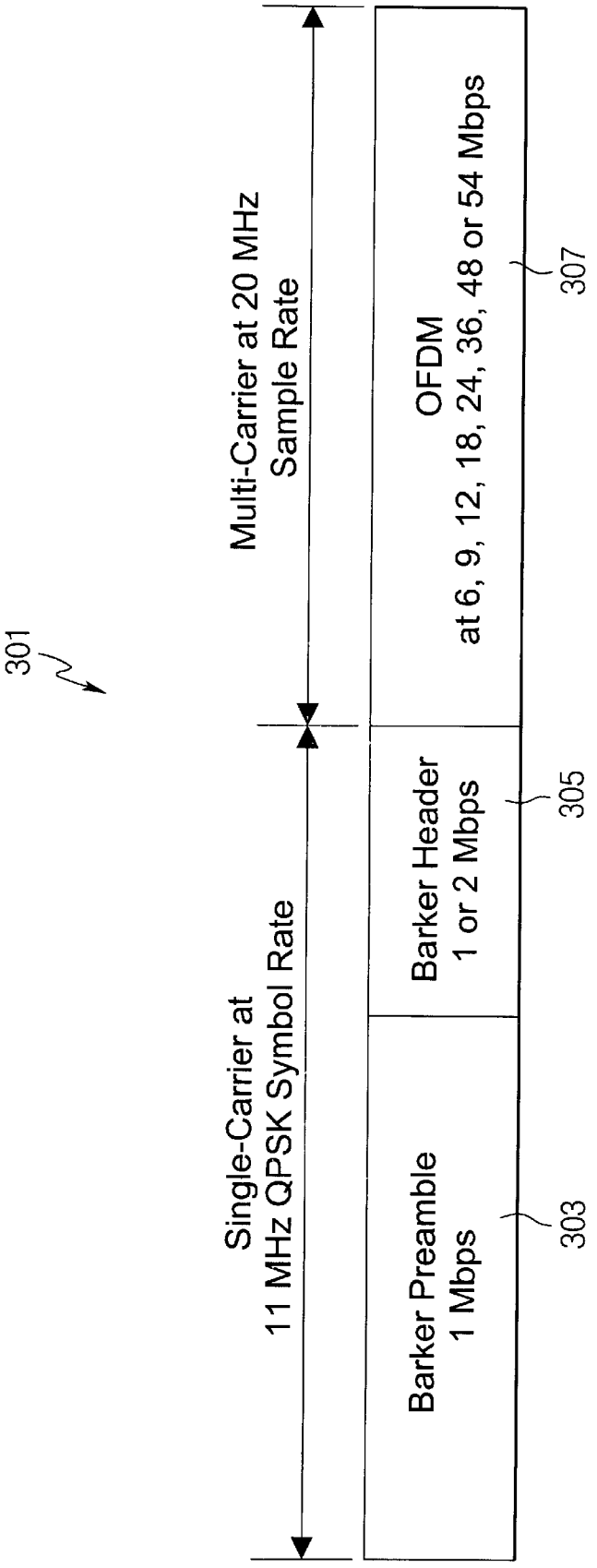

301
Multi-Carrier at 20 MHz
Sample Rate
Single-Carrier at
11 MHz QPSK Symbol Rate
OFDM
at 6, 9, 12, 18, 24, 36, 48 or 54 Mbps
307
Barker Header
1 or 2 Mbps
305
Barker Preamble
1 Mbps
303

FIG. 3

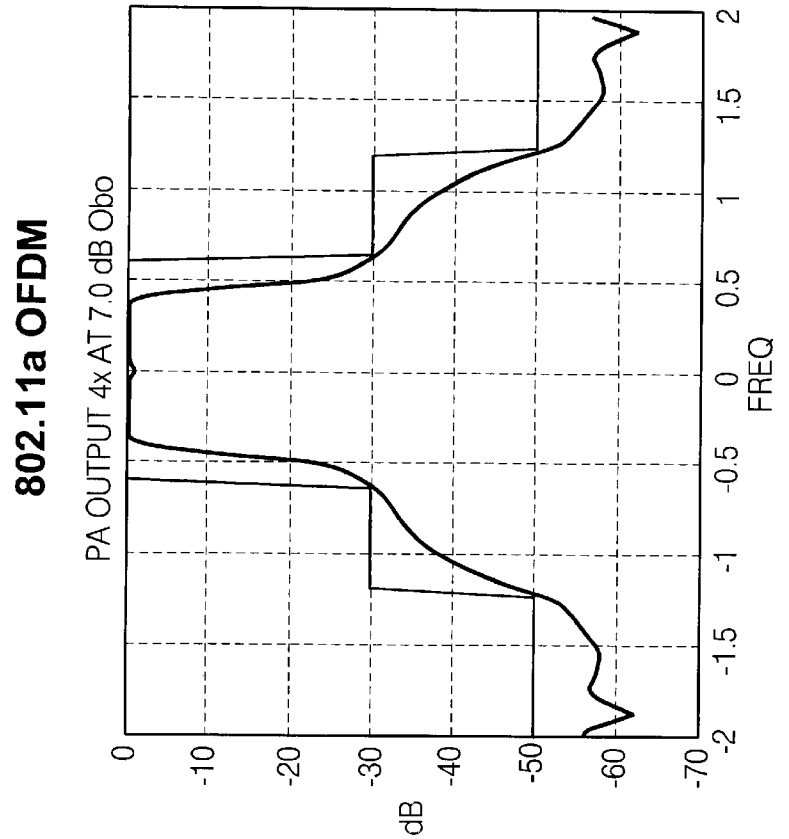

802.11a OFDM
PA OUTPUT 4x AT 7.0 dB Obo
0
-10
-20
-30
-40
-50
-60
-70
dB
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
FREQ

FIG. 4B

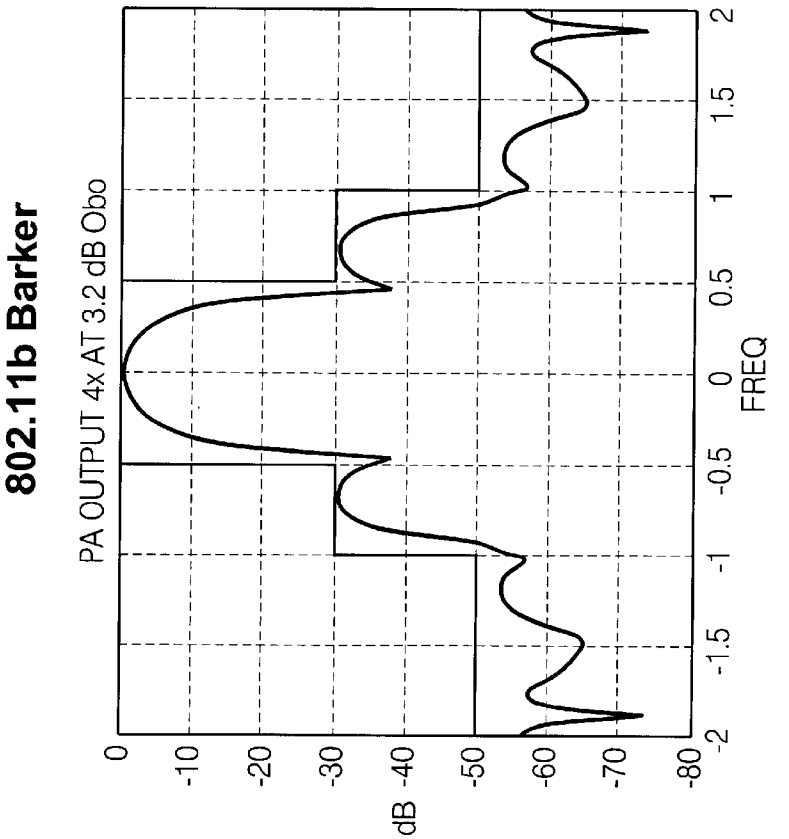

802.11b Barker
PA OUTPUT 4x AT 3.2 dB Obo
0
-10
-20
-30
-40
-50
-60
-70
-80
dB
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
FREQ

FIG. 4A

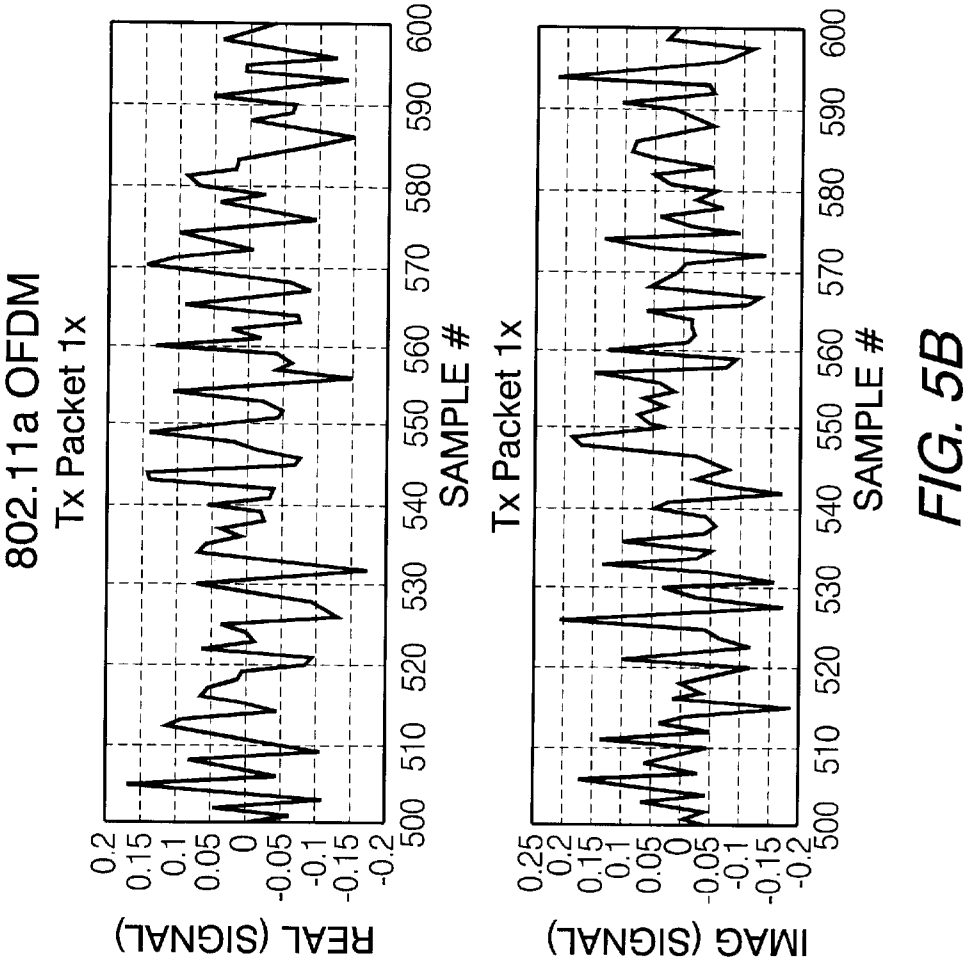

802.11a OFDM
Tx Packet 1x
REAL (SIGNAL)
SAMPLE #
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
500
510
520
530
540
550
560
570
580
590
600
Tx Packet 1x
IMAG (SIGNAL)
SAMPLE #
0.25
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2

FIG. 5B

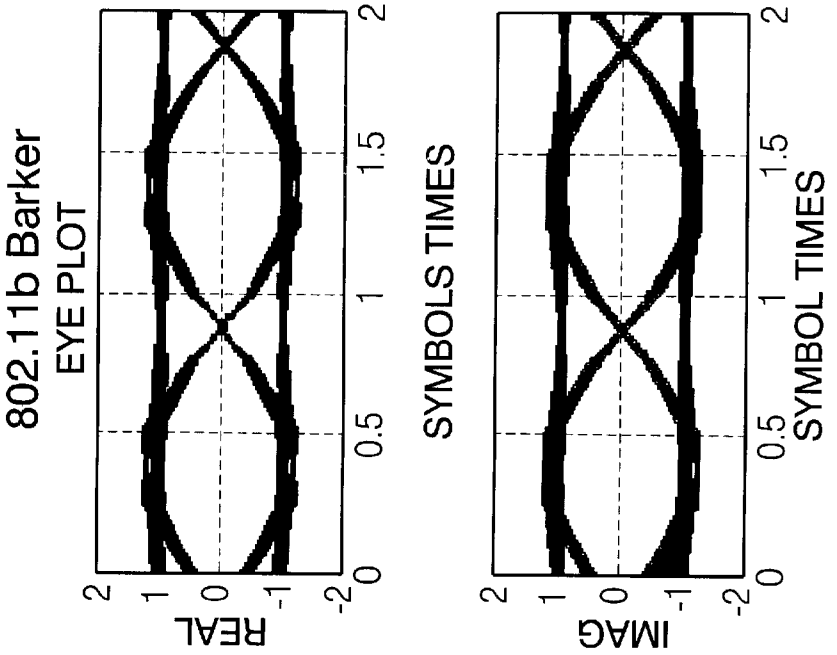

802.11b Barker
EYE PLOT
REAL
2
1
0
-1
-2
0
0.5
1
1.5
2
SYMBOLS TIMES
IMAG
SYMBOL TIMES

FIG. 5A

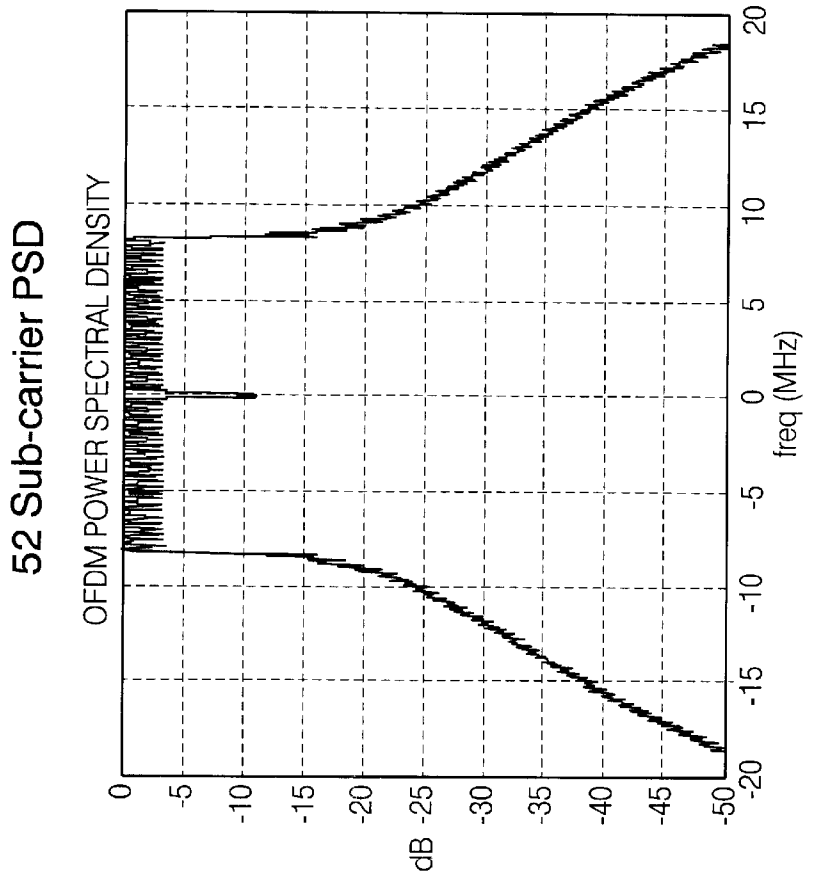

52 Sub-carrier PSD
OFDM POWER SPECTRAL DENSITY
dB
freq (MHz)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
20
15
10
5
0
-5
-10
-15
-20

FIG. 6B

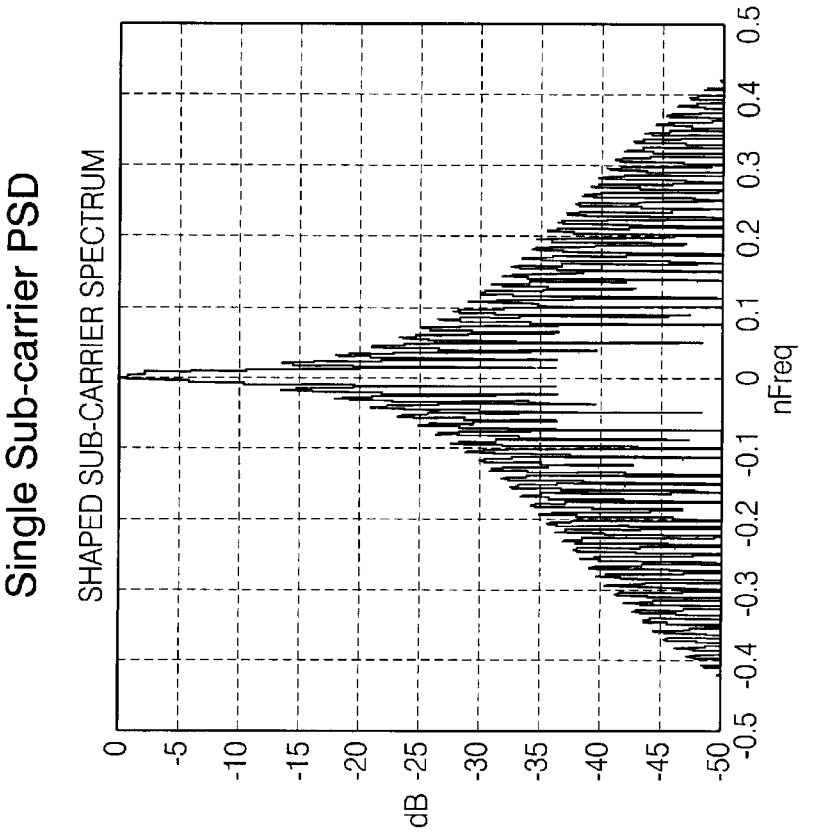
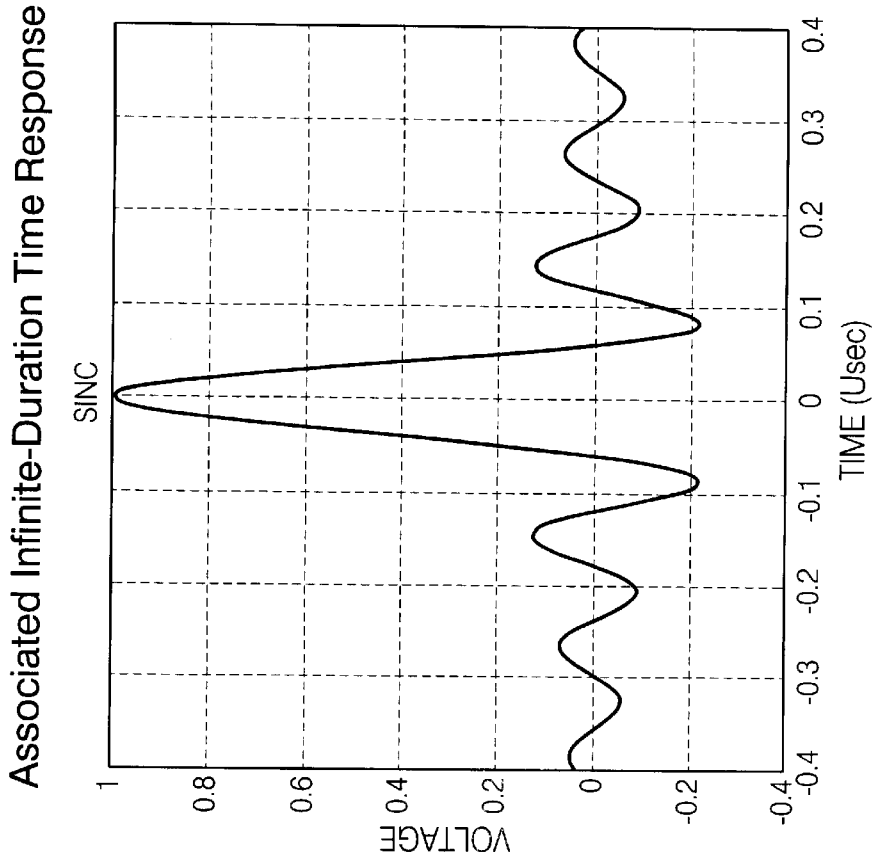

Single Sub-carrier PSD
SHAPED SUB-CARRIER SPECTRUM
dB
nFreq
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5

FIG. 6A



$$h_{IdealBW}(t) = f_W \frac{\sin(\pi f_W t)}{\pi f_W t} = f_W sinc(f_W t),$$

$$where\ f_W = 52(20/64)MHz$$

FIG. 7B

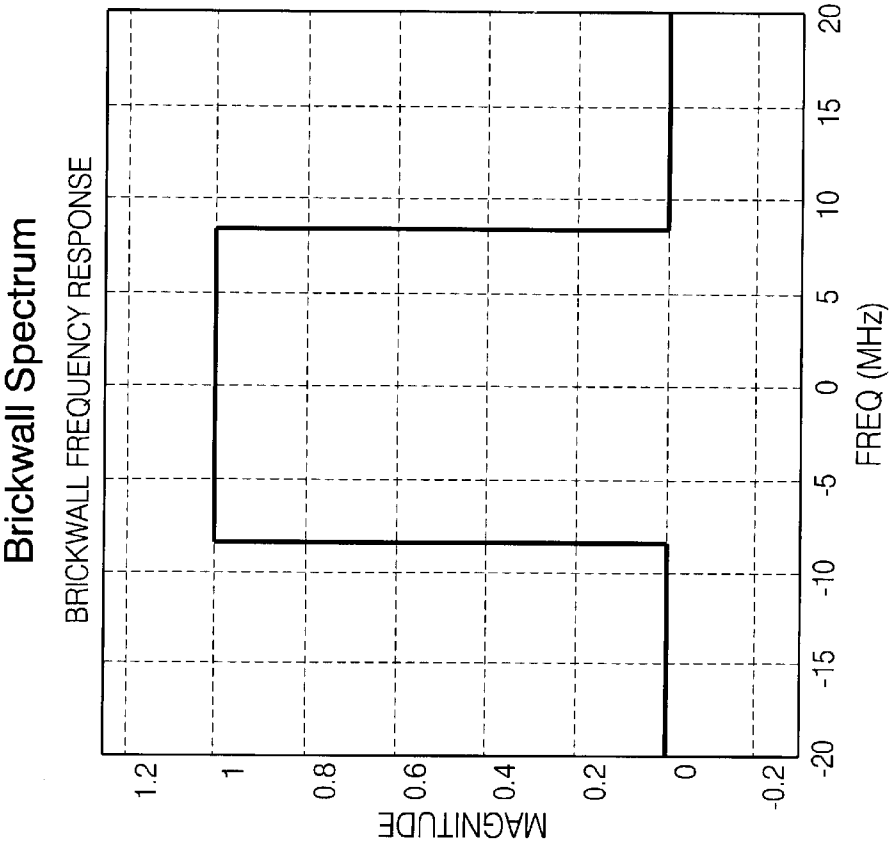


FIG. 7A

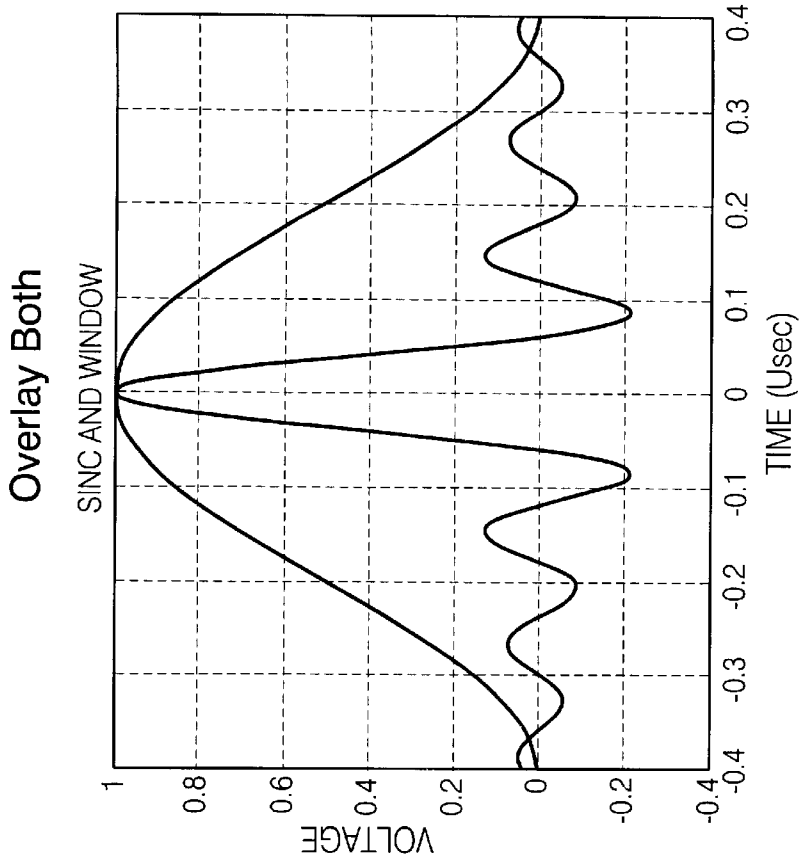
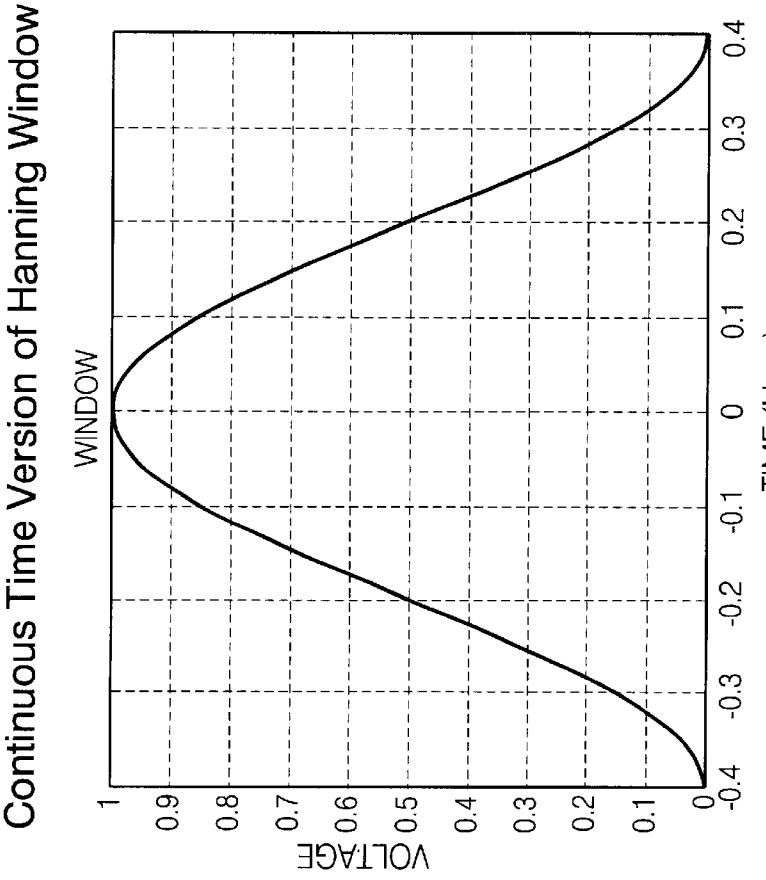


FIG. 9



$$h_{Window}(t) = 0.5\left[1+\cos\left(2\pi\frac{t}{T_{SPAN}}\right)\right],$$

where $T_{SPAN} = 0.8$ *usecs*

FIG. 8

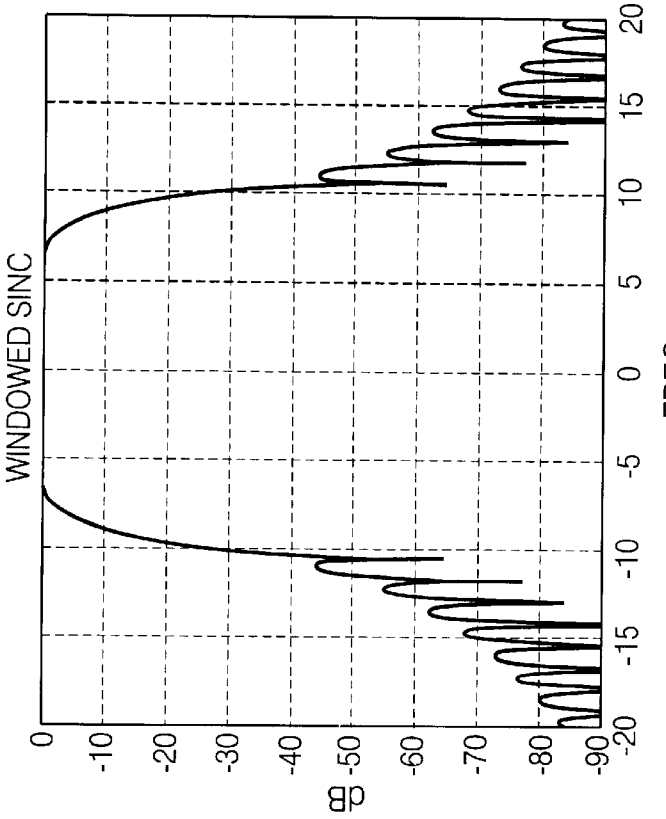
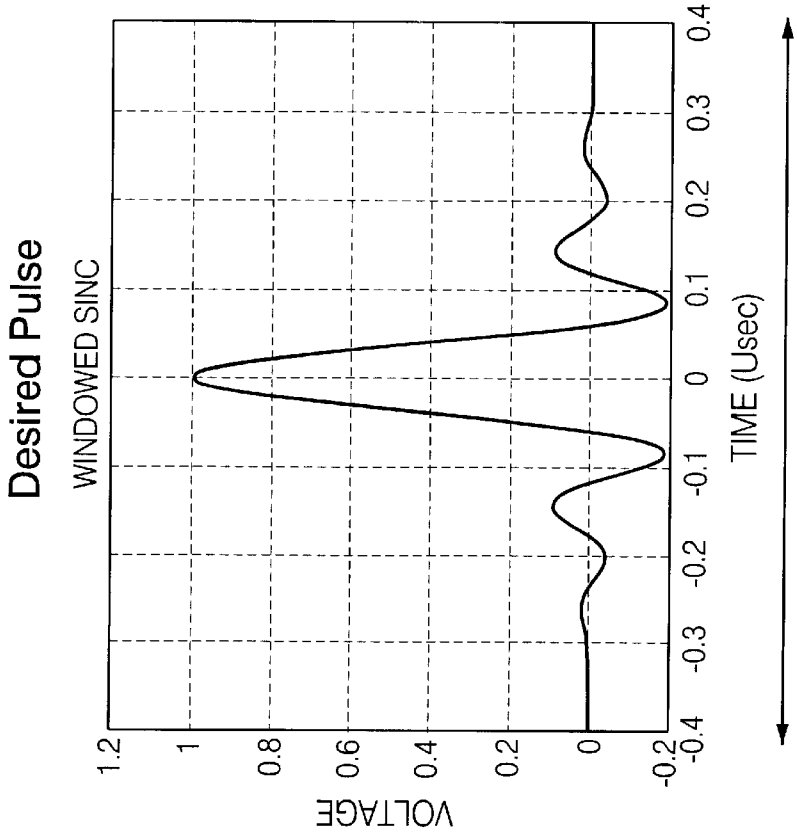


FIG. 11



$$p(t) = h_{Window}(t)\, h_{IdealBW}(t)$$

FIG. 10

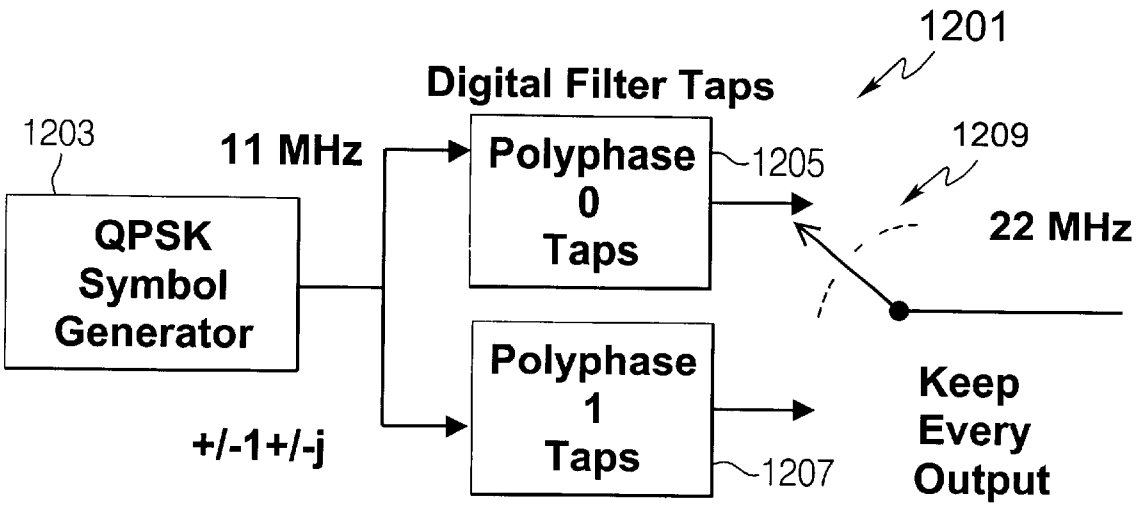

1201
Digital Filter Taps
1203
11 MHz
Polyphase 0 Taps
1205
1209
22 MHz
QPSK Symbol Generator
Polyphase 1 Taps
Keep Every Output
+/-1+/-j
1207

FIG. 12

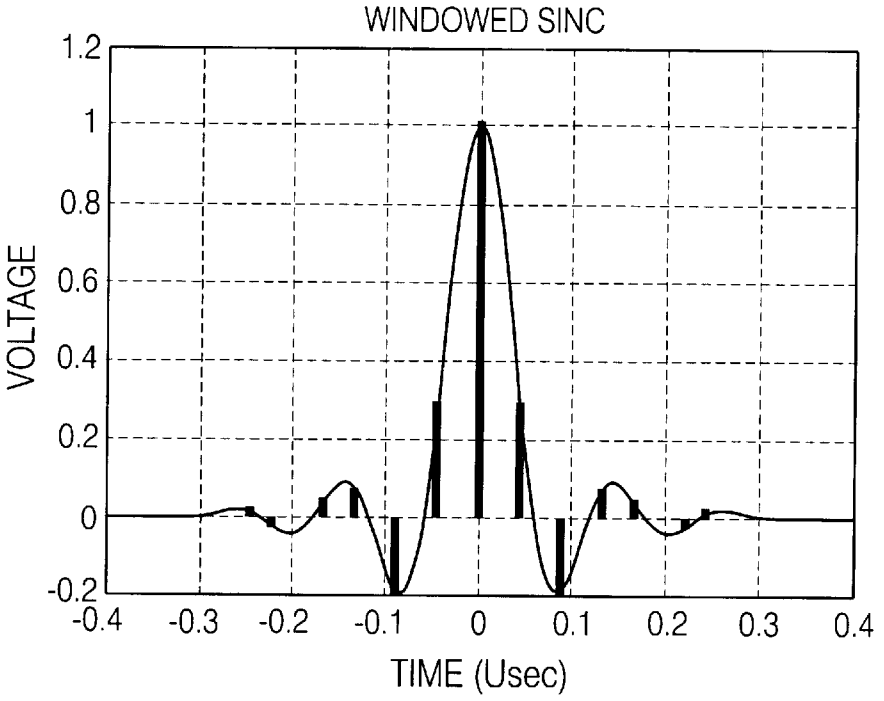

WINDOWED SINC
VOLTAGE
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
TIME (Usec)

FIG. 13

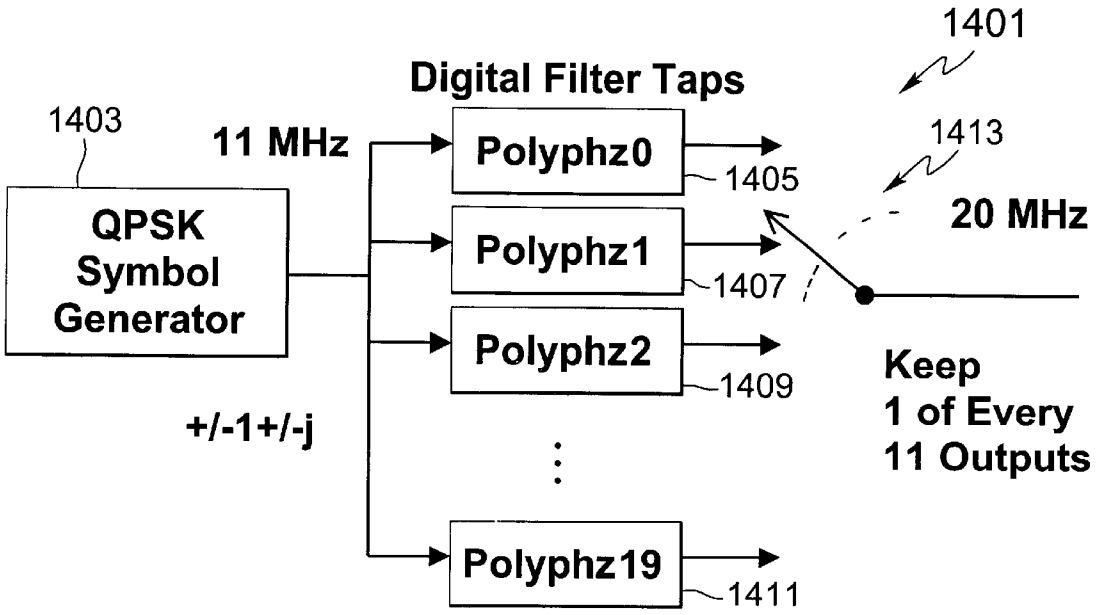

1401
Digital Filter Taps
1403
11 MHz
Polyphz0
1405
1413
20 MHz
QPSK
Symbol
Generator
Polyphz1
1407
Polyphz2
1409
Keep
1 of Every
11 Outputs
+/-1+/-j
Polyphz19
1411

FIG. 14

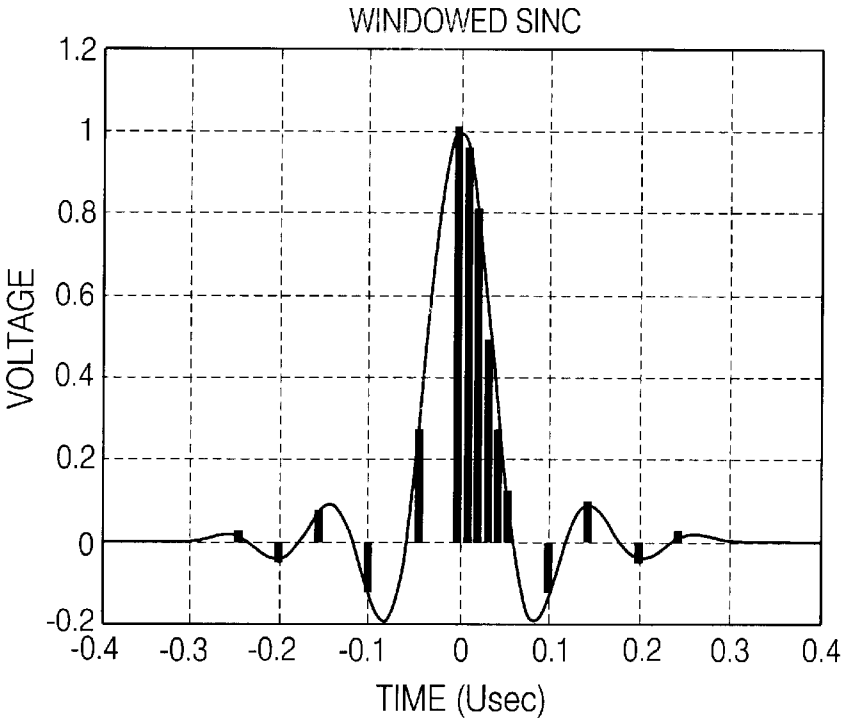

WINDOWED SINC
VOLTAGE
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
TIME (Usec)

FIG. 15

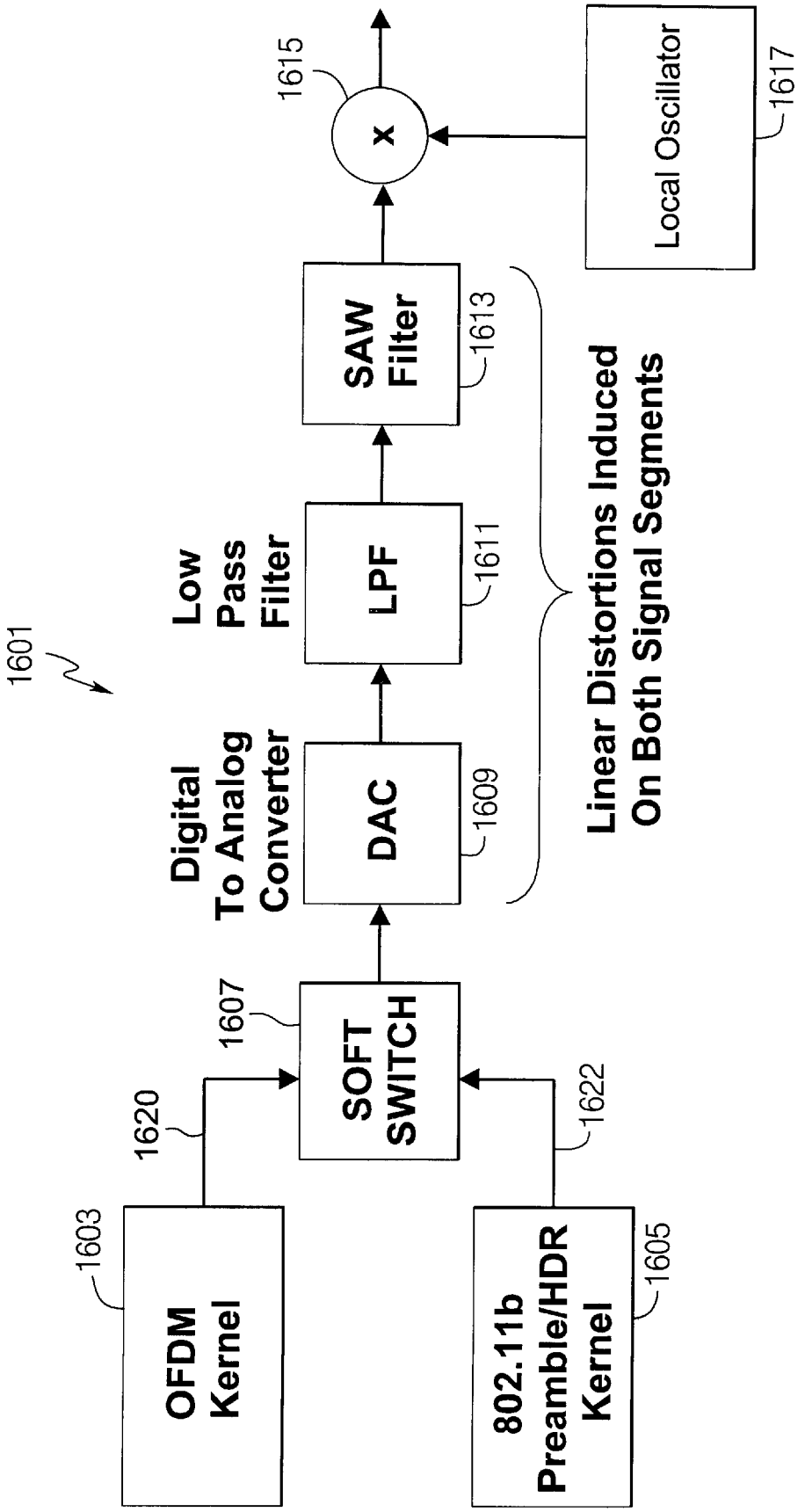

1601
OFDM Kernel
1603
802.11b Preamble/HDR Kernel
1605
1620
1622
SOFT SWITCH
1607
DAC
1609
LPF
1611
SAW Filter
1613
x
1615
Local Oscillator
1617
Digital To Analog Converter
Low Pass Filter
Linear Distortions Induced On Both Signal Segments

FIG. 16

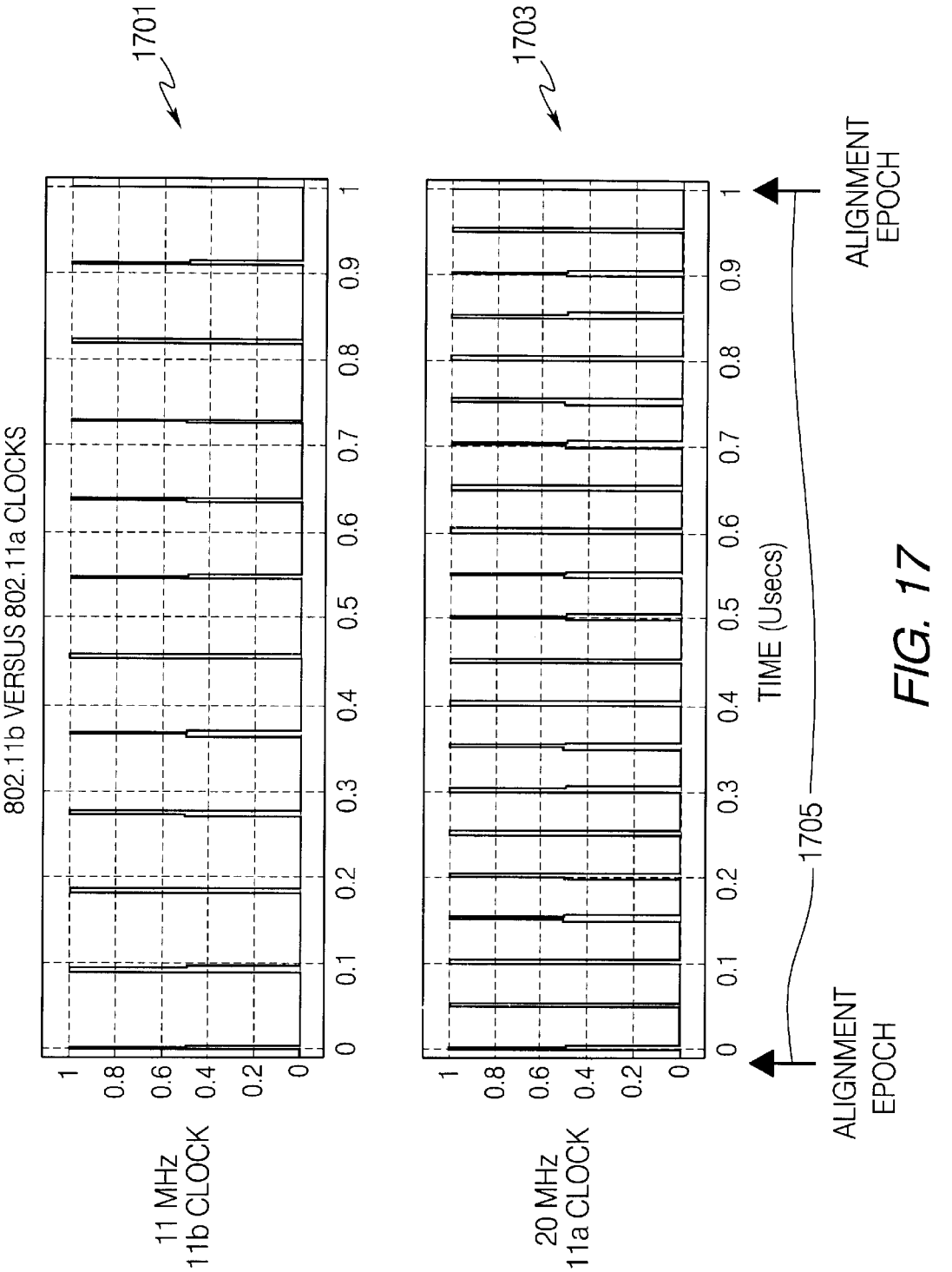

1701
1703
802.11b VERSUS 802.11a CLOCKS
11 MHz
11b CLOCK
20 MHz
11a CLOCK
TIME (Usecs)
ALIGNMENT
EPOCH
ALIGNMENT
EPOCH
1705
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
0.2
0.4
0.6
0.8
1

FIG. 17

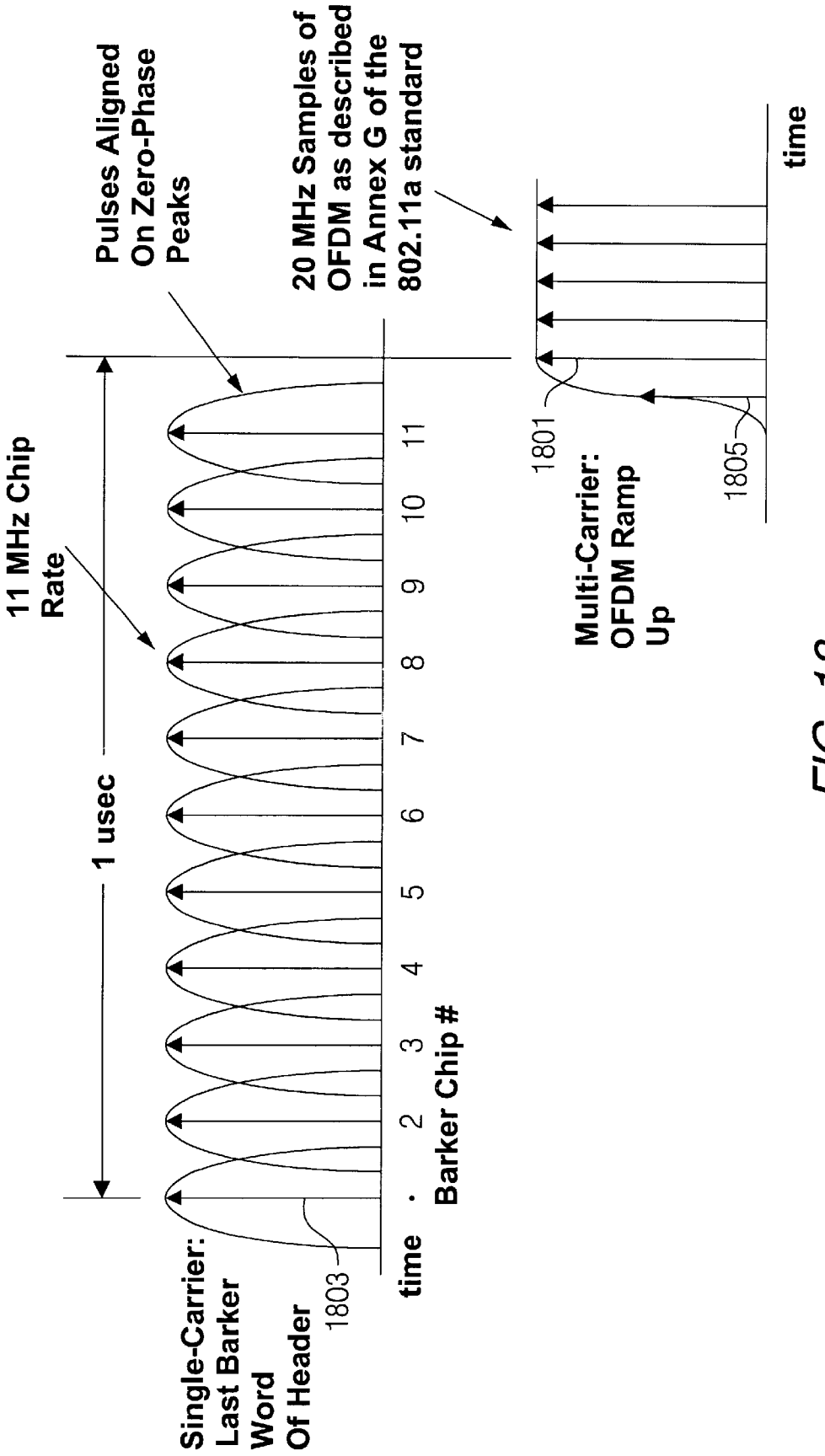

Pulses Aligned On Zero-Phase Peaks
20 MHz Samples of OFDM as described in Annex G of the 802.11a standard
11 MHz Chip Rate
1 usec
Single-Carrier: Last Barker Word Of Header
1803
time
Barker Chip #
1
2
3
4
5
6
7
8
9
10
11
1801
1805
Multi-Carrier: OFDM Ramp Up
time

FIG. 18

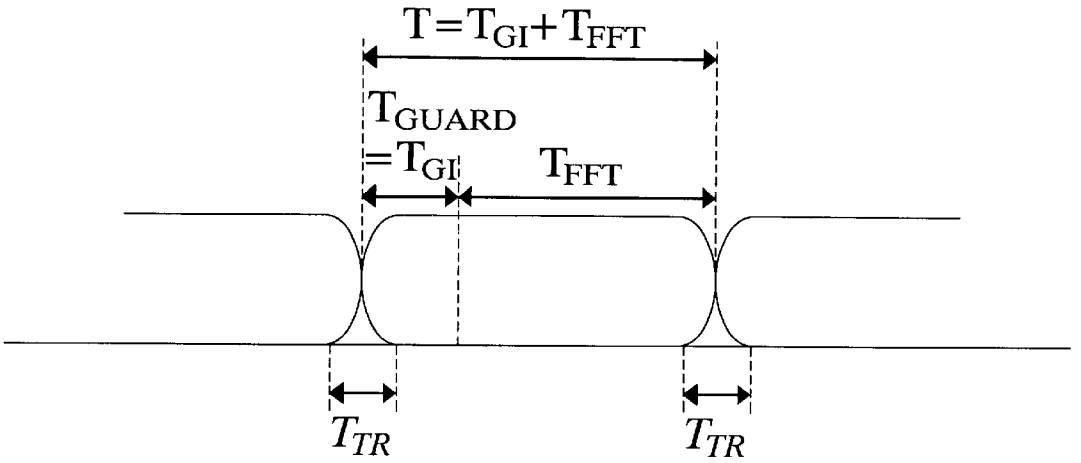

T=TGI+TFFT
TGUARD
=TGI
TFFT
TTR
TTR

FIG. 19

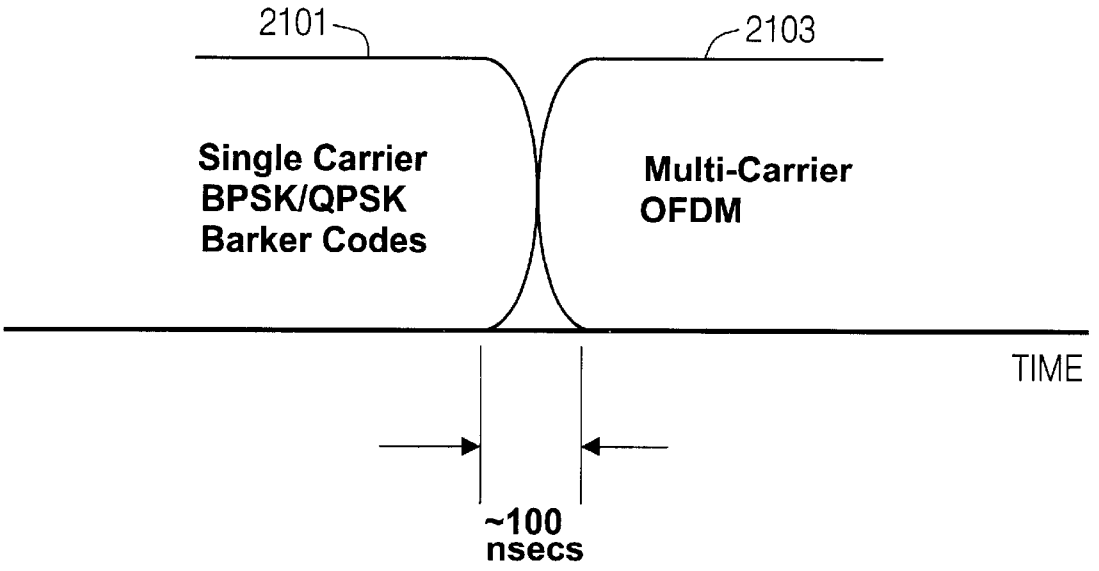

2101
2103
Single Carrier
BPSK/QPSK
Barker Codes
Multi-Carrier
OFDM
TIME
~100
nsecs

FIG. 21

$$w_T(t)=\sin^2\left[\frac{\pi}{2}\left(0.5+\frac{t}{T_{TR}}\right)\right] \quad for \quad \left(-\frac{T_{TR}}{2}<t<\frac{T_{TR}}{2}\right)$$

$$w_T(t)=1 \quad for \quad \left(\frac{T_{TR}}{2}<t<T-\frac{T_{TR}}{2}\right)$$

$$w_T(t)=\sin^2\left[\frac{\pi}{2}\left(0.5-\frac{(t-T)}{T_{TR}}\right)\right] \quad for \quad \left(T-\frac{T_{TR}}{2}<t<T+\frac{T_{TR}}{2}\right)$$

where TTR is the Transition Duration

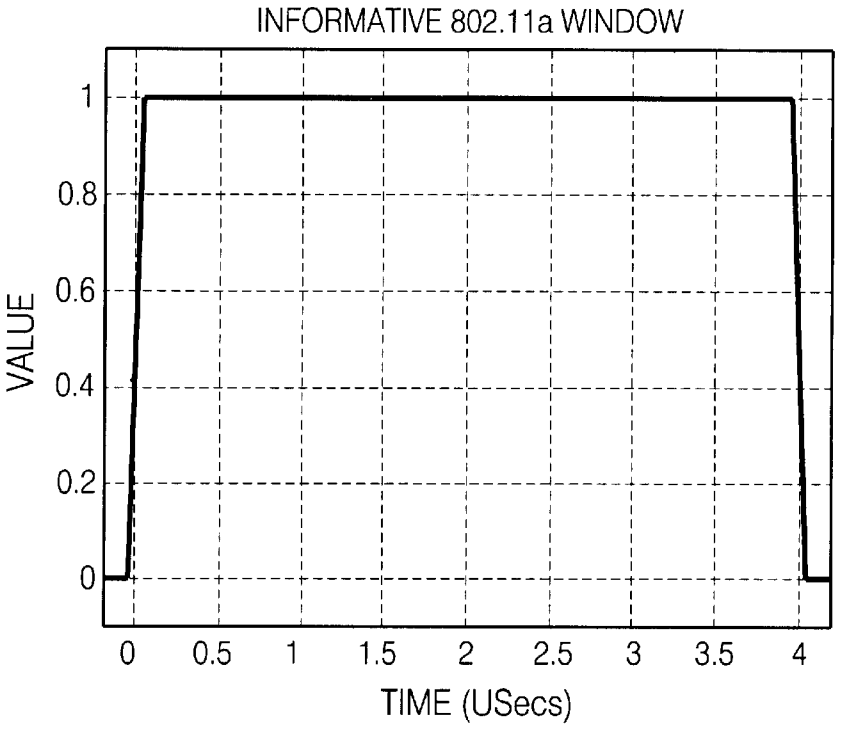


FIG. 20

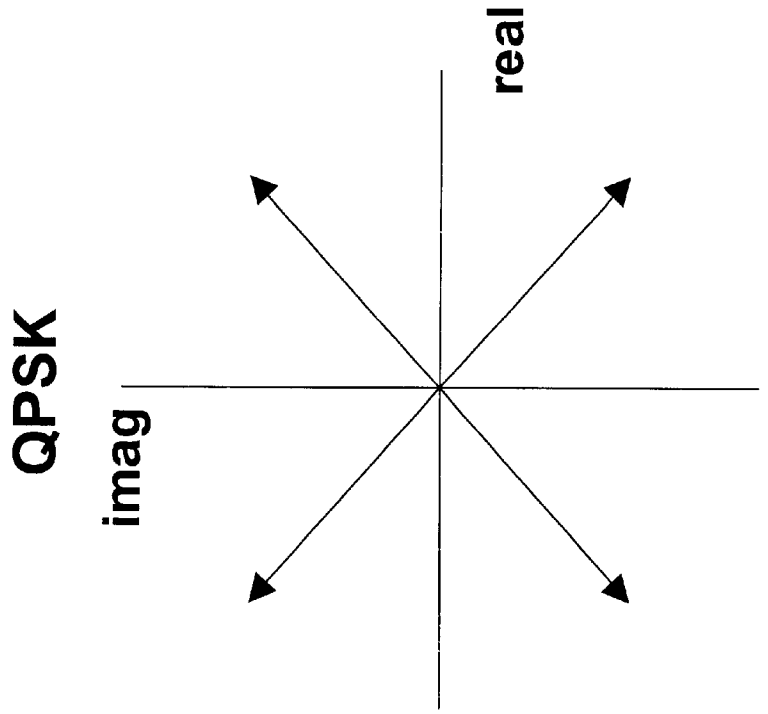


FIG. 22B

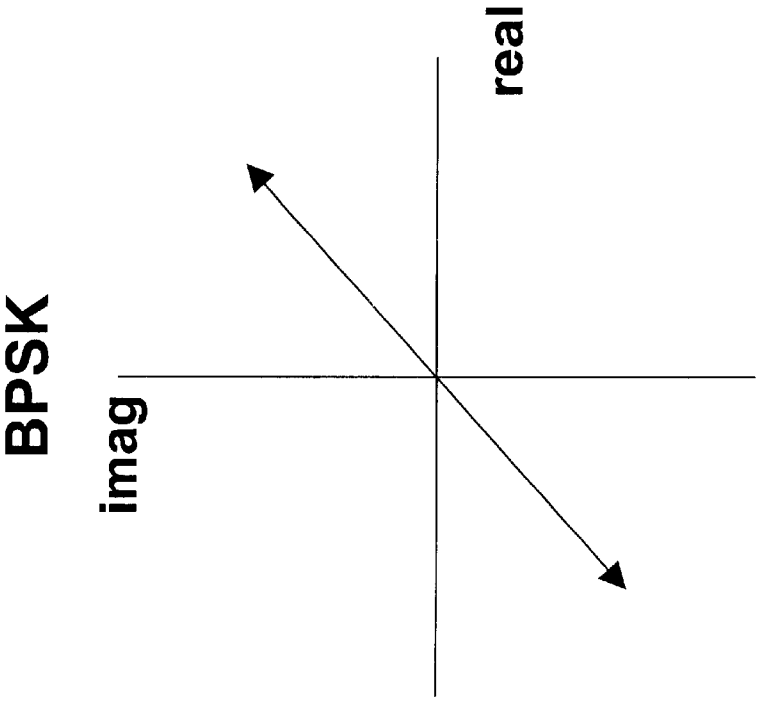


FIG. 22A

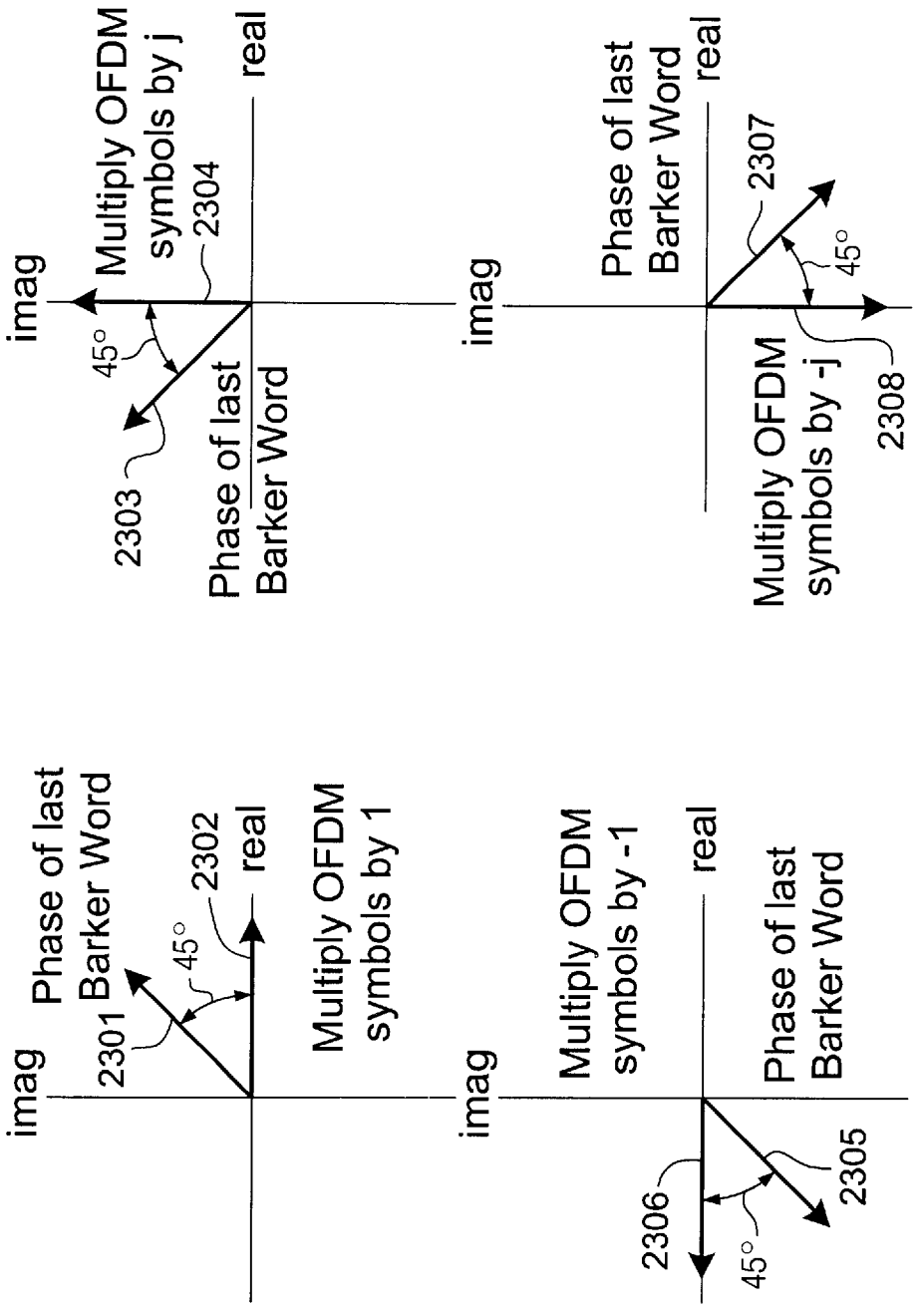

imag
real
Multiply OFDM symbols by j
2304
45°
2303
Phase of last Barker Word
imag
real
Phase of last Barker Word
2307
45°
Multiply OFDM symbols by -j
2308
imag
real
Phase of last Barker Word
2301
45°
2302
Multiply OFDM symbols by 1
imag
real
Multiply OFDM symbols by -1
Phase of last Barker Word
2306
45°
2305

FIG. 23

WIRELESS COMMUNICATION SYSTEM CONFIGURED TO COMMUNICATE USING A MIXED WAVEFORM CONFIGURATION

CROSS-REFERENCE TO RELATED APPLICATION(S)

The present application is based on U.S. Provisional Patent Application entitled "Wireless Communication System Configured to Communicate Using a Mixed Waveform Configuration", Serial No. 60/306,438, filed Jul. 6, 2001, which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to wireless communications, and more particularly to a wireless communication system configured to communicate using a single-carrier to multi-carrier mixed waveform configuration.

BACKGROUND OF THE INVENTION

The Institute of Electrical and Electronics Engineers, Inc. (IEEE) 802.11 standard is a family of standards for wireless local area networks (WLAN) in the unlicensed 2.4 and 5 Gigahertz (GHz) bands. The current 802.11 b standard defines various data rates in the 2.4 GHz band, including data rates of 1, 2, 5.5 and 11 Megabits per second (Mbps). The 802.11b standard uses direct sequence spread spectrum (DSSS) with a chip rate of 11 Megahertz (MHz), which is a serial modulation technique. The 802.11a standard defines different and higher data rates of 6, 12, 18, 24, 36 and 54 Mbps in the 5 GHz band. It is noted that systems implemented according to the 802.11 a and 802.11b standards are incompatible and will not work together.

A new standard is being proposed, referred to as 802.11 g (the "802.11 g proposal"), which is a high data rate extension of the 802.11b standard at 2.4 GHz. It is noted that, at the present time, the 802.11 g proposal is only a proposal and is not yet a completely defined standard. Several significant technical challenges are presented for the new 802.11 g proposal. It is desired that the 802.11 g devices be able to communicate at data rates higher than the standard 802.11b rates in the 2.4 GHz band. In some configurations, it is desired that the 802.11b and 802.11 g devices be able to coexist in the same WLAN environment or area without significant interference or interruption from each other, regardless of whether the 802.11b and 802.1 g devices are able to communicate with each other. It may further be desired that the 802.11 g and 802.11b devices be able to communicate with each other, such as at any of the standard 802.11b rates.

A dual packet configuration for wireless communications has been previously disclosed in U.S. patent application entitled, "A Dual Packet Configuration for Wireless Communications", Ser. No. 09/586,571 filed on Jun. 2, 2000, which is hereby incorporated by reference in its entirety. This previous system allowed a single-carrier portion and an orthogonal frequency division multiplexing (OFDM) portion to be loosely coupled. Loosely coupled meant that strict control of the transition was not made to make implementations simple by allowing both an existing single-carrier modem and an OFDM modem together with a simple switch between them with a minor conveyance of information between them (e.g., data rate and packet length). In particular, it was not necessary to maintain strict phase, frequency, timing, spectrum (frequency response) and power continuity at the point of transition (although the power step would be reasonably bounded). Consequently, the OFDM system needed to perform an acquisition of its own, separate from the single-carrier acquisition, including re-acquisition of phase, frequency, timing, spectrum (including multi-path) and power (Automatic Gain Control [AGC]). A short OFDM preamble following the single carrier was used in one embodiment to provide reacquisition.

An impairment to wireless communications, including WLANs, is multi-path distortion where multiple echoes (reflections) of a signal arrive at the receiver. Both the single-carrier systems and OFDM systems must include equalizers that are designed to combat this distortion. The single-carrier system designs the equalizer on its preamble and header. In the dual packet configuration, this equalizer information was not reused by the OFDM receiver. Thus, the OFDM portion employed a preamble or header so that the OFDM receiver could reacquire the signal. In particular, the OFDM receiver had to reacquire the power (AGC), carrier frequency, carrier phase, equalizer and timing parameters of the signal.

Interference is a serious problem with WLANs. Many different signal types are starting to proliferate. Systems implemented according to the Bluetooth standard present a major source of interference for 802.11-based systems. The Bluetooth standard defines a low-cost, short-range, frequency-hopping WLAN. Preambles are important for good receiver acquisition. Hence, losing all information when transitioning from single-carrier to multi-carrier is not desirable in the presence of interference.

There are several potential problems with the signal transition, particularly with legacy equipment. The transmitter may experience analog transients (e.g., power, phase, filter delta), power amplifier back-off (e.g. power delta) and power amplifier power feedback change. The receiver may experience AGC perturbation due to power change, AGC perturbation due to spectral change, AGC perturbation due to multi-path effects, loss of channel impulse response (CIR) (multi-path) estimate, loss of carrier phase, loss of carrier frequency, and loss of timing alignment.

SUMMARY OF THE INVENTION

A wireless communication system configured to communicate using a mixed waveform configuration is disclosed and includes a transmitter configured to transmit according to a mixed waveform configuration and a receiver configured to acquire and receive packets with a mixed waveform configuration. The mixed waveform includes a first portion modulated according to a single-carrier scheme with a preamble and header and a second portion modulated according to a multi-carrier scheme. The waveform is specified so that a channel impulse response (CIR) estimate obtainable from the first portion is reusable for acquisition of the second portion.

In one configuration, the transmitter maintains power, carrier phase, carrier frequency, timing, and multi-path spectrum between the first and second portions of the waveform. The transmitter may include first and second kernels and a switch. The first kernel modulates the first portion according to the single-carrier modulation scheme and the second kernel generates the second portion according to the multi-carrier modulation scheme. The switch selects the first kernel for the first portion and the second kernel for the second portion to develop a transmit waveform. In one embodiment, the first kernel operates at a first sample rate and the second kernel operates at a second sample rate. The

first kernel may employ a single-carrier spectrum that resembles a multi-carrier spectrum of the multi-carrier modulation scheme.

The first kernel may employ a time shaping pulse that is specified in continuous time. The time shaping pulse may be derived by employing an infinite impulse response of a brick wall approximation that is truncated using a continuous-time window that is sufficiently long to achieve desired spectral characteristics and sufficiently short to minimize complexity. The first kernel may sample the time shaping pulse according to a Nyquist criterion. The average output signal power of the first kernel and the average output signal power of the second kernel may be maintained substantially equal. The first kernel may employ a first sample rate clock while the second kernel employs a second sample rate clock. In this latter case, the first and second sample rate clocks are aligned at predetermined timing intervals. Also, a first full sample of the multi-carrier modulation scheme begins one timing interval after the beginning of a last sample of the single-carrier modulation scheme.

The single-carrier signal from the first kernel may be terminated according to a windowing function specified for OFDM signal shaping defined in the 802.11a standard. The carrier frequency may be coherent between the first and second kernels. The carrier phase may be coherent between the first and second kernels. In one embodiment to achieve coherent phase, carrier phase of the second kernel multi-carrier signal is determined by carrier phase of a last portion of the second kernel single-carrier signal. The carrier phase of the second kernel multi-carrier signal may further be rotated by a corresponding one of a plurality of rotation multiples, each rotation multiple corresponding to one of a plurality of predetermined phases of the last portion of the second kernel single-carrier signal. In a particular embodiment, the first kernel single-carrier modulation scheme is according to 802.11b Barkers in which each Barker word is one of first, second, third and fourth possible phases and the second kernel multi-carrier modulation scheme is according to OFDM as defined in Annex G of the 802.11a standard. In this case, the OFDM symbols are rotated by the second kernel by zero if the last Barker word has the first phase, by 90 degrees if the last Barker word has the second phase, by 180 degrees if the last Barker word has the third phase, and by −90 degrees if the last Barker word has the fourth phase.

The requisite fidelity of the entire mixed waveform configuration may be specified by a requisite fidelity specified for the multi-carrier scheme. In one embodiment, the requisite fidelity is a function of data rate of the second portion and is determined by mean-squared-error normalized by signal power as specified for OFDM in the 802.11a standard.

The symbol rate clock and carrier frequency of the waveform may be derived from the same reference clock. The part per million (PPM) error of a clock fundamental for symbol rate and PPM error of a clock fundamental for carrier frequency may be substantially equal.

The receiver may include a single-carrier receiver, a multi-carrier receiver, and a switch that provides a first portion of a signal being received to the single-carrier receiver and that provides a second portion of the signal being received to the multi-carrier receiver. The single-carrier receiver acquires a first portion of an incoming signal including the preamble and header and determines a CIR estimate, and the multi-carrier receiver uses the CIR estimate for a second portion of the incoming signal. In a specific configuration, the single-carrier receiver programs taps of the first equalizer based on the CIR estimate, the multi-carrier receiver includes a second equalizer, and the multi-carrier receiver modifies taps of the second equalizer based on the CIR estimate determined by the first equalizer.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. **1** is a block diagram of a WLAN system including four devices operating within the same room or area, where two of the devices are implemented according to the 802.11b standard and the other two are implemented according to the 802.11 g proposal.

FIG. **2** is a block diagram of a mixed signal receiver implemented according to an embodiment of the present invention that may be used in either or both of the high rate devices of FIG. **1**.

FIG. **3** is a conceptual diagram of a mixed signal packet implemented according to an embodiment of the present invention.

FIGS. **4**A and **4**B are graph diagrams of plots of the spectrum of the 802.11b Barker chips and the 802.11a OFDM, respectively.

FIGS. **5**A and **5**B are graph diagrams of time domain plots of the 802.11b QPSK Barker chips and the 802.11a OFDM, respectively, illustrating that the waveforms are radically different.

FIG. **6**A is a graph diagram of a plot of the power spectral density (PSD) of a single sub-carrier out of the possible 64 possible sub-carriers defined in the 802.11a standard.

FIG. **6**B is a graph diagram of a plot of the composite PSD of the 52 non-zero sub-carriers used in 802.11a.

FIG. **7**A is a graph diagram of a plot of an exemplary "brickwall" double-sided spectrum centered at 0 MHz.

FIG. **7**B is a graph diagram of a portion of the associated infinite-duration time response corresponding to the brickwall spectrum of FIG. **7**A.

FIG. **8** is a graph diagram of a plot of an exemplary continuous-time window, which is a continuous time version of a Hanning window.

FIG. **9** is a graph diagram of a plot of the Hanning window of FIG. **8** overlayed with the portion of the infinite-duration time response corresponding to the brickwall spectrum of FIG. **7**A.

FIG. **10** is a graph diagram of a plot of the exemplary pulse p(t) resulting from the overlaying illustrated in FIG. **9** and truncated to approximately 0.8 μs.

FIG. **11** is a graph diagram of a plot of the spectral characteristics of the pulse p(t) illustrating that it is a close match to the OFDM spectrum.

FIG. **12** is a block diagram of an exemplary digital filter employed to architect a digital 22 MHz output sample rate using the continuous time pulse p(t).

FIG. **13** is a graph diagram illustrating the sampling and polyphase decomposition of the continuous time pulse p(t) using the sampling scheme of FIG. **12**.

FIG. **14** is a block diagram of another exemplary digital filter employed to architect a digital 20 MHz output sample rate using the pulse p(t).

FIG. **15** is a graph diagram illustrating the sampling and polyphase decomposition of the continuous time pulse p(t) using the sampling scheme of FIG. **14**.

FIG. **16** is a block diagram of a transmitter implemented according to an embodiment of the present invention.

FIG. **17** is a graph diagram comparing the 11 MHz Barker chip clock versus the 20 MHz OFDM sample clock.

FIG. **18** is a conceptual graph diagram illustrating alignment of the OFDM signal portion with the last Barker word of the header of the single-carrier portion.

FIG. **19** is a graph diagram illustrating normal OFDM symbol overlap.

FIG. **20** is a graph diagram illustrating exemplary 802.11a OFDM symbol onset and termination.

FIG. **21** is a graph diagram illustrating exemplary single-carrier termination, shaped consistent with 802.11a, and OFDM onset shaped identical to 802.11 a.

FIG. **22**A is a simplified graph diagram of a BPSK plot illustrating that BPSK incorporates both real and imaginary portions in two quadrants (1 of 2 phases).

FIG. **22**B is a simplified graph diagram of a QPSK plot illustrating that QPSK incorporates both real and imaginary portions in all four quadrants (1 of 4 phases).

FIG. **23** is a graph diagram of a plot illustrating the phase of the last Barker word in the 802.11 g header and the relative phase of the OFDM symbol in accordance with that described in Annex G of the 802.11a standard.

DETAILED DESCRIPTION OF EMBODIMENT (S) OF THE INVENTION

A configuration according to the present invention reuses the equalizer information obtained during acquisition of the single-carrier portion of the signal. In this manner, no OFDM preamble is required, although it still may be present for both convenience and fine tuning. The present disclosure describes a technique for providing complete continuity between the single-carrier and OFDM (multi-carrier) segments. This continuity is provided by specifying the transmit waveform completely for both the single-carrier and OFDM segments and specifying the transition. This enables complete continuity between the two signal segments, including AGC (power), carrier phase, carrier frequency, timing and spectrum (multi-path). In this manner, the signal does not have to be reacquired by the multi-path portion of the receiver since the information developed during the single-carrier portion (preamble/header) is valid and used to initiate capture of the multi-carrier portion. Maintaining and accumulating information makes the signal much more robust in the face of common interferences experience in wireless communications.

FIG. **1** is a block diagram of a wireless local area network (WLAN) system **100** operating within a particular room or area **101**, including four WLAN devices **103**, **105**, **107** and **109** (**103**–**109**) are located within the area **101**. The devices **103** and **105** are implemented according to at least one of several embodiments of the present invention with the 802.11 g proposal in mind, whereas the devices **107** and **109** are implemented according to the 802.11b standard. All of the devices **103**–**109** operate in the 2.4 GHz band. The devices **103**–**109** may be any type of wireless communication device, such as any type of computer (desktop, portable, laptop, etc.), any type of compatible telecommunication device, any type of personal digital assistant (PDA), or any other type of network device, such as printers, fax machines, scanners, hubs, switches, routers, etc. It is noted that the present invention is not limited to the 802.11 g proposal, the 802.11b standard, the 802.11a standard or the 2.4 GHz frequency band, although these standards and frequencies may be utilized in certain embodiments.

The devices **107** and **109** communicate with each other at any of the standard 802.11b rates, including 1, 2, 5.5 and 11 Mbps. The devices **103** and **105** are mixed signal mode devices that communicate with each other at different or higher data rates using a mixed signal configuration according to any one of several embodiments, such as the standard 802.11a data rates of 6, 9, 12, 18, 24, 36, 48 or 54 Mbps. Alternative data rate groups are considered herein. The second group is advantageous as including two of the 802.11b standard data rates, namely 5.5 and 11 Mbps.

In one or more first embodiments, the mixed signal devices **103**–**109**may operate or coexist in the same area **101** without significant interference from each other, where the devices **103**, **105** communicate with each other at different or higher data rates than the 802.11b devices **107**, **109**. In the first embodiments, the devices **103**, **105** may communicate with each other while the devices **107**, **109** may communicate with each other, but the devices **103**, **105** do not communicate with the devices **107**, **109**. In one or more second embodiments, at least one of the mixed signal devices **103**, **105** is configured with a standard mode to be able to communicate with either of the devices **107**, **109** at any one or more of the standard 802.11b data rates. In at least one third embodiment, the mixed signal devices **103**, **105** communicate at different or higher data rates and are incompatible with the devices **107** and **109**, so that the devices **103**–**109** are not able to coexist within the same area **101**. The mixed signal devices **103**, **105** may be implemented to operate in the 2.4 GHz band, although other frequency bands are contemplated.

In the first or second embodiments, it is desired that the devices **103** and **105** be able to communicate with each other without interruption or interference from either of the devices **107** and **109**. This presents a significant technical challenge since the devices **103**, **105** operate at different data rates when communicating with each other. The present invention solves this problem by enabling the devices **103** and **105** to be implemented to be able to communicate with each other at different or at higher data rates while residing in a same area **101** as the 802.11b devices **107**, **109**. Further, in the second embodiments the devices **103**, **105** may also communicate with either of the devices **107**, **109** at the 802.11b data rates.

FIG. **2** is a block diagram of a mixed signal receiver **201** implemented according to an embodiment of the present invention that may be used in either or both of the devices **103**, **105**. The incoming signal is received by an automatic gain control (AGC) **203** that adjusts receive power and provides a corresponding signal to a switch **205**. The switch **205** initially provides the received signal to a single-carrier receiver **207**. The single-carrier receiver **207** includes an equalizer and other circuitry that analyzes the predetermined preamble of the received signal compared to known data and "learns" the parameters associated with the multi-path medium through which the signal was propagated. The single-carrier receiver **207** also examines the header to determine if the packet is intended for the mixed signal receiver **201** and if the packet is a mixed packet, and if so, causes the switch **205** to provide the remaining portion of the incoming signal to a multi-carrier receiver **209**. It is noted that the header includes a mixed mode identifier (not shown), such as a mode bit or the like, that identifies the packet as a mixed mode packet. Thus, in one embodiment, the single-carrier receiver **207** determines that the packet is intended for the mixed signal receiver **201** from a destination address or the like, and determines that the packet is a mixed mode packet from the mode identifier. If the packet

is intended for the mixed signal receiver **201** but is not a mixed mode packet (e.g., a standard 802.11b packet), then the single-carrier receiver **207** continues to process the packet. A length field is also provided in the header which includes a length value that identifies the total length of the mixed mode packet. Thus, any device, including mixed mode or legacy devices (e.g. 802.11b devices), may determine that the packet is not intended for it, and backs-off by an amount of time corresponding to the length value.

The multi-carrier receiver **209** is configured to receive the signal, which is transmitted according to OFDM or the like. The multi-carrier receiver **209** is coupled to the single-carrier receiver **207** so that the multi-path information determined by the single-carrier receiver **207** is re-used to enable a smooth transition between the packet portions of the incoming signal. In particular, the AGC (power), carrier frequency, carrier phase, equalizer, and timing parameters from the single-carrier receiver **207** are used by the multi-carrier receiver **209** to receive the incoming signal. The OFDM multi-carrier receiver **209** need not re-acquire the signal, since the information used by the single-carrier receiver **207** is obtained and used.

FIG. **3** is a conceptual diagram of a mixed signal packet **301** implemented according to an embodiment of the present invention. The packet **301** includes a Barker Preamble **303**, which is transmitted at 1 megabits per second (Mbps), followed by a Barker Header **305**, which is transmitted at 1 or 2 Mbps, followed by one or more OFDM symbols **307** incorporating payload data, which is transmitted at any selected data rate from among typical data rates of 6, 9, 12, 18, 24, 36, 48 or 54 Mbps with a selected sample rate of 20 megahertz (MHz). The preamble **303** and header **305** are transmitted with a single carrier at the 11 MHz Quadrature Phase Shift Keying (QPSK) symbol rate (and Binary Phase Shift Keying [BPSK] is also contemplated). Different OFDM sample rates are contemplated, such as 18.333 megahertz (MHz), 22 MHz, etc., in which the same principles apply. The transmit signal is specified for complementary code keying OFDM, or CCK-OFDM (802.11b preamble and header using Barkers [single carrier] followed by OFDM [multi-carrier]). The OFDM portion of the waveform can optionally be one of several effective sample rates (e.g., 22, 20, or 18.33 MHz). The packet **301** is shown employing the 802.11a sample rate of 20 MHz. The goal is to specify the signal so that the channel impulse response (CIR) estimate obtained on the preamble and header is reusable on the OFDM. Hence, the transition is completely specified, with no free variables, which allows important equalizer information to be retained at switch-over. Also, it is desirable to eliminate receiver power changes due to the signal transition. A power step may cause legacy equipment to enter an undefined state, since they do not have knowledge of the OFDM, nor the capability to receive it.

FIGS. **4**A and **4**B are graph diagrams of plots of the spectrum of the 802.11b Barker chips and the 802.11a OFDM, respectively, in decibels (dB) versus normalized frequency (freq). Spectrum refers to center frequency, power spectral density, and frequency response. The 802.11b Barker chip spectrum has a round "top" whereas the 802.11a OFDM spectrum has a flat top. The 3 dB bandwidths are also different. FIGS. **5**A and **5**B are graph diagrams of time domain plots of the 802.11b QPSK Barker chips and the 802.11a OFDM, respectively, illustrating that the waveforms are radically different. It is desired to create a smooth transition between the preamble/header single-carrier portion **303**, **305** and the OFDM symbol portion **307** even though the waveforms are different. One solution is to make the 802.11b Barker preamble and header look like OFDM with approximately the same transmit spectrum and approximately the same power.

FIG. **6**A is a graph diagram of a plot of the power spectral density (PSD) of a single sub-carrier out of the possible 64 possible sub-carriers defined in the 802.11a standard, in dB versus frequency. FIG. **6**B is a graph diagram of a plot of the composite PSD of the 52 non-zero sub-carriers used in 802.11a. The curves are plotted versus normalized frequency (nfreq) and frequency in MHz, respectively. It is desired to design a spectrum/time shaping pulse, which makes the spectrum of the single-carrier portion of the signal resemble OFDM. This pulse is made known so that the receiver is able to compensate the CIR for the OFDM portion of the packet. The pulse is specified in continuous time, so that it is implementation independent. For digital implementations, the pulse may be sampled at any desired appropriate implementation rate. The signal should provide a nearly flat spectrum in the pass-band with sufficiently steep roll-off on the band edges. It is desired that the transmit pulse be easily handled by 802.11b legacy receivers. It should have a dominant peak, therefore, with a small amount of spread in the impulse response. This allows the 802.11b receiver to lock on to this impulse response component. It is desired that the signal have a short duration to minimize complexity.

FIG. **7**A is a graph diagram of a plot of an exemplary "brickwall" double-sided spectrum centered at 0 MHz, having a magnitude of 1 at a selected bandwidth of approximately 2(8.5)=17 MHz and 0 otherwise. A brickwall spectrum is essentially an idealized low-pass filter. The exemplary frequency range is selected as (2)(27)(20 MHz/64)=16.875 MHz in the embodiment shown. FIG. **7**B is a graph diagram of a portion of the associated infinite-duration time response corresponding to the brickwall spectrum. In general, a target spectrum is chosen for the single carrier system. This is done by specifying a brickwall approximation to the desired spectrum. A brickwall spectrum has an infinite impulse response in the time domain (i.e., spans from +/−infinity). The pulse is then truncated using a continuous-time window. A long enough window is chosen to give the desired spectral characteristics while a short enough window is chosen to minimize complexity, each generally employing engineering judgment.

FIG. **8** is a graph diagram of a plot of an exemplary continuous-time window, which is a continuous time version of a Hanning window. It is appreciated that this is only one of many different window configurations that may be successfully employed to achieve desirable results. FIG. **9** is a graph diagram of a plot of the Hanning window overlayed with the portion of the infinite-duration time response corresponding to the brickwall spectrum. FIG. **10** is a graph diagram of a plot of the resulting exemplary pulse p(t) truncated to approximately 0.8 μs so that it is zero outside +/−0.4 μs. The short duration of the pulse p(t) provides low complexity. FIG. **11** is a graph diagram of a plot of the spectral characteristics of the pulse p(t) illustrating that it is a close match to the OFDM spectrum. The spectral characteristics of the pulse p(t) include a nearly flat spectrum where OFDM is flat and a fast roll-off where OFDM rolls off. The continuous time pulse can be used to construct any digital filter unambiguously and is independent of particular implementations. The Nyquist criteria (sampling of the continuous time pulse) should be satisfied at the level of the target fidelity. The pulse p(t) is "digitized" or sampled according to the Nyquist criterion. In some embodiments, the samples are then decomposed as described further below.

FIG. **12** is a block diagram of an exemplary digital filter **1201** employed to architect a digital 22 MHz output sample

rate using the continuous time pulse p(t). In this case, an exemplary QPSK symbol generator **1203** provides an 11 MHz signal to respective inputs of each of a pair of polyphase digital filters **1205** and **1207**. The QPSK symbol generator **1203**, used as an exemplary transmitter for illustration, passes each symbol (a complex number) to both of the digital filters **1205** and **1207** at a rate of 11 MHz each. Each digital filter **1205** and **1207** samples the input waveform and generates an output at 11 MHz. The digital filter taps **1205** are composed of even numbered samples and the digital filter taps **1207** are composed of odd numbered samples of the pulse p(t). Select logic **1209**, such as multiplexor (MUX) circuitry or the like, selects every output of the polyphase digital filter taps **1205** and **1207** to achieve a 2(11)=22 MHz sample rate signal. FIG. **13** is a graph diagram illustrating the sampling and polyphase decomposition of the continuous time pulse p(t) (plotted versus time in microseconds, "μs"). Since every output of every filter is used, the effective sampling rate is 22 MHz.

FIG. **14** is a block diagram of another exemplary digital filter **1401** employed to architect a digital 20 MHz output sample rate using the pulse p(t). In this case, an exemplary QPSK symbol generator **1403**, similar to the generator **1203**, provides an 11 MHz signal to respective inputs of twenty polyphase digital filters **1405**, **1407**, **1409**, . . . **1411**. Each digital filter **1405–1411** generates an output at 11 MHz, so that the sampling rate is increased from 11 MHz to 220 MHz. Each filter consists of the samples spaced 20 samples apart. Select logic **1413**, such as multiplexor (MUX) circuitry or the like, selects one of every 11 outputs of the polyphase digital filters **1405–1411** to achieve a 20 MHz sample signal. For example, for the first QPSK symbol, the respective outputs of filters **1** and **11** are used and for the second QPSK symbol, the respective outputs of filters **19** and **10** are used, etc. Also, one out of every eleven input symbols will generate **1** output sample, whereas the remaining input samples each generate two output samples. FIG. **15** is a graph diagram illustrating the sampling and polyphase decomposition of the continuous time pulse p(t) plotted versus time. Since one out of every 11 outputs is used of the 220 MHz combined output of the filters **1405–1411**, the effective sampling rate is 20 MHz.

FIG. **16** is a block diagram of a transmitter **1601** implemented according to an embodiment of the present invention. The transmitter **1601** includes an OFDM Kernel block **1603** supplying the OFDM portion of the signal to a soft switch block **1607**, which receives the 802.11b preamble and header portion from an 802.11b preamble/header Kernel block **1605**. The soft switch block **1607** provides the 802.11 g signal to a digital to analog converter (DAC) **1609**, which provides a resulting analog signal to a low-pass filter (LPF) **1611**. The filtered signal is provided to a SAW filter **1613**, illustrating that linear distortions are induced on both signal segments. The output of the SAW filter **1613** is provided to one input of a mixer **1615**, having another input which receives a local oscillator (LO) signal from a local oscillator **1617**. The mixer **1615** asserts a mixed or combined signal at its output.

Distortions can be induced in the transmitter, multi-path channel and receiver. An obvious linear distortion in the transmitter is a SAW filter, such as the SAW filter **1613**. In communications systems, it is frequently assumed that linear distortions are common and (essentially) time-invariant across waveform symbols. For example, linear distortions are assumed common between the preamble/header and payload portions for both 802.11a and 802.11b communications. In a similar manner, linear distortions of the transmit radio are assumed to be common to both the single-carrier segment and the multi-carrier segment. In this manner, a spectral binding requirement is imposed to allow the equalizer information and the AGC to carry over from single- to multi-carrier.

The transmitter **1601** further illustrates a sample-power matching scheme to enable the AGC information to carry over from single-carrier to multi-carrier portions of the signal. In particular, it is desired that the average signal power output from the OFDM Kernel block **1603**, as shown at **1620**, be approximately the same as the average signal power output from the 802.11b preamble/header Kernel block **1605**, as shown at **1622**.

FIG. **17** is a graph diagram comparing the 11 MHz Barker chip clock shown at **1701** versus the 20 MHz OFDM sample clock shown at **1703**, both plotted versus time in μs. The 802.11b communication scheme uses a chip rate of 11 MHz. The 802.11b preamble/header uses 11 chip Barker words, so that there are 11 chips/μs. The 802.11a OFDM uses a 20 MHz sample rate. In the embodiment shown, in order to achieve transition time alignment, the 802.11b (11 MHz) and 802.11a (20 MHz) signal segments are aligned at the 1 MHz boundary, every 1 μs interval, illustrated by alignment epochs **1705** at each 1 μs interval. FIG. **18** is a conceptual graph diagram illustrating alignment of the OFDM signal portion with the last Barker word of the header of the single-carrier portion. The first chip of each Barker word, shown at **1803**, is centered on the 1 μs alignment. The first full 20 MHz sample of the OFDM signal, shown at **1801**, occurs 1 μs after the zero-phase peak of first chip of the last Barker word in the header. Effectively, one half-scale OFDM sample, shown at **1805**, occurs before the full scale sample (for smoothing). Such transition time alignment allows the equalizer information and the timing information to carry over between the single- and multi-phase portions of the signal.

FIG. **19** is a graph diagram illustrating normal OFDM symbol overlap. FIG. **20** is a graph diagram illustrating exemplary 802.11a OFDM symbol onset and termination. FIG. **21** is a graph diagram illustrating exemplary single-carrier termination, shaped consistent with 802.11a as shown at **2101**, and OFDM onset shaped identical to 802.11a, as shown at **2103**. As illustrated in these graph diagrams, the single-carrier is terminated in a controlled fashion when transitioning from single-carrier to multi-carrier. This single-carrier termination maintains the AGC at the point of transition, minimizes the signal power gap, which in turn minimizes the corruption of one signal by the other. The single-carrier termination of the 802.11b segment is similar to that used for 802.11a OFDM shaping. 802.11a specifies a windowing function for OFDM symbols, which is employed to define termination of single-carrier segment. The single-carrier signal is terminated in a predetermined window of time, such as nominally 100 nanoseconds (ns). It is not necessary to completely flush the single-carrier pulse-shaping filter. The resulting distortion to the last Barker word in the header is trivial compared to the 11 chips processing gain, thermal noise and multi-path distortion. The termination may be accomplished either explicitly in the digital signal processing or by analog filtering.

It is further desired that the carrier frequency be coherent for both waveform segments, achieved by using a single LO signal via the local oscillator **1617**. This allows the equalizer information to carry over. Carrier frequency lock may be maintained with a phase-lock loop (PLL) circuit or the like.

It is further desired that the carrier phase be aligned, which allows the equalizer information to carry over. FIG.

22A is a simplified graph diagram of a BPSK plot illustrating that BPSK incorporates both real and imaginary portions in two quadrants (1 of 2 phases). FIG. **22**B is a simplified graph diagram of a QPSK plot illustrating that QPSK incorporates both real and imaginary portions in all four quadrants (1 of 4 phases). The single-carrier signals, employing Direct Sequence Spread Spectrum (DSSS), are fundamentally different as compared to the OFDM signal format and modulation schemes. For 802.11 g CCK-ODFM, either of these formats are re-used for the header.

FIG. **23** is a series of graph diagrams illustrating the phase relationship between the last Barker word, rather than the last chip, in the 802.11 g header and subsequent OFDM symbol samples. Annex G of the 802.11a standard describes how to transmit an OFDM symbol including real and imaginary components. The arrows shown at **2301**, **2303**, **2305** and **2307** illustrate the four possible phases of the last Barker word. The phase of the OFDM symbol is determined by the phase of the last Barker word, in that each OFDM sample is either not rotated or rotated by the same, predetermined amount based on the phase of the last Barker word. The arrows shown at **2302**, **2304**, **2306** and **2308** represent the corresponding four relative phase shifts applied to the OFDM symbol corresponding to the Barker phase illustrated by arrows **2301**, **2303**, **2305** and **2307**, respectively. For example, if the phase of the last Barker word is in the first quadrant, then the phase of the OFDM symbols will be rotated by zero degrees (not rotated, or multiplied by 1) relative to the OFDM phase as described in Annex G of the 802.11a standard. Furthermore, if the phase of the last Barker word is in the second quadrant (135 degree phase rotation), then the phase of the OFDM symbols will be rotated by 90 degrees relative to the phase of the samples in 802.11a Annex G (i.e., multiplied by "j"); if the phase of the last Barker word is in the third quadrant (−135 degree phase rotation), then the phase of the OFDM symbols will be rotated by 180 degrees relative to the phase of the samples in 802.11a Annex G (i.e., multiplied by "−1"); and if the phase of the last Barker word is in the fourth quadrant (−45 degree phase rotation), then the phase of the OFDM symbols will be rotated by −90 degrees relative to the phase of the samples in 802.11a Annex G (i.e., multiplied by "−j").

In many design implementations, it is often desired to know the relative accuracy and fidelity requirements to maintain signal integrity and compatibility among different transceivers. In this manner, designers are able to reduce costs and maximize efficiency while maintaining parameters and characteristics within specification. The accuracy characteristic constrains the short-cuts the transmit designer may make which may otherwise significantly harm receiver performance. In one embodiment, the requisite fidelity of the entire waveform behavior is established using a metric based on the fidelity requirements of the OFDM signal of the 802.11a standard. Thus, the requisite fidelity of the single-carrier portion is the same as the multi-carrier portion even though the single-carrier portion is typically at a reduced data rate. As described in the 802.11a specification, the requisite fidelity for OFDM is set by the error vector magnitude (EVM) specification, as illustrated in the following Data Rate versus EVM Table 1:

TABLE 1

Data Rate versus EVM specification

Data Rate Mbps	EVM Spec
6	−5
9	−8
12	−10
18	−13
24	−16
36	−19
48	−22
54	−25

where data rate is specified in Mbps and EVM is specified in dB. As illustrated in Table 1, the OFDM accuracy is a function of the data rate. The higher the data rate, the more complex and intricate the transmit waveform, and the greater the accuracy necessary. This requisite fidelity is applied to the entire waveform. EVM is the same thing as mean-squared-error (MSE) normalize by the signal power. MSE may be measured after best-fit time alignment, best-fit gain alignment, and best-fit phase alignment. Also, linear distortion common to OFDM and the single-carrier Barker chips may be backed-out, if desired. If and when the 802.11b accuracy specification becomes more stringent, it may be used for the single-carrier portion.

Portions of 802.11b specification and all of the 802.11a specification employ a locked-oscillator requirement. A locked oscillator characteristic allows timing tracking information to be derived from carrier frequency and phase. There are two fundamental clocks in a transmit waveform: a symbol rate clock and a carrier frequency. In at least one embodiment of the transmitter, all of the 802.11 g signals have a symbol rate clock and carrier frequency derived from the same clock reference. It is further desired that the part-per-million (PPM) error on these two clock signals be equal. The receiver is allowed to track symbol rate timing from carrier frequency error.

The multi-carrier receiver **209** portion of the mixed signal receiver **201** obtains the behavior of the transition from the single-carrier receiver **207** of the waveform as described herein to receive the ODFM portion of the signal. The carrier frequency and phase is coherent. Furthermore, the time alignment, the signal level (AGC), and the channel impulse response (CIR) are each coherent. The single-carrier receiver **207** determines the CIR estimate during the single-carrier portion. The multi-carrier receiver **209** modifies the CIR estimate for the OFDM using the known pulse shape used by the single-carrier segment. In particular, the equalizer taps of the multi-carrier receiver **209** are modified using the known pulse shape used by the transmitter during the single-carrier preamble and header. In this manner, the multi-carrier receiver **209** does not have to reacquire the OFDM portion of the signal, but uses the information obtained by the single-carrier receiver **207** along with predetermined or known information for a smooth single-carrier to multi-carrier signal transition. Also, a separate OFDM preamble/header is not necessary, although it may be employed for both convenience and fine tuning, if desired.

Although a system and method according to the present invention has been described in connection with the preferred embodiment, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention.

What is claimed is:

1. A wireless communication system that is configured to communicate using a mixed waveform configuration, comprising:

a transmitter configured to transmit according to a mixed waveform configuration including a first portion modulated according to a single-carrier scheme with a preamble and header and a second portion modulated according to a multi-carrier scheme;

the waveform being specified so that a channel impulse response estimate obtainable from the first portion is reusable for acquisition of the second portion; and

a receiver configured to acquire and receive packets with a mixed waveform configuration.

2. The wireless communication system of claim 1, wherein the transmitter maintains power, carrier phase, carrier frequency, timing, and multi-path spectrum between the first and second portions of the waveform.

3. The wireless communication system of claim 2, wherein the transmitter comprises:

a first kernel that modulates the first portion according to the single-carrier modulation scheme;

a second kernel that generates the second portion according to the multi-carrier modulation scheme; and

a switch, coupled to the first and second kernels, that selects the first kernel for the first portion and the second kernel for the second portion to develop a transmit waveform.

4. The wireless communication system of claim 3, wherein the first kernel operates at a first sample rate and wherein the second kernel operates at a second sample rate.

5. The wireless communication system of claim 3, wherein the first kernel employs a single-carrier spectrum that resembles a multi-carrier spectrum of the multi-carrier modulation scheme.

6. The wireless communication system of claim 5, wherein the first kernel employs a time shaping pulse that is specified in continuous time.

7. The wireless communication system of claim 6, wherein the time shaping pulse is derived employing an infinite impulse response of a brick wall approximation that is truncated using a continuous-time window that is sufficiently long to achieve desired spectral characteristics and sufficiently short to minimize complexity.

8. The wireless communication system of claim 6, wherein the first kernel samples the time shaping pulse according to a Nyquist criterion.

9. The wireless communication system of claim 3, wherein the average output signal power of the first kernel and the average output signal power of the second kernel are maintained substantially equal.

10. The wireless communication system of claim 3, wherein the single-carrier modulation scheme is according to 802.11b Barkers and wherein the multi-carrier modulation scheme is according to the 802.11a standard employing orthogonal frequency division multiplexing (OFDM).

11. The wireless communication system of claim 3, wherein the first kernel employs a first sample rate clock, wherein the second kernel employs a second sample rate clock, wherein the first and second sample rate clocks are aligned at predetermined timing intervals, and wherein a first full sample of the multi-carrier modulation scheme begins one timing interval after the beginning of a last sample of the single-carrier modulation scheme.

12. The wireless communication system of claim 3, wherein the single-carrier signal from the first kernel is terminated according to a windowing function specified for OFDM signal shaping defined in the 802.11a standard.

13. The wireless communication system of claim 3, wherein carrier frequency is coherent between the first and second kernels.

14. The wireless communication system of claim 3, wherein carrier phase is coherent between the first and second kernels.

15. The wireless communication system of claim 14, wherein carrier phase of the second kernel multi-carrier signal is determined by carrier phase of a last portion of the second kernel single-carrier signal.

16. The wireless communication system of claim 15, wherein carrier phase of the second kernel multi-carrier signal is rotated by a corresponding one of a plurality of rotation multiples, each rotation multiple corresponding to one of a plurality of predetermined phases of the last portion of the second kernel single-carrier signal.

17. The wireless communication system of claim 16, wherein the first kernel single-carrier modulation scheme is according to 802.11b Barkers in which each Barker word is one of first, second, third and fourth possible phases, wherein the second kernel multi-carrier modulation scheme is according to OFDM as defined in Annex G of the 802.11a standard, and wherein OFDM symbol are rotated by the second kernel by zero if the last Barker word has the first phase, by 90 degrees if the last Barker word has the second phase, by 180 degrees if the last Barker word has the third phase, and by −90 degrees if the last Barker word has the fourth phase.

18. The wireless communication system of claim 3, wherein a requisite fidelity of the entire mixed waveform configuration is specified by a requisite fidelity specified for the multi-carrier scheme.

19. The wireless communication system of claim 18, wherein the requisite fidelity is a function of data rate of the second portion and is determined by mean-squared-error normalized by signal power as specified for OFDM in the 802.11a standard.

20. The wireless communication system of claim 2, wherein a symbol rate clock and a carrier frequency of the waveform are derived from the same reference clock.

21. The wireless communication system of claim 20, wherein part per million (PPM) error of a clock fundamental for symbol rate and PPM error of a clock fundamental for carrier frequency are substantially equal.

22. The wireless communication system of claim 2, wherein the receiver comprises:

a single-carrier receiver;

a multi-carrier receiver, coupled to the single-carrier receiver; and

a switch, coupled to the single-carrier receiver and the multi-carrier receiver, that provides a first portion of a signal being received to the single-carrier receiver and that provides a second portion of the signal being received to the multi-carrier receiver;

wherein the single-carrier receiver acquires a first portion of an incoming signal including the preamble and header and determines a channel impulse response (CIR) estimate, and wherein the multi-carrier receiver uses the CIR estimate for a second portion of the incoming signal.

23. The wireless communication system of claim 22, further comprising:

the single-carrier receiver including a first equalizer, wherein the single-carrier receiver programs taps of the first equalizer based on the CIR estimate; and

the multi-carrier receiver including a second equalizer, and wherein the multi-carrier receiver modifies taps of the second equalizer based on the CIR estimate determined by the first equalizer.

* * * * *

EXHIBIT G

US005712870A

United States Patent [19]

Petrick

[11] Patent Number: 5,712,870

[45] Date of Patent: Jan. 27, 1998

[54] **PACKET HEADER GENERATION AND DETECTION CIRCUITRY**

[75] Inventor: **Al Petrick**, Orlando, Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **509,462**

[22] Filed: **Jul. 31, 1995**

[51] **Int. Cl.**[6] **H04B 15/00**

[52] **U.S. Cl.** **375/206**; 375/200; 375/279; 375/308; 370/206; 370/320

[58] **Field of Search** 375/200, 206, 375/207, 208, 219, 220, 261, 298, 279, 280, 308, 329, 364, 367, 332; 370/206, 207, 320, 335, 342, 349, 350, 465, 466, 474

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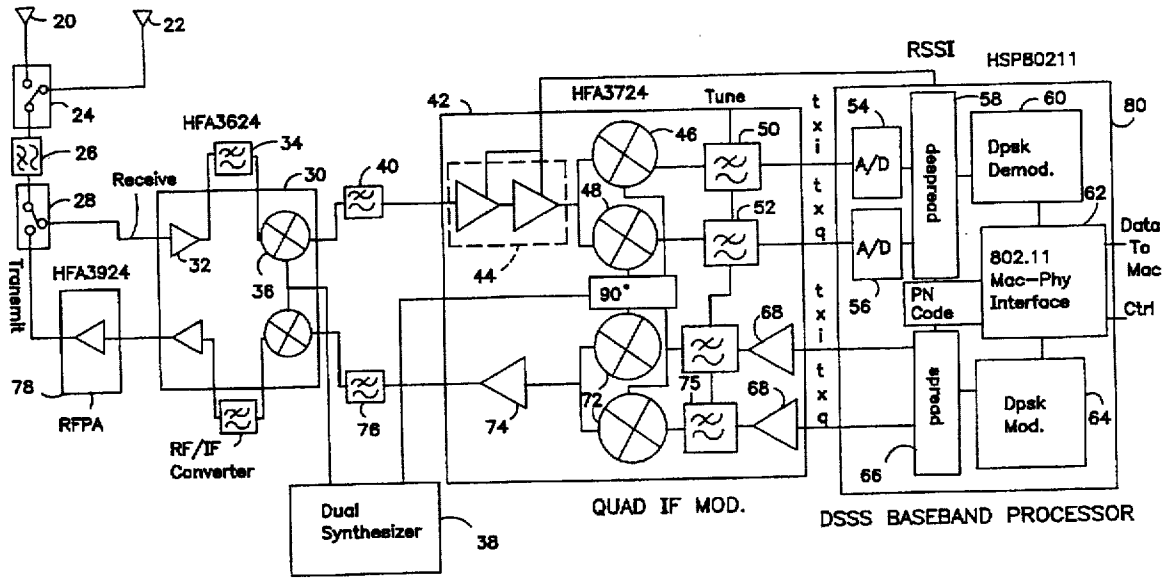
Primary Examiner—Wellington Chin
Assistant Examiner—Congvan Tran
Attorney, Agent, or Firm—Rogers & Killeen

[57] **ABSTRACT**

A method and apparatus for receiving and transmitting direct sequence spread spectrum signals uses a single integrated device for converting and demodulating an RF signal into a serial data signal. Critical timing relationships during the acquisition and demodulation of the received signal are satisfied by the use of an integrated circuit specially designed to perform all operations needed to convert the physical signal to an media access circuit level data signal.

20 Claims, 3 Drawing Sheets



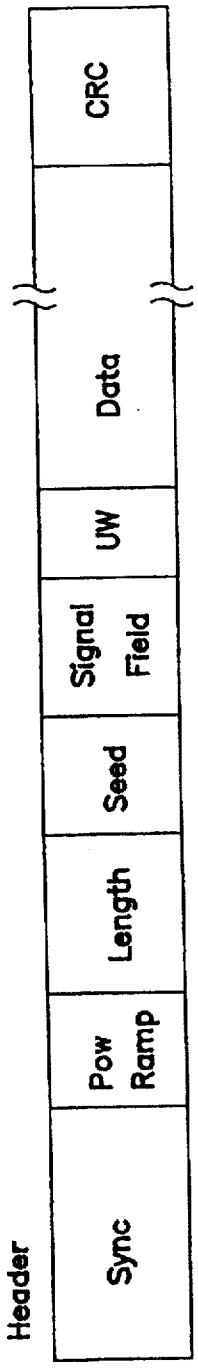


FIG. 1

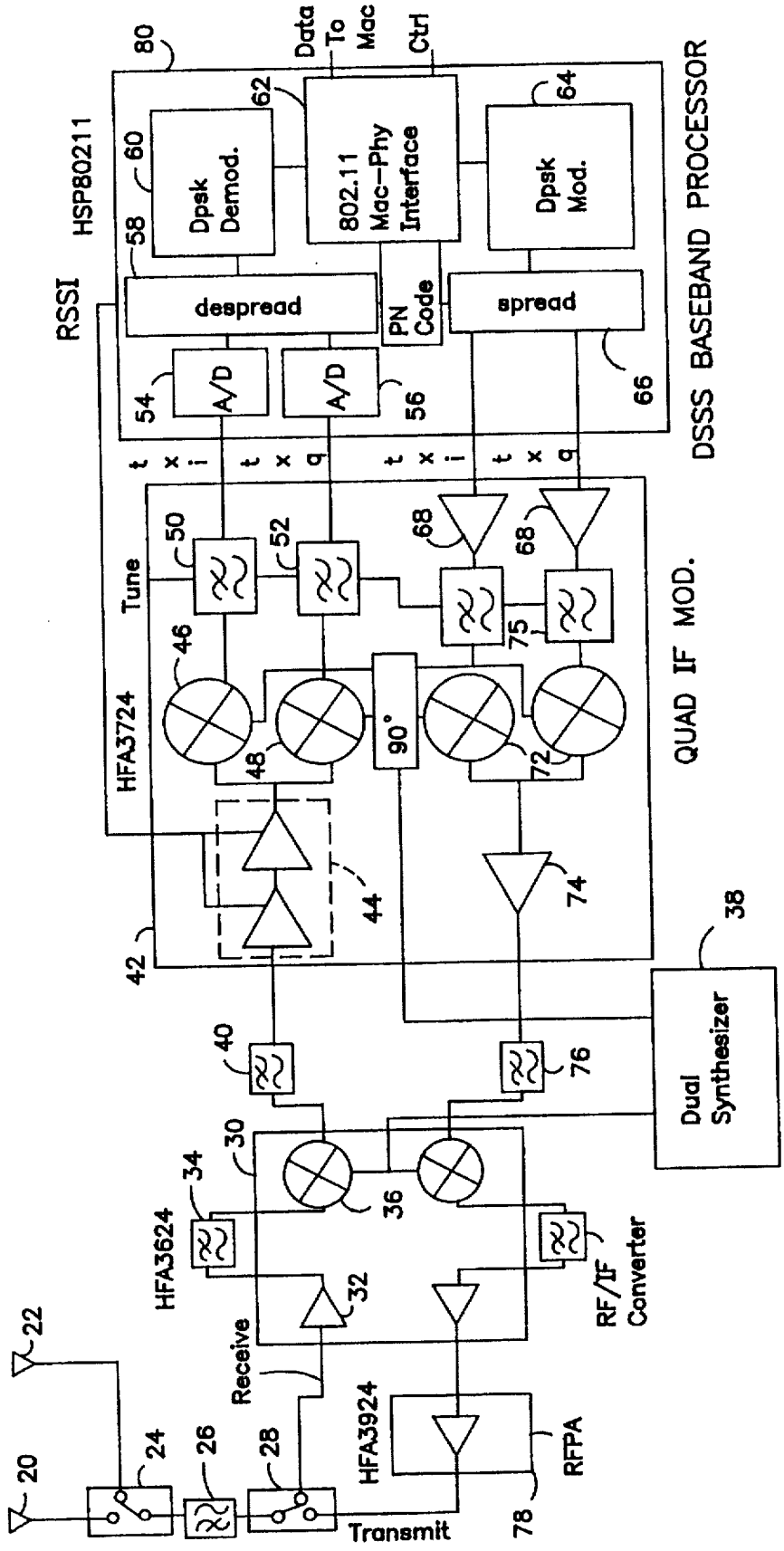

80
Data To Mac
Ctrl
HSP80211
62
64
60
58
Dpsk Demod.
802.11 Mac-Phy Interface
Dpsk Mod.
RSSI
despread
PN Code
spread
DSSS BASEBAND PROCESSOR
54
A/D
56
A/D
66
t x i
t x q
t x i
t x q
50
52
68
68
Tune
75
46
HFA3724
48
90°
72
QUAD IF MOD.
44
74
42
38
Dual Synthesizer
40
76
30
34
36
HFA3624
32
RF/IF Converter
22
Receive
HFA3924
RFPA
20
24
26
28
Transmit
78

FIG. 2

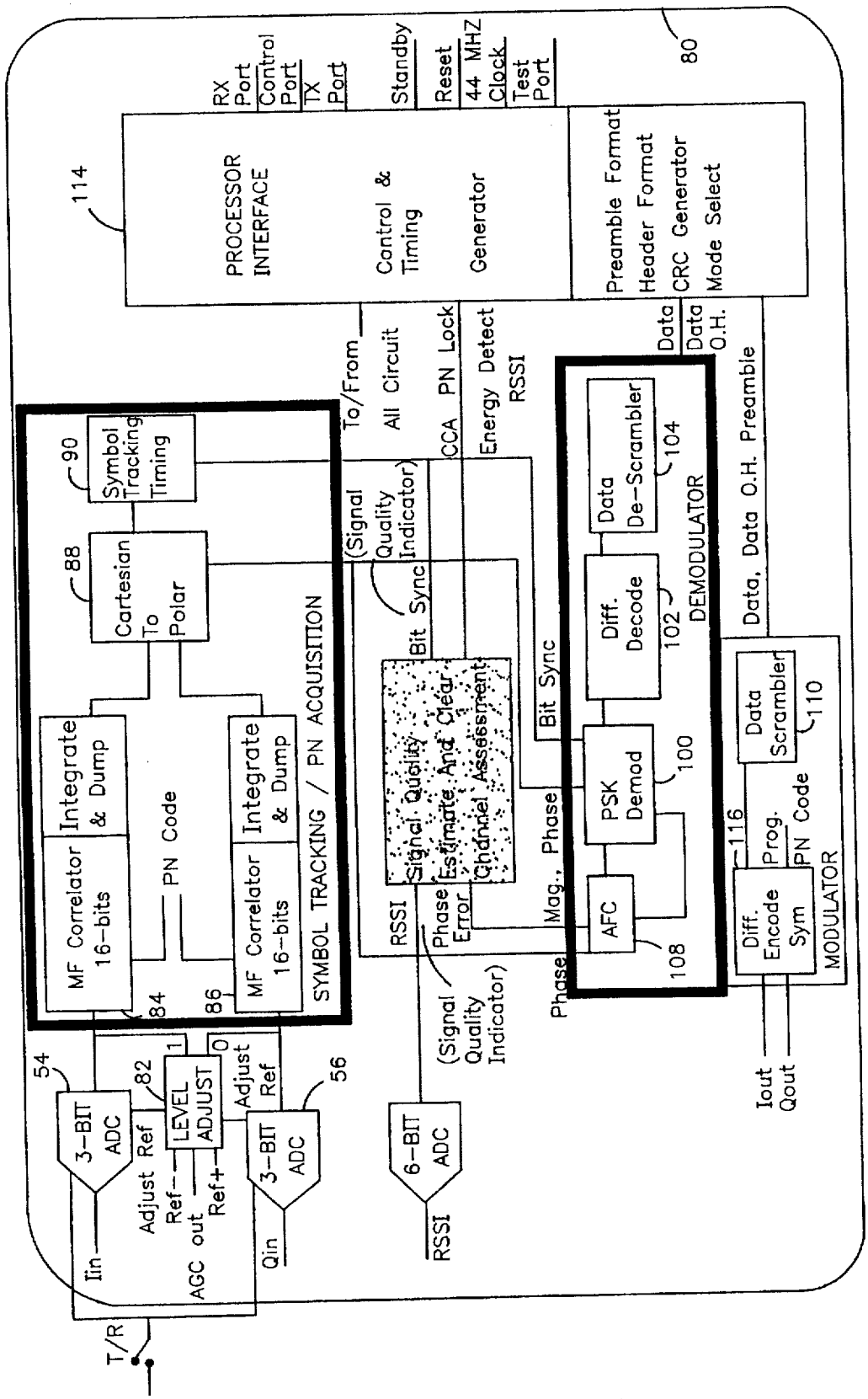

80
RX Port
Control Port
TX Port
Standby
Reset
44 MHZ Clock
Test Port
114
PROCESSOR INTERFACE
Control & Timing Generator
Preamble Format
Header Format
CRC Generator
Mode Select
To/From All Circuit
CCA
PN Lock
Energy Detect
RSSI
Data
Data O.H.
Data, Data O.H. Preamble
90
Symbol Tracking Timing
88
Cartesian To Polar
(Signal Quality Indicator)
Bit Sync
Signal Quality And Channel Assessment
Integrate & Dump
MF Correlator 16-bits
PN Code
84
86
SYMBOL TRACKING / PN ACQUISITION
Data De-Scrambler
104
Diff. Decode
102
DEMODULATOR
PSK Demod
100
AFC
108
Mag., Phase
Phase Error
RSSI
Phase
(Signal Quality Indicator)
Data Scrambler
110
116
Prog. PN Code
Diff. Encode Sym
MODULATOR
Iout
Qout
54
3-BIT ADC
Iin
82
LEVEL ADJUST
Adjust Ref
Ref-
Ref+
AGC out
1
0
Adjust Ref
56
3-BIT ADC
Qin
6-BIT ADC
RSSI
T/R

FIG. 3

PACKET HEADER GENERATION AND DETECTION CIRCUITRY

BACKGROUND OF THE INVENTION

The present invention is related generally to receivers for acquiring radio-frequency signals and, particularly, to receivers for acquiring data from signals which may have been transmitted in a spread spectrum system.

Wireless systems have been developed and proposed in the prior art in which plural radio frequency ("RF") transmitters send bursts of messages to a receiver which must acquire the signal from each transmitter and decode the data contained therein. For example, in a wireless Local Area Network ("LAN") plural nodes which are not necessarily geolocated together may each communicate with a base station (or even with each other) and transmit data to and from the base station for the use by applications located at the nodes. Because the system is wireless, the transmissions are made using the ether. In simple systems, a base station may be able to communicate with only a single remote node during any given time period. Obviously, such an arrangement limits the amount of data which can be passed between the nodes and the base station in a given period of time. To increase the amount of data which may be transmitted, it is known for a wireless system to use plural distinct frequencies the use of which is arbitrated or determined by the system. In this way, several remote nodes may be transmitting to or receiving data from the base station simultaneously. Such systems tend to use a relatively large bandwidth of the available spectrum and are relatively expensive in forcing the base station to have plural transceivers and for the nodes to be capable of communicating on plural frequencies. In addition, in such prior art systems, the allocation of frequencies for communications may consume a relatively large portion of the available processing resources and degrade the ability of the system to communicate data. In still other prior art systems, the various nodes and the base station may use a time-division multiplex protocol in which a base unit allots periods of time to nodes requiring data communications and controls the communication by the nodes during the assigned time periods. Again, the overhead in processing resources needed to manage the system and the consumption of communication resources by control messages may be relatively high for such systems.

Another means by which plural remote nodes may communicate with a base station or other nodes is the use of PN-encoded spread spectrum technology. In a typical spread spectrum signal, the signal to be transmitted is modulated with a pseudorandom noise ("PN") code. Demodulating such a signal generally involves the demodulating of a received signal by the same PN code as was used to modulate the signal. Once the signal is demodulated, it may be correlated to ensure that an actual signal was present, and subsequently demodulated/decoded to extract the data. One of the benefits of such spread spectrum systems is that multiple nodes may be simultaneously transmitting without necessarily destroying each other's signals. Thus, some of the inter-nodal timing problems of other prior art systems are reduced. The use of such spread spectrum systems is also often beneficial to the ability of the receiver to acquire and decode the signal in high noisy environments.

In spread spectrum signal communications, as in many wireless communications systems, it is often desirable to communicate between nodes and the base station in short, bursty packets of data. Bursty communications generally permits many nodes (which often have bursty communications needs) to be joined in a system without significant degradation at any one node, i.e., each node receives an opportunity to communicate within a desired latency period. Thus, in some communications systems, it is desirable to have messages be relatively short to ensure that each node has an opportunity to communicate within an acceptable latency period.

Typical spread spectrum messages generally include a data portion containing the data to be transmitted preceded by a preamble or header portion used for synchronization of the receiver to the signal being transmitted and a check portion (often a Cyclical Redundancy Check, CRC) which provides signals whereby the correctness of the decoded message may be determined. Particularly when data messages are desired to be bursty, and thus short, the length of the preamble may be significant in determining the data bandwidth of the system or the amount of data which can be communicated within a particular period of time. Generally, the smaller the preamble for a system having a particular speed, the greater is the available data bandwidth. Short preambles, however, generally provide the receiver with less information on which to synchronize.

In a typical wireless LAN using bursty communications, the system can be characterized as having multiple bursts from various transmitters, each of which must be acquired and decoded by the receiver. The problems of acquiring such signals is made all the more difficult if, as is sometimes the case, the plural nodes provide communication signals having varying signal strengths and signal to noise ratios and if the start of the communications from the various nodes is not synchronous. Often in such wireless LAN systems, the receiver has no apriori knowledge of the time of the start of a communication, or the particular off-nominal characteristics of the sending node. Each sending node, for example, may have a different frequency offset or frequency drift which affects how its signal must be acquired and/or decoded.

In prior art systems, baseband processors were typically used to extract data from PN modulated spread spectrum signals (and to modulate a signal to be transmitted with PN modulation). Typical prior art baseband processors used a symbol length matched filter correlator, with the output acquired by a phase locked loop, to remove the offset frequency of the carrier. In such systems, the matched filter is set to match the PN code sequence used for the spread spectrum link. Generally, in such prior arts systems, acquisition of the signal is declared based on the amplitude of the correlation output peaks from the matched filter. The disadvantage of this typical prior art approach is that the phase locked loop is relatively slow and may have large amounts of jitter if the signal is near the noise level. If the presence of the signal is falsely declared on the basis of the noise, the desired signal may be rejected. In addition, the slow acquisition may preclude the use of a diversity of antennas, particularly where the message preamble is relatively short in duration. In some prior art systems, plural parallel receive paths are used for the diverse antennae so that each antenna may be evaluated in parallel. Obviously, such duplication of elements is relatively expensive in terms of cost, power and area.

Another aspect which influences the design and operation of prior art baseband processors involves the A/D sampling of the baseband signal. A low cost direct sequence baseband demodulator utilizes as few bits as possible in the A/D sampling converter used to sample the I and Q signals while maintaining acceptable system performance. Each bit of an additional A/D flash converter approximately doubles the

number of comparators needed. Additionally, in the light of the fact that the A/D converter will experience several dB of variation at the Rf and IF chain because of variances in manufacturing tolerances and temperature effects, unless means are taken to eliminate the effects of these variances, up to one-half the dynamic range of a prior art A/D device may become unavailable.

One prior art solution to the problems of dynamic range in a direct sequence spread spectrum system is to increase the number of bits in the A/D converter until acceptable performance is achieved by the demodulator. The nominal signal level may then be set such that at the minimum signal level into the A/D converter, the required number of effective bits is met, and at the maximum signal level, saturation of the A/D converter is held to an acceptable level. The disadvantages of such an approach are generally seen in the additional size and corresponding cost of the A/D converter which would not be required for operation at nominal signal levels. Additionally, such approaches are generally disadvantageous in that the circuits following the A/D converter must also be designed to carry these additional bits, substantially increasing the amount of hardware and operational power requirements.

During signal acquisition and synchronization in direct sequence spread spectrum systems, it is usually necessary to adjust the timing of the receiving system to the bit timing of the received signal. By adjusting the timing, the receiving system can increase the probability that it is correctly acquiring and demodulating the correct signal. Many prior art systems used a voltage controlled oscillator ("VCO") to adjust the A/D sampling phase. This solution has the advantage of obtaining very fine sampling phase resolution but generally requires costly analog components. Another prior art solution has been to oversample the A/D input and use the closest samples. This solution, however, generally requires very fast and high power consumption A/D converters.

It is known in the prior art to demodulate a received direct sequence spread spectrum signal by using the in phase (I) and quadrature (Q) components from the correlator in the demodulator system and to use the bit synch amplitude to determine the signal quality. In such prior art systems, carrier frequency offset may be compensated for by the use of differential demodulation or by phase locked loop tracking of the carrier. Independent processing of both the I and Q components, however, generally requires twice the hardware through most of the signal processing path (one complete set of hardware for each signal component). In addition, in prior art systems, the phase locked loops can be relatively hardware intensive ad complex in order to achieve the speed necessary to acquire the short preambles of bursty communications.

Within the environment of a wireless LAN or other plural node system, it is desirable to be able to decode the communicated signals reliably: not permitting false data to be accepted as true and capturing with a high degree of probability the data which is transmitted. In addition, it is desirable to obtain such high performance while keeping relatively low the costs, sizes and power consumption of the hardware used in such systems.

Accordingly, it is an object of the present invention to provide a novel method and apparatus of acquiring a spread spectrum signal reliably and without false alarms.

It is another object of the present invention to provide a novel method and apparatus of acquiring a spread spectrum signal from one of plural transmitting nodes without prior knowledge of the time of the start of the signal.

It is yet another object of the present invention to provide a novel method and apparatus of acquiring a spread spectrum signal with a relatively small preamble in comparison to prior art systems.

It is still another object of the present invention to provide a novel method and apparatus of acquiring a spread spectrum signal from one or more of plural transmitters, having independent frequency and/or phase offsets.

It is a further object of the present invention to provide a novel method and apparatus of acquiring a spread spectrum signal in an environment having a relatively low signal to noise ratio and/or having a rapidly changing noise characteristic.

It is yet a further object of the present invention to provide a novel method and apparatus of acquiring a signal transmitted in accordance with the IEEE 802.11 standard.

It is still a further object of the present invention to provide a novel method and apparatus to acquire spread spectrum signals whether or not transmitted using the IEEE 802.11 standard.

These and many other objects and advantages of the present invention will be readily apparent to one skilled in the art to which the invention pertains from a perusal of the claims, the appended drawings, and the following detailed description of the preferred embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a representational diagram of the format of a type of signal which can be communicated in one embodiment of the present invention;

FIG. **2** is a functional block diagram of a communications transceiver which may be used in accordance with the present invention; and

FIG. **3** is a functional block diagram of a baseband processor which may be used in the transceiver of FIG. **2**.

DESCRIPTION OF PREFERRED EMBODIMENTS

Standards have been proposed and are being developed for the communication of signals in a wireless LAN system. These standards include IEEE 802.11 typically utilize a short, bursty message format. As shown in FIG. **1**, a typical message may consist of a fixed length preamble having the fields for power ramping, synchronization, a signal field, a descrambling seed, and a unique word. Immediately upon the end of the preamble, the data starts followed by a CRC field. As specified in IEEE 802.11, the preamble may be modulated onto the carrier signal using digital Binary Phase Shift Keyed ("BPSK") modulation. The data and CRC signals may be modulated using either BPSK or Quarternary Phase Shift Keyed modulation ("QPSK"). A transceiver in accordance with the present invention may readily acquire and decode the preamble, data and CRC portions of a standard message packet. However, the present invention is in no way limited to this one packet format and may be used in many other formats.

With reference to FIG. **2**, a transceiver using one aspect of the present invention may include dual antennae **20**, **22** which can be operatively connected to the remainder of the transceiver through a selector switch **24** and a conventional antenna coupler **26** which matches the impedance of the signal to/from the antennae **20**, **22** to the transceiver. A second selector switch **28** connects the antenna coupler **26** to either a transmit circuit or a receive circuit of the transceiver. In the receive circuit, the second selector switch **28** is

connected to an RF/IF converter **30** which amplifies the incoming signal through an amplifier **32**, a bandpass filter **34** and a down conversion mixer **36**. The down conversion mixer **36** also receives a clock signal from a synthesizer **38**.

With continued reference to FIG. **2**, the received signal exiting the RF/IF converter **30** may again be filtered to remove higher frequency signals therefrom in a second filter **40** and provided to a quadrature IF modulator/demodulator **42**. Within the modulator/demodulator **42**, the received signal may be passed through a two stage integrating limiting amplifier **44** which amplifies the received signal and provides a signal indicating the Received Signal Strength (RSSI) of the incoming signal. The amplified incoming signal may be split into I and Q (in-phase (real) and quadrature (imaginary)) components and mixed in dual mixers **46**, **48** with a demodulating signal and a signal 90 degrees out of phase with the demodulating signal. Each of the mixed signals may be filtered by conventional antialiasing and shaping filters **50**, **52** to provide two baseband signals, one of which is the I component and the other is the Q component of the intermediate frequency demodulated signal (RXI RXQ). (note that at this time, the received signal contains data which has been PN modulated (i.e., spread) and PSK modulated). The I and Q component signals may be provided to a baseband processor which converts the analog signals to digital signals at A/D converters and which despreads the spread spectrum signal through a despreader **58**. The despread signal may be demodulated by a demodulator to provide a digital data signal which may be passed to an application system through an interface circuit **62**.

With continued reference to FIG. **2**, data to be transmitted may be received by the interface circuit **62** and then used to generate a spread spectrum modulated signal through a modulator **64** and a data spreader **66**. The spread signal from the spreader **66**, in the form of its I and Q components, may be amplified, filtered and modulated within the modulator/demodulator **42** by amplifiers **68**, filters **70** and mixers **72**. The modulated signal output from the mixers **72** may be amplified by an amplifier **74**, filtered by a filter **76** and upconverted to RF by the RF/IF converter **30**. The transmit signal output from the converter **30** may be power amplified by power amplifier **78** and then provided to one of the antennae, as selected by the switch **24**.

In operation, a signal received at the antennae **20**, **22** may be passed through the coupler **26**. In one aspect of the present invention, each antennae may be used for a portion of the preamble of a message and the antenna receiving the better signal can be utilized to receive the data signal. Additional details regarding the antenna selection method and apparatus may be obtained from U.S. Pat. No. 5,694,417, entitled "Short Burst Acquisition Circuit for Direct Sequence Spread Spectrum Links" assigned to the same assignee as the present application and filed on even date herewith, which is incorporated herein by reference.

The signal received at the antennae may be provided to the receive portion of the RF/IF converter **30** and there be amplified by the amplifier **32**, which may be a low noise amplifier. The amplified signal may be filtered by a bandpass filter, such as a filter centered at 2.5 GHz and having a 1 GHz RF frequency range. The filtered signal may be mixed in the mixer **36** with a downconversion signal to develop an Intermediate Frequency ("IF") signal. In an embodiment of the present invention, the downconversion signal may be a sinusoidal signal generated by a local synthesizer and may have a frequency in the range of 2.1 to 2.49 GHz. Thus, in one embodiment, the IF signal may have a range of from 10 to 400 MHz.

The RF/IF converter **30** may have independent enable and power circuits for each of the receive and transmit portions. By powering down the portions of the circuit not in use, the RF/IF converter **30** reduces the power consumption of the device and, significantly, provides isolation between the receive and transmit portions of the circuit. Such isolation may be particularly significant in time division multiplexed systems.

The receive signal output from the RF/IF converter **30** may be filtered through a bandpass filter **40** and provided to the quadrature IF modulator/demodulator **42** in which the signal is amplified in the two stage integrating limiting amplifier **44**. The limiting amplifier **44** may include circuits to provide baseband antialiasing and shaping to the received signal. The limiting amplifier **44** may also provide a Receive Signal Strength Indicator (RSSI) signal to receive-downstream elements.

With continued reference to FIG. **2**, after the receive signal has been amplified by the limiting amplifier **44**, the signal may be split and each form of the resulting signal provided to the input the mixers **46**, **48**. One mixer mixes the receive signal by a locally synthesized periodic signal and the other mixer mixes the receive signal by a signal which is ninety degrees out of phase with the first periodic signal, as is well known in quadrature demodulation. The result of the signal mixing are two signals, one the I (in-phase or real) component of the demodulated receive signal and the other the Q (quadrature or imaginary) component of the demodulated receive signal. Note that if the receive signal is a spread spectrum PSK signal, the I and Q components signals are spread spectrum PSK modulated signals at the output of the mixers **46**, **48**. The I and Q component signals may each be filtered in tunable filters **50**, **52**.

In one embodiment of the present invention, the quadrature IF modulator/demodulator **42** may have a frequency range of between 10 to 400 MHz and the limiting amplifier **44** may provide in excess of 80 dB of gain.

In similar (but opposite) manner to the receive side of the quadrature IF modulator/demodulator **44**, the transmit portion may amplify, filter and quadrature mix I and Q signals received from the baseband processor for transmission as a transmit signal. The transmit signal output from the transmit mixers **72** may be amplified, upconverted (by the RF/IF converter **30**) and further amplified (by the power amplifier **78**) to radiating power levels. The amplified transmit signal may thereafter be provided to one of the antennae **20**, **22** after being impedance matched in the impedance matching circuit **26**.

With reference to FIG. **3**, a baseband processor in accordance with the present invention may provide all of the functions necessary for spreading and despreading, modulating and demodulating, differential phase shift keyed signals ("DPSK") for full duplex data packet transmission. While the present invention is not necessarily limited to a single device, the performance of all of these functions on a single device provides substantial advantages over other designs in which these functions or portions of these functions are handled by plural hardware or software driven devices. These advantages include lower power requirements, better signal timing and synchronization, reduced device area and reduced cost.

With continued reference to FIG. **3**, in which like reference numerals are used for like elements to those of FIG. **2**, the baseband processor receives the I and Q signals from the modulator/demodulator **42** via the A/D converters **54**, **56**. The A/D converters are maintained in tolerance over a

variety of conditions through a level adjust circuit **82**. The A/D converters may be three bit converters which each provide their digital outputs to correlator circuits **84**, **86** which acquire the signal of interest by detecting the pseudorandom noise ("PN") code in use for the particular spread spectrum link. The correlators **84**, **86** may be matched filter correlators which (1) despread the wideband direct sequence spread spectrum ("DSSS") signal information to convert it back to the original data rate; and (2) spread unwanted interfering signals and noise to separate them spectrally from the data.

The correlators **84**, **86** may receive a PN code of variable length, programmable up to 16 bits. The correlators **84**, **86** are each dedicated to one of the component channels (I and Q) and have a common correlation reference which can be varied in both length and sequence to permit the system to be used to demodulate a wide variety of signal types. As is explained in more detail in the copending application entitled "SHORT BURST ACQUISITION CIRCUIT FOR DIRECT SEQUENCE SPREAD SPECTRUM LINES" filed on even date herewith, and incorporated herein by reference, the received signal may be sampled at twice the chip rate and the correlators have taps on every other stage. The output signal from the correlators are converted from I and Q form to polar form by a cartesian to polar converter **88**. The polar form of the signal is used in the remainder of the demodulator processing, reducing the need for duplicate hardware for the independent I and Q channels.

A symbol tracking and timing circuit **90** is used to track the peak correlation magnitude and to control chip timing resolution to plus/minus one-quarter chip. The symbol tracking and timing circuit **90** can be a circuit such as described in more detail in "FAST ACQUISITION BIT TIMING LOOP METHOD AND APPARATUS", filed on even date herewith and incorporated herein by reference. The symbol tracking and timing circuit **90** averages the individual correlator samples over a desired period, such as the dwell period of the system on one of the antennae during the preamble. By averaging the samples, the effect of noise is reduced, permitting an improved ability to resolve a small early or late bias.

In the tracking and timing circuit **90**, the magnitude of the correlator output ample are accumulated modulo the number of samples in a symbol. In this way, a sum of the correlator magnitudes is formed at each one sample phase of symbol timing. The best sample phase will produce a discernible peak with smaller samples on either side. All other samples will generally consist of accumulated noise and will be smaller in the sum of magnitudes. If the received signal is strong, the magnitudes provided by the correlator will be large and, in conventional designs, would have required an accumulator and other downstream equipment to maintain extra bits to prevent overflow. In contrast, in the present invention, overflow is prevented in large signals while maintaining accuracy on poor signals by barrel shifting the accumulations of magnitude when the largest value gets above one-half full scale. In one embodiment of the present invention, this value can be readily trapped by tracking the most significant bit ("MSB") of the accumulation. When the MSB of an accumulation is set to 1 (all numbers from the correlator are magnitudes and therefor positive), all of the accumulations and the subsequent outputs of the correlator are right shifted by one bit. The number of shifts may be counted and is similar in fashion to an exponent. Thus, the sample having the largest sum of magnitudes may be identified without adding extra bits to the accumulators and downstream equipment while maintaining, with the accumulator and exponent, and absolute indication of the strength of the received signal.

With continued reference to FIG. **3**, the polar signal produced by the cartesian to polar converter **88** is provided to a PSK demodulator **100**, and in turn to a differential decoder **102** and to a data descrambler **104**. The PSK demodulator can demodulate both BPSK and QPSK signalling. In one aspect of the present invention, the preamble of a received signal may be in BPSK format and the data of the received signal may be in either BPSK or QPSK format. Because QPSK and BPSK signals are modulated differentially, the symbol information is based upon the state of the previous symbol. Phase errors introduced by multipath and oscillator offset drifts are compensated by a phase locked carrier tracking loop **108**. In one embodiment, the loop uses an NCO providing eight bits of phase output to the PSK demodulator **100**, and may be variously set to track and adjust for phase offset errors by rotation of the signal phase. The phase and frequency information developed during the preamble of a message is used to preset the loop **100** for minimum loop settling time.

With continued reference to FIG. **3**, in one embodiment of the present invention, signal quality (SQ) and signal frequency (SF) measurements are made simultaneously with symbol timing measurements. When the bit synch level, signal quality (SG) and the Received Signal Strength Indicator (RSSI) are all above their respective thresholds, the received signal is declared present. As explained in detail in co-pending U.S. application Ser. No. 509,586, entitled "A METHOD OF ESTIMATING SIGNAL QUANTITY FOR A DIRECT SEQUENCE SPREAD SPECTRUM RECEIVER", filed on even date herewith and incorporated herein by reference, decisions as to which of two antennae would be used to receive data can be made after taking measurements during the dwell period for each antenna. Once a particular antenna is selected, the measured symbol timing and carrier frequency offset for the selected antenna is jammed into the symbol timing and into the phase-locked-loop of the NCO tracking the carrier to begin carrier de-rotation. In this way, the demodulating circuitry gets a "head start" in reacquiring and demodulating the incoming preamble data within the brief period desired for bursty communications.

The data descrambler **104** may be a self synchronizing circuit having programmable (or user settable) taps comprising 7 bit shift registers. For data to be transmitted, a similar data scrambler **110** is used. The data scrambler **110** can be selectively disabled for measuring RF carrier suppression, during which an alternating **1/0** pattern is transmitted. Likewise, the data descrambler may be selectively disabled to permit data to pass without change from the differential decoder **102** to the processor interface **114**.

Data to be transmitted may be received from an external device by the processor interface **114**. The processor interface **114** may generate a preamble, CRC and other protocols to be sent along with the data and to provide the data and other protocol signals to the data scrambler **110** and to a differential encoder **116** to develop PN modulated I and Q signals which can be provided to a quadrature IF modulator such as the modulator **42** of FIG. **2** for eventual transmission on an antenna.

Descrambled data may be provided to a processor interface **114** which may control the passage of the data to another device such as a media access control ("MAC") circuit.

With continued reference to FIG. **3**, it has been found that placing the entire baseband processor onto a single chip can

provide considerable benefit to accurate and timely demodulation of received signals and the extraction of data therefrom, particularly for bursty, brief data packets. As contrasted with the known prior art in which various of the portions of circuits similar to the circuits of the baseband processor of FIG. **3** have been provided by separate hardware devices and/or by separate complex programmable devices, the present invention is particularly suited to integration into a single device.

The baseband processor of FIG. **3** may be used to transfer packetized data received in the form of serial data in a physical layer to a media access control ("MAC") layer imbedded in the packetized data are header information used to control the physical layer. The header information may include fields of preamble/sync, unique word, signal field, service field, length field and a CRC field. The signal field is used to specify the signalling type used to modulate the data: either DPSK or QPSK. In one embodiment, the processor may receive data in which the header is in BPSK but the data is in QPSK. In such situations, the timing of switching the receiver from one signalling format to another is time critical. In another aspect of the present invention, the number of fields in the header may be user selectable.

It is known in the prior art that interfaces between the physical layer and the MAC level may be either serial or parallel. Most prior art implementations are parallel because the of the severe timing restrictions in which parallel circuits permit quicker timing but at the considerable additional expense of parallel hardware. Often the physical layer tasks of header generation and detection are done at the MAC layer, usually by separate devices. In contrast, in the present invention, all of the header detection and similar physical layer tasks may be imbedded into a single device.

In prior art devices where the header and similar physical layer tasks are handled by separate circuits/devices, there passes some period of time between when the circuit detects and demodulates an acceptable header and the transmission of that state to the circuit demodulating the data. In the preset invention, where the number of bits in the header is held to a minimum and may be used to determine which of plural antennae are to be used in addition to the other customary header functions, the slip of a single bit may mean the difference between successfully decoding a message and missing the message.

During demodulation of the header, the present invention monitors and uses the header data to both identify the type of signalling to be used for the data but to select between plural antennae. By using the data developed in the preamble for immediate data decoding, the number of lost bits is minimized. In receiving the header, the baseband processor converts the serial data from the data descrambler **104** into a 16 but parallel word which is compared with the preselected vales for the unique word and the signalling fields. The unique word is searched for a fixed amount of time and if it is not found, the modulator/demodulator is reset and acquisition of the RF signal is restarted. Once the unique word is found, a field counter searches through the incoming bits in a parallel fashion for the fields making up the header. As each fields is detected, the received data is stored into internal registers for access through the serial control bus the signalling field, when detected, is used to switch the receiver modulator/demodulator between BPSK and QPSK at the correct time with respect to the data portion of the packet. When the length field is detected, this value is loaded into a counter and is used to track the incoming bits of the data packet and to signal the MAC layer when the last bit of the packet is received. The processor interface **114** may also compute the CRC on the fly and compare the computed CRC to the CRC received within the message. If the CRCs do not match the receive data packet may be terminated and the receiver reset into reacquisition.

While preferred embodiments of the present invention have been described, it is to be understood that the embodiments described are illustrative only and the scope of the invention is to be defined solely by the appended claims when accorded a full range of equivalence, many variations and modifications naturally occurring to those of skill in the art from a perusal hereof.

What is claimed is:

1. A circuit for detecting a message header in a signal which has been transmitted using direct sequence spread spectrum modulation, comprising a single device having:

means for receiving an analog signal having modulated thereon in a spread spectrum format a message having a header portion and a data portion;

means for converting said analog signal into a digital signal;

means for demodulating the header of the digital signal using digital binary phase shift keyed (BPSK) demodulation and for demodulating the data portion of the same message using quarterary phase shift keyed demodulation (QPSK);

means contained on said single device for timing a transition from BPSK mosulation to QPSK modulation; and,

means for providing the demodulated data signal to a media access control (MAC) layer.

2. The circuit of claim **1** further comprising means for adjusting said means for timing to account for headers of variable length.

3. The circuit of claim **2** wherein said means for adjusting is contained within said single device and wherein said means for adjusting is responsive to a data field within said message header.

4. The circuit of claim **1** wherein said single device is a single monolithic device.

5. The circuit of claim **1** wherein said analog signal is in the form of in-phase and quadrature components.

6. The circuit of claim **5** wherein the data within said signal is modulated using PN modulation and phase shift keyed modulation.

7. The circuit of claim **5** further comprising means to evaluate during the header portion of the message the signals received from plural antennae and to select one of said antennae for use during the receipt of the data portion of the same message.

8. The circuit of claim **7** wherein the circuit is contained on a single monolithic device.

9. The circuit of claim **8** wherein said circuit acquires a unique word within a message header and if no unique word is acquired within a predetermined period of time resets the circuit.

10. In a communication system capable of receiving RF direct sequence spread spectrum signals, said system having a message header detection circuit comprising a single device having:

an analog receiver for receiving a spread spectrum modulated signal having a header portion and a data portion;

an analog-to-digital converter operable on said modulated signal;

a digital demodulator for binary phase shift keyed (BPSK) demodulation of said header portion and quaternary phase shift keyed (QPSK) demodulation of said data portion;

a timer for transitioning between the BPSK demodulation and the QPSK demodulation; and,

an interface for providing the demodulated data signal to a media access control (MAC) layer.

11. The circuit of claim **10** wherein said timer is adjustable to account for headers of variable length.

12. The circuit of claim **11** wherein the adjustability of said timer is based on information contained within a data field of said header portion.

13. The circuit of claim **10** further comprising antenna selection circuitry for selecting, upon evaluation of said header portion obtained from a plurality of antennae, one of said plurality for receipt of the associated data portion of said header portion.

14. The circuit of claim **13** wherein the circuit is contained on a single monolithic device.

15. The circuit of claim **14** wherein said circuit acquires a unique word within said header portion and if no unique word is acquired within a predetermined period of time the circuit resets.

16. The circuit of claim **10** wherein the analog signal received is in the form of in-phase and quadrature components and the data within the signal is modulated using PN modulation and phase shift keyed modulation.

17. A direct sequence spread spectrum receiver, said receiver having a physical layer associated with the receiving of RF signals and a media access control (MAC) layer associated with the using of data within said RF signals, said physical layer comprising a single device having:

an analog receiver for receiving a spread spectrum modulated signal having a header portion and a data portion;

an analog-to-digital converter operable on said modulated signal;

a digital demodulator for binary phase shift keyed (BPSK) demodulation of said header portion and quaternary phase shift keyed (QPSK) demodulation of said data portion;

a timer for transitioning between the BPSK demodulation and the QPSK demodulation; and,

an interface for providing the demodulated data signal to said MAC layer.

18. The receiver of claim **17** wherein the single device transmits the data from said physical layer to said MAC layer in a serial data stream.

19. The receiver of claim **18** wherein the single device is a single monolithic device.

20. The receiver of claim **17** wherein the data is modulated within the signals by both PN and phase shift keyed modulation.

* * * * *

EXHIBIT H

US006977944B2

(12) **United States Patent**
Brockmann et al.

(10) **Patent No.: US 6,977,944 B2**
(45) **Date of Patent: Dec. 20, 2005**

(54) **TRANSMISSION PROTECTION FOR COMMUNICATIONS NETWORKS HAVING STATIONS OPERATING WITH DIFFERENT MODULATION FORMATS**

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(52) **U.S. Cl.** **370/461**; 370/445
(58) **Field of Search** 370/431, 433, 370/437, 445, 450, 456, 461, 462, 464, 471, 370/483, 487, 341, 329, 322, 348, 349, 373, 370/377, 384, 389, 392, 439, 443, 447, 454, 370/203, 310, 235, 229, 236, 455, 459

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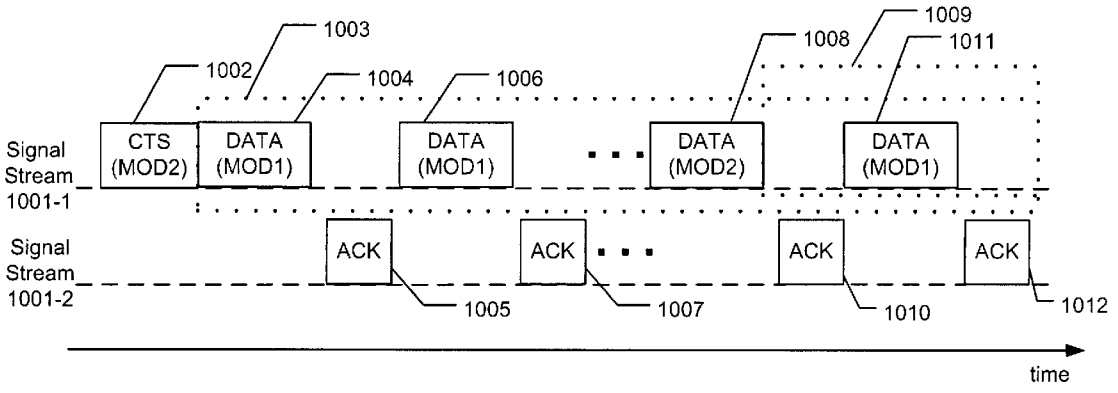
Primary Examiner—Brenda Pham
(74) *Attorney, Agent, or Firm*—Thomas, Kayden, Horstemeyer & Risley, LLP

(57) **ABSTRACT**

A technique to allow enhanced stations and legacy stations to work with each other without the inefficiencies of signaling overhead in the prior art is disclosed. An enhanced station transmits an initial, short frame using a modulation compatible with legacy stations. The frame sets the duration for a frame exchange—consisting of a data frame, followed by acknowledgement frame—in which the data frame is transmitted using an enhanced modulation format. The duration specified in the transmitted initial frame covers the time interval of the subsequent frame exchange. All stations, including legacy stations, listen in on the frame exchange and refrain subsequently from transmitting spontaneously for the time interval covered by the duration. Alternatively, the frame exchange can comprise multiple data frames with corresponding acknowledgement frames. The enhanced station can also transmit, during the remaining frame exchange, one or more intermediate frames that indicate duration.

24 Claims, 11 Drawing Sheets



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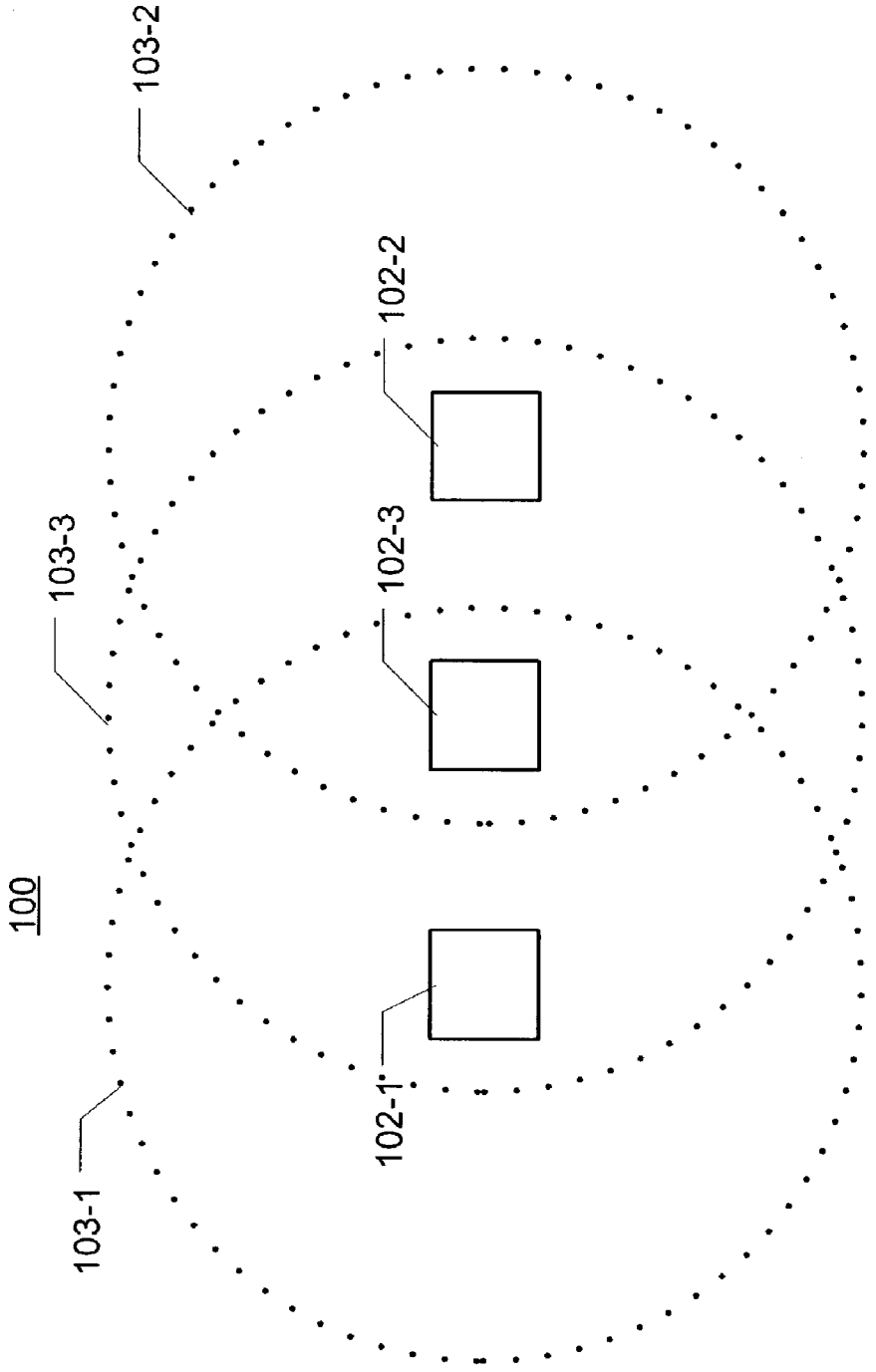


FIG. 1 (Prior Art)

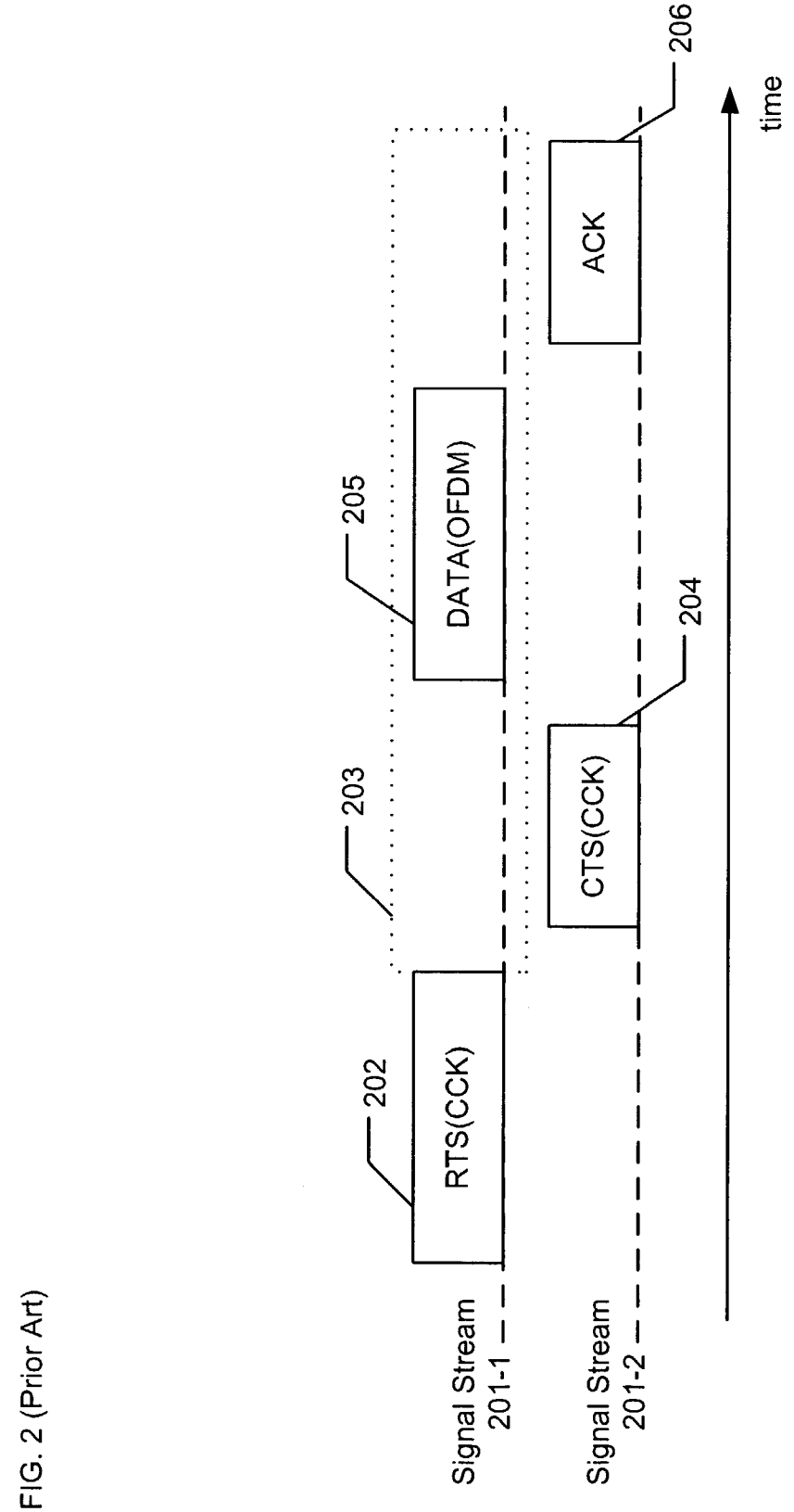


FIG. 2 (Prior Art)

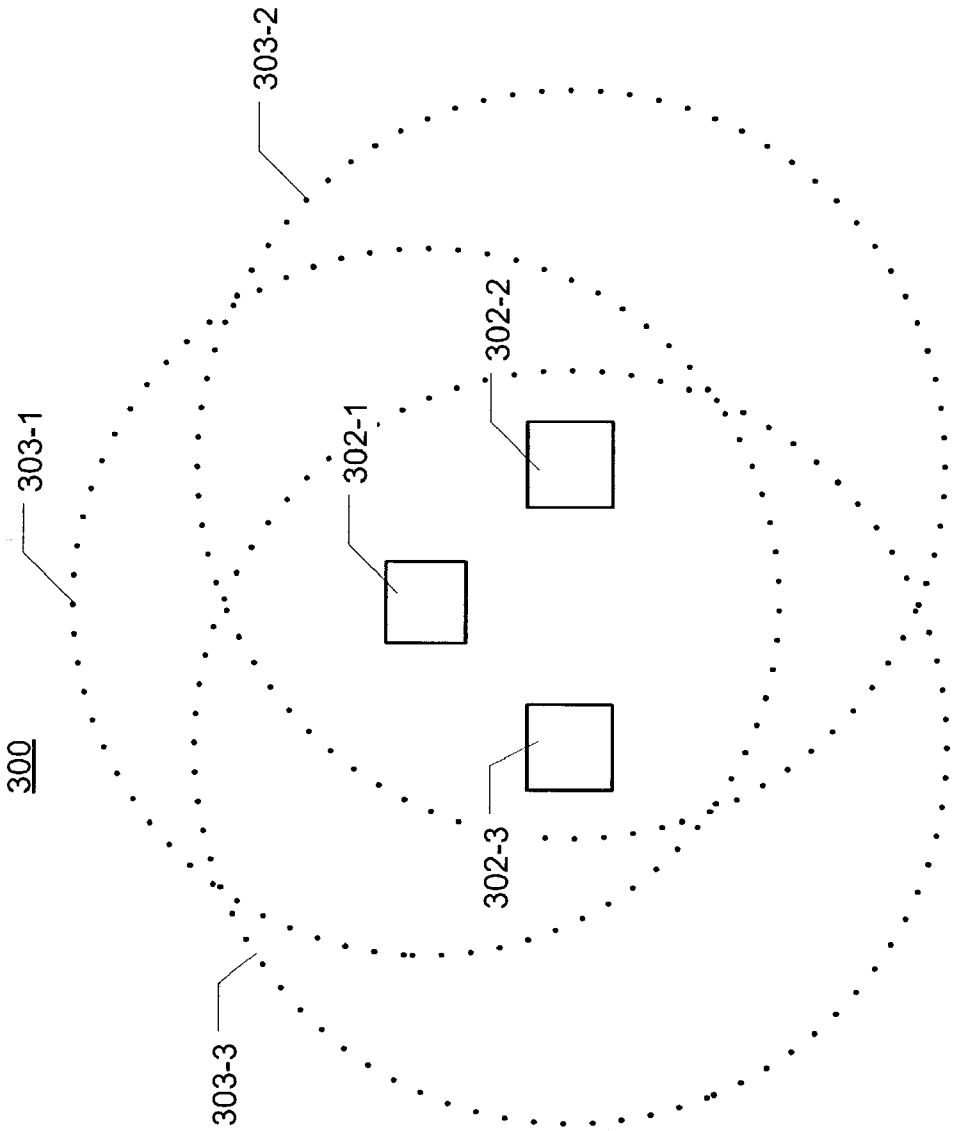


FIG. 3 (Prior Art)

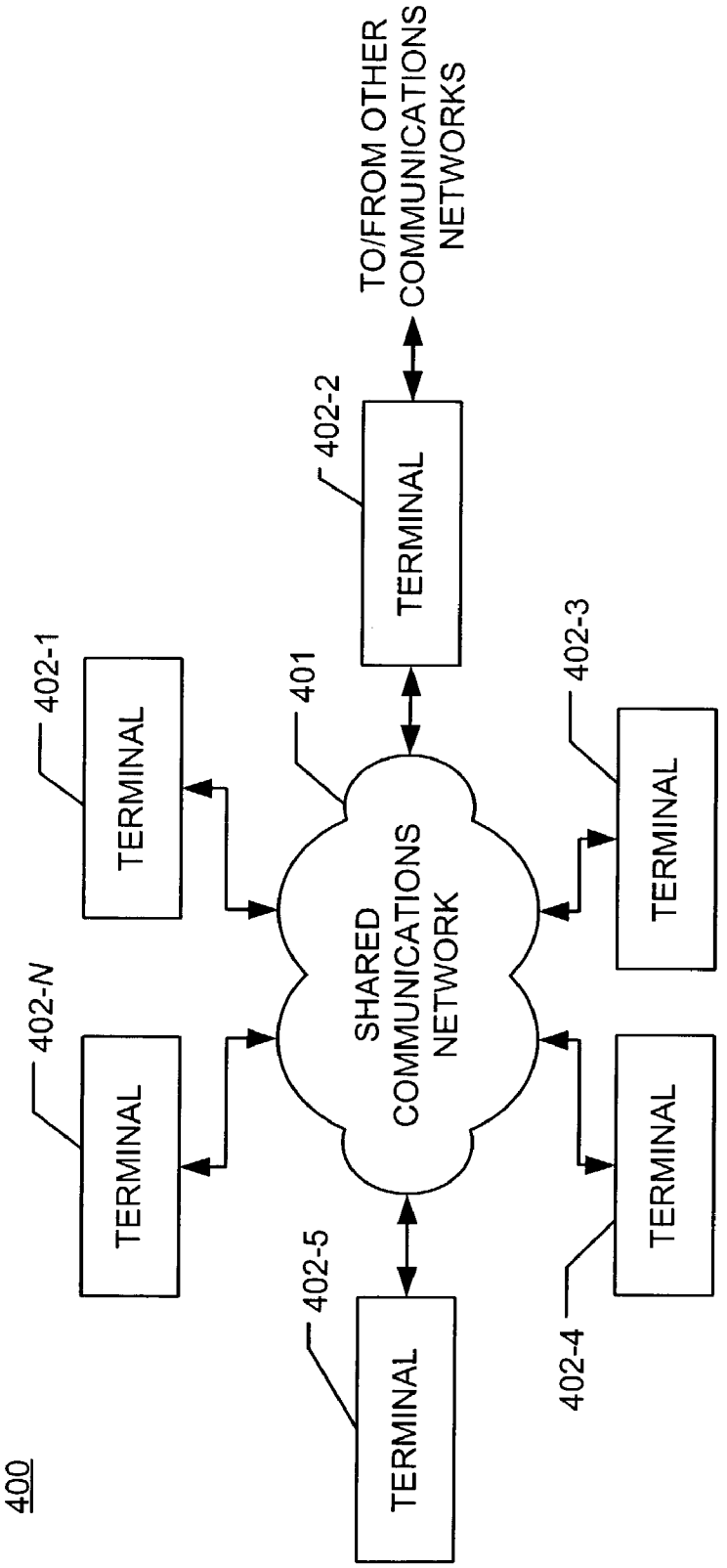

400
SHARED COMMUNICATIONS NETWORK
401
TO/FROM OTHER COMMUNICATIONS NETWORKS
TERMINAL
402-1
402-2
402-3
402-4
402-5
402-N

FIG. 4

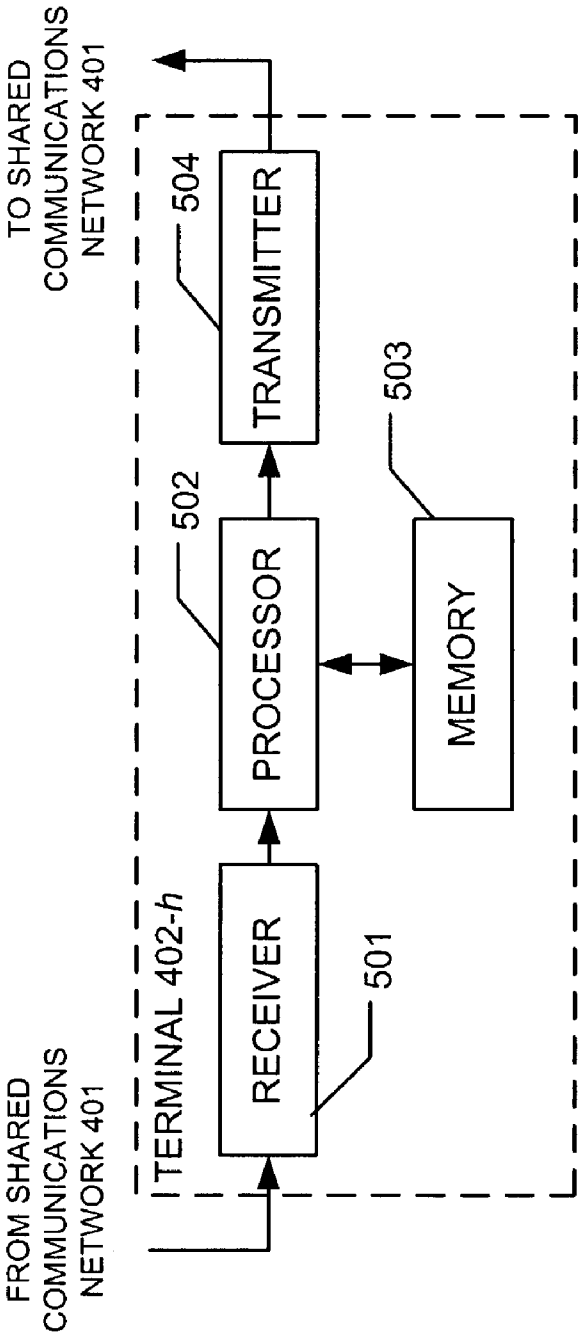

TO SHARED COMMUNICATIONS NETWORK 401
504
TRANSMITTER
503
502
PROCESSOR
MEMORY
TERMINAL 402-h
RECEIVER
501
FROM SHARED COMMUNICATIONS NETWORK 401

FIG. 5

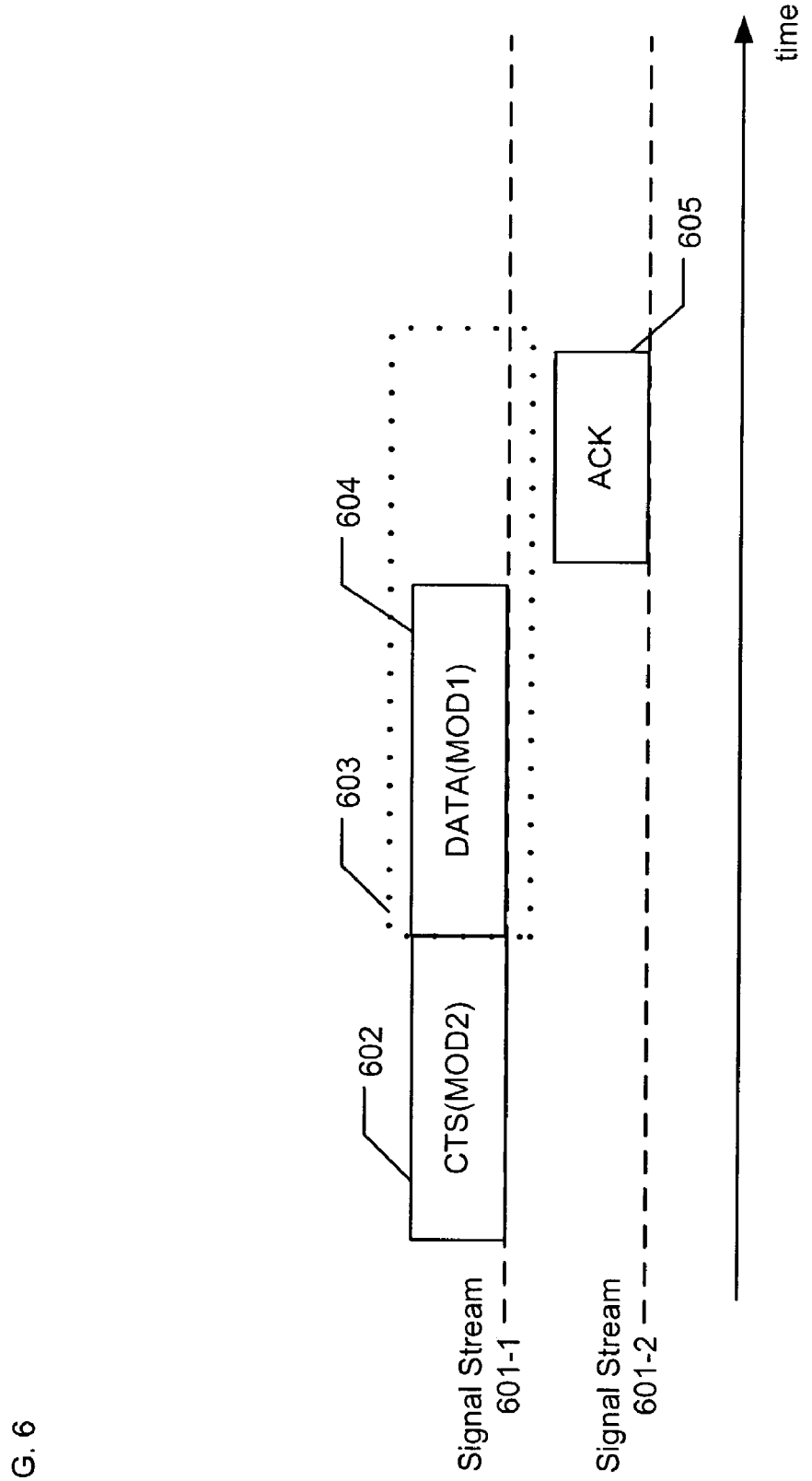
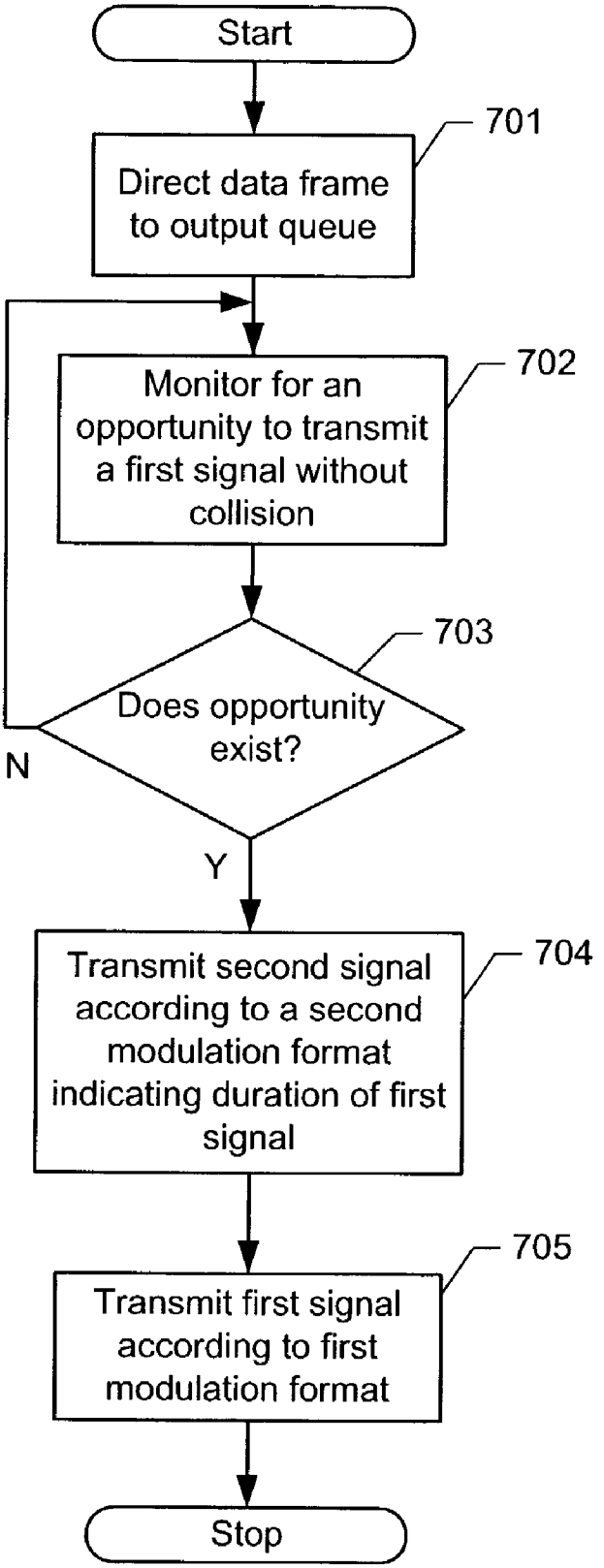

time
605
ACK
604
603
DATA(MOD1)
602
CTS(MOD2)
Signal Stream
601-1
Signal Stream
601-2

FIG. 6

FIG.7


Start
701
Direct data frame to output queue
702
Monitor for an opportunity to transmit a first signal without collision
703
Does opportunity exist?
N
Y
704
Transmit second signal according to a second modulation format indicating duration of first signal
705
Transmit first signal according to first modulation format
Stop

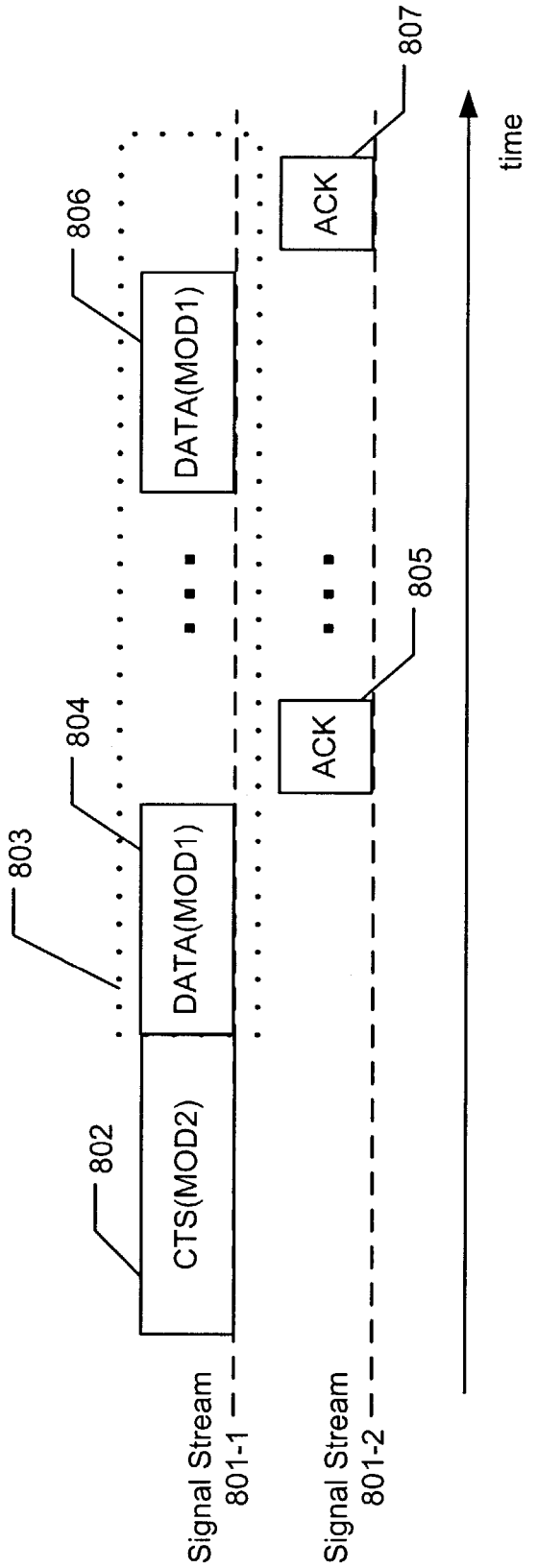

807
806
805
804
803
802
ACK
DATA(MOD1)
ACK
DATA(MOD1)
CTS(MOD2)
time
Signal Stream
801-1
Signal Stream
801-2

FIG. 8

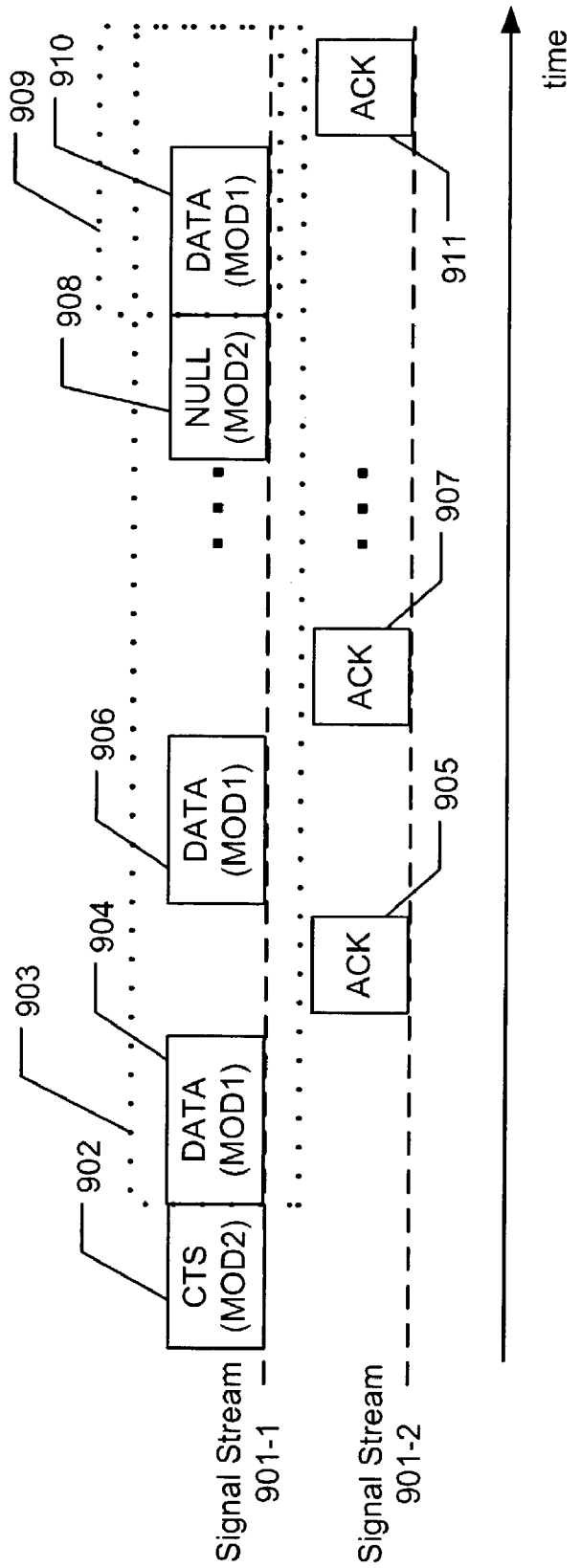

time
Signal Stream 901-1
Signal Stream 901-2
CTS (MOD2)
DATA (MOD1)
NULL (MOD2)
DATA (MOD1)
DATA (MOD1)
ACK
ACK
ACK
902
903
904
905
906
907
908
909
910
911

FIG. 9

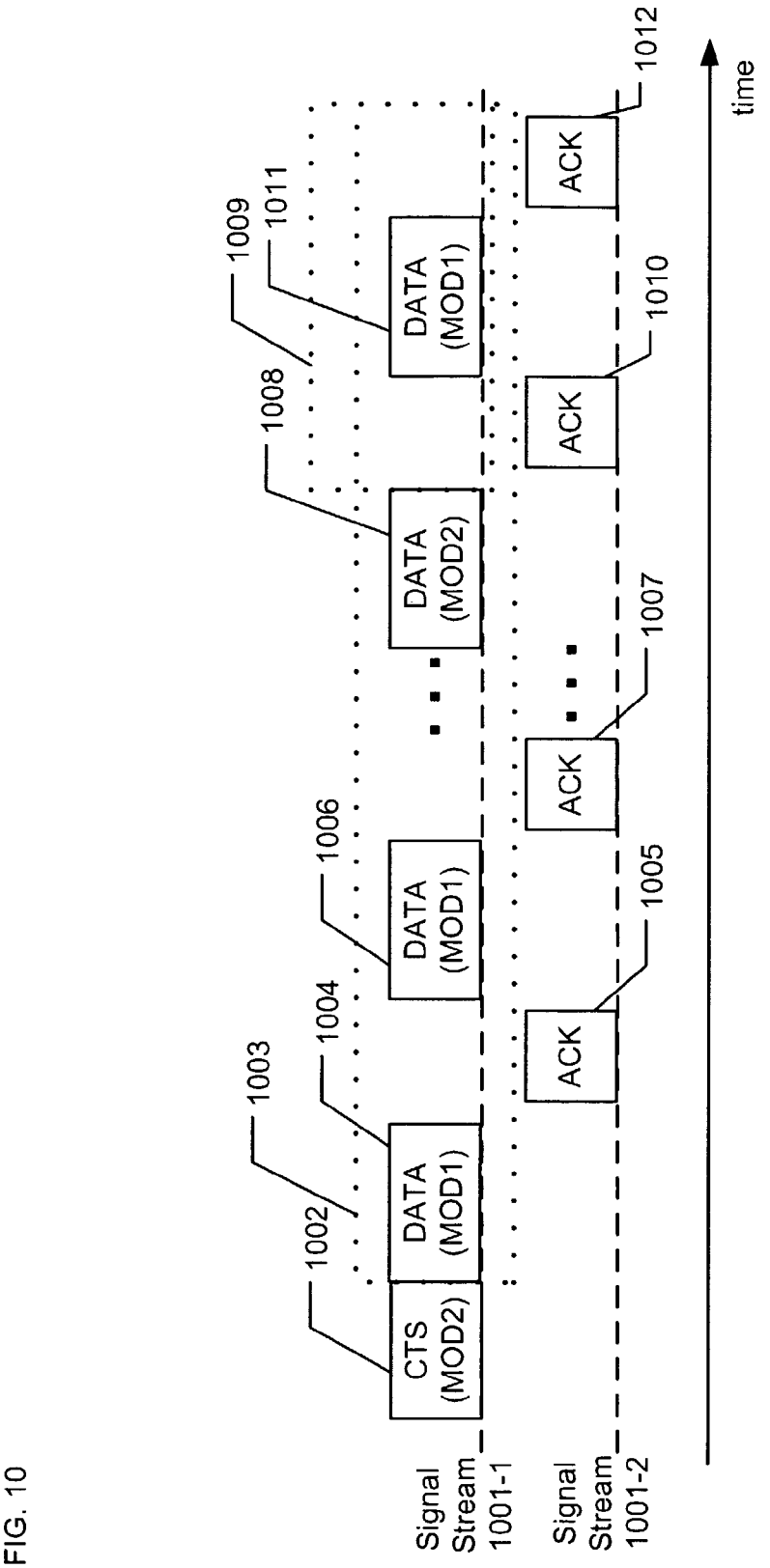
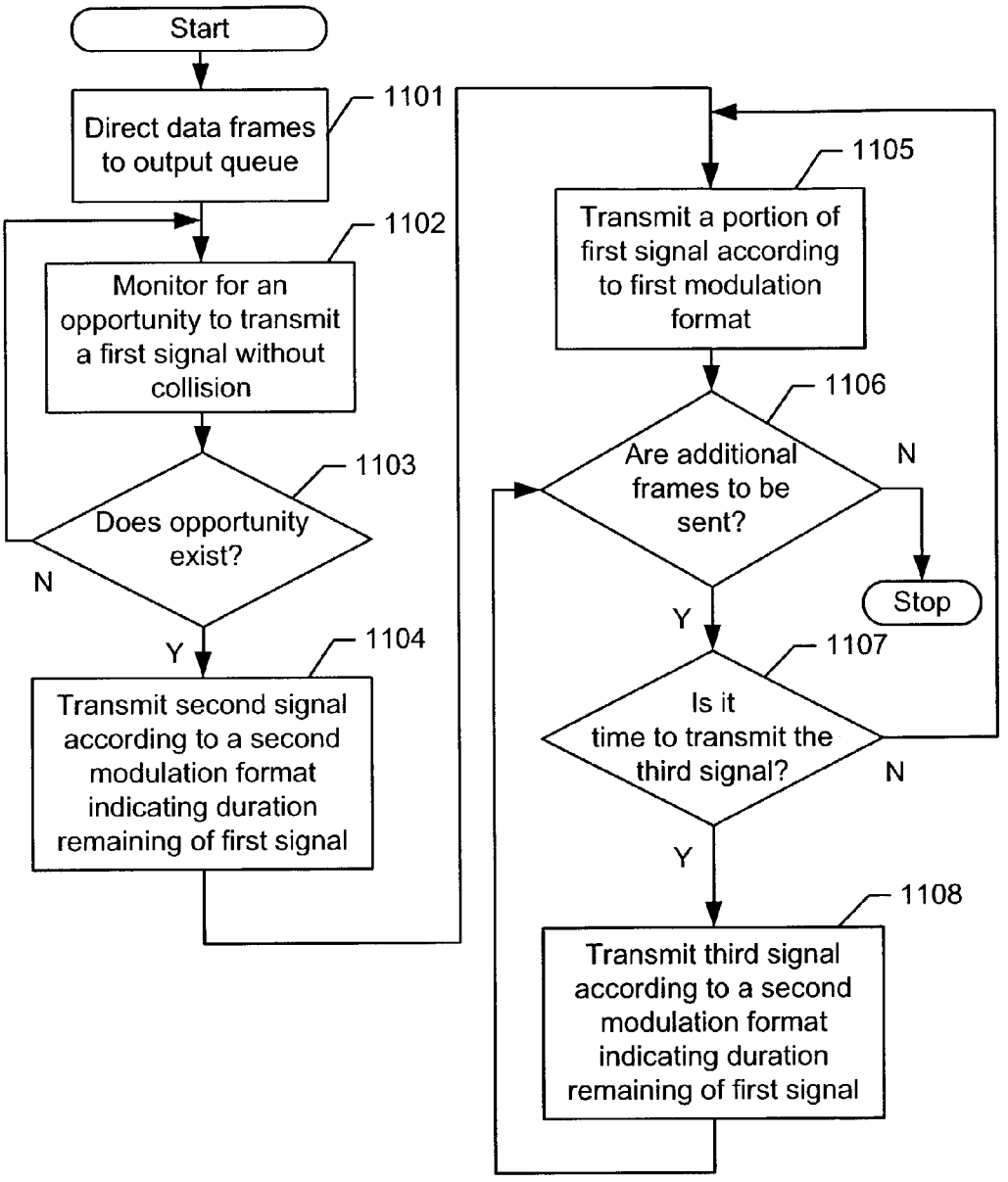

time
Signal Stream 1001-1
Signal Stream 1001-2
CTS (MOD2)
DATA (MOD1)
DATA (MOD2)
ACK
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012

FIG. 10

FIG.11


Start
Direct data frames to output queue
1101
Monitor for an opportunity to transmit a first signal without collision
1102
Does opportunity exist?
1103
N
Y
Transmit second signal according to a second modulation format indicating duration remaining of first signal
1104
Transmit a portion of first signal according to first modulation format
1105
Are additional frames to be sent?
1106
N
Y
Stop
Is it time to transmit the third signal?
1107
N
Y
Transmit third signal according to a second modulation format indicating duration remaining of first signal
1108

TRANSMISSION PROTECTION FOR COMMUNICATIONS NETWORKS HAVING STATIONS OPERATING WITH DIFFERENT MODULATION FORMATS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application Ser. No.: 60/347,412, entitled "Transmission Protection For Wireless LAN Stations Operating With Different Modulation Formats," filed on Jan. 12, 2002 and incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to communications protocols in general, and, more particularly, to techniques for reducing the likelihood of collisions between data packets in wireless communications channels.

BACKGROUND OF THE INVENTION

The IEEE 802.11 set of protocols includes 802.11(b) and 802.11(a). Also known as 802.11 High Rate or Wi-Fi (i.e., "wireless fidelity"), the 802.11(b) approach was approved by the IEEE in 1999 and is currently the mainstream technology adopted by wireless device manufacturers. Essentially using a Direct-Sequence Spread Spectrum (DSSS) technique, 802.11(b) uses a modulation scheme known as Complementary Code Keying (CCK) to transmit data signals at 11 megabits per second (Mbps) over an unlicensed portion of the radio frequency spectrum at around 2.4 GHz. IEEE 802.11(b) enabled a new generation of products to communicate wirelessly with an Ethernet-like connection. Unfortunately, however, the speed of 802.11(b) is only one-tenth that of its wired counterpart, IEEE 802.3.

The IEEE 802.11(a) standard was approved concurrently with 802.11(b), but utilizes Orthogonal Frequency Division Multiplexing (OFDM) as the modulation technique for signal transmission. OFDM is not compatible with 802.11 (b) devices because they use CCK modulation. IEEE 802.11 (a) technology can transmit data signals at up to 54 Mbps and operates in the 5 GHz frequency spectrum.

It would be desirable to extend the benefits of higher bit rate OFDM transmission to the 2.4 GHz band, which, between the two modulations, is the exclusive domain of the CCK scheme of 802.11(b). The IEEE 802.11(g) standard attempts to merge these operational characteristics together. IEEE 802.11(g) OFDM transmissions, however, are hidden from the legacy 802.11(b) nodes, because the 802.11(b) "physical carrier sense mechanism," explained shortly, does not detect the OFDM carrier.

In the prior art, 802.11(g) nodes can fall back to the "virtual carrier sense mechanism" to protect OFDM transmissions from colliding (i.e., experiencing collisions) with transmissions using other modulations. The 802.11 medium access control (MAC) is based around a collision avoidance mechanism, meaning that nodes defer to an active transmission because they see that the shared channel (or "medium") is busy. Their clear channel assessment is a mechanism that senses a physical carrier on the medium.

Furthermore, the MAC protocol defines a virtual carrier sense mechanism, in addition to the traditional physical carrier sense mechanism. To implement the virtual carrier sense mechanism, each node maintains a network allocation vector (NAV) counter that indicates whether the medium must be considered busy or not. After each frame reception at a node (whether the frame has been directed to the node or not), the node initializes its NAV counter with a duration value that is obtained from the duration field in the frame header of the received frame. Over time, this duration value decrements down until it reaches zero, indicating that it is presumptively safe to transmit. Conversely, a non-zero NAV value indicates that the virtual carrier sense (and the share channel) is busy.

An acknowledgement (ACK) frame acknowledges receipt of each transmitted data frame. The ACK frame is NAV protected by the preceding data frame, in which the duration field in the data frame specifies a duration value that reserves the medium until the end of the ACK transmission. Alternatively, the first frame transmitted in a signal stream can carry a value in the duration field that covers the entire remaining frames exchanged, possibly comprising multiple data frames and ACK frames. In other words, the duration value covers the subsequent frame exchange, in which each frame exchange is typically one or more pairs of a data frame responded to with an ACK frame.

The virtual carrier sense mechanism, a familiar part of the 802.11 standard, has been previously used to solve a different problem unique to wireless networks. First and second nodes can potentially be separated by a distance greater than their respectively transmitted signals (carriers) can reach, while an intermediate third node can be close enough to each of the first and second nodes to hear both signals.

FIG. **1** depicts telecommunications system **100** of the prior art, comprising nodes **102-1**, **102-2**, and **102-3**. Rings **103-1**, **103-2**, and **103-3** represent the respective limits of signal coverage for nodes **102-1**, **102-2**, and **102-3**. As depicted, ring **103-1** does not encompass node **102-2**, and ring **103-2** does not encompass node **102-1**, meaning that the signals from each of the two nodes does not reach the other node. In the example, the intermediate third node (i.e., node **102-3**) is already receiving from the first node (i.e., node **102-1**), and the second node (i.e., node **102-2**) has data packets to transmit. The situation can arise that the second node will not defer its transmission, but instead will also try to transmit and, in the process, potentially corrupt the active transmission from the first node. In the example, nodes **102-1** and **102-2** are essentially hidden from each other.

If a hidden node case is suspected, then 802.11 nodes can invoke an RTS/CTS mechanism of the prior art before any data transmission, depicted in FIG. **2**. This means that prior to sending a data frame, a node transmits, as part of its signal stream **201-1**, Request to Send (RTS) frame **202**, which contains a duration value that covers interval **203** needed for the pending data transmission, including data frame **205** and ACK frame **206**. RTS frame **202** will set the NAV locally around the sender using this duration value. If the medium is free around the receiver, it responds, as part of its signal stream **201-2**, with Clear to Send (CTS) frame **204**, which sets the NAV for all other nodes in the vicinity of the receiver. After the RTS/CTS exchange, other nodes in the areas around the sending and receiving nodes defer their transmission through the virtual carrier sense mechanism.

Although the RTS/CTS mechanism provides interoperability with legacy stations, it is suboptimal because it requires the transmission of two CCK frames (RTS and CTS) prior to the OFDM transmission. The RTS/CTS mechanism is targeted specifically at hidden node situations, in which the area at both the sender and the receiver must be NAV protected, each by a different frame. NAV protection, however, does not necessarily have to be imposed in all

OFDM transmissions, especially where it is known that no hidden nodes exist, as shown in the configuration of FIG. **3**.

Telecommunications system **300** of the prior art comprises nodes **302-1**, **302-2**, and **302-3**, each with a limit of signal coverage represented by rings **303-1**, **303-2**, and **303-3**, respectively. Note that all three nodes are in each of the three areas of signal coverage, signifying that no hidden nodes exist in the configuration. In such a situation where no hidden nodes exist—a property that can be readily determined—it is disadvantageous to use the additional overhead of the RTS/CTS mechanism.

The need exists for a technique to allow enhanced stations and legacy stations to work with each other without the inefficiencies of signaling overhead in the prior art.

SUMMARY OF THE INVENTION

The present invention provides a technique to allow enhanced stations and legacy stations to work with each other without the inefficiencies of signaling overhead in the prior art.

In accordance with the illustrative embodiment of the present invention, an enhanced station transmits an initial, short frame using a modulation compatible with legacy stations. The frame sets the duration for a frame exchange—consisting of a data frame, followed by acknowledgement frame—in which the data frame is transmitted using an enhanced modulation format. The duration specified in the transmitted initial frame covers the time interval of the subsequent frame exchange. All stations, including legacy stations, listen in on the frame exchange and refrain subsequently from transmitting spontaneously for the time interval covered by the duration. This protects the frame exchange, even where legacy stations are incapable of listening in on the enhanced modulation. Alternatively, the frame exchange can comprise multiple data frames with corresponding acknowledgement frames.

An additional means of providing protection of the frame exchange, in accordance with another illustrative embodiment of the present invention, is by the enhanced station transmitting, during the remaining frame exchange, one or more intermediate frames that indicate duration. The enhanced station transmits the intermediate protection frame or frames using the legacy-compatible modulation. In accordance with a variation of the illustrative embodiment, each intermediate frame can also carry actual data.

The illustrative embodiment of the present invention comprises: directing to an output queue at a station a data frame to be transmitted over a shared communications network; monitoring at the station for an opportunity to transmit a first signal without colliding with signals present on the shared communications network wherein the first signal, when transmitted, is modulated according to a first modulation format and conveys the data frame; and responsive to identifying an opportunity to transmit without colliding with signals present on the shared communications network, transmitting during the opportunity a second signal modulated according to a second modulation format prior to transmitting the first signal, wherein the second signal indicates the duration of the frame exchange of the first signal and corresponding acknowledgement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** depicts a schematic diagram of the respective coverage areas of three communication nodes, hidden nodes present, in the prior art.

FIG. **2** depicts a message flow diagram of transmissions between two communication nodes in the prior art.

FIG. **3** depicts a schematic diagram of the respective coverage areas of three communication nodes, no hidden nodes present, in the prior art.

FIG. **4** depicts a schematic diagram of the illustrative embodiment of the present invention.

FIG. **5** depicts a block diagram of the salient components of station **402**-x, for x=1 through N, in accordance with the illustrative embodiment of the present invention.

FIG. **6** depicts a message flow diagram of the first variation of the first embodiment of the present invention.

FIG. **7** depicts a flowchart of the tasks performed by an enhanced station in transmitting a frame in the first embodiment of the present invention.

FIG. **8** depicts a message flow diagram of the second variation of the first embodiment of the present invention.

FIG. **9** depicts a message flow diagram of the first variation of the second embodiment of the present invention.

FIG. **10** depicts a message flow diagram of the second variation of the second embodiment of the present invention.

FIG. **11** depicts a flowchart of the tasks performed by an enhanced station in transmitting a frame in the second embodiment of the present invention.

DETAILED DESCRIPTION

FIG. **4** depicts a schematic diagram of the illustrative embodiment of the present invention, telecommunications system **400**, which transmits signals between stations (i.e., nodes) **402-1** through **402**-N, wherein N is a positive integer, over shared communications network **401**. Each of stations **402-1** through **402**-N can be a stationary, portable, or mobile type with different types in the mix.

In accordance with the illustrative embodiment, telecommunications system **400** is a packet-switched network, in contrast to a circuit-switched network, as is well known to those skilled in the art. In other words, a macro data structure (e.g., a text file, a portion of a voice conversation, etc.) of indefinite size is not necessarily transmitted across shared communications network **401** intact, but rather might be transmitted in small pieces.

Each of these small pieces is encapsulated into a data structure called a "data frame," and each data frame traverses shared communications network **401** independently of the other data frames. The intended receiver of the macro data structure collects all of the data frames as they are received, recovers the small pieces of data from each, and reassembles them into the macro data structure. This process is described in more detail below.

Shared communications network **401** can be a wireless or wireline or hybrid wireless and wireline network. A salient characteristic of shared communications network **401** is that every data frame transmitted on shared communications network **401** by any station is received or "seen" by every station on shared communications network **401**, regardless of whether the data frame was intended for it or not. In other words, shared communications network **401** is effectively a broadcast medium.

If shared communications network **401** is wireless, in whole or in part, embodiments of the present invention can use a variety of radio or optical frequencies and transmission methods. Possible radio frequency spectrum, if used, includes the Industrial, Scientific, and Medical (ISM) frequency band in the range of 2.4 GHz. Shared communications network **401** could be a wireless local area network.

It will be clear to those skilled in the art how to make and use shared communications network **401**. It will also be clear to those skilled in the art that the shared communications network depicted in FIG. **4** is illustrative only and that other types of communications networks are within the scope of the present invention.

Stations **402-1** through **402**-N receive or generate the macro data structure and prepare it for transmission over shared communications network **401**. The macro data structure can represent, for example, telemetry, text, audio, video, etc. Alternatively, one or more of stations **402-1** through **402**-N (e.g., station **402-2**, etc.) can function as gateways between shared communications network **401** and other communications networks. In functioning as a gateway, a station receives the macro data structure from another communications network.

FIG. **5** depicts a block diagram of the salient components of station **402**-x, for x=1 through N, in accordance with the illustrative embodiment of the present invention. Receiver **501** comprises the wireless or wireline or hybrid wireless and wireline interface circuitry that enables station **402**-x to receive data frames from communications network **401**. When receiver **501** receives a data frame from shared communications network **401**, it passes the data frame to processor **502** for processing. It will be clear to those skilled in the art how to make and use receiver **501**.

Processor **502** is a general-purpose or special-purpose processor that is capable of performing the functionality described below and with respect to FIG. **6** through **10**. In particular, processor **502** is capable of storing data into memory **503**, retrieving data from memory **503**, and of executing programs stored in memory **503**. Memory **503** accommodates input queues and output queues for incoming data and outgoing messages (including data frames), respectively. It will be clear to those skilled in the art how to make and use processor **502** and memory **503**.

Transmitter **504** comprises the wireless or wireline or hybrid wireless and wireline interface circuitry that enables station **502**-x to transmit data frames onto shared communications network **401**. It will be clear to those skilled in the art how to make and use transmitter **504**.

In accordance with the illustrative embodiment of the present invention, not all of stations **402-1** through **402**-N are of identical capability. Situations involving stations with heterogeneous capabilities can occur, for example, where modern stations are added to a telecommunication system that comprises only legacy stations. Additionally, the situation can result where some, but not all, of the stations in a telecommunications system are upgraded with additional capabilities. Whatever the reason, it will be clear to those skilled in the art why telecommunications systems exist that comprise stations with heterogeneous capabilities.

In accordance with the illustrative embodiment of the present invention, some of stations **402-1** through **402**-N are capable of transmission using an older modulation format, but not a newer modulation format. For the purposes of this specification, these stations are hereinafter called "legacy stations." The example of a legacy station in the illustrative embodiment is an 802.11(b)-capable station using CCK modulation only. In contrast, others of stations **402-1** through **402**-N are capable of transmission using the newer modulation format, in addition to the older modulation format. For the purposes of this specification, these stations are hereinafter called "upgraded stations." The example of a legacy station in the illustrative embodiment is an 802.11 (g)-capable station using both OFDM modulation and CCK modulation. In accordance with the illustrative embodiment of the present invention, legacy stations and upgraded stations are capable of communicating with each other because the upgraded stations transmit data frames that are intended for legacy stations in the modulation format that is used by the legacy stations.

FIG. **6** depicts a message flow diagram of the first variation of the first illustrative embodiment of the present invention. Signal stream **601-1** represents the sequence of messages transmitted by a first station on shared communications network **401**, in which at least some of the messages are intended for a second station. Signal stream **601-2** represents the sequence of messages transmitted by the second station on shared communications network **401**, in which at least some of the messages are intended for the first station. Both stations are of the upgraded type.

Prior to sending a data frame, the first station transmits, as part of its signal stream **601-1**, a frame indicating clear to send, CTS frame **602**. CTS frame **602** contains a duration field with a value that covers time interval **603** associated with the frame exchange of pending data transmission and corresponding acknowledgement. Time interval **603** comprises the transmission times for data frame **604** and ACK frame **605**. The value of the duration field representing time interval **603** can be calculated, for example, by adding up the anticipated transmission times of the relevant signals to be subsequently transmitted. The value can be determined empirically, it can be estimated, or it can be determined in another way. It can comprise a margin of variation in transmission, or it can comprise no extra margin. It will be clear to those skilled in the art how to calculate and set the value of the duration field in CTS frame **602**.

It will be clear to those skilled in the art that a different frame can be used in place of CTS frame **602**, such as a null frame, a data frame with an empty payload, etc., to achieve the same purpose of indicating duration.

As part of the illustrative embodiment, although the first station is capable of transmitting in an enhanced first modulation format (i.e., "MOD1"), the first station transmits CTS frame **602** using a legacy-compatible second modulation format (i.e., "MOD2"). This allows legacy stations to listen in and set their NAV counters to the value of the transmitted duration field in CTS frame **602**, causing those stations to refrain from transmitting spontaneously during the duration of the frame exchange. An example of the first modulation format is orthogonal frequency division multiplexing (OFDM). An example of the second modulation format is complementary code keying (CCK). As part of the illustrative embodiment, the first station transmits CTS frame **602** (or equivalent) to itself, consequently not requiring a second station to respond. Furthermore, the first station does not have to acknowledge CTS frame **602**, since the node sent the frame to itself, minimizing message overhead.

The first station then immediately transmits data frame **604** using the enhanced first modulation format. The second station, upon receiving data frame **604**, responds by transmitting ACK frame **605**. ACK frame **605** can be sent using either the first modulation format or second modulation format, since the first station can understand either format. If ACK frame **605** is sent in the legacy second modulation format, then additional protection is added against legacy stations newly arriving into shared communications network **401** that were previously unavailable to set their NAV counters. Both data frame **604** and ACK frame **605** are protected by the NAV counter running in nearby legacy stations.

Throughout the time interval occupied by signal streams **601-1** and **601-2**, other stations present on shared communications network **401**, comprising legacy stations (if present) and other enhanced stations (if present), are presumably monitoring for an opportunity to transmit signals without colliding with signals already present. The legacy stations sense shared communications network **401** for signals modulated according to the second modulation format. The stations refrain from transmitting spontaneously if a signal is present. Furthermore, the stations refrain from transmitting during the time interval specified by the value in the transmitted duration field.

It will be clear to those skilled in the art how to format, encode, transmit, receive, and decode CTS frame **602** (or equivalent, as discussed), data frame **604**, and ACK frame **605**.

FIG. **7** depicts a flowchart of the tasks constituting the first illustrative embodiment and performed by an upgraded station in queuing and transmitting a data frame in the presence of legacy stations on shared communications network **401**. It will be clear to those skilled in the art which of the tasks depicted in FIG. **7** can be performed simultaneously or in a different order than that depicted.

At task **701**, the upgraded station directs a formed data frame to an output queue. It will be clear to those skilled in the art how to form the data frame and how to make and use the output queue.

At task **702**, the upgraded station monitors for an opportunity to transmit a first signal that conveys the queued data frame, without collision and by using a first modulation format. The first modulation format can be, for example, the OFDM format existing within an 802.11(g)-based wireless local area network. It will be clear to those skilled in the art how to recognize when it is improper to transmit and how to recognize when it is appropriate to transmit. If it is determined at task **703** that an opportunity exists, control proceeds to task **704**.

At task **704**, the upgraded station transmits onto shared communications network **401** a second signal that is modulated according to a second modulation format. As part of the illustrative embodiment, the second modulation format is the legacy format understood by all the stations. For example, this can be CCK format, as opposed to the enhanced OFDM format also existing within an 802.11(g)-based wireless local area network. As part of the illustrative embodiment, the information conveyed by the second signal indicates the allotted duration of subsequently transmitted signals, in this case, the first signal transmitted by the transmitting station and the corresponding acknowledgement from the receiving station. The value of the duration field can be calculated, for example, by adding up the anticipated transmission times of the relevant signals to be subsequently transmitted. The value can be determined empirically, it can be estimated, or it can be determined in another way. It can comprise a margin of variation in transmission, or it can comprise no extra margin. It will be clear to those skilled in the art how to calculate and set the duration.

The second signal (e.g., conveying a clear to send indication, etc.) is transmitted by the transmitting station to itself (e.g., by the station specifying its own address as the destination, etc.). It will be clear to those skilled in the art how a station can transmit a signal to itself.

At task **705**, the upgraded station transmits onto shared communications network **401** the first signal. The first signal can convey a data frame or it can convey other information. The upgraded station transmits the first signal (and can receive a signal indicating an acknowledgement) while under NAV protection as specified in the duration field sent previously in the second signal.

It will be clear to those skilled in the art how to perform each of tasks **701** through **705**.

FIG. **8** depicts a message flow diagram of the second variation of the first illustrative embodiment of the present invention. Signal stream **801-1** represents the sequence of messages transmitted by a first station on shared communications network **401**, in which at least some of the messages are intended for a second station. Signal stream **801-2** represents the sequence of messages transmitted by the second station on shared communications network **401**, in which at least some of the messages are intended for the first station. Both stations are of the upgraded type.

Prior to sending a data frame, the first station transmits, as part of its signal stream **801-1**, a frame indicating clear to send, CTS frame **802**, which contains a duration field with a value that covers time interval **803** associated with the frame exchange of pending data transmissions and acknowledgements. Time interval **803** comprises the transmission times for multiple data frames (e.g., data frames **804** and **806**, etc.) and corresponding ACK frames (e.g., ACK frames **805** and **806**, etc.). The value of the duration field representing time interval **803** can be calculated, for example, by adding up the anticipated transmission times of the relevant signals to be subsequently transmitted. The value can be determined empirically, it can be estimated, or it can be determined in another way. It can comprise a margin of variation in transmission, or it can comprise no extra margin. It will be clear to those skilled in the art how to calculate and set the value of the duration field in CTS frame **802**.

It will be clear to those skilled in the art that a different frame can be used in place of CTS frame **802**, such as a null frame, a data frame with an empty payload, etc., to achieve the same purpose of indicating duration. As part of the illustrative embodiment, although the first station is capable of transmitting in an enhanced first modulation format (i.e., "MOD1"), the first station transmits CTS frame **802** in similar fashion as is CTS frame **602** and for similar reasons.

The first station then immediately transmits first data frame **804** using the enhanced first modulation format. The second station, upon receiving first data frame **804**, responds by transmitting ACK frame **805**. ACK frame **805** can be sent using either the first modulation format or second modulation format, since the first station can understand either format. If ACK frame **805** is sent in the legacy second modulation format, then additional protection is added against legacy stations newly arriving into shared communications network **401** that were previously unavailable to set their NAV counters. Both first data frame **804** and ACK frame **805** are protected by the NAV counter running in nearby legacy stations.

The first station can then subsequently transmit additional data frames, paired with additional ACK frames sent by the second station. Finally, the first station transmits last data frame **806** using the enhanced first modulation format. The second station, upon receiving last data frame **806**, responds by transmitting ACK frame **807**. ACK frame **807** is sent in similar fashion as ACK frame **805**. Both last data frame **806** and ACK frame **807** are protected by the NAV counter running in nearby legacy stations.

Throughout the time interval occupied by signal streams **801-1** and **801-2**, other stations present on shared communications network **401**, comprising legacy stations (if present) and other enhanced stations (if present), are presumably monitoring for an opportunity to transmit signals

without colliding with signals already present. The legacy stations sense shared communications network **401** for signals modulated according to the second modulation format. The stations refrain from transmitting spontaneously if a signal is present. Furthermore, the stations refrain from transmitting during the time interval specified by the value in the transmitted duration field.

It will be clear to those skilled in the art how to format, encode, transmit, receive, and decode CTS frame **802** (or equivalent, as discussed), first data frame **804**, last data frame **806**, and ACK frames **805** and **807**.

FIG. **9** depicts a message flow diagram of the first variation of the second illustrative embodiment of the present invention. Signal stream **901-1** represents the sequence of messages transmitted by a first station on shared communications network **401**, in which at least some of the messages are intended for a second station. Signal stream **901-2** represents the sequence of messages transmitted by the second station on shared communications network **401**, in which at least some of the messages are intended for the first station. Both stations are of the upgraded type.

Prior to sending a data frame, the first station transmits, as part of its signal stream **901-1**, a frame indicating clear to send, CTS frame **902**. CTS frame **902** contains a duration field with a value that covers time interval **903** associated with the frame exchange of pending data transmissions and acknowledgements. Time interval **903** comprises the transmission times for multiple data frames (e.g., data frames **904**, **906**, and **910**; etc.) and corresponding ACK frames (e.g., ACK frames **905**, **907**, and **911**; etc.). The value of the duration field representing time interval **903** can be calculated, for example, by adding up the anticipated transmission times of the relevant signals to be subsequently transmitted. The value can be determined empirically, it can be estimated, or it can be determined in another way. It can comprise a margin of variation in transmission, or it can comprise no extra margin. It will be clear to those skilled in the art how to calculate and set the value of the duration field in CTS frame **902**.

It will be clear to those skilled in the art that a different frame can be used in place of CTS frame **902**, such as a null frame, a data frame with an empty payload, etc., to achieve the same purpose of indicating duration. As part of the illustrative embodiment, although the first station is capable of transmitting in an enhanced first modulation format (i.e., "MOD1"), the first station transmits CTS frame **902** in similar fashion as CTS frame **602** and for similar reasons.

The first station can then immediately transmit first data frame **904** using the enhanced first modulation format. The second station, upon receiving first data frame **904**, responds by transmitting ACK frame **905**. ACK frame **905** can be sent using either the first modulation format or second modulation format, since the first station can understand either format. If ACK frame **905** is sent in the legacy second modulation format, then additional protection is added against legacy stations newly arriving into shared communications network **401** that were previously unavailable to set their NAV counters. Both first data frame **904** and ACK frame **905** are protected by the NAV counter running in nearby legacy stations.

The first station can then subsequently transmit additional data frames (e.g., data frame **906**, etc.), paired with additional ACK frames (e.g., ACK frame **907**, etc.) sent by the second station.

At some point interposed in the series of data frame transmissions, the first station can choose to transmit an intermediate, reinforcing protection frame. Specifically, the first station transmits, as part of its signal stream **901-1**, null frame **908**, which contains a duration field with a value that covers time interval **909** associated with the frame exchange of pending data transmissions and acknowledgements that remain. Time interval **909** comprises the transmission times for multiple data frames (e.g., data frame **910**, etc.) and corresponding ACK frames (e.g., ACK frame **911**, etc.). It will be clear to those skilled in the art how to calculate and set the value of the duration field in null frame **908**.

It will be clear to those skilled in the art that a different frame can be used in place of null frame **908** to achieve the same purpose of indicating duration. As part of the illustrative embodiment, although the first station is capable of transmitting in an enhanced first modulation format (i.e., "MOD1"), the first station transmits null frame **908** in similar fashion as CTS frame **602** and for similar reasons. The first station can transmit null frame **908** intermittently whenever it is determined to do so. The transmission can be based upon time, new stations arriving into shared communications network **401**, etc. If based upon time, the transmission can be periodic or aperiodic. It will be clear to those skilled in the art how to determine when null frame **908** (or equivalent, as discussed) is transmitted.

The first station transmits data frame **910** using the enhanced first modulation format. The second station, upon receiving data frame **910**, responds by transmitting ACK frame **911**. ACK frame **911** is sent in similar fashion as ACK frame **905**. The NAV counter running in nearby legacy stations protects both data frame **910** and ACK frame **911**, in addition to any additional data frame/ACK frame pairs transmitted during the duration period.

Throughout the time interval occupied by signal streams **901-1** and **901-2**, other stations present on shared communications network **401**, comprising legacy stations (if present) and other enhanced stations (if present), are presumably monitoring for an opportunity to transmit signals without colliding with signals already present. The legacy stations sense shared communications network **401** for signals modulated according to the second modulation format. The stations refrain from transmitting spontaneously if a signal is present. Furthermore, the stations refrain from transmitting during the time interval specified by the value in the transmitted duration field.

It will be clear to those skilled in the art how to format, encode, transmit, receive, and decode CTS frame **902** (or equivalent, as discussed); null frame **908** (or equivalent, as discussed); data frames **904**, **906**, and **910**; and ACK frames **905**, **907**, and **911**. Finally, it will be clear to those skilled in the art that multiple intermediate frames (e.g., null frame **908**, etc.) can be transmitted to reinforce the NAV protection.

FIG. **10** depicts the second variation of the second illustrative of the present invention. Signal stream **1001-1** as transmitted by a first station comprises CTS frame **1002**, and data frames **1004**, **1006**, **1008**, and **1011**. Signal stream **1001** as transmitted by a second station comprises ACK frames **1005**, **1007**, **1010**, and **1012**. The variation depicted is similar to that depicted in FIG. **9**, except that a data frame (i.e., data frame **1008**) is used to reinforce the NAV protection, instead of a null frame.

Specifically, the first station transmits, as part of its signal stream **1001-1** and at an intermediate point, data frame **1008**, which contains a duration field with a value that covers time interval **1009** associated with the frame exchange of pending data transmissions and acknowledgements that remain. Time interval **1009** comprises the transmission times for multiple data frames (e.g., data frame **1011**, etc.) and corresponding

ACK frames (e.g., ACK frames **1010** and **1012**, etc.). It will be clear to those skilled in the art how to calculate and set the value of the duration field in data frame **1008**.

As part of the illustrative embodiment, although the first station is capable of transmitting in an enhanced first modulation format (i.e., "MOD1"), the first station transmits data frame **1008** using a legacy-compatible second modulation format (i.e., "MOD2"). This allows legacy stations to listen in and set their NAV counters to the value of the transmitted duration field in data frame **1008**, causing those stations to refrain from transmitting spontaneously during the duration of the frame exchange. Note that data frame **1008** also contains valid data that had to be transmitted in some data frame.

Throughout the time interval occupied by signal streams **1001-1** and **1001-2**, other stations present on shared communications network **401**, comprising legacy stations (if present) and other enhanced stations (if present), are presumably monitoring for an opportunity to transmit signals without colliding with signals already present. The legacy stations sense shared communications network **401** for signals modulated according to the second modulation format. The stations refrain from transmitting spontaneously if a signal is present. Furthermore, the stations refrain from transmitting during the time interval specified by the value in the transmitted duration field.

It will be clear to those skilled in the art how to format, encode, transmit, receive, and decode CTS frame **1002** (or equivalent, as discussed); data frames **1004**, **1006**, **1008**, and **1011**; and ACK frames **1005**, **1007**, **1010**, and **1012**. Finally, it will be clear to those skilled in the art that multiple intermediate frames (e.g., data frame **1008**, etc.) can be transmitted to reinforce the NAV protection.

FIG. **11** depicts a flowchart of the tasks constituting the second illustrative embodiment and performed by an upgraded station in queuing and transmitting a data frame in the presence of legacy stations on shared communications network **401**. It will be clear to those skilled in the art which of the tasks depicted in FIG. **11** can be performed simultaneously or in a different order than that depicted.

At task **1101**, the upgraded station directs formed data frames to an output queue. It will be clear to those skilled in the art how to form data frames and how to make and use the output queue.

At task **1102**, the upgraded station monitors for an opportunity to transmit a first signal that conveys the queued data frames, without collision and by using a first modulation format. The first modulation format can be, for example, the OFDM format existing within an 802.11(g)-based wireless local area network. It will be clear to those skilled in the art how to recognize when it is improper to transmit and how to recognize when it is appropriate to transmit. If it is determined at task **1103** that an opportunity exists, control proceeds to task **1104**.

At task **1104**, the upgraded station transmits onto shared communications network **401** a second signal that is modulated according to a second modulation format. As part of the illustrative embodiment, the second modulation format is the legacy format understood by all the stations. For example, this can be CCK format, as opposed to the enhanced OFDM format also existing within an 802.11(g)-based wireless local area network. As part of the illustrative embodiment, the information conveyed by the second signal indicates the allotted duration of subsequently transmitted signals, in this case, the first signal comprising a plurality of data frames, the third signal comprising intermediate protection frames, and the corresponding acknowledgements from the receiving station. The value of the duration field can be calculated, for example, by adding up the anticipated transmission times of the relevant signals to be subsequently transmitted. The value can be determined empirically, it can be estimated, or it can be determined in another way. It can comprise a margin of variation in transmission, or it can comprise no extra margin. It will be clear to those skilled in the art how to calculate and set the duration.

The second signal (e.g., conveying a clear to send indication, etc.) is transmitted by the transmitting station to itself (e.g., by the station specifying its own address as the destination, etc.). It will be clear to those skilled in the art how a station can transmit a signal to itself.

At task **1105**, the upgraded station transmits onto shared communications network **401** a portion of the first signal. The portion of the first signal can convey a single data frame or it can convey other information. The upgraded station transmits the portion of the first signal (and can receive a signal indicating an acknowledgement) while under NAV protection as specified in the duration field sent previously in the second signal.

At task **1106**, if additional frames of any kind are to be transmitted, control proceeds to task **1107**. If not, execution of the tasks depicted in FIG. **11** stops.

At task **1107**, if it is time to transmit a third signal, control proceeds to task **1108**. If not, control proceeds to task **1105**.

At task **1108**, the upgraded station transmits onto shared communications network **401** a third signal that is modulated according to the second modulation format, which, as explained earlier, is the legacy format understood by all the stations. For example, this can be CCK format, as opposed to the enhanced OFDM format also existing within an 802.11(g)-based wireless local area network. As part of the illustrative embodiment, the information conveyed by the third signal indicates the allotted duration of subsequently transmitted signals, in this case, the remaining portions of the first signal comprising one or more data frames, any remaining third signals comprising intermediate protection frames, and the corresponding one or more acknowledgements from the receiving station. The duration represented in the third signal can be calculated by adding up the anticipated transmission times of the relevant signals to be subsequently transmitted. It will be clear to those skilled in the art how to calculate and set the duration.

The third signal, if conveying a null frame or similar non-data frame message, is transmitted by the transmitting station to itself (e.g., by the station specifying its own address as the destination, etc.). It will be clear to those skilled in the art how a station can transmit a signal to itself. Alternatively, the third signal can convey a data frame carrying underlying data that would had to have been transmitted to another station, anyway. In this alternative case, the third signal is actually intended for a receiving station, although all stations are able to listen to it (since it is transmitted in the second modulation format) and read the duration field information.

The first station can transmit the third signal intermittently whenever it is determined to do so. The transmission can be based upon time, new stations arriving into shared communications network **401**, etc. If based upon time, the transmission can be periodic or aperiodic. It will be clear to those skilled in the art how to determine when the third signal is transmitted.

It will be clear to those skilled in the art how to perform each of tasks **1101** through **1108**.

It is to be understood that the above-described embodiments are merely illustrative of the present invention and that many variations of the above-described embodiments can be devised by those skilled in the art without departing from the scope of the invention. It is therefore intended that such variations be included within the scope of the following claims and their equivalents.

What is claimed is:

1. A method comprising:

(a) monitoring a shared-communications medium for an opportunity to transmit a first signal and a second signal;

(b) transmitting said second signal in accordance with a second modulation scheme on said shared-communications medium, wherein:

(i) said second signal conveys a frame indicating clear to send that is addressed to the sender of said frame indicating clear to send; and

(ii) said frame indicating clear to send comprises a duration field that has a value based on the expected length of time required to transmit at least one data frame; and

(c) transmitting said first signal in accordance with a first modulation scheme on said shared-communications medium after said second signal, wherein said first signal conveys said at least one data frame;

wherein said frame indicating clear to send and said at least one data frame are addressed to different stations.

2. The method of claim **1**, wherein said second modulation scheme is different than said first modulation scheme.

3. The method of claim **1**, wherein said first modulation scheme comprises orthogonal frequency division multiplexing and said second modulation scheme comprises complementary code keying.

4. The method of claim **1**, wherein said frame indicating clear to send is at least one of a clear-to-send frame and a frame with an empty payload.

5. The method of claim **1**, further comprising transmitting a third signal on said shared-communications medium, wherein said third signal conveys a data frame in accordance with said second modulation scheme.

6. The method of claim **1**, wherein said shared-communications medium is operative in the 2.4 GHz Industrial, Scientific, Medical band of the radio frequency spectrum.

7. A station comprising:

(a) a receiver for monitoring a shared-communications medium for an opportunity to transmit a first signal and a second signal; and

(b) a transmitter for:

(1) transmitting said second signal in accordance with a second modulation scheme on said shared-communications medium, wherein:

(i) said second signal conveys a frame indicating clear to send that is addressed to the sender of said frame indicating clear to send; and

(ii) said frame indicating clear to send comprises a duration field that has a value based on the expected length of time required to transmit at least one data frame; and

(2) transmitting said first signal in accordance with a first modulation scheme on said shared-communications medium after said second signal, wherein said first signal conveys said at least one data frame;

wherein said frame indicating clear to send and said at least one data frame are addressed to different stations.

8. The station of claim **7**, wherein said second modulation scheme is different than said first modulation scheme.

9. The station of claim **7**, wherein said first modulation scheme comprises orthogonal frequency division multiplexing and said second modulation scheme comprises complementary code keying.

10. The station of claim **7**, wherein said frame indicating clear to send is at least one of a clear-to-send frame and a frame with an empty payload.

11. The station of claim **7**, wherein said transmitter also transmits a third signal on said shared-communications medium, conveying a data frame in accordance with said second modulation scheme.

12. The station of claim **7**, wherein said shared-communications medium is operative in the 2.4 GHz Industrial, Scientific, Medical band of the radio frequency spectrum.

13. A method comprising:

(a) monitoring a shared-communications medium for an opportunity to transmit a first signal, a second signal, and a third signal;

(b) transmitting said second signal in accordance with a second modulation scheme on said shared-communications medium, wherein:

(i) said second signal conveys a frame indicating clear to send that is addressed to the sender of said frame indicating clear to send; and

(ii) said frame indicating clear to send comprises a duration field that has a value based on the expected length of time required to transmit at least one data frame;

(c) transmitting said first signal in accordance with a first modulation scheme on said shared-communications medium after said second signal, wherein said first signal conveys said at least one data frame; and

(d) transmitting said third signal in accordance with said second modulation scheme on said shared-communications medium after said first signal, wherein said third signal conveys a data frame;

wherein said frame indicating clear to send and said at least one data frame are addressed to different stations.

14. The method of claim **13**, wherein said second modulation scheme is different than said first modulation scheme.

15. The method of claim **13**, wherein said first modulation scheme comprises orthogonal frequency division multiplexing and said second modulation scheme comprises complementary code keying.

16. The method of claim **13**, wherein said frame indicating clear to send is at least one of a clear-to-send frame and a frame with an empty payload.

17. The method of claim **13**, wherein said frame indicating clear to send and said data frame are addressed to different stations.

18. The method of claim **13**, wherein said shared-communications medium is operative in the 2.4 GHz Industrial, Scientific, Medical band of the radio frequency spectrum.

19. A station comprising:

(a) a receiver for monitoring a shared-communications medium for an opportunity to transmit a first signal, a second signal, and a third signal; and

(b) a transmitter for:

(1) transmitting said second signal in accordance with a second modulation scheme on said shared-communications medium, wherein:

(i) said second signal conveys a frame indicating clear to send that is addressed to the sender of said frame indicating clear to send; and

(ii) said frame indicating clear to send comprises a duration field that has a value based on the expected length of time required to transmit the subsequent data frames conveyed by said first signal and said third signal;

(2) transmitting said first signal in accordance with a first modulation scheme on said shared-communications medium after said second signal, wherein said first signal conveys said at least one data frame; and

(3) transmitting said third signal in accordance with said second modulation scheme on said shared-communications medium after said first signal, wherein said third signal conveys a data frame;

wherein said frame indicating clear to send and said at least one data frame are addressed to different stations.

20. The station of claim **19**, wherein said second modulation scheme is different than said first modulation scheme.

21. The station of claim **19**, wherein said first modulation scheme comprises orthogonal frequency division multiplexing and said second modulation scheme comprises complementary code keying.

22. The station of claim **19**, wherein said frame indicating clear to send is at least one of a clear-to-send frame and a frame with an empty payload.

23. The station of claim **19**, wherein said transmitter also transmits the third signal on said shared-communications medium, conveying a data frame in accordance with said second modulation scheme.

24. The station of claim **19**, wherein said shared-communications medium is operative in the 2.4 GHz Industrial, Scientific, Medical band of the radio frequency spectrum.

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