UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

ZETEC, INC, Plaintiff, v. WESTINGHOUSE ELECTRIC COMPANY LLC, Defendant.	Case No.: **COMPLAINT FOR PATENT INFRINGEMENT** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Zetec, Inc. ("Zetec") hereby sues Westinghouse Electric Company, LLC ("Westinghouse") for willful patent infringement.

NATURE OF ACTION

1. This is an action for patent infringement in violation of the patent laws of the United States, 35 U.S.C. §§ 271, *et seq.*, to enjoin and obtain damages resulting from Westinghouse's willful infringement of U.S. Patent No. 6,734,669 ("the '669 Patent") (Ex. A), U.S. Patent No. 6,798,197 ("the '197 Patent") (Ex. B), and U.S. Patent No. 6,809,671 ("the '671 Patent") (Ex. C).

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2. Zetec seeks injunctive relief to prevent Westinghouse from continuing to infringe the '669, '197, and '671 Patents.

3. In addition, Zetec seeks recovery of monetary damages resulting from Westinghouse's past infringement of the '669, '197 and '671 Patents, including treble damages and attorney fees.

THE PLAINTIFF ZETEC

4. Plaintiff Zetec is a Washington corporation with offices at 8226 Bracken Place SE, Suite 100, Snoqualmie, WA 98065. Zetec is the assignee and owner of the entire right, title, and interest in and to the '669, '197 and '671 Patents.

THE DEFENDANT WESTINGHOUSE

5. Upon information and belief, Defendant Westinghouse is a corporation organized and existing under the laws of Delaware, having its headquarters at 1000 Westinghouse Drive, Cranberry Township, Pennsylvania 16066.

JURISDICTION AND VENUE

6. The claims asserted in this Complaint arise under Patent Laws of the United States, 35 U.S.C. §§ 1–376.

7. Subject matter jurisdiction is proper under 28 U.S.C. §§ 1331 and 1338.

8. This Court has personal jurisdiction over Westinghouse because Westinghouse conducts substantial business in Washington.

9. Venue is proper under 28 U.S.C. §§ 1391(b)(2) because, upon information and belief, a substantial part of the events giving rise to the claims described in this Complaint occurred in Washington, and under 28 U.S.C. §1391(c), as Westinghouse is subject to the personal jurisdiction in Washington.

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COUNT I: WESTINGHOUSE'S WILLFUL DIRECT INFRINGEMENT OF THE '669 PATENT

10. Zetec realleges and incorporates by reference each of paragraphs 1–9 above.

11. Westinghouse directly infringes at least claim 1 of the '669 Patent by its use of the CoreStar International Corporation OMNI-200.

12. Westinghouse has profited and will continue to profit from its direct infringement of the '669 Patent.

13. Westinghouse's actions with regard to its direct infringement of the '669 Patent have caused and will continue to cause Zetec substantial harm and irreparable injury, for which Zetec is entitled to receive injunctive relief and adequate compensatory damages under 35 U.S.C. §§ 283 and 284.

14. Westinghouse's actions with regard to its direct infringement of the '669 Patent were and are willful such that Zetec is entitled to treble damages under 35 U.S.C. § 284.

COUNT II: WESTINGHOUSE'S WILLFUL DIRECT INFRINGEMENT OF THE '197 PATENT

15. Zetec realleges and incorporates by reference each of paragraphs 1–9 above.

16. Westinghouse directly infringes at least claim 1 of the '197 Patent by its use of the CoreStar International Corporation OMNI-200.

17. Westinghouse has profited and will continue to profit from its direct infringement of the '197 Patent.

18. Westinghouse's actions with regard to its direct infringement of the '197 Patent have caused and will continue to cause Zetec substantial harm and irreparable injury, for which Zetec is entitled to receive injunctive relief and adequate compensatory damages under 35 U.S.C. §§ 283 and 284.

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19. Westinghouse's actions with regard to its direct infringement of the '197 Patent were and are willful such that Zetec is entitled to treble damages under 35 U.S.C. § 284.

COUNT III: WESTINGHOUSE'S WILLFUL DIRECT INFRINGEMENT OF THE '671 PATENT

20. Zetec realleges and incorporates by reference each of paragraphs 1–9 above.

21. Westinghouse directly infringes at least claim 1 of the '671 Patent by its use of the CoreStar International Corporation OMNI-200.

22. Westinghouse has profited and will continue to profit from its direct infringement of the '671 Patent.

23. Westinghouse's actions with regard to its direct infringement of the '671 Patent have caused and will continue to cause Zetec substantial harm and irreparable injury, for which Zetec is entitled to receive injunctive relief and adequate compensatory damages under 35 U.S.C. §§ 283 and 284.

24. Westinghouse's actions with regard to its direct infringement of the '671 Patent were and are willful such that Zetec is entitled to treble damages under 35 U.S.C. § 284.

JURY DEMAND

25. Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Zetec requests a trial by jury for all issues so triable.

PRAYER OF RELIEF

WHEREFORE, Zetec respectfully requests that the Court enter judgment against Westinghouse as follows:

A. Find that Westinghouse has and continues to directly infringe claim 1 of the '669 Patent;

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B. Find that Westinghouse has and continues to directly infringe at least claim 1 of the ’197 patent;

C. Find that Westinghouse has and continues to directly infringe at least claim 1 of the ’671 patent;

D. Permanently enjoin Westinghouse, its officers, agents, servants, employees, and attorneys, and all those persons in active concert or participation with them or any of them who receive actual notice of the judgment, from further infringement of the ’669, ’197 and ’671 Patents;

E. Order Westinghouse to account for and pay Zetec all damages suffered by Zetec as a consequence of Westinghouse’s direct willful infringement and direct active inducement of infringement of the ’669, ’197 and ’671 Patents;

F. Award Zetec prejudgment and post-judgment interest on the damages it suffered as a consequence of Westinghouse’s willful infringement of the ’669, ’197 and ’671 Patents;

G. Award Zetec treble damages pursuant to 35 U.S.C. § 284 as a result of Westinghouse’s willfulness in directly infringing the ’669, ’197 and ’671 Patents;

H. Find that this is an “exceptional case” under 35 U.S.C. § 285 and award Zetec its reasonable attorney fees; and

I. Grant Zetec such other and further relief as the Court may deem just and proper at law or in equity.

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DATED November 17, 2014, at Seattle, Washington.

Respectfully Submitted,

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US006734669B2

(12) **United States Patent**
Lopez

(10) **Patent No.: US 6,734,669 B2**
(45) **Date of Patent: May 11, 2004**

(54) **DIGITAL DEMODULATION OF AN EDDY CURRENT SIGNAL**

(75) Inventor: **Estell Lopez**, Issaquah, WA (US)

(73) Assignee: **Zetec, Inc**, Issaquah, WA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 89 days.

(21) Appl. No.: **10/167,166**

(22) Filed: **Jun. 11, 2002**

(65) **Prior Publication Data**

US 2003/0227288 A1 Dec. 11, 2003

(51) **Int. Cl.**[7] **G01N 27/82**
(52) **U.S. Cl.** **324/238**; 324/242
(58) **Field of Search** 324/228, 234–243, 324/226

(56) **References Cited**

U.S. PATENT DOCUMENTS

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4,849,693 A * 7/1989 Prince et al. 324/225
5,508,610 A * 4/1996 Feeney et al. 324/233
2002/0163333 A1 * 11/2002 Schicker et al. 324/242

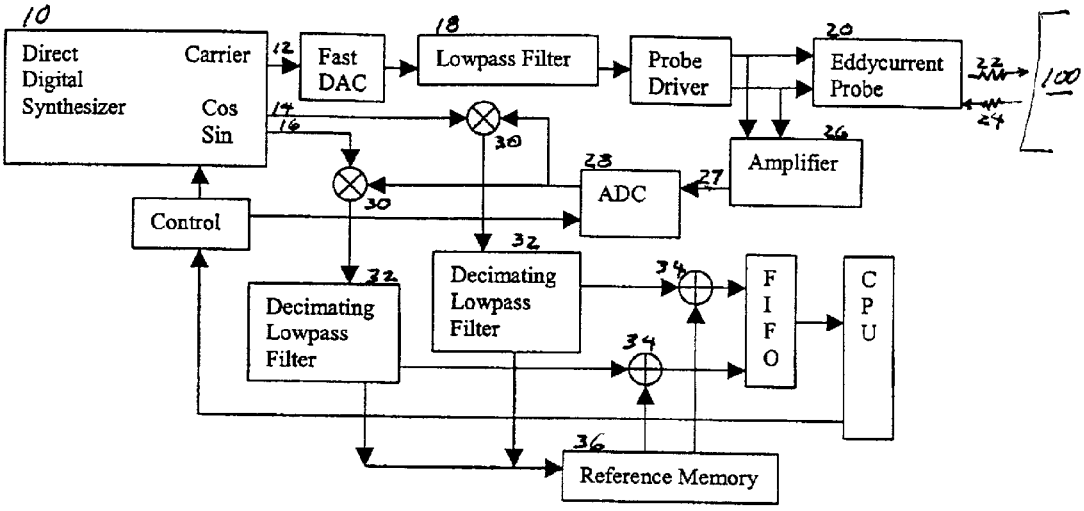
* cited by examiner

Primary Examiner—Jay Patidar
(74) *Attorney, Agent, or Firm*—David L. Tingey

(57) **ABSTRACT**

A digital synthesizer generates an electrical digital carrier that drives probe coil to generate an electromagnetic wave propagated into a test material proximate the probe coil. A return electromagnetic wave generated by eddy currents in the material includes signatures of material defects modulated on the return carrier electromagnetic wave. The return wave is detected by one or more probe coils, amplified, converted from an analog signal to a digital signal and then digitally mixed with digital sine and cosine functions also generated by the digital synthesizer to yield sum and difference values, mathematically expressing various eddy current signals received by the probe in a complete set of orthogonal functions. A low pass filter then removes all but the difference values. A direct current reference component is subtracted from the mixed digital signal, which translates the signal to center about a zero axis for ease of display and analysis.

17 Claims, 2 Drawing Sheets



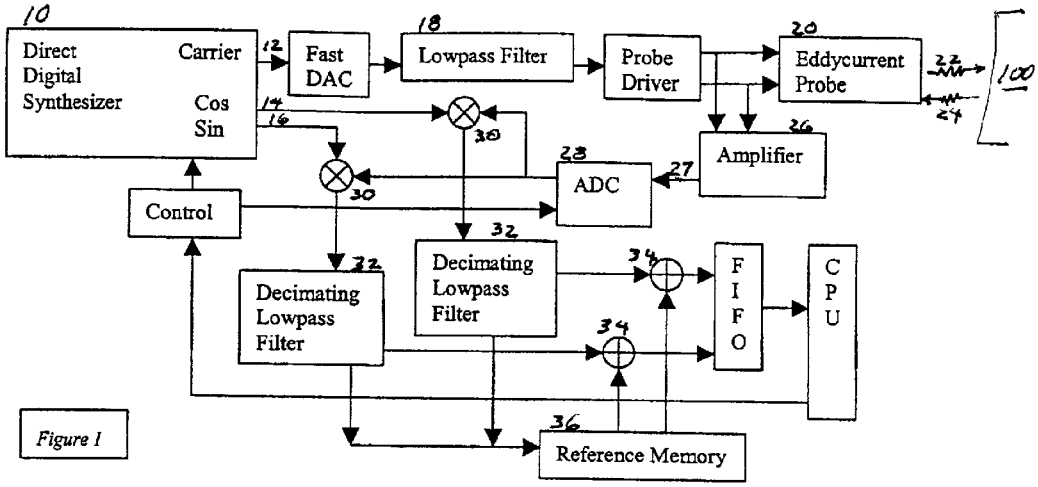

10
Direct Digital Synthesizer
Carrier
Cos
Sin
12
Fast DAC
18
Lowpass Filter
Probe Driver
20
Eddycurrent Probe
22
24
100
14
16
30
26
Amplifier
28
ADC
27
Control
32
Decimating Lowpass Filter
34
F I F O
C P U
Decimating Lowpass Filter
34
36
Reference Memory

Figure 1

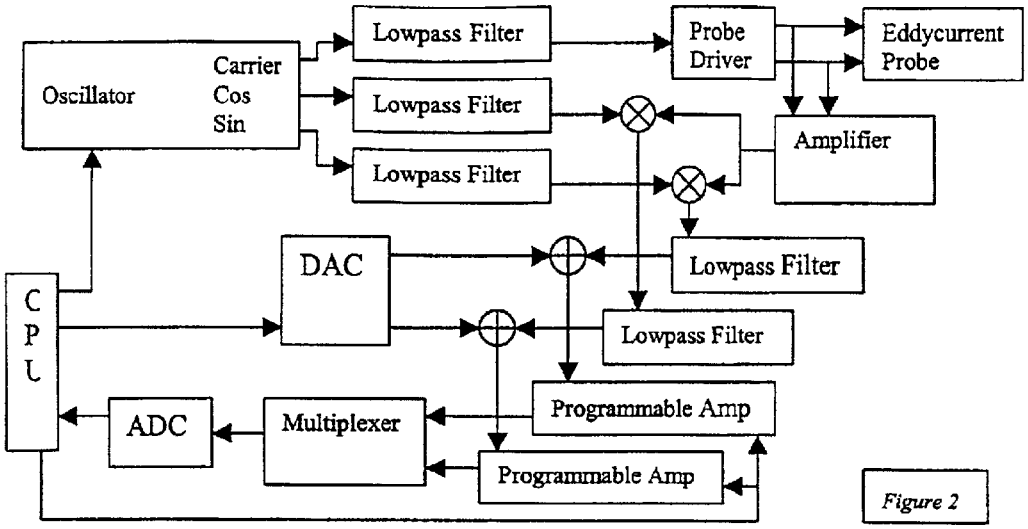


Figure 2

PRIOR ART

DIGITAL DEMODULATION OF AN EDDY CURRENT SIGNAL

BACKGROUND

1. Field of Technology

This invention relates to eddy current signal processing, and more particularly to extraction of an eddy current signal by digitally demodulating a carrier signal returned from an eddy current probe.

2. Prior Art

When an eddy current probe is in the vicinity of a flaw in a material, such as a hole or a crack, the flaw will modulate a carrier signal introduced into the material from an alternating current in a coil in the eddy current probe.

It is well known to extract the signal through analog signal processing. Generally, an oscillator generates a carrier signal and corresponding sine and cosine waves, which are then low-pass filtered. The carrier signal drives a probe coil that generates an electromagnetic field that penetrates into a nearby material. An eddy current is generated in the material, which generates its own electromagnetic field that is detected by the probe coil. When the material is without flaws, the two electromagnetic fields are largely out of phase and the fields partially cancel. However, when a flaw exists in the material, the amplitude and phase of the second field are modified and a small detectable signal results, modulated on the return carrier signal. The signal is amplified and then mixed, or multiplied, with the sine and cosine waves and again low-pass filtered. That is, the signal is mathematically factored into components of a complete set of orthogonal functions, which are represented by the sine and cosine functions. The signals out of the multipliers contain sum and difference products of the two frequencies that contain the amplitude and phase information of the flaw and of the harmonics of those frequencies. The low-pass filters reject all but the difference frequencies and any low-frequency harmonic products.

A programmable summer and a programmable amplifier then shift and scale the eddy current signals so that they optimize the input range of the analog to digital converter. A multiplexer than connects one signal component at a time to the computer through an analog to digital converter. The computer controls the frequency setting, the programmable summer, and the programmable amplifier. It also dictates the rate at which the analog to digital converter digitizes the eddy current signals.

Recent availability of digital components allows digital circuitry to perform many of the above functions digitally, yielding several advantages over analog processing. Digital processing reduces the number of components that must be installed on a circuit board, which may then be reduced in size. Fewer components may also lead to lower manufacturing costs and fewer manufacturing defects. Digital processing is also not concerned with variations caused by component tolerances or drift due to temperature and age, both of which are concerns for the analog method. It is also likely that the digital method will consume less power, especially as advances in CMOS continue to decrease the power consumption of digital circuits. These advantages of digital processing outweigh the disadvantage that digital circuitry is more complex, which is offset in that the digital circuitry still costs less than the analog multipliers.

SUMMARY

A digital synthesizer generates an electrical digital carrier that drives probe coil to generate an electromagnetic wave propagated into a test material proximate the probe coil. A return electromagnetic wave generated by eddy currents in the material includes signatures of material defects modulated on the return carrier electromagnetic wave. The return wave is detected by one or more probe coils, amplified, converted from an analog signal to a digital signal and then digitally mixed with digital sine and cosine functions also generated by the digital synthesizer to yield sum and difference values, mathematically expressing various eddy current signals received by the probe in a complete set of orthogonal functions. A low pass filter then removes all but the difference values. A direct current reference component is subtracted from the mixed digital signal, which translates the signal to center about a zero axis for ease of display and analysis.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a circuit for digital signal processing of an eddy current signal.

FIG. **2** is a block diagram of a circuit for analog signal processing of an eddy current signal, for comparison with digital signal processing of FIG. **1**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention comprises a digital eddy current signal processing method functionally similar to analog signal processing. A digital synthesizer **10** produces three digital sine waves **12**, **14**, and **16** that all have the same frequency, two of which are separated in phase by ninety degrees, establishing sine and cosine waves **14** and **16**. The third wave **12** is the carrier sine wave, which has variable amplitude and phase relative to the sine and cosine waves. Where a comparable oscillator of an analog method includes three high-speed digital-to-analog converters to generate the sine waves, in the digital method, only one is needed to generate a single wave (the carrier), typically using a digital phase accumulator and sine and cosine look-up tables. Each of the three waves is then derived from those tables.

The carrier signal **12** passes through a low-pass filter **18** and driven to the eddy current probe **20**, which transmits an electromagnetic wave **22** into material **100** proximate the probe **20**, generating eddy currents in the material. Defects in the material cause amplitude and phase differences in a return electromagnetic wave generated by the eddy currents. The phase differences, or equivalently frequency changes, constitute a signature of the defects as a modulation of the return wave. The probe detects the return electromagnetic wave **24** through one or more probe coils. An analog amplifier **26** amplifies the return signal from the probe. The analog amplifier may include a selectable gain value to optimize the input range of the analog-to-digital converter, increasing the gain of the amplifier to detect small flaws.

After amplification, an analog-to-digital converter **28** digitizes the modulated carrier signal **27**, the digitizing rate determined by digital control logic. If the signal is digitized prior to amplification, the amplifier is also digital.

A digital mixer **30** demodulates the signal from the carrier signal **12**. Digital sine and cosine waves **14** and **16** from the synthesizer **10** mathematically multiply digital input samples of the carrier signal **27** from the analog to digital converter **28** in the digital mixer **30**. Multiplication by the sine and cosine waves creates in-phase and quadrature outputs useful for maintaining amplitude and phase information contained in the modulated input carrier signal **27** and a single-sideband complex translation of the real part of

the input carrier wave **27**. Unlike analog mixers, which also generate many unwanted mixer products, the digital mixer produces only sum and difference frequency signals without harmonics of the two signals.

Decimating low-pass filters **32** then reject all but the difference frequencies, which together comprise the eddy current signal, effectively translating frequencies in the input signal to lower frequencies. With higher frequencies no longer present, the signal can be represented by a much smaller data sample in keeping with the Nyquist sampling theorem (any signal can be represented by discrete samples if the sampling rate is at least twice the bandwidth of the signal).

Following the decimating low-pass filters **32** is a digital direct current null circuit **34**. To conveniently center the eddy current signal at zero so that it appears at the center of a display, the direct current value of the eddy current signal, which is stored in a reference memory **36**, is subtracted from all signals that follow. The direct current reference signal is one of the outputs of the decimating low-pass filters **32**. With the eddy current signal thus demodulated from the carrier wave **27** and centered about zero, it is available for display and analysis.

Having described the invention, what is claimed is as follows:

1. The method of measuring anomalies, or defects, in a test material proximate one or more coils of an eddy current probe, comprising the following steps:

a. in an electrical circuit, synthesizing a digital carrier signal and digital functions;

b. converting the digital carrier signal to an analog carrier signal;

c. driving a probe test coil in an eddy current probe with the analog carrier signal therein generating a probe electromagnetic field from the probe test coil into the proximate test material which excites eddy currents in the test material that cause a return electromagnetic wave generally out of phase with the probe electromagnetic wave;

d. passing the probe test coil over a material anomaly, or material defect, the anomaly causing amplitude and phase differences in said return electromagnetic wave, which wave causes an electric current in the probe test coil to vary as a modulation of the return electromagnetic wave, the phase differences, or equivalently frequency changes, constituting an eddy current signature of the anomaly;

e. receiving said return electromagnetic wave in a probe detection coil causing an electrical analog carrier signal within the coil;

f. amplifying the analog carrier signal;

g. digitizing said analog carrier signal into a digital carrier signal;

h. mixing said digital carrier signal with said digital functions;

i. isolating the eddy current signature of the anomaly by filtering said mixed digital carrier signal with a low-pass filter.

2. The method of claim **1** wherein the digital functions comprise a mathematically complete orthogonal set.

3. The method of claim **2** wherein the digital functions are sine and cosine functions.

4. The method of claim **3** further comprising the step of separating the eddy current signal from extraneous signals after the step of mixing said digital carrier signal with said digital functions.

5. The method of claim **1** wherein the step of mixing said digital carrier signal with said digital functions further comprises the step of rejecting all but difference frequencies between the digital carrier signal and the digital functions, which difference frequencies comprise the eddy current signature demodulated from the digital carrier signal.

6. The method of claim **5** wherein the step of rejecting all but difference frequencies further comprises translating frequencies in the digital carrier signal to lower frequencies.

7. The method of claim **1** wherein the step of mixing said digital carrier signal with said digital functions comprises mathematically multiplying said digital carrier signal by said digital functions digitally in a mixer, producing only sum and difference frequency signals without harmonics of the mixed digital carrier signal.

8. The method of claim **7** wherein said digital functions are sine and cosine functions.

9. The method of claim **1** further comprising the step of translating the eddy current signature after the step of mixing said digital carrier signal with said digital functions.

10. The method of claim **9** wherein the step of translating the eddy current signature comprises the step of subtracting a reference component.

11. The method of claim **10** wherein the step of separating the eddy current signal from extraneous signals includes the step of applying a digital low pass frequency filter.

12. The method of claim **10** wherein the step of subtracting a reference component further comprises the step of subtracting a direct current component of the eddy current signal.

13. The method of claim **12** wherein the step of subtracting a direct current component of the eddy current signal includes the step of storing said direct current component of the eddy current signal in a reference memory for later extraction as said reference component.

14. The method of measuring anomalies, or defects, in a test material proximate one or more coils of an eddy current probe, comprising the following steps:

a. in an electric circuit, synthesizing a digital carrier signal and digital sine and cosine functions;

b. converting the digital carrier signal to an analog carrier signal;

c. driving a probe test coil in an eddy current probe with the analog carrier signal therein generating a probe electromagnetic field from the probe test coil into the proximate test material which excites eddy currents in the test material that cause a return electromagnetic field generally out of phase with the probe electromagnetic field;

d. passing the probe test coil over a material anomaly, or material defect, the anomaly causing amplitude and phase differences in said return electromagnetic wave, which wave causes an electric current in the probe test coil to vary as a modulation of the return electromagnetic wave, the phase differences, or equivalently frequency changes, constituting an eddy current signature of the anomaly.

e. receiving said return electromagnetic wave in a probe detection coil causing an electrical analog carrier signal within the coil;

f. amplifying the analog carrier signal;

g. digitizing said analog carrier signal into a digital carrier signal;

h. mathematically multiplying said digital carrier signal digitally by said digital sine and cosine functions in a mixer that produces only sum and difference frequency signals without harmonics of the mixed digital carrier signal;

i. passing said mixed digital carrier signal through a low-pass filter functionally isolating the eddy current signature of the anomaly thereby rejecting all but difference frequencies between the digital carrier signal and the digital functions, which difference frequencies comprise the eddy current signature demodulated from the digital carrier signal.

j. subtracting a direct current reference component of the eddy current signature from the eddy current signature, the reference component having been extracted from a prior eddy current signature and stored in a reference memory for later application as said reference component.

15. The method of claim **14** further comprising the step of translating the eddy current signature alter the step of mixing said digital carrier signal with said digital functions.

16. The method of claim **14** further comprising the step of separating the eddy current signal from extraneous signals after the step of mixing said digital carrier signal with said digital functions.

17. An electrical circuit operationally generating and digitally demodulating an electrical eddy current signature derived from defects in a material proximate one or more eddy current coils of an eddy current probe, said electrical circuit comprising:

a. a signal synthesizer operationally generating a digital carrier signal and digital sine and cosine functions;

b. a digital to analog converter electrically converting the digital carrier generated by the signal synthesizer to an analog carrier signal, the digital to analog converter electrically communicating with the probe test coil to drive it to generate an electromagnetic carrier wave into said test material, therein generating eddy currents from material defects found in the material by the carrier wave, the eddy currents producing an electromagnetic return wave detected by said probe coils, an electrical return analog carrier signal generated in the probe coils;

c. an amplifier electrically amplifying said the analog carrier signal;

d. an analog to digital converter converting said analog carrier signal into a digital carrier signal;

e. a mixer mathematically multiplying said digital carrier signal digitally by said digital sine and cosine functions producing only sum and difference frequency signals without harmonics of the mixed digital carrier signal;

f. a digital low-pass filter through which said mixed digital carrier signal passes, therein operationally rejecting all but difference frequencies between the carrier signal and the digital functions in filtering said mixed digital signal, which difference frequencies comprise the eddy current signature demodulated from the digital carrier signal, thereby functionally digitally isolating the eddy current signature;

g. a reference memory in which a prior eddy current signature is stored for later application as a direct current reference component, said reference component being electrically extractable from said reference memory for subtraction from said eddy current signature.

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US006798197B2

(12) **United States Patent**
Lopez

(10) **Patent No.: US 6,798,197 B2**
(45) **Date of Patent: Sep. 28, 2004**

(54) **DYNAMIC GAIN CONTROL IN A DIGITAL EDDY CURRENT SIGNAL PROCESSOR**

(75) Inventor: **Estell Lopez**, Issaquah, WA (US)

(73) Assignee: **Zetec, Inc.**, Issaquah, WA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 164 days.

(21) Appl. No.: **10/266,845**

(22) Filed: **Oct. 8, 2002**

(65) **Prior Publication Data**

US 2004/0066189 A1 Apr. 8, 2004

(51) **Int. Cl.**[7] **G01N 27/82**
(52) **U.S. Cl.** **324/238**; 324/242
(58) **Field of Search** 324/234–243, 324/228, 226

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5,461,312 A	*	10/1995	Hosohara et al.	324/220
5,508,610 A	*	4/1996	Feeney et al.	324/233

* cited by examiner

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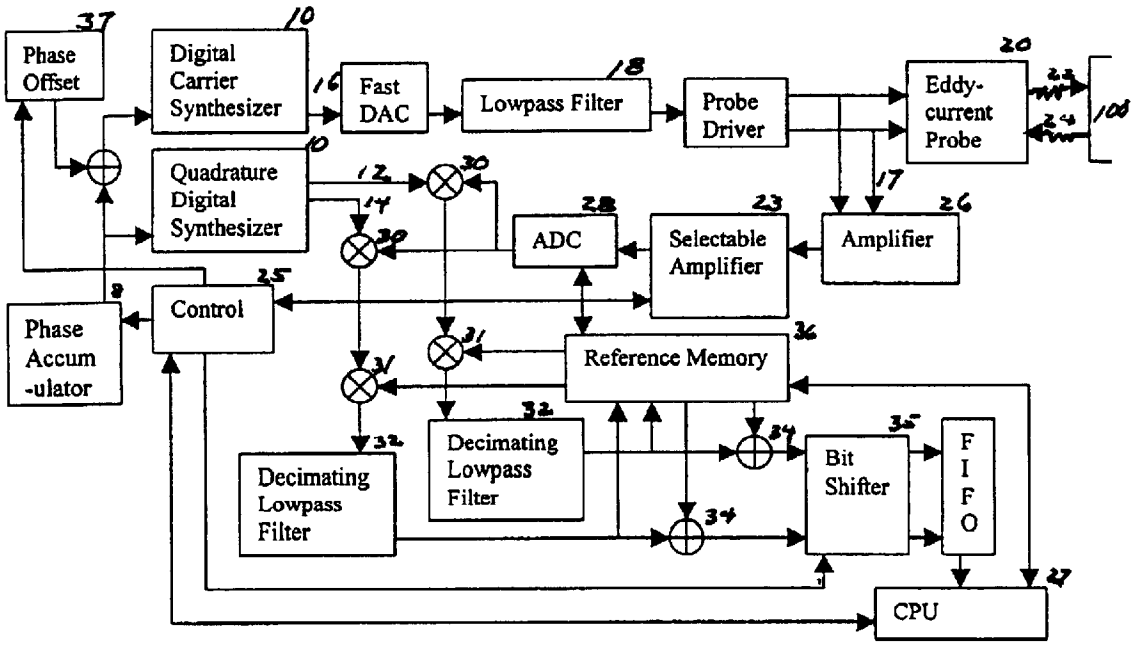
(57) **ABSTRACT**

A method and apparatus of a digital synthesizer generating an electrical digital carrier that is converted to analog and driven a probe coil to generate an electromagnetic wave propagated into a test material proximate the probe coil. A return electromagnetic wave generated by eddy currents in the material includes signatures of material defects modulated on the return carrier electromagnetic wave. The return wave is detected by one or more probe coils and amplified. A second amplifier is applied selectively amplifying the signal in segments such that each segment exploits the input range of the analog to digital converter. The signal is then converted from an analog signal to a digital signal and then digitally mixed with digital sine and cosine functions also generated by the digital synthesizer to yield sum and difference values. A gain scaling stage then trims the signal to overcome circuit imprecision such that the amplification in each respective segment is a power of two. A low pass filter then removes all but the difference values, leaving only the small eddy current signal. A direct current reference component is subtracted from the mixed digital signal, which translates the signal to center about a zero axis for ease of display and analysis. A bit shifter than reverses the selective signal amplification by simply shifting bits in the digital representation of the signal corresponding to the prior selective amplification.

15 Claims, 5 Drawing Sheets



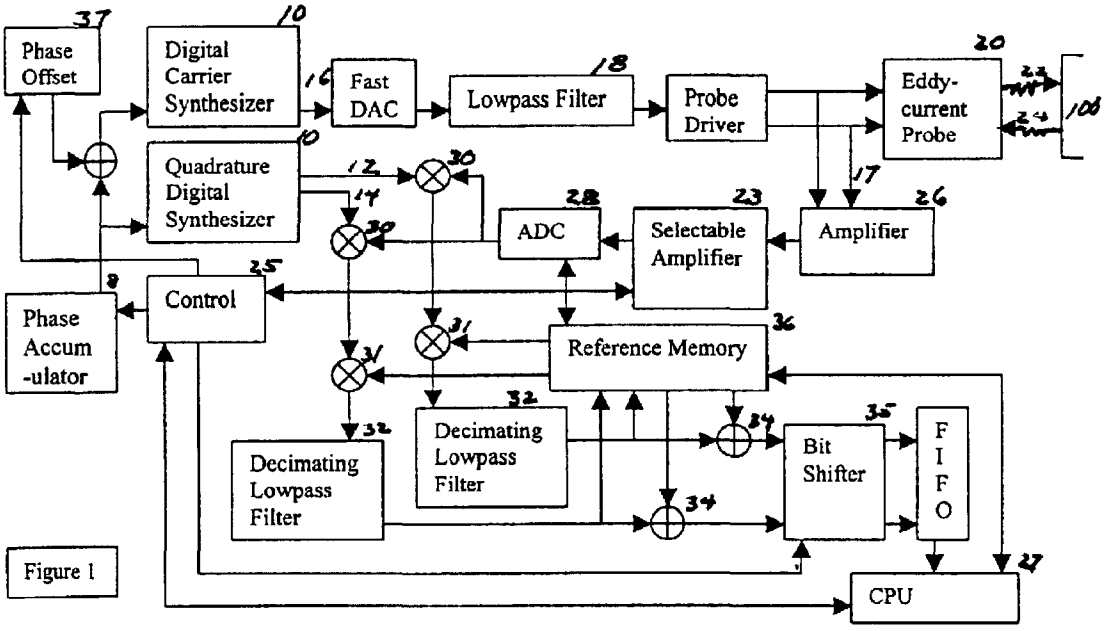

Phase Offset
Digital Carrier Synthesizer
Fast DAC
Lowpass Filter
Probe Driver
Eddy-current Probe
Quadrature Digital Synthesizer
ADC
Selectable Amplifier
Amplifier
Control
Phase Accum -ulator
Reference Memory
Decimating Lowpass Filter
Decimating Lowpass Filter
Bit Shifter
FIFO
CPU

Figure 1

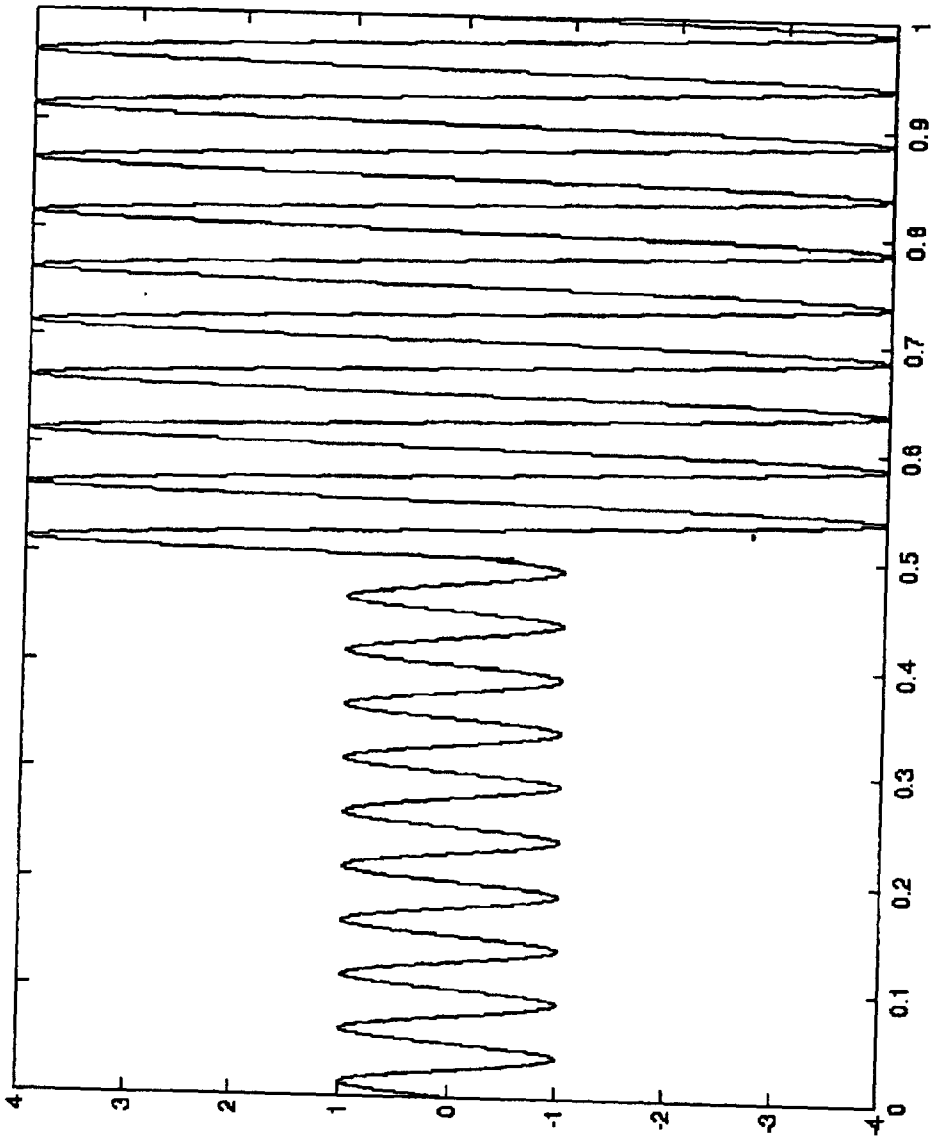


Fig. 2

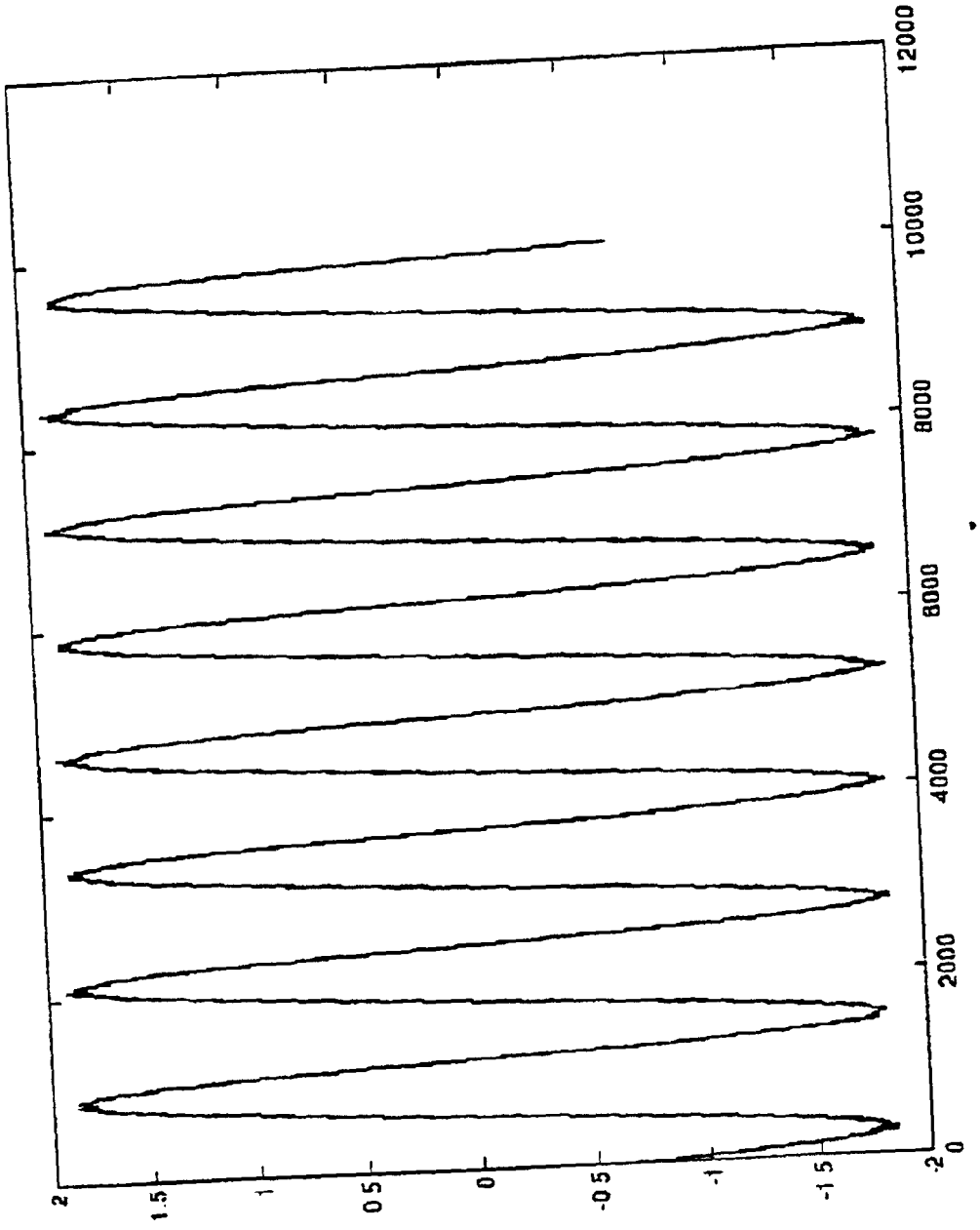


Fig. 3

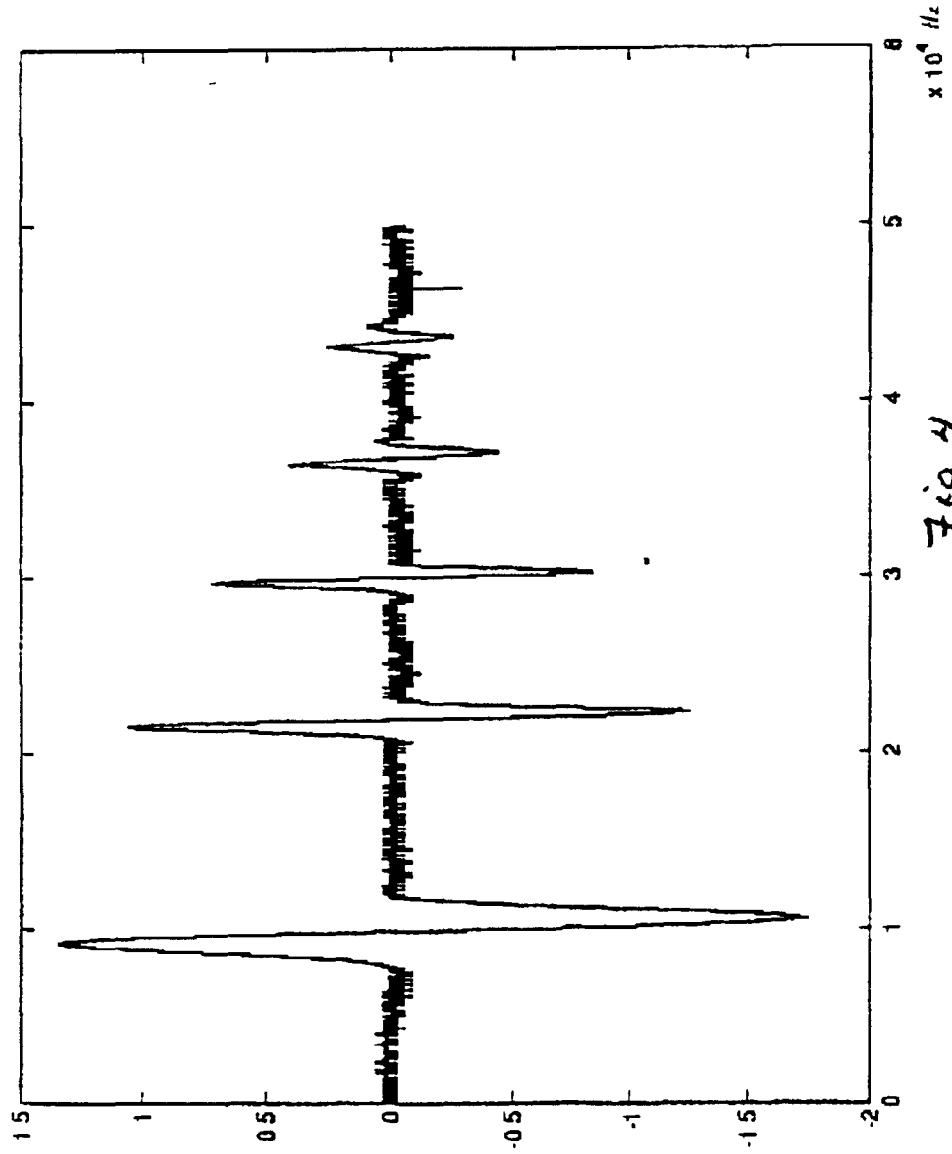


Fig. 4

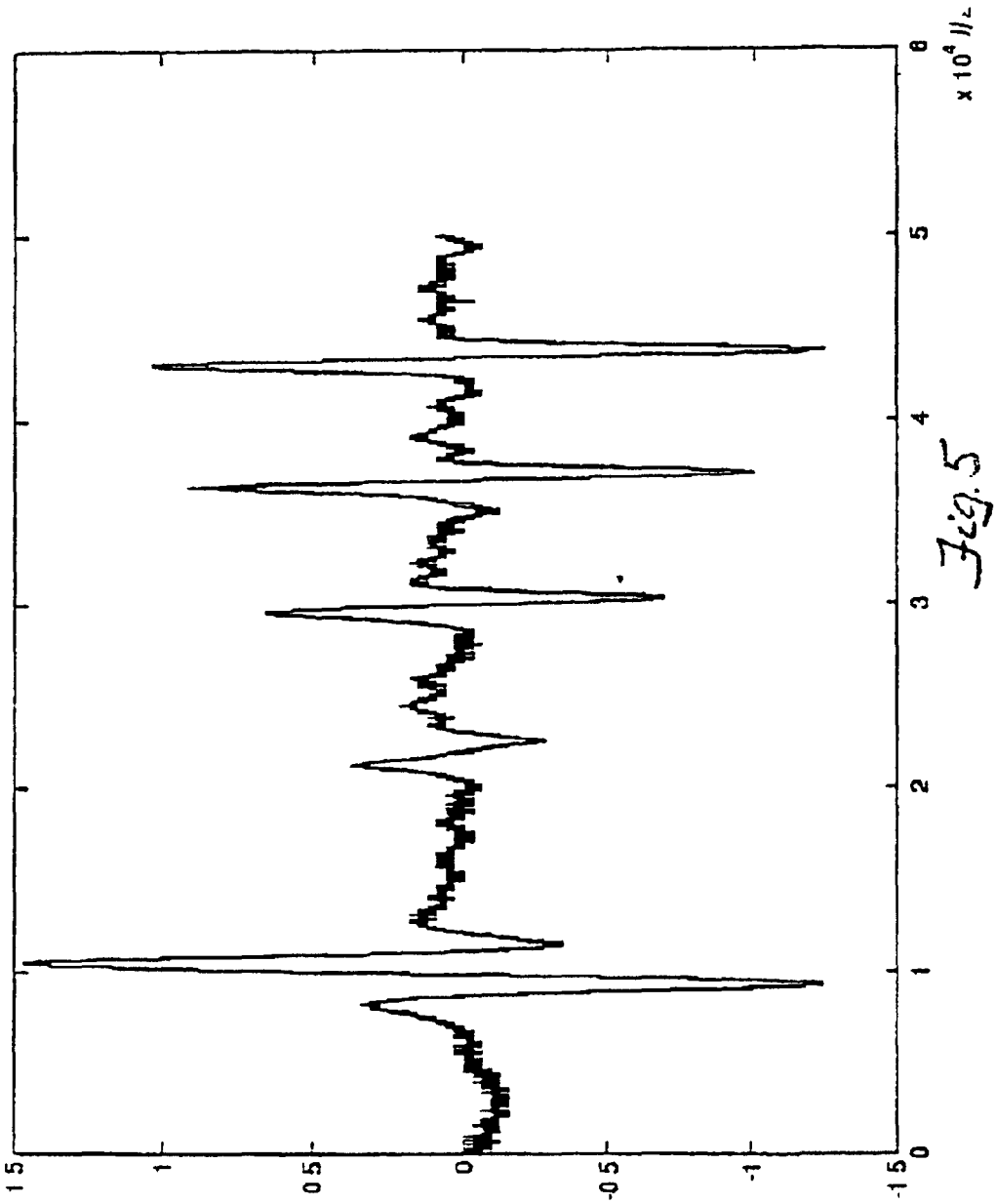


Fig. 5

DYNAMIC GAIN CONTROL IN A DIGITAL EDDY CURRENT SIGNAL PROCESSOR

BACKGROUND

1. Field of Technology

This invention relates to eddy current signal processing, and more particularly to digital extraction of an eddy current signal employing dynamic signal amplification and phase compensation.

2. Prior Art

When an eddy current probe is in the vicinity of a flaw in a material, such as a hole or a crack, the flaw will modulate a carrier signal introduced into the material from an alternating current in a coil in the eddy current probe.

It is known to extract the signal through digital signal processing. Generally, a digital oscillator generates a digital carrier signal and corresponding sine and cosine waves. The carrier is then converted to an analog signal, low-pass filtered, and then directed to a probe coil that generates an electromagnetic field that penetrates into a nearby material. An eddy current is generated in the material, which generates its own electromagnetic field that is detected by the probe coil. When the material is without flaws, the two electromagnetic fields are largely out of phase and the fields partially cancel. However, when a flaw exists in the material, the amplitude and phase of the second field are modified and a small detectable signal results, modulated on the return carrier signal. A programmable return signal amplifier optimizes the input range of the analog to digital converter where the signal is converted to a digital signal. The signal is then mixed, or multiplied, with the digital sine and cosine waves. The signals out of the multipliers contain sum and difference products of the mixed signals that contain the amplitude and phase information of the material flaw. Low-pass filters then apply to reject all but the difference frequencies. Then a direct current signal is subtracted from the eddy current signal to shift its axis to zero, which makes it easier to display on a screen.

As stated, the return signal amplifier is to optimize the input range of the analog to digital converter. In doing so, it is limited to scaling the maximum amplitude to the input range of the converter. Though this is an advantage in expanding the eddy current signal modulated on the carrier signal, the small eddy current signal in parts of the return signal other than near the signal maximum amplitude remains relatively small, possibly with insufficient resolution to exploit the information it contains or buried in signal noise below the quantization noise of the analog to digital converter.

SUMMARY

A digital synthesizer generates an electrical digital carrier that is converted to an analog signal and then driven to a probe coil. The coil generates an electromagnetic wave that propagates into a test material proximate the probe coil. A return electromagnetic wave generated by eddy currents in the material includes signatures of material defects modulated on the return carrier electromagnetic wave. The return wave is detected by one or more probe coils and amplified by a return signal amplifier. The signal is then again selectively amplified. That is, sections of the signal out of the return signal amplifier with relatively small amplitudes are again amplified to also exploit the range of the analog to digital converter. Sections of the signal with relatively large amplitudes are less amplified or passed through unchanged. The result is a signal that more fully exploits the range of the analog to digital converter throughout the signal, not just at the signal maximum amplitude. This more general amplification then amplifies the carrier signal and the eddy current signal on the carrier signal even at low signal amplitudes to effectively present the carrier signal and the eddy current signal for digitization with improved signal resolution.

When the signal is demodulated by mixing with the digital sine and cosine functions and low pass filter, only the eddy current signal remains. However, the resultant eddy current signal with the selective amplification yields a high resolution representation of the eddy current signal and signature of the material defect.

To make the selective amplification transparent to the signal analyst, the signal must be restored, while carrying the improved resolution of the defect signature. A bit shifter is used to attenuate the digital output signals by the same ratio that the selectable amplifier amplifies the signal prior to the analog to digital converter. This is achieved by recording the performance of the selective amplifier in a reference memory and reversing it after demodulation of the signal by effecting the bit shift. The digital signal is represented in a series of words having a word width in bits more than needed to fully express the signal amplitude. When the digital signal is bit shifted, it simply moves into previously unused bit places.

The bit shifter operates as a power of two multiplier when shifted to the left into unused bits and a divider when shifted to the right. Therefore, to consistently match the bit shifter, the selectable amplifier must generally also employ quantized steps of amplification in powers of two.

If the gain of the selectable amplifier were constant across the frequency range, then nothing else would need to be added to the digital eddy current signal processor. However, as is the case with any analog amplifier, the magnitude and phase of the selectable amplifier change with respect to frequency. Furthermore, the requirement for amplification in steps of powers of two is ideal. The actual ratio of amplification obtained in a real circuit does not exactly equal a power of two because the tolerance of the resistors in the circuit will cause the ratio to vary slightly. Also, the parasitic capacitance of the circuit board will cause the phase of the selectable amplifier to vary. Therefore in order to accomplish the goal of transparent gain switching, the gain and phase changes of the selectable amplifier must be compensated.

A phase offset is added to the digital synthesizer of the carrier wave to compensate for the phase change of the selectable amplifier. The phase-offset value is equal but opposite to the phase change of the selectable amplifier at the frequency generated by the phase accumulator. The phase change will vary with the gain setting of the selectable amplifier, therefore the phase-offset value will vary to correspond to the gain setting. The phase-offset value, calculated in a calibration procedure, may be zero when the gain setting is low and equal but opposite to the phase change of the selectable amplifier when the gain setting is high.

The gain variation of the selectable amplifier is compensated with a scaling stage after the demodulating mixers but before the low pass filters. The gain-scaling value that is used in the scaling stage is also calculated in the calibration procedure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a circuit for digital signal processing of an eddy current signal.

FIG. **2** is an example of selective amplification of a signal. Because the carrier signal was generated as a sine wave, and the carrier signal modulation due to return magnetic fields generated by eddy currents is small, the carrier signal continues to appear as a sinusoid. It is the nature of eddy current signal processing to remove this large carrier signal to reveal the remaining modulation on the carrier due to eddy currents. Eddy current probes are often employed in a differential circuit with two signal returns subtracted to remove much of the carrier signal. Where the differential amplifier is successful in removing a large portion of the carrier signal, this signal may be small. Otherwise, the signal will remain large. In some single-ended probe types a differential amplifier cannot be used, in which case the full carrier signal is amplified. FIG. **2** shows in the first half of the figure a sinusoid carrier signal with amplitude equal to 1.0, representative of a small signal after the differential amplifier. The second half shows it with amplitude 4.0 after being amplified in the selective amplifier. If the signal size from the differential amplifier later increases, then the selectable amplifier may be returned to a gain of 1.0. In cases where the carrier is well rejected and the eddy current signal is large, the signal may rise above and fall below a threshold at which the gain of the selectable amplifier is switched. In this case, the reate at which the selectable gain is switched is fully dependent upon the frequency characteristics of the eddy current signal and it is independent of the carrier signal frequency.

FIG. **3** illustrates a simple sinusoidal carrier with a relatively small and unnoticeable eddy current signal after amplification.

FIG. **4** and FIG. **5** are in-phase and quadrature components of an actual standard eddy current signal after it has been demodulated from the carrier signal of FIG. **3**, derived by moving a probe through a tube that has some standard eddy current flaw signals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention comprises a digital eddy current signal processing method and electronic circuit employing a dynamic gain control on signal amplification.

A phase accumulator **8** generates a linearly-increasing phase by iteratively adding an increment value to the current phase value. When the phase value exceeds the maximum value that can be expressed in the phase accumulator (2^N–1, where N is the number of bits in the phase accumulator), the overflow bit is simply discarded and the phase accumulator continues incrementing. The phase accumulator values represent a phase range from zero to 360 degrees. Larger increment values cause the phase accumulator to sweep through its range more frequently, thus generating higher frequencies. Therefore, the phase accumulator determines the frequency of synthesized carrier waves and sine and cosine waves.

A digital synthesizer **10** produces three digital sine waves **12**, **14**, and **16** from the phase output of the phase accumulator **8** that all have the same frequency, two of which are separated in phase by ninety degrees, establishing sine and cosine waves **12** and **14**. The third wave **16** is the carrier sine wave, which has variable amplitude and phase relative to the sine and cosine waves.

The carrier signal **16** passes through a low-pass filter **18** and is driven to eddy current probe **20**, which transmits an electromagnetic wave **22** into material **100** proximate the probe **20**, generating eddy currents in the material. Defects in the material cause amplitude and phase differences in a return electromagnetic wave **24** generated by the eddy currents. The phase differences, or equivalently frequency changes, constitute a signature of the defects as a modulation of the return wave. The probe detects the return electromagnetic wave **24**, now a modulated input carrier signal **17**, through one or more probe coils. A first analog amplifier **26** amplifies the return signal from the probe. The first analog amplifier **26** typically includes an adjustable gain value that scales the return signal maximum amplitude to the input range of the analog-to-digital converter **28**. A second analog amplifier **23**, a selectable amplifier under computer control or user control, selectively scales the signal in sections to optimize the respective sections of the signal to the input range of the analog-to-digital converter **28**.

After amplification, an analog-to-digital converter **28** digitizes the modulated input carrier signal **17**, the digitizing rate determined by digital control logic. If the signal is digitized prior to amplification, the amplifier is also digital.

A digital mixer **30** demodulates the signal from the carrier signal **16**. Digital sine and cosine waves **12** and **14** from the synthesizer **10** mathematically multiply digital input samples of the carrier signal **16** from the analog to digital converter **28** in the digital mixer **30**. Multiplication by the sine and cosine waves creates in-phase and quadrature outputs useful for maintaining amplitude and phase information contained in the modulated input carrier signal **17** and a single-sideband complex translation of the real part of the modulated carrier wave **17**. Unlike analog mixers, which also generate many unwanted mixer products, the digital mixer produces only sum and difference frequency signals without harmonics of the two signals.

A gain scaling stage **31** occurs after the demodulation stage as a fine adjustment to the gain introduced by the selectable filter to adjust for small differences between a desired amplification and the actual resulting amplification. In the scaling stage, each component of the eddy current signal is multiplied by a gain-scaling value. The gain-scaling value is equal to the desired gain ratio (a power of two) of the selectable amplifier divided by the actual (observed) gain ratio. In mathematical terms, the gain-scaling value is

$$G_C = \frac{G_H \cdot G'_L}{G_L \cdot G'_H}$$

where G_H/G_L is the desired gain ratio of the selectable amplifier, and G'_L/G'_H is the ratio of the actual low gain of the selectable amplifier **23** to its actual high gain at the frequency of the phase accumulator. The actual gain ratio is calculated via a calibration procedure. The value G_C is applied to the scaling multipliers in the gain scaling stage **31** when the high gain setting is selected in the selectable amplifier. The value 1.0 is applied to the scaling multipliers when the low gain setting is selected. For each treated signal section, both values are stored in reference memory **36**.

To correct for phase changes of the selectable amplifier, controller **25** directs a phase offset **37** to adjust phase from the phase accumulator **8** before it outputs to the digital carrier synthesizer. The controller **25** examines the size of the digital signal from the analog to digital converter to determine and set the gain of the selectable amplifier. If the controller chooses a low gain (because the signal is large), then it also sets the phase offset **37** to zero degrees and the gain scaling value to 1.0. If the controller chooses a high gain for the selectable amplifier (because the signal is small), then it sets the phase offset **37** to be equal and opposite the

phase change of the selectable amplifier, and it sets the gain scaling value to G_C. The controller also directs the bit shifter **35** to right-shift the quadrature eddy current signals when it chooses the high gain of the selectable amplifier. A computer **27** calculates the values of the phase offset and the gain scaling in a calibration procedure, which is an algorithm that is programmed into the computer.

While executing the calibration procedure, the computer **27** recognizes amplitude and phase discontinuities after the bit shifter and dictates adjustments in the gain scaling value and the phase offset value. The computer **27** communicates the adjusted values to the controller, which communicates them to the gain scaling stage **31**, and to the phase offset stage **37**. Then the controller sets the selectable amplifier **23** and bit shifters **35** accordingly in order to remove amplitude and phase discontinuities.

Decimating low-pass filters **32** then reject all but the difference frequencies, which together comprise the eddy current signal, effectively translating frequencies in the input signal to lower frequencies. With higher frequencies no longer present, the signal can be represented by a much smaller data sample in keeping with the Nyquist sampling theorem (any signal can be represented by discrete samples if the sampling rate is at least twice the bandwidth of the signal).

Following the decimating low-pass filters **32** is a digital direct current null circuit **34**. To conveniently center the eddy current signal at zero so that it appears at the center of a display, the direct current value of the eddy current signal, which is stored in a reference memory **36**, is subtracted from all signals that follow. The direct current reference signal is one of the outputs of the decimating low-pass filters **32**. The reference memory **36** is queried for the direct current reference signal, which is then output and summed (subtracted) from the signal from the decimating low-pass filters. With the eddy current signal thus demodulated from the carrier wave **16** and centered about zero, it is available for display and analysis.

The bit shifter **35** reverses the sectional amplitude gain of the selectable amplifier **23** by shifting the bits in the signal words to the right to correspond with the gain applied by the selectable amplifier **23**. Because each bit shift amounts precisely to a division by two the resultant signature will not be an exact reversal of the gain of selectable amplifier **23** although might be set to amplify the signal from the first amplifier by a power of two. Any real amplifier will not have a gain exactly equal to a power of two across the required frequency range (10 Hz to 10 MHz). This happens due to circuit performance shortcomings, such as electronic component drift from age or temperature, the variation of resistor values and the parasitic capacitances that exist on circuit boards. Therefore, a fine-tuning digital gain stage **31** is introduced after the multipliers **30** to trim the gain of the signal so the combination of the selectable amplifier and the digital gain stage results in an overall gain exactly equal to a power of two. Then the bit shifter **35** divides by the same power of two after the filters. Therefore, the combination of the selective amplification and the bit shifting is transparent to later signal analysis.

The invention being fully described, what is claimed is as follows:

1. The method of measuring anomalies, or defects, in a test material proximate one or more coils of an eddy current probe, comprising the following steps:

a. In an electrical circuit, synthesizing a digital carrier signal and two digital sinusoidal functions that all have a same frequency;

b. Converting the digital carrier signal to an analog carrier signal;

c. Driving a probe test coil in an eddy current probe with the analog carrier signal therein generating a probe electromagnetic field from the probe test coil into the proximate test material which excites eddy currents in the test material that cause a return electromagnetic wave generally out of phase with the probe electromagnetic wave;

d. Passing the probe test coil over a material anomaly, or material defect, the anomaly causing amplitude and phase differences in said return electromagnetic wave, which wave causes an electric current in the probe test coil to vary as a modulation of the return electromagnetic wave, amplitude and phase changes constituting an eddy current signature of the anomaly;

e. Receiving said return electromagnetic wave in a probe detection coil causing an electrical modulated return analog carrier signal within the coil;

f. Amplifying the return analog carrier signal;

g. Selectively amplifying segments of the return analog carrier signal;

h. Digitizing said analog carrier signal into a modulated digital carrier signal;

i. Mixing said modulated digital carrier signal with said digital sinusoidal functions into quadrature components;

j. Adjusting amplification achieved in selectively amplifying segments of the modulated digital carrier signal in a gain scaling stage such that resulting amplification of said signal segments is a power of two;

k. Isolating the eddy current signature of the anomaly by filtering said mixed modulated digital carrier signal with a low-pass filter;

l. Reversing said selective amplification of said signal segments by shifting bits in the modulated digital carrier signal.

2. The method of claim **1** in which the step of amplifying the return analog carrier signal includes scaling the return analog carrier signal to a maximum amplitude within the input range of the analog-to-digital converter.

3. The method of claim **1** in which the step of selectively amplifying segments of the return analog carrier signal includes employing a selectable amplifier under computer control that selectively scales the signal in sections to optimize the respective sections of the signal to the input range of the analog-to-digital converter.

4. The method of claim **1** including the step of adjusting phase of the digital carrier signal before it is converted to an analog signal correcting for unwanted phase changes to the return analog carrier signal that occur in the selectable amplifier.

5. The method of claim **1** including the step of a controller directing introduction of a phase offset to wave defining information from a phase accumulator before introducing said wave defining information to a synthesizer of said digital carrier signal.

6. The method of claim **1** including the step of a controller directing gain adjustment after examining the size of a digital signal from the analog to digital converter to set the gain of the selectable amplifier.

7. The method of claim **6** including the step of the controller also setting the phase offset to zero degrees and the gain scaling value to 1.0 if the controller chooses a low gain because the signal is large.

8. The method of claim **6** including the step of the controller also setting the phase offset to be equal and opposite the phase change of the selectable amplifier if the controller sets a high gain for the selectable amplifier because the signal is small.

9. The method of claim **8** including the step of the controller setting the gain scaling value to

$$G_C = \frac{G_H \cdot G'_L}{G_L \cdot G'_H}$$

where G_H/G_L is the desired gain ratio of the selectable amplifier, and G'_L/G'_H is the ratio of the actual low gain of the selectable amplifier to its actual high gain at the frequency of the phase accumulator.

10. The method of claim **8** in which the controller also directs the bit shifter to right-shift the demodulated quadrature components of the signal when it sets the high gain of the selectable amplifier.

11. The method of claim **8** in which a computer calculates values of the phase offset and the gain scaling in a calibration algorithm, which algorithm is programmed into the computer, in which said algorithm recognizes amplitude and phase discontinuities after the bit shifter and dictates adjustments in the gain scaling value and the phase offset value.

12. The method of claim **11** in which the computer communicates the adjustments to the controller, which communicates them to the gain scaling and phase offset stage.

13. The method of claim **12** in which the controller sets the selectable amplifier and bit shifters in order to remove amplitude and phase discontinuities.

14. The method of measuring anomalies, or defects, in a test material proximate one or more coils of an eddy current probe, comprising the following steps:

a. In an electrical circuit, synthesizing a digital carrier signal and two digital sinusoidal functions that all have a same frequency;

b. Converting the digital carrier signal to an analog carrier signal;

c. Driving a probe test coil in an eddy current probe with the analog carrier signal therein generating a probe electromagnetic field from the probe test coil into the proximate test material which excites eddy currents in the test material that cause a return electromagnetic wave generally out of phase with the probe electromagnetic wave;

d. Passing the probe test coil over a material anomaly, or material defect, the anomaly causing amplitude and phase differences in said return electromagnetic wave, which wave causes an electric current in the probe test coil to vary as a modulation of the return electromagnetic wave, amplitude and phase changes constituting an eddy current signature of the anomaly;

e. Receiving said return electromagnetic wave in a probe detection coil causing an electrical analog modulated return carrier signal within the coil;

f. Amplifying the return analog carrier signal to a maximum amplitude of an input range of the analog-to-digital converter;

g. Selectively amplifying segments of the return analog carrier signal by employing a selectable amplifier under control of a computer that selectively scales the signal in sections in optimizing respective sections of the signal to the input range of the analog-to-digital converter;

h. Digitizing said analog carrier signal into a modulated digital carrier signal;

i. Mixing said modulated digital carrier signal with said digital sinusoidal functions into quadrature components;

j. Adjusting amplification achieved in selectively amplifying segments of the modulated digital carrier signal in a gain scaling stage such that resulting amplification of said signal segments is a power of two, a controller directing gain adjustment after examining the size of a digital signal from the analog to digital converter in order to set the gain of the selectable amplifier, and wherein the controller sets the gain scaling value to

$$G_C = \frac{G_H \cdot G'_L}{G_L \cdot G'_H}$$

where G_H/G_L is the desired gain ratio of the selectable amplifier, and G'_L/G'_H is the ratio of the actual low gain of the selectable amplifier to its actual high gain at the frequency of the phase accumulator,

k. Adjusting phase of the digital carrier signal before it is converted to analog correcting for unwanted phase changes to the carrier signal that occur in the selectable amplifier by a controller directing introduction of a phase offset to wave defining information from a phase accumulator before introducing said wave defining information to a synthesizer of said digital carrier signal, if the controller chooses a low gain because the signal is large, then including the step of the controller also setting the phase offset to zero degrees and the gain scaling value to 1.0, but if the controller sets a high gain for the selectable amplifier because the signal is small, then including the step of the controller also setting the phase offset to be equal and opposite the phase change of the selectable amplifier;

l. Isolating the eddy current signature of the anomaly by filtering said mixed digital carrier signal with a low-pass filter;

m. Reversing said amplification of said signal segments selectively amplified by the controller setting the selectable amplifier and a bit shifter to remove amplitude and phase discontinuities, the bit shifter shifting bits in a digital representation of the carrier signal, the computer calculating values of the phase offset and the gain scaling in a calibration algorithm programmed into the computer, said algorithm recognizing amplitude and phase discontinuities after the bit shifter and dictating adjustments in the gain scaling value and the phase offset value, the computer communicating the adjustments to the controller, which communicates them to the gain scaling and phase offset stage.

15. An electrical circuit operationally generating and digitally demodulating an electrical eddy current signature derived from defects in a material proximate one or more eddy current coils of an eddy current probe, said electrical circuit comprising:

a signal synthesizer operationally generating a digital carrier signal and digital sine and cosine functions;

a digital to analog converter electrically converting the digital carrier generated by the signal synthesizer to an analog carrier signal, the digital to analog converter electrically communicating with the probe test coil to drive it to generate an electromagnetic carrier wave into said test material, therein generating eddy currents

from material defects found in the material by the carrier wave, the eddy currents producing an electromagnetic return wave detected by said probe coils, an electrical return analog carrier signal generated in the probe coils;

an amplifier electrically amplifying said the return analog carrier signal;

a selective amplifier selectively amplifying segments of the carrier signal;

an analog to digital converter converting said analog carrier signal into a digital carrier signal;

a first mixer mathematically multiplying said digital carrier signal digitally by said digital sine and cosine functions producing only sum and difference frequency signals without harmonics of the mixed digital carrier signal;

a second mixer comprising a gain scaling stage to overcome circuit imprecision, adjusting amplification achieved in selectively amplifying segments of the carrier signal such that resulting amplification of said signal segments is a power of two;

a digital low-pass filter through which said mixed digital carrier signal passes, therein operationally rejecting all but difference frequencies between the carrier signal and the digital sine and cosine functions in filtering said mixed digital signal, which difference frequencies comprise the eddy current signature demodulated from the digital carrier signal, thereby functionally digitally isolating the eddy current signature,

a bit shifter reversing said selective amplification of said signal segments by shifting bits in a digital representation of the carrier signal,

a reference memory in which a prior eddy current signature is stored for later application as a direct current reference component, said reference component being electrically extractable from said reference memory for subtraction from said eddy current signature.

* * * * *

US006809671B1

(12) **United States Patent**
Lopez

(10) **Patent No.: US 6,809,671 B1**
(45) **Date of Patent: Oct. 26, 2004**

(54) **DYNAMIC GAIN CONTROL IN A DIGITAL EDDY CURRENT SIGNAL PROCESSOR**

(75) Inventor: **Estell Lopez**, Issaquah, WA (US)

(73) Assignee: **Zetec, Inc.**, Issaquah, WA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/809,964**

(22) Filed: **Mar. 26, 2004**

Related U.S. Application Data

(62) Division of application No. 10/266,845, filed on Oct. 8, 2002.

(51) **Int. Cl.**[7] **H03M 1/62**
(52) **U.S. Cl.** **341/139**; 324/234
(58) **Field of Search** 324/234, 228, 324/226; 341/139

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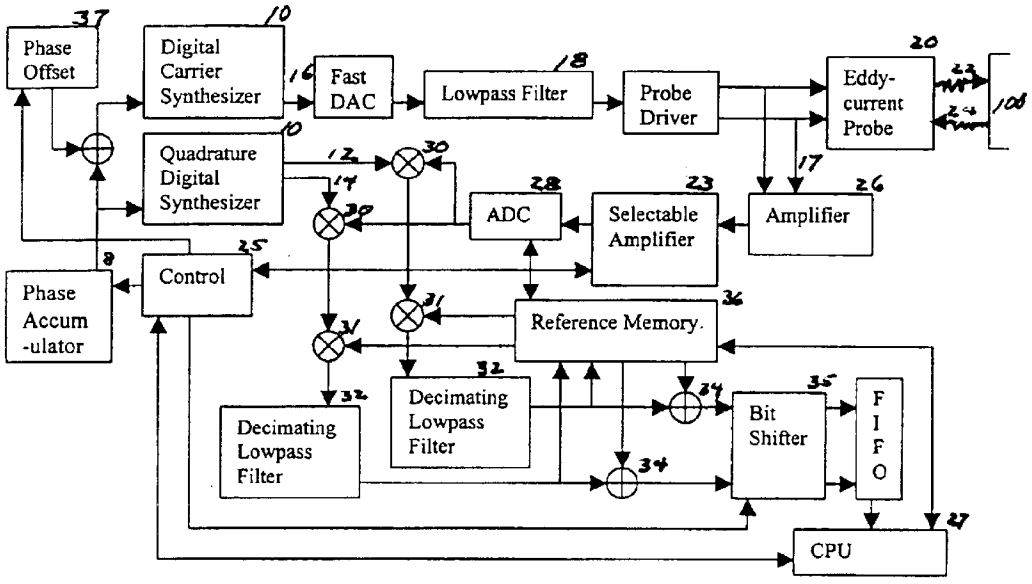
Primary Examiner—Brian Young
Assistant Examiner—Joseph Lauture

(74) *Attorney, Agent, or Firm*—David L. Tingey

(57) **ABSTRACT**

A digital synthesizer generates an electrical digital carrier that is converted to analog and driven a probe coil to generate an electromagnetic wave propagated into a test material proximate the probe coil. A return electromagnetic wave generated by eddy currents in the material includes signatures of material defects modulated on the return carrier electromagnetic wave. The return wave is detected by one or more probe coils and amplified. A second amplifier is applied selectively amplifying the signal in segments such that each segment exploits the input range of the analog to digital converter. The signal is then converted from an analog signal to a digital signal and then digitally mixed with digital sine and cosine functions also generated by the digital synthesizer to yield sum and difference values. A gain scaling stage then trims the signal to overcome circuit imprecision such that the amplification in each respective segment is a power of two. A low pass filter then removes all but the difference values, leaving only the small eddy current signal. A direct current reference component is subtracted from the mixed digital signal, which translates the signal to center about a zero axis for ease of display and analysis. A bit shifter than reverses the selective signal amplification by simply shifting bits in the digital representation of the signal corresponding to the prior selective amplification.

3 Claims, 5 Drawing Sheets



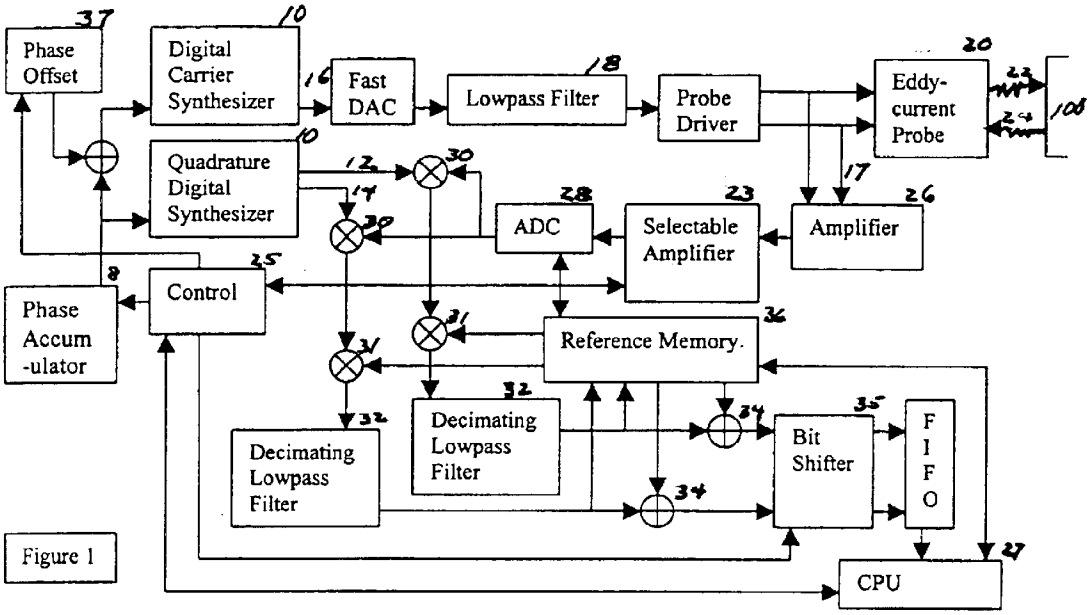

Phase Offset
Digital Carrier Synthesizer
Fast DAC
Lowpass Filter
Probe Driver
Eddy-current Probe
Quadrature Digital Synthesizer
ADC
Selectable Amplifier
Amplifier
Control
Phase Accum-ulator
Reference Memory
Decimating Lowpass Filter
Decimating Lowpass Filter
Bit Shifter
FIFO
CPU

Figure 1

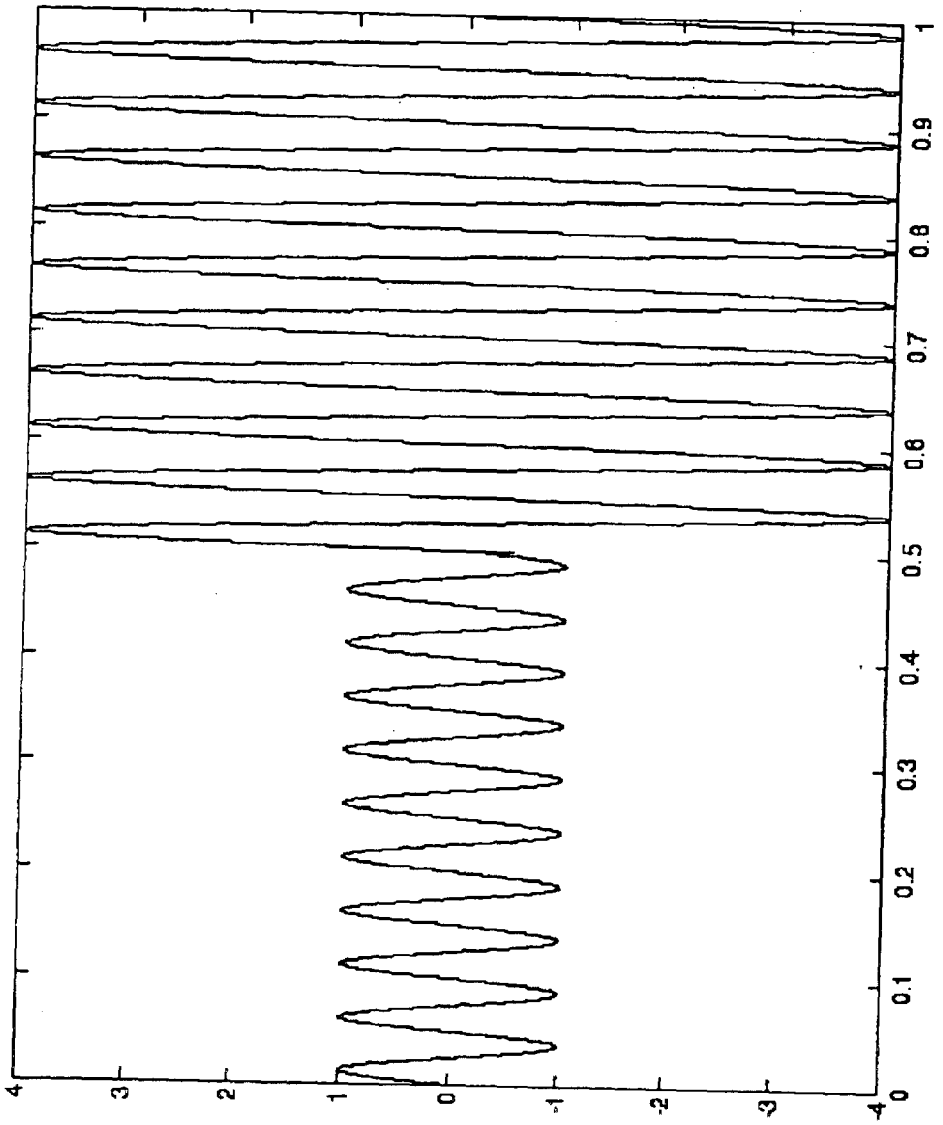


Fig. 2

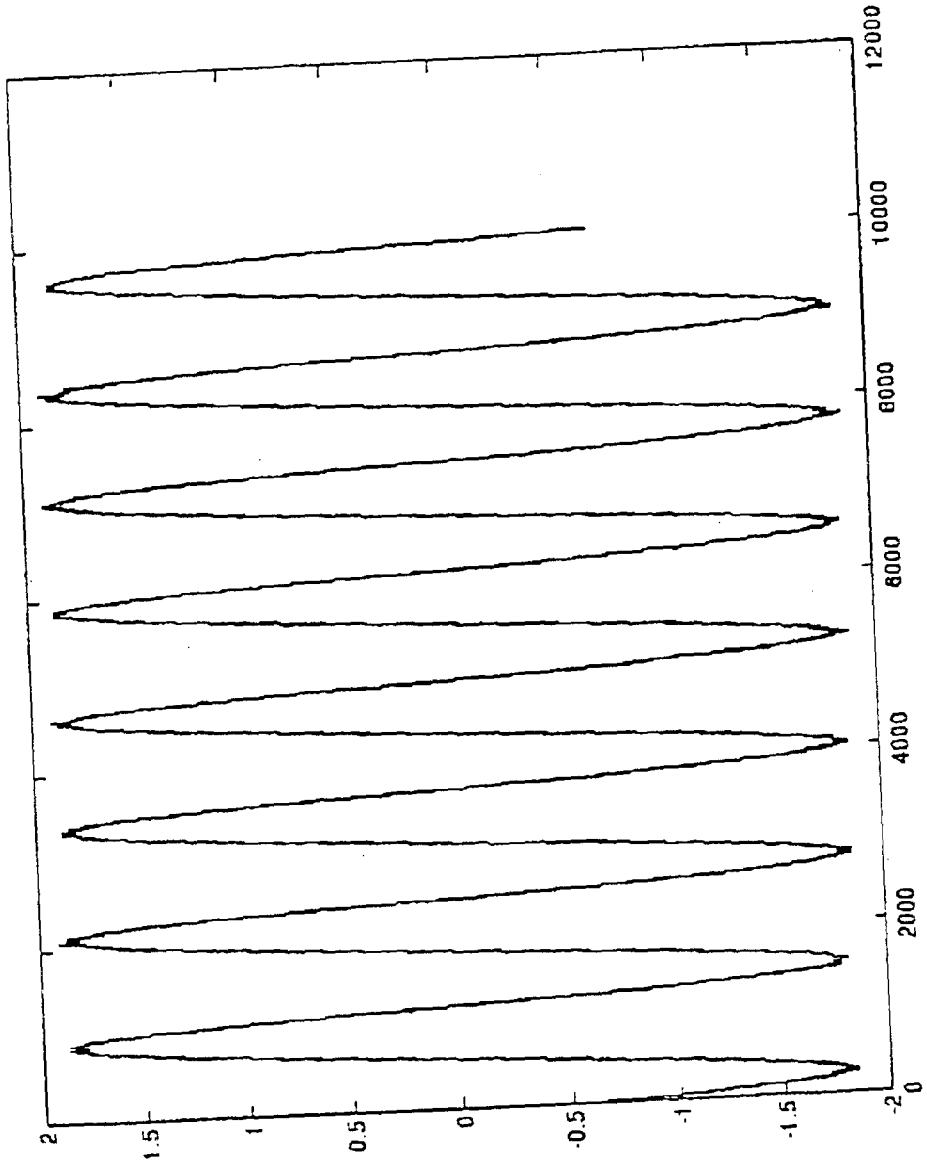


Fig. 3

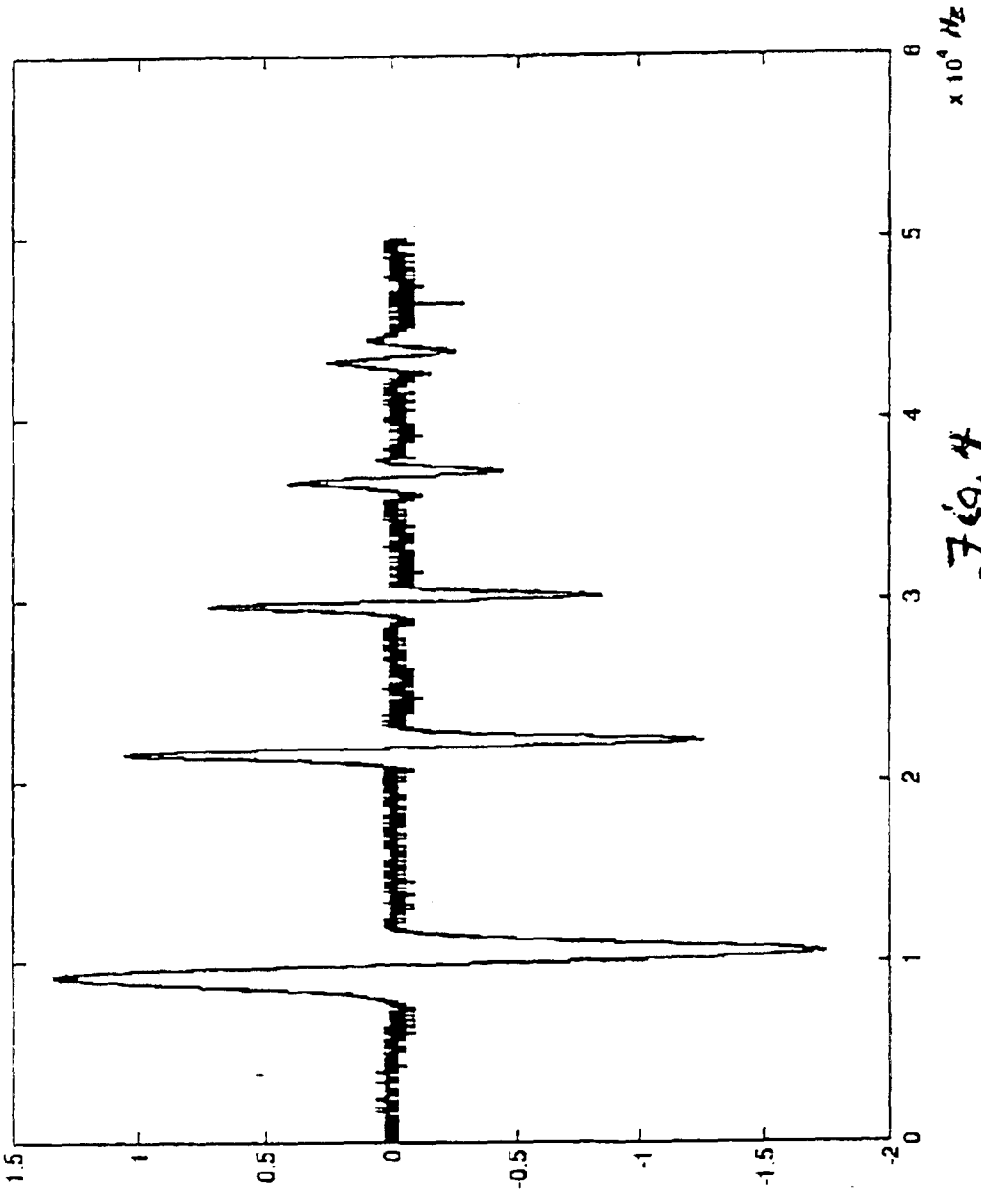


Fig. 4

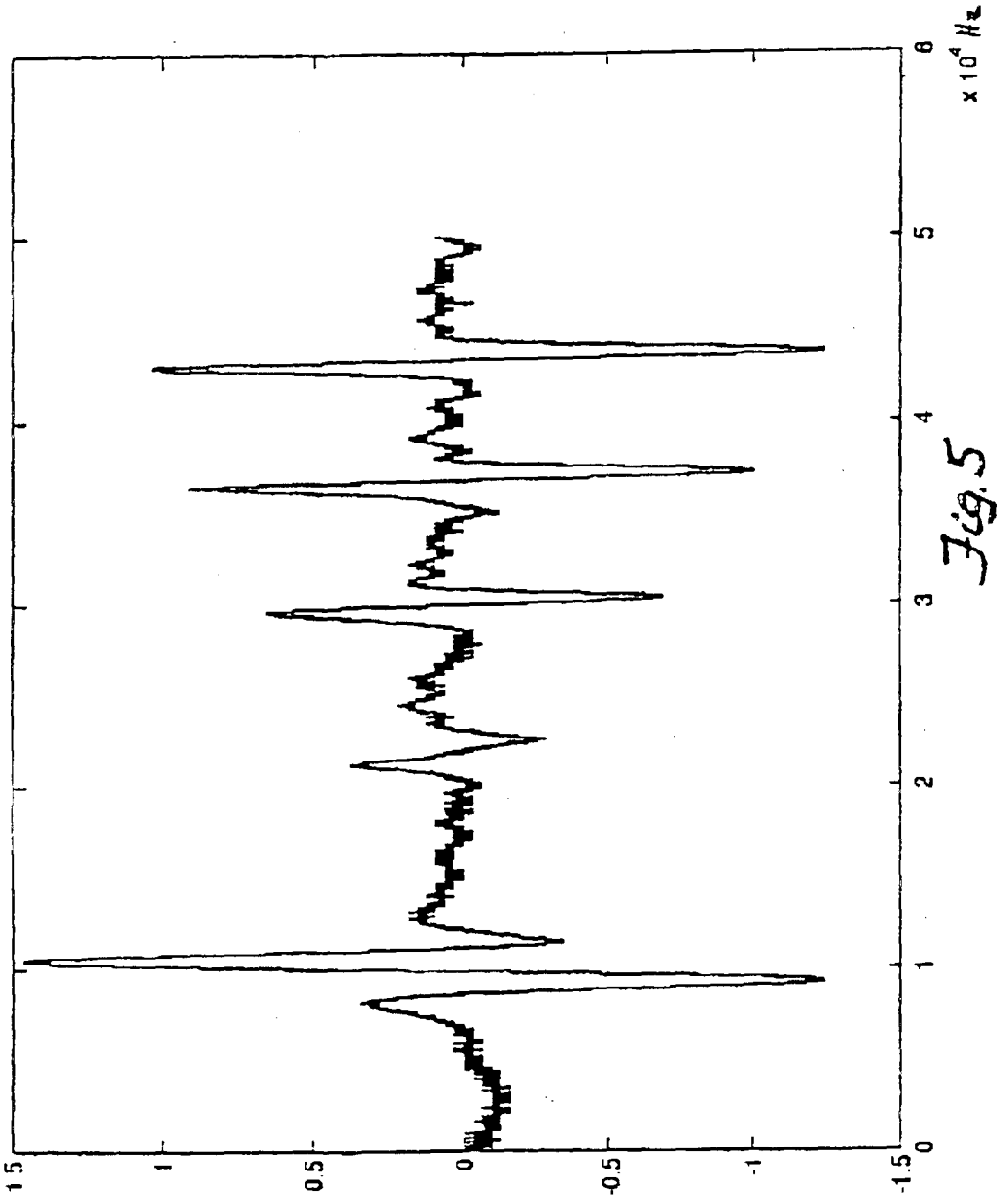


Fig. 5

DYNAMIC GAIN CONTROL IN A DIGITAL EDDY CURRENT SIGNAL PROCESSOR

This is a divisional application of that application filed Oct. 8, 2002 under Ser. No. 10/266,845, which is still pending.

BACKGROUND

1. Field of Technology

This invention relates to eddy current signal processing, and more particularly to digital extraction of an eddy current signal employing dynamic signal amplification and phase compensation.

2. Prior Art

When an eddy current probe is in the vicinity of a flaw in a material, such as a hole or a crack, the flaw will modulate a carrier signal introduced into the material from an alternating current in a coil in the eddy current probe.

It is known to extract the signal through digital signal processing. Generally, a digital oscillator generates a digital carrier signal and corresponding sine and cosine waves. The carrier is then converted to an analog signal, low-pass filtered, and then directed to a probe coil that generates an electromagnetic field that penetrates into a nearby material. An eddy current is generated in the material, which generates its own electromagnetic field that is detected by the probe coil. When the material is without flaws, the two electromagnetic fields are largely out of phase and the fields partially cancel. However, when a flaw exists in the material, the amplitude and phase of the second field are modified and a small detectable signal results, modulated on the return carrier signal. A programmable return signal amplifier optimizes the input range of the analog to digital converter where the signal is converted to a digital signal. The signal is then mixed, or multiplied, with the digital sine and cosine waves. The signals out of the multipliers contain sum and difference products of the mixed signals that contain the amplitude and phase information of the material flaw. Low-pass filters then apply to reject all but the difference frequencies. Then a direct current signal is subtracted from the eddy current signal to shift its axis to zero, which makes it easier to display on a screen.

As stated, the return signal amplifier is to optimize the input range of the analog to digital converter. In doing so, it is limited to scaling the maximum amplitude to the input range of the converter. Though this is an advantage in expanding the eddy current signal modulated on the carrier signal, the small eddy current signal in parts of the return signal other than near the signal maximum amplitude remains relatively small, possibly with insufficient resolution to exploit the information it contains or buried in signal noise below the quantization noise of the analog to digital converter.

SUMMARY

A digital synthesizer generates an electrical digital carrier that is converted to an analog signal and then driven to a probe coil. The coil generates an electromagnetic wave that propagates into a test material proximate the probe coil. A return electromagnetic wave generated by eddy currents in the material includes signatures of material defects modulated on the return carrier electromagnetic wave. The return wave is detected by one or more probe coils and amplified by a return signal amplifier. The signal is then again selectively amplified. That is, sections of the signal out of the return signal amplifier with relatively small amplitudes are again amplified to also exploit the range of the analog to digital converter. Sections of the signal with relatively large amplitudes are less amplified or passed through unchanged. The result is a signal that more fully exploits the range of the analog to digital converter throughout the signal, not just at the signal maximum amplitude. This more general amplification then amplifies the carrier signal and the eddy current signal on the carrier signal even at low signal amplitudes to effectively present the carrier signal and the eddy current signal for digitization with improved signal resolution.

When the signal is demodulated by mixing with the digital sine and cosine functions and low pass filter, only the eddy current signal remains. However, the resultant eddy current signal with the selective amplification yields a high resolution representation of the eddy current signal and signature of the material defect.

To make the selective amplification transparent to the signal analyst, the signal must be restored, while carrying the improved resolution of the defect signature. A bit shifter is used to attenuate the digital output signals by the same ratio that the selectable amplifier amplifies the signal prior to the analog to digital converter. This is achieved by recording the performance of the selective amplifier in a reference memory and reversing it after demodulation of the signal by effecting the bit shift. The digital signal is represented in a series of words having a word width in bits more than needed to fully express the signal amplitude. When the digital signal is bit shifted, it simply moves into previously unused bit places.

The bit shifter operates as a power of two multiplier when shifted to the left into unused bits and a divider when shifted to the right. Therefore, to consistently match the bit shifter, the selectable amplifier must generally also employ quantized steps of amplification in powers of two.

If the gain of the selectable amplifier were constant across the frequency range, then nothing else would need to be added to the digital eddy current signal processor. However, as is the case with any analog amplifier, the magnitude and phase of the selectable amplifier change with respect to frequency. Furthermore, the requirement for amplification in steps of powers of two is ideal. The actual ratio of amplification obtained in a real circuit does not exactly equal a power of two because the tolerance of the resistors in the circuit will cause the ratio to vary slightly. Also, the parasitic capacitance of the circuit board will cause the phase of the selectable amplifier to vary. Therefore in order to accomplish the goal of transparent gain switching, the gain and phase changes of the selectable amplifier must be compensated.

A phase offset is added to the digital synthesizer of the carrier wave to compensate for the phase change of the selectable amplifier. The phase-offset value is equal but opposite to the phase change of the selectable amplifier at the frequency generated by the phase accumulator. The phase change will vary with the gain setting of the selectable amplifier, therefore the phase-offset value will vary to correspond to the gain setting. The phase-offset value, calculated in a calibration procedure, may be zero when the gain setting is low and equal but opposite to the phase change of the selectable amplifier when the gain setting is high.

The gain variation of the selectable amplifier is compensated with a scaling stage after the demodulating mixers but before the low pass filters. The gain-scaling value that is used in the scaling stage is also calculated in the calibration procedure.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a circuit for digital signal processing of an eddy current signal.

FIG. **2** is an example of selective amplification of a signal. Because the carrier signal was generated as a sine wave, and the carrier signal modulation due to return magnetic fields generated by eddy currents is small, the carrier signal continues to appear as a sinusoid. It is the nature of eddy current signal processing to remove this large carrier signal to reveal the remaining modulation on the carrier due to eddy currents. Eddy current probes are often employed in a differential circuit with two signal returns subtracted to remove much of the carrier signal. Where the differential amplifier is successful in removing a large portion of the carrier signal, this signal may be small. Otherwise, the signal will remain large. In some single-ended probe types a differential amplifier cannot be used, in which case the full carrier signal is amplified. FIG. **2** shows in the first half of the figure a sinusoid carrier signal with amplitude equal to 1.0, representative of a small signal after the differential amplifier. The second half shows it with amplitude 4.0 after being amplified in the selective amplifier. If the signal size from the differential amplifier later increases, then the selectable amplifier may be returned to a gain of 1.0. In cases where the carrier is well rejected and the eddy current signal is large, the signal may rise above and fall below a threshold at which the gain of the selectable amplifier is switched. In this case, the reate at which the selectable gain is switched is fully dependent upon the frequency characteristics of the eddy current signal and it is independent of the carrier signal frequency.

FIG. **3** illustrates a simple sinusoidal carrier with a relatively small and unnoticeable eddy current signal after amplification.

FIG. **4** and FIG. **5** are in-phase and quadrature components of an actual standard eddy current signal after it has been demodulated from the carrier signal of FIG. **3**, derived by moving a probe through a tube that has some standard eddy current flaw signals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention comprises a digital eddy current signal processing method and electronic circuit employing a dynamic gain control on signal amplification.

A phase accumulator **8** generates a linearly-increasing phase by iteratively adding an increment value to the current phase value. When the phase value exceeds the maximum value that can be expressed in the phase accumulator (2^N–1, where N is the number of bits in the phase accumulator), the overflow bit is simply discarded and the phase accumulator continues incrementing. The phase accumulator values represent a phase range from zero to 360 degrees. Larger increment values cause the phase accumulator to sweep through its range more frequently, thus generating higher frequencies. Therefore, the phase accumulator determines the frequency of synthesized carrier waves and sine and cosine waves.

A digital synthesizer **10** produces three digital sine waves **12**, **14**, and **16** from the phase output of the phase accumulator **8** that all have the same frequency, two of which are separated in phase by ninety degrees, establishing sine and cosine waves **12** and **14**. The third wave **16** is the carrier sine wave, which has variable amplitude and phase relative to the sine and cosine waves.

The carrier signal **16** passes through a low-pass filter **18** and is driven to eddy current probe **20**, which transmits an electromagnetic wave **22** into material **100** proximate the probe **20**, generating eddy currents in the material. Defects in the material cause amplitude and phase differences in a return electromagnetic wave **24** generated by the eddy currents. The phase differences, or equivalently frequency changes, constitute a signature of the defects as a modulation of the return wave. The probe detects the return electromagnetic wave **24**, now a modulated input carrier signal **17**, through one or more probe coils. A first analog amplifier **26** amplifies the return signal from the probe. The first analog amplifier **26** typically includes an adjustable gain value that scales the return signal maximum amplitude to the input range of the analog-to-digital converter **28**. A second analog amplifier **23**, a selectable amplifier under computer control or user control, selectively scales the signal in sections to optimize the respective sections of the signal to the input range of the analog-to-digital converter **28**.

After amplification, an analog-to-digital converter **28** digitizes the modulated input carrier signal **17**, the digitizing rate determined by digital control logic. If the signal is digitized prior to amplification, the amplifier is also digital.

A digital mixer **30** demodulates the signal from the carrier signal **16**. Digital sine and cosine waves **12** and **14** from the synthesizer **10** mathematically multiply digital input samples of the carrier signal **16** from the analog to digital converter **28** in the digital mixer **30**. Multiplication by the sine and cosine waves creates in-phase and quadrature outputs useful for maintaining amplitude and phase information contained in the modulated input carrier signal **17** and a single-sideband complex translation of the real part of the modulated carrier wave **17**. Unlike analog mixers, which also generate many unwanted mixer products, the digital mixer produces only sum and difference frequency signals without harmonics of the two signals.

A gain scaling stage **31** occurs after the demodulation stage as a fine adjustment to the gain introduced by the selectable filter to adjust for small differences between a desired amplification and the actual resulting amplification. In the scaling stage, each component of the eddy current signal is multiplied by a gain-scaling value. The gain-scaling value is equal to the desired gain ratio (a power of two) of the selectable amplifier divided by the actual (observed) gain ratio. In mathematical terms, the gain-scaling value is

$$G_C = \frac{G_H \cdot G'_L}{G_L \cdot G'_H}$$

where G_H/G_L is the desired gain ratio of the selectable amplifier, and G'_L/G'_H is the ratio of the actual low gain of the selectable amplifier **23** to its actual high gain at the frequency of the phase accumulator. The actual gain ratio is calculated via a calibration procedure. The value G_C is applied to the scaling multipliers in the gain scaling stage **31** when the high gain setting is selected in the selectable amplifier. The value 1.0 is applied to the scaling multipliers when the low gain setting is selected. For each treated signal section, both values are stored in reference memory **36**.

To correct for phase changes of the selectable amplifier, controller **25** directs a phase offset **37** to adjust phase from the phase accumulator **8** before it outputs to the digital carrier synthesizer. The controller **25** examines the size of the digital signal from the analog to digital converter to determine and set the gain of the selectable amplifier. If the controller chooses a low gain (because the signal is large), then it also sets the phase offset **37** to zero degrees and the gain scaling value to 1.0. If the controller chooses a high gain for the selectable amplifier (because the signal is small), then it sets the phase offset **37** to be equal and opposite the

phase change of the selectable amplifier, and it sets the gain scaling value to G_C. The controller also directs the bit shifter **35** to right-shift the quadrature eddy current signals when it chooses the high gain of the selectable amplifier. A computer **27** calculates the values of the phase offset and the gain scaling in a calibration procedure, which is an algorithm that is programmed into the computer.

While executing the calibration procedure, the computer **27** recognizes amplitude and phase discontinuities after the bit shifter and dictates adjustments in the gain scaling value and the phase offset value. The computer **27** communicates the adjusted values to the controller, which communicates them to the gain scaling stage **31**, and to the phase offset stage **37**. Then the controller sets the selectable amplifier **23** and bit shifters **35** accordingly in order to remove amplitude and phase discontinuities.

Decimating low-pass filters **32** then reject all but the difference frequencies, which together comprise the eddy current signal, effectively translating frequencies in the input signal to lower frequencies. With higher frequencies no longer present, the signal can be represented by a much smaller data sample in keeping with the Nyquist sampling theorem (any signal can be represented by discrete samples if the sampling rate is at least twice the bandwidth of the signal).

Following the decimating low-pass filters **32** is a digital direct current null circuit **34**. To conveniently center the eddy current signal at zero so that it appears at the center of a display, the direct current value of the eddy current signal, which is stored in a reference memory **36**, is subtracted from all signals that follow. The direct current reference signal is one of the outputs of the decimating low-pass filters **32**. The reference memory **36** is queried for the direct current reference signal, which is then output and summed (subtracted) from the signal from the decimating low-pass filters. With the eddy current signal thus demodulated from the carrier wave **16** and centered about zero, it is available for display and analysis.

The bit shifter **35** reverses the sectional amplitude gain of the selectable amplifier **23** by shifting the bits in the signal words to the right to correspond with the gain applied by the selectable amplifier **23**. Because each bit shift amounts precisely to a division by two the resultant signature will not be an exact reversal of the gain of selectable amplifier **23** although might be set to amplify the signal from the first amplifier by a power of two. Any real amplifier will not have a gain exactly equal to a power of two across the required frequency range (10 Hz to 10 MHz). This happens due to circuit performance shortcomings, such as electronic component drift from age or temperature, the variation of resistor values and the parasitic capacitances that exist on circuit boards. Therefore, a fine-tuning digital gain stage **31** is introduced after the multipliers **30** to trim the gain of the signal so the combination of the selectable amplifier and the digital gain stage results in an overall gain exactly equal to a power of two. Then the bit shifter **35** divides by the same power of two after the filters. Therefore, the combination of the selective amplification and the bit shifting is transparent to later signal analysis.

What is claimed is:

1. A method of amplifying an analog signal as it is being converted to a digital signal so as to exploit the range of an analog-to-digital converter throughout the signal through dynamic gain control, comprising the following steps:

a. First, amplifying the signal;

b. Second, selectively amplifying segments of the signal;

c. Digitizing said signal;

d. Adjusting amplification achieved in selectively amplifying segments of the carrier signal in a gain scaling stage such that resulting amplification of said signal segments is a power of two;

e. Analyzing said amplified signal;

f. Reversing said selective amplification of said signal segments selectively amplified by shifting bits in a digital representation of the signal.

2. A method of extracting a small signal modulated on an analog carrier signal in a digital circuit, comprising the following steps:

a. In an electrical circuit, synthesizing digital sine and cosine functions;

b. Amplifying the analog carrier signal to a maximum amplitude of an input range of an analog-to-digital converter;

c. Selectively amplifying segments of the analog carrier signal by employing a amplifier under control of a computer that selectively scales the signal in sections by optimizing respective sections of the signal to the input range of the analog-to-digital converter;

d. Digitizing said analog carrier signal into a digital carrier signal with the analog to digital converter;

e. Mixing said digital carrier signal with said digital sinusoidal functions into quadrature components;

f. Adjusting amplification achieved in selectively amplifying segments of the carrier signal in a gain scaling stage such that a resulting amplification of said signal segments is a power of two, a controller directing gain adjustment after examining the size of a digital signal from the analog to digital converter in order to set the gain of the amplifier, and wherein the controller sets the gain scaling value to

$$G_C = \frac{G_H \cdot G'_L}{G_L \cdot G'_H}$$

where G_H/G_L is a desired gain ratio of a selectable amplifier, and G'_L/G'_H is the ratio of the actual low gain of the amplifier to its actual high gain at a frequency of a phase accumulator;

g. Isolating the small signal by filtering said mixed digital carrier signal with a low-pass filter;

h. Reversing said amplification of said signal segments selectively amplified by the controller setting the amplifier and a bit shifter to remove amplitude and phase discontinuities, the bit shifter shifting bits in a digital representation of the carrier signal, a computer calculating values of a phase offset and the gain scaling in a calibration algorithm programmed into the computer, said algorithm recognizing amplitude and phase discontinuities after the bit shifter and dictating adjustments in the gain scaling value and the phase offset value, the computer communicating the adjustments to the controller, which communicates them to the gain scaling and phase offset stage.

3. The method of claim **2** further including the step of adjusting a phase of the digital carrier signal before it is converted to analog correcting for unwanted phase changes to the carrier signal that occur in the amplifier by a controller directing introduction of a phase offset, if the controller chooses a low gain because the signal is large, then including the step of the controller also setting the phase offset to zero degrees and the gain scaling value to 1.0, but if the controller sets a high gain for the amplifier because the signal is small, then including the step of the controller also setting the phase offset to be equal and opposite the phase change of the amplifier.

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