ORIGINAL

GLENN W. TROST (State Bar No. 116203)
COUDERT BROTHERS
333 South Hope Street, 23rd Floor
Los Angeles, California 90071
tel: (213) 229-2900
fax: (213) 229-2999

DAVID E. KILLOUGH (SBN 110719)
O'MELVENY & MYERS LLP
275 Battery Street
San Francisco, California 94111-3305
tel: (415) 984-8700
fax: (415) 984-8701

SAMUEL H. WEINER
OSTROLENK, FABER, GERB & SOFFEN
1180 Avenue of the Americas
New York, NY 10036
tel: (212) 382-0700
fax: (212) 382-0888

Attorneys for Plaintiff International Rectifier Corporation

FILED
2000 JUN 22 PM 3:40
CLERK, U.S. DISTRICT COURT
CENTRAL DIST. OF CALIF.
LOS ANGELES
BY

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

INTERNATIONAL RECTIFIER CORPORATION, **PLAINTIFF,** **VS.** **IXYS CORPORATION, AND DOES 1-10,** **DEFENDANTS.**	Case No. 00-06756 MMM(BQRx) **COMPLAINT FOR DAMAGES AND INJUNCTIVE RELIEF (PATENT INFRINGEMENT); DEMAND FOR JURY TRIAL**

ENTERED ON ICMS
JUN 27 2000
CV

For its Complaint, plaintiff International Rectifier Corporation ("IR") avers as follows:

06/22/00 3:47:59 PM
LA 4-2 GIN Receipt # 061902
======NO REFUND WITHOUT RECEIPT======
CASE #
00-6756

086900 Filing Fee Civil
60.00
510000 Special Fund F/F
90.00
===== T O T A L =======
150.00
CHECK TENDERED $ $150.00
======NO REFUND WITHOUT RECEIPT======

JURISDICTION AND VENUE

1. The claims alleged below are brought under the Patent Laws of the United States, 35 U.S.C. §§ 1 et seq. This Court has jurisdiction over these claims pursuant to 28 U.S.C. §§ 1338(a). Venue is based on 28 U.S.C. §§ 1391(b), 1391(c), 1391(d) and 1400(b).

PARTIES

2. IR is a corporation duly organized and existing under the laws of the State of Delaware, with its corporate headquarters and principal place of business within the Central District of California at 233 Kansas Street, El Segundo, California 90245.

3. IR is informed and believes, and on that basis alleges, that defendant IXYS Corporation ("IXYS") is a corporation organized under the laws of the State of Delaware, doing business in this District, *inter alia*, through its Sales Representative, Select Electronics, in Santa Ana, California.

4. The true names and/or culpabilities of defendant DOES 1-10 are unknown to IR at this time. IR is informed and believes, and on that basis alleges, that DOES 1-10, as more fully alleged below, as well as the other defendants, are legally responsible for the occurrences, acts and wrongs alleged herein and for the damages to IR proximately caused thereby. In particular, IR is informed and believes, and on that basis alleges, that IXYS relies on sales representatives and distributors, including DOES 1-10, to sell devices in this District and elsewhere within the United States, where such devices practice one or more of the claims (or are made by one or more of the claimed processes) of the patents identified below. Such sales are direct infringements of the patents in suit. IR will amend this Complaint to correctly identify any DOE defendant whose identity and culpability is made known to IR.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

FIRST CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 4,959,699)

5. IR is and has been the owner by mesne assignment of United States Letters Patent No. 4,959,699 (the "'699 patent"), which issued September 25, 1990 (Reexamination Certificates issued October 12, 1993 and January 19, 1999), for HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE. A copy of the '699 patent, together with its reexamination certificates, is attached hereto as Exhibit A.

6. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '699 patent (including, but not limited to, Claim 1 of the '699 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is further informed and believes, and on that basis alleges, that this infringement will continue unless and until enjoined by this Court.

7. IR has notified IXYS of its infringement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

SECOND CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 5,008,725)

8. IR is and has been the owner by mesne assignment of United States Letters Patent No. 5,008,725 (the "'725 patent") which issued April 16, 1991 (Reexamination

1 certificate issued January 12, 1993), for PLURAL POLYGON SOURCE PATTERN FOR
2 MOSFET. A copy of the '725 patent, together with its reexamination certificate, is
3 attached hereto as Exhibit B.
4
5 9. IR is informed and believes, and on that basis alleges, that (a) IXYS has made,
6 used, sold or offered for sale in this District and elsewhere in the United States articles
7 (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50,
8 IXFH35N30, and IXTH24N50) infringing the '725 patent (including, but not limited to,
9 Claims 3, 7 and 8 of the '725 patent) and (b) DOES 1-10 have in this District and elsewhere
10 in the United States sold and offered for sale such articles. IR is further informed and
11 believes, and on that basis alleges, that this infringement will continue unless and until
12 enjoined by this Court.
13
14 10. IR has notified IXYS of its infringement, which has been and continues to be
15 willful and deliberate. IR has been and continues to be damaged by the above-alleged
16 infringement and will suffer irreparable harm until such time as that infringement is
17 enjoined.
18
19 **THIRD CLAIM FOR RELIEF**
20 **(Against All Defendants For Patent Infringement, U.S. Patent No. 5,130,767)**
21
22 11. IR is and has been the owner by mesne assignment of United States Letters
23 Patent No. 5,130,767 (the "'767 patent"), which issued July 14, 1992, for PLURAL
24 POLYGON SOURCE PATTERN FOR MOSFET. A copy of the '767 patent is attached
25 hereto as Exhibit C.
26
27 12. IR is informed and believes, and on that basis alleges, that (a) IXYS has made,
28 used, sold or offered for sale in this District and elsewhere in the United States articles

(including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '767 patent (including, but not limited to, Claims 3, 5 and 7 of the '767 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is further informed and believes, and on that basis alleges, that this infringement will continue unless and until enjoined by this Court.

13. IR has notified IXYS of its infringement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

FOURTH CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 4,642,666)

14. IR is and has been the owner by mesne assignment of United States Letters Patent No. 4,642,666 (the "'666 patent"), which issued February 10, 1987 (Reexamination Certificate issued October 27, 1998), for HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE. A copy of the '666 patent, together with its reexamination certificate, is attached hereto as Exhibit D.

15. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '666 patent (including, but not limited to, Claim 1 of the '666 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

16. IR notified IXYS of its infringement, which was willful and deliberate. IR has been damaged by the above-alleged infringement.

FIFTH CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 4,705,759)

17. IR is and has been the owner by mesne assignment of United States Letters Patent No. 4,705,759 (the "'759 patent"), which issued November 10, 1987, (Reexamination Certificate issued February 14, 1995), for HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE. A copy of the '759 patent, together with its reexamination certificate, is attached hereto as Exhibit E.

18. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '759 patent (including, but not limited to, Claim 1 of the '759 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is further informed and believes, and on that basis alleges, that this infringement will continue unless and until enjoined by this Court.

19. IR has notified IXYS of its infringement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

Wherefore, International Rectifier prays for judgment as follows:

1. For a preliminary and permanent injunction against infringement of the '699 patent;

2. For an award of actual damages sustained by IR (but no less than a reasonable royalty) as a result of infringement of the '699 patent;

3. For a preliminary and permanent injunction against infringement of the '725 patent;

4. For an award of actual damages sustained by IR (but no less than a reasonable royalty) as a result of infringement of the '725 patent;

5. For a preliminary and permanent injunction against infringement of the '767 patent;

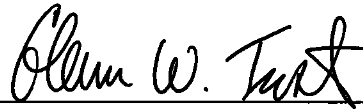
6. For an award of actual damages sustained by IR (but no less than a reasonable royalty) as a result of infringement of the '767 patent;

7. For an award of actual damages sustained by IR (but no less than a reasonable royalty) as a result of infringement of the '666 patent;

8. For a preliminary and permanent injunction against infringement of the '759 patent;

9. For an award of actual damages sustained by IR (but no less than a reasonable royalty) as a result of infringement of the '759 patent;

10. For treble damages under 35 U.S.C. § 285;

1 11. For IR's attorneys fees and costs incurred in prosecution of this action under,
2 *inter alia*, 35 U.S.C. § 285; and
3
4 12. For such other and further relief as this Court may deem just and proper.
5
6 Dated: June 22, 2000 **COUDERT BROTHERS**
7 **O'MELVENY & MYERS LLP**
8 **OSTROLENK, FABER, GERB & SOFFEN**
9
10 By: 
11
Attorneys for Plaintiff International Rectifier Corporation
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

DEMAND FOR JURY TRIAL

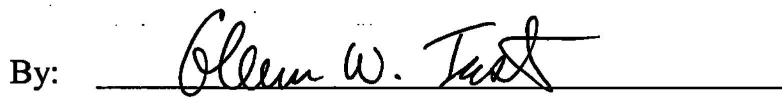
Plaintiff International Rectifier Corporation hereby demands trial by jury.

Dated: June 22, 2000

COUDERT BROTHERS

O'MELVENY & MYERS LLP

OSTROLENK, FABER, GERB & SOFFEN

By: 

Attorneys for Plaintiff International Rectifier Corporation

United States Patent [19]
Lidow et al.
[11] Patent Number: 4,959,699
[45] Date of Patent: Sep. 25, 1990

[54] **HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE**

[75] Inventors: Alexander Lidow, Manhattan Beach; Thomas Herman, Redondo Beach, both of Calif.

[73] Assignee: International Rectifier Corporation, El Segundo, Calif.

[21] Appl. No.: 371,678

[22] Filed: Jun. 22, 1989

Related U.S. Application Data

[60] Continuation of Ser. No. 90,664, Aug. 27, 1987, abandoned, which is a division of Ser. No. 456,813, Jan. 10, 1983, abandoned, which is a division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] Int. Cl.[5] H01L 29/68; H01L 29/10; H01L 27/02

[52] U.S. Cl. 357/23.7; 357/23.8; 357/23.4; 357/41; 357/43

[58] Field of Search 357/23.7, 23.8, 23.4, 357/41, 43, 86

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,271,640 9/1966 Moore .
3,319,311 5/1967 Mutter .
3,458,781 7/1969 Simon .
3,461,360 8/1969 Barson et al. .

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

2136509 11/1972 Fed. Rep. of Germany .
5046081 8/1973 Japan .
48-40814 12/1973 Japan .
51-85381 7/1976 Japan .
52-23277 2/1977 Japan .
52-42080 4/1977 Japan .
52-106688 9/1977 Japan .

(List continued on next page.)

OTHER PUBLICATIONS

I. Yoshida et al., "A High Power MOSFET with a Vertical Drain Electrode and a Meshed Gate Structure," IEEE Journal of Solid-State Circuits, vol. SC-11 #4, Aug. 1976, pp. 472-477.
J. Plummer et al., "A Monolithic 200-V CMOS Analog Switch," IEEE Journal of Solid-State Circuits, vol. SC-11 #6, Dec. 1976, pp. 809-817.
B. Scharf et al., "A MOS-Controlled Triac Device," 1978 IEEE International Solid-State Circuits Conference, San Francisco, Calif., Feb. 15-17, 1978, pp. 222-223.
K. Lisiak et al., "Optimization of Non-Planar Power MOS Transistors," IEEE Transactions on Electron Devices, vol. Ed-25 #10, Oct. 1978, pp. 1229-1234.
H. Sigg et al., "D-MOS Transistor for Microwave

(List continued on next page.)

Primary Examiner—Rolf Hille
Assistant Examiner—Fetsum Abraham
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

24 Claims, 5 Drawing Sheets

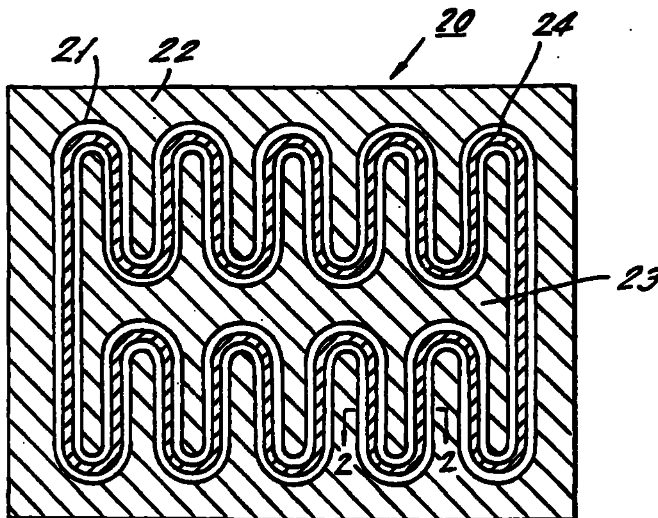


FIG. 1

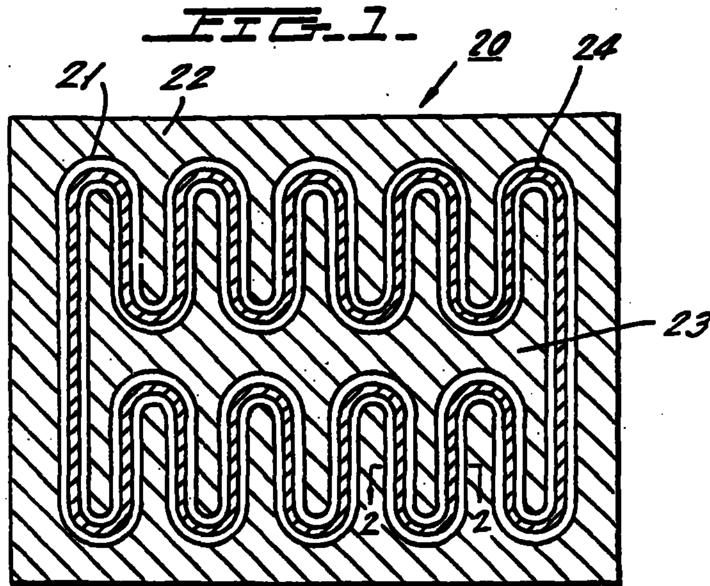
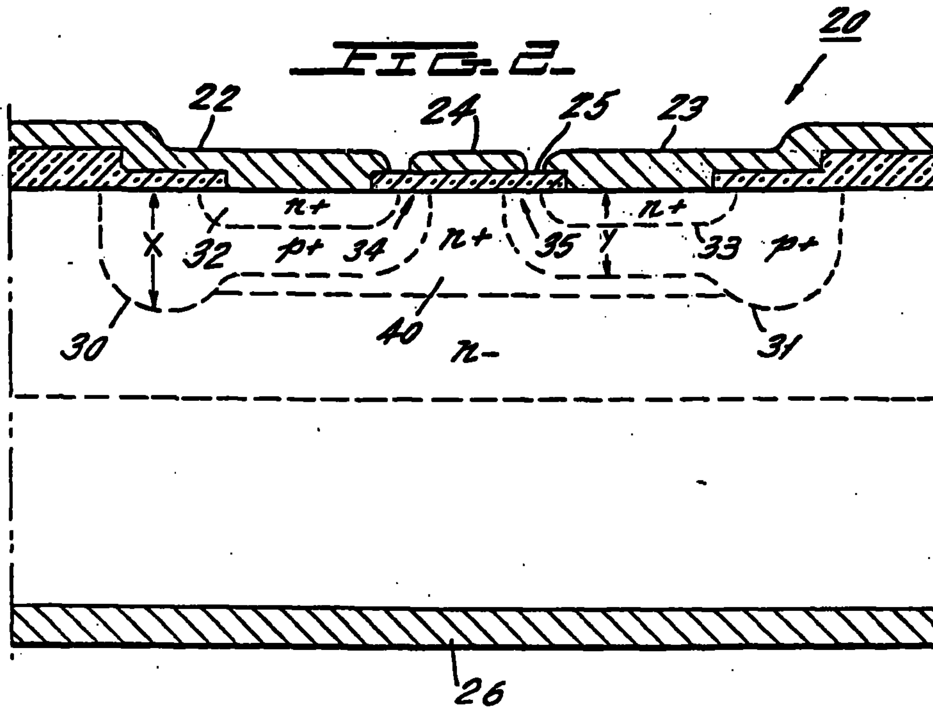


FIG. 2



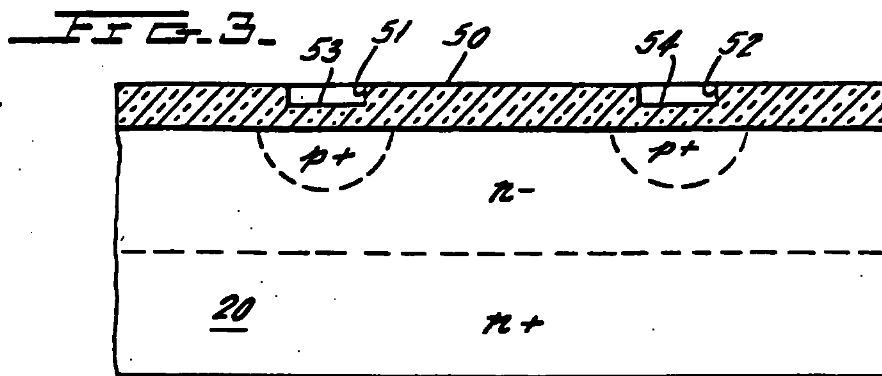


FIG. 3
53
51
50
54
52
p+
p+
n-
20
n+

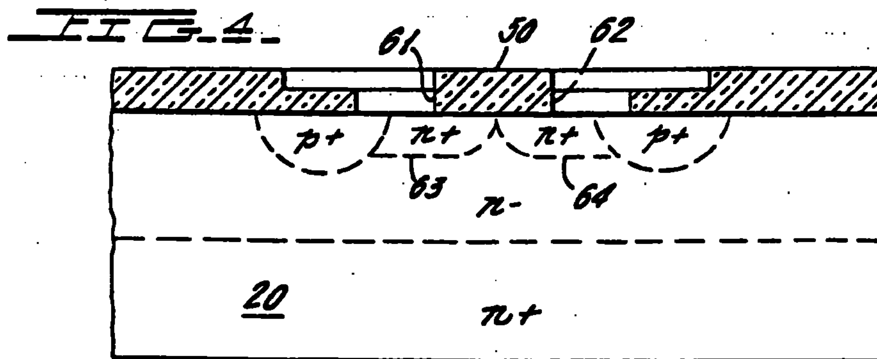


FIG. 4
61
50
62
p+
n+
n+
p+
63
n-
64
20
n+

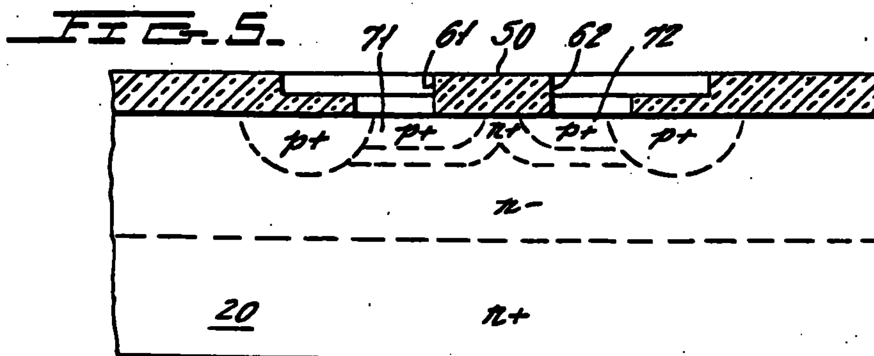


FIG. 5
71
61
50
62
72
p+
p+
n+
p+
p+
n-
20
n+

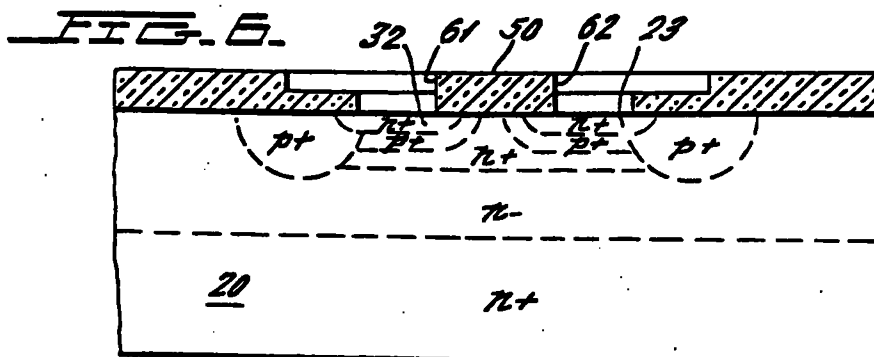


FIG. 6
32
61
50
62
23
p+
n+
p+
p+
n-
20
n+

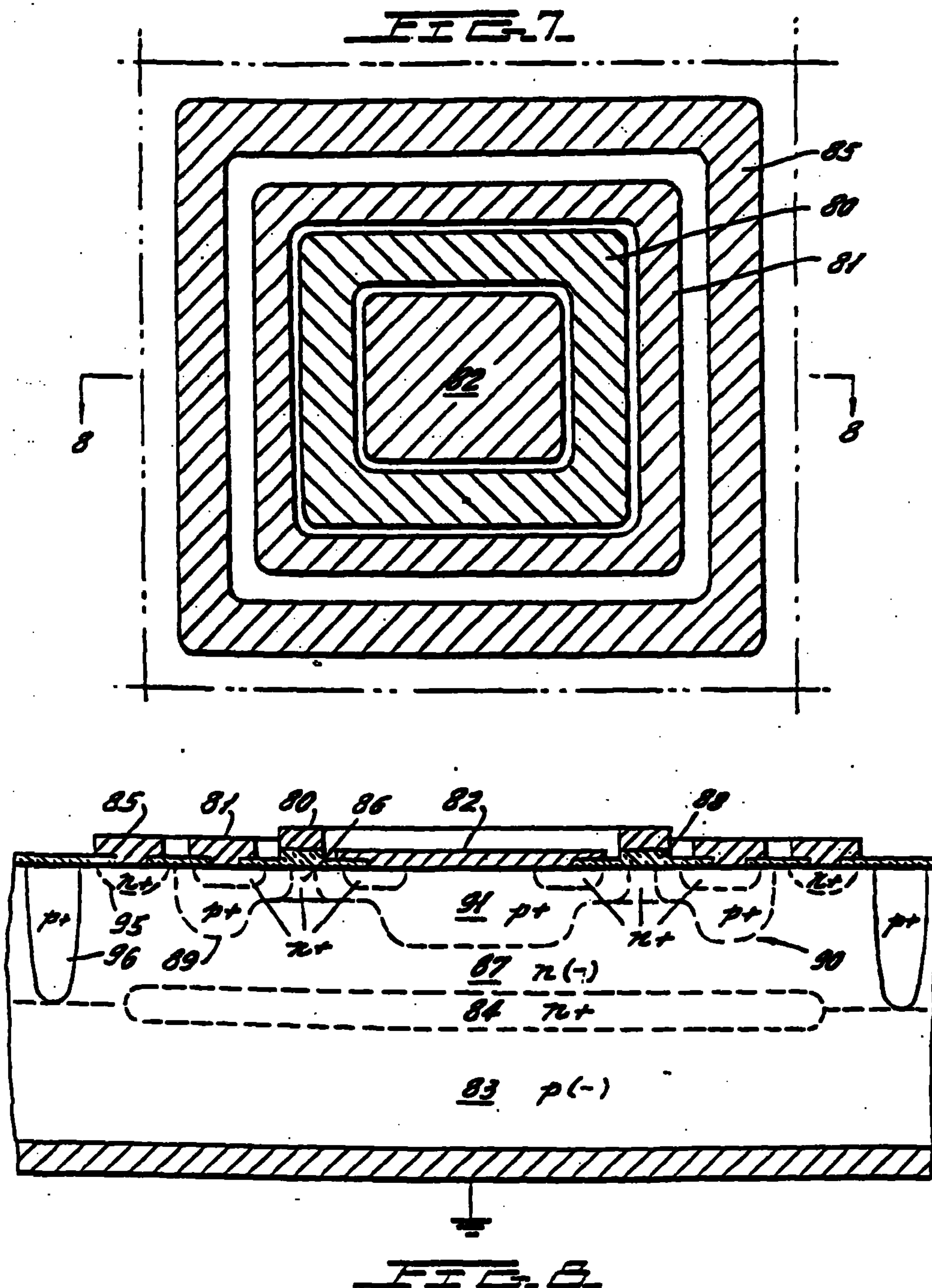


FIG. 7
85
80
81
82
8
8
85
81
80
86
82
88
n+
p+
p+
95
96
89
n+
91
p+
n+
p+
n+
p+
p+
90
87
n(-)
84
n+
83
p(-)
FIG. 8

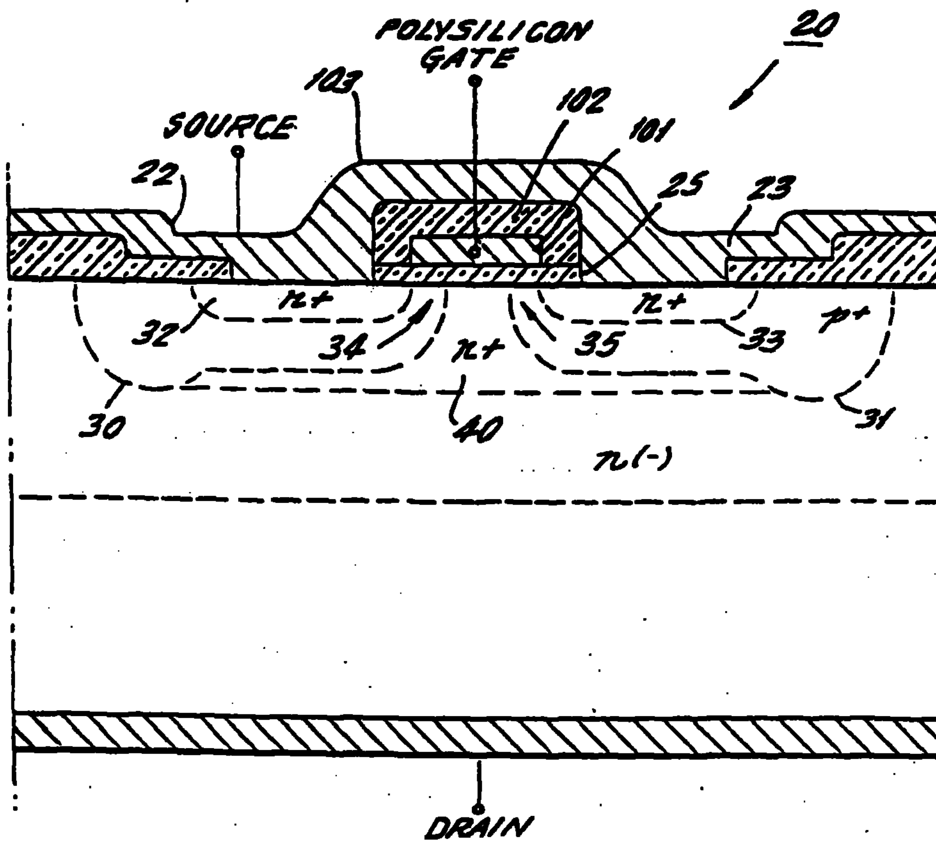


FIG. 8a

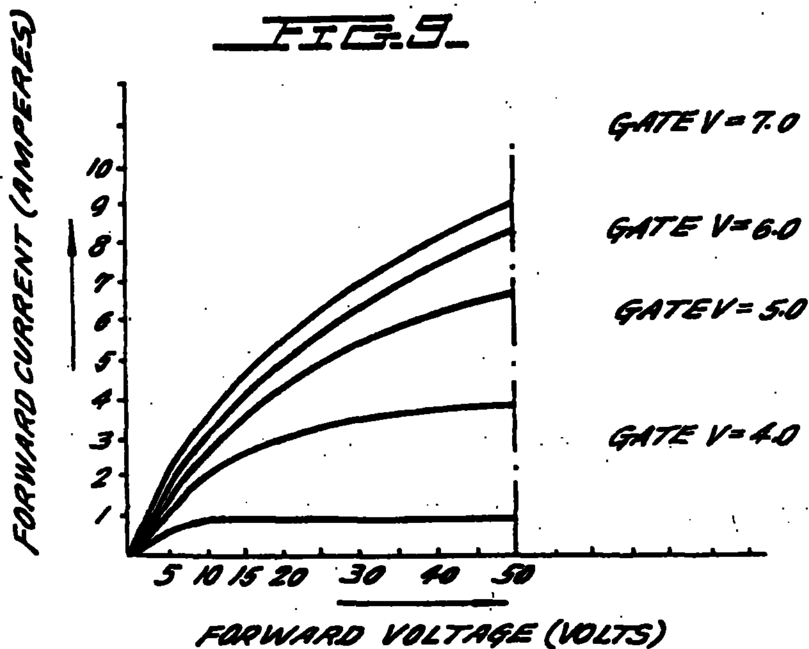


FIG. 9
GATE V=7.0
GATE V=6.0
GATE V=5.0
GATE V=4.0
FORWARD CURRENT (AMPERES)
1
2
3
4
5
6
7
8
9
10
5 10 15 20 30 40 50
FORWARD VOLTAGE (VOLTS)

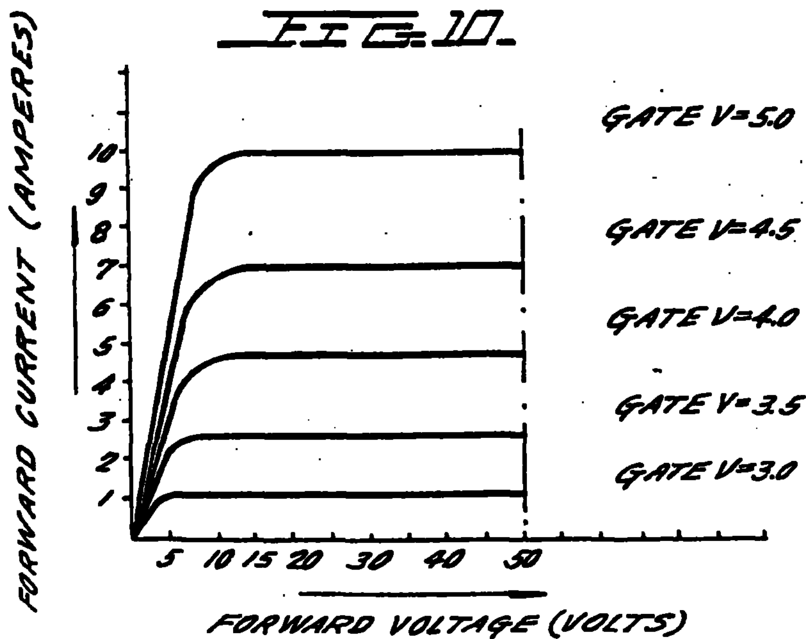


FIG. 10
GATE V=5.0
GATE V=4.5
GATE V=4.0
GATE V=3.5
GATE V=3.0
FORWARD CURRENT (AMPERES)
1
2
3
4
5
6
7
8
9
10
5 10 15 20 30 40 50
FORWARD VOLTAGE (VOLTS)

HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

This is a continuation of application Ser. No. 07/090,664 filed on Aug. 27, 1987, now abandoned, which is a division of application Ser. No. 456,813, filed Jan. 10, 1983 now abandoned which in turn, is a division of application Ser. No. 232,713, filed Feb. 9, 1981, now U.S. Pat. No. 4,376,286, issued Mar. 8, 1983 which, in turn, is a continuation of application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices and more specifically relates to a novel structure for a MOSFET device which permits it to be used in high power applications with a relatively high reverse voltage and with an exceptionally low on-resistance. The major advantage of the bipolar transistor over the MOSFET transistor is that the bipolar transistor has a very low on-resistance per unit conductive area. The MOSFET transistor has numerous advantages over the bipolar transistor including very high switching speed, very high gain and lack of the secondary breakdown characteristics exhibited by a minority carrier device. However, because the MOSFET transistor has high on-resistance, its use in high power switching applications has been limited.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device which has a low forward resistance so that the device becomes more competitive with bipolar devices in a switching type application while retaining all of the numerous advantages of the MOSFET over the bipolar device. In particular, with the present invention, the forward resistance per unit area of the device has been reduced by at least a factor of two, compared to the limiting resistance per unit area previously existing in a MOSFET-type device.

In one embodiment of the invention, two sources are placed on the same surface of a semiconductor wafer and are laterally spaced from one another. A gate electrode, deposited on a conventional gate oxide, is disposed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced from one another by an n-type bulk region. Current from each source can flow through its respective channel (after the creation of the inversion layer defining the channel), so that majority carrier conduction current can flow through the bulk region and across the wafer or chip to the drain electrode. The drain electrode may be on the opposite surface of the wafer or on a laterally displaced surface region from the source electrodes. This configuration is made using the desirable manufacturing techniques of the D-MOS device, which permits precise alignment of the various electrodes and channels and permits use of extremely small channel lengths. While the above configuration may have been previously described for a MOSFET signal-type device, the structure is not that of the commonly used signal MOSFET.

The device is basically formed in an n(−) substrate which has the relatively high resistivity which is necessary to obtain the desired reverse voltage capability of the device. For example, for a 400 volt device, the n(−) region will have a resistivity of about 20 ohm-centimeters. However, this same necessary high resistivity characteristic has caused the on-resistance of the MOSFET device, when used as a power switch, to be relatively high.

In accordance with the present invention, it has been found that in the upper portion of the central bulk region to which the two inversion layers feed current in the path to the drain electrode, the central region immediately beneath the gate oxide can be a relatively low resistivity material formed, for example, by an n(+) diffusion in that channel region, without affecting the reverse voltage characteristics of the device.

More specifically, and in accordance with the invention, this common channel will have an upper portion beneath the gate oxide and a lower bulk portion extending toward the drain electrode. The lower portion has the high resistivity desired to produce high reverse voltage ability, and will have a depth dependent on the desired reverse voltage for the device. Thus, for a 400 volt device, the lower n(−) region may have a depth of about 35 microns, while for a 90 volt device it will have a depth of about 8 microns. Other depths will be selected, depending on the desired reverse voltage of the device to provide the necessary thicker depletion region required to prevent punch-through during reverse voltage conditions. The upper portion of the common channel is made highly conductive (n+) to a depth of from about 3 to about 6 microns. It has been found that this does not interfere with the reverse voltage withstand ability of the device. However, it decreases the on-resistance per unit area of the device by more than a factor of two. The resulting device becomes competitive with conventional high power bipolar switching devices since it retains all of the advantages of the MOSFET device over the bipolar device but now has the relatively low forward resistance which was the major characterizing advantage of the bipolar device.

In accordance with another feature of the present invention, the p-type region which defines the channel beneath the gate oxide has a relatively deeply diffused portion beneath the source so that the p-type diffusion region will have a large radius of curvature in the n(−) epitaxial layer forming the body of the device. This deeper diffusion or deeper junction has been found to improve the voltage gradient at the edge of the device and thus permits the use of the device with higher reverse voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a high power MOSFET chip which incorporates the present invention and particularly illustrates the metalizing patterns of the two sources and the gate.

FIG. 2 is a cross-sectional view of FIG. 1 taken across the section line 2—2 in FIG. 1.

FIG. 3 is a cross-sectional view similar to FIG. 2 showing the initial step in the process of manufacture of the chip of FIGS. 1 and 2 and particularly shows the p(+) conductivity implant and diffusion step.

FIG. 4 shows the second step in the manufacturing process and shows the n(+) implant and diffusion step.

FIG. 5 shows a further step in the process of manufacture of the chip of FIGS. 1 and 2 and shows the channel implant and diffusion step.

FIG. 6 shows a further step in the process of manufacture and illustrates the source predeposition and diffusion step. This precedes the last step in which the

gate oxide is cut for the metalization step which produces the device of FIG. 2.

FIG. 7 is a plan view of the metalizing pattern of a second embodiment of the invention.

FIG. 8 is a cross-sectional view of FIG. 7 taken across the section line 8—8 in FIG. 7.

FIG. 8a is a view similar to FIG. 2 and shows a modified source contact configuration.

FIG. 9 shows the shape of forward-current characteristics of a device like that of FIG. 2 where the region 40 beneath the oxide is n(−).

FIG. 10 shows the shape of the characteristic of a device identical to that of FIG. 2 where the region 40 has high n(+) conductivity.

DETAILED DESCRIPTION OF THE DRAWINGS

A first embodiment of the novel MOSFET device of the present invention is shown in FIGS. 1 and 2 which show a chip of monocrystalline silicon 20 (or some other suitable material), with the device electrodes following the serpentine path 21 best shown in FIG. 1 in order to increase the current-carrying area of the device. Other geometries could be used. The device illustrated has a reverse voltage of about 400 volts and an on-resistance less than about 0.4 ohm with a channel width of 50 centimeters. Devices having reverse voltages of from 90 to 400 volts have been made. The 400 volt devices have carried pulse currents of 30 amperes. The 90 volt devices have had forward on-resistances of about 0.1 ohm with a channel width of 50 centimeters and have carried pulse currents up to about 100 amperes. Higher and lower voltage devices can also be made with varying channel widths.

Presently known MOSFET devices have much higher on-resistances than the above. For example, a 400 volt MOSFET comparable to that described below but made with prior art techniques would normally have an on-resistance much greater than about 1.5 ohms, as compared to an on-resistance less than about 0.4 ohm in a device made according to this invention. Moreover, the MOSFET switching device of the present invention will exhibit all of the desirable advantages of the MOSFET device, since it operates as a majority carrier device. These advantages include high switching speed, high gain and avoidance of the secondary breakdown characteristics which exist in minority carrier devices.

The device of FIGS. 1 and 2 has two source electrodes 22 and 23 which are separated by a metalized gate electrode 24 which is fixed to but spaced from the semiconductor device surface by a silicon dioxide layer 25. The serpentine path followed by gate oxide 25 has a length of 50 centimeters and has 667 undulations, but is shown more simply in FIG. 1. Other channel widths can be used. Source electrodes 22 and 23 can be laterally extended as shown to serve as field plates to help spread the depletion region created during reverse voltage conditions. Each of source electrodes 22 and 23 supply current to a common drain electrode 26 which is fixed to the bottom of the wafer. The relative dimensions for the device, particularly in thickness, have been grossly exaggerated in FIG. 2 for purposes of clarity. *The silicon chip or wafer 20 is formed on an n(+) substrate* which may have a thickness of about 14 mils. An n(−) epitaxial layer is deposited on substrate 20 and will have a thickness and resistivity depending on the desired reverse voltage. All junctions are formed in this epitaxial layer which can have a relatively high resistivity. In the embodiment disclosed, the epitaxial layer has a thickness of about 35 microns and a resistivity of about 20 ohm-centimeters. For a 90 volt device, epitaxial layer 20 would be about 10 microns thick and would have a resistivity of about 2.5 ohm-centimeters. A channel width of 50 centimeters is also used to provide the desired current carrying capacity for the device.

In a preferred embodiment of the invention, there is an elongated serpentine p(+) conductivity region beneath each of the source electrodes 22 and 23 which thus extends around the serpentine path shown in FIG. 1. These p(+) regions are shown in FIG. 2 as the p(+) regions 30 and 31, respectively, and are similar to those of the prior art except that the maximum p(+) region depth is greatly exaggerated in order to form a large radius of curvature. This allows the device to withstand higher reverse voltages. By way of example, the depth of regions 30 and 31 is preferably about 4 microns at the dimension X in FIG. 2 and about 3 microns at the dimension Y in FIG. 2.

By using D-MOS fabrication techniques, two n(+) regions 32 and 33 are formed beneath source electrodes 22 and 23, respectively, and define, with the p(+) regions 30 and 31, n-type channel regions 34 and 35, respectively. Channel regions 34 and 35 are disposed beneath the gate oxide 25 and can be inverted by the appropriate application of a biasing signal to the gate 24 in order to permit conduction from the source 22 and the source 23 through the inversion layers into the central region disposed beneath the gate 24 and then to the drain electrode 26. Channels 34 and 35 may each have a length of about 1 micron.

It has previously been thought necessary that the central n(−) region between channels 34 and 35 (and between p(+) regions 30 and 31) should have a high resistivity in order to permit the device to withstand high reverse voltages. However, the relatively high resistivity n(−) material is also a significant contributing factor to the high forward on-resistance of the device.

In accordance with the significant feature of the present invention, a significant portion of this central conducting region is made relatively highly conductive and consists of an n(+) region 40 disposed immediately beneath the gate oxide 25. The n(+) region 40 has a depth of about 4 microns and could range from about 3 microns to about 6 microns. While its exact conductivity is not known, and varies with depth, it is high relative to the n(−) region beneath it. More particularly, region 40 has a high conductivity which would be determined by a total ion implanted dose of from about 1×10^{12} to 1×10^{14} phosphorus atoms/cm^2 at 50 kV followed by a diffusion drive at from 1150° C. to 1250° C. for from 30 minutes to 240 minutes. It has been found that by making this region 40 relatively highly conductive n(+) material through a diffusion or other operation, the device characteristics are significantly improved and the forward on-resistance of the device is reduced by a factor greater than two. Moreover, it has been found that the provision of the high conductivity region 40 does not interfere with the reverse voltage characteristics of the device. Accordingly, by making the region beneath the gate oxide 25 and between channels 34 and 35 more highly conductive, the forward on-resistance of the ultimate high power switching device has been significantly reduced and the MOSFET device becomes far more competitive with an equiva-

lent junction-type device while still retaining all of the advantages of the MOSFET majority carrier operation.

In the above description of FIGS. 1 and 2, it has been assumed that the conduction channels 34 and 35 are of p(+) material and are, accordingly, inverted to an n-type conductivity to provide a majority carrier conduction channel from sources 22 and 23 to the central region 40 upon the application of an appropriate gate voltage. Clearly, however, all of these conductivity types could be reversed so that the device could work as a p-channel device rather than an n-channel device as disclosed.

One process by which the device of FIGS. 1 and 2 could be constructed is shown in FIGS. 3 to 6. Referring to FIG. 3, the base wafer 20 is shown as an n(+) material having an n(−) epitaxially deposited region on top thereof. A thick oxide layer 50 is formed on wafer 20 and windows 51 and 52 are opened therein. The open windows 51 and 52 are exposed to a beam of boron atoms in an ion implanting apparatus to form p(+) regions. Thereafter the implanted boron atoms are caused to diffuse deeper into the wafer to form the rounded p(+) concentration region shown in FIG. 3 which might have a depth of about 4 microns. During this diffusion operation, shallow oxide layers 53 and 54 grow over the windows 51 and 52.

As is next shown in FIG. 4, windows 61 and 62 are cut in the oxide layer 50 and an n(+) implant takes place to implant the n(+) regions 63 and 64 into the n(−) epitaxial layer. This n(+) implantation can be carried out with a phosphorus beam. Thereafter, the implanted regions are subjected to a diffusion step to cause the regions 63 and 64 to expand and deepen to a depth of about 3½ microns with a concentration determined by an implantation dose of 1×10^{12} to 1×10^{14} phosphorus atoms/cm^2 followed by a drive for 30 minutes to 4 hours at from 1150° C. to 1250° C. As will be later seen, regions 63 and 64 produce the novel n(+) region which substantially reduces the on-resistance of the device.

It should be noted that the n(+) regions 63 and 64 could, if desired, be epitaxially deposited and need not be diffused. Similarly, the resulting device being described herein could be manufactured by any desired process as would be apparent to those skilled in the art.

The next step in the process is shown in FIG. 5 and is the channel implantation and diffusion step in which the p(+) regions 71 and 72 are formed through the same windows 61 and 62 that were used for the n(+) implantation for regions 63 and 64. The p(+) regions 71 and 72 are formed by implanting with a boron beam to a dose of about 5×10^{13} to 5×10^{14} atoms/cm^2 followed by a diffusion drive for 30 to 120 minutes at 1150° C. to 1250° C.

Thereafter, and as shown in FIG. 6, steps are carried out for the source predeposition and the diffusion of the source regions 32 and 33. This is carried out by a conventional and non-critical phosphorus diffusion step where the diffusion proceeds through the windows 61 and 62 so that the source regions 32 and 33 are automatically aligned relative to the other preformed regions. Thus, the wafer is placed in a furnace and exposed to $POCl_3$ suspended in a carrier gas for from 10 minutes to 50 minutes at a temperature of from 850° C. to 1000°.

When this step is completed, the basic junction configuration required in FIG. 2 is formed with short p(+) regions disposed beneath the oxide 50 to serve as the conducting channel for the ultimately constructed device and with an n(+) region filling the area between the channels 34 and 35 and between p(+) regions 30 and 31. The manufacturing process then continues from the step of FIG. 6 to the device shown in FIG. 2 wherein the oxide surfaces on top of the chip are suitably stripped and the metalizing patterns for contacts 22, 23 and 24 are formed to establish electrical contacts to the device. The drain contact 26 is applied to the device in a subsequent metalizing operation. Thereafter, the entire device may be appropriately coated with a suitable passivation coating and wire leads are connected to the source electrodes 22 and 23 and the gate 24. The device is then mounted within a suitable protective housing, with the drain electrode fixed to the housing or other conductive support which serves as a drain connection.

The device shown in FIGS. 1 and 2 utilizes a serpentine path for each of the source regions and gate regions and a drain on the surface of the wafer opposite to the source electrodes. Other configurations can be used. FIGS. 7 and 8 illustrate a planar configuration which is a simple rectangular arrangement having a ring-shaped gate 80 which is disposed between a first source electrode 81 of ring shape and a central source 82. The device as shown in FIG. 8 is contained within a base wafer of p(−) monocrystalline silicon 83 which may have a buried n(+) region 84 to reduce the lateral resistance of the various current paths of the device leading to the laterally displaced drain electrode 85 which surrounds source 81.

A ring-shaped n(+) region 86 is formed within the device as shown in FIG. 8 and, in accordance with the present invention, the ring-shaped region 86 is of much higher conductivity than the n(−) epitaxially deposited region 87 which contains all the junctions of the device. The ring-shaped region 86 extends from the region beneath the gate oxide 88 and adjoins the ends of the two conducting channels formed between the ring-shaped p(+) region 89 and the central p(+) region 91 disposed beneath the ring-shaped source 81 and central source 82, respectively.

It will also be noted in FIG. 8 that the outer periphery 90 of the p(+) ring 89 has a large radius to assist the device in withstanding high reverse voltages.

An n(+) region 95 in FIG. 8 is provided to ensure good contact to drain electrode 85. Drain electrode 85 is widely laterally spaced from source 81 (by greater than about 90 microns). The drain contact 85 is surrounded by a p(+) isolation diffusion 96 to isolate the device from other devices on the same chip or wafer.

In the arrangement of FIG. 8, like that of FIG. 2, current flow from sources 81 and 82 goes through the width of epitaxial region 87, through the region 86. The current then flows laterally outward and then up to the drain contact 85. As in the embodiment of FIG. 2, device resistance is greatly reduced by the relatively highly conductive region 86.

In carrying out the above invention, it should be noted that any type of contact material can be used to make the source and gate contacts. By way of example, aluminum could be used for the source electrodes while a polysilicon material can be used for the conductive gate 80 in FIG. 8 or the conductive gate 24 in FIG. 2.

Numerous other geometries can be used to make the device of the invention, including a plurality of pairs of straight, parallel source elements with respectively interposed gates and the like.

The source electrodes 22 and 23 have been shown as separate electrodes which can be connected to separate leads. Clearly, the sources 22 and 23 could be directly connected as shown in FIG. 8a where components similar to those of FIG. 2 have been given similar identifying numerals. In FIG. 8a, however, the gate electrode is a polysilicon layer 101 (in place of aluminum) deposited atop gate oxide 25. The gate 101 is then covered with oxide layer 102 and a conductive layer 103 connects the two sources 22 and 23 together to form a single source conductor which is insulated from gate 101. Connection is made to the gate at some suitable edge portion of the wafer.

FIGS. 9 and 10 show the shape of measured curves which demonstrate the reduction in forward resistance when the region 40 is made highly conductive (n+). In FIG. 9, the device tested had a region 40 which had the n(−) resistivity of the epitaxial region. Thus, the forward resistance is characteristically high at different gate biases as shown in FIG. 9.

In the device of the invention where region 40 is of n(+) conductivity, there is a dramatic decrease in the on-resistance as shown in FIG. 10 for all gate voltages before velocity saturation of the electrons occurs.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface location to a depth less than said first depth; the outer rim of each of said first and second source regions being laterally spaced along said first semiconductor surface from the lateral outer periphery of its said base region to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion;

a drain electrode coupled to said drain conductive region; and

at least said first base region being a cellular polygonal region; said cellular polygonal region being surrounded by said common conduction region; said first source region having the shape of an annular ring disposed within said cellular polygonal first base region.

2. The device of claim 1 wherein said common conduction region is relatively highly doped compared to said relatively highly doped major body portion and extends from said given first semiconductor surface location to a depth greater than the depth of said source region, but less than said first depth of said first and second spaced base regions, whereby resistance to current flow at the junctures between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced.

3. The device of claim 1 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

4. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said first depth; the outer rim of each of said first and second source regions being laterally spaced along said first semiconductor surface from the lateral outer periphery of its said base region to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

material disposed over and contacting each of said source regions.

15. The device of claim 8, wherein said common conduction region is relatively highly doped compared to said relatively lightly doped major body portion and extends from said given first semiconductor surface location to a depth greater than the depth of said source region but less than said depth of said first and second base regions, whereby resistance to current flow at the junctures between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced.

16. The device of claim 7 wherein said source electrode means makes electrical contact to the surface of said cellular polygonal region and the surface of said annular ring-shaped region.

17. The device of claim 8 wherein said source electrode means makes electrical contact to the surface of said cellular polygonal region and the surface of said annular ring-shaped ring.

18. The device of claim 15 wherein said source electrode means makes electrical contact to the surface of said cellular polygonal region and the surface of said annular ring-shaped ring.

19. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance; said device comprising:

- a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;
- at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;
- first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said first depth; the outer rim of each of said first and second source regions being laterally spaced along said first semiconductor surface from the lateral outer periphery of its said base region to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively, and said common conduction region;
- source electrode means connected to said source regions;
- gate insulation layer means on said first surface, disposed at least on said first and second channel regions;
- gate electrode means on said gate insulation layer means and overlying said first and second channel regions;
- said wafer including a further region of opposite conductivity type adjoining said lightly doped major body portion; and
- an electrode coupled to said further region.

20. The device of claim 19 wherein at least said first base region comprises a cellular polygonal region; said cellular polygonal region being surrounded by said common conduction region; said first source region having the shape of an annular ring disposed within said cellular polygonal first base region.

21. The device of claim 19 wherein said common conduction region is relatively highly doped compared to said relatively lightly doped major body portion and wherein said common conduction region extends from said given first semiconductor surface location to a depth greater than the depth of said source region but less than said depth of said first and second base regions, whereby resistance to current flow in the path between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced.

22. The device of claim 19 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

23. The device of claim 19 wherein said source electrode means makes electrical contact to the surface of said cellular polygonal base region and the surface of said annular ring-shaped source region.

24. The device of claim 19 wherein each of said at least first and second spaced base regions of said opposite conductivity type have respective profiles which include relatively shallow depth regions extending from said common conduction region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common conduction region; said shallow base regions partially underlying their respective source regions.

* * * * *

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion; and

a drain electrode coupled to said drain conductive region;

said common conduction region being relatively highly doped compared to said relatively lightly doped major body portion and extending from said given first semiconductor surface location to a depth greater than the depth of said source region but less than said first depth of said first and second spaced base regions, whereby resistance to current flow at the junctures between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced, wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

5. The device of claim 2 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

6. The device of claim 1 wherein said source electrode means makes electrical contact to the surface of said cellular polygonal region and the surface of said annular region-shaped ring.

7. A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively and said common conduction region;

source electrode means connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain conductive region remove from said common region and separated therefrom by said relatively lightly doped major body portion;

a drain electrode coupled to said drain conductive region and comprising a third terminal;

each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include relatively shallow depth regions extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region;

at least said first base region being a cellular polygonal region; said cellular polygonal region being surrounded by said common conduction region; said first source region having the shape of an annular ring disposed within said cellular polygonal first base region; said relatively shallow depth region of said first base region surrounding the outer periphery of said relatively deep portion of said first base region.

8. The device of claim 7 wherein said shallow base regions partially underlie their respective source regions.

9. The device of claim 7 wherein said common conduction region is relatively highly doped compared to said relatively lightly doped major body portion and extends from said given first semiconductor surface location to a depth greater than the depth of said source region but less than said depth of said first and second base regions, whereby resistance to current flow at the junctures between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced.

10. The device of claim 8 wherein said common conduction region is relatively highly doped compared to said relatively lightly doped major body portion and extends from said given first semiconductor surface location to a depth greater than the depth of said source region but less than said depth of said first and second base regions, whereby resistance to current flow at the junctures between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced.

11. The device of claim 7 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

12. The device of claim 8 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

13. The device of claim 9 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said source regions.

14. The device of claim 10 wherein said source electrode means comprises a single sheet of conductive

US004959699B1

REEXAMINATION CERTIFICATE (2105th)

United States Patent [19]

[11] **B1 4,959,699**

Lidow et al.

[45] Certificate Issued **Oct. 12, 1993**

[54] **HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE**

[76] Inventors: **Alexander Lidow**, Manhattan Beach; **Thomas Herman**, Redondo Beach, both of Calif.

Reexamination Request:
No. 90/002,515, Nov. 13, 1991

Reexamination Certificate for:

Patent No.: **4,959,699**
Issued: **Sep. 25, 1990**
Appl. No.: **371,678**
Filed: **Jun. 22, 1989**

Certificate of Correction issued May 25, 1993.

Related U.S. Application Data

[60] Continuation of Ser. No. 90,664, Aug. 27, 1987, abandoned, which is a division of Ser. No. 456,813, Jan. 10, 1983, abandoned, which is a division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] Int. Cl.^{5} H01L 29/10; H01L 29/78; H01L 29/68; H01L 27/02

[52] U.S. Cl. 257/328; 257/339; 257/342; 257/487; 257/653

[58] Field of Search 357/23.4, 23.8

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,015,278	3/1977	Fukuta .	
4,028,717	6/1977	Joy et al.	357/23.8
4,072,975	2/1978	Ishitani .	
4,078,947	3/1978	Johnson et al.	357/23.4
4,145,700	3/1979	Jambotkar .	
4,145,703	3/1979	Blanchard et al. .	
4,148,047	4/1979	Hendrickson .	
4,199,774	4/1980	Plummer .	
4,376,286	3/1983	Lidow et al. .	
5,047,820	9/1991	Garnett	357/23.8

FOREIGN PATENT DOCUMENTS

51-85381	7/1976	Japan .
52-106688	9/1977	Japan .
53-74385	7/1978	Japan .

OTHER PUBLICATIONS

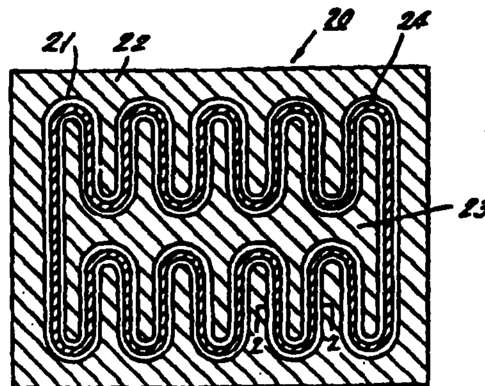
R. J. Duchynski, "Ion implantation for semiconductor devices", *Solid State Technology*, (Nov. 1977) pp. 53–58.
J. D. Plummer, "Process physics: Implications for manufacturing of submicron silicon devices", *Solid State Technology* (Mar. 1986) pp. 61–66.
Introductions to Sessions 6, 12, 18 and 29, International Electron Devices Meeting (1989) *Technical Digest*, four pages.
J. J. Carroll et al., "Ellipsometry-LEED study of the absorption of oxygen on (011) tungsten", *Surface Science*, vol. 16 (1969) pp. 251–264.

(List continued on next page.)

Primary Examiner—J. Carroll

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.



OTHER PUBLICATIONS

J. L. Stone et al., "Recent advances in ion implantation—a state of the art review", *Solid State Technology,* (Jun. 1976) pp. 35–44.

J. Sansbury, "Applications of ion implantation in semiconductor processing", *Solid State Technology,* (Nov. 1976) pp. 31-37.

A High Power MOSFET with a Vertical Drain Electrode and a Meshed Gate Structure, Yoshida, et al., IEEE Journal of Solid State Circuits, vol. SC-11, No. 4 (Aug. 1976) pp. 472–477.

Power Handling Capability of MOSFET, Minoru Nagata, Japanese Journal of Applied Physics, vol. 16, Supp. 16-1, pp. 217-222 (1977).

IBM Technical Disclosure Bulletin, vol. 16, No. 11, pp. 3519–3520, Cady, et al. (Apr. 1974).

DSA MOS Transistor and Its Integrated Circuit, Japanese Journal of Applied Physics, vol. 16, Suppl. 16-1, pp. 163-166, Y. Haysashi, et al. (1977).

Optimization of Nonplanar Power MOS Transistors, IEEE Transactions on Electron Devices, vol. ED-25, No. 10, K. P. Lisiak, et al. (Oct. 1978) 6 pages.

Diffusion Self-Aligned MOST: A New Approach for High Speed Device, Proceedings of the 1st Conference on Solid State Devices, Tokyo, 1969 Supplement to the Journal of the Japan Society of Applied Physics, vol. 39, Y. Tarui, et al. (1970) 6 pages.

Japanese Take Two Steps Forward In MOST-Bipolar Compatibility, Electronics International (Oct. 13, 1969) 4 pages.

REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims 1 to 3 and 5 to 24 is confirmed.

Claim 4 is cancelled.

* * * * *

US004959699B1

REEXAMINATION CERTIFICATE (3706th)

United States Patent [19]

[11] **B2 4,959,699**

Lidow et al.

[45] Certificate Issued **Jan. 19, 1999**

[54] **HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE**

[76] Inventors: **Alexander Lidow**, 4005 Strand Ave., Manhattan Beach, Calif. 90266; **Thomas Herman**, 1623 Herrin Dr., Redondo Beach, Calif. 90278

Reexamination Requests:
No. 90/003,490, Jul. 12, 1994
No. 90/003,900, Jul. 25, 1995

Reexamination Certificate for:

Patent No.:	**4,959,699**
Issued:	**Sep. 25, 1990**
Appl. No.:	**371,678**
Filed:	**Jun. 22, 1989**

Reexamination Certificate B1 4,959,699 issued Oct. 12, 1993

Certificate of Correction issued May 25, 1993.

Related U.S. Application Data

[60] Continuation of Ser. No. 90,664, Aug. 27, 1987, abandoned, which is a division of Ser. No. 456,813, Jan. 10, 1983, abandoned, which is a division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] Int. Cl.^{6} **H01L 29/76**

[52] U.S. Cl. 257/328; 257/339; 257/342; 257/487; 257/653

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 33,209	5/1990	Plummer	357/23.4
3,619,740	11/1971	Nakanuma et al.	317/235 R
3,831,187	8/1974	Neilson	257/137
4,072,975	2/1978	Ishitani	357/23
4,145,700	3/1979	Jambotkar	357/23
4,145,703	3/1979	Blanchard et al.	357/55
4,148,047	4/1979	Hendrickson	357/23
4,163,246	7/1979	Aomura et al.	257/776
4,190,850	2/1980	Tihanyi et al.	357/23
4,199,774	4/1980	Plummer	357/41
4,206,469	6/1980	Hanes et al.	257/341
4,219,835	8/1980	van Loon et al.	257/330
4,233,615	11/1980	Takemoto et al.	357/22
4,376,286	3/1983	Lidow et al.	357/23
4,599,576	7/1986	Yoshida et al.	257/408
4,642,666	2/1987	Lidow et al.	357/23.4
4,705,759	11/1987	Lidow et al.	437/29
5,130,767	7/1992	Lidow et al.	257/339

FOREIGN PATENT DOCUMENTS

47-21739	6/1972	Japan .
51-85381	7/1976	Japan .
51-134076	11/1976	Japan .
52-104878	9/1977	Japan .
52-106688	9/1977	Japan .

OTHER PUBLICATIONS

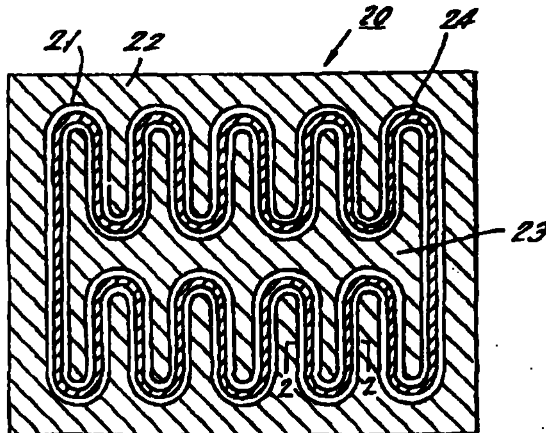
E. S. Oxner, *Power FETs and Their Applications*, Prentice-Hall, Inc., New Jersey (1982) pp. 67–71.

(List continued on next page.)

Primary Examiner—Stanley Miller

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.



OTHER PUBLICATIONS

K. Lisiak et al., "Optimization of Non-Planar Power MOS Transistors", *IEEE Transactions on Electron Devices*, vol. ED-25 (Oct. 1978) pp. 1229-1234.
S. M. Sze, Semiconductor Devices Physics and Technology, John Wiley & Sons, New York (1985) pp. 105-107.
B. J. Baliga et al., "Analytical Solutions for the Breakdown Voltage of Abrupt Cylindrical and Spherical Junctions", *Solid-State Electronics*, vol. 19 (1976) pp. 739-744.
S. M. Sze, *Semiconductor Devices Physics and Technology*, John Wiley & Sons, New York (1985) p. 203.
S. Krishna, "Secondary Breakdown in High Voltage MOS Transistors", *Solid-State Electronics*, vol. 20 (1977) pp. 875-878.
S. M. Sze, *Semiconductor Devices Physics and Technology*, John Wiley & Sons, New York (1985) pp. 401-402.
Full English Translation of Japan Kokai Patent Publication No. 51-134076 as per USPTO.
H. F. Gray et al., "Sleep and AES Applied to Solid State Devices and Materials" *IEDM 74*, (Dec. 1974) pp. 561-564.
S. R. Combs et al., "Characterization and Modeling of Simultaneously Fabricated DMOS and VMOS Transistors", *IEDM 76*, (Dec. 1976) pp. 569-572.
Full English Translation of Japan Kokai Patent Publication No. 52-104878.
Certificate of Correction dated 25 May 1993 for US Patent No. 4,959,699.
D. B. Lee, "Anisotropic Etching of Silicon", *Journal of Applied Physics*, vol. 40, No. 11 (Oct. 1969) ppm 4569-4574.
M. J. Declercq et al., "Optimization of the Hydrazine-Water Solution for Anisotropic Etching of Silicon in Integrated Circuit Technology", *J. Electrochem. Soc.: Solid-State Science and Technology*, vol. 122, No. 4 (Apr. 1975) pp. 545-552.
Tarui et al., "Diffusion Self-Aligned MOST: A New Approach for High Speed Device," *J. of Japan Society of Applied Physics*, vol. 39, 1970, pp. 105-110.
Pocha et al., "A Computer-Aided Design Model for High-Voltage Double Diffused MOS (DMOS) Transistors," *IEEE Journal of Solid-State Circuits*, vol. SC-11, No. 5, (Oct. 1976, pp. 718-726.
Yoshida et al., "A High power MOSFET with a Vertical Drain Electrode and a Meshed Gate Structure," *IEEE Journal of Solid-State Circuits*, vol. SC-11, No. 4, Aug. 1976, pp. 472-477.
Plummer et al., "A Monolithic 200-V CMOS CMOS Analog Switch," *IEEE Journal of Solid-State Circuits*, vol. SC-11, No. 6, Dec. 1976, pp. 809-817.
Scharf et al., "A MOS-Controlled Triac Device," *1978 IEEE International Solid-State Circuits Conference*, San Francisco, Calif., Feb. 15-17, 1978, pp. 222-223.
E. S. Oxner, *Power FETs and Their Applications*, Prentice-Hall, Inc., New Jersey (1982) pp. 59-67.

REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claim 4 was previously cancelled.

Claims **1**, **7**, **19** and **24** are determined to be patentable as amended.

Claims **2**, **3**, **5**, **6**, **8–18** and **20–23**, dependent on an amended claim, are determined to be patentable.

New claims **25–28** and **29** are added and determined to be patentable.

1. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a *vertical* common conduction region of one conductivity type at a given first semiconductor surface location; *the concentration of carriers of said one conductivity type in said common conduction region at said first semiconductor surface being less than the concentration of carriers of said opposite conductivity type of said first and second base regions at said first semiconductor surface;*

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface location to a depth less than said first depth; the outer rim of each of said first and second source regions being laterally spaced along said first semiconductor surface from the lateral outer periphery of its said base region to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion;

a drain electrode coupled to said drain conductive region; and

at least said first base region being a cellular polygonal region; said cellular polygonal region being surrounded by said common conduction region; said first source region having the shape of an annular ring disposed within said cellular polygonal first base region.

7. A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a *vertical* common conduction region of one conductivity type at a given first semiconductor surface location; *the concentration of carriers of said one conductivity type in said common conduction region at said first semiconductor surface being less than the concentration of carriers of said opposite conductivity type of said first and second base regions at said first semiconductor surface;*

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions being laterally spaced along said first semconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion;

a drain electrode coupled to said drain conductive region and comprising a third terminal;

each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include, *to allow the device to withstand relatively high breakdown voltages,* relatively shallow depth regions *having a relatively small radius of curvature* extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region;

at least said first base region being a cellular polygonal region; said cellular polygonal region being surrounded by said common conduction region; said first source

region having the shape of an annular ring disposed within said cellular polygonal first base region; said relatively shallow depth region of said first base region surrounding the outer periphery of said relatively deep portion of said first base region.

19. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance; said device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a *vertical* common conduction region of one conductivity type at given first semiconductor surface location; *the concentration of carriers of said one conductivity type in said common conduction region at said first semiconductor surface being less than the concentration of carriers of said opposite conductivity type of said first and second base regions at said first semiconductor surface;*

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said first depth; the outer rim of each of said first and second source regions being laterally spaced along said first semiconductor surface from the lateral outer periphery of its said base region to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively, and said common conduction region;

source electrode means connected to said source regions;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

said wafer including a further region of opposite conductivity type adjoining said lightly doped major body portion; and

an electrode coupled to said further region.

24. The device of claim 19 wherein each of said at least first and second spaced base regions of said opposite conductivity type have respective profiles which include, *to allow the device to withstand relatively high breakdown voltages,* relatively shallow depth regions *having a relatively small radius of curvature* extending from said common conduction region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common conduction region; said shallow base regions partially underlying their respective source regions.

25. The device of claim 1 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

26. The device of claim 7 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

27. The device of claim 19 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

28. The device of claim 1 wherein said common conduction region is continuous and uninterrupted.

29. The device of claim 7 wherein said common conduction region is continuous and uninterrupted.

* * * * *

United States Patent [19] | [11] Patent Number: 5,008,725
Lidow et al. | [45] Date of Patent: Apr. 16, 1991

[54] PLURAL POLYGON SOURCE PATTERN FOR MOSFET

[75] Inventors: Alexander Lidow, Manhattan Beach; Thomas Herman, Redondo Beach; Vladimir Rumennik, El Segundo, all of Calif.

[73] Assignee: International Rectifier Corporation, El Segundo, Calif.

[21] Appl. No.: 291,423

[22] Filed: Dec. 23, 1988

Related U.S. Application Data

[63] Continuation of Ser. No. 243,544, Mar. 13, 1981, abandoned, which is a continuation of Ser. No. 38,662, May 14, 1979, abandoned.

[51] Int. Cl.[5] H01L 29/100; H01L 29/780; H01L 29/060; H01L 27/100

[52] U.S. Cl. 357/23.4; 357/20; 357/45

[58] Field of Search .... 357/23 VD, 20, 45, 86, 357/23.4

[56] References Cited

U.S. PATENT DOCUMENTS

4,015,278 3/1977 Fukuta .... 357/23 VD
4,072,975 2/1978 Ishitani .... 357/23 VD
4,148,047 4/1979 Hendrickson .... 357/23 VD

FOREIGN PATENT DOCUMENTS

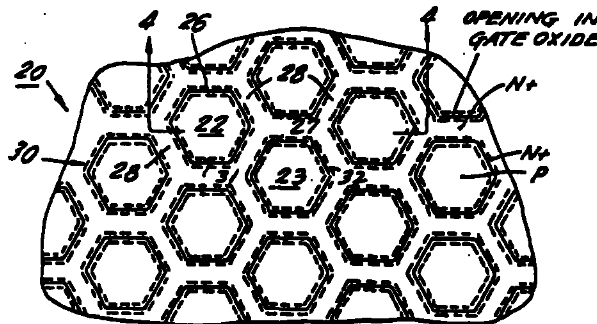
0085381 7/1976 Japan .... 357/23 VD
0000885 1/1979 Japan .... 357/23 VD

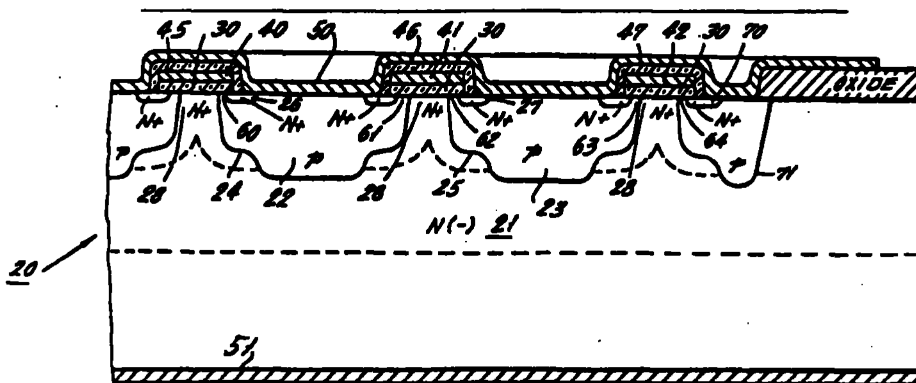
Primary Examiner—Michael C. Wimer
Assistant Examiner—Peter Toby Brown
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen

[57] ABSTRACT

A high power MOSFET has a plurality of closely packed polygonal sources spaced from one another on one surface of a semiconductor body. An elongated gate electrode is exposed in the spacing between the polygonal sources and cooperates with two channels, one for each adjacent source electrode, to control conduction from the source electrode through the channel and them to a drain electrode on the opposite surface of the semiconductor body. The conductive region adjacent the channel and between adjacent sources is relatively highly conductive in the section of the channel adjacent to the surface containing the sources. The polygonal shaped source members are preferably hexagonal so that the distances between adjacent sources is relatively constant throughout the device. Each polygonal region has a relatively deep central portion and a shallow outer shelf portion. The shelf portion generally underlies an annular source region. The deep central portion underlies an aluminum conductive electrode and is sufficiently deep that it will not be fully penetrated by aluminum spiking.

14 Claims, 3 Drawing Sheets





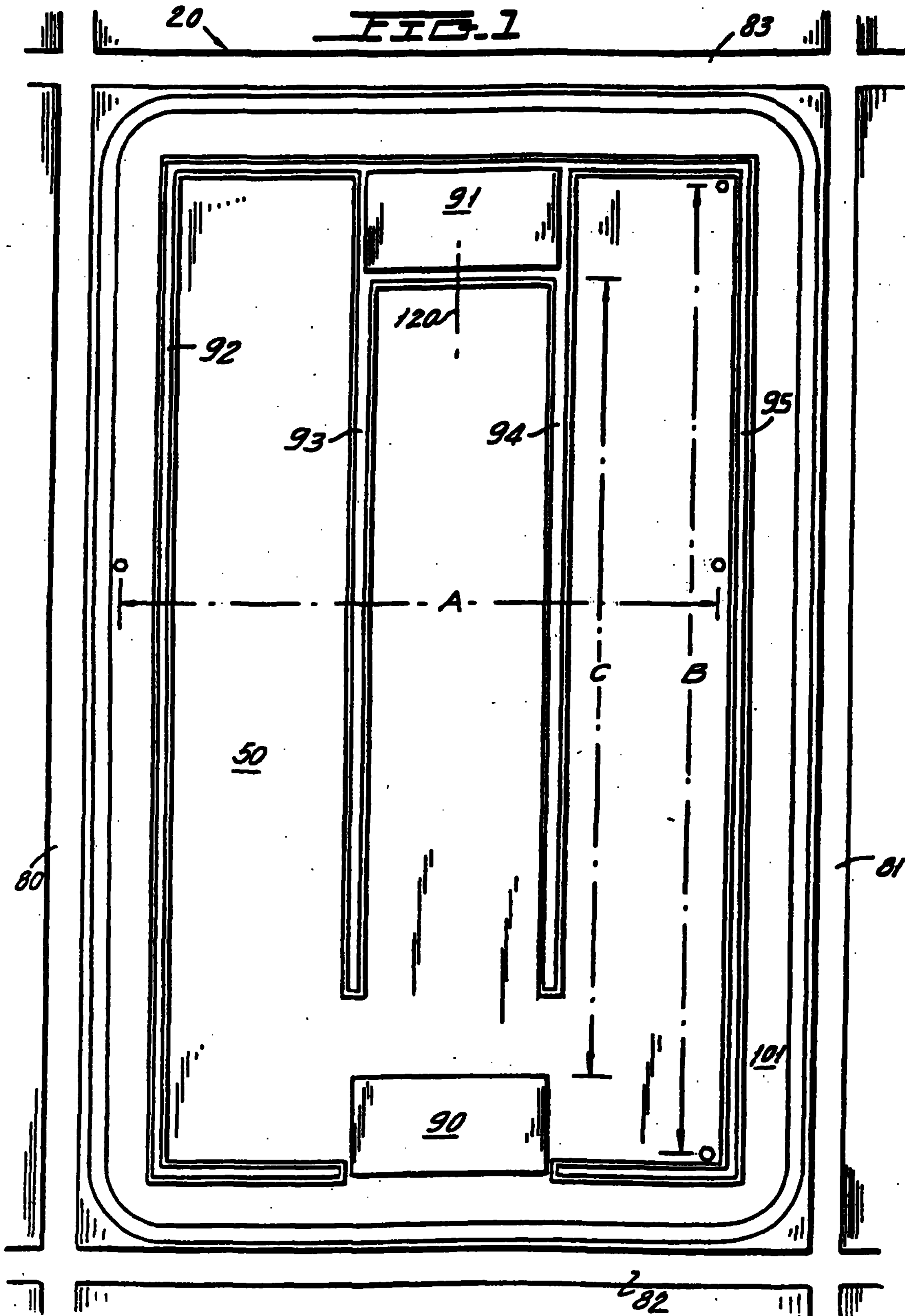


FIG.1
20
83
91
120
92
93
94
95
A
C
B
50
80
81
101
90
82

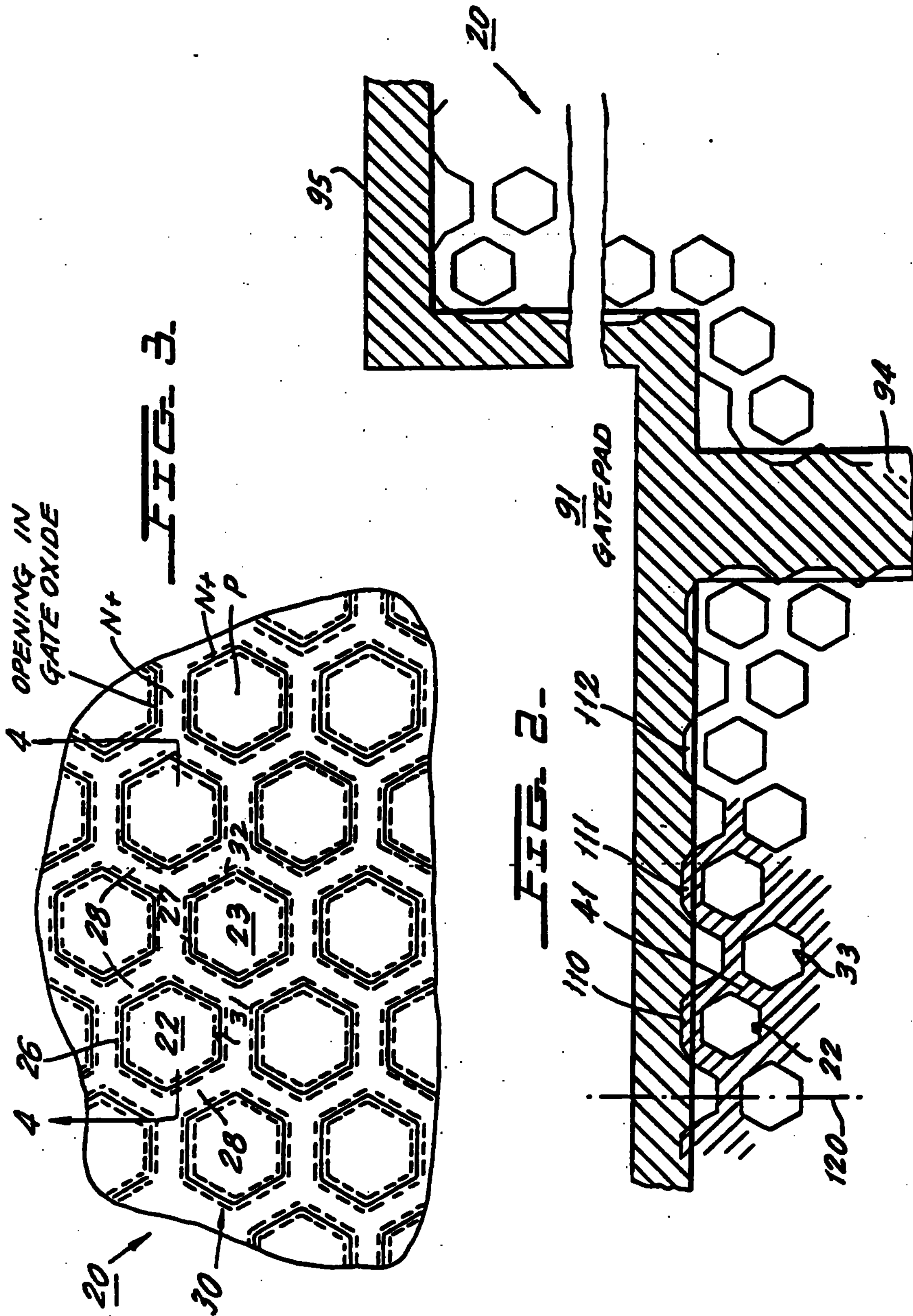


FIG. 3.
OPENING IN GATE OXIDE
N+
N+
P
4
4
20
30
26
22
28
28
27
23
32
31
FIG. 2.
20
95
94
91
GATE PAD
112
111
41
110
33
22
120

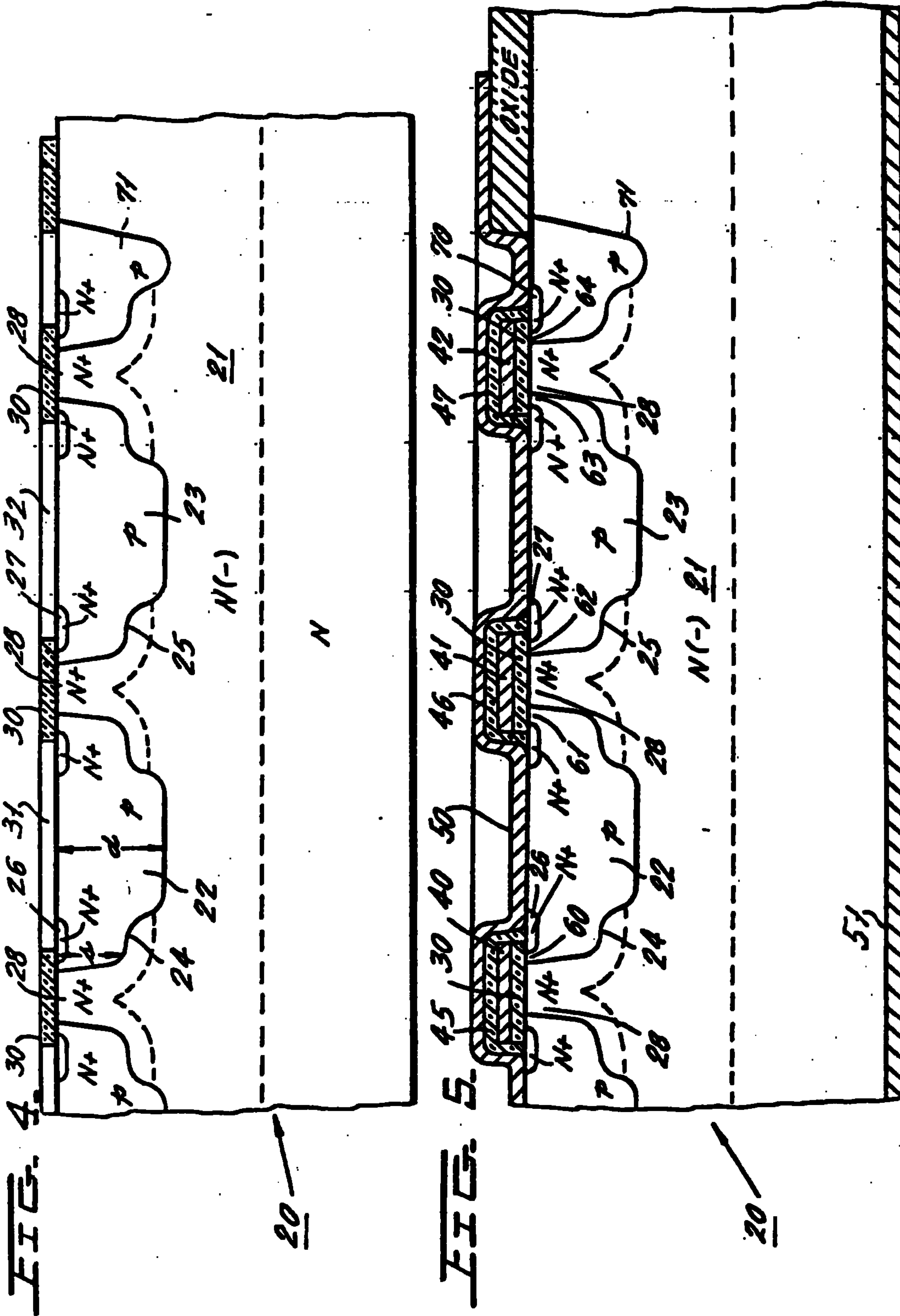


FIG. 4
FIG. 5
OXIDE
N+
P
N(-)
N
21
20
51

PLURAL POLYGON SOURCE PATTERN FOR MOSFET

This application is a continuation of application Ser. No. 243,544, filed Mar. 13, 1981, now abandoned, which was a continuation of application Ser. No. 038,662, filed May 14, 1979, now abandoned.

RELATED APPLICATIONS

This application is related to application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned and refiled as continuation application Ser. No. 232,713, filed Feb. 9, 1981, now U.S. Pat. No. 4,376,286, entitled HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE, in the names of Alexander Lidow and Thomas Herman, and assigned to the assignee of the present invention.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices, and more specifically relates to a novel source pattern for a MOSFET device of the type disclosed in above-mentioned U.S. Pat. No. 4,376,286 wherein a plurality of polygonal-shaped source elements are disposed over the surface of a semiconductor body and are spaced from one another by a closely controlled dimension.

High power MOSFETS having low on-resistance and high breakdown voltage are known and are shown in the above-noted U.S. Pat. No. 4,376,286. In the above application, the source electrodes are spaced, interdigitated source regions spaced from one another by two parallel channel regions covered by a common gate. The device has exceptionally low on-resistance along with the usual advantages of the MOSFET device over the bi-polar device particularly by virtue of a relatively high conductivity region disposed between the two adjacent channels and leading to a common drain electrode.

It has been found that an interdigitated structure has a relatively low packing density. Moreover, the interdigitated arrangement disclosed in the above U.S. Pat. No. 4,376,286 requires relatively complicated masks and has a relatively high capacitance.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device with low forward resistance where a very high packing density is available and which can be made with relatively simple masks. The device further has relatively low capacitance. Typically, the device may be made through the use of phosphorus implantation and D-MOS fabrication techniques but any desired technique can be used.

Each of the individual spaced source regions, in accordance with the invention, is polygonal in configuration and is preferably hexagonal to ensure a constant spacing along the major lengths of the sources disposed over the surface of the body. An extremely large number of small hexagonal source elements may be formed in the same surface of the semiconductor body for a given device. By way of example, 6,600 hexagonal source regions can be formed in a chip area having a dimension of about 100 by 140 mils to produce an effective channel width of about 22,000 mils, thus permitting very high current capacity for the device.

The space between the adjacent sources may contain a polysilicon gate or any other gate structure where the gate structure is contacted over the surface of the device by elongated gate contact fingers which ensure good contact over the full surface of the device.

Each of the polygonal source regions is contacted by a uniform conductive layer which engages the individual polygonal sources through openings in an insulation layer covering the source regions, which openings can be formed by conventional D-MOS photolithographic techniques. A source pad connection region is then provided for the source conductor and a gate pad connection region is provided for the elongated gate fingers and a drain connection region is made to the reverse surface of the semiconductor device.

A plurality of such devices can be formed from a single semiconductor wafer and the individual elements can be separated from one another by scribing or any other suitable method.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a completed element on a semiconductor wafer prior to the separation of the element away from the remainder of the wafer.

FIG. 2 is an enlarged detail of the gate pad to illustrate the relationship of the gate contact and the source polygons in the region of the gate pad.

FIG. 3 is a detailed plan view of a small portion of the source region during one stage of the manufacturing process of the device.

FIG. 4 is a cross-sectional view of FIG. 3 taken across the section line 4—4 in FIG. 3.

FIG. 5 is similar to FIG. 4 and shows the addition of a polysilicon gate, a source electrode means and drain electrode to the wafer.

DETAILED DESCRIPTION OF THE DRAWINGS

The polygon configuration of the source regions of the present invention is best shown in FIGS. 3, 4 and 5 which are first described.

Referring first to FIGS. 3 and 4, the device is shown prior to the application of the gate, source and drain electrodes. The manufacturing process can be of any desired type. The manufacturing process described in U.S. Pat. No. 4,376,286, referred to above, which is incorporated herein by reference, can be used whereby D-MOS fabrication techniques and ion implantation techniques can be advantageously employed for the formation of the junction and placement of the electrode in the most advantageous way.

The device is described as an N channel enhancement type device. It will be apparent that the invention will also apply to P channel devices and to depletion mode devices.

The device of FIGS. 3 and 4 has a plurality of polygonal source regions on one surface of the device, where these polygonal regions are preferably hexagonal in shape. Other shapes such as squares could have been used but the hexagonal shape provides better uniformity of spacing between adjacent source region perimeters.

In FIGS. 3 and 4, the hexagonal source regions are formed in a basic semiconductor body or wafer which can be an N type wafer 20 of monocrystalline silicon which has a thin N-epitaxial region 21 deposited thereon as best shown in FIG. 4. All junctions are formed in epitaxial region 21. By using suitable masks, a plurality of P type base regions such as regions 22 and 23 in FIGS. 3 and 4 are formed in one surface of the semiconductor wafer region 21, where these regions are

generally polygonal in configuration and, preferably, are hexagonal.

A very large number of such polygonal regions are formed. For example, in a device having a surface dimension of 100 by 140 mils, approximately 6600 polygonal regions are formed to produce a total channel width of about 22,000 mils. Each of the polygonal regions may have a width measured perpendicular to two opposing sides of the polygon of about 1 mil or less. The regions are spaced from one another by a distance of about 0.6 mil when measured perpendicularly between the adjacent straight sides of adjacent polygonal regions.

The P+ regions 22 and 23 will have a depth d which is preferably about 5 microns to produce a high and reliable field characteristic. Each of the P regions has an outer shelf region shown as shelf regions 24 and 25 for P regions 22 and 23, respectively, having a depth s of about 1.5 microns. This depth should be as small as possible to reduce the capacitance of the device.

Each of the polygon regions including polygonal regions 22 and 23 receive N+ polygonal ring regions 26 and 27, respectively. Shelves 24 and 25 are located beneath regions 26 and 27, respectively. N+ regions 26 and 27 cooperate with a relatively conductive N+ region 28 which is the N+ region disposed between adjacent P type polygons to define the various channels between the source regions and a drain contact which will be later described.

The highly conductive N+ regions 28 are formed in the manner described in U.S. Pat. No. 4,376,286, referred to above, and are the subject of that application and produce a very low forward resistance for the device.

In FIGS. 3 and 4, it will be noted that the entire surface of the wafer is covered with an oxide layer or combined conventional oxide and nitride layers which are produced for the formation of the various junctions. This layer is shown as the insulation layer 30. The insulation layer 30 is provided with polygonal shaped openings such as openings 31 and 32 immediately above polygonal regions 22 and 23. Openings 31 and 32 have boundaries overlying the N+ type source rings 26 and 27 for the regions 22 and 23, respectively. The oxide strips 30, which remain after the formation of the polygonal shaped openings, define the gate oxide for the device.

Electrodes may then be applied to the device as shown in FIG. 5. These include a polysilicon grid which includes polysilicon sections 40, 41 and 42 which overlie the oxide sections 30.

A silicon dioxide coating is then deposited atop the polysilicon grid 40 shown as coating sections 45, 46 and 47 in FIG. 5 which insulates the polysilicon control electrode and the source electrode which is subsequently deposited over the entire upper surface of the wafer. In FIG. 5 the source electrode is shown as conductive coating 50 which may be of any desired material, such as aluminum. A drain electrode 51 is also applied to the device.

The resulting device of FIG. 5 is an N channel type device wherein channel regions are formed between each of the individual sources and the body of the semiconductor material which ultimately leads to the drain electrode 51. Thus, a channel region 60 is formed between the source ring 26, which is connected to source electrode 50, and the N+ region 28 which ultimately leads to the drain electrode 51. Channel 60 is inverted to N type conductivity upon the application of a suitable control voltage to the gate 40. In a similar manner, channels 61 and 62 are formed between the source region 26, which is connected to the conductor 50, and the surrounding N+ region 28 which leads to the drain 51. Thus, upon application of a suitable control voltage to the polysilicon gate (including finger 41 in FIG. 5), channels 61 and 62 become conductive to permit majority carrier conduction from the source electrode 50 to the drain 51. Note that channels labeled 60 and 61 of FIG. 5 are the same annular channel which is formed within the region 22. Similarly, channels 62 and 63 are the same annular channel formed in the region 23.

Each of the sources form parallel conduction paths where, for example, channels 63 and 64 beneath gate element 42 permit conduction from the source ring 27 and an N type source strip 70 to the N+ region 28 and then to the drain electrode 51.

It is to be noted that FIGS. 4 and 5 illustrate an end P type region 71 which encloses the edge of the wafer.

The contact 50 of FIG. 5 is preferably an aluminum contact. It will be noted that the contact region for the contact 50 lies entirely over and in alignment with the deeper portion of the P type region 22. This is done since it was found that aluminum used for the electrode 50 might spike through very thin regions of the P type material. Thus, one feature of the present invention is to ensure that the contact 50 lies principally over the deeper portions of the P regions such as P regions 22 and 23. This then permits the active channel regions defined by the annular shelves 24 and 25 to be as thin as desired in order to substantially reduce the device capacitance.

FIG. 1 illustrates one completed device using the polygonal source pattern of FIG. 5. The completed device shown in FIG. 1 is contained within the scribe regions 80, 81, 82 and 83 which enable the breaking out of a plurality of unitary devices each having a dimension of 100 by 140 mils from the body of the wafer.

The polygonal regions described are contained in a plurality of columns and rows. By way of example, the dimension A contains 65 columns of polygonal regions and may be about 83 mils. The dimension B may contain 100 rows of polygonal regions and may be about 148 mils. Dimension C, which is disposed between a source connection pad 90 and a gate connection pad 91, may contain 82 rows of polygonal elements.

The source pad 90 is a relatively heavy metal section which is directly connected to the aluminum source electrode 50 and permits convenient lead connection for the source.

The gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which extend symmetrically over the outer surface of the area containing the polygonal regions and make electrical connection to the polysilicon gate as will be described in connection with FIG. 2.

Finally the outer circumference of the device contains the P+ (shown as "P" in the drawings) deep diffusion ring 71 which may be connected to a field plate 101 shown in FIG. 1.

FIG. 2 shows a portion of the gate pad 91 and the gate fingers 94 and 95. It is desirable to make a plurality of contacts to the polysilicon gate in order to reduce the R-C delay constant of the device. The polysilicon gate has a plurality of regions including regions 110, 111, 112 and the like which extend outwardly and receive extensions of the gate pad and the gate pad elements 94 and 95. The polysilicon gate regions may be left exposed

during the formation of the oxide coating 45-46-47 in FIG. 5 and are not coated by the source electrode 50. Note that in FIG. 2 the axis 120 is the axis of symmetry 120 which is that shown in FIG. 1.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of symmetrically disposed laterally distributed hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface;

said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;

each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;

a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

a drain electrode connected to said second planar surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

2. The MOSFET device of claim 1, wherein the material of said lattice of said first conductivity type has a relatively high impurity concentration region compared to the concentration of the remainder of said first portion of said wafer; said relatively high concentration region having a depth greater than the depth of said source regions and less than the depths of said plurality of base regions.

3. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of symmetrically disposed laterally distributed polygonal base regions each having a second conductivity type formed in said lightly doped region and extending for given depth beneath said first planar semiconductor surface;

said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

a drain electrode connected to said second planar semiconductor surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

4. The MOSFET device of claim 1 or 3, wherein each of said base regions occupies a total lateral area having a diameter less than about 1 mil and are spaced from adjacent base regions by about 0.6 mil.

5. The device of claim 1 or 3, wherein said 40M, is an N type conductivity, said base regions are a P type conductivity and said source regions are an N type conductivity.

6. The MOSFET device of claim 3, wherein the material of said lattice of said first conductivity type has a relatively high impurity concentration region compared to the concentration of the remainder of said first portion of said wafer; said relatively high concentration region having a depth greater than the depth of said source regions and less than the depths of said plurality of base regions.

7. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconduc-

tor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type; the space between adjacent ones of said polygonal base regions defining a common conduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface; and

a drain electrode coupled to said drain conductive region.

8. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

each of said at least first and second spaced base regions having a polygonal configuration; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region.

9. The MOSFET device of claims 7 or 8 wherein said common conduction region is relatively highly doped, compared to said relatively lightly doped major body portion and extends downwardly from said first planar semiconductor surface to a depth greater than the depth of said source regions, whereby resistance to current flow at the boundaries between said channel regions and said common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced without reducing breakdown voltage.

10. The MOSFET device of claim 9, wherein the depth of said common conduction region is less than said first depth of said base regions.

11. The MOSFET device of claim 1, 3, 35 or 36, wherein each of said base regions has a deepened central region and a shallower outer peripheral region, said deepened central region extending laterally under only a portion of its associated source region.

12. The MOSFET device of claim 11, wherein said deepened central region has a depth of approximately 5 microns and said shallower outer peripheral region has a depth of greater than approximately 1.5 microns.

13. The device of claim 32, 35 or 36, wherein there are in excess of about 1000 source regions each having a width of about 1 mil.

14. The device of claim 7 or 8, wherein said lightly doped wafer portion is an N type conductivity, said base regions are a P type conductivity and said source regions are an N type conductivity.

* * * * *

US005008725A

REEXAMINATION CERTIFICATE (1900th)

United States Patent [19]

[11] **B1 5,008,725**

Lidow et al.

[45] Certificate Issued **Jan. 12, 1993**

[54] **PLURAL POLYGON SOURCE PATTERN FOR MOSFET**

[76] Inventors: **Alexander Lidow**, Manhattan Beach; **Thomas Herman**, Redondo Beach; **Vladimir Rumennik**, El Segundo, all of Calif.

Reexamination Request:
No. 90/002,478, Oct. 9, 1991

Reexamination Certificate for:

Patent No.:	5,008,725
Issued:	Apr. 16, 1991
Appl. No.:	291,423
Filed:	Dec. 23, 1988

Certificate of Correction issued May 5, 1992.

Related U.S. Application Data

[63] Continuation of Ser. No. 243,544, Mar. 13, 1981, abandoned, which is a continuation of Ser. No. 38,662, May 14, 1979, abandoned.

[51] **Int. Cl.^{5}** H01L 29/10; H01L 29/78; H01L 29/68

[52] **U.S. Cl.** 257/335; 257/341; 257/776

[58] **Field of Search** 357/23.4, 23.8

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,015,278	3/1977	Fukuta	357/22
4,028,717	6/1977	Joy et al.	357/23.8
4,072,975	2/1978	Ishitani	357/23.4
4,078,947	3/1978	Johnson et al.	357/23.4
4,145,700	3/1979	Jambotkar	357/23
4,145,703	3/1979	Blanchard	357/55
4,959,699	9/1990	Lidow et al.	357/23.7
5,047,820	9/1991	Garnett	357/23.8

FOREIGN PATENT DOCUMENTS

51-85381	7/1976	Japan .	
52-106688	9/1977	Japan	29/78
54-885	1/1979	Japan	357/23.4

OTHER PUBLICATIONS

Yoshida et al., "A High Power MOSFET With A Vertical Drain Electrode And A Meshed Gate Structure," *IEEE Journal of Solid-State Circuits*, vol. SC-11, No. 4, Aug. 1976, pp. 472-477.

Hayashi et al., "DNA MOS Transistor And Its Integrated Circuit," Proceedings of the Eighth Conference on Solid State Devices, *Japanese Journal of Applied Physics*, vol. 16, pp. 163-166 (1976).

Tarui et al., "Diffusion Self-aligned MOST: A New Approach for High Speed Device," Proceedings of the First Conference on Solid State Devices, *Journal of the Japan Society of Applied Physics*, vol. 39, pp. 105-110 (1969).

Nagata, "Power Handling Capability of MOSFET," *Japanese Journal of Applied Physics*, vol. 16 (1977), Supplement 16-1, pp. 217-222.

Rexer Declaration Executed 16 Jan. 1991.

Rexer Declaration Executed 14 Jun. 1991.

Neilson Declaration Executed 16 Jan. 1991.

Neilson Declaration Executed 14 Jun. 1991.

J. Sansbury, "Applications of Ion Implantation in Semiconductor Processing", *Solid State Technology* (Nov. 1976), pp. 31-37.

J. L. Stone et al., "Recent Advances in Ion Implantation—A State of the Art Review", *Solid State Technology* (Jun. 1976) pp. 35-44.

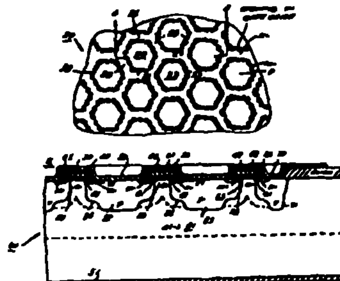
R. J. Duchynski, "Ion Implantation for Semiconductor Devices", *Solid State Technology* (Nov. 1977) pp. 53-58.

Overviews of Sessions 6, 12, 18 and 29, *Technical Digest, International Electron Devices Meeting* (Dec. 1989).

Primary Examiner—J. Carroll

[57] **ABSTRACT**

A high power MOSFET has a plurality of closely packed polygonal sources spaced from one another on one surface of a semiconductor body. An elongated gate electrode is exposed in the spacing between the polygonal sources and cooperates with two channels, one for each adjacent source electrode, to control conduction from the source electrode through the channel and then to a drain electrode on the opposite surface of the semiconductor body. The conductive region adjacent the channel and between adjacent sources is relatively highly conductive in the section of the channel adjacent to the surface containing the sources. The polygonal shaped source members are preferably hexagonal so that the distances between adjacent sources is relatively constant throughout the device. Each polygonal region has a relatively deep central portion and a shallow outer shelf portion. The shelf portion generally underlies an annular source region. The deep central portion underlies an aluminum conductive electrode and is sufficiently deep that it will not be fully penetrated by aluminum spiking.



REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; *matter printed in italics indicates additions made to the patent.*

AS A RESULT OR REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims 1, 3, 7 and 8 are determined to be patentable as amended.

Claims 2, 4 to 6, and 9 to 14, dependent on an amended claim, are determined to be patentable.

1. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:
- a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;
- a plurality of symmetrically disposed laterally distributed *identical* hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface;
- said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;
- *said lattice being continuous and uninterrupted;*
- each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;
- a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;
- an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;
- a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;
- a drain electrode connected to said second planar surface of said wafer;
- an insulation layer means on said first planar surface and overlying at least said annular channels; and
- a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

3. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:
- a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;
- a plurality of symmetrically disposed laterally distributed *identical* polygonal base regions each having a second conductivity type formed in said lightly doped region and extending for given depth beneath said first planar semiconductor surface;
- said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;
- *said lattice being continuous and uninterrupted;*
- each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;
- a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;
- an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;
- a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;
- a drain electrode connected to said second planar *semiconductor surface of said wafer;*
- an insulation layer means on said first planar surface and overlying at least said annular channels; and
- a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

7. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:
- a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;
- a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;
- *said lattice being continuous and uninterrupted;* the space between adjacent ones of said polygonal base regions defining a commonconduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface; and

a drain electrode coupled to said drain conductive region.

8. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

the surface of said common conduction region being continuous and uninterrupted and of said first conductivity type;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

each of said at least first and second spaced base regions having [a polygonal configuration] *identical polygonal configurations*; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,008,725

DATED : April 16, 1991

INVENTOR(S) : Alexander Lidow et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page item [57]:

Abstract line 8, change "them" to -- then --.

Column 6, line 44, change "40M," to -- epitaxially deposited region --.

Column 8, line 46, change "35 or 36" to -- 7 or 8 --.

line 55, change "32, 35 or 36" to -- 3, 7 or 8 --.

Signed and Sealed this

Fifth Day of May, 1992

Attest:

DOUGLAS B. COMER

Attesting Officer

Acting Commissioner of Patents and Trademarks

US005130767A

United States Patent [19]

Lidow et al.

[11] Patent Number: 5,130,767

[45] Date of Patent: * Jul. 14, 1992

[54] PLURAL POLYGON SOURCE PATTERN FOR MOSFET

[75] Inventors: Alexander Lidow, Manhattan Beach; Thomas Herman, Redondo Beach; Vladimir Rumennik, El Segundo, all of Calif.

[73] Assignee: International Rectifier Corporation, El Segundo, Calif.

[*] Notice: The portion of the term of this patent subsequent to Apr. 16, 2008 has been disclaimed.

[21] Appl. No.: 653,017

[22] Filed: Feb. 8, 1991

Related U.S. Application Data

[63] Continuation of Ser. No. 291,423, Dec. 23, 1988, Pat. No. 5,008,725, which is a continuation of Ser. No. 243,544, Mar. 13, 1981, abandoned, which is a continuation of Ser. No. 38,662, May 14, 1979, abandoned.

[51] Int. Cl.[5] H01L 29/78

[52] U.S. Cl. 357/23.4; 357/23.1; 357/23.14; 357/45

[58] Field of Search 357/23.1, 23.4, 23.14, 357/45

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,484,865	12/1969	Nienhuis	357/23.4
3,786,319	1/1974	Tomisaburo	357/23.4
4,015,278	3/1977	Fukuta	357/23.4
4,072,975	2/1978	Ishitani	357/23.4
4,145,700	3/1979	Jambotkar	357/23.4
4,145,703	3/1979	Blanchard et al.	357/23.4
4,148,047	4/1979	Hendrickson	357/23.4
4,173,022	10/1979	Dingwall	357/23.4
4,206,469	6/1980	Hanes et al.	357/23.4
4,376,286	3/1983	Lidow et al.	357/23.4
4,399,449	8/1983	Herman et al.	357/23.4
4,593,302	6/1986	Lidow et al.	357/23.4
4,680,853	7/1987	Lidow et al.	357/23.4
5,008,725	4/1991	Lidow et al.	357/45

FOREIGN PATENT DOCUMENTS

51-85381	7/1976	Japan	357/23.4
54-885	1/1979	Japan	357/23.4
1153428	5/1969	United Kingdom	357/23.4
1224335	3/1971	United Kingdom	357/23.4
1372086	10/1974	United Kingdom	357/23.4
1390135	4/1975	United Kingdom	357/23.4
1400574	7/1975	United Kingdom	357/23.4
145580	11/1976	United Kingdom	357/23.4
1465244	2/1977	United Kingdom	357/23.4

OTHER PUBLICATIONS

R. C. Cady, Jr. and R. R. Silverman, Integration Technique for Closed Field-Effect Transitors, Apr. 1974, IBM Technical Disclosure Bulletin, vol. 16, Nov. 11, pp. 3519-3520.

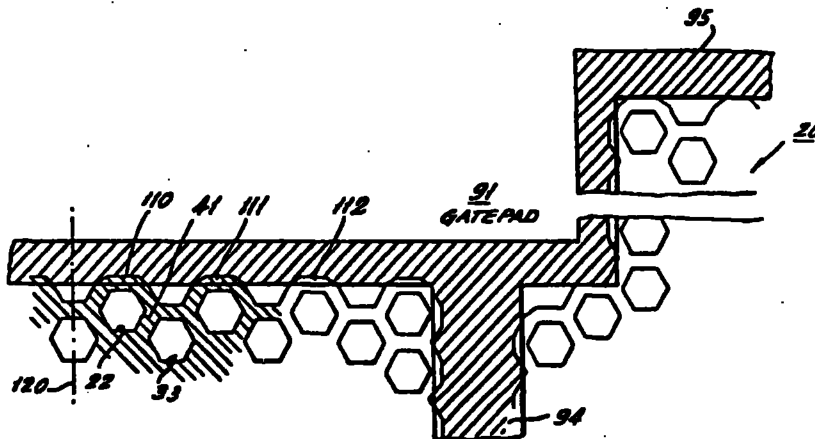
H. William Collins, The Hexfet: A new high in power MOS, Jun. 7, 1979, Electronic Design.

Primary Examiner—Rolf Hille
Assistant Examiner—Steven Loke
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen

[57] **ABSTRACT**

A high power MOSFET has a plurality of closely packed polygonal sources spaced from one another on one surface of a semiconductor body. An elongated gate electrode is exposed in the spacing between the polygonal sources and cooperates with two channels, one for each adjacent source electrode, to control conduction from the source electrode through the channel and then to a drain electrode on the opposite surface of the semiconductor body. The conductive region adjacent the channel and between adjacent sources is relatively highly conductive in the section of the channel adjacent to the surface containing the sources. The polygonal shaped source members are preferably hexagonal so that the distance between adjacent sources is relatively constant throughout the device. Each polygonal region has a relatively deep central portion and a shallow outer shelf portion. The shelf generally underlies an annular source region. The deep central portion underlies an aluminum conductive electrode and is sufficiently deep that it will not be fully penetrated by aluminum spiking.

8 Claims, 3 Drawing Sheets



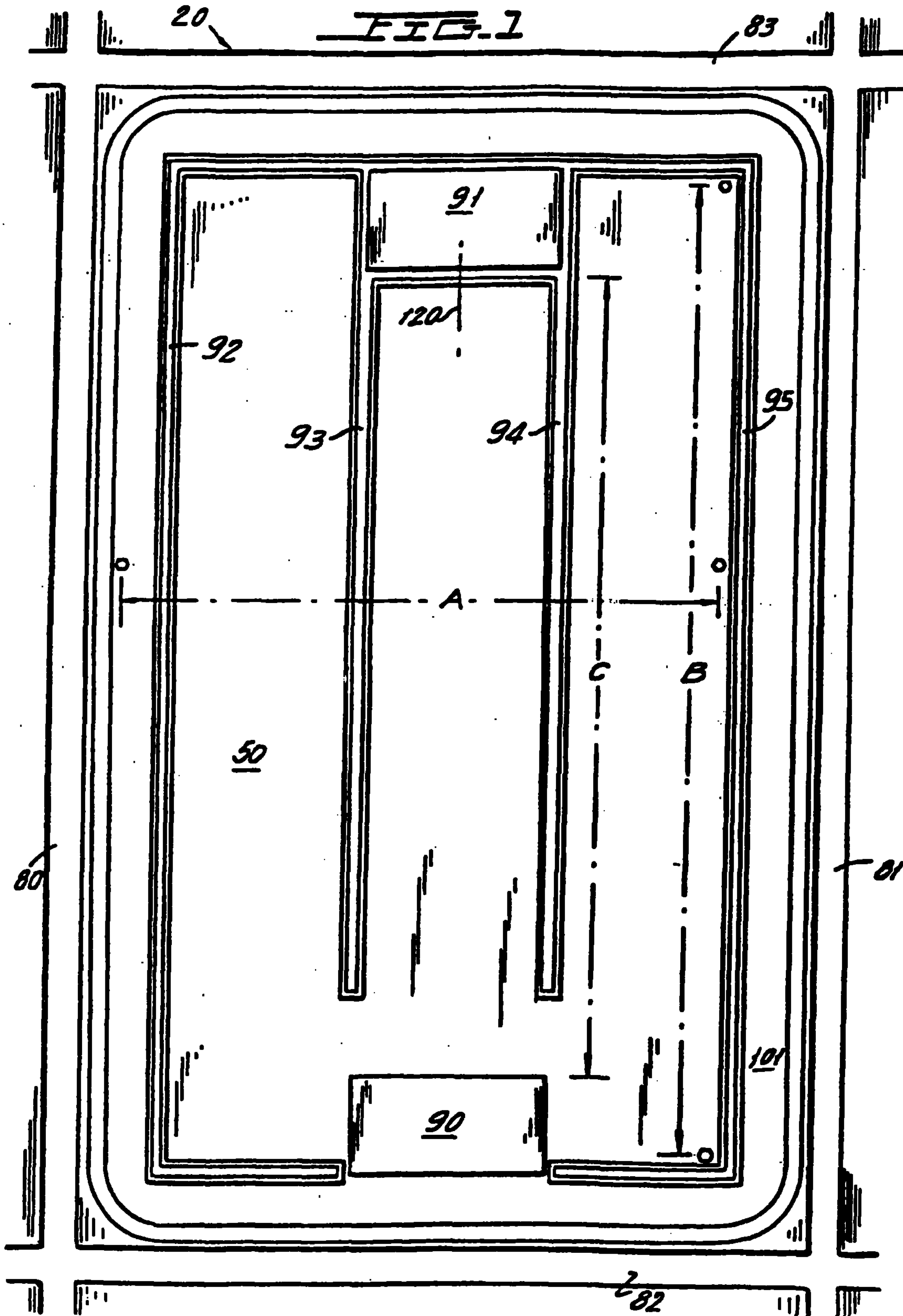


FIG-1
20
83
91
120
92
93
94
95
A
C
B
50
80
81
101
90
82

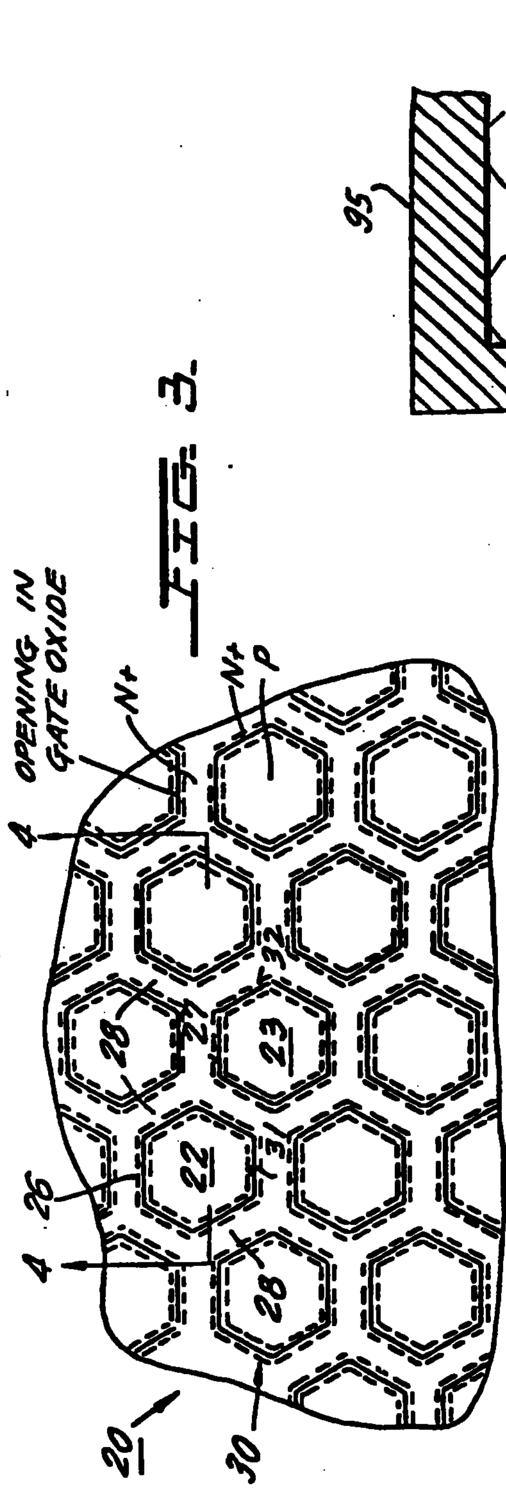


FIG. 3.

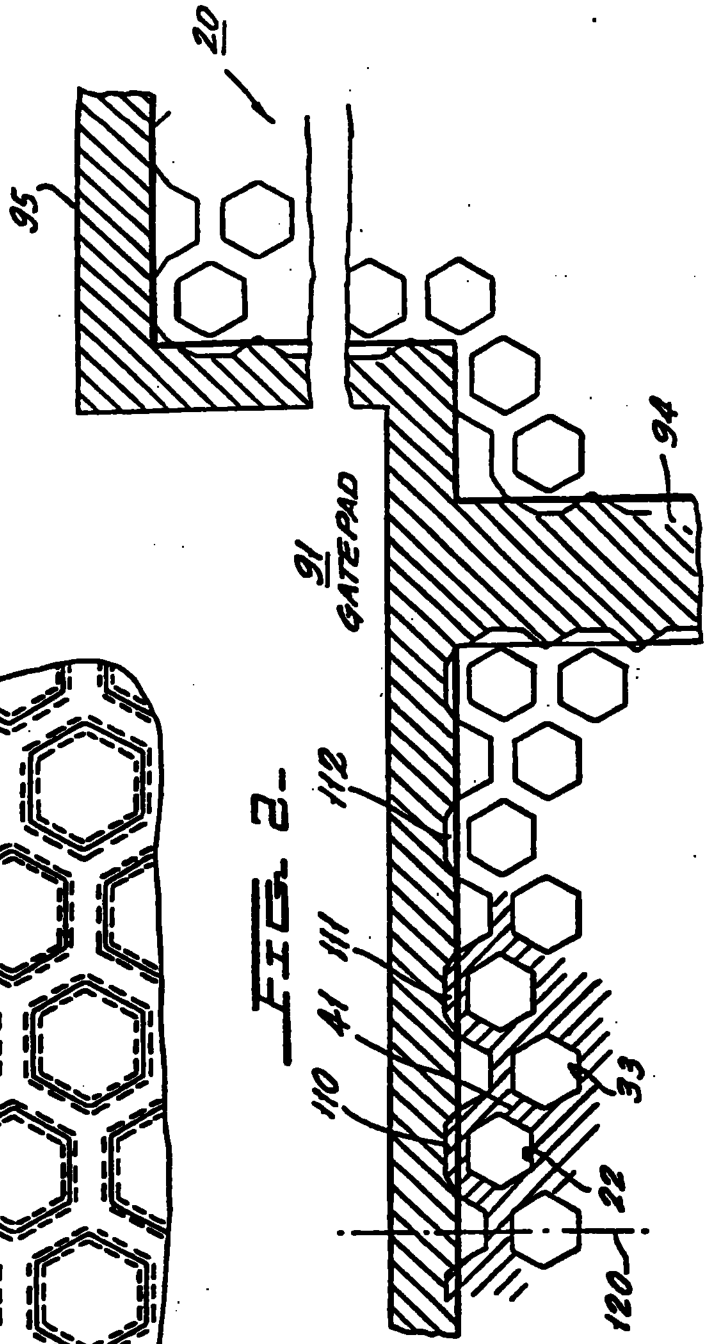
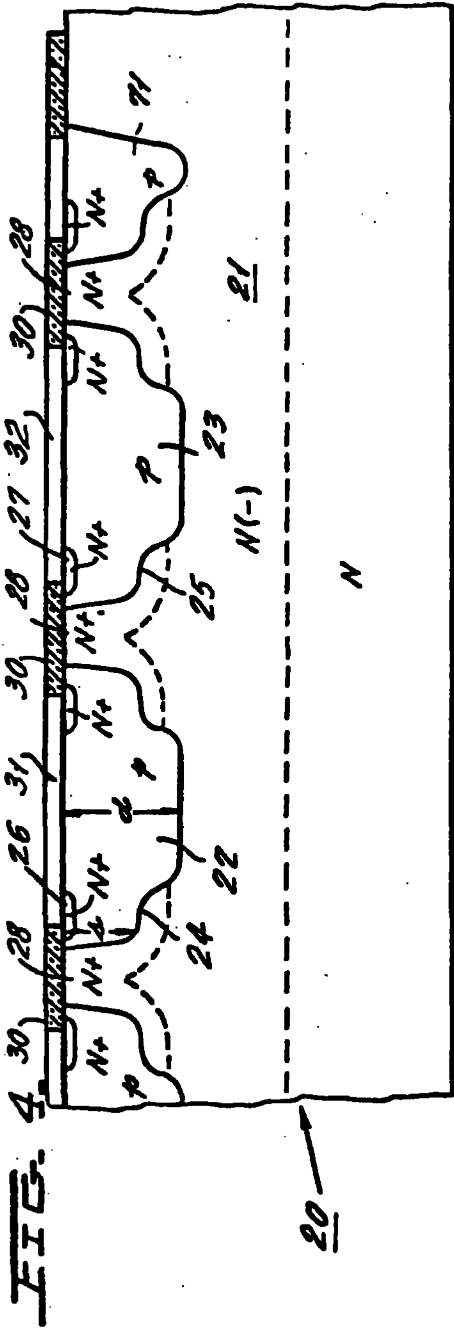
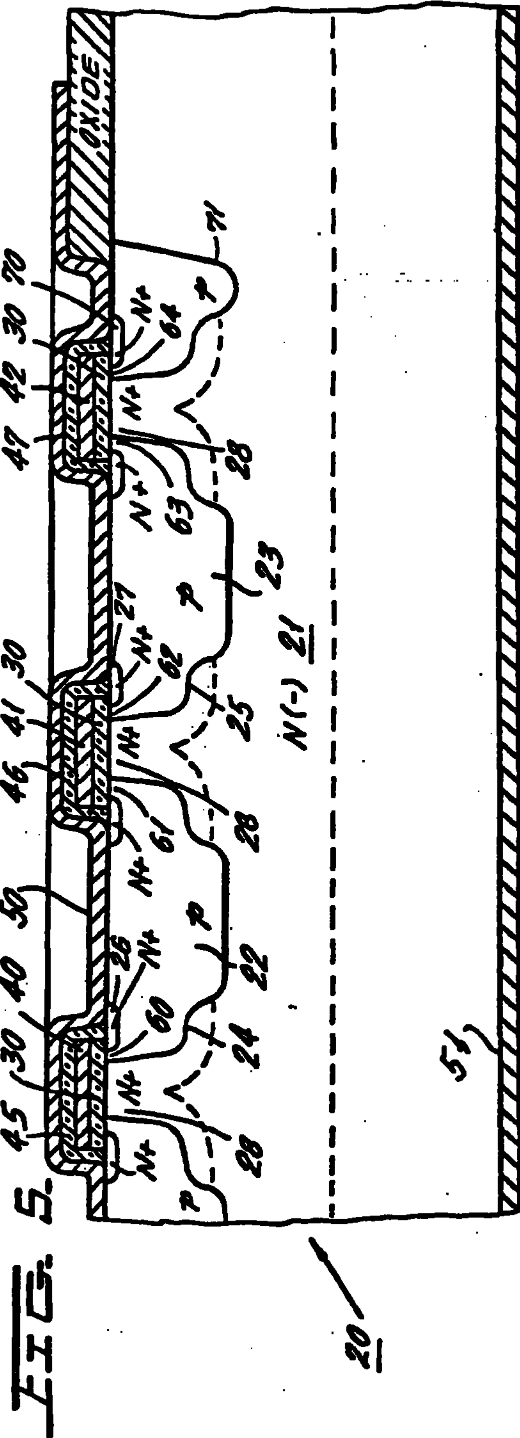


FIG. 2.

Case 2:00-cv-06756-R-CT Document 1 Filed 06/22/00 Page 45 of 76 Page ID #:973





PLURAL POLYGON SOURCE PATTERN FOR MOSFET

This is a continuation of application Ser. No. 07/291,423, filed Dec. 23, 1988, now U.S. Pat. No. 5,008,725, which, in turn, is a continuation of application Ser. No. 06/243,544, filed Mar. 13, 1981 (now abandoned) which, in turn, is a continuation of application Ser. No. 06/038,662, filed May 14, 1979 (now abandoned).

RELATED APPLICATIONS

This application is related to application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned and refiled as continuation application Ser. No. 232,713, filed Feb. 9, 1981, now U.S. Pat. No. 4,376,286, entitled HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE, in the names of Alexander Lidow and Thomas Herman, and assigned to the assignee of the present invention.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices, and more specifically relates to a novel source pattern for a MOSFET device of the type disclosed in above-mentioned U.S. Pat. No. 4,376,286 wherein a plurality of polygonal-shaped source elements are disposed over the surface of a semiconductor body and are spaced from one another by a closely controlled dimension.

High power MOSFETS having low on-resistance and high breakdown voltage are known and are shown in the above-noted U.S. Pat. No. 4,376,286. In the above application, the source electrodes are spaced, interdigitated source regions spaced from one another by two parallel channel regions covered by a common gate. The device has exceptionally low on-resistance along with the usual advantages of the MOSFET device over the bi-polar device particularly by virtue of a relatively high conductivity region disposed between the two adjacent channels and leading to a common drain electrode.

It has been found that an interdigitated structure has a relatively low packing density. Moreover, the interdigitated arrangement disclosed in the above U.S. Pat. No. 4,376,286 requires relatively complicated masks and has a relatively high capacitance.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device with low forward resistance where, a very high packing density is available and which can be made with relatively simple masks. The device further has relatively low capacitance. Typically, the device may be made through the use of phosphorus implantation and D-MOS fabrication techniques but any desired technique can be used.

Each of the individual spaced source regions, in accordance with the invention, is polygonal in configuration and is preferably hexagonal to ensure a constant spacing along the major lengths of the sources disposed over the surface of the body. An extremely large number of small hexagonal source elements may be formed in the same surface of the semiconductor body for a given device. By way of example, 6,600 hexagonal source regions can be formed in a chip area having a dimension of about 100 by 140 mils to produce an effective channel width of about 22,000 mils, thus permitting very high current capacity for the device.

The space between the adjacent sources may contain a polysilicon gate or any other gate structure where the gate structure is contacted over the surface of the device by elongated gate contact fingers which ensure good contact over the full surface of the device.

Each of the polygonal source regions is contacted by a uniform conductive layer which engages the individual polygonal sources through openings in an insulation layer covering the source regions, which openings can be formed by conventional D-MOS photolithographic techniques. A source pad connection region is then provided for the source conductor and a gate pad connection region is provided for the elongated gate fingers and a drain connection region is made to the reverse surface of the semiconductor device.

A plurality of such devices can be formed from a single semiconductor wafer and the individual elements can be separated from one another by scribing or any other suitable method.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a completed element on a semiconductor wafer prior to the separation of the element away from the remainder of the wafer.

FIG. 2 is an enlarged detail of the gate pad to illustrate the relationship of the gate contact and the source polygons in the region of the gate pad.

FIG. 3 is a detailed plan view of a small portion of the source region during one stage of the manufacturing process of the device.

FIG. 4 is a cross-sectional view of FIG. 3 taken across the section line 4—4 in FIG. 3.

FIG. 5 is similar to FIG. 4 and shows the addition of a polysilicon gate, a source electrode means and drain electrode to the wafer.

DETAILED DESCRIPTION OF THE DRAWINGS

The polygon configuration of the source regions of the present invention is best shown in FIGS. 3, 4 and 5 which are first described.

Referring first to FIGS. 3 and 4, the device is shown prior to the application of the gate, source and drain electrodes. The manufacturing process can be of any desired type. The manufacturing process described in U.S. Pat. No. 4,376,286, referred to above, which is incorporated herein by reference, can be used whereby D-MOS fabrication techniques and ion implantation techniques can be advantageously employed for the formation of the junction and placement of the electrode in the most advantageous way.

The device is described as an N channel enhancement type device. It will be apparent that the invention will also apply to P channel devices and to depletion mode devices.

The device of FIGS. 3 and 4 has a plurality of polygonal source regions on one surface of the device, where these polygonal regions are preferably hexagonal in shape. Other shapes such as squares could have been used but the hexagonal shape provides better uniformity of spacing between adjacent source region perimeters.

In FIGS. 3 and 4, the hexagonal source regions are formed in a basic semiconductor body or wafer which can be an N type wafer 20 of monocrystalline silicon which has a thin N-epitaxial region 21 deposited thereon as best shown in FIG. 4. All junctions are

formed in epitaxial region 21. By using suitable masks, a plurality of P type regions such as regions 22 and 23 in FIGS. 3 and 4 are formed in one surface of the semiconductor wafer region 21, where these regions are generally polygonal in configuration and, preferably, are hexagonal.

A very large number of such polygonal regions are formed. For example, in a device having a surface dimension of 100 by 140 mils, approximately 6600 polygonal regions are formed to produce a total channel width of about 22,000 mils. Each of the polygonal regions may have a width measured perpendicular to two opposing sides of the polygon of about 1 mil or less. The regions are spaced from one another by a distance of about 0.6 mil when measured perpendicularly between the adjacent straight sides of adjacent polygonal regions.

The P+ regions 22 and 23 will have a depth d which is preferably about 5 microns to produce a high and reliable field characteristic. Each of the P regions has an outer shelf region shown as shelf regions 24 and 25 for P regions 22 and 23, respectively, having a depth s of about 1.5 microns. This depth should be as small as possible to reduce the capacitance of the device.

Each of the polygon regions including polygonal regions 22 and 23 receive N+ polygonal ring regions 26 and 27, respectively. Shelves 24 and 25 are located beneath regions 26 and 27, respectively. N+ regions 26 and 27 cooperate with a relatively conductive N+ region 28 which is the N+ region disposed between adjacent P type polygons to define the various channels between the source regions and a drain contact which will be later described.

The highly conductive N+ regions 28 are formed in the manner described in U.S. Pat. No. 4,376,286, referred to above, and are the subject of that application and produce a very low forward resistance for the device.

In FIGS. 3 and 4, it will be noted that the entire surface of the wafer is covered with an oxide layer or combined conventional oxide and nitride layers which are produced for the formation of the various junctions. This layer is shown as the insulation layer 30. The insulation layer 30 is provided with polygonal shaped opening such as openings 31 and 32 immediately above polygonal regions 22 and 23. Openings 31 and 32 have boundaries overlying the N+ type source rings 26 and 27 for the regions 22 and 23, respectively. The oxide strips 30, which remain after the formation of the polygonal shaped openings, define the gate oxide for the device.

Electrodes may then be applied to the device as shown in FIG. 5. These include a polysilicon grid which includes polysilicon sections 40, 41 and 42 which overlie the oxide sections 30.

A silicon dioxide coating is then deposited atop the polysilicon grid 40 shown as coating sections 45, 46 and 47 in FIG. 5 which insulates the polysilicon control electrode and the source electrode which is subsequently deposited over the entire upper surface of the wafer. In FIG. 5 the source electrode is shown as conductive coating 50 which may be of any desired material, such as aluminum. A drain electrode 51 is also applied to the device.

The resulting device of FIG. 5 is an N channel type device wherein channel regions are formed between each of the individual sources and the body of the semiconductor material which ultimately leads to the drain electrode 51. Thus, a channel region 60 is formed between the source ring 26, which is connected to source electrode 50, and the N+ region 28 which ultimately leads to the drain electrode 51. Channel 60 is inverted to N type conductivity upon the application of a suitable control voltage to the gate 40. In a similar manner, channels 61 and 62 are formed between the source region 26, which is connected to the conductor 50, and the surrounding N+ region 28 which leads to the drain 51. Thus, upon application of a suitable control voltage to the polysilicon gate (including finger 41 in FIG. 5), channels 61 and 62 become conductive to permit majority carrier conduction from the source electrode 50 to the drain 51. Note that channels labeled 60 and 61 of FIG. 5 are the same annular channel which is formed within the region 22. Similarly, channels 62 and 63 are the same annular channel formed in the region 23.

Each of the sources form parallel conduction paths where, for example, channels 63 and 64 beneath gate element 42 permit conduction from the source ring 27 and an N type source strip 70 to the N+ region 28 and then to the drain electrode 51.

It is to be noted that FIGS. 4 and 5 illustrate an end P type region 71 which encloses the edge of the wafer.

The contact 50 of FIG. 5 is preferably an aluminum contact. It will be noted that the contact region for the contact 50 lies entirely over and in alignment with the deeper portion of the P type region 22. This is done since it was found that aluminum used for the electrode 50 might spike through very thin regions of the P type material. Thus, one feature of the present invention is to ensure that the contact 50 lies principally over the deeper portions of the P regions such as P regions 22 and 23. This then permits the active channel regions defined by the annular shelves 24 and 25 to be as thin as desired in order to substantially reduce the device capacitance.

FIG. 1 illustrates one completed device using the polygonal source pattern of FIG. 5. The completed device shown in FIG. 1 is contained within the scribe regions 80, 81, 82 and 83 which enable the breaking out of a plurality of unitary devices each having a dimension of 100 by 140 mils from the body of the wafer.

The polygonal regions described are contained in a plurality of columns and rows. By way of example, the dimension A contains 65 columns of polygonal regions and may be about 83 mils. The dimension B may contain 100 rows of polygonal regions and may be about 148 mils. Dimension C, which is disposed between a source connection pad 90 and a gate connection pad 91, may contain 82 rows of polygonal elements.

The source pad 90 is a relatively heavy metal section which is directly connected to the aluminum source electrode 50 and permits convenient lead connection for the source.

The gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which extend symmetrically over the outer surface of the area containing the polygonal regions and make electrical connection to the polysilicon gate as will be described in connection with FIG. 2.

Finally the outer circumference of the device contains the P+ (shown as "P" in the drawings) deep diffusion ring 71 which may be connected to a field plate 101 shown in FIG. 1.

FIG. 2 shows a portion of the gate pad 91 and the gate fingers 94 and 95. It is desirable to make a plurality of contacts to the polysilicon gate in order to reduce the R-C delay constant of the device. The polysilicon gate

has a plurality of regions including regions 110, 111, 112 and the like which extend outwardly and receive extensions of the gate pad and the gate pad elements 94 and 95. The polysilicon gate regions may be left exposed during the formation of the oxide coating 45-46-47 in FIG. 5 and are not coated by the source electrode 50. Note that in FIG. 2 the axis 120 is the axis of symmetry 120 which is that shown in FIG. 1.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising;

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of symmetrically disposed laterally distributed hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface;

said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;

each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;

a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

a drain electrode connected to said second planar surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels;

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

2. The device of claim 1 wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

3. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of symmetrically disposed laterally distributed polygonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for given depth beneath said first planar semiconductor surface;

said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

a drain electrode connected to said second planar semiconductor surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels;

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

4. The device of claim 3 wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

5. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising;

a wafer of semiconductor material having planar first and second opposing semiconductor surface; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type; the space between adjacent ones of said polygonal base regions defining a common conduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

6. The device of claim 5 wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

7. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region;

each of said at least first and second spaced base regions having a polygonal configuration; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region; and

a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality of spaced locations over the surface of said polysilicon gate electrode, thereby to reduce the R-C delay constant of said device.

8. The device of claim 7 wherein said annular channels have at least one leg in longitudinal alignment with other legs of other of said annular channels; said plurality of spaced locations disposed along a line defined by said legs of said annular channels which are in longitudinal alignment.

* * * * *

United States Patent [19]
Lidow et al.
[11] Patent Number: 4,642,666
[45] Date of Patent: Feb. 10, 1987

[54] **HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE**

[75] Inventors: Alexander Lidow, Manhattan; Thomas Herman, Redondo, both of Calif.

[73] Assignee: International Rectifier Corporation, Los Angeles, Calif.

[21] Appl. No.: 471,818

[22] Filed: Mar. 3, 1983

Related U.S. Application Data

[60] Division of Ser. No. 232,713, Feb. 9, 1981, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] Int. Cl.^{4} H01L 29/78
[52] U.S. Cl. 357/23.4
[58] Field of Search .... 357/23 VD, 23 R

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,461,360	8/1969	Barson	357/23 VD
4,001,860	1/1977	Cauge	357/23 VD
4,072,975	2/1978	Ishitani	357/23 VD

FOREIGN PATENT DOCUMENTS

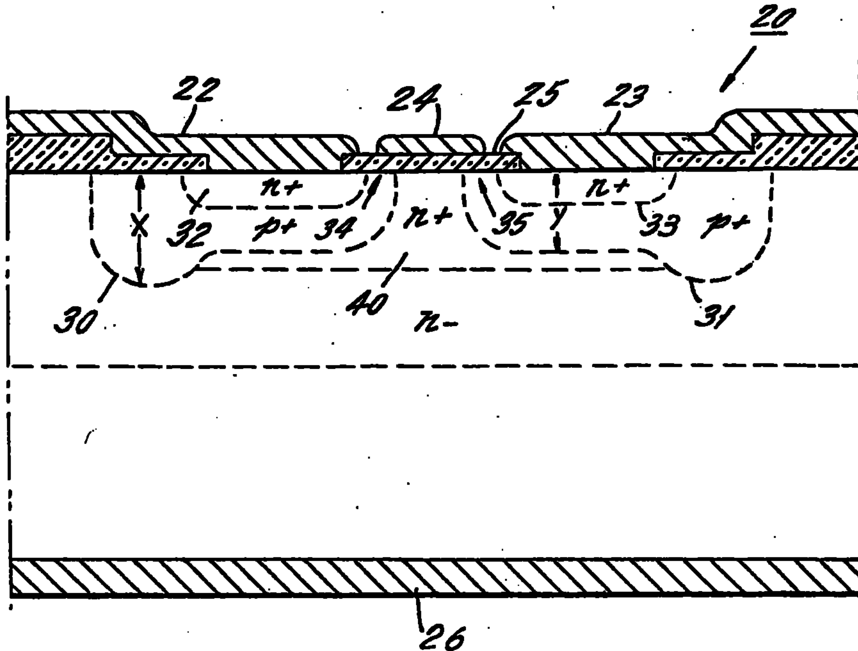
5046081	8/1973	Japan	357/23 VD
52-106688	9/1977	Japan .	

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

10 Claims, 11 Drawing Figures



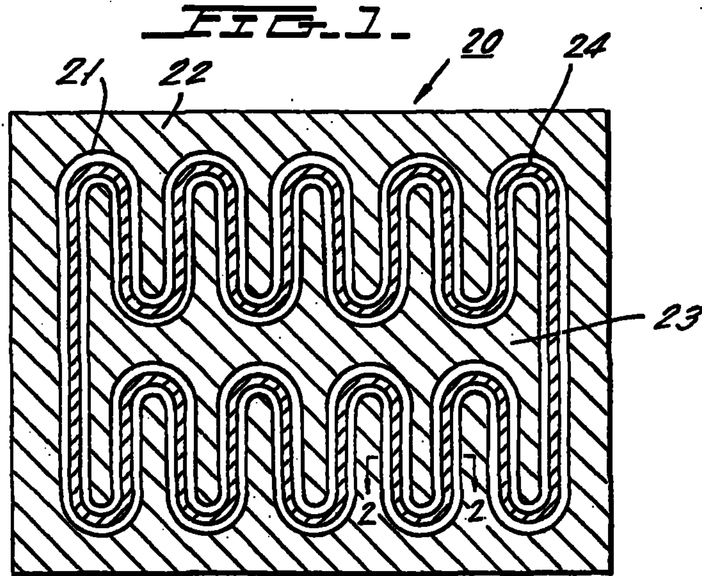


FIG. 1
20
24
21
22
23
2
2

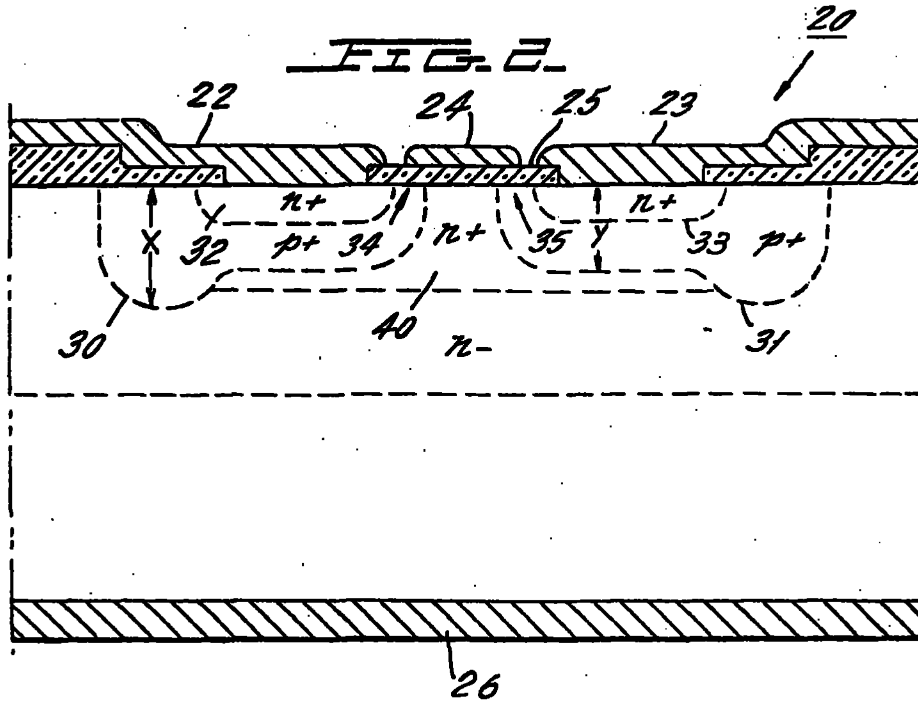


FIG. 2
20
22
24
25
23
n+
n+
X
32
p+
34
n+
35
Y
33
p+
30
40
n-
31
26

FIG. 3.

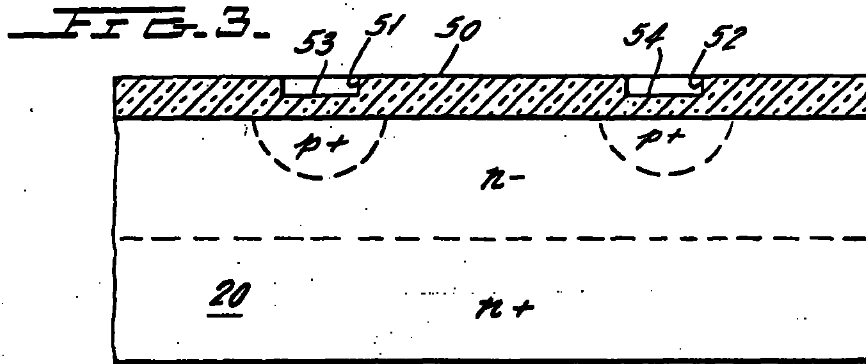


FIG. 4.

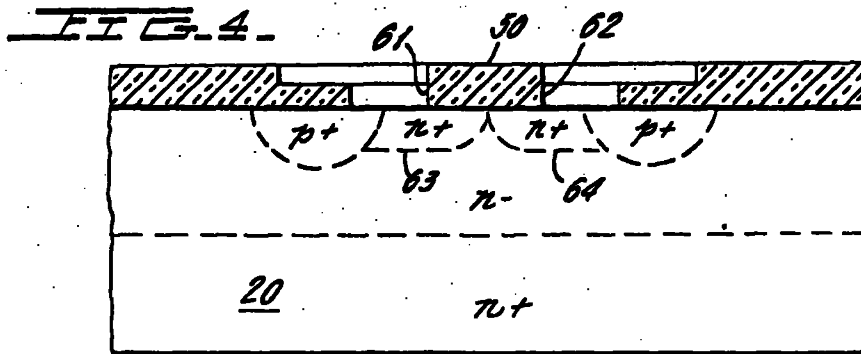


FIG. 5.

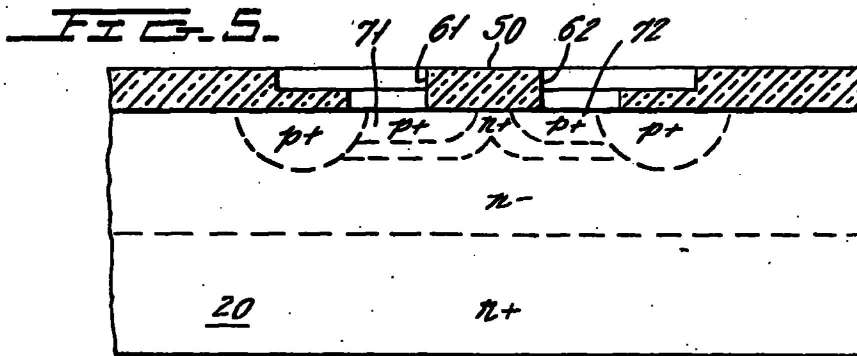
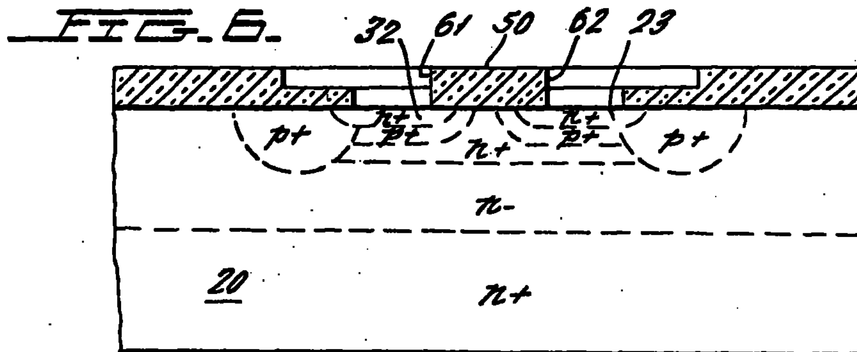
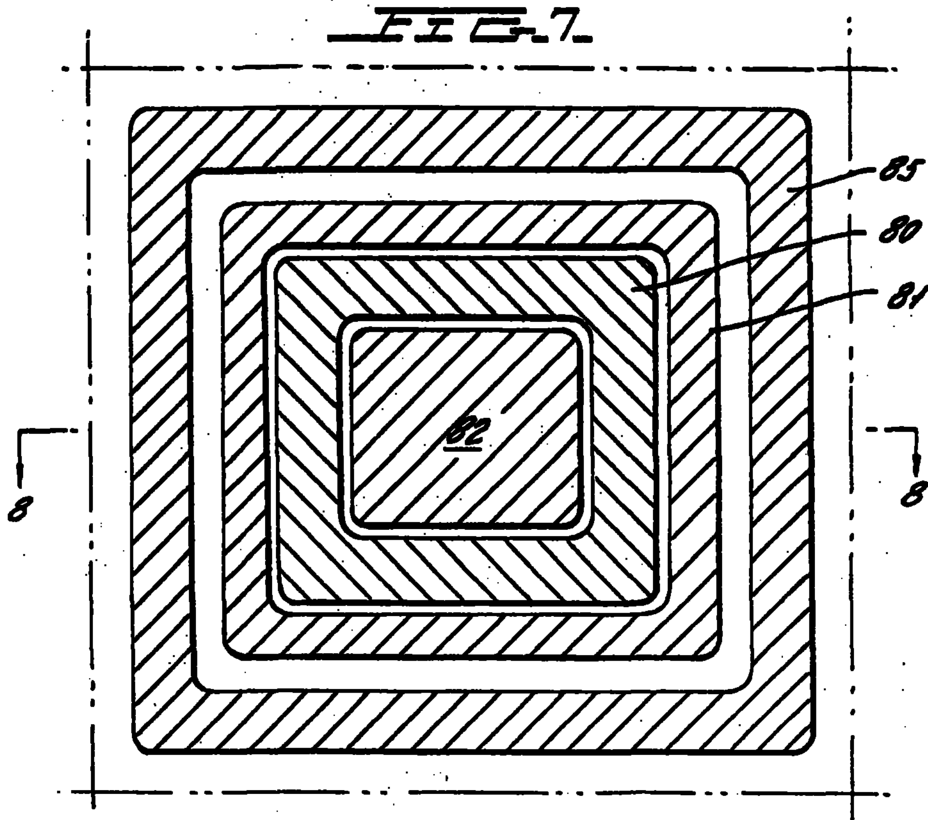


FIG. 6.





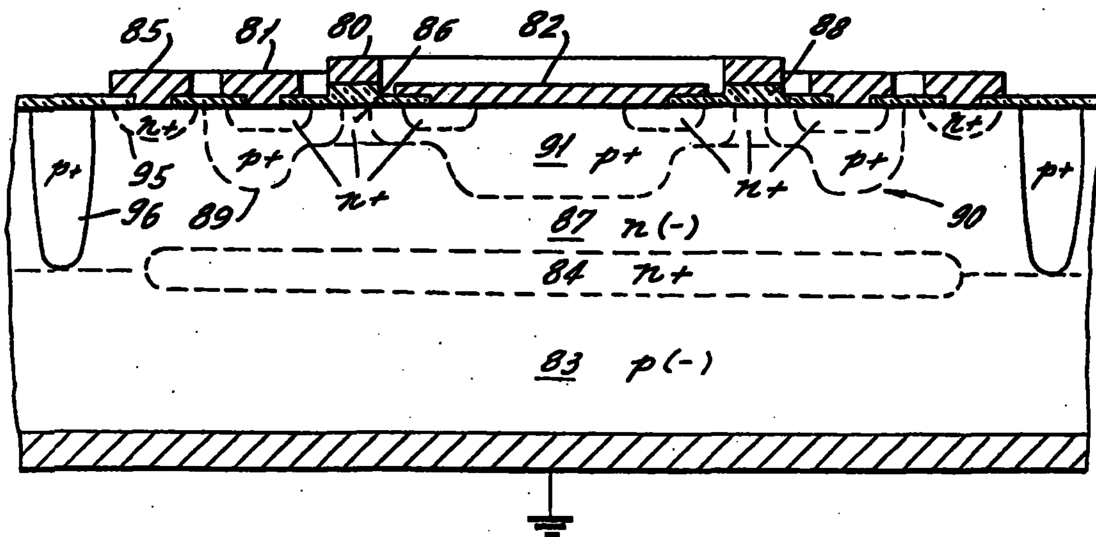


FIG. 8

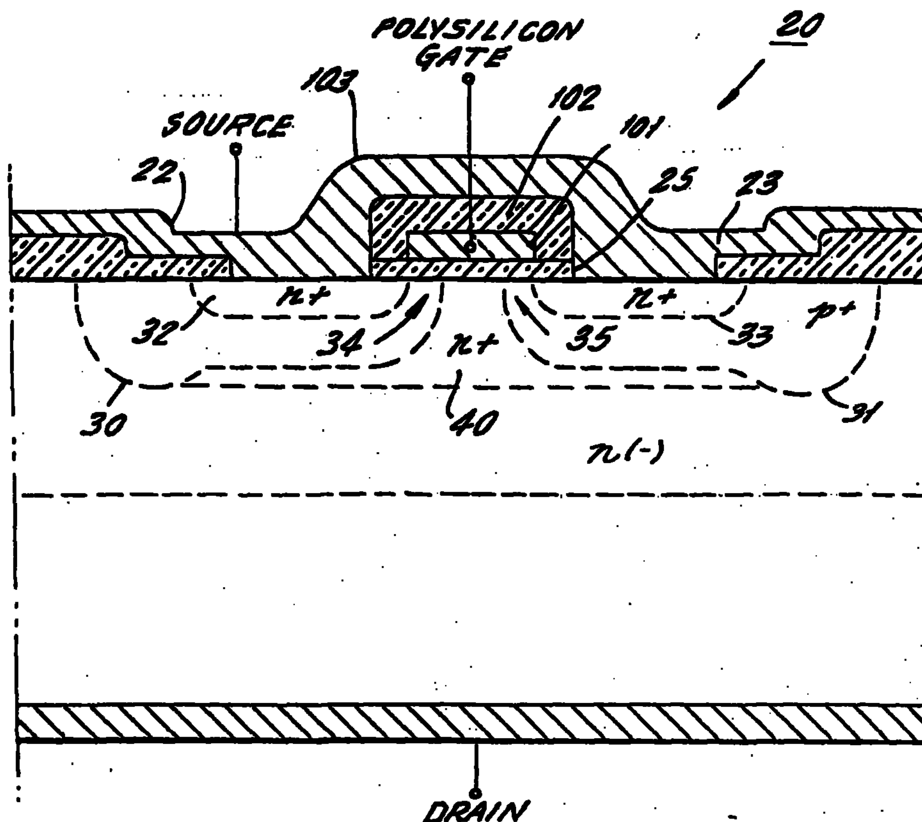


FIG. 8a

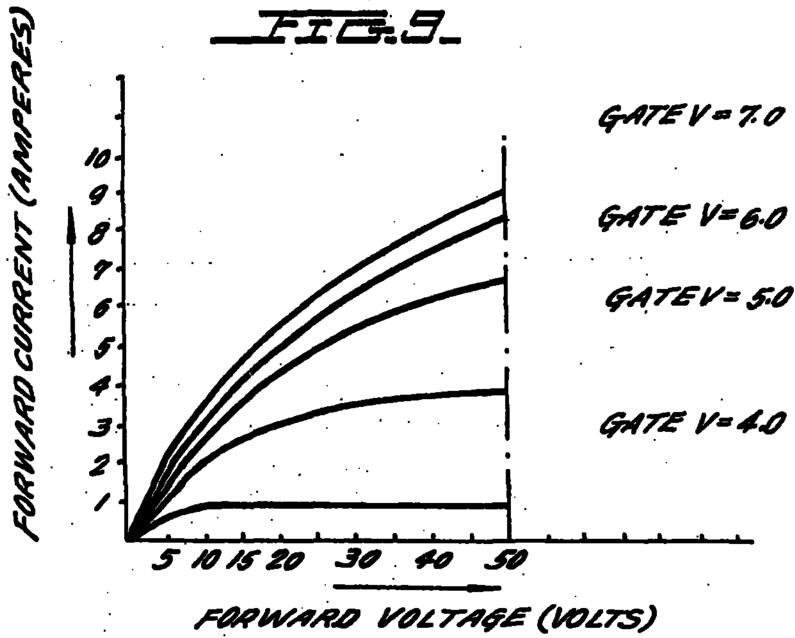


FIG. 9
FORWARD CURRENT (AMPERES)
1
2
3
4
5
6
7
8
9
10
GATE V=7.0
GATE V=6.0
GATE V=5.0
GATE V=4.0
5 10 15 20 30 40 50
FORWARD VOLTAGE (VOLTS)

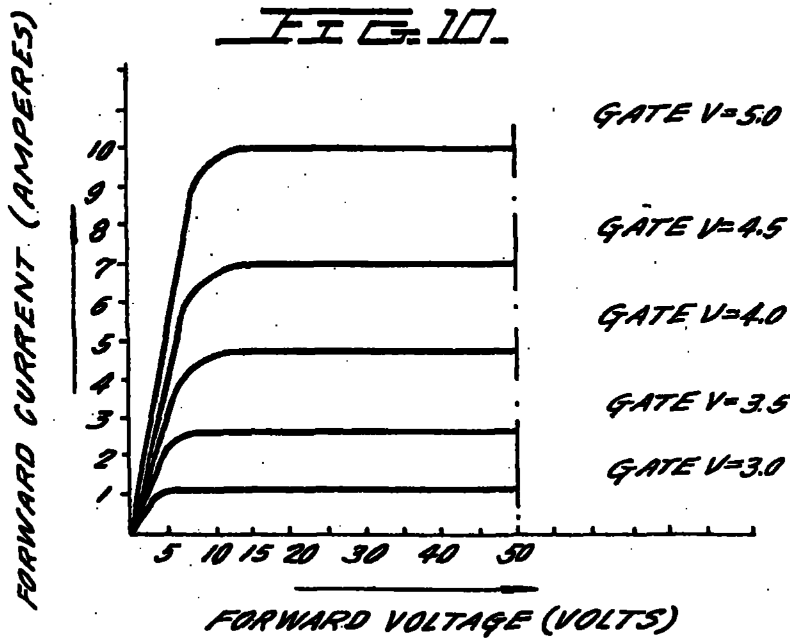


FIG. 10
FORWARD CURRENT (AMPERES)
1
2
3
4
5
6
7
8
9
10
GATE V=5.0
GATE V=4.5
GATE V=4.0
GATE V=3.5
GATE V=3.0
5 10 15 20 30 40 50
FORWARD VOLTAGE (VOLTS)

HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

This is a division of application Ser. No. 232,713, filed Feb. 9, 1981 which, in turn, is a continuation of application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices and more specifically relates to a novel structure for a MOSFET device which permits it to be used in high power applications with a relatively high reverse voltage and with an exceptionally low on-resistance. The major advantage of the bipolar transistor over the MOSFET transistor is that the bipolar transistor has a very low on-resistance per unit conductive area. The MOSFET transistor has numerous advantages over the bipolar transistor including very high switching speed, very high gain and lack of the secondary breakdown characteristics exhibited by a minority carrier device. However, because the MOSFET transistor has high on-resistance, its use in to high power switching applications has been limited.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device which has a low forward resistance so that the device becomes more competitive with bipolar devices in a switching type application while retaining all of the numerous advantages of the MOSFET over the bipolar device. In particular, with the present invention, the forward resistance per unit area of the device has been reduced by at least a factor of two, compared to the limiting resistance per unit area previously existing in a MOSFET-type device.

In one embodiment of the invention, two sources are placed on the same surface of a semiconductor wafer and are laterally spaced from one another. A gate electrode, deposited on a conventional gate oxide, is disposed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced from one another by an n-type bulk region. Current from each source can flow through its respective channel (after the creation of the inversion layer defining the channel), so that majority carrier conduction current can flow through the bulk region and across the wafer or chip to the drain electrode. The drain electrode may be on the opposite surface of the wafer or on a laterally displaced surface region from the source electrodes. This configuration is made using the desirable manufacturing techniques of the D-MOS device, which permits precise alignment of the various electrodes and channels and permits use of extremely small channel lengths. While the above configuration may have been previously described for a MOSFET signal-type device, the structure is not that of the commonly used signal MOSFET.

The device is basically formed in an n(−) substrate which has the relatively high resistivity which is necessary to obtain the desired reverse voltage capability of the device. For example, for a 400 volt device, the n(−) region will have a resistivity of about 20 ohm-centimeters. However, this same necessary high resistivity characteristic has caused the on-resistance of the MOSFET device, when used as a power switch, to be relatively high.

In accordance with the present invention, it has been found that in the upper portion of the central bulk region to which the two inversion layers feed current in the path to the drain electrode, the central region immediately beneath the gate oxide can be a relatively low resistivity material formed, for example, by an n(+) diffusion in that channel region, without effecting the reverse voltage characteristics of the device.

More specifically, and in accordance with the invention, this common channel will have an upper portion beneath the gate oxide and a lower bulk portion extending toward the drain electrode. The lower portion has the high resistivity desired to produce high reverse voltage ability, and will have a depth dependent on the desired reverse voltage for the device. Thus, for a 400 volt device, the lower n(−) region may have a depth of about 35 microns, while for a 90 volt device it will have a depth of about 8 microns. Other depths will be selected, depending on the desired reverse voltage of the device to provide the necessary thicker depletion region required to prevent punch-through during reverse voltage conditions. The upper portion of the common channel is made highly conductive (n+) to a depth of from about 3 to about 6 microns. It has been found that this does not interfere with the reverse voltage withstand ability of the device. However, it decreases the on-resistance per unit area of the device by more than a factor of two. The resulting device becomes competitive with conventional high power bipolar switching devices since it retains all of the advantages of the MOSFET device over the bipolar device but now has the relatively low forward resistance which was the major characterizing advantage of the bipolar device.

In accordance with another feature of the present invention, the p-type region which defines the channel beneath the gate oxide has a relatively deeply diffused portion beneath the source so that the p-type diffusion region will have a large radius of curvature in the n(−) epitaxial layer forming the body of the device. This deeper diffusion or deeper junction has been found to improve the voltage gradient at the edge of the device and thus permits the use of the device with higher reverse voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a high power MOSFET chip which incorporates the present invention and particularly illustrates the metalizing patterns of the two sources and the gate.

FIG. 2 is a cross-sectional view of FIG. 1 taken across the section line 2—2 in FIG. 1.

FIG. 3 is a cross-sectional view similar to FIG. 2 showing the initial step in the process of manufacture of the chip of FIGS. 1 and 2 and particularly shows the p(+) conductivity implant and diffusion step.

FIG. 4 shows the second step in the manufacturing process and shows the n(+) implant and diffusion step.

FIG. 5 shows a further step in the process of manufacture of the chip of FIGS. 1 and 2 and shows the channel implant and diffusion step.

FIG. 6 shows a further step in the process of manufacture and illustrates the source predeposition and diffusion step. This precedes the last step in which the gate oxide is cut for the metalization step which produces the device of FIG. 2.

FIG. 7 is a plan view of the metalizing pattern of a second embodiment of the invention.

FIG. 8 is a cross-sectional view of FIG. 7 taken across the section line 8—8 in FIG. 7.

FIG. 8a is a view similar to FIG. 2 and shows a modified source contact configuration.

FIG. 9 shows the shape of forward-current characteristics of a device like that of FIG. 2 where the region 40 beneath the oxide is n(−).

FIG. 10 shows the shape of the characteristic of a device identical to that of FIG. 2 where the region 40 has high n(+) conductivity.

DETAILED DESCRIPTION OF THE DRAWINGS

A first embodiment of the novel MOSFET device of the present invention is shown in FIGS. 1 and 2 which show a chip of monocrystalline silicon 20 (or some other suitable material), with the device electrodes following the serpentine path 21 best shown in FIG. 1 in order to increase the current-carrying area of the device. Other geometries could be used. The device illustrated has a reverse voltage of about 400 volts and an on-resistance less than about 0.4 ohm with a channel width of 50 centimeters. Devices having reverse voltages of from 90 to 400 volts have been made. The 400 volt devices have carried pulse currents of 30 amperes. The 90 volt devices have had forward on-resistances of about 0.1 ohm with a channel width of 50 centimeters and have carried pulse currents up to about 100 amperes. Higher and lower voltage devices can also be made with varying channel widths.

Presently known MOSFET devices have much higher on-resistances than the above. For example, a 400 volt MOSFET comparable to that described below but made with prior art techniques would normally have an on-resistance much greater than about 1.5 ohms, as compared to an on-resistance less than about 0.4 ohm in a device made according to this invention. Moreover, the MOSFET switching device of the present invention will exhibit all of the desirable advantages of the MOSFET device, since it operates as a majority carrier device. These advantages include high switching speed, high gain and avoidance of the secondary breakdown characteristics which exist in minority carrier devices.

The device of FIGS. 1 and 2 has two source electrodes 22 and 23 which are separated by a metalized gate electrode 24 which is fixed to but spaced from the semiconductor device surface by a silicon dioxide layer 25. The serpentine path followed by gate oxide 25 has a length of 50 centimeters and has 667 undulations, but is shown more simply in FIG. 1. Other channel widths can be used. Source electrodes 22 and 23 can be laterally extended as shown to serve as field plates to help spread the depletion region created during reverse voltage conditions. Each of source electrodes 22 and 23 supply current to a common drain electrode 26 which is fixed to the bottom of the wafer. The relative dimensions for the device, particularly in thickness, have been grossly exaggerated in FIG. 2 for purposes of clarity. The silicon chip or wafer 20 is formed on an n(+) substrate which may have a thickness of about 14 mils. An n(−) epitaxial layer is deposited on substrate 20 and will have a thickness and resistivity depending on the desired reverse voltage. All junctions are formed in this epitaxial layer which can have a relatively high resistivity. In the embodiment disclosed, the epitaxial layer has a thickness of about 35 microns and a resistivity of about 20 ohm-centimeters. For a 90 volt device, epitaxial layer 20 would be about 10 microns thick and would have a resistivity of about 2.5 ohm-centimeters. A channel width of 50 centimeters is also used to provide the desired current carrying capacity for the device.

In a preferred embodiment of the invention, there is an elongated serpentine p(+) conductivity region beneath each of the source electrodes 22 and 23 which thus extends around the serpentine path shown in FIG. 1. These p(+) regions are shown in FIG. 2 as the p(+) regions 30 and 31, respectively, and are similar to those of the prior art except that the maximum p(+) region depth is greatly exaggerated in order to form a large radius of curvature. This allows the device to withstand higher reverse voltages. By way of example, the depth of regions 30 and 31 is preferably about 4 microns at the dimension X in FIG. 2 and about 3 microns at the dimension Y in FIG. 2.

By using D-MOS fabrication techniques, two n(+) regions 32 and 33 are formed beneath source electrodes 22 and 23, respectively, and define, with the p(+) regions 30 and 31, n-type channel regions 34 and 35, respectively. Channel regions 34 and 35 are disposed beneath the gate oxide 25 and can be inverted by the appropriate application of a biasing signal to the gate 24 in order to permit conduction from the source 22 and the source 23 through the inversion layers into the central region disposed beneath the gate 24 and then to the drain electrode 26. Channels 34 and 35 may each have a length of about 1 micron.

It has previously been thought necessary that the central n(−) region between channels 34 and 35 (and between p(+) regions 30 and 31) should have a high resistivity in order to permit the device to withstand high reverse voltages. However, the relatively high resistivity n(+) material is also a significant contributing factor to the high forward on-resistance of the device.

In accordance with the significant feature of the present invention, a significant portion of this central conducting region is made relatively highly conductive and consists of an n(+) region 40 disposed immediately beneath the gate oxide 25. The n(+) region 40 has a depth of about 4 microns and could range from about 3 microns to about 6 microns. While its exact conductivity is not known, and varies with depth, it is high relative to the n(−) region beneath it. More particularly, region 40 has a high conductivity which would be determined by a total ion implanted dose of from about 1×10^{12} to 1×10^{14} phosphorus atoms/cm^2 at 50 kV followed by a diffusion drive at from 1150° C. to 1250° C. for from 30 minutes to 240 minutes. It has been found that by making this region 40 relatively highly conductive n(+) material through a diffusion or other operation, the device characteristics are significantly improved and the forward on-resistance of the device is reduced by a factor greater than two. Moreover, it has been found that the provision of the high conductivity region 40 does not interfere with the reverse voltage characteristics of the device. Accordingly, by making the region beneath the gate oxide 25 and between channels 34 and 35 more highly conductive, the forward on-resistance of the ultimate high power switching device has been significantly reduced and the MOSFET device becomes far more competitive with an equivalent junction-type device while still retaining all of the advantages of the MOSFET majority carrier operation.

In the above description of FIGS. 1 and 2, it has been assumed that the conduction channels 34 and 35 are of

p(+) material and are, accordingly, inverted to an n-type conductivity to provide a majority carrier conduction channel from sources 22 and 23 to the central region 40 upon the application of an appropriate gate voltage. Clearly, however, all of these conductivity types could be reversed so that the device could work as a p-channel device rather than an n-channel device as disclosed.

One process by which the device of FIGS. 1 and 2 could be constructed is shown in FIGS. 3 to 6. Referring to FIG. 3, the base wafer 20 is shown as an n(+) material having an n(−) epitaxially deposited region on top thereof. A thick oxide layer 50 is formed on wafer 20 and windows 51 and 52 are opened therein. The open windows 51 and 52 are exposed to a beam of boron atoms in an ion implanting apparatus to form p(+) regions. Thereafter the implanted boron atoms are caused to diffuse deeper into the wafer to form the rounded p(+) concentration region shown in FIG. 3 which might have a depth of about 4 microns. During this diffusion operation, shallow oxide layers 53 and 54 grow over the windows 51 and 52.

As is next shown in FIG. 4, windows 61 and 62 are cut in the oxide layer 50 and an n(+) implant takes place to implant the n(+) regions 63 and 64 into the n(−) epitaxial layer. This n(+) implantation can be carried out with a phosphorus beam. Thereafter, the implanted regions are subjected to a diffusion step to cause the regions 63 and 64 to expand and deepen to a depth of about 3½ microns with a concentration determined by an implantation dose of 1×10^{12} to 1×10^{14} phosphorus atoms/cm^2 followed by a drive for 30 minutes to 4 hours at from 1150° C. to 1250° C. As will be later seen, regions 63 and 64 produce the novel n(+) region which substantially reduces the on-resistance of the device.

It should be noted that the n(+) regions 63 and 64 could, if desired, be epitaxially deposited and need not be diffused. Similarly, the resulting device being described herein could be manufactured by any desired process as would be apparent to those skilled in the art.

The next step in the process is shown in FIG. 5 and is the channel implantation and diffusion step in which the p(+) regions 71 and 72 are formed through the same windows 61 and 62 that were used for the n(+) implantation for regions 63 and 64. The p(+) regions 71 and 72 are formed by implanting with a boron beam to a dose of about 5×10^{13} to 5×10^{14} atoms/cm^2 followed by a diffusion drive for 30 to 120 minutes at 1150° C. to 1250° C.

Thereafter, and as shown in FIG. 6, steps are carried out for the source predeposition and the diffusion of the source regions 32 and 33. This is carried out by a conventional and non-critical phosphorus diffusion step where the diffusion proceeds through the windows 61 and 62 so that the source regions 32 and 33 are automatically aligned relative to the other preformed regions. Thus, the wafer is placed in a furnace and exposed to $POCl_3$ suspended in a carrier gas for from 10 minutes to 50 minutes at a temperature of from 850° C. to 1000°.

When this step is completed, the basic junction configuration required in FIG. 2 is formed with short p(+) regions disposed beneath the oxide 50 to serve as the conducting channel for the ultimately constructed device and with an n(+) region filling the area between the channels 34 and 35 between p(+) regions 30 and 31. The manufacturing process then continues from the step of FIG. 6 to the device shown in FIG. 2 wherein

the oxide surfaces on top of the chip are suitably stripped and the metalizing patterns for contacts 22, 23 and 24 are formed to establish electrical contacts to the device. The drain contact 26 is applied to the device in a subsequent metalizing operation. Thereafter, the entire device may be appropriately coated with a suitable passivation coating and wire leads are connected to the source electrodes 22 and 23 and the gate 24. The device is then mounted within a suitable protective housing, with the drain electrode fixed to the housing or other conductive support which serves as a drain connection.

The device shown in FIGS. 1 and 2 utilizes a serpentine path for each of the source regions and gate regions and a drain on the surface of the wafer opposite to the source electrodes. Other configurations can be used. FIGS. 7 and 8 illustrate a planar configuration which is a simple rectangular arrangement having a ring-shaped gate 80 which is disposed between a first source electrode 81 of ring shape and a central source 82. The device as shown in FIG. 8 is contained within a base wafer of p(−) monocrystalline silicon 83 which may have a buried n(+) region 84 to reduce the lateral resistance of the various current paths of the device leading to the laterally displaced drain electrode 85 which surrounds source 81.

A ring-shaped n(+) region 86 is formed within the device as shown in FIG. 8 and, in accordance with the present invention, the ring-shaped region 86 is of much higher conductivity than the n(−) epitaxially deposited region 87 which contains all the junctions of the device. The ring-shaped region 86 extends from the region beneath the gate oxide 88 and adjoins the ends of the two conducting channels formed between the ring-shaped p(+) region 89 and the central p(+) region 91 disposed beneath the ring-shaped source 81 and central source 82, respectively.

It will also be noted in FIG. 8 that the outer periphery 90 of the p(+) ring 89 has a large radius to assist the device in withstanding high reverse voltages.

An n(+) region 95 in FIG. 8 is provided to ensure good contact to drain electrode 85. Drain electrode 85 is widely laterally spaced from source 81 (by greater than about 90 microns). The drain contact 85 is surrounded by a p(+) isolation diffusion 96 to isolate the device from other devices on the same chip or wafer.

In the arrangement of FIG. 8, like that of FIG. 2, current flow from sources 81 and 82 goes through the width of epitaxial region 87, through the region 86. The current then flows laterally outward and then up to the drain contact 85. As in the embodiment of FIG. 2, device resistance is greatly reduced by the relatively highly conductive region 86.

In carrying out the above invention, it should be noted that any type of contact material can be used to make the source and gate contacts. By way of example, aluminum could be used for the source electrodes while a polysilicon material can be used for the conductive gate 80 in FIG. 8 or the conductive gate 24 in FIG. 2.

Numerous other geometries can be used to make the device of the invention, including a plurality of pairs of straight, parallel source elements with respectively interposed gates and the like.

The source electrodes 22 and 23 have been shown as separate electrodes which can be connected to separate leads. Clearly, the sources 22 and 23 could be directly connected as shown in FIG. 8*a* where components similar to those of FIG. 2 have been given similar identifying numerals. In FIG. 8*a*, however, the gate electrode

is a polysilicon layer 101 (in place of aluminum) deposited atop gate oxide 25. The gate 101 is then covered with oxide layer 102 and a conductive layer 103 connects the two sources 22 and 23 together to form a single source conductor which is insulated from gate 101. Connection is made to the gate at some suitable edge portion of the wafer.

FIGS. 9 and 10 show the shape of measured curves which demonstrate the reduction in forward resistance when the region 40 is made highly conductive (n+). In FIG. 9, the device tested had a region 40 which had the n(−) resistivity of the epitaxial region. Thus, the forward resistance is characteristically high at different gate biases as shown in FIG. 9.

In the device of the invention where region 40 is of n(+) conductivity, there is a dramatic decrease in the on-resistance as shown in FIG. 10 for all gate voltages before velocity saturation of the electrons occurs.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively and said common conduction region;

source electrode means connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion;

a drain electrode coupled to said drain conductive region and comprising a third terminal;

each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include relatively shallow depth regions extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region.

2. The high power metal oxide silicon field effect transistor device of claim 1 wherein said device is formed by D-MOS manufacturing techniques.

3. The device of claim 1 wherein said drain electrode is on said second semiconductor surface.

4. The device of claim 1 wherein said drain electrode is on said first surface.

5. The device of claim 4 wherein said drain conductive region contacts a second conductivity-type region which extends from said drain conductive region to said second surface.

6. The device of claim 1 wherein said gate insulation layer means is silicon dioxide.

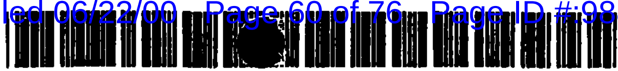
7. The device of claim 1 wherein said one conductivity type is the n-type and wherein said opposite conductivity type is the p-type.

8. The device of claim 1 wherein said relatively deep regions have a depth of about 4 microns.

9. The device of claim 1 wherein said gate electrode means is formed of polysilicon.

10. The device of claim 1 wherein said relatively lightly doped body portion has a resistivity greater than about 2.5 ohm centimeters.

* * * * *



US004642666B1

REEXAMINATION CERTIFICATE (3649th)

United States Patent [19]

[11] B1 4,642,666

Lidow et al.

[45] Certificate Issued *Oct. 27, 1998

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

[75] Inventors: Alexander Lidow, Manhattan; Thomas Herman, Redondo, both of Calif.

[73] Assignee: International Rectifier Corporation

Reexamination Requests:
No. 90/002.818, Aug. 24, 1992
No. 90/003.481, Jun. 29, 1994
No. 90/003.888, Jul. 20, 1995

Reexamination Certificate for:
Patent No.: 4,642,666
Issued: Feb. 10, 1987
Appl. No.: 471,818
Filed: Mar. 3, 1983

[*] Notice: The portion of the term of this patent subsequent to Mar. 8, 2000, has been disclaimed.

Related U.S. Application Data

[62] Division of Ser. No. 232,713, Feb. 9, 1981, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] Int. Cl.^{6} H01L 29/76

[52] U.S. Cl. 257/337; 257/339; 257/341; 257/342

[58] Field of Search 257/337, 339, 257/341, 342, 536

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,924,265 12/1975 Rodgers 357/23
4,072,975 2/1978 Ishitani 357/23
4,145,700 3/1979 Jambotkar 357/23
4,145,703 3/1979 Blanchard et al. 357/55
4,163,246 7/1979 Aomura et al. 257/776
4,190,850 2/1980 Tihanyi et al. 357/23
4,206,469 6/1980 Hanes et al. 257/341
4,219,835 8/1980 van Loon et al. 257/330
4,599,576 7/1986 Yoshida et al. 257/408
5,130,767 7/1992 Lidow et al. 257/339

FOREIGN PATENT DOCUMENTS

51-134076 11/1976 Japan .
52-104878 9/1977 Japan .
52-106688 9/1977 Japan .
54-4079 1/1979 Japan .

OTHER PUBLICATIONS

Tarui et al., "Diffusion Self-Aligned MOST: A New Approach for High Speed Device," J. of Japan Society of Applied Physics, vol. 39, 1970, pp. 105-110.

E. S. Oxner, *Power FETs and Their Applications*, Prentice-Hall, Ind., New Jersey (1982) pp. 59-67.

K. Lisiak et al., "Optimization of Nonplanar Power MOS Transistors" *Solid-State Electronics*, vol. 20 (1977) pp. 875-878.

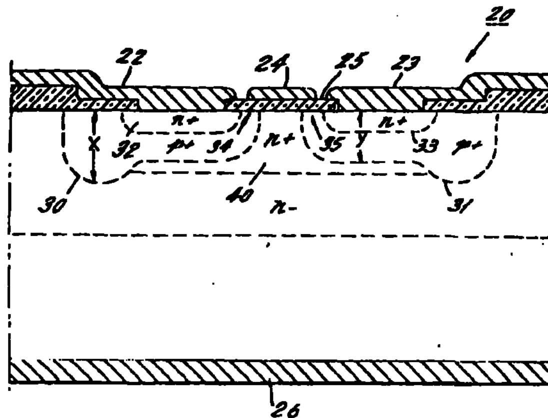
S. M. Sze, *Semiconductor Devices Physics and Technology*, John Wiley & Sons, New York, (1985) pp. 104-107.

(List continued on next page.)

Primary Examiner—J. Carroll

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.



OTHER PUBLICATIONS

B. J. Baliga et al., "Analytical Solutions for the Breakdown Voltage of Abrupt Cylindrical and Spherical Junctions", *Solid-State Electronics*, vol. 19 (1976) pp. 739–744.

E. S. Oxner. *Power FETs and Their Applications*, Prentice-Hall, Inc., New Jersey (1982) pp. 67–71.

Full English Translation of Japan Kokai 54-4079 as per USPTO.

REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claim **1** is determined to be patentable as amended.

Claims **2**, **3**, **6**, **7**, **8**, **9**, **4**, **5** and **10**, dependent on an amended claim, are determined to be patentable.

New claims **11** and **12** are added and determined to be patentable.

1. A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a *vertical* common conduction region of one conductivity type at a given first semiconductor surface location;

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions

being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively and said common conduction region; *the concentration of carriers of said one conductivity type in said common conduction region at said first semiconductor surface being less than the concentration of carriers of said opposite conductivity type of said first and second base regions at said first semiconductor surface;*

source electrode means connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion;

a drain electrode coupled to said drain conductive region and comprising a third terminal;

each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include, *to allow the device to withstand relatively high breakdown voltages,* relatively shallow depth regions *having a relatively small radius of curvature* extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region.

11. The device of claim 1 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

12. The device of claim 1 wherein said common conduction region is continuous and uninterrupted.

* * * * *

United States Patent [19]
Lidow et al.
[11] Patent Number: 4,705,759
[45] Date of Patent: Nov. 10, 1987

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

[75] Inventors: Alexander Lidow, Manhatta; Thomas Herman, Redondo, both of Calif.

[73] Assignee: International Rectifier Corporation, Los Angeles, Calif.

[21] Appl. No.: 456,813

[22] Filed: Jan. 10, 1983

Related U.S. Application Data

[60] Division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] Int. Cl.[4] H01L 21/265; H01L 21/31

[52] U.S. Cl. 437/29; 357/20; 357/23.4; 357/41; 357/52; 357/89; 437/30; 437/41; 437/149; 437/150; 437/153; 437/913; 437/931; 437/958; 437/984

[58] Field of Search .... 29/571, 576 B, 578; 148/1.5, 187, 190; 357/23 VD, 20, 41, 52, 89, 91

[56] References Cited

U.S. PATENT DOCUMENTS

3,909,320	9/1975	Cauge et al.	148/187
4,055,884	11/1977	Jambutkar	29/571
4,072,975	2/1978	Ishitani	357/23 VD
4,190,850	2/1980	Tihanyi et al.	357/23 VD
4,344,081	8/1982	Pao et al.	29/571 X

FOREIGN PATENT DOCUMENTS

2136509	11/1972	Fed. Rep. of Germany	357/23
48-40814	12/1973	Japan	357/23
50-46081	4/1975	Japan	357/23
51-85381	7/1976	Japan	357/23.4
52-23277	2/1977	Japan	357/23
53-74385	7/1978	Japan	357/23

OTHER PUBLICATIONS

Lin et al., "Optimum Load Device for DMOS Integrated Circuits", IEEE J. Solid-State Circuits, vol. SC-11, No. 4, Aug. 1976, pp. 443-452.

Plummer et al., "Monolithic 200-V CMOS Analog Switch, IEEE J. Solid-State Circuits, vol. SC-11, No. 6, Dec. 1976, pp. 809-817.

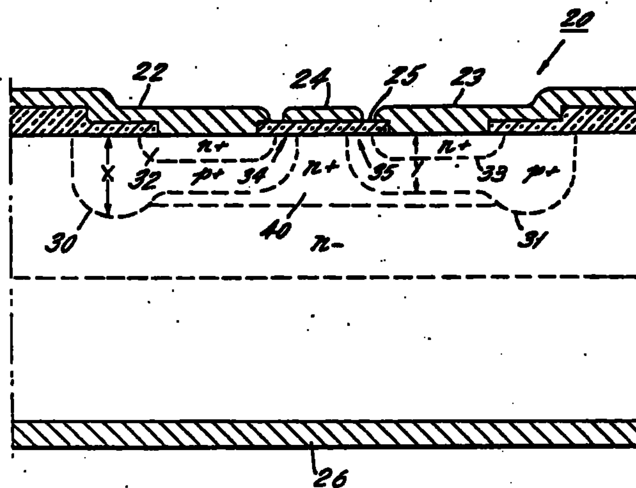
Sun et al., "Modeling of—LDMOS, VDMOS and VMOS—Transistors", IEEE Trans. Electron Dev., vol. 60-27, No. 2, Feb. 1980, pp. 356-367.

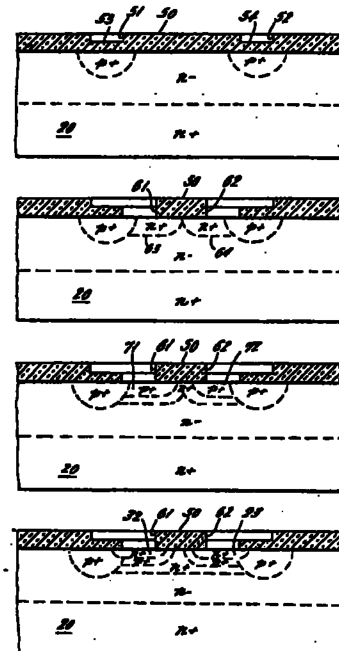
Primary Examiner—William G. Saba
Attorney, Agent, or Firm—Ostrolink, Faber, Gerb & Soffen

[57] ABSTRACT

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

7 Claims, 11 Drawing Figures





Case 2:00-cv-06756-R-CT Document 1 Filed 06/22/00 Page 64 of 76 Page ID #:992

FIG. 1

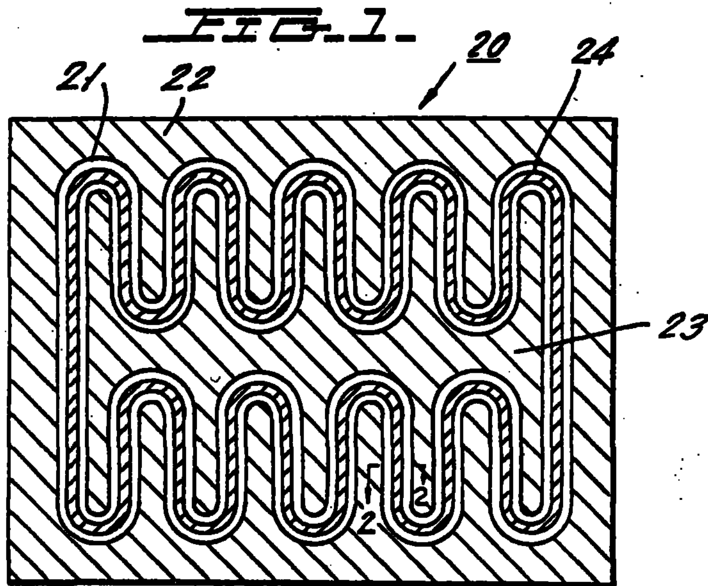
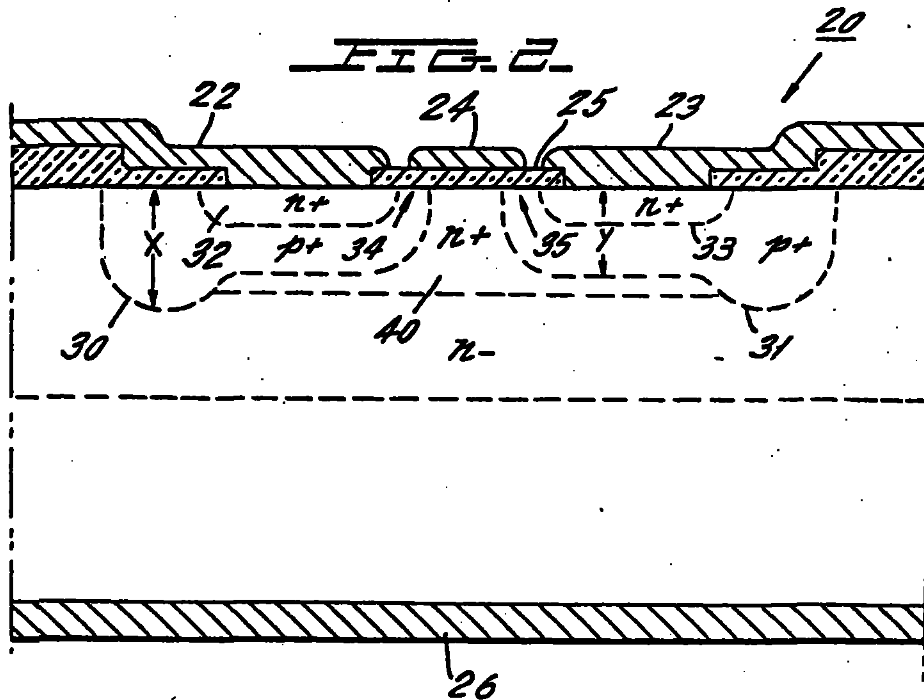


FIG. 2



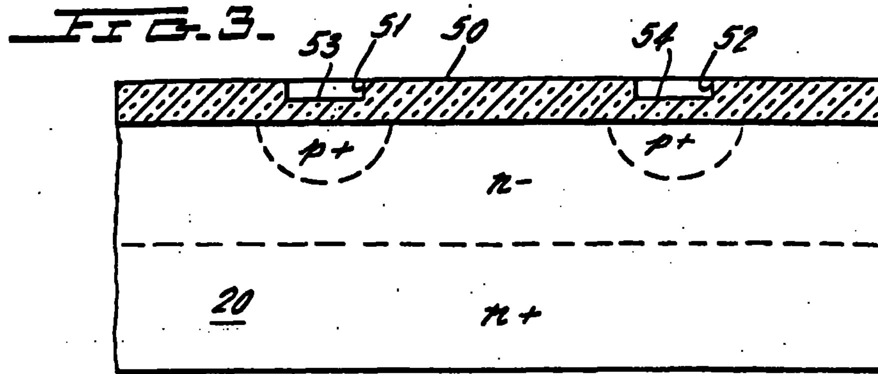


FIG-3-
53
51
50
54
52
p+
p+
n-
20
n+

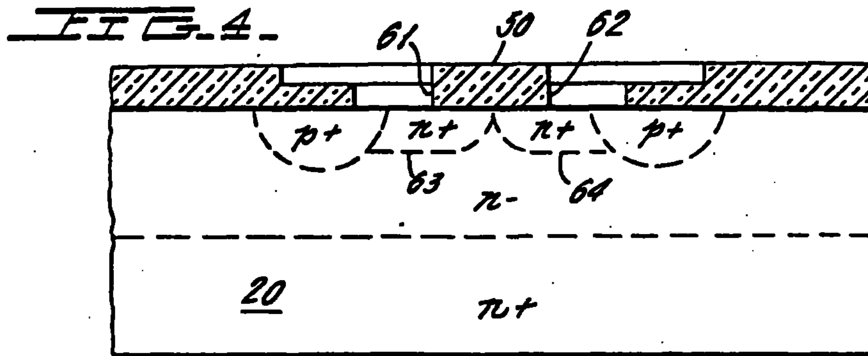


FIG-4-
61
50
62
p+
n+
n+
p+
63
n-
64
20
n+

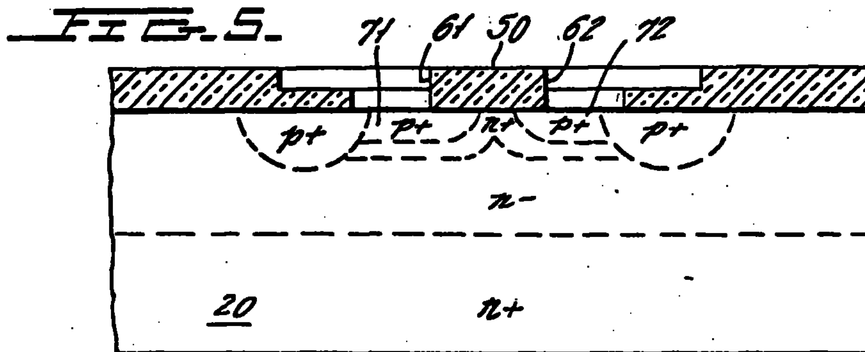


FIG-5-
71
61
50
62
72
p+
p+
n+
p+
p+
n-
20
n+

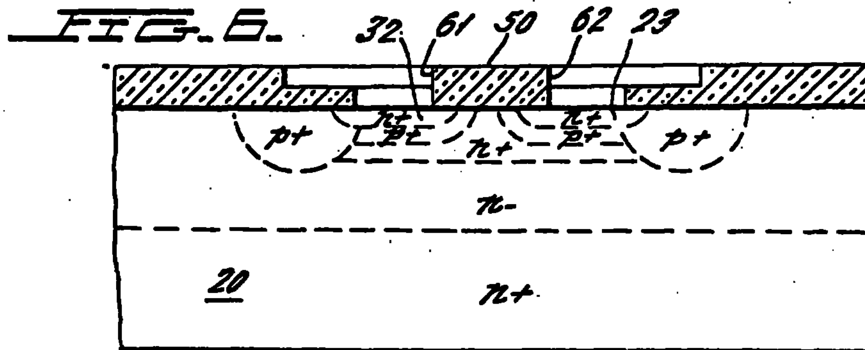
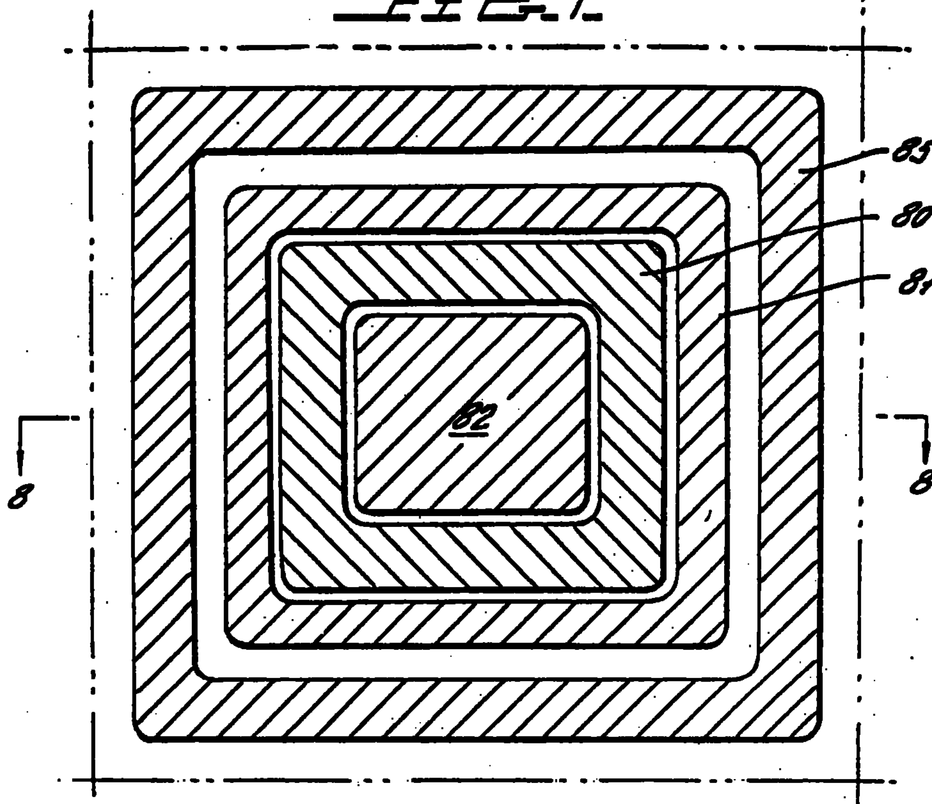


FIG-6-
32
61
50
62
23
p+
n+
p+
n+
n+
p+
p+
n-
20
n+

FIG. 7



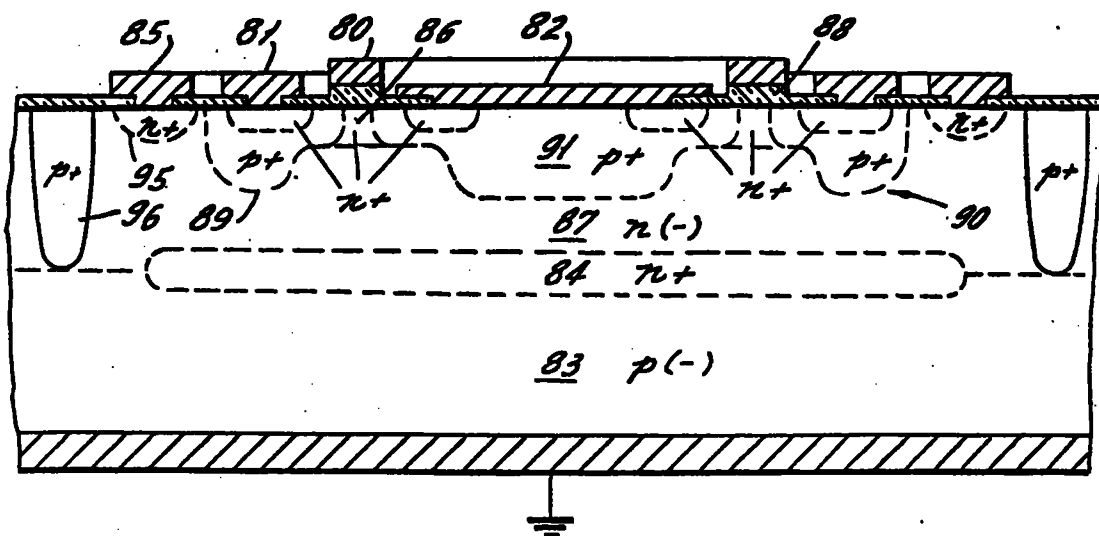


FIG. 8

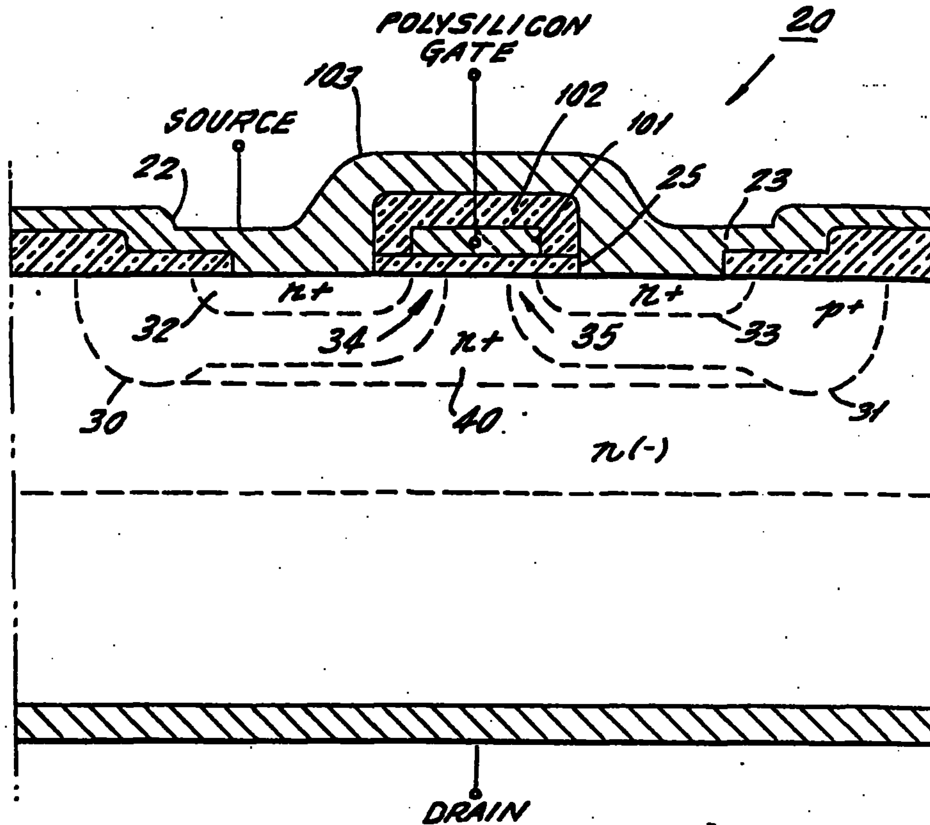


FIG. 8a

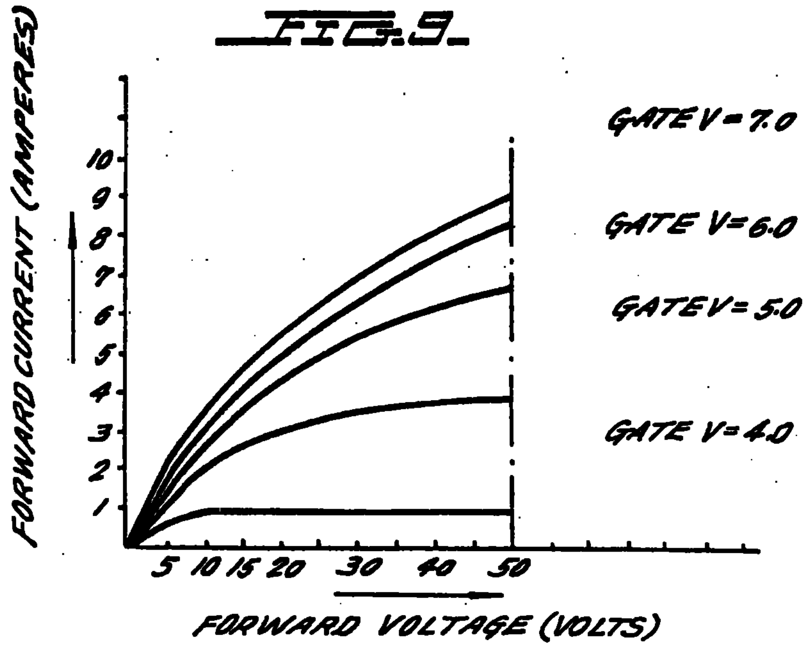


FIG. 9
GATE V=7.0
GATE V=6.0
GATE V=5.0
GATE V=4.0
FORWARD CURRENT (AMPERES)
10
9
8
7
6
5
4
3
2
1
5 10 15 20 30 40 50
FORWARD VOLTAGE (VOLTS)

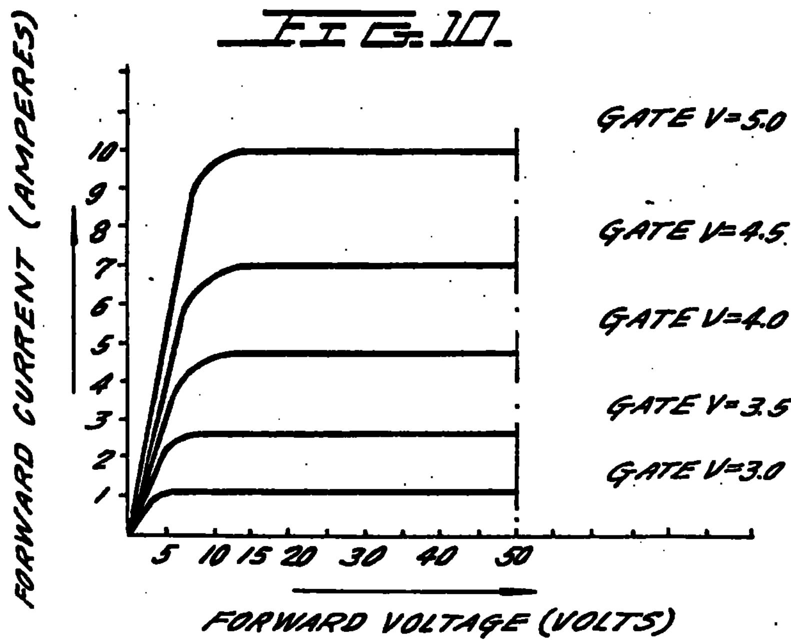


FIG. 10
GATE V=5.0
GATE V=4.5
GATE V=4.0
GATE V=3.5
GATE V=3.0
FORWARD CURRENT (AMPERES)
10
9
8
7
6
5
4
3
2
1
5 10 15 20 30 40 50
FORWARD VOLTAGE (VOLTS)

HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

This application is a division of application Ser. No. 232,713, filed Feb. 9, 1981, now U.S. Pat. No. 4,376,286, issued Mar. 8, 1983, which, in turn, is a continuation of application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices and more specifically relates to a novel structure for a MOSFET device which permits it to be used in high power applications with a relatively high reverse voltage and with an exceptionally low on-resistance. The major advantage of the bipolar transistor over the MOSFET transistor is that the bipolar transistor has a very low on-resistance per unit conductive area. The MOSFET transistor has numerous advantages over the bipolar transistor including very high switching speed, very high gain and lack of the secondary breakdown characteristics exhibited by a minority carrier device. However, because the MOSFET transistor has high on-resistance, its use in high power switching applications has been limited.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device which has a low forward resistance so that the device becomes more competitive with bipolar devices in a switching type application while retaining all of the numerous advantages of the MOSFET over the bipolar device. In particular, with the present invention, the forward resistance per unit area of the device has been reduced by at least a factor of two, compared to the limiting resistance per unit area previously existing in a MOSFET type device.

In one embodiment of the invention, two sources are placed on the same surface of a semiconductor wafer and are laterally spaced from one another. A gate electrode, deposited on a conventional gate oxide, is disposed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced from one another by an n-type bulk region. Current from each source can flow through its respective channel (after the creation of the inversion layer defining the channel), so that majority carrier conduction current can flow through the bulk region and across the wafer or chip to the drain electrode. The drain electrode may be on the opposite surface of the wafer or on a laterally displaced surface region from the source electrodes. This configuration is made using the desirable manufacturing techniques of the D-MOS device, which permits precise alignment of the various electrodes and channels and permits use of extremely small channel lengths. While the above configuration may have been previously described for a MOSFET signal-type device, the structure is not that of the commonly used signal MOSFET.

The device is basically formed in an n(−) substrate which has the relatively high resistivity which is necessary to obtain the desired reverse voltage capability of the device. For example, for a 400 volt device, the n(−) region will have a resistivity of about 20 ohm centimeters. However, this same necessary high resistivity characteristic has caused the on-resistance of the MOSFET device, when used as a power switch, to be relatively high.

In accordance with the present invention, it has been found that in the upper portion of the central bulk region to which the two inversion layers feed current in the path to the drain electrode, the central region immediately beneath the gate oxide can be a relatively low resistivity material formed, for example, by an n(+) diffusion in that channel region, without affecting the reverse voltage characteristics of the device.

More specifically, and in accordance with the invention, this common channel will have an upper portion beneath the gate oxide and a lower bulk portion extending toward the drain electrode. The lower portion has the high resistivity desired to produce high reverse voltage ability, and will have a depth dependent on the desired reverse voltage for the device. Thus, for a 100 volt device, the lower n(−) region may have a depth of about 35 microns, while for a 90 volt device it will have a depth of about 8 microns. Other depths will be selected, depending on the desired reverse voltage of the device to provide the necessary thicker depletion region required to prevent punch-through during reverse voltage conditions. The upper portion of the common channel is made highly conductive (n+) to a depth of from about 3 to about 6 microns. It has been found that this does not interfere with the reverse voltage withstand ability of the device. However, it decreases the on-resistance per unit area of the device by more than a factor of two. The resulting device becomes competitive with conventional high power bipolar switching devices since it retains all of the advantages of the MOSFET device over the bipolar device but now has the relatively low forward resistance which was the major characterizing advantage of the bipolar device.

In accordance with another feature of the present invention, the p-type region which defines the channel beneath the gate oxide has a relatively deeply diffused portion beneath the source so that the p-type diffusion region will have a large radius of curvature in the n(−) opitaxial layer forming the body of the device. This deeper diffusion or deeper junction has been found to improve the voltage gradient at the edge of the device and thus permits the use of the device with higher reverse voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a high power MOSFET chip which incorporates the present invention and particularly illustrates the metalizing patterns of the two sources and the gate.

FIG. 2 is a cross-sectional view of FIG. 1 taken across the section line 2—2 in FIG. 1.

FIG. 3 is a cross-sectional view similar to FIG. 2 showing the initial step in the process of manufacture of the chip of FIGS. 1 and 2 and particularly shows the p(+) conductivity implant and diffusion step.

FIG. 4 shows the second step in the manufacturing process and shows the n(+) implant and diffusion step.

FIG. 5 shows a further step in the process of manufacture of the chip of FIGS. 1 and 2 and shows the channel implant and diffusion step.

FIG. 6 shows a further step in the process of manufacture and illustrates the source predeposition and diffusion step. This precedes the last step in which the gate oxide is cut for the metalization step which produces the device of FIG. 2.

FIG. 7 is a plan view of the metalizing pattern of a second embodiment of the invention.

FIG. 8 is a cross-sectional view of FIG. 7 taken across the section line 8—8 in FIG. 7.

FIG. 8*a* is a view similar to FIG. 2 and shows a modified source contact configuration.

FIG. 9 shows the shape of forward-current characteristics of a device like that of FIG. 2 where the region 40 beneath the oxide is n(−).

FIG. 10 shows the shape of the characteristic of a device identical to that of FIG. 2 where the region 40 has high n(+) conductivity.

DETAILED DESCRIPTION OF THE DRAWINGS

A first embodiment of the novel MOSFET device of the present invention is shown in FIGS. 1 and 2 which show a chip of monocrystalline silicon 20 (or some other suitable material), with the device electrodes following the serpentine path 21 best shown in FIG. 1 in order to increase the current-carrying area of the device. Other geometries could be used. The device illustrated has a reverse voltage of about 400 volts and an on-resistance less than about 0.4 ohm with a channel width of 50 centimeters. Devices having reverse voltages of from 90 to 400 volts have been made. The 400 volt devices have carried pulse currents of 30 amperes. The 90 volt devices have had forward on-resistances of about 0.1 ohm with a channel width of 50 centimeters and have carried pulse currents up to about 100 amperes. Higher and lower voltage devices can also be made with varying channel widths.

Presently known MOSFET devices have much higher on-resistances than the above. For example, a 400 volt MOSFET comparable to that described below but made with prior art techniques would normally have an on-resistance much greater than about 1.5 ohms, as compared to an on-resistance less than about 0.4 ohm in a device made according to this invention.

Moreover, the MOSFET switching device of the present invention will exhibit all of the desirable advantages of the MOSFET device, since it operates as a majority carrier device. These advantages include high switching speed, high gain and avoidance of the secondary breakdown characteristics which exist in minority carrier devices.

The device of FIGS. 1 and 2 has two source electrodes 22 and 23 which are separated by a metalized gate electrode 24 which is fixed to but spaced from the semiconductor device surface by a silicon dioxide layer 25. The serpentine path followed by gate oxide 25 has a length of 50 centimeters and has 667 undulations, but is shown more simply in FIG. 1. Other channel widths can be used. Source electrodes 22 and 23 can be laterally extended as shown to serve as field plates to help spread the depletion region created during reverse voltage conditions. Each of source electrodes 22 and 23 supply current to a common drain electrode 26 which is fixed to the bottom of the wafer. The relative dimensions for the device, particularly in thickness, have been grossly exaggerated in FIG. 2 for purposes of clarity. The silicon chip or wafer 20 is formed on an n(+) substrate which may have a thickness of about 14 mils. An n(−) epitaxial layer is deposited on substrate 20 and will have a thickness and resistivity depending on the desired reverse voltage. All junctions are formed in this epitaxial layer which can have a relatively high resistivity. In the embodiment disclosed, the epitaxial layer has

a thickness of about 35 microns and a resistivity of about 20 ohm-centimeters. For a 90 volt device, epitaxial layer 20 would be about 10 microns thick and would have a resistivity of about 2.5 ohm-centimeters. A channel width of 50 centimeters is also used to provide the desired current carrying capacity for the device.

In a preferred embodiment of the invention, there is an elongated serpentine p(+) conductivity region beneath each of the source electrodes 22 and 23 which thus extends around the serpentine path shown in FIG. 1. These p(+) regions are shown in FIG. 2 as the p(+) regions 30 and 31, respectively, and are similar to those of the prior art except that the maximum p(+) region depth is greatly exaggerated in order to form a large radius of curvature. This allows the device to withstand higher reverse voltages. By way of example, the depth of regions 30 and 31 is preferably about 4 microns at the dimension X in FIG. 2 and about 3 microns at the dimension Y in FIG. 2.

By using D-MOS fabrication techniques, two n(+) regions 32 and 33 are formed beneath source electrodes 22 and 23, respectively, and define, with the p(+) regions 30 and 31, n-type channel regions 34 and 35, respectively. Channel regions 34 and 35 are disposed beneath the gate oxide 25 and can be inverted by the appropriate application of a biasing signal to the gate 24 in order to permit conduction from the source 22 and the source 23 through the inversion layers into the central region disposed beneath the gate 24 and then to the drain electrode 26. Channels 34 and 35 may each have a length of about 1 micron.

It has previously been thought necessary that the central n(−) region between channels 34 and 35 (and between p(+) regions 30 and 31) should have a high resistivity in order to permit the device to withstand high reverse voltages. However, the relatively high resistivity n(−) material is also a significant contributing factor to the high forward on-resistance of the device.

In accordance with the significant feature of the present invention, a significant portion of this central conducting region is made relatively highly conductive and consists of an n(+) region 40 disposed immediately beneath the gate oxide 25. The n(+) region 40 has a depth of about 4 microns and could range from about 3 microns to about 6 microns. While its exact conductivity is not known, and varies with depth, it is high relative to the n(−) region beneath it. More particularly, region 40 has a high conductivity which would be determined by a total ion implanted dose of from about 1×10^{12} to 1×10^{14} phosphorus atoms/cm^2 at 50 KV followed by a diffusion drive at from 1150° C. to 1250° C. for from 30 minutes to 240 minutes. It has been found that by making this region 40 relatively highly conductive n(+) material through a diffusion or other operation, the device characteristics are significantly improved and the forward on-resistance of the device is reduced by a factor greater than two. Moreover, it has been found that the provision of the high conductivity region 40 does not interfere with the reverse voltage characteristics of the device. Accordingly, by making the region beneath the gate oxide 25 and between channels 34 and 35 more highly conductive, the forward on-resistance of the ultimate high power switching device has been significantly reduced and the MOSFET device becomes far more competitive with an equivalent junction-type device while still retaining all of the advantages of the MOSFET majority carrier operation.

In the above description of FIGS. 1 and 2, it has been assumed that the conduction channels 34 and 35 are of p(+) material and are, accordingly, inverted to an n-type conductivity to provide a majority carrier conduction channel from sources 22 and 23 to the central region 40 upon the application of an appropriate gate voltage. Clearly, however, all of these conductivity types could be reversed so that the device could work as a p-channel device rather than an n-channel device as disclosed.

One process by which the device of FIGS. 1 and 2 could be constructed is shown in FIGS. 3 to 6. Referring to FIG. 3, the base wafer 20 is shown as an n(+) material having an n(−) epitaxially deposited region on top thereof. A thick oxide layer 50 is formed on wafer 20 and windows 51 and 52 are opened therein. The open windows 51 and 52 are exposed to a beam of boron atoms in an ion implanting apparatus to form p(+) regions. Thereafter the implanted boron atoms are caused to diffuse deeper into the wafer to form the rounded p(+) concentration region shown in FIG. 3 which might have a depth of about 4 microns. During this diffusion operation, shallow oxide layers 53 and 54 grow over the windows 51 and 52.

As is next shown in FIG. 4, windows 61 and 62 are cut in the oxide layer 50 and an n(+) implant takes place to implant the n(+) regions 63 and 64 into the n(−) epitaxial layer. This n(+) implantation can be carried out with a phosphorus beam. Thereafter, the implanted regions are subjected to a diffusion step to cause the regions 63 and 64 to expand and deepen to a depth of about 3½ microns with a concentration determined by an implantation dose of 1×10^{12} to 1×10^{14} phosphorus atoms/cm^2 followed by a drive for 30 minutes to 4 hours at from 1150° C. to 1250° C. As will be later seen, regions 63 and 64 produce the novel n(+) region which substantially reduces the on-resistance of the device.

It should be noted that the n(+) regions 63 and 64 could, if desired, be epitaxially deposited and need not be diffused. Similarly, the resulting device being described herein could be manufactured by any desired process as would be apparent to those skilled in the art.

The next step in the process is shown in FIG. 5 and is the channel implantation and diffusion step in which the p(+) regions 71 and 72 are formed through the same windows 61 and 62 that were used for the n(+) implantation for regions 63 and 64. The p(+) regions 71 and 72 are formed by implanting with a boron beam to a dose of about 5×10^{13} to 5×10^{14} atoms/cm^2 followed by a diffusion drive for 30 to 120 minutes at 1150° C. to 1250° C.

Thereafter, and as shown in FIG. 6, steps are carried out for the source predeposition and the diffusion of the source regions 32 and 33. This is carried out by a conventional and non-critical phosphorus diffusion step where the diffusion proceeds through the windows 61 and 62 so that the source regions 32 and 33 are automatically aligned relative to the other preformed regions. Thus, the wafer is placed in a furnace and exposed to $pocl_3$ suspended in a carrier gas for from 10 minutes to 50 minutes at a temperature of from 850° C. to 1000° C.

When this step is completed, the basic junction configuration required in FIG. 2 is formed with short p(+) regions disposed beneath the oxide 50 to serve as the conducting channel for the ultimately constructed device and with an n(+) region filling the area between the channels 34 and 35 and between p(+) regions 30 and 31. The manufacturing process then continues from the step of FIG. 6 to the device shown in FIG. 2 wherein the oxide surfaces on top of the chip are suitably stripped and the metalizing patterns for contacts 22, 23 and 24 are formed to establish electrical contacts to the device. The drain contact 26 is applied to the device in a subsequent metalizing operation. Thereafter, the entire device may be appropriately coated with a suitable passivation coating and wire leads are connected to the source electrodes 22 and 23 and the gate 24. The device is then mounted within a suitable protective housing, with the drain electrode fixed to the housing or other conductive support which serves as a drain connection.

The device shown in FIGS. 1 and 2 utilizes a serpentine path for each of the source regions and gate regions and a drain on the surface of the wafer opposite to the source electrodes. Other configurations can be used. FIGS. 7 and 8 illustrate a planar configuration which is a simple rectangular arrangement having a ring-shaped gate 80 which is disposed between a first source electrode 81 of ring shape and a central source 82. The device as shown in FIG. 8 is contained within a base wafer of p(−) monocrystalline silicon 83 which may have a buried n(+) region 84 to reduce the lateral resistance of the various current paths of the device leading to the laterally displaced drain electrode 85 which surrounds source 81.

A ring-shaped n(+) region 86 is formed within the device as shown in FIG. 8 and, in accordance with the present invention, the ring-shaped region 86 is of much higher conductivity than the n(−) epitaxially deposited region 87 which contains all the junctions of the device. The ring-shaped region 86 extends from the region beneath the gate oxide 88 and adjoins the ends of the two conducting channels formed between the ring-shaped p(+) region 89 and the central p(+) region 91 disposed beneath the ring-shaped source 81 and central source 82, respectively.

It will also be noted in FIG. 8 that the outer periphery 90 of the p(+) ring 89 has a large radius to assist the device in withstanding high reverse voltages.

An n(+) region 95 in FIG. 8 is provided to ensure good contact to drain electrode 85. Drain electrode 85 is widely laterally spaced from source 81 (by greater than about 90 microns). The drain contact 85 is surrounded by a p(+) isolation diffusion 96 to isolate the device from other devices on the same chip or wafer.

In the arrangement of FIG. 8, like that of FIG. 2, current flow from sources 81 and 82 goes through the width of epitaxial region 87, through the region 86. The current then flows laterally outward and then up to the drain contact 85. As in the embodiment of FIG. 2, device resistance is greatly reduced by the relatively highly conductive region 86.

In carrying out the above invention, it should be noted that any type of contact material can be used to make the source and gate contacts. By way of example, aluminum could be used for the source electrodes while a polysilicon material can be used for the conductive gate 80 in FIG. 8 or the conductive gate 24 in FIG. 2.

Numerous other geometries can be used to make the device of the invention, including a plurality of pairs of straight, parallel source elements with respectively interposed gates and the like.

The source electrodes 22 and 23 have been shown as separate electrodes which can be connected to separate leads. Clearly, the sources 22 and 23 could be directly

connected as shown in FIG. 8a where components similar to those of FIG. 2 have been given similar identifying numerals. In FIG. 8a, however, the gate electrode is a polysilicon layer 101 (in place of aluminum) deposited atop gate oxide 25. The gate 101 is then covered with oxide layer 102 and a conductive layer 103 connects the two sources 22 and 23 together to form a single source conductor which is insulated from gate 101. Connection is made to the gate at some suitable edge portion of the wafer.

FIGS. 9 and 10 show the shape of measured curves which demonstrate the reduction in forward resistance when the region 40 is made highly conductive (n+). In FIG. 9, the device tested had a region 40 which had the n(−) resistivity of the epitaxial region. Thus, the forward resistance is characteristically high at different gate biases as shown in FIG. 9.

In the device of the invention where region 40 is of n(+) conductivity, there is a dramatic decrease in the on-resistance as shown in FIG. 10 for all gate voltages before velocity saturation of the electrons occurs.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. The method of manufacture of a high power MOSFET device which comprises the steps of:

(a) forming an insulation coating on the upper surface of a flat chip of a monocrystalline semiconductor of one of the conductivity types;

(b) opening at least first and second spaced windows in said insulation coating which have at least first respective portions thereof which are elongated and parallel to one another;

(c) applying impurity carriers of a conductivity type opposite said one conductivity type to said upper surface which is exposed by said first and second windows and heating said chip to cause said carriers to diffuse into said chip to form first and second respective regions of said opposite conductivity type in said chip which have a first depth;

(d) opening at least third and fourth spaced windows in any insulation coating on said upper surface which are coextensive with and adjacent to said first and second windows; said third and fourth windows being disposed inwardly of the space between said first and second windows and being laterally removed from atop said first and second regions respectively;

(e) applying impurity carriers of said opposite conductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers to diffuse into said chip to form third and fourth respective regions of said opposite conductivity type which are continuous with the adjacent sides of said first and second regions respectively but are shallower than said first and second regions; the opposite edges of parallel portions of said third and fourth regions being laterally diffused until they are spaced from one another by a given distance by a common neck region of said one conductivity type of said chip;

(f) applying impurity carriers of said one conductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers from said one conductivity type to diffuse into said third and fourth regions for only a portion of the depth and width of said third and fourth regions to define first and second source regions; said first and second source regions having facing edges which are spaced from said common neck region, thereby to define first and second channel regions in said third and fourth regions respectively;

(g) and forming an insulated gate means atop said upper surface and over said first and second channel regions, and forming source electrode means on said source regions and drain electrode means on the surface of said chip which is opposite said upper surface.

2. The method of claim 1 wherein said impurity carriers of said opposite conductivity type which are applied through said first and second windows, and said impurity carriers of said opposite conductivity type which are applied through said third and fourth windows, are each applied by ion implantation.

3. The method of claim 1 wherein said chip has an epitaxial layer thereon which extends to said upper surface and wherein all of said regions are contained within said epitaxial layer.

4. The method of manufacture of a high power MOSFET device which comprises the steps of:

(a) forming an insulation coating on the upper surface of a flat chip of a monocrystalline semiconductor of one of the conductivity types;

(b) opening at least first and second spaced windows in said insulation coating which have at least first respective portions thereof which are elongated and parallel to one another;

(c) applying impurity carriers of a conductivity type opposite said one conductivity type to said upper surface which is exposed by said first and second windows and heating said chip to cause said carriers to diffuse into said chip to form first and second respective regions of said opposite conductivity type in said chip which have a first depth;

(d) opening at least third and fourth spaced windows in said insulation coating on said upper surface which are coextensive with and adjacent to said first and second windows respectively; said third and fourth windows being disposed inwardly of the space between said first and second windows and being laterally removed from atop said first and second regions respectively;

(e) applying impurity carriers of said one conductivity type to said upper surface through said third and fourth windows and heating said chip to cause said impurity carriers of said one conductivity type to diffuse into said chip to form relatively highly doped regions of said one conductivity type which spread laterally until they join one another in a common neck region beneath said insulation coating which is between said third and fourth windows;

(f) applying impurity carriers of said opposite conductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers to diffuse into said chip to form third and fourth respective regions of said opposite conductivity type which are continuous with the adjacent sides of said first and second regions respectively but are shallower than said first and second regions; the opposite edges of

parallel portions of said third and fourth regions being laterally diffused until they are spaced from one another by a given distance by said common neck region of said one conductivity type of said chip;

(g) applying impurity carriers of said one conductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers from said one conductivity type to diffuse into said third and fourth regions for only a portion of the depth and width of said third and fourth regions to define first and second source regions; said first and second source regions having facing edges which are spaced from said common neck region, thereby to define first and second channel regions in said third and fourth regions respectively;

(h) and forming an insulated gate means atop said upper surface and over said first and second channel regions, and forming source electrode means on said source regions and drain electrode means on the surface of said chip which is opposite said upper surface.

5. The method of claim 4 wherein said impurity carriers of said opposite conductivity type which are applied through said first and second windows, and said impurity carriers of said opposite conductivity type which are applied through said first and second windows, and said impurity carriers of said opposite conductivity type which are applied through said third and fourth windows, are each applied to said upper surface by ion implanation.

6. The method of claim 4 wherein said chip has an epitaxial layer thereon which extends to said upper surface and wherein all of said regions are contained within said epitaxial layer.

7. The method of claim 1, 2 or 3 wherein, following the step of forming said first and second regions of said opposite conductivity type, impurity carriers of said one conductivity type are applied to at least selected regions of said upper surface to cause impurities of said one conductivity type to diffuse into said chip to form relatively lightly doped regions of said one conductivity type which are disposed laterally within said common neck region and which extend to said upper surface of said chip.

* * * * *

5 10 15 20 25 30 35 40 45 50 55 60 65

US004705759B1

REEXAMINATION CERTIFICATE (2474th)

United States Patent [19] [11] **B1 4,705,759**

Lidow et al. [45] **Certificate Issued Feb. 14, 1995**

[54] **HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE**

[75] Inventors: **Alexander Lidow**, Manhatta; **Thomas Herman**, Redondo, both of Calif.

[73] Assignee: **International Rectifier Corporation**, Los Angeles, Calif.

Reexamination Request:
No. 90/003,141, Jul. 26, 1993

Reexamination Certificate for:

Patent No.:	**4,705,759**
Issued:	**Nov. 10, 1987**
Appl. No.:	**456,813**
Filed:	**Jan. 10, 1983**

Related U.S. Application Data

[60] Division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.

[51] **Int. Cl.**[6] **H01L 21/265; H01L 21/31**
[52] **U.S. Cl.** **437/29**; 257/337; 257/339; 257/341; 257/342; 257/343; 437/30; 437/41; 437/149; 437/150; 437/153; 437/913; 437/931; 437/958; 437/984
[58] **Field of Search** 437/29, 30, 41, 149, 437/150, 153, 913, 931, 958, 984; 257/337, 339, 341, 342, 343

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,055,884	11/1977	Jambotkar	29/571
4,072,975	2/1978	Ishitani	357/23
4,190,850	2/1980	Tihanyi et al.	357/23

FOREIGN PATENT DOCUMENTS

2136509	11/1972	Germany .
50-46081	4/1975	Japan .
52-106688	9/1977	Japan .

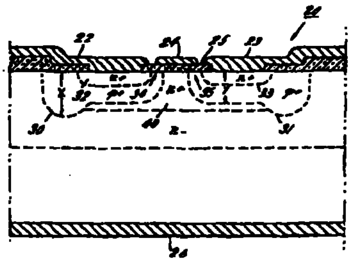
OTHER PUBLICATIONS

Plummer et al., "Monolithic 200-V CMOS Analog Switch," *IEEE J. Solid-State Circuits*, vol. SC-11, No. 6, Dec. 1976.
Tarui et al., "Diffusion Self-Aligned MOST: A New Approach for High Speed Device," *J. of Japan Society of Applied Physics*, vol. 39, 1970.
Pocha, "High Voltage Double Diffused MOS Transistors for Integrated Circuits," *Stanford Electronics Laboratories Technical Report* No. 4956-1, Stanford University, Mar. 1976.

Primary Examiner—William G. Saba

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.



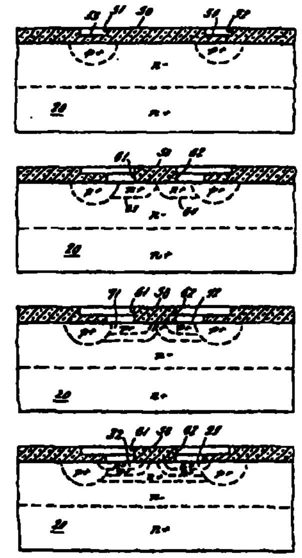


Exhibit E – Page 73

REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims 4–6 is confirmed.

Claim 1 is determined to be patentable as amended.

Claims 2, 3 and 7, dependent on an amended claim, are determined to be patentable.

1. The method of manufacture of a high power MOS-FET device which comprises the steps of:

(a) forming an insulation coating on the upper surface of a flat chip of a monocrystalline semiconductor of one [of the] conductivity [types] *type;*

(b) opening at least first and second spaced windows in said insulation coating which have at least first respective portions thereof which are elongated and parallel to one another;

(c) applying impurity carriers of a conductivity type opposite said one conductivity type to said upper surface which is exposed by said first and second windows and heating said chip to cause said carriers to diffuse into said chip to form first and second respective regions of said opposite conductivity type in said chip which have a first depth *and a relatively large radius of curvature to allow the device to withstand higher reverse voltages;*

(d) opening at least third and fourth spaced windows in any insulation coating on said upper surface which are coextensive with and adjacent to said first and second windows; said third and fourth windows being disposed inwardly of the space between said first and second windows and being laterally removed from atop said first and second regions respectively;

(e) applying impurity carriers of said opposite conductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers to diffuse into said chip to form third and fourth respective regions of said opposite conductivity type which are continuous with the adjacent sides of said first and second regions respectively but are shallower *and have a smaller radius of curvature* than said first and second regions; the opposite edges of parallel portions of said third and fourth regions being laterally diffused until they are spaced from one another by a given distance by a common neck region of said one conductivity type of said chip;

(f) applying impurity carriers of said one conductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers from said one conductivity type to diffuse into said third and fourth regions for only a portion of the depth and width of said third and fourth regions to define first and second source regions; said first and second source regions having facing edges which are spaced from said common neck region, thereby to define first and second channel regions in said third and fourth regions respectively; *and*

(g) [and] forming an insulated gate means atop said upper surface and over said first and second channel regions, and forming source electrode means on said source regions and drain electrode means on the surface of the chip which is opposite said upper surface.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,959,699

DATED : September 25, 1990

INVENTOR(S) : Alexander Lidow et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 37, please change "19" to -- 20 --.

Signed and Sealed this

Twenty-fifth Day of May, 1993

Attest:

MICHAEL K. KIRK

Attesting Officer *Acting Commissioner of Patents and Trademarks*