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3:47:59 m Lfl ~^4^BIN Receipt # 061902 NO REFUND WITHOUT RECEIPT====== 06/22/00 CRSE « OO—evss OB6900 510000 Filing Fee Civil _ $\frac{1}{2}$ **E** $\frac{1}{2}$ **C** $\frac{1}{2}$ **o** $\frac{1}{2}$ **o** $\frac{1}{2}$ **o** $\frac{1}{2}$ **o** $\frac{1}{2}$ **Special Fund F/F_ ^ 150.00**
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JURISDICTION AND VENUE

1. The claims alleged below are brought under the Patent Laws of the United States, 35 U.S.C. §§ 1 et seq. This Court has jurisdiction over these claims pursuant to 28 U.S.C. §§ 1338(a). Venue is based on 28 U.S.C. §§ 1391(b), 1391(c), 1391(d) and 1400(b).

PARTIES

9 10 2. IR is a corporation duly organized and existing under the laws of the State of Delaware, with its corporate headquarters and principal place of business within the Central District of Califomia at 233 Kansas Street, El Segundo, Califomia 90245.

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13 14 15 16 3. IR is informed and believes, and on that basis alleges, that defendant IXYS Corporation ("IXYS") is a corporation organized under the laws of the State of Delaware, doing business in this District, inter alia, through its Sales Representative, Select Electronics, in Santa Ana, Califomia.

18 19 20 21 22 23 24 25 26 27 28 4. The true names and/or culpabilities of defendant DOES 1-10 are unknown to IR at this time. IR is informed and believes, and on that basis alleges, that DOES 1-10, as more fully alleged below, as well as the other defendants, are legally responsible for the occurrences, acts and wrongs alleged herein and for the damages to IR proximately caused thereby. In particular, IR is informed and believes, and on that basis alleges, that IXYS relies on sales representatives and distributors, including DOES 1-10, to sell devices in this District and elsewhere within the United States, where such devices practice one or more of the claims (or are made by one or more of the claimed processes) of the patents identified below. Such sales are direct infringements of the patents in suit. IR will amend this Complaint to correctly identify any DOE defendant whose identity and culpability is made known to IR.

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FIRST CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 4,959,699)

5. IR is and has been the owner by mesne assignment of United States Letters Patent No. 4,959,699 (the "'699 patent"), which issued September 25, 1990 (Reexamination Certificates issued October 12, 1993 and January 19,-1999), for HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE. A copy of the '699 patent, together with its reexamination certificates, is attached hereto as Exhibit A.

10 11 12 13 14 15 16 17 6. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '699 patent (including, but not limited to. Claim 1 of the '699 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is further informed and believes, and on that basis alleges, that this infringement will continue unless and until enjoined by this Court.

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19 20 22 7. IR has notified IXYS of its infringement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

SECOND CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 5,008,725)

8. IR is and has been the owner by mesne assignment of United States Letters Patent No. 5,008,725 (the "'725 patent") which issued April 16, 1991 (Reexamination Gase 2:00-cv-06756-R-CT Document 1 Filed 06/22/00 Page 5 of 76 Page ID #:933

1 2 3 certificate issued January 12, 1993), for PLURAL POLYGON SOURCE PATTERN FOR MOSFET. A copy of the '725 patent, together with its reexamination certificate, is attached hereto as Exhibit B.

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5 6 7 8 9 10 11 12 9. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '725 patent (including, but not limited to, Claims 3, 7 and 8 of the '725 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is further informed and believes, and on that basis alleges, that this infiingement will continue unless and until enjoined by this Court.

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14 15 16 17 10. IR has notified IXYS of its infiingement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

THIRD CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 5,130,767)

11. IR is and has been the owner by mesne assignment of United States Letters Patent No. 5,130,767 (the "'767 patent"), which issued July 14, 1992, for PLURAL POLYGON SOURCE PATTERN FOR MOSFET. A copy of the '767 patent is attached hereto as Exhibit C.

12. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles

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1 2 3 4 5 6 (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '767 patent (including, but not limited to, Claims 3, 5 and 7 of the '767 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is fiarther informed and believes, and on that basis alleges, that this infringement will continue unless and until enjoined by this Court.

13. IR has notified IXYS of its infringement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

FOURTH CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 4,642,666)

14. IR is and has been the owner by mesne assignment of United States Letters Patent No. 4,642,666 (the "'666 patent"), which issued February 10, 1987 (Reexamination Certificate issued October 27, 1998), for HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE. A copy of the '666 patent, together with its reexamination certificate, is attached hereto as Exhibit D.

15. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '666 patent (including, but not limited to. Claim 1 of the '666 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles.

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16. IR notified IXYS of its infringement, which was willful and deliberate. IR has been damaged by the above-alleged infringement.

FIFTH CLAIM FOR RELIEF

(Against All Defendants For Patent Infringement, U.S. Patent No. 4,705,759)

17. IR is and has been the owner by mesne assignment of United States Letters Patent No. 4,705,759 (the "'759 patent"), which issued November 10, 1987, (Reexamination Certificate issued Febmary 14, 1995), for HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE. A copy of the '759 patent, together with its reexamination certificate, is attached hereto as Exhibit E.

18. IR is informed and believes, and on that basis alleges, that (a) IXYS has made, used, sold or offered for sale in this District and elsewhere in the United States articles (including, but not necessarily limited to, part numbers IXFX55N50, IXFH21N50, IXFH35N30, and IXTH24N50) infringing the '759 patent (including, but not limited to, Claim 1 of the '759 patent) and (b) DOES 1-10 have in this District and elsewhere in the United States sold and offered for sale such articles. IR is further informed and believes, and on that basis alleges, that this infringement will continue unless and until enjoined by this Court.

19. IR has notified IXYS of its infringement, which has been and continues to be willful and deliberate. IR has been and continues to be damaged by the above-alleged infringement and will suffer irreparable harm until such time as that infringement is enjoined.

Wherefore, Intemational Rectifier prays for judgment as follows:

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Lidow et al.

[34] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

- **[73] Inventors: Alezander Lidow, Manhattan Beach; Thonna Hcnnni, Redondo Beacii, both of Calif.**
- [73] Assignee: International Rectifier Corporation, **El Segundo, Calif.**
- **[21] Appi. No.: 371,fi78**
- **[22] Filed: Jan. 22,1989**

Related U.S. Application Data

- **[60] Continuation of Ser. No. 90,664, Aug. 27, 1987, aban**doned, which is a division of Ser. No. 456,813, Jan. 10, **1983, abandoned, which is a division of Ser. No. 232,713, Feb. 9, 1981, Pat No. 4,376,286, which is a continuation of Ser. No. 931,310, Oct. 13, 1978, abandoned. «**
- [51] Int. Cl.⁵ H01L 29/68; H01L 29/10; **HOIL 27/02**
- **[52] VS. CL 357/23.7; 337/23.8; 357/23.^ 357/41; 357/43**
- [58] **Field of Search 357/23.7, 23.8, 23.4, 357/41,43, 86**

[56] Referanees Qted

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

(List continued on next page.)

im Patent Number 11 of 76,959,699 [45] **Date of Patent: Sep. 25,1990**

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j. Plummer et aL, "A Monolithic 200-V CMOS Analog Switch," IEEE Joumal of Solid-State Circuits, vol. SC-11 #6, Dec. 1976. pp. 809-817.

B. Scharf et al., "A MOS-ControUed Triac Device," 1978 IEEE Intemational Solid-State Circuits Conference, San Francisco, Calif., Feb. 13-17, 1978, pp. 222-223.

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H. Sigg et al., "D-MOS Transistor for Microwave (List continued on next page.)

Primary Examiner—Rolf Hille

Aaatant Examiner—Fetsum Abraham Attorney, Agent, or Firm-Ostrolenk, Faber, Gerb & **SofFen**

[57] ABSTRACT

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor **chip which are controlled by the same gate. The channels lead firom the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by form**ing a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

24 Claiau, 5 Drawing Sheets

Exhibit A - Page

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U.S. Patent Sep. 25, 1990 Sheet 1 of 4,959,699

Exhibit A - Page $\frac{1}{2}$

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U.S. Patent Sep. 25, 1990

Sheet 3 of 5

4,959,699

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U.S. Patent •Sep. 25, 1990 Sheet 5 of **4,959,699**

FORWARD VOLTAGE (VOLTS)

Exhibit $A-Page_15$

s

HIGH POWER MOSFET WIIH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

10 of application Ser. No. 232,713, filed Feb. 9,1981. now This is a continuation of application Ser. Na 07/090,664 filed on Aug. 27. 1987, now abandoned, which is a division of application Ser. No. 436.813, filed Jan. 10,1983 now abandoned which in turn, is a division U.S. Pat No. 4,376.286. issued Mar. 8. 1983 which, in turn, is a continuation of application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices and more specificaUy relates to a novel structure for a MOSFET device which permits it to be used in high power applications with a relativdy high reverse voltage and with an exceptionally low on-resistance. The major advan- 20 tage of the bipolar transistor over the MOSFET transistor is that the bipolar transistor has a very low on-resistance per unit conductive area. The MOSFET transistor **has numerous advantages over fhe bipolar transistor including very high switching speed, very high gain and 23 lack of the secondary breakdown characteristics exhibited by a minority carrier device. However, because the MOSFET transistor has high on-resistance. its use m** high power switching applications has been limited.

BRIEF DESCRIPTION OF THE INVENTION

33 devices in a switching type application while retaining The present invention provides a novel high power MOSFET device wliich has a low forward resistance so that the device becomes more competitive with bipolar all of the numerous advantages of the MOSFET over the bipolar device. In particular, with the present invention, the forward resistance per unit area of the device has been reduced by at least a factor of two, compared to the limiting resistance per unit area previously existing in a MOSFET-type device.

In one embodiment of the invention, two sources are **placed on the same surface of a semiconductor wafer and are laterally spaced from one another. A gate electrode, deposited on a conventional gate oxide, is dis- 43 posed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced from one another by an n-type bulk region. Current** from each source can flow through its respective chan**nel (after the creation of the inversion layer defining the 30** channel), so that majority carrier conduction current **can flow through the bulk region and across the wafer or chip to the drain electrode. The drain electrode may be on the opposite surface of the wafer or on a laterally displaced surface region from the source electrodes. 33 This configiiration is made using the desirable manufacturing techniques of the D-MOS device, which permits precise alignment of the various electrodes and channels and permits use of extremely small channel lengths.** heis and permits use of extremely small channel lengths. The clup of FIOS. I and 2 and particularly show
While the above configuration may have been previ- 60 $p(+)$ conductivity implant and diffusion step. **ously described fbr a MOSFET signal-type device, the structure is not that of the commonly used signal MOS-FET.**

The device is basically formed in an n(—) substrate which has the relatively high resistivity which is neces- 65 channel implant and diffusion step. **sary to obtain the desired revene voltage capability of** the device. For example, for a 400 volt device, the $n(-)$ region will have a resistivity of about 20 ohm-centime-

ters. However, this same necessary high resistivity characteristic has caused the on-resistance of the MOSFET device, when used as a power switch, to be relatively **high.**

In accordance with the present invention, it has been found that in the upper portion of the central bulk re**gion to which the two inversion layers feed current in the path to the drain electrode, the central region immediately beneath the gate oxide can be a relatively low** resistivity material formed, for example, by an $n(+)$ diffusion in that channel region, without affecting the **reverse voltage characteristics of the device.**

13 30 More specifically, and in accordance with the invention, this common channel will have an upper portion beneath the gate oxide and a lower bulk portion extending toward the drain electrode. The lower portion has the high resistivity desired to produce high reverse voltage ability, and will have a depth dependent on the desired reverse voltage for the device. Thus, for a 400 volt device, the lower n(—) region may have a depth of about 33 microns, while for a 90 volt device it will have a depth of about 8 microns. Other depths will be se**lected, depending on the desired reverse voltage of the device to provide the necessary thicker depletion region required to prevent punch-through during reverse voltage conditions. The upper portion of the common channel is made highly conductive (a+) to a depth of firom about 3 to about 6 microns. It has been found that this does not interfere with the reverse voltage withstand ability of the device. However, it decreases the on-resistance per unit area of the device by more than a on-resistance per unit area of the device by more than a**
factor of two. The resulting device becomes competi**tactor of two. The resulting device becomes competi-**
tive with conventional high ipower bipolar switching tive with conventional high power bipolar switching devices since it retains all of the advantages of the **MOSFET** device over the bipolar device but now has **major characterizing advantage of the bipolar device.**

:In accordance .with another feature of the present invention, the p-type region which defines the channel **beneath the gate oxide has a relatively deeply diffused portion beneath the source so that the p-type diffusion** portion beneath the source so that the p-type diffusion region will have a large radius of curvature in the $n(-)$ epitaxial layer forming the body of the device. This **improve the voltage gradient at the edge of the device unprove the voltage gradient at the edge of the device and thus permits the use of the device with higher re**and thus permits the use of the device with higher reverse voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a high power MOSFET chip **which incorporates the present invention and particularly illustrates the metalizing pattems of the two sources and the gate.**

FIG. 2 is a cross-sectional view of FIG. 1 taken across the section line 2—2 in FIG. 1.

FIQ. 3 is a cross-sectional view similar to FIG. 2 showing the initial step m the process of manufacture of the chip of FIGS. 1 and 2 and particularly shows the

FIG. 4 shows the second step in the manufacturing process and shows the $n(+)$ implant and diffusion step.

FIG. S shows a further step in the process of manufacture of the chip of FIGS. 1 and 2 and shows the

FIO. 6 shows a further step in the process of manufacture and illustrates the source predeposition and diffusion step. This precedes the last step in which the

Exhibit A – Page 16

gate oxide is cut for the metalization step which produces the device of FIG. 2.

FIG. 7 is a plan view of the metalizing pattern of a second embodiment of the invention.

FIG. 8 is a cross-sectional view of FIG. 7 taken 5 across the section line 8—8 in FIG. 7.

FIG. 8a is a view similar to FIG. 2 and shows a modified source contact configuration.

teristics of a device like that of FIG. 2 where the region 10 an elongated serpentine $p(+)$ conductivity region be-FIG. 9 shows the shape of forward-current charac-40 beneath the oxide is $n(-)$.

FIG. 10 shows the shape of the characteristic of a device identical to tbat of FIG. 2 where the region 40 has high $n(+)$ conductivity.

DETAILED DESCRIPTION OF THE DRAWINGS

A first embodiment of the novel MOSFET device of the present invention is shown in FIGS. 1 and 2 which show a chip of monocrystalline silicon 20 (or some 20 other suitable material), with the device electrodes fol-
lowing the serpentine path 21 best shown in FIG. 1 in By using D-MOS fabrication techniques, two $n(+)$ lowing the serpentine path 21 best shown in FIG. 1 in By using D-MOS fabrication techniques, two $n(+)$ order to increase the current-carrying area of the de-regions 32 and 33 are formed beneath source electrodes order to increase the current-carrying area of the de-
vice. Other geometries could be used. The device illustrated has a reverse voltage of about 400 volts and an 25 on-resistance less than about 0.4 ohm with a channel spectively. Channel regions 34 and 35 are disposed width of 50 centimeters. Devices having reverse volt-
beneath the gate oxide 25 and can be inverted by the width of 50 centimeters. Devices having reverse volt-
ages of from 90 to 400 volts have been made. The 400 appropriate application of a biasing signal to the gate 24 volt devices have carried pulse currents of 30 amperes. in order to permit conduction from the source 22 and
The 90 volt devices have had forward on-resistances of 30 the source 23 through the inversion layers into the cen The 90 volt devices have had forward on-resistances of 30 about 0.1 ohm with a channel width of 50 centimeters about 0.1 ohm with a channel width of 50 centimeters tral region disposed beneath the gate 24 and then to the
and have carried pulse currents up to about 100 am-
drain electrode 26. Channels 34 and 35 may each have a peres. Higher and lower voltage devices can also be made with varying channel widths.

higher on-resistances than the above. For example, a between $p(+)$ regions 30 and 31) should have a high 400 volt MOSFET comparable to that described below resistivity in order to permit the device to withstand 400 volt MOSFET comparable to that described below resistivity in order to permit the device to withstand but made with prior art techniques would normally high reverse voltages. However, the relatively high but made with prior art techniques would normally high reverse voltages. However, the relatively high have an on-resistance much greater than about 1.5 resistivity $n(-)$ material is also a significant contributohms, as compared to an on-resistance less than about 40 0.4 ohm in a device made according to this invention. Moreover, the MOSFET switching device of the present invention will exhibit all of the desirable advantages of the MOSFET device, since it operates as a majority carrier device. These advantages include high switch- 45 ing speed, high gain and avoidance of the secondary breakdown characteristics which exist in minority carrier devices.

The device of FIGS. 1 and 2 has two source electrodes 22 and 23 which are separated by a metalized 50 gate electrode 24 which is fixed to but spaced from the semiconductor device surface by a silicon dioxide layer 25. The serpentine path followed by gate oxide 25 has a length of 50 centimeters and has 667 undulations, but is shown more simply in FIG. 1. Other channel widths 55 can be used. Source electrodes 22 and 23 can be laterally extended as shown to serve as field plates to help spread the depletion region created during reverse voltage conditions. Each of source electrodes 22 and 23 supply current to a common drain electrode 26 which is 60 reduced by a factor greater than two. Moreover, it has fixed to the bottom of the wafer. The relative dimen-
been found that the provision of the high conductivity sions for the device, particularly in thickness, have been region 40 does not interfere with the reverse voltage grossly exaggerated in FIG. 2 for purposes of clarity. characteristics of the device. Accordingly, by making grossly exaggerated in FIG. 2 for purposes of clarity. characteristics of the device. Accordingly, by making The silicon chip or wafer 20 is formed on an $n(+)$ sub-
the region beneath the gate oxide 25 and between chan-The silicon chip or wafer 20 is formed on an $n(+)$ sub-
strate which may have a thickness of about 14 mils. An 65 nels 34 and 35 more highly conductive, the forward strate which may have a thickness of about 14 mils. An 65 nels 34 and 35 more highly conductive, the forward $n(-)$ epitaxial layer is deposited on substrate 20 and will on-resistance of the ultimate high power switching d $n(-)$ epitaxial layer is deposited on substrate 20 and will on-resistance of the ultimate high power switching de-
have a thickness and resistivity depending on the de-
vice has been significantly reduced and the MOSFET have a thickness and resistivity depending on the de-
sired reverse voltage. All junctions are formed in this device becomes far more competitive with an equiva-

epitaxial layer which can have a relatively high resistivity. In the embodiment disclosed, the epitaxial layer has a thickness of about 33 microns and a resistivity of about 20 ohm-centimeters. For a 90 volt device, epitaxial layer 20 would be about 10 microns thick and would have a resistivity of about 2.3 ohm-centimeters. A channel width of 30 centimeters is also used to provide the desired current carrying capacity for the device.

15 of the prior art except that the maximum $p(+)$ region In a preferred embodiment of the invention, there is neath each of the source electrodes 22 and 23 which thus extends around the serpentine path shown in FIG. 1. These $p(+)$ regions are shown in FIG. 2 as the $p(+)$ regions 30 and 31, respectively, and are similar to those depth is greatly exaggerated in order to form a large radius of curvature. This allows the device to withstand higher reverse voltages. By way of example, the depth of regions 30 and 31 is preferably about 4 microns at the

22 and 23, respectively, and define, with the $p(+)$ regions 30 and 31, n-type channel regions 34 and 35, reappropriate application of a biasing signal to the gate 24
in order to permit conduction from the source 22 and drain electrode 26. Channels 34 and 35 may each have a length of about 1 micron.

It has previously been thought necessary that the Presently known MOSFET devices have much 33 central n(—) region between channels 34 and 35 (and resistivity $n(-)$ material is also a significant contribut-
ing factor to the high forward on-resistance of the device.

> In accordance with the significant feature of the present invention, a significant portion of this central conducting region is made relatively highly conductive and consists of an $n(+)$ region 40 disposed immediately beneath the gate oxide 25. The $n(+)$ region 40 has a depth of about 4 microns and could range from about 3 microns to about 6 microns. While its exact conductivity is not known, and varies with depth, it is high relative to the $n(-)$ region beneath it. More particularly, region 40 has a high conductivity which would be determined by a total ion implanted dose of from about 1×10^{12} to 1×10^{14} phosphorus atoms/cm² at 50 kV followed by a diffusion drive at from 1150° C. to 1250° C. for from 30 minutes to 240 minutes. It has been found that by making this region 40 relatively highly conductive $n(+)$ material through a diffusion or other operation, the device characteristics are significantiy improved and the forward on-resistance of the device is been found that the provision of the high conductivity device becomes far more competitive with an equiva-

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lent junction-type device while still retaining all of the

assumed that the conduction channels 34 and 35 are of the step of FIG: 6 to the device shown in FIG. 2 **p(+) material and are. accordingily, inverted to an n- S wherem the oxide surfaces on top of the chip are suittype conductivity to provide a majority carrier conduc- ably stripped and the metalizing pattems for contacts** tion channel from sources 22 and 23 to the central re- 22, 23 and 24 are formed to establish electrical contacts gion 40 upon the application of an appropriate gate to the device. The drain contact 26 is applied to the voltage. Clearly, however, all of these conductivity device in a subsequent metalizing operation. Thereafter, types could be reversed so that the device could work 10 the entire device may be appropriately coated with a as a p-channel device rather than an n-channel device as suitable passivation coating and wire leads are con-

could be constructed is shown in FIGS. 3 to 6. Refer-

tive housing, with the drain electrode fixed to the housring to FIG. 3, the base wafer 20 is shown as an $n(+)$ 15 ing or other conductive support which serves as a drain **material having an n(—) epitaxially deposited region on connection.** top thereof. A thick oxide layer 50 is formed on wafer The device shown in FIGS. 1 and 2 utilizes a serpen-
20 and windows 51 and 52 are opened therein. The open time nath for each of the source regions and gate regions windows 51 and 52 are exposed to a beam of boron and a drain on the surface of the wafer opposite to the atoms in an ion implanting apparatus to form $p(+)$ 20 source electrodes. Other configurations can be used.
regions. Thereafter the implanted boron atoms are $p(1/2S - 7 - 4R)$ illustrate a plane configuration which is regions. Therefore the implanted boron atoms are **FIGS.** 7 and 8 illustrate a planar configuration which is caused to diffuse deeper into the wafer to form the a single accessories are approximately $\frac{1}{2}$ rounded $p(+)$ concentration region shown in FIG. 3 $\frac{1}{2}$ and 80 which might have a depth of about 4 microns. During $\frac{1}{2}$ and a flux of sing shape and a gentral source elecwhich imight have a depth of about 4 microns. During
this diffusion operation, shallow oxide layers 53 and 54 25 degrees of shown in FIC1 **0** is contributed within a boost

cut in the oxide layer 50 and an $n(+)$ implant takes
also to implant the $n(1)$ orders 63 and 64 into the state of the various current paths of the device leading place to implant the $n(+)$ regions 63 and 64 into the same of the various current paths of the device leading $n(-)$ enjoying $n(-)$ and $n(-)$ implantation can be 20, to the laterally displaced drain electrode 85 which sur $n(-)$ epitaxial layer. This $n(+)$ implantation can be 30 ^{to the} ^{atterativ} ^{dia} carried out with a phosphorus beam. Thereafter, the $\frac{1}{\text{N}}$ $\frac{1}{\text{N}}$ ring-shaped $n(+)$ region **36** is formed within the implanted regions are subjected to a diffusion step to \sim nig-shaped n(+) region 86 is formed within the \sim device as shown in FIG. 8 and, in accordance with the cause the regions 63 and 64 to expand and deepen to a ^{concurce} as shown in FIG. 6 and, in accordance with the concentration determines with a concentration of the **cordination** of the **cordination** of the concentration o depth of about 3¹ microns with a concentration deter-
mined by an implemention does of 1×10^{12} to 1×10^{14} as higher conductivity than the n(-) epitaxially deposited mined by an implantation dose of 1×10^{12} to 1×10^{14} 35 mgner conductivity tian the n(-) epitaxially deposited phoenhorus stoms/cm2 followed by a drive for 30 min. region 87 which contains all the junctions of th phosphorus atoms/cm² followed by a drive for 30 min-
where to 4 hours at from 1150° C to 1250° C As will be. The ring-shaped region **36** extends from the region utes to 4 hours at from 1150° C. to 1250° C. As will be The ring-shaped region 60 extends from the region
later seen regions 63 and 64 produce the novel $n(+)$ beneath the gate oxide 88 and adjoins the ends of the later seen, regions 63 and 64 produce the novel $n(+)$ beneath the gate oxide 88 and adjoins the ends of the ring-
region which substantially reduces the on-resistance of the WO-conducting channels formed between the ring**region which substantially reduces the on-resistance of** \cdot **the device.**

could, if desired, be epitaxially deposited and need not source 82, respectively.
he diffused Similarly, the resulting device being de-
It will also be noted in FIG. 8 that the outer periphbe diffused. Similarly, the resulting device being de-
scribed herein could be manufactured by any desired

process as would be apparent to those skilled in the art. 45
The next step in the process is shown in FIG. 5 and is the channel implantation and diffusion step in which the good contact to drain electrode 85. Drain electrode 85
 $p(+)$ regions 71 and 72 are formed through the same is widely laterally spaced from source 81 (by greater $p(+)$ regions 71 and 72 are formed through the same is widely laterally spaced from source 81 (by greater windows 61 and 62 that were used for the $p(+)$ implan-
than about 90 microns). The drain contact 85 is surwindows 61 and 62 that were used for the n(+) implantation for regions 63 and 64. The $p(+)$ regions 71 and 72 so rounded by a $p(+)$ isolation diffusion 96 to isolate the are formed by implanting with a boron beam to a dose device from other devices on the same chip or wafe of about 5×10^{13} to 5×10^{14} atoms/cm² followed by a diffusion drive for 30 to 120 minutes at 1150° C. to 1250° current flow from sources 81 and 82 goes through the

out for the source predeposition and the diffusion of the drain contact 85. As in the embodiment of FIG. 2, de-
source regions 32 and 33. This is carried out by a con-
vice resistance is greatly reduced by the relatively source regions 32 and 33. This is carried out by a conventional and non-critical phosphorus diffusion step highly conductive region 86. where the diffusion proceeds through the windows 61 In carrying out the above invention, it should be and 62 so that the source regions 32 and 33 are automati- 60 noted that any type of contact material can be used to cally aligned relative to the other preformed regions. make the source and gate contacts. By way of exampl cally aligned relative to the other preformed regions. make the source and gate contacts. By way of example, Thus, the wafer is placed in a furnace and exposed to aluminum could be used for the source electrodes while Thus, the wafer is placed in a furnace and exposed to aluminum could be used for the source electrodes while **POCl**₃ suspended in a carrier gas for from 10 minutes to a polysilicon material can be used for the conductive POCI₃ suspended in a carrier gas for from 10 minutes to a polysilicon material can be used for the conductive 30 minutes at a temperature of from 850° C. to 1000°. gate **30** in FIG. 8 or the conductive gate 24 in FIG. 2.

When this step is completed, the basic junction con- 65 figuration required in FIG. 2 is formed with short $p(+)$ conducting channel for the ultimately constructed de-

lent junction-type device while still retaining all of the vice and with an $n(+)$ region filling the area between $p(+)$ regions 30 avartages of the MOSFET majority carrier operation. the channels 34 and 35 and between $p(+$ the channels 34 and 35 and between $p(+)$ regions 30 In the above description of FIGS. 1 and 2, it has been and 31. The manufacturing process then continues from **disclosed, nected to the source electrodes 22 and 23 and the gate** One process by which the device of FIGS. 1 and 2 24. The device is then mounted within a suitable protec-

tine path for each of the source regions and gate regions a simple rectangular arrangement having a ring-shaped device as shown in FIG. 8 is contained within a base wafer of $p(-)$ monocrystalline silicon 83 which may grow over the windows 51 and 52.
As is next shown in FIG. 4, windows 61 and 62 are
wafer of p(-) monocrystalline silicon 83 which may
not in the oride laure 50 and an $r(1)$ implest takes
a buried $n(+)$ region 84 to reduc

 $\frac{1}{40}$ shaped $p(+)$ region 89 and the central $p(+)$ region 91
It should be noted that the $n(+)$ regions 63 and 64 $\frac{1}{40}$ disposed beneath the ring-shaped source 81 and central disposed beneath the ring-shaped source 81 and central source 82, respectively.

 $\exp 90$ of the $p(+)$ ring 89 has a large radius to assist the device in withstanding high reverse voltages.

An n(+) region 95 in FIG. 8 is provided to ensure good contact to drain electrode 85. Drain electrode 85

device from other devices on the same chip or wafer.
In the arrangement of FIG. 8, like that of FIG. 2, **C. width of epitaxial region 87. through the region 86. The Thereafter, and as shown in FIG. 6, steps are carried 33 current then flows laterally outward and then up to the**

Solute 30 in FIG. 8 or the conductive gate 24 in FIG. 2. Numerous other geometries can be used to make the **figuration required in FIG. 2 is formed with short** $p(+)$ **device of the invention, including a plurality of pairs of regions disposed beneath the oxide 50 to serve as the straight, parallel source elements with respective** straight, parallel source elements with respectively interposed gates and the like.

The source electrodes 22 and 23 have been shown as separate electrodes which can be connected to separate leads. Qearly. the sources 22 and 23 could be directiy connected as shown in, FIG. 8a where components similar to those ofFIG. 2 faave been given sunilar identi- 5 fying numerals. In FIG. 8a, however, the gate electrode **is a polysilicon layer 101 (in place of aluminum) deposited atop gate oxide 25. The gate 101 is then covered with oxide layer 102 and a conductive layer 103 connects the two sources 22 and 23 togetfaer to form a 10** single source conductor which is insulated from gate **101. Connection is made to the gate at some suitable edge portion of the wafer.**

FIGS. 9 and 10 show the shape of measured curves **which demonstrate the reduction in forward resistance** when the region 40 is made highly conductive $(n+)$. In FIG. 9, the device tested had a region 40 which had the **n(—) resistivity of the epitaxial region. Thus, the for**ward resistance is characteristically high at different ₂₀ **gate biases as shown in FIG. 9. ^**

In the device of the invention where region 40 is of $n(+)$ conductivity, there is a dramatic decrease in the *on-resistance as shown in FIG. 10 for all gate voltages before velocity saturation of the electrons occurs. ^*

Although the present invention has been described in ²⁵ **connection with a preferred embodiment thereof, many variations and modifications will now become apparent** to those skilled in the art. It is preferred, therefore, that **the present invention be limited not by the specific JQ disclosure herein, but only by the appended claims.**

What is claimed is:

1. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

- **a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a rela^ tively lightiy doped major body portion for receiv- 40 ing junctions and being doped with impurities of one conductivity type;**
- **at leaat first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from 45 said first semiconductor surface to a first depth** beneath said first semiconductor surface; the space **between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor sur- so face location;**
	- **first and second source regions of said one conductiv**ity type formed in each pair of said at least first and **second base regions respectively at first and second** first surface location to a depth less than said first 55 **depth; the outer rim of each of said first and second source regions being laterally spaced along said first semiconductor surface firom the lateral outer periphery of its said base region to define first and second channel regions along said first semicon- 60 ductor surface between each pair of said first and second source regions, respectively, and said common conduction region;**
	- **source electrode means connected to said source regions; 63**
	- **gate insulation layer means on said first surface, disposed at least on said first and second channel regions;**
- gate electrode means on said gate insulation layer means and overlying said first and second channel **regions;**
- **a drafai conductive region remote firom said common region and separated therefirom by said relatively** lightly doped major body portion;
- **a drain electrode coupled to said drain conductive region; and**
- **at least said first base region being a cellular polygo**nal region; said cellular polygonal region being **surrounded by said common conduction region; said first source region having the shape of an annular ring disposed within said cellular polygonal first base region.**

2. The device of claim 1 wherein said common con**duction region is relatively-highly doped compared to** said relatively highly doped major body portion and **extends from said given first semiconductor surface** location to a depth greater than the depth of said source region, but less than said first depth of said first and second spaced base regions, whereby resistance to cur**rent flow at the junctures between said first and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightiy doped major body portion is reduced.**

3. The device of claim 1 wherein said source elec**trode means comprises a suigle sheet of conductive material disposed over and contacting each of said source regions.**

4. A high power metal oxide silicon field effect trau; sistor device exhibiting relatively low on-resistance and relatively high: breakdown : voltage; said-device comprising:

- **a wafer of semiconductor material having first and second oppoang semiconductor surfaces; said wafer of semiconductor material having, a relatively lightiy doped major body portion for receiving junctions and being doped with impurities of one conductivity type;**
- **at least first and seccmd spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a first depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a common conduction region of one conductivity type at a given first semiconductor sur**face location:
- **first and second source regions of said one conductiv**ity type formed in each pair of said at least first and second base regions respectively at first and second **first surface locations and extending firom said first . and second first surface locations to a depth less than said first depth; the outer rim of each of said** first and second source regions being laterally **spaced along said fint semiconductor surface from the lateral outer peripfaery of its said base region to** define first and second channel regions along said first semiconductor surface between each pair of **said first and second source regions, respectively, and said common conduction region;**
- **source electrode means connected to said source regions; ,**
- **gate insulation layer means on said first surface, disposed at least on said fint and second channel region^**

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11 material disposed over and contacting each of said source regions.

15. The device of claim 8, wherein said common conduction region is relatively faigfaly doped compared to said relatively lightiy doped major body portion and 3 extends from said given first semiconductor surface location to a depth greater than the depth of said source region but less than said depth of said firat and second base regions, whereby resistance to current flow at the junctures between said first and second surface channel 10 **regions and said common conduction region and between said common conduction region and said relatively lightiy doped major body portion is reduced.**

16. The device of claim 7 wherein said source elec**trode means makes electrical contact to the surface of 13 said cellular polygonal region and the surface of said annular ring-shaped region.**

17. The device of claim 8 wherein said source elec**trode means makes electrical contact to the surface of** said cellular polygonal region and the surface of said 20 **annular ring-sliaped ring.**

18. The device of claim 15 wherein said source electrode means makes electrical contact to the surfiace of said cellular polygonal region and the surface of said annular ring-shaped ring. 19. A high power metal oxide silicoh field effect tran-

sistor device exhibiting relatively low on-resistance; said device comprising:

- **a wafer of semiconductor material having first and** second opposing semiconductor surfaces; said 30 **wafer of semiconductor material having a relatively lightiy doped major body portion for receiving junctions and being doped with impurities of one conductivity type;**
- **at least fint and second spaced base regions of the 33** opposite conductivity type to said one conductiv**ity type formed in said wafer and extending from said fint semiconductor surface to a fint depth beneath said first semiconductor surface; the space between said at least fint and second base regions 40 said annular ring-shaped source region,** defining a common conduction region of one con-
 24. The device of claim 19 wherein each of said at ductivity type at a given first semiconductor sur-

least first and second spaced base regions of said oppo-
- **first and second source regions of said one conductivity type formed in each pair of said at least first and 45 define fint and second cfaannel regions along said regions.** first semiconductor surface between each pair of

said firat and second source regions, respectively, and said common conduction region;

- **source electrode means connected to said source regions;**
- **gate insulation layer means on said first surface, disposed at least on said fint and second channel re-**
- **gato electrode means on said gate insulation layer** means and overlying said first and second channel **regions;**
- said wafer including a further region of opposite **conductivity type adjoining said lightly doped major body portion; and**

an electrode coupled to said further region.

20. The device of claim 19 wherein at least said first **base region comprises a cellular polygonal region; said cellular polygonal region bemg surrounded by said common conduction region; said fint source region** having the shape of an annular ring disposed within said cellular polygonal first base region.

21. The device of claim 19 wherein said common conduction region is relatively highly doped compared to said relatively lightly doped major body portion and **wherein said common conduction region extends from** said given first semiconductor surface location to a **depth greater than the depth of said source region but less than said depth of said fint and second base regions,** whereby resistance to current flow in the path between said first and second surface channel regions and said **common conduction region and between said common** conduction region and said relatively lightly doped **major body portion is reduced.**

22. The device of claim 19 wherein said source electrode means comprises a.single sfaeet of conductive material disposed over and contacting each of said source regions.

23. The device of claim 19 wherein said source electrode means .makes.electrical contact.to the surface of said cellular polygonal base.region and the. surface of

ductivity type at a given fint semiconductor sur- least first and second spaced base regions of said oppoface location; site conductivity type have respective profiles which ity type formed in eacfa pair of said at least firat and 43 said common conduction region and underlying their second base regions respectively at first and second said respective first and-second source regions, and **first** surface locations and extending from said first respective relatively deep, relatively large radius re**fint surface locations and extending from said firat respective relatively deep, relatively large radius re**and second first surface locations to a depth less gions extending from said shallow depth regions which than said first depth; the outer rim of each of said are laterally spaced from beneath said respective source are laterally spaced from beneath said respective source first and second source regions being laterally 50 regions on the side of said source regions which is away spaced along said first semiconductor surface from from said common conduction region; said shallow base spaced along said first semiconductor surface from from said common conduction region; said shallow base
the lateral outer periphery of its said base region to regions partially underlying their respective source regions partially underlying their respective source

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gate electrode means on said gate insulation layer **means and overlying said fint and second channel regions;**

- **a drain conductive region remote from said common region and separated therefrom by said relatively lightiy doped major body portion; and**
- **a drain electrode coupled to said drain conductive region;**
- said common conduction region being relatively **faigfaly doped compared to said relativdy lightiy 10 doped major body portion and extending from said given fint semiconductor surface location to a depth greater than the depth of said source region but less than said first depth of said first and second** spaced base regions, whereby resistance to current ¹⁵ **flow at the junctures between said first and second** surface channel regions and said common conduc**tion region aad between said common conduction region and said rdativdy lightiy doped major body portion is reduced, wfaerein said source dectrode means comprises a siiigle sheet of conductive material disposed over and contacting each of. said source regions. 20**

5. The device of claim 2 wherein said source electrode means comprises a single sheet of conductive **materid disposed over and contacting each of said source regions. 25**

6. The device of claim 1 wherein said source elec**trode means makes electricd contact to the surface of said cellular polygond region and the'surface of said annular region-shaped ring. 30**

7. A three-terminal power metal oxide silicon field **effect transistor device comprisuig:**

- a wafer of semiconductor material having first and second opposing semiconductor surfaces; said **wafer of semiconductor materid having a rela**tively lightly doped major body portion for receiving junctions and being doped with impurities of **one conductivity type;**
- one conductivity type;
at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between $\overline{45}$ **said at least fint and second base regions defining a common conduction region of one conductivity** type at a given first semiconductor surface loca-**. tion;**
- **fint and second source regions of said one conductiv-50 ity type fonned in each pair of said at least first and** second base regions respectively at first and second first surface locations and extending from said first **and second fint surface locations to a depth less than said depth of said base regions; said first and 55** second source regions being laterally spaced along said first semiconductor surface from the facing **respective edges of said conunon conduction re**gion thereby to define first and second channel
regions along said first semiconductor surface be- 60 tween each pair of said first and second source **regions, respectivdy and said common conduction region;**
- **source electrode means connected to said source regions and comprising a fint terminal;**
- gate insulation layer means on said first surface, disposed at least on said first and second channel re**gions;**

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- gate electrode means on said gate insulation layer **means, overlying said first and second cfaaimel regions and comprisuig a second termind;**
- **a drain conductive region remove firom sud common region and separated therefrom by said relativdy lightiy doped major body portion;**
- **a drain electrode coupled to said drain conductive region and comprising a third terminal;**
- **each of said at least first and second spaced base re**gions of said opposite conductivity type having respective profiles which include relatively shal**low depth regions extending from said common** region and underlying their said respective first and second source regions, and respective rela**tivdy deep, relatively large radius regions extenduig from said shallow depth regions which are laterdly spaced from beneath said respective source regions on the side of said source regions** which is away from said common region;
- at least said first base region being a cellular polygo**nd region; said cellular polygond region being surrounded by said common conduction region;** said first source region having the shape of an annular ring disposed within said cellular polygonal **fint base region; said relatively shallow depth region of said first base region surrounding the outer** periphery of said relatively deep portion of said **first base region.**

8. The device of daim 7 wherein said shallow base regions partially underlie their respective source re-

9. The device of claim 7 wherein said common con- . duction region is relatively highly doped compared to said relatively lightly doped major body portion and **extends'firom said given first semiconductor surface** location to a depth greater than the depth of said source **region but.less.tfaan said depth of said fint and second** base regions, whereby resistance to current flow at the **junctures between said first and second surface channel regions and said common conduction region and be**tween said common conduction region and said rela**tivdy lightiy doped major body portion is reduced.**

10. The device of claim 8 wherein said common conduction region is relatively highly doped compared to **said relativdy lightly doped major body portion and extends from said given fint semiconductor surface** location to a depth greater than the depth of said source **region but less than said depth of said fint and second base regions, whereby resistance to current flow at the junctures between said fint and second surface channel regions and said common conduction region and between said common conduction region and said relatively lightiy doped major body portion is reduced.**

11. Tbe device of daim 7 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said **source regions.**

12. The device of claim 8 wherein said source electrode means comprises a single sheet of conductive material disposed over and contacting each of said **source regions.**

65 material disposed over and contacting each of said 13. The device of claim 9 wherein said source elec**trode means comprises a single sfaeet of conductive source regions.**

14. The device of claim 10 wherein said source elec**trode meana comprises a single sheet of conductive**

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United States Patent [19] **REEXAM EXAMPLE 111 B1 4,959,699**

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

[76] Inventors: Alexander Lidow, Manhattan Beach; Thomas Herman, Redondo Beach, both of Calif.

Reexamination Request:

No. 90/002.515, Nov. 13, 1991

Reesamination Certificate for:

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- [60] Continuation of Ser. No. 90,664, Aug. 27, 1987, abandoned, which is a division of Ser. No. 456,813, Jan. 10, 1983, abandoned, which is a division of Ser. No. 232,713. Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.
- [51] Int. Cl.⁵ H01L 29/10; H01L 29/78; HOIL 29/68; HOIL 27/02
- [52] VS . a 257/328; 257/339; 257/342; 257/487; 257/653
- [58] Field of Search 357/23.4, 23.8

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Primary Examiner—J. Carroll

[57] ABSIKACT

A high power MOSFET is disclosed in which two laterdly spaced sources each supply current through respective channels in one surface of a semiconductor chip'which are controlled.by .the-same'gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either- on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantidly reduce the on-resistance of the device without eflecting the breakdown voltage of the device. The breakdown voltage of the device is substantidly increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

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REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

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THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

 \ddotsc

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims 1 to 3 and 5 to 24 is con-5 firmed.

Claim 4 is cancelled.

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REEXAMINATION CERTIFICATE (3706th) REEXAMINATION CERTIFICATE (3706th)
States Patent ₁₉₁ R2 4

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Lidow et al. **M** B2 4,959,099

[54] HIGH POWER MOSFET WITH LOW ON-KESIS1 ANCE ANI) HIGH BREAKDOWN VOLTAGE

[76] Inventors: Alexander Lidow. 4005 Strand Ave.. Manhattan Beach. Calif. 90266; Thomas Herman, 1623 Ilcrrin Dr., Redondo Beach, Calif. 90278

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Related U.S. Application Data

- [60] Continuation of Ser. No. 90,664, Aug. 27, 1987, abandoned, which is a division of Ser. No. 456,813, Jan. 10, 1983, abandoned, which is a division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4376,286, which is a coalinualion of Ser. No. 951.310, Ocl 13.. 1978, abandoned.
- j.Sll InLCL' HOIL29/76
- [52] U.S. Cl. 257/328; 257/339; 257/342;
- 257/487; 257/653

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Primary Examiner—Stanley Miller

[57] **ABSTRACT**

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are contrdled. by'the same. gate.. The'diannels lead firom.the source electrodes to a relatively low resistivity region.and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the oa-resistanoe of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relativdy deep p-type diffusion with a large radius in the n-type cpitaxial layer beneath each of the sources.

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1 **REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307**

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

10 Matter endosed in heavy brackets [] appeared in the pat ent, but has been deleted and is no longer a part of the **paloit; matter printed in italics iidicates additions made 1(1 the patent.**

AS A RESULT OF REEXAMINATION, TT HAS BEEN DETERMINED THAT:

Qaim 4 was previously cancelled.

Claims 1.7, 19 and 24 arc determined to be patentable as **amended.**

20 Ciaims 2. 3. 5. 6. 8-18 and 20-23, dependent on an amended claim, are determined to be patentable.

New claims 25-2X and 29 are added and determined to be l>alcntable.

1. A high power metd oxide silicon field effect transistor 25 device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

- **30 conductor materid having a rdatively lightly doped a wafer of semiconductor materid having first and second opposing semiconductor siufaces; said wafer of semimajor body portion for receiving junctions and being doped with impurities of one conductivity type;**
- *at least first and second spaced base regions of the opposite conductivity type to sdd .one conductivity type formed in said wder and extending from sdd first* **35** *semiconductor surface to a first depth beneath sdd first* semiconductor surface; the space between said at least first and second base regions defining a vertical common conduction region of one conductivity type at a *given flrst semiconductor surfsce location; the concentration of carriers of said one conductivity type in said common conduction region at said first semiconductor surface being tess lhan the concentration of carriers of said opposite conductivity type of saidfirst and second base regions at said first semiconductor surface;* **40 45**
- **first and second source regions of said one conductivity type formed in each pair of sdd at least first and second base regions respectively at first and second first surface location to a depth less than said first depth'; the outer rim of each of sud first and second source regions** being laterally spaced along said first semiconductor surface from the lateral outer periphery of its said base **region to define first and second diannel regions dong** said first semiconductor surface between each pair of said first and second source regions, respectively, and ⁵⁵ said common conduction region; **SO**

source electrode means connected to said source regions; **gate insdation layer means on said first surface, disposed**

- **at least on sdd flrst and second channel regions; gate electrode means on said gate in.sulation layer means** and ovcriying said first and second channel regions; **60**
- a drain conductive region remote from said common region and separated therefrom by said relatively **li^fly doped major body portion;**
- a drain electrode coupled to said drain conductive region; **and**

at least said first base region being a cellular polygonal region; said cellular polygonal region being surrounded **by sdd common conduction region; sdd first source** region having the shape of an annular ring disposed **Within sdd celldar polygond first base region.**

7. A three-termind power metd oxide silicon fidd effect transistor device comprising:

- **a wafer of seim'oonductor materid having first and second** opposing semiconductor surfaces; said wafer of semi**conductor materid having a relativdy lightiy doped** major body portion for receiving junctions and being doped with impurities of one conductivity type;
- *at least first and second spaced ha.% regions of the opposite conductivity type to said one conductivity type formed in sdd wafer and extending from sdd first semiconductor surface to a depth beneath sdd first* semiconductor surface; the space between said at least *first and second base regions defidag a vertical common conduction region of one conductivity type at a given first semiconductor surface location; tite concentration of carriers af said one conductivity type in said common conduction region at saidfirst semiconductor surface being less tium the concentration of carriers of said opposite conductivity type of said first and second base regions at said first semiconductor surface;*
- first and second source regions of said one conductivity **type fonned in each pair of sdd at least first and second** base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of **sdd base regions; sdd first and second source regions** being laterally spaced along said first semconductor surface from the facing respective edges of said com**mon conduction region thereby to define first and •secoid channd regions dong sdd first semiconductor** surface between each pair of said first and second source regions, respectively, and said common conduc**tion region;**
- source electrode means connected to said source regions **and comprising a first termind:**
- **gate insulation layermeans on sdd first surface, disposed** at least on said first and second channel regions;
- gate electrode means on said gate insulation layer means, **overlying sdd first and second channel regions and ooniprising a second termind;**
- a drain conductive region remote from said common region and separated therefrom by said relatively **lightiy dopci major body portion;**
- a drain electrode coupled to said drain conductive region and comprising a third terminal;
- each of said at least first and second spaced base regions **. of sdd opposite conductivity type having respective** profiles which include, to allow the device to withstand **relatively high breakdown voltages, relativdy shallow** depth regions having a relatively small radius of curvature extending from said common region and underlying their said respective first and second source **regions, and respective rdativdy deep, rdativdy large** radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region;
- least said first base region being a cellular polygonal **region; sdd celldar polygond region being surrounded** by said common conduction region; said first source-

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3 4 region having the shape of an annular ring disposed source electrode means connected to said source regions;

within said cellular polygonal first base region; said said said said in ver means on said first surface, dispos relatively shallow depth region of said first base region
surrounding the outer periphery of said relatively deep

19. A high power metal oxide silicon field effect transistor device exhibiting relatively low on-resistance; said device comprising:

a wafer of semiconductor material having first and second
an electrode coupled to said further region. opposing semiconductor surfaces; said wafer of semi- 10 major body portion for receiving junctions and being

opposite conductivity type to said one conductivity ¹⁵ type formed in said wafer and extending from said first **common conduction region at said first senuctmductor source regions.** *said opposite conductivity type of soid firsl and second conduction region is disposed beneatii said gate insulation base regions al said firsl semiconductor surface; layer means on said first surface.*

base regions respectively at first and second first sur- 30 face locations and extending from said first and second *face locations and extending from said first and second* ²⁷ 27. The device of claim 19 wherein said vertical common first surface locations to a depth less than said first conduction region is disposed beneath said gate *depth*; the outer rim. of each of said first and second source regions being laterally spaced along said first *semiconductor surface from the lateral outer periphery of its said base region to define first and second channel regions dong sdd first semiconductor surface between ' tion region is continuous atul uninterrupted* **each pair of sdd first and second source regions,** respectively, and said common conduction region;

gate insulation layer means on said first surface, disposed
at least on said first and second channel regions;

surrounding the outer periphery of said relatively deep gate electrode means on said gate insulation layer means
portion of said first base region. and overlying said first and second channel regions;

- said wafer including a further region of opposite conductivity type adjoining said lightly doped major body portion; and
-

opposing semiconductor surfaces; said wafer of semi- 10

conductor material having a relatively lightly doped

mist and second spaced base regions of said opposite con-

mist and second spaced base regions of said opposite *major body portion for receiving junctions and being* ductivity type have respective profiles which include, to doped with impurities of one conductivity type;
allow the device to withstand polarizate has been high boothe doped with unpurintes of one conductivity type;
at least first and second spaced base regions of the *relatively shallow denth regions having a relatively* voltages, relatively shallow depth regions having a relatively
small radius of curvature extending from said common type formed in said wafer and extending from said first conduction region and underlying their said respective first conductor surface to a first depth beneath said first and second source regions, and respective relativel semiconductor surface to a first depth beneath said first and second source regions, and respective relatively deep,
semiconductor surface; the space between said at least relatively large radius regions extending from sai semiconductor surface; the space between said at least relatively large radius regions extending from said shallow
first and second base regions defining a vertical comfirst and second base regions defining a *vertical* com-
mon conduction region of one conductivity type at ²⁰ respective source regions on the side of said source regions mon conduction region of one conductivity type at ²⁰ respective source regions on the side of said source regions given first semiconductor surface location; *shid* $\frac{1}{2}$ which is away from said common conduction reg given first semiconductor surface location; *the concen*- which is away from said common conduction region; said
tration of carriers of said one conductivity type in said shallow base regions partially underlying their r shallow base regions partially underlying their respective

surface hang less than tiie concentration of carriers cf 25. The device cf claim 1 wherem said vertical common

first .and second source regions of sdd one conductivity . 2d. The device af claim 7 wherein stud vertical common type formed in each pair of said at least first and second conduction region is disposed beneath said gale insulation

first surface locations to a depth less than sdd first conduction repon is disposed beneath said gale insulation

28. The device of claim 1 wherein said common conduc-
tion region is continuous and uninterrupted.

29. The device of claim 7 wherein said common conduc-

United States Patent 119]

Lidow et al.

[54] PLURAL POLYGON SOURCE PATTERN FOR MOSFET

- **[75] Inventors: Alexander Lidow, Manhattan Beach; Thomaa-Hemaa, Redondo Beadi;** Vladimir Rumennik, El Segundo, all **ofCdif.**
- [73] Assignee: International Rectifier Corporation, El Segundo, Calif.
- **[21] AppLNo.: 291,423**
- **[22] Filed: Dec. 23,1988**

Related UJ5. Application Data

- **[63] Continuation of Ser. No. 243,544, Mar. 13, 1981, abandoned, which is a continuation of Ser. No. 38,662, May 14, 1979, abandoned.**
- [51] Int. Cl.⁵ H01L 29/100; H01L 29/780;
- **HOIL 29/060; HOIL 27/100**
- **[52] U.S. CL 357/23.4; 357/20, 357/45**
- [58] Field of Search 357/23 VD, 20, 45, 86, **357/23.4**

[56] References Cited

U.S. PATENT DOCUMENTS

[4S] Date of Patent: Apr. 16, 1991

FOREIGN PATENT DOCUMENTS

Primary Examiner—^Michael C. Wimer Assistant Examiner—Peter Toby Brown

Attomey, Agent, or Firm—Ostrolenk, Faber, Gerb & SofTen

[57] ABSTRACT

A high power MOSFET has a plurality of closdy packed polygond sources spaced from one another on one surface of a semiconductor body. An elongated gate electrode is exposed in the spacing between the polygond sources and cooperates with two channels, one for each adjacent source dectrode, to control conduction from the source electrode through the channel and them to a drain electrode on the opposite surface of the semiconductor body. The conductive region adja**cent the channel and between adjacent sources is rela**tively highly conductive in the section of the channel **adjacent to the surface containing the sources. The polygond shaped soiirce members are preferably hexagond so that the distances between adjacent sources is relatively constant throughout the device. Each polygond region has a relatively deep centrd portion and a shdlow outer shelf portion. The shelf portion generdly** underlies an annular source region. The deep central **portion underlies an duminum conductive electrode and is sufliciently deep that it will not be fully penetrated by aluminum spiking.**

14 Chdms, 3 Drawing Sheets

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No. 243,544, filed Mar. 13, 1981, now abandoned, which was a continuation of application Ser. No.

as contmuation application Ser. No. 232,713, filed Feb. surface of the semiconductor device. 9, 1981, now U.S. Pat. No. 4,376,286, entitled **HIGH** POWER MOSFET WITH LOW ON-RESISTANCE 15 single semiconductor wafer and the individual elements AND HIGH BREAKDOWN VOLTAGE, in the can be separated from one another by scribing or any AND HIGH BREAKDOWN VOLTAGE, in the can be separated from names of Alexander Lidow and Thomas Herman, and other suitable method. names of Alexander Lidow and Thomas Herman, and assigned to the assignee of the present invention.

specifically relates to a novel source pattern for a MOS- **ment away from the remainder of the water.**
EET device of the type disclosed in above mentioned **EIG-2** is an enlarged detail of the gate pad to **FET device of the type disclosed in above-mentioned FIG. 2 is an enlarged detail of the gate pad to illus-**
If S. Det. No. 4.276.286 wherein a pluselity of polygon. Hertalthe relationship of the gate contact and the sourc U.S. Pat. No. 4,376,286 wherein a plurality of polygon-
al-shaped source elements are disposed over the surface 25 polygons in the region of the gate pad. **d-shaped source dements are disposed over the surface 25 polygons in the region of the gate pad.** of a semiconductor body and are spaced from one an-
other by a closely controlled dimension.

High power MOSFETS having low on-resistance process of the device.

In bigh breakdown voltage are known and are shown FIG. 4 is a cross-sectional view of FIG. 3 taken and high breakdown voltage are known and are shown FIG. 4 is a cross-sectional view of in the above-noted U.S. Pat. No. 4,376,286. In the above 30 across the section line 4–4 in FIG. 3. **in the above-noted U.S. Pat. No. 4,376,286. In the above 30 across the section lme 4—4 in FIG. 3.** application, the source electrodes are spaced, interdigitated source regions spaced from one another by two parallel channel regions covered by a common gate. The device has exceptionally low on-resistance along
with the usual adventages of the MOSEET device over 26 with the usual advantages of the MOSFET device over 35 **DETAILED DESCRIPTIVER**
the binshed device postimidadly by virtue of a relatively. the bi-polar device particularly by virtue of a relatively
high conductivity region disposed between the two The polygonsconfiguration of the source regions of high conductivity region disposed between the two adjacent channels and leading to a common drain elec**adjacent chaimels and leading to a common drain dec- the present invention is best shown in FIGS. 3,4 and 5**

It has been found that an interdigitated structure has 40 a relatively low packing density. Moreover, the interdigitated arrangement disclosed in the above U.S. Pat.
No. 4,376,286 requires relatively complicated masks

very high packing density is available and which can be trode in the most advantageous way. made with relatively simple masks. The device further 50 has relatively low capacitance. Typically, the device has relatively low capacitance. Typically, the device type device. It will be apparent that the invention will may be made through the use of phosphorus implanta-
also apply to P channel devices and to depletion mode tion and D-MOS fabrication techniques but any desired technique can be used.

cordance with the invention, is polygonal in configuration and is preferably hexagonal to ensure a constant **tion and is preferably hexagcmal to ensure a constant shape. Other shapes such as squares could have been** over the surface of the body. An extremely large num-
ber of small hexagonal source elements may be formed 60 In FIGS. 3 and 4, the hexagonal source regions are ber of small hexagonal source elements may be formed 60 in the same surface of the semiconductor body for a **in the same surface of the semiconductor body for a formed in a basic semiconductor body or wafer which** given device. By way of example, 6,600 hexagonal can be an N type wafer 20 of monocrystalline silicon source regions can be formed in a chip area having a which has a thin N-epitaxial region 21 deposited source regions can be formed in a chip area having a which has a thin N-epitaxial region 21 deposited dimension of about 100 by 140 mils to produce an effec-
thereon as best shown in FIG. 4. All junctions are

gate structure is contacted over the surface of the de-PLURAL POLYGON SOURCE PATTERN FOR vice by elongated gate contact fingers which ensure
 MOSFET good contact over the full surface of the device. good contact over the full surface of the device.

Each of the polygond source regions is contacted by This application is a continuation of application Ser. 5 a uniform conductive layer which engages the individency
 C. 243,544, filed Mar. 13, 1981, now abandoned, ual polygonal sources through openings in an insulation which was a continuation of application Ser. No. layer covering the source regions, which openings can 038,662, filed May 14, 1979, now abandoned. be formed by conventional D-MOS photolithographic be formed by conventional D-MOS photolithographic **nisr A-ran A-ran A-ran A region is then**
**nisr A-range A-range Connection region is then
10-provided for the source conductor and a gate pad con-RELATED APPLICATIONS** 10 provided for the source conductor and a gate pad con-
This application is related to application Ser. No. nection region is provided for the elongated gate fingers This application is related to application Ser. No. nection region is provided for the elongated gate fingers 951,310, filed Oct. 13, 1978, now abandoned and refiled and a drain connection region is made to the reverse and a drain connection region is made to the reverse surface of the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS
BACKGROUND OF THE INVENTION. ω BIG 1 is a plan view of a completed algunary or

BACKGROUND OF THE INVENTION 30 FIG. 1 is a plan view of a completed element on a This invention relates to MOSFET devices, and more semiconductor wafer prior to the separation of the ele-This invention relates to MOSFET devices, and more semiconductor wafer prior to the separation of the ele-
specifically relates to a novel source pattern for a MOS- ment away from the remainder of the wafer.

source region during one stage of the manufacturing process of the device.

a polysilicon gate, a source electrode means and drain electrode to the wafer.

which are first described.
Referring first to FIGS. 3 and 4, the device is shown

prior to the application of the gate, source and drain electrodes. The manufacturing process can be of any No. 4,376,286 requires relatively complicated masks desired type. The manufacturing process described in and has a relatively high capacitance.
U.S. Pat. No. 4,376,286, referred to above, which is **U.S. Pat. No. 4,376,286, referred to above, which is 45 incorporated herein by reference, can be used whereby** BRIEF DESCRIPTION OF THE INVENTION To most position techniques and ion implantation The present invention provides a novel high power techniques can be advantageously employed for the **MOSFET** device with low forward resistance where a formation of the junction and placement of the elecformation of the junction and placement of the electrode in the most advantageous way.

also apply to P channel devices and to depletion mode devices.

chnique can be used.

Each of the individual spaced source regions, in ac-55 onal source regions on one surface of the device, where **Each of the space regions on one surface of the device, where these polygonal regions are preferably hexagonal in** used but the hexagonal shape provides better uniformity

thereon as best shown in FIG. 4. All junctions are tive channel width of about 22,000 mils, thus permitting 65 formed in epitaxial region 21. By using suitable masks, a **permitting 65** formed in epitaxial region 21. By using suitable masks, a **permitting** 65 plurality of P **very high current capacity for the device.** plurality of P type base regions such as regions 22 and
The space between the adjacent sources may contain 23 in FIGS. 3 and 4 are formed in one surface of the The space between the adjacent sources may contain 23 in FIGS. 3 and 4 are formed in one surface of the a polysilicon gate or any other gate structure where the **semiconductor wafer region 21**, where these regions are semiconductor wafer region 21, where these regions are

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mension of 100 by 140 mils, approximately 6600 polygo- 5 **51.** Thus, upon application of a suitable control voltage rad regions are formed to produce a total channel width to the polysilicon gate (including finger 41 in FI nal regions are formed to produce a total channel width **of about 22,000 mils. Each of the polygond regions may channels 61 and 62 become conductive to permit major**have a width measured perpendicular to two opposing ity carrier conduction from the source electrode 50 to **sides of the polygon of about 1 mil or less. The regions the drain 51. Note that channels labeled 60 and 61 of are spaced from one another by a distance of about 0.6 10 FIG. 5 are the same annular channel which is formed** mil when measured perpendicularly between the adjacent straight sides of adjacent polygonal regions. the same annular channel formed in the region 23.
The P+ regions 22 and 23 will have a depth d which Each of the sources form parallel conduction paths

The $P+$ regions 22 and 23 will have a depth d which is preferably about 5 microns to produce a high and is preferably about 5 microns to produce a high and where, for example, channels 63 and 64 beneath gate reliable field characteristic. Each of the P regions has an 15 element 42 permit conduction from the source ring 27 reliable field characteristic. Each of the P-regions has an 15 element 42 permit conduction from the source ring 27 outer shelf region shown as shelf regions 24 and 25 for and an N type source strip 70 to the N+ region 28 P regions 22 and 23, respectively, having a depth s of about 1.5 microns. This depth should be as small as **possible to reduce the capacitance of the device.** P type region 71 which encloses the edge of the wafer.
Each of the polygon regions including polygonal 20 The contact 50 of FIG. 5 is preferably an aluminum

Each of the polygon regions including polygonal 20 regions 22 and 23 receive N+ polygonal ring regions 26 and 27, respectively. Shelves 24 and 25 are located beneath regions 26 and 27, respectively. N+ regions 26 **beneath regions 26 and 27, respectively. N+ regions 26 deeper portion of the P type region 22. This is done and 27 cooperate with a relatively conductive N+ since it was found that aluminum used for the electrode region 28 which is the N+ region disposed between 25 adjacent P type polygons to define the various channels** between the source regions and a drain contact which will be later described.

the manner described in U.S. Pat. No. 4,376,286, re- 30 defined by the annular shelves 24 and 25 to be as thin as

ferred to above, and are the subject of that application desired in order to substantially reduce the devic ferred to above, and are the subject of that application desired in and produce a very low forward resistance for the de-
 and produce a very low forward resistance for the device.

surface of the wafer is covered with an oxide layer or 35 combined conventional oxide and nitride layers which combined conventional oxide and nitride layers which regions 80, 81, 82 and 83 which enable the breaking out are produced for the formation of the various junctions. of a plurality of unitary devices each having a dimen-**This layer is shown as the insulation layer 30. The insu- sion of 100 by 140 mils from, the body of the wafer,** lation layer 30 is provided with polygonal shaped open-

ings such as openings 31 and 32 immediately above 40 plurality of columns and rows. By way of example, the ings such as openings 31 and 32 immediately above 40 polygonal regions 22 and 23. Openings 31 and 32 have boundaries overlying the N + type source rings 26 and and may be about 83 mils. The dimension B may contain 27 for the regions 22 and 23, respectively. The oxide 100 rows of polygonal regions and may be about 148 27 for the regions 22 and 23, respectively. The oxide strips 30, which remain after the formation of the polygstrips 30, which remain after the formation of the polyg- mils. Dimension C, which is disposed between a source onal shaped openings, define the gate oxide for the 45 connection pad 90 and a gate connection pad 91, may **onal shaped openings, defme the gate oxide for the 45 connection pad 90 and a gate connection pad 91, may** vice. contain 82 rows of polygonal elements.
Electrodes may then be applied to the device as The source pad 90 is a relatively heav

which includes polysilicon sections 40, 41 and 42 which electrode 50 a
overlie the oxide sections 30. **1998** SO for the source.

overlie the oxide sections 30.
50 A silicon dioxide coating is then deposited atop the **A silicon dioxide coating is then deposited atop the The gate connection pad 91 is electricdly connected 47 in FIG. 5 which insulates the polysilicon control which extend symmetricdly over the outer surface of** electrode and the source electrode which is subse-
quently deposited over the entire upper surface of the 55 electrical connection to the polysilicon gate as will be quently deposited over the entire upper surface of the 55 electrical connection to the polysilic wafer. In FIG. 5 the source electrode is shown as con-
described in connection with FIG. 2. wafer. In FIG. 5 the source electrode is shown as con-
ductive coating 50 which may be of any desired mateductive coating 50 which may be of any desired mate-

rial, such as aluminum. A drain electrode 51 is also tains the P+ (shown as "P" in the drawings) deep diffurial, such as aluminum. A drain electrode 51 is also tains the P+ (shown as "P" in the drawings) deep diffu-
sion ring 71 which may be connected to a field plate 101

The resulting device of FIG. 5 is an N channel type 60 device wherein channel regions are formed between **device wherein channel regions are formed between FIG. 2 shows a portion of the gate pad 91 and the** conductor material which ultimately leads to the drain of contacts to the polysilicon gate in order to reduce the **electrode 51. Thus, a channel region 60 is formed be- R-C delay constant of the device. The polysilicon gate** tween the source ring 26, which is connected to source 65 electrode 50, and the $N+$ region 28 which ultimately electrode 50, and the N+ region 28 which ultimately and the like which extend outwardly and receive exten-
leads to the drain electrode 51. Channel 60 is inverted to sions of the gate pad and the gate pad elements 94 and leads to the drain electrode 51. Channel 60 is inverted to sions of the gate pad and the gate pad elements 94 and N type conductivity upon the application of a suitable 95. The polysilicon gate regions may be left exposed

generdly polygond in configuration and, preferably, control voltage to the gate 40. In a similar manner, are hexagonal. **are channels 61 and 62 are formed between the source re-
A very large number of such polygonal regions are gion 26, which is connected to the conductor 50, and** A very large number of such polygonal regions are gion 26, which is connected to the conductor 50, and formed. For example, in a device having a surface di-
the surrounding N + region 28 which leads to the drain the surrounding $N+$ region 28 which leads to the drain **51**. Thus, upon application of a suitable control voltage

and an N type source strip 70 to the N+ region 28 and then to the drain electrode 51.

It is to be noted that FIGS. 4 and 5 illustrate an end

contact. It will be noted that the contact region for the contact 50 lies entirely over and in alignment with the since it was found that aluminum used for the electrode **50** might spike through very thin regions of the P type material. Thus, one feature of the present invention is to ensure that the contact 50 lies principally over the **will be later described. deeper portions of the P regions such as P regions 22** and 23. This then permits the active channel regions defined by the annular shelves 24 and 25 to be as thin as

vice. FIG. 1 illustrates one completed :.device using the polygonal source pattern of FIG. 5. The completed device shown in FIG. 1 is contained within the scribe of a plurality of unitary devices each having a dimension of 100 by 140 mils from the body of the wafer.

dimension A contains 65 columns of polygonal regions and may be about 83 mils. The dimension B may contain

The source pad 90 is a relatively heavy metal section which is directly connected to the aluminum source **shown in FIG. 5. These include a polysilicon grid which is directly connected to the duminum source**

to a plurality of extending fingers 92, 93, 94 and 95 which extend symmetrically over the outer surface of

sion ring 71 which may be connected to a field plate 101 shown in FIG. 1.

gate fingers 94 and 95. It is desirable to make a plurality **95. The polysilicon gate regions may be left exposed**

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during the formation of the oxide coating 45-46-47 in FIG. 5 and are not coated by the source electrode 50. Note that in FIG. 2 the axis 120 is the axis of symmetry 120 which is that shown in FIG. 1.

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Although the present invention has been described in S connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. I.t is preferred, therefore, that the present invention be limited not by the spedfic disclosure herein, but only by the appended claims. 10

What is claimed is: 1. A high power MOSFET device having more than IOOO pardlel-connected individud FET devices closely packed into a relativdy smdl area comprising:

- **a thin wafer of semiconductor materid having first IS** and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of **an epitaxidly deposited region of a first conductivity type; 20**
- **a plurality of symmetricdly disposed laterally distributed hexagonal base regions each having a second** conductivity type formed in said epitaxially depos**ited region and extending for a given depth beneath** said first planar surface;
- said hexagonal base regions spaced at said first sur**face from surrounding ones by a symmetric hexagonal lattice of semiconductor materid of sdd first conductivity type;**
- **each side of each of said hexagond base regions being 30 pardlel to an adjacent side of another of said hexagond base regions;**
- **a hexagond annular source region of said first conductivity type formed in an outer peripherd region of each of said hexagond base regions and extend- 35 ing downwardly from said first planar surface to a** depth less than the depth of said base regions;
- an outer rim of each of said annular source regions **being radially inwardly spaced from an outer periphery of its respective hexagond base region to 40 form an annular channel between each of sud outer rims of said annular source regions and said symmetric hexagond lattice of semiconductor materid of said first portion of sdd wafer;**
- nar surface and connected to a plurality of said **annular source regions and to interiorly adjacent** surface areas of their said respective hexagonal **base regions;**
- **a drain electrode connected to sdd second planar SO** surface of said wafer;
- **an insdation layer means on said first planar surface** and overlying at least said annular channels; and
- a polysilicon gate electrode atop said insulation layer **means and operable to invert sdd anndar channels. 55 of base regions.**

2. The MOSFET device of claim 1, wherem the' materid of said lattice of sdd first conductivity type has a relatively high impurity concentration region compared to the concentration of the remainder of said first portion of sdd wafer; sdd rdativdy high concentration 60 region having a depth greater than the depth of said source regions and less than the depths of said plurality **of base regions.**

3. A high power MOSFET device having more than 1000 parallel-connected individud FET devices closdy 65 packed into a relatively smdl area comprising:

a thin wafer of semiconductor materid having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which **extends from said first planar'surface consisting of an epitaxially deposited region of a first conductivity type;**

- **a plurdity of symmetricdly disposed laterdly distributed polygond base regions each having a second** conductivity type formed in said lightly doped region and extending for given depth beneath said **first planar semiconductor surface;**
- said polygonal base regions spaced at said first sur**face from surrounding ones by a symmetric polygond lattice of semiconductor materid of sdd first** conductivity type;
- each side of each of said polygonal base regions being parallel to an adjacent side of another of said po**lygonal base regions;**
- a polygonal annular source region of said first con**ductivity type formed in an outer peripherd region of each of said polygond base regions and extending downwardly from said first planar surface to a depth less than the depth of sdd base regions;**
- an outer rim of each of said annular source regions **being radidly inwardly spaced from an outer periphery of its respective polygond base region to** form an annular channel between each of said outer rims of said annular source regions and said sym**metric polygonal lattice of semiconductor materid of said first portion of said wafer;**
- a common source electrode formed on said first pla**nar surface and connected to a plurdity of said annular source regions and to interiorly adjacent** surface areas of their said respective polygonal **base regions;**
- a drain electrode connected to said second planar semiconductor surface of said wafer;
- an insulation layer means on said first planar surface **and overlying at least said annular channels; and**
- a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

4. The MOSFET device of claim 1 or 3, wherein each of sdd base regions occupies a totd lateral area having a diameter less than about 1 mil and are spaced from adjacent base regions by about 0.6 miL

a common source electrode formed on sdd first pla- 43 N type conductivity, "sdd base regions are a P type 5. The device of claim 1 or 3, wherein said 40M, is an conductivity and said source regions are an N type **conductivity.**

> **6. The MOSFET device of claim 3, wherein the materid of said lattice of said first conductivity type has a relatively high impurity concentration region compared to the concentration of the remainder of said first** portion of said wafer; said relatively high concentration **region havmg a depth greater than the depth of said** source regions and less than the depths of said plurality

> 7. A vertical conduction high power MOSFET de**vice exhibiting relatively low on-resistance and relativdy high breakdown voltage; said device comprising:**

- **a wafer of semiconductor materid having planar first** and second opposing semiconductor surfaces; said **wafer of semiconductor materid having a relativdy lightly doped major body portion for receiv**ing junctions and being doped with impurities of a **first conductivity type;**
- **a plurdity of highly packed, equdly spaced symmetrically disposed identicd polygonal base regions of** a second conductivity type formed in said wafer, each extending from said first planar semiconduc-
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tor surface to a first depth beneath said first planar **semiconductor surface; sdd polygond base regions spaced from surrounding ones by a symmetric polygond lattice of semiconductor materid of sdd first conductivity type; the space between adjacent 5 ones of sdd polygcmd base regions defining a common conduction region of sud first conductivity** type extending downwardly from said first planar **semiconductor surface;**

- **a respective polygond annular source region of sud 10 first conductivity type formed within each of sdd polygond base regions and extending downwardly from sdd first planar semiconductor surface to a** depth less than said first depth; each of said polygo**nd annular source regions being laterally spaced 15 dong sdd first planar semiconductor surface from** the facing respective edges of said common con**duction region thereby to define respective copla**nar annular channel regions along said first planar **semiconductor surface between the polygond sides 20 of each of sud polygond annular , source regions and said common conduction region;**
- **a common source electrode means connected to sud polygond annular source regions and their respective base regions; 25**
- gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;
- **gate electrode means on sdd gate insulation layer means and overlying sdd coplanar channel re- 30 gions;**
- **a drain conductive region remote from sud common conduction region and separated therefrom by said relatively lightly doped major body portion and and**
- a drain electrode coupled to said drain conductive **region.**

8. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown 40 voltage; said device comprising:

- **a wafer of semiconductor material having planar first and second .opposing semiconductor surfaces; sud** wafer of semiconductor material having a rela**tively lightly doped major body portion for receiv- 45 ing junctions and being doped with impurities of a first conductivity type;**
- **at least first and second spaced base regions of a sec**ond conductivity type formed in said wafer and **extending downwardly from sud first planar semi- 50 conductor surface to a first depth beneath sud first planar semiconductor surface; the space between sdd at least first and second spaced base regions defining a conunon conduction region of a first conductivity type at a given first planar semicon- 55** ductor surface location; said common conduction region extending downwardly from said first pla**nar semiconductor surface;**
- first and second annular source regions of said first conductivity type formed in said first and second 60 **spaced base regions respectivdy at sud first planar semiconductor surface locations to a depth less**

source regions being laterally spaced along said **first planar semiconductor surface from the facing respective edges of sud common conduction region thereby to defme first and second channel regions dong said first planar semiconductor surface between each pair of sud first and second** annular source regions, respectively, and said common conduction region; each of said first and sec**ond cfaannel regions being coplanar with one another;**

- **a common source electrode means connected to sud** first and second annular source regions and their **respective first and second base regions;**
- **gate-insulation layer means on sud first planar semi**conductor surface, disposed at least on said first and second channel regions;
- **gate dectrode means on said gate insulation layer means and overlying sud first and second channd regions;**
- **a drain conductive region remote from sud common** conduction region and separated therefrom by said **relatively lightly doped major body portion and extending to said second semiconductor surface;**
- a drain electrode coupled to said drain conductive **region; and**
- each of said at least first and second spaced base re**gions having a polygond configuration; each of. said first and second annular source regions having a polygond configuration conforming to that of** their respective base region.

extending to said second semiconductor surface; 35 portion and extends downwardly from said first planar **9. The MOSFET device of claims 7 or 8 wherein said common conduction region is. relatively highly doped, compared to said.relatively .lightly .doped major body semiconductor surface to a depth greater than the depth** of said source regions, whereby resistance to current flow at the boundaries between said channel regions **and sud common conduction region and between said common conduction region and said relatively lightly doped major body portion is reduced without reducing breakdown voltage.**

10. The MOSFET device of claim 9, wherein the depth of said common conduction region is less than said first depth of said base regions.

11. The MOSFET device of claim 1, 3, 35 or 36, wherein each of said base regions has a deepened central region and a shallower outer peripheral region, said **deepened centrd region extending laterdly under only a portion of its associated source region.**

12. The MOSFET device of claim 11, wherein said deepened central region has a depth of approximately 5 **microns and said shallower outer peripherd region has** a depth of greater than approximately 1.5 microns.

13. The device of claim 32, 35 or 36, wherein there are in excess of about 1000 source regions each having **a width of about 1 mil.**

14. the device of claim 7 or 8, wherein sud lightly doped wafer portion is an N type conductivity, said base regions are a P type conductivity and said source **regions are an N type conductivity.**

Exhibit B – Page

US00S0O8725A REEXAMINATION CERTIFICATE (1900th)
I States Patent [19] B1 5,008,725

United States Patent [19]

I.idow et al. [45] Certificate Issued Jan. 12,1993

|.S4] PLURAL POLYGON SOURCE PATTERN FOR MOSFET

[76] Inventors: Alexander Lidow, Manhattan Beach; Thomas Herman, Redondo Beach; Vladimir Rumcnnik, El Segundo, all of Calif.

Itecxamination Request: No. 90/002,478, Oct. 9, 1991

Necxamination Certificate for:

Certificate of Correction issued May 5, 1992.

Related U.S. Application Data

- [63] Continuation of Ser. No. 243.544, Mar. 13, 1981, abandoned, which is • continuation of Ser. No. 38,662, May 14, 1979, abandoned.
- [51] Int. Cl.⁵ :................... H01L 29/10; H01L 29/78;
- HOIL 29/68
:257/335; 257/341 **[53] U.S. a 257/335; 257/341; 257/776**
- [58] Field of Search 357/23.4, 23.8

[56] **References Cited**

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Primary Examiner—J. Carroll

[57] ABSTRACT

A high power MOSFET has a plurality of closely packed polygond sources spaced from one another on one surface of a semiconductor body. An elongated gate electrode is exposed in the spacing between the polygonal sources and cooperates with two channels, one for each adjacent source electrode, to control conduction from the source dectrode through the channel and then to a drain electrode on the opposite surface of the semiconductor body. The conductive region adjacent the channel and between adjacent sources is relatively highly conductive in the section of the channel adjacent to the surface containing the sources. The polygond shaped soiirce members are preferably hexagonsl so that the distances between adjacent sources is relativdy constant throughout the device. Each polygonal region has a relatively deep central portion and a shallow outer shelf portion. The shelf portion generally underlies an annular source region. The deep central portion underlies an duminum conductive electrode and is sufficiently deep that it will not be fully penetrated by duminum spiking.

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IS

Rl'EXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

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1 111: PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets **[]** appeared in the patent, but has been deleted and is no longer a part of the **(•Kiciit; iii»ti»r priated in italics indicates additions made III Ihr ptirnt. 10**

A.S A RHSULT OR REEXAMINATION, IT HAS REEN DETERMINED THAT:

Claims 1, 3, 7 and 8 are determined to be patentable as amended.

Cliiiiiis 2, 4 to 6, and 9 to 14, dependent on an 20 amended claim, are determined to be patentable.

1. A high power MOSFET device having more than 1(100 fwrallel-connected individual FET devices closely packc:d into a relatively small area comprising: 25

- **a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of** an epitaxially deposited region of a first conductiv- 30 **iiy lype;**
- **a plurality of symmetrically disposed laterally distribiiied identical hexagonal base regions each having a second conductivity type formed in said epitaxially de|Kisitcd region and extending for a given depth' 35 licncath said first planar surface;**
- **said liexagonal base regions spaced al said first sur**face from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first 40 conductivity type;

soid laiiice being continuous and uninterrupted;

- **r.ach side ofeach of said hexagonal base regions being parallel to an adjacent side of another of said hexagnnal base regions;**
- a hexagonal annular source region of said first con**ductivity lype formed in an outer peripheral region of C3ch of said, hexagonal base regions and extending, downwardly from said first planar surface to a dcptli less than the depth of said base regions; 45**
- **an outer rim of each of said annular source regions being radially inwardly spaced from an outer pe**riphery of its respective hexagonal base region to form an annular channel between each of said outer **rims of said annular source regions and said sym-55 metric hexagond lattice of semiconductor material of s;iid first portion of said wafer;**
- **a common source electrode fonned on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagond base regions;**
- **x drain electrode connected to said second planar surface of said wafer;**
- an insulation layer means on said first planar surface 65 **and ovcriying at leasl said annular channels; and**
- **;i |)Cily.silicon gate electrode atop said insulation layer iiiraiis and operable lo invert said annular channels.**

3. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closdy packed into a rdativdy small area comprising:

- **a thin wder of semiconductor material having first and second spaced, pardlel planar surfaces; at least a first portion ofthe thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;**
- **a plurality of symmetricdly disposed laterdly distributed identical polygond base regions each having a** second conductivity type formed in said lightly **doped region and extendmg for given depth beneath said first planar semiconductor surface;**
- said polygonal base regions spaced at said first sur**face from surrounding ones.by a symmetric polygonal lattice of semiconductor materid of said first conductivity type;**

said lattice being continuous and uninterrupted;

- each side of each of said polygonal base regions being parallel to an adjacent side of another of said po**lygond base regions;**
- polygonal annular source region of said first con**ductivity type formed in an outer peripheral region** of each of said polygonal base regions and extending downwardly from said first planar surface to a **depth less than Ihe depth of said base regions;**
- **an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between.each of said outer** rims of said annular source regions and said sym**metric polygonal lattice of semiconductor materid of sdd first portion of said wafer;**
- a common source electrode formed on said first pla**nar surface and connected , to a' plurality of said annular source regions and to interiorly adjacent** surface areas of their said respective polygonal **base regions;**
- **a drain electrode connected to said second planar** semiconductor surface of said wafer;
- **an insulation layer means on said firsl planar surface** and overlying at least said annular channels; and
- **a polysilicon gate dectrode-atop said insulation layer means and operable to invert said.annular channels.**

7. A vertical conduction high power MOSFET device exhibiting rdatively low on-resistance and relatively high breakdown voltage; said device comprising:

50 and second opposing semiconductor surfaces; said **a wafer of semiconductor material having planar first wafer of semiconductor material having a relatively** lightly doped major body portion for receiving junc**tions and being doped with impurities of a first conductivity type;**

- **a plurdity of highly packed, equdly spaced symmetricdly disposed identicd polygonal base regions of** a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar **semiconductor surface; sdd polygond base regions** spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said **first conductivity type;**
- **said lattice being continuous and uninterrupted; the** space between adjacent ones of said polygonal base **regions defining a commonconduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;**

Exhibit B – Page 38

Bl 5,008,725

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- **10 nar annular channel regions dong said first planar a respective polygond annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplasemiconductor surface between the polygond sides** of each of said polygonal annular source regions **and said common conduction region;**
- polygonal annular source regions and their respec- 15 **a common source electrode means connected to sdd tive base regions;**
- **gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;**
- **gate electrode means on said gate insulation layer 20 means and overlying said coplanar channel regions;**
- **a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and 25 extending to said second semiconductor surface; and**
- **H drain electrode coupled to said drain conductive region.**

8. A high power MOSFET device exhibiting rela-30 tively low on-resistance and relatively high breakdown voltage; said device comprising:

- **a wafer of semiconductor material having planar first and second opposing, semiconductor surfaces; said wafer of semiconductor, material having a rela-35 tively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;**
- **at least first and second spaced base regions of a second conductivity type formed in said wafer and 40 extending downwardly from said first planar semi**conductor surface to a first depth beneath said first **planar semiconductor surface; the' space between said at least first and second spaced base regions defining a common conduction region of a first 45**

conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first pla**nar semiconductor surface;**

the surface of said common conduction region being continuous and uninterrupted and of said firsl conductivity type;

- **first and second annular source regions of said first** conductivity type formed in said first and second spaced base regions respectively at said first planar **semiconductor surface locations to a depth less than sdd first depth; said fint and second anndar** source regions being laterally spaced along said **first planar semiconductor surface from the facing** respective edges of said common conduction re**gion thereby to define firsl and second channel regions along sdd first planar semiconductor siir**face between each pair of said first and second **. annular source regions, respectively, and said com**mon conduction region; each of said first and sec**ond channel regions being coplanar with one another;**
- **a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;**
- **gate insulation layer means on said first planar semi**conductor surface, disposed at least on said first **and second channel regions;**
- **gate electrode means on sdd :gate insulation layer means.-andi'overlying'said first and second channel regions;**
- ..a drain conductive region remote from said common **conduction-region and separated.therefrom by said rdatively .'lightiy. doped ;major body ponion and** extending to said second semiconductor surface;
- **'.a drain electrode couplcd'to said.drdn. conductive region; and**
- **each of said at least first and second spaced base re**gions having **[a** polygonal configuration] identi**cal polygonal configurations; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region.-**

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Case 2:00-cv-06756-R-CT Document 1 Filed 06/22/00 Page 41 of 76 Page ID #:969

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. 5,008,725

DATED $\ddot{\cdot}$ April 16, 1991

INVENTOR(S) Alexander Lidow et al

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby cofiected as shown below:

On the title page item [57]: .

Abstract line 8, change "them" to — then — . '

Column 6, line 44, change "40M," to — epitaxially

deposited region — .

Column 8, line 46, change "35 or 36" to — 7 or 8 — .

line 55, change "32, 35 or 36" to — 3, 7 or 8

Signed and Sealed this Fifth Day of May, 1992

DOUGLAS B. COMER

Attesting Officer

 ${\bf Exhibit~B}$

Attest:

Acting Commissioner of Pmtas and Thidemarics

United States **Fatent** [19]

Lidow et al.

[S4] PLURAL POLYGON SOURCE PATTERN FOR MOSFET

- [75] Inventors: Alezander Lidow, Manhattan Beach; Thomas Herman, Redondo Beach; Vladimir Rumennik, El Segundo, all of Cdif.
- [73] Assignee: Intemationd Rectifier Corporation, El Segundo, Calif.
- $[•]$ Notice: The portion of the term of this patent subsequent to Apr. 16, 2008 has been disclaimed.
- [21] Appi. No.: 653,017
- [22] Filed: Feb. 8, 1991

Related U.S. Application Data

- [63] Continuation of Ser. No. 291,423. Dec. 23, 1988, Pat No. 3,008,725, which is a continuation of Ser.. No. 243,544, Mar. 13,1981, abandoned, which is a continuation of Ser. No. 38,662, May 14, 1979, abandoned.
- [51] Int. a. ' HOIL 29/78
- [52] U.S. a 357/23.4; 357/23.1;
- [58] Field of Search 357/23.1, 23.4, 23.14, 357/23.14; 357/45 357/45

[56] References Cited

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**i.
Delg** US|B130767A **[11] Patent NBbber: 5,130,767**

[45] Date of Patent: * Jul. 14,1992

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Primary Examiner—Rolf Hille

Assistant Examiner—Steven Loke Attomey, Agent, or Firm—Ostrolenk, Faber, Gerb & **Soffen**

[57] ABSTRACT

A high power MOSFET has a plurality of closely packed polygond sources spaced from one another on one surface of a semiconductor body. An elongated gate electrode is exposed in the spacing between the polygonal sources and cooperates with two channels, one for each adjacent source electrode, to control conduction from the source electrode through the channel and then to a drain electrode on the opposite surface of the semiconductor body. The conductive region adjacent the channel and between adjacent sources is relatively highly conductive in the section of the channel adjacent to the surface containing the sources. The polygond shaped source members are preferably hexagonal so that the distance between adjacent sources is relatively constant throughout the device. Each polygrelatively constant infoughout the device. Each polyg-
onal region has a relatively deep central portion and a onar region nas a relatively usep central portion and a lies an anndar source region. The deep centrd portion underlies an aluminum conductive electrode and is sufficiently deep that it will not be fully penetrated by duminum spiking.

Exhibit $C-Page$ \mathcal{U}

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Case SOP at Ent⁶-R-CT Burument 1 Filed 06/22/00 Page 43 of 765,130,1767 971

Cas. Patent 56-R-CT July 44, 40 and 5,130,767:972

Exhibit C - Page $\frac{43}{3}$

Case 2:00-cv-06756-R-CT Document 1 Filed 06/22/09 of age 45 of **3,130,767**#:973

07/291.423, filed Dec. 23, 1988, now U.S. Pat. No. vice by elongated gate contact fingers which entitled and **0.008.725**, which in turn, is a continuation of applica-
1.008.725, which, in turn, is a continuation of appli **5,008,725, which, in tum. is a continuation of applica- good contact over the full surface of the device,** tion Ser. No. 06/243,544, filed Mar. 13, 1981 (now aban-

951,310, filed Oct. 13, 1978, now abandoned and refiled ¹⁵ **as continuation application Ser. No. 232,713. filed Feb.** and a drain connection region is made to the reverse
a 1981 now IIS Pat No. 4 376 286 entitled HIGH surface of the semiconductor device. 9, 1981, now U.S. Pat. No. 4,376,286, entitled HIGH surface of the semiconductor device.
POWER MOSEET WITH LOW ON RESISTANCE A plurality of such devices can be formed from a AND HIGH BREAKDOWN VOLTAGE, in the single semiconductor water and the individual elements

name of Alexander I idous and Thomas Herman, and 20 can be separated from one another by scribing or any names of Alexander Lidow and Thomas Herman, and ²⁰ can be separated from one another suitable method. assigned to the assignee of the present invention.

specifically relates to a novel source pattern for a MOS- ²⁵ semiconductor water prior to the separation of the separation of the separation of the separation of the de-**FET device of the type disclosed in above-mentioned** " FIG. 2 is an enlarged detail of the gate pad to illus-

FIG. 2 is an enlarged detail of the gate pad to illus-U.S. Pat. No. 4,376,286 wherein a plurality of polygon-
also have a plure of the gate contact and the source al-shaped source elements are disposed over the surface " sale in Felalousinp of the gate contact" **polygons** in the region of the gate pad. of a semiconductor body and are spaced from one an-

of a semiconductor body and are spaced from one an-

30 FIG. 3 is a detailed plan view of a small portion of the

High power MOSFETS having low on-resistance source region during
and high hearldown values are having and are shared and high breakdown voltage are known and are shown and high breakdown voltage are known and are shown FIG. 4 is a cross-sectional view of FIG. 3 taken in the above-noted U.S. Pat. No. 4,376,286. In the above across the section line 4-4 in FIG. 3. application, the source electrodes are spaced, interdigi- 35 FIG. 5 is similar to FIG. 4 and shows the addition of tated source regions spaced from one another by two **a** polysilicon gate, a source electrode means and drain parallel channel regions covered by a common gate. electrode to the wafer. The device has exceptionally low on-resistance along
with the usual advantages of the MOSFET device over
DETAILED DESCRIPTION OF THE with the usual advantages of the MOSFET device over the bi-polar device particularly by virtue of a relatively ₄₀ DRAWINGS high conductivity region disposed between the two
adjacent channels and leading to a common drain elec-
the present invention is best shown in FIGS 3.4 and 5 adjacent channels and leading to a common drain elec-
the present invention is best shown in FIGS. 3, 4 and 5
which are first described

It has been found that an interdigitated structure has **Referring first to FIGS.** 3 and 4, the device is shown a relatively low packing density. Moreover, the inter- 45 prior to the application of the gate, source and drain digitated arrangement disclosed in the above U.S. Pat. electrodes. The manufacturing process can be of any No. 4,376,286 requires relatively complicated masks desired type. The manufacturing process described in

The Present Invention present in a november in the present of the convery high packing density is available and which can be arrode in the most advantageous way. very high packing density is available and which can be trode in the most advantageous way.
made with relatively simple masks. The device further The device is described as an N channel enhancement made with relatively simple masks. The device further has relatively low capacitance. Typically, the device 55 type device. It will be apparent that the invention will may be made through the use of phosphorus implanta-
also apply to P channel devices and to depletion mode tion and D-MOS fabrication techniques but any desired devices.

cordance with the invention, is polygonal in configura- 60 these polygonal regions are preferably hexagonal in tion and is preferably hexagonal to ensure a constant shape. Other shapes such as squares could have been spacing along the major lengths of the sources disposed used but the hexagonal shape provides better uniformity over the surface of the body. An extremely large num-
of spacing between adjacent source region permeters. ber of small hexagonal source elements may be formed **h** FIGS. 3 and 4, the hexagonal source regions are ber of small hexagonal source elements may be formed In TIGS. 3 and 4, the hexagonal source regions are in the same surface of the semiconductor body for a 65 formed in a basic semiconductor body or wafer which in the same surface of the semiconductor body for a 65 formed in a basic semiconductor body or water which
given device. By way of example, 6,600 hexagonal can be an N type wafer 20 of monocrystalline silicon **given device. By way of example, 6,600 hexagonal can be an N type wafer 20 of monocrystdline silicon** dimension of about 100 by 140 mils to produce an effec-

tive channel width of about 22,000 mils, thus permitting very high current capacity for the device.

The space between the adjacent sources may contain **a polysilicon gate or any other gate structure where the** This is a continuation of application Ser. No. 5 gate structure is contacted over the surface of the de-

1/291.423. filed Dec. 23, 1988, now U.S. Pat. No. vice by elongated gate contact fingers which ensure

doned) which, in turn, is a continuation of application a uniform conductive layer which engages the individ-Ser. No. 06/038,662, filed May 14, 1979 (now aban- 10 ual polygonal sources through openings in an insulation doned). We consume the source regions, which openings can layer covering the source regions, which openings can **be formed by conventiond D-MOS photolithographic RELATED APPLICATIONS techniques. A source pad connection region is then** This application is related to application Ser. No. provided for the source conductor and a gate pad con-
 11.310. filed Oct. 13. 1978. now shandoned and refiled. 15 nection region is provided for the elongated gate fing

POWER MOSFET WITH LOW ON-RESISTANCE
A ND HIGH BREAK DOWN VOLTAGE is the single semiconductor wafer and the individual elements

BACKGROUND OF THE INVENTION BRIEF DESCRIPTION OF THE DRAWINGS

This invention relates to MOSFET devices, and more
equipment of a completed element on a powel source pattern for a MOS₂₅ semiconductor wafer prior to the separation of the ele-

other by a closely controlled dimension.
Night agrees MOSEETS having law as graintened as **source** region during one stage of the manufacturing

which are first described.

and has a relatively high capacitance. **We also also we also desired to above**, which is **BRIEF DESCRIPTION OF THE INVENTION** incorporated herein by reference, can be used whereby BRIEF DESCRIPTION OF THE INVENTION **50** D-MOS fabrication techniques and ion implantation
The present invention provides a novel high power techniques can be advantageously employed for the techniques can be advantageously employed for the

technique can be used. the action of FIGS. 3 and 4 has a plurality of polyg-Each of the individual spaced source regions, in ac-

onal source regions on one surface of the device, where

thereon as best shown in FIG. 4. All junctions are

r r \cdot *<i>r r r r r r r r r r i Exhibit e - Page HS*

formed in epitaxial region 21. By using suitable masks, a tween the source ring 2a, which is connected to source ally polygonal in configuration and, preferably, are 5

A very large number of such polygonal regions are formed. For example, in a device having a surface diformed. For example, in a device having a surface di-
mension of 100 by 140 mils, approximately 6600 polygo-
51. Thus, upon application of a suitable control voltage mension of 100 by 140 mils, approximately 6600 polygo-

nal regions are formed to produce a total channel width 10 to the polysilicon gate (including finger 41 in FIG. 5), **of about 22,000 mils. Each of the polygond regions may channels 61 and 62 become conductive to permit major**have a width measured perpendicular to two opposing sides of the polygon of about 1 mil or less. The regions sides of the polygon of about 1 mil or less. The regions the drain 51. Note that channels labeled 60 and 61 of are spaced from one another by a distance of about 0.6 FIG. 5 are the same annular channel which is formed mil when measured perpendicularly between the adja- 15 within the region 22. Similarly, channels 62 and 63 are cent straight sides of adjacent polygonal regions.

the same annular channel formed in the region 23. **. cent strdght sides of adjacent polygond regions. the same aimular chaimel formed in the region 23.**

The P+ regions 22 and 23 will have a depth d which **is preferably about 5 microns to produce a high and where, for example, channels 63 and 64 beneath gate** reliable field characteristic. Each of the P regions has an element 42 permit conduction from the source ring 27
outer shelf region shown as shelf regions 24 and 25 for 20 and an N type source strip 70 to the N+ region 28 outer shelf region shown as shelf regions 24 and 25 for 20 and an N type source strip 70 to P regions 22 and 23, respectively, having a depth s of the N-t- to the drain electrode 51. **P** regions 22 and 23, respectively, having a depth s of . then to the drain electrode 51.

about 1.5 microns. This depth should be as small as . It is to be noted that FIGS. 4 and 5 illustrate an end about 1.5 microns. This depth should be as small as possible to reduce the capacitance of the device. **possible to reduce the capacitance of the device.** P type region 71 which encloses the edge of the wafer.
 P type region 71 which encloses the edge of the wafer.

regions 22 and 23 receive N+ polygonal ring regions 26 25 and 27, respectively. Shelves 24 and 25 are located beneath regions 26 and 27, respectively. $N +$ **regions 26.** and 27 cooperate with a relatively conductive $N+$ since it was found that aluminum used for the electrode region 28 which is the $N+$ region disposed between 50 might spike through very thin regions of the P type adjacent P type polygons to define the various channels 30 material. Thus, one feature of the present invention is to between the source regions and a drain contact which ensure that the contact 50 lies principally over the

ferred to above, and are the subject of that application 35 and produce a very low forward resistance for the de- pacitance.

combined conventional oxide and nitride layers which 40 are produced for the formation of the various junctions. This layer is shown as the insulation layer 30. The insu-

lation layer 30 is provided with polygonal shaped open-

The polygonal regions described are contained in a lation layer 30 is provided with polygonal shaped open-
ing such as openings 31 and 32 immediately above polygonal regions 22 and 23. Openings 31 and 32 have 45 dimension A contains 65 columns of polygonal regions **both**
boundaries overlying the N+ type source rings 26 and and may be about 83 mils. The dimension B may contain **boundaries overlying the N+ type source rings 26 and 27 for the regions 22 and 23, respectively. The oxide** 27 for the regions 22 and 23, respectively. The oxide 100 rows of polygonal regions and may be about 148 strips 30, which remain after the formation of the polyg- mils. Dimension C, which is disposed between a source **onal shaped openings, defme the gate oxide for the connection pad 90 and a gate connection pad 91, may** vice.
Electrodes may then be applied to the device as The source pad 90 is a relatively heavenuate The source pad 90 is a relatively heavenuate.

shown in FIG. 5. These include a polysilicon grid which includes polysilicon sections 40, 41 and 42 which **overlie the oxide sections 30. A silicon dioxide coating is then deposited atop the 55**

polysilicon grid 40 shown as coating sections 45, 46 and 47 in FIG. 5 which insulates the polysilicon control **47 in FIG. 5 which insulates the polysilicon control which extend symmetrically over the outer surface of** wafer. In FIG. 5 the source electrode is shown as con- 60 **ductive coating 50 which may be of any desired mate- Findly the outer circumference of the device con**rial, such as aluminum. A drain electrode **51** is also tains the P+ (shown as "P" in the drawings) deep diffu-

The resulting device of FIG. 5 is an N channel type shown in FIG. 1. device wherein channel regions are formed between 65 FIG. 2 shows a portion of the gate pad 91 and the each of the individual sources and the body of the semi-
gate fingers 94 and 95. It is desirable to make a plurality **each of the individud sources and the body of the semi- gate fingers 94 and 95. It is desirable to make a plurdity conductor materid which ultimately leads to the drain of contacts to the polysilicon gate in order to reduce the**

plurality of P type regions such as regions 22 and 23 in electrode 50, and the N+ region 28 which ultimately **Planetical CO** is inverted to **Planetical CO** is inverted to **FIGS. 3 and 4 are formed in one surface of the semicon- leads to the drain dectrode 51. Channel 60 is invened to duction 21, we conductivity upon the application of a suitable control voltage to the gate 40.** In a similar manner, **hexagonal.** channels 61 and 62 are formed between the source re-
A very large number of such polygonal regions are gion 26, which is connected to the conductor 50, and to the polysilicon gate (including finger 41 in FIG. 5), channels 61 and 62 become conductive to permit major-FIG. 5 are the same annular channel which is formed

The contact 50 of FIG. 5 is preferably an aluminum contact. It will be noted that the contact region for the contact 50 lies entirely over and in alignment with the deeper portion of the P type region 22. This is done **50 might spike through very thin regions of the P type** will be later described.
The highly conductive N+ regions 28 are formed in and 23. This then permits the active channel regions 20
Response 28 are formed in and 23. This then permits the active channel regions The highly conductive N+ regions 28 are formed in and 23. This then permits the active channel regions the manner described in U.S. Pat. No. 4,376,286, re-
defined by the annular shelves 24 and 25 to be as thin as defined by the annular shelves 24 and 25 to be as thin as desired in order to substantially reduce the device ca-

vice.
In FIGS. 3 and 4, it will be noted that the entire polygonal source pattern of FIG. 5. The completed
In FIGS. 3 and 4, it will be noted that the entire polygonal source pattern of FIG. 5. The completed In FIGS. 3 and 4, it will be noted that the entire polygonal source pattern of FIG. 5. The completed surface of the wafer is covered with an oxide layer or device shown in FIG. 1 is contained within the scribe device shown in FIG. 1 is contained within the scribe regions 80, 81, 82 and 83 which enable the breaking out of a plurality of unitary devices each having a dimension of 100 by 140 mils from the body of the wafer.

> plurality of columns and rows. By way of example, the dimension A contains 65 columns of polygonal regions mils. Dimension C, which is disposed between a source

> The source pad 90 is a relatively heavy metal section which is directly connected to the aluminum source electrode 50 and permits convenient lead connection for the source.

The gate connection pad 91 is electrically connected
to a plurality of extending fingers **92**, **93**, **94** and **95 electrode and the source electrode which is subse- the area containing the polygond regions and make** electrical connection to the polysilicon gate as will be described in connection with FIG. 2.

applied to the device. sion ring 71 which may be connected to a field plate 101

R-C delay constant of the device. The polysilicon gate

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has a plurdity of regions includmg regions 110, 111. 112 and the like which extend outwardly and receive exten**sions of the gate pad and the gate pad elements 94 and 95. The polysilicon gate regions may be left exposed** during the formation of the oxide coating 45-46-47 in ⁵ **FIG. 5 and are not coated by the source dectrode 50.** Note that in FIG. 2 the axis 120 is the axis of symmetry 120 which is that shown in FIG. 1.

10 connection with a preferred embodiment thereof, many 15 Although the present invention has been described in variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A high power MOSFET device having more than 1000 pardlel-connected individud FET devices closely packed into a relatively small area comprising;

- **20 and second spaced, pardlel planar surfaces; at least a thin wafer of semiconductor materid having first** a first portion of the thickness of said wafer which extends from said first planar surface consisting of **an epitaxidly deposited region of a first conductivity type;**
- **25 a plurdity of symmetricdly disposed laterdly distributed hexagond base regions each having a second** conductivity type formed in said epitaxially depos**ited region and extending for a given depth beneath sdd first planar surface;**
- **30** said hexagonal base regions spaced at said first sur**face from surroundmg ones by a symmetric hexag**onal lattice of semiconductor material of said first **conductivity type;**
- each side of each of said hexagonal base regions being 35 parallel to an adjacent side of another of said hex**agond base regions;**
- a hexagonal annular source region of said first con**ductivity type formed in an outer peripherd region** of each of said hexagonal base regions and extend- 40 ing downwardly from said first planar surface to a depth less than the depth of said base regions;
- an outer rim of each of said annular source regions **being radidly inwardly spaced from an outer periphery of its respective hexagond base region to 43** form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer:
- a common source electrode formed on said first pla- 50 nar surface and connected to a plurality of said **anndar source regions and to interiorly adjacent** surface areas of their said respective hexagonal **base regions;**
- a drain electrode connected to said second planar 55 surface of said wafer;
- an insulation layer means on said first planar surface and overlying at least said annular channels;
- a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels; 60 **and**
- a gate pad electrode section on the surface of said **device and at least one finger extending from said** gate pad; said at least one finger electrically contacting said polysilicon gate electrode at a plurality 65 mal alignment.
of spaced locations over the surface of said polysili-
5. A vertica

 $\sim 10^{11}$

2. The device of claim 1 wherein said annular chan**nels have at least oat leg in longitudind dignment with** other legs of other of said annular channels; said plural**ity of spaced locations disposed dong a line defined by** said legs of said annular channels which are in longitudi**nd dignment.**

3. A high power MOSFET device having more than 1000 pardlel-connected individud FET devices closdy packed into a relatively smdl area comprising:

- a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which **extends from sdd first planar surface consisting of an epitaxidly deposited region of a first conductivity type;**
- **a plurdity of symmetricdly disposed laterally distributed polygond base regicms each having a second** conductivity type formed in said epitaxially depos**ited region and extending for given depth beneath** said first planar semiconductor surface;
- said polygonal base regions spaced at said first sur**face from surrounding ones by a symmetric polyg**onal lattice of semiconductor material of said first **conductivity type;**
- each side of each of said polygonal base regions being parallel to an adjacent side of another of said po**lygond base regions;**
- a polygonal annular source region of said first con**ductivity type formed in an outer peripherd region** of each of said polygonal base regions and extend**mg downwardly from said first planar surface to a** depth less than the depth of said base regions;
- an outer rim of each of said annular source regions **'being.radidly inwardly ispaced from an outer periphery; of its respective polygond base region to** form an annular channel between each of said outer **. rims of .sdd anndar source regions and sdd sym* numerically in the set of semiconductor material of sdd first portion of sdd wafer;**
- a common source electrode formed on said first planar surface and connected to a plurality of said **annular source regions and to interiorly adjacent** surface areas of their said respective polygonal **base regions;**
- a drain electrode connected to said second planar semiconductor surface of said wafer;
- an insulation layer means on said first planar surface and overlying at least said annular channels;
- **a polysilicon gate dectrode atop sdd insulation layer** means and operable to invert said annular channels; **and**
- a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically con**tactmg sdd polysilicon gate dectrode at a plurality** of spaced locations over the surface of said polysili**con gate electrode, thereby to reduce the R-C** delay constant of said device.

4. The device of claim 3 wherein said annular chan**nels have at least one leg in longitudind dignment with** other legs of other of said annular channels; said plural**ity of spaced locations disposed dong a line defmed by** said legs of said annular channels which are in longitudi-

5. A vertical conduction high power MOSFET decon gate electrode, thereby to reduce the R-C vice exhibiting relatively low on-resistance and rela-
delay constant of said device.
gively high breakdown voltage; said device comprising; tively high breakdown voltage; said device comprising;

- **a wafer of semiconductor materid having planar first** and second opposing semiconductor surface; said **wafer of semiconductor materid having a relatively lightly doped major body ponion for receiving junctions and being doped with impurities of a first conductivity type;**
- each extending from said first planar semiconduc- 10 first conductivity type; the space between adjacent 15 **a plurdity of highly packed, equdly spaced symmetricdly disposed identicd polygond base regions of** a second conductivity type formed in said wafer, tor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions **spaced from surrounding ones by a symmetric po**lygonal lattice of semiconductor material of said **ones of sdd polygond base regions defining a common conduction region of sdd first conductivity** type extending downwardly from said first planar **semiconductor surface;**
- a respective polygonal annular source region of said 20 first conductivity type formed within each of said **polygond base regions and extending downwardly from sdd first planar semiconductor surface to a** depth less than said first depth; each of said polygo**nd annular source regions being laterdly spaced 25 dong sdd first planar semiconductor surface from** the facing respective edges of said common con**duction region thereby to defme respective coplanar annular channel regions dong said first planar semiconductor surface between the polygond sides 30 of each of sdd polygonal annular source regions** and said common conduction region;
- **a common source electrode means connected to sdd** polygonal annular source regions and their respec**tive base regions; 35**
- gate insulation layer means on said first planar semiconductor surface, disposed at least on said copla**nar channel, regions;**
- gate electrode means on said gate insulation layer means and overlying said coplanar channel re- 40 **gions;**
- **a drain conductive region remote from said common** conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface; **4S**
- a drain electrode coupled to said drain conductive **region; and**
- a gate pad electrode section on the surface of said device and at least one finger extending from said **gate pad; sdd at least one finger electricdly con-SO tacting sdd polysilicon gate electrode at a plurality** of spaced locations over the surface of said polysili**con gate electrode, thereby to reduce the R-C** delay constant of said device.

6. The device of claim 5 wherein said annular chan- 55 **nels have at least one leg in longitudind dignment with** other legs of other of said annular channels; said plural**ity of spaced locations disposed dong a line defined by** said legs of said annular channels which are in longitudi**nd dignment.**

7. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; sdd device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said 65 wafer of semiconductor material having a rela**tively lightly doped major body portion for receiv**ing junctions and being doped with impurities of a **first conductivity type;**

- **at least first and second spaced base regions of a sec**ond conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first **planar semiconductor surface; the space between sdd at least fust and second spaced base regions defining a common conduction region of a first conductivity type at a given first planar semicon**ductor surface location; said common conduction region extending downwardly from said first pla**nar semiconductor surface;**
- first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less **than sdd first depth; sdd first and second anndar** source regions being laterally spaced along said **first planar semiconductor surface from the facing** respective edges of said common conduction re**gion thereby to defme first and second channel** regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one an**other;**
- a common source electrode means connected to said **first and second annular source regions and their respective first.and second base .regions;**
- gate insulation layer means on said first planar semiconductor/surface, disposed at least on said first **and second channel regions;**
- gate electrode means on said gate insulation layer means and overlying said first and second channel **regions;**
- a drain conductive region remote from said common conduction region and separated therefrom by said **relatively lightly doped major body portion and** extending to said second semiconductor surface;
- a drain electrode coupled to said drain conductive **region:**
- each of said at least first and second spaced base re**gions havmg a polygond configuration; each of said first and second annular source regions having a polygond configuration conforming to that of their respective base region; and**
- a gate pad electrode section on the surface of said device and at least one finger extending from said gate pad; said at least one finger electrically con**tacting sdd polysilicon gate dectrode at a plurdity** of spaced locations over the surface of said polysili**con gate electrode, thereby to reduce the R-C** delay constant of said device.

8. The device of claim 7 wherein said annular chan-60 nels have at least one leg in longitudind aUgnment with other legs of other of said annular channels; said plural**ity of spaced locations disposed dong a line defmed by** said legs of said annular channels which are in longitudi**nd dignment.**

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United States Fatent [19]

Lidow et al.

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

- [75] Inventors: Alexander Lidow, Manhattan; Thomas Herman, Redondo, both of Cdif.
- [73] Assignee: Intemationd Rectifier Corporation,. Los Angeles, Cdif.
- [21] Appi. No.: 471,818
- [22] Filed: Mar. 3,1983

Related U.S. Application Data

- [60] Division of Ser. No. 232,713, Feb. 9, 1981, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.
- [51] Inta.« HOIL 29/78
- [52] U.S. CL 357/23.4
- [58] Field of Search 357/23 VD, 23 R

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Primary Examiner—Martin H. Edlow

Attomey, Agent, or Firm—Ostrolenk, Faber, Gerb & **Soffen**

[57] ABSTRACT

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A high power MOSFET is disdosed in which two laterdly spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited. on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor materid immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius m the n-type epitaxial layer beneath each of the sources.

10 Claims, 11 Drawing Figures

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[11] Patent Number: **4,642,666**

[45] Date of Patent: Feb. 10,1987 **Case 2:00-cv-06756-R-CT** Document 1 Filed 06/22/00 Page 51 of 76 Page ID #:979
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HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

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This is a division of application Ser. No. 232,713,.filed Feb. 9,1981 which, in tum, is a continuation of application Ser. No. 951,310, filed Oct. 13, 1978, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices and more specifically relates to a novel structure for a MOSFET device which permits it to be used ih high power applications with a relatively high reverse voltage and with IS an exceptiondly low on-resistance. The major advantage of the bipolar transistor over the MOSFET transistor is that the bipolar transistor has a very low on-resist**ance per unit conductive area. The MOSFET transistor** has numerous advantages over the bipolar transistor 20 device to provide the necessary thicker depletion re-**25** including very high switching speed, very high gain and **lack of the secondary breakdown characteristics exhibited by a minority carrier device. However, because the MOSFET transistor has high on-resistance, its use in tb high power switching applications has been limited. -**

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power **MOSFET device which has a low forward resistance so** that the device becomes more competitive with bipolar 30 devices in a switching type application while retaining **all of the numerous advantages of the MOSFET over the bipolar device. In particular, with the present invention, the forward resistance per imit area of the device has been reduced by at least a factor of two, compared 35** to the limiting resistance per unit area previously exist**ing in a MOSFET-type device.**

In one embodiment of the invention, two sources are **placed on the same surface of a semiconductor wafer and are laterdly spaced from one another. A gate dectrode, deposited on a conventiond gate oxide, is disposed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced** from one another by an n-type bulk region. Current **from each source can flow through its respective chan- 45 BRIEF DESCRIPTION OF THE DRAWINGS nel (after the creation of the inversion layer defining the channel), so that majority carrier conduction current can flow through the bulk region and across the wafer or chip to the drain dectrode. The drdn dectrode.may** be on the opposite surface of the wafer or on a laterally 50 sources and the gate.

displaced surface region from the source electrodes. FIG. 2 is a cross-This configuration is made using the desirable manufac-

turing techniques of the D-MOS device, which permits FIG. 3 is a cross-sectional view similar to FIG. 2 turing techniques of the D-MOS device, which permits precise alignment of the various electrodes and channels and permits use of extremely small channel lengths. 55 **While the above configuration may have been previously described for a MOSFET signd-type device, the** structure is not that of the commonly used signal MOS-**FET.**

The device is basically formed in an $n(-)$ substrate 60 which has the relatively high resistivity which is necessary to obtain the desired reverse voltage capability of the device. For example, for a 400 volt device, the $n(-)$ **region will have a resistivity of about 20 ohm-centimeters. However, this same necessary high resistivity diar- 65 acteristic has caused the on-resistance of the MOSFET device, when used as a power switeh, to be relativdy high.**

In accordance with the present invention, it has been found that in the upper portion of the central bulk region to which the two inversion layers feed current in the path to the drain electrode, the central region imme**diately beneath the gate oxide can be a relatively low** resistivity material formed, for example, by an $n(+)$ **diffusion in that channel region, without effecting the reverse voltage characteristics of the device.**

10 tion, this common channel will have an upper portion **More specifically, and in accordance with the invenbeneath the gate oxide and a lower bulk portion extend**ing toward the drain electrode. The lower portion has **the high resistivity desired to produce high reverse voltage ability, and will have a depth dependent on the desired reverse voltage for the device. Thus, for a 400 volt device, the lower n(—) region may have a depth of about 35 microns, while for a 90 volt device it will have a depth of about 8 microns. Other depths will be selected, depending on the desired reverse voltage of the** gion required to prevent punch-through during reverse **voltage conditions. The upper portion of the common** channel is made highly conductive $(n+1)$ to a depth of **from about 3 to about 6 microns. It has been found that this does not interfere with the reverse voltage withstand ability of the device. However, it decreases the** on-resistance per unit area of the device by more than a factor of two. The resulting device becomes competi**tive with conventiond high power bipolar switching devices since it retains dl of the advantages of the MOSFET device over the bipolar device but now has the relatively low forward; resistance which was the** major characterizing advantage of the bipolar device.

. In accordance with > another feature of the present invention, the p-type region which, defines the channel beneath the gate oxide has:a rdatively deeply.diffused portion-beneath the source so; that: the p-type diffusion **region.will have a large radius of curvature in the n(—)** epitaxial layer forming the body of the device. This **deeper diffusion or deeper junction has been found to unprove the voltage gradient at the edge of the device** and thus permits the use of the device with higher re**verse voltages.**

FIG. 1 is a plan view of a high power MOSFET chip which incorporates the present invention and particularly illustrates the metalizing pattems of the two

FIG. 2 is a cross-sectional view of FIG. 1 taken across the section line 2--2 in FIG. 1.

showing the initial step in the process of manufacture of the chip of FIGS. 1 and 2 and particularly shows the $p(+)$ conductivity implant and diffusion step.

FIG. 4 shows the second step in the manufacturing process and shows the $n(+)$ implant and diffusion step.

FIG. 5 shows a further step in the process of manufacture of the chip of FIGS. 1 and 2 and shows the channel implant and diffusion step.

FIG. 6 shows a.further step m the process of manufacture and illustrates the source predeposition and diffusion step. This precedes the last step in which the gate oxide is cut for the metalization step which pro**duces the device of FIG. 2.**

FIG. 7 is a plan view of the metdizing pattem of a second embodiment of the invention.

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3 3 FIG. 8 is a cross-sectional view of FIG. 7 taken FIG. 8 is a cross-sectional view of FIG. 7 taken 20 would be about 10 microns thick and would have a across the section line 8-8 in FIG. 7. resistivity of about 2.5 ohm-centimeters. A channel

fied source contact configuration. The shows a model of the shows a model of 50 centers is also used current carrying capacity for the device.

teristics of a device like that of FIG. 2 where the region an elongated serpentine $p(+)$ conductivity region be-

the present invention is shown in FIGS. 1 and 2 which 15 show a chip of monocrystalline silicon 20 (or some other suitable material), with the device electrodes fol-
lowing the serpentine path 21 best shown in FIG. 1 in By using D-MOS fabrication techniques, two $n(+)$ lowing the serpentine path 21 best shown in FIG. 1 in order to increase the current-carrying area of the device. Other geometries could be used. The device illus- 20 trated has a reverse voltage of about 400 volts and an gions 30 and 31, n-type channel regions 34 and 35, reon-resistance less than about 0.4 ohm with a channel spectively. Channel regions 34 and 35 are disposed width of 50 centimeters. Devices having reverse volt-
beneath the gate oxide 25 and can be inverted by the ages of from 90 to 400 volts have been made. The 400 appropriate application of a biasing signd to the gate 24 volt devices have carried pulse currents of 30 amperes. 25 in order to permit conduction from the source 22 and The 90 volt devices have had forward on-resistances of the source 23 through the inversion layers into the cenabout 0.1 ohm with a channel width of 50 centimeters tral region disposed beneath the gate 24 and then to the and have carried pulse currents up to about 100 am- drain electrode 26. Channels 34 and 35 may each have a peres. Higher and lower voltage devices can also be length of about 1 micron.

higher on-resistances than the above. For example, a between $p(+)$ regions 30 and 31) should have a high 400 volt MOSFET comparable to that described below resistivity in order to permit the device to withstand but made with prior art techniques would normally high reverse voltages. However, the relatively high have an on-resistance much greater than about 1.5 35 resistivity $n(+)$ material is also a significant contributohms, as compared to an on-resistance less than about ing factor to'the high forward on-resistance of the de-0.4 ohm in a device made according to this invention. vice. Moreover, the MOSFET switching device of the pres-
ent invention will exhibit all of the desirable advantages ent invention, a significant portion of this central conent invention will exhibit all of the desirable advantages ent invention, a: significant portion of this central con-
of the MOSFET device, since it operates as a majority 40 ducting region is made relatively highly conduc of the MOSFET device, since it operates as a majority 40 ducting region is made relatively highly conductive and carrier device. These advantages include high switch-
consists of an $n(+)$ region 40 disposed immediately ing speed, high gain and avoidance of the secondary beneath the gate oxide 25. The $n(+)$ region 40 has a breakdown characteristics which exist in minority car- depth of about 4 microns and could range from about 3 rier devices. The microns to about 6 microns. While its exact conductiv-

trodes 22 and 23 which are separated by a metalized tive to the $n(-)$ region-beneath it. More particularly, gate electrode 24 which is fixed to but spaced from the region 40 has a high conductivity which would be degate electrode 24 which is fixed to but spaced from the region 40 has a high conductivity which would be desemiconductor device surface by a silicon dioxide layer termined by a total ion implanted dose of from about 25. The serpentine path followed by gate oxide 25 has a 1×10^{12} to. 1×10^{14} phosphorus atoms/cm² at 50 kV length of 50 centimeters and has 667 undulations, but is 50 followed by a diffusion drive at from 1150° length of 50 centimeters and has 667 undulations, but is 50 followed by a diffusion drive at from 1150° C. to 1250° shown more simply in FIG. 1. Other channel widths C. for from 30 minutes to 240 minutes. It has been found can be used. Source electrodes 22 and 23 can be later- that by making this region 40 relatively highly conducally extended as shown to serve as field plates to help tive $n(+)$ material through a diffusion or other operaspread the depletion region created during reverse volt-
tion, the device characteristics are significantly image conditions. Each of source electrodes 22 and 23 55 proved and the forward on-resistance of the device is supply current to a common drain electrode 26 which is reduced by a factor greater than two. Moreover, it has fixed to the bottom of the wafer. The relative dimen- been found that the provision of the high conductivity sions for the device, particularly in thickness, have been region 40 does not mterfere with the reverse voltage grossly exaggerated in FIG. 2 for purposes of clarity. characteristics of the device. Accordingly, by making The silicon chip or wafer 20 is formed on an $n(+)$ sub- 60 the region beneath the gate oxide 25 and between chanstrate which may have a thickness of about 14 mils. An nels . 34 and 35 more highly conductive, the forward $n(-)$ epitaxial layer is deposited on substrate 20 and will on-resistance of the ultimate high power switching dehave a thickness and resistivity depending on the de-
vice has been significantly reduced and the MOSFET sired reverse voltage. All junctions are formed in this device becomes far more competitive with an equivaepitaxial layer which can have a rdatively high resistiv- 65 lent junction-type device while still retaining all of the ity. In the embodiment disclosed, the epitaxial layer has ity. In the embodiment disclosed, the epitaxial layer has advantages of the MOSFET majority carrier operation.
a thickness of about 35 microns and a resistivity of about In the above description of FIGS. 1 and 2, it has be

FIG. $8a$ is a view similar to FIG. 2 and shows a modi-
width of 50 centimeters is also used to provide the de-

FIG. 9 shows the shape of forward-current charac- 5 In a preferred embodiment of the invention, there is 40 beneath the oxide is $n(-)$. The region and region and region and region and region be-FIG. 10 shows the shape of the characteristic of a thus extends around the serpentine path shown in FIG. device identical to that of FIG. 2 where the region 40 1. These $p(+)$ regions are shown in FIG. 2 as the $p(+)$ has high $n(+)$ conductivity. $\qquad \qquad$ 10 regions 30 and 31, respectively, and are similar to those DETAILED DESCRIPTION OF THE
DRAWINGS DEALER THE DRAWINGS DRAWINGS radius of curvature. This allows the device to withstand A first embodiment of the novel MOSFET device of higher reverse voltages. By way of example, the depth e present invention is shown in FIGS. 1 and 2 which 15 of regions 30 and 31 is preferably about 4 microns at the dimension X in FIG. 2 and about 3 microns at the dimension Y in FIG. 2.

regions 32 and 33 are formed beneath source electrodes 22 and 23, respectively, and define, with the $p(+)$ re-

made with varying channel widths. 30 It has previously been thought necessary that the
Presently known MOSFET devices have much central $n(-)$ region between channels 34 and 35 (and Presently known MOSFET devices have much central $n(-)$ region between channels 34 and 35 (and higher on-resistances than the above. For example, a between $p(+)$ regions 30 and 31) should have a high resistivity in. order to permit the device to withstand

consists of an $n(+)$ region 40 disposed immediately The device of FIGS. 1 and 2 has two source elec- 45 ity is not known, and varies with depth, it is high rela-
trodes 22 and 23 which are separated by a metalized tive to the $n(-)$ region-beneath it. More particularly, termined by a total ion implanted dose of from about C. for from 30 minutes to 240 minutes. It has been found

20 ohm-centimeters. For a 90 volt device, epitaxid layer assumed that the conduction channels 34 and 35 are of

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p(-l-) material and are, accordingly, inverted to an n- the oxide surfaces on top of the chip are suitably type conductivity to provide a majority carrier conduc-
tion channel from sources 22 and 23 to the central re-
and 24 are formed to establish electrical contacts to the gion 40 upon the application of an appropriate gate device. The drain contact 26 is applied to the device in voltage. Clearly, however, all of these conductivity 5 a subsequent metalizing operation. Thereafter, the envoltage. Clearly, however, all of these conductivity 5 types could be reversed so that the device could work types could be reversed so that the device could work tire device may be appropriately coated with a suitable as a p-channel device rather than an n-channel device as passivation coating and wire leads are connected to the as a p-channel device rather than an n-channel device as passivation coating and wire leads are connected to the disclosed.
source electrodes 22 and 23 and the gate 24. The device

could be constructed is shown in FIGS. 3 to 6. Refer- 10 with the drain electrode fixed to the housing or other ring to FIG. 3, the base wafer 20 is shown as an $n(+)$ conductive support which serves as a drain connection. material having an n(-) epitaxially deposited region on The device shown in FIGS. 1 and 2 utilizes a serpentiop thereof. A thick oxide layer 50 is formed on wafer time path for each of the source regions and gate regions top thereof. A thick oxide layer 50 is formed on wafer 20 and windows 51 and 52 are opened therein. The open windows 51 and 52 are exposed to a beam of boron 15 source electrodes. Other configurations can be used, atoms in an ion implanting apparatus to form $p(+)$ FIGS. 7 and 8 illustrate a planar configuration which is regions. Thereafter the implanted boron atoms are caused to diffuse deeper into the wafer to form the caused to diffuse deeper into the wafer to form the gate 80 which is disposed between a first source electrounded $p(+)$ concentration region shown in FIG. 3 trode 81 of ring shape and a central source 82. The which might have a depth of about 4 microns. During 20 device as shown in FIG. 8 is contained within a base this diffusion operation, shallow oxide layers 53 and 54 wafer of $p(-)$ monocrystalline silicon 83 which may this diffusion operation, shallow oxide layers 53 and 54 wafer of $p(-)$ monocrystalline silicon 83 which may grow over the windows 51 and 52.
have a buried $n(+)$ region 84 to reduce the lateral resis-

cut in the oxide layer 50 and an $n(+)$ implant takes place to implant the $n(+)$ regions 63 and 64 into the 25 rounds source 81.
 $n(-)$ epitaxial layer. This $n(+)$ implantation can be A ring-shaped $n(+)$ region 86 is formed within the $n(-)$ epitaxial layer. This $n(+)$ implantation can be carried out with a phosphorus beam. Thereafter, the **carried out with a phosphorus beam. Thereafter, the device as shown ih FIG. 8 and, in accordance with the implanted regions are subjected to a diffusion step to present invention, the ring-shaped region 86 is of much** depth of about 3[}] microns with a concentration deter- 30 region 87, which contains all the junctions of the device.
mined by an implantation dose of 1×10^{12} to 1×10^{14} The ring-shaped region 86 extends from th mined by an implantation dose of 1×10^{12} to 1×10^{14} The ring-shaped region 86 extends from the region phosphorus atoms/cm² followed by a drive for 30 min-
beneath the gate oxide 88 and adjoins the ends of the phosphorus atoms/cm² followed by a drive for 30 min- beneath the gate oxide 88 and adjoins the ends of the utes to 4 hours at from 1150° C. to 1250° C. As will be two conducting channels formed between the ringutes to 4 hours at from 1150^{\degree} C. to 1250 \degree C. As will be later seen, regions 63 and 64 produce the novel $n(+)$ region which substantially reduces the on-resistance of 35 the device. **the device.** source 82, respectively.
 the device is source 82, respectively.
 the deviation of the model of the mo

be diffused. Similarly, the resulting device being de-
scribed herein could be manufactured by any desired 40 An n(+) region 95 in FIG. 8 is provided to ensure scribed herein could be manufactured by any desired 40 process as would be apparent to those skilled in the art.

the channel implantation and diffusion step in which the than about 90 microns). The drain contact 85 is sur-
 $p(+)$ regions 71 and 72 are formed through the same rounded by a $p(+)$ isolation diffusion 96 to isolate the windows 61 and 62 that were used for the $n(+)$ implan- 45 device from other devices on the same chip or wafer.

tation for regions 63 and 64. The $p(+)$ regions 71 and 72 In the arrangement of FIG. 8, like that of FIG. 2, tation for regions 63 and 64 . The $p(+)$ regions 71 and 72 are formed by implanting with a boron beam to a dose of about 5×10^{13} to 5×10^{14} atoms/cm² followed by a diffusion drive for 30 to 120 minutes at 1150° C. to 1250°

out for the source predeposition and the diffusion of the highly conductive region 86.

source regions 32 and 33. This is carried out by a con-

In carrying out the above invention, it should be source regions 32 and 33. This is carried out by a con-
ventional and non-critical phosphorus diffusion step where the diffusion proceeds through the windows 61 55 and 62 so that the source regions 32 and 33 are automatiand 62 so that the source regions 32 and 33 are automati-
cally aligned relative to the other preformed regions. a polysilicon material can be used for the conductive cally aligned relative to the other preformed regions. a polysilicon material can be used for the conductive
Thus, the wafer is placed in a furnace and exposed to gate 80 in FIG. 8 or the conductive gate 24 in FIG. 2.

50 minutes at a temperature of from 850[°] C. to 1000[°]. 60 When this step is completed, the basic junction con**figuration required in FIG. 2 is formed with short** $p(+)$ terposed gates and the like.

regions disposed beneath the oxide 50 to serve as the The source electrodes 22 and 23 have been shown as regions disposed beneath the oxide 50 to serve as the conducting channel for the ultimately constructed dethe channels 34 and 35 between $p(+)$ regions 30 and 31. The manufacturing process then continues from the step of FIG. 6 to the device shown in FIG. 2 wherein

and 24 are formed to establish electrical contacts to the **disclosed. source electrodes 22 and 23 and the gate 24. The device One process by which the device of FIGS. 1 and 2 is then mounted within a suitable protective housing,**

ring to FIGS. 3, conductive support which serves as a drain connection.
The device shown in FIGS. 1 and 2 utilizes a serpenand a drain on the surface of the wafer opposite to the **FIGS. 7 and 8 illustrate a planar configuration which is a simple rectangular arrangement having a ring-shaped** trode 81 of ring shape and a central source 82. The ow over the windows 51 and 52. have a buried n(+) region 84 to reduce the lateral resis-
As is next shown in FIG. 4, windows 61 and 62 are tance of the various current paths of the device leading tance of the various current paths of the device leading to the laterally displaced drain electrode 85 which sur-

> higher conductivity than the $n(-)$ epitaxially deposited region 87 which contains all the junctions of the device. shaped $p(+)$ region 89 and the central $p(+)$ region 91 disposed beneath the ring-shaped source 81 and central

It should be noted that the n(+) regions 63 and 64 It will also be noted in FIG. 8 that the outer periph-

could, if desired, be epitaxially deposited and need not erv 90 of the p(+) ring 89 has a large radius to assist th ery 90 of the $p(+)$ ring 89 has a large radius to assist the device in withstanding high reverse voltages.

process as would be apparent to those skilled in the art. good contact to drain electrode 85. Drain electrode 85
The next step in the process is shown in FIG. 5 and is is widely laterally spaced from source 81 (by greate The next step in the process is shown in FIG. 5 and is is widely laterally spaced from source 81 (by greater the channel implantation and diffusion step in which the than about 90 microns). The drain contact 85 is surrounded by a $p(+)$ isolation diffusion 96 to isolate the device from other devices on the same chip or wafer.

current flow from sources 81 and 82 goes through the width of epitaxial region 87, through the region 86. The current then flows laterally outward and then up to the 50 drain contact 85. As in the embodiment of FIG. 2, de-50 drain contact 85. As in the embodiment of FIG. 2, de-
Thereafter, and as shown in FIG. 6, steps are carried vice resistance is greatly reduced by the relatively vice resistance is greatly reduced by the relatively highly conductive region 86.

noted that any type of contact material can be used to make the source and gate contacts. By way of example,

Thus, the water is placed m a fumerous other geometries can be used to make the conductive gate θ . POCl₃ suspended in a carrier gas for from 10 minutes to
50 minutes at a temperature of from 850° C. to 1000°. 60 device of the invention, including a plurality of pairs of straight, parallel source elements with respectively interposed gates and the like.

separate electrodes which can be connected to separate leads. Clearly, the sources 22 and 23 could be directly vice and with an $n(+)$ region filling the area between 65 leads. Clearly, the sources 22 and 23 could be directly the channels 34 and 35 between $p(+)$ regions 30 and 31. connected as shown in FIG. 8a where components similar to those of FIG. 2 have been given similar identi-
fying numerals. In FIG. 8*a*, however, the gate electrode

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is a polysilicon layer 101 (in place of aluminum) deposited atop gate oxide 25. The gate 101 is then covered with oxide layer 102 and a conductive layer 103 connects the two sources 22 and 23 together to form a **single source conductor which is insulated from gate 5 101. Connection is made to the gate at some suitable edge portion of the wafer.**

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FIGS. 9 and 10 show the shape of measured curves which demonstrate the reduction in forward resistance when the region 40 is made highly conductive $(n+)$. In 10 **FIG. 9, the device tested had a region 40 which had the** n(-) resistivity of the epitaxial region. Thus, the forward resistance is characteristically high at different **gate biases as shown in FIC. 9.**

In the device of the invention where region 40 is of IS $n(+)$ conductivity, there is a dramatic decrease in the **on-resistance as shown in FIG. 10 for dl gate voltages before velocity saturation of the electrons occurs.**

Although the present invention has been described in connection with a preferred embodiment thereof, many 20 variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims. **25**

What is claimed is:

1. A three-terminal power metal oxide silicon field **effect transistor device comprising:**

- **a wder of semiconductor materid having first and** second opposing semiconductor surfaces; said tively lightly doped major body portion for receiving junctions and being doped with impurities of **one conductivity type;**
- **at least first and second spaced base regions of the opposite conductivity type to sdd one conductiv- 35 is on said first surface..** ity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least first and second base regions defining a **common conduction region of one conductivity 40 type at a given first semiconductor surface location;**
- **first and second source regions of said one conductiv**ity type formed in each pair of said at least first and **second base regions respectively at first and second 45** first surface locations and extending from said first **and second first surface locations to a depth less** than said depth of said base regions; said first and second source regions being laterally spaced along respective edges of said common conduction region thereby to define first and second channel

regions along said first semiconductor surface between each pair of said first and second source regions, respectively and said common conduction region;

- **source electrode means connected to said source regions and comprising a first terminal;**
- **gate insulation layer means on said first surface, disposed at least on said first and second channel regions;**
- gate electrode means on said gate insulation layer **means, overlying said first and second channel regibns and comprising a second terminal;**
- **a drain conductive region remote from said common region and separated therefrom by said relatively lightiy doped major body portion;**
- a drain electrode coupled to said drain conductive **region and comprising a third terminal;**
- each of said at least first and second spaced base regions of said opposite conductivity type having **respective profiles which include relatively shallow depth regions extending from said common** region and underlying their said respective first **and second source regions, and respective relatively deep, relatively large radius regions extend**ing from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region.

wafer of semiconductor material having a rela- 30 transistor device of claim 1 wherein said device is **2. The high power metd oxide silicon field effect formed by D-MOS manufacturing techniques.**

- **3. The device of cldm 1 wherein.sdd.drain electrode is on sdd second; semiconductor'surface.**
- 4. The device of claim 1 wherein said drain electrode

5. The device of claim 4 wherein said drain conduc**tive region: contacte a second conductivity-type region** which extends from said drain conductive region to said **second surface.**

6. The device of claim 1 wherein said gate insulation layer means is silicon dioxide.

7. The device of claim 1 wherein said one conductiv**ity type is the n-type and wherein said opposite conductivity type is the p-type.**

8. The device of claim 1 wherein said relatively deep regions have a depth of about 4 microns.

9. The device of claim 1 wherein said gate electrode means is formed of polysilicon.

said first semiconductor surface from the facing 50 lightly doped body portion has a resistivity greater than $\frac{1}{2}$ 10. The device of claim 1 wherein said relatively **about 2.5 ohm centimeters.**

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United States Patent $[19]$

Lidow et al. [45] Certificate Issued *Oct. 27, 1998

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

- \'iS] Inventors: Alexander Lidow. Manhattan; Thomas Herman. Redondo. both of Calif.
- |73] Assignee: International Rectifier Corporation
- **Reexamination Requests:**

No. 90/002,818. Aug. 24. 1992 No. 90/003,481. Jun. 29. 1994 No. 90/003.888. Jul. 20. 1995

Krcxamination Certificate for:

[*] Notice: The portion of the term of this patent subsequent to Mar. 8. 2000. has been disclaimed.

Related U.S. Applicalion Data

- 162] Division of Ser. No. 232,713, Feb. 9. 1981, which is a continuation of Ser. No. $951,310,$ Oct. 13, 1978, abandoned.
- I.SIl Int. ei. ' HOIL 29/76
- \S2\ U.S. Cl 257/337; 257/339;.257/341; 257/342
- I5XJ Field of Search 257/337.339. 257/341. 342, 536

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(List continued on next page.)

Primary Examiner—J. Carroll

|57] ABSTRACT

A'high power MOSFET is disclosed in which, two laterally spaced sources each supply current through respective channels in one'surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source dectrodes to a relatively, low resistivity region and from there to a relativdy high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor materid immediately^ adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

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UICEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent. 10

AS A RESULT OF REEXAMINATION. IT HAS BEEN DETERMINED THAT:

Claim 1 is determined to be patentable as amended.

Claims 2, 3, 6, 7, 8, 9, 4, 5 and 10, dependent on an amended claim, are determined to be patentable.

New claims II and 12 are added and detennined to be **20** patentable.

1. A three-terminal power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second **25** opposing semiconductor surfaces; said wafer of semiconductor materid having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one conductivity type;

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the space between said at least 35 first and second base regions defining a vertical common conduction region of one conductivity type at a given first semiconductor surface location; **30**

first and second source regions of said one conductivity type formed in each pair of said at least first and second base regions respectively at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions

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- being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first semiconductor surface between each pair of said first and second source regions, respectively and said common conduction region; the concentration of carriers of said one conductivity type in said common conduction region at said first semiconductor surface being less than the concentration of carriers of said opposite conductivity type of said first and second base regions at said first semiconductor surface;
- source electrode means connected to said source regions and comprising a first termind;
- gate insulation layer means on said first surface, disposed at least on said first and second channel regions;
- gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second tennind;
- a drain conductive region remote from said common region and separated therefrom by said relatively lightly doped major body portion;
- a drain electrode coupled to said drain conductive region and comprising a third terminal;
- each of said at least first and second spaced base regions of said opposite conductivity type having respective profiles which include, to allow the device to withstand relatively high breakdown voltages, relatively shallow depth regions having a relatively small radius of curvature extending from said common region and underlying their said respective first and second source regions, and respective relatively deep, relatively large radius regions extending from said shallow depth regions which are laterally spaced from beneath said respective source regions on the side of said source regions which is away from said common region.

11. The device of claim 1 wherein said vertical common conduction region is disposed beneath said gate insulation 40 layer means on said first surface.

12. The device of claim I wherein said conunon conduction region is contirmous and uninterrupted.

United States Patent [19]

Lidow et al.

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE

- [75] Inventors: Alexander Udow, Manhatta; Thomas Herman, Redondo, both of Calif.
- [73] Assignee: Intemationd Rectifier Corporation, Los Angeles, Calif.
- [21] Appi. No.: 456,813
- [22] Filed: Jan. 10,1983

Related U.S. Application Data

- [60] Division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. $4.376.286$, which is a continuation of Ser. No. 951.310 , Oct: 13, 1978, abandoned.
- [51] Int. Cl.⁴ H01L 21/265; H01L 21/31
- **[52] VS. a 437/29; 357/2(^ 357/23.4; 357/41; 357/52; 357/89; 437/30; 437/41; 437/149; 437/15(h 437/153; 437/913; 437/931; 437/958; 437/984**
- **[58] Fidd of Seardi 29/571, 576 B, 578; 148/1.5,187,190; 357/23 VD, 20,41,52,89,91**

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- **[11] Patent 4,705,759**
- **[45] Date of Patent: NOT. 10,1987**

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Primary Examiner—William G. Saba

Attorney, Agent, or Firm-Ostrolink, Faber, Gerb & Soffen

[57] ABSTRACT

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channds in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source dectrodes to a relativdy low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor materid immediatdy adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by. forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

7 Claims, 11 Drawing Figures

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Case 2:00-cv-06756-R-CT Document 1 Filed 06/22/00 Page 66 of 76 Page ID #:994 **U.S. Patent Nov. 10, 1987** Sheet 3 of 5⁰ 4,705,759

FIG.B.

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POLYSILICON
GATE *2a* 10 102 SOURCE 22 5 12 s 12 F 35 34 $\boldsymbol{\varkappa}$ d **.J ³⁰** DRAIN EIG. 8a ..

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FORWARD VOLTAGE (VOLTS)

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4,705,759

HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN

232,713, filed Feb. 9, 1981, now U.S. Pat. No. 4,376,286, issued Mar. 8, 1983, which, in turn, is a continuation of

device which permits it to be used in high power appli-¹⁵ cations with a relatively high reverse voltage and with cations with a relatively high reverse voltage and with voltage ability, and will have a depth dependent on the an exceptionally low on-resistance. The major advan-
desired reverse voltage for the device. Thus, for a 100 tage of the bipolar transistor over the MOSFET transis-
tor is that the bipolar transistor has a very low on-resist-
about 35 microns, while for a 90 volt device it will have tor is that the bipolar transistor has a very low on-resist-
ance per unit conductive area. The MOSFET transistor ²⁰ a depth of about 8 microns. Other depths will be seance per unit conductive area. The MOSFET transistor ²⁰ has numerous advantages over the bipolar transistor including very high switching speed, very high gain and device to provide the necessary thicker depletion re-
lack of the secondary breakdown characteristics exhib-
gion required to prevent punch-through during reverse ited by a minority carrier device. However, because the voltage conditions. The upper portion of the common MOSFET transistor has high on-resistance, its use in 25 channel is made highly conductive $(n+)$ to a depth of MOSFET transistor has high on-resistance, its use in 25 channel is made highly conductive $(n+)$ to a depth of high power switching applications has been limited. from about 3 to about 6 microns. It has been found that

that the device becomes more competitive with bipolar tive with conventional high power bipolar switching devices in a switching type application while retaining devices since it retains all of the advantages of the devices in a switching type application while retaining devices since it retains all of the advantages of the all of the numerous advantages of the MOSFET over MOSFET device over the bipolar device but now has all of the numerous advantages of the MOSFET over MOSFET device over the bipolar device but now has the bipolar device. In particular, with the present inven- ₂₅ the relatively low forward resistance which was the the bipolar device. In particular, with the present inven- 35 tion, the forward resistance per unit area of the device has been reduced by at least a factor of two, compared In accordance with another feature of the present to the limiting resistance per unit area previously exist-
invention, the p-type region which defines the channel to the limiting resistance per unit area previously existing in a MOSFET type device.

In one embodiment of the invention, two sources are ₄₀ placed on the same surface of a semiconductor wafer placed on the same surface of a semiconductor wafer region will have a large radius of curvature in the n(-) and are laterally spaced from one another. A gate elec-
opitaxial layer forming the body of the device. This trode, deposited on a conventional gate oxide, is dis-
posed between the sources. Two p-type conduction channels are disposed beneath the gate and are spaced ₄₅ and thus permit from one another by an n-type bulk region. Current verse voltages. from one another by an n-type bulk region. Current from each source can flow through its respective chan-
 BRIEF DESCRIPTION OF THE DRAWINGS *nel (after the creation of the inversion layer defining the*
 nel is a plan view of a high power MOSFET chip
 FIG. 1 is a plan view of a high power MOSFET chip channel), so that majority carrier conduction current FIG. 1 is a plan view of a high power MOSFET chip can flow through the bulk region and across the wafer s_0 which incorporates the present invention and particucan flow through the bulk region and across the wafer 50 or chip to the drain electrode. The drain electrode may be on the opposite surface of the wafer or on a laterally sources and the gate.
 be on the source surface region from the source electrodes. FIG. 2 is a cross-sectional view of FIG. 1 taken displaced surface region from the source electrodes. FIG. 2 is a cross-sectional view of This configuration is made using the desirable manufac-
 EXEC 1. This configuration is made using the desirable manufac-
 across t This configuration is made using the desirable manufac-

turing techniques of the D-MOS device, which permits 55 FIG. 3 is a cross-sectional view similar to FIG. 2 turing techniques of the D-MOS device, which permits 55 precise alignment of the various electrodes and chanprecise alignment of the various electrodes and chan-
nels and permits use of extremely small channel lengths. the chip of FIGS. 1 and 2 and particularly shows the While the above configuration may have been previ-
ously described for a MOSFET signal-type device, the structure is not that of the commonly used signal MOS- 60 process and shows the $n(+)$ implant and diffusion step.
 FIG. 5 shows a further step in the process of manu-

which has the relatively high resistivity which is neces-

sary to obtain the desired reverse voltage capability of FIG. 6 shows a further step in the process of manusary to obtain the desired reverse voltage capability of the device. For example, for a 400 volt device, the $n(-)$ 65 facture and illustrates the source predeposition and region will have a resistivity of about 20 ohm centime-
diffusion step. This precedes the last step in whic **region will have a resistivity of about 20 ohm centime- diffusion step. This precedes the last step in which the** acteristic has caused the on-resistance of the MOSFET

1 $\frac{1}{2}$ device, when used as a power switch, to be relatively high.

C AND HIGH BREAKDOWN In accordance with the present invention, it has been **VOLTAGE** found that in the upper portion of the central bulk refound that in the upper portion of the central bulk re-**5 gion to which the two mversion layers feed current m** This application is a division of application Ser. No. the path to the drain electrode, the central region imme-
12,713, filed Feb. 9, 1981, now U.S. Pat. No. 4,376,286, diately beneath the gate oxide can be a relatively l issued Mar. 8, 1983, which, in turn, is a continuation of resistivity material formed, for example, by an $n(+)$ application Ser. No. 951,310, filed Oct. 13, 1978, now diffusion in that channel region, without affecting th application Ser. No. 951,310, filed Oct. 13, 1978, now diffusion in that channel region, without affecting the
¹⁰ reverse voltage characteristics of the device. **abandoned. 10 reverse voltage characteristics of the device.**

HACKGROUND OF THE INVENTION More specifically, and in accordance with the inven-
 EXECURD OF THE INVENTION tion, this common channel will have an upper portion This invention relates to MOSFET devices and more beneath the gate oxide and a lower bulk portion extend-
specifically relates to a novel structure for a MOSFET ing toward the drain electrode. The lower portion has ing toward the drain electrode. The lower portion has the high resistivity desired to produce high reverse desired reverse voltage for the device. Thus, for a 100 volt device, the lower $n(-)$ region may have a depth of lected, depending on the desired reverse voltage of the gion required to prevent punch-through during reverse high power switching applications has been limited. from about 3 to about 6 microns. It has been found that
his does not interfere with the reverse voltage with-BRIEF DESCRIPTION OF THE INVENTION stand ability of the device. However, it decreases the The present invention provides a novel high power ₃₀ on-resistance per unit area of the device by more than a MOSFET device which has a low forward resistance so ³⁰ factor of two. The resulting device becomes competifactor of two. The resulting device becomes competi-
tive with conventional high power bipolar switching

the formulate in formulate resistance of the bipolar device. In accordance with another feature of the present beneath the gate oxide has a relatively deeply diffused portion beneath the source so that the p-type diffusion **and are laterally space on the space one and space decree.** This deeper diffusion or deeper junction has been found to improve the voltage gradient at the edge of the device and thus permits the use-of the device with higher re-

larly illustrates the metalizing patterns of the two sources and the gate.

the chip of FIGS. 1 and 2 and particularly shows the $p(+)$ conductivity implant and diffusion step.

FIG. 4 shows the second step in the manufacturing

ET.
The device is basically formed in an $n(-)$ substrate facture of the chip of FIGS. 1 and 2 and shows the facture of the chip of FIGS. 1 and 2 and shows the channel implant and diffusion step.

gate oxide is cut for the metalization step which pro-
duces the device of FIG. 2.

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FIG. 7 is a plan view of the metalizing pattern of a a thickness of about 35 microns and a resistivity of about second embodiment of the invention. 20 ohm-centimeters. For a 90 volt device, epitaxial layer

FIG. 8a is a view similar to FIG. 2 and shows a modi- 5 width of 50 centimeters is also used to provide the de-
fied source contact configuration.
Solution sired current carrying capacity for the device. Figuration sired current carrying capacity for the device.
FIG. 9 shows the shape of forward-current charac-
In a preferred embodiment of the invention.

FIG. 10 shows the shape of the characteristic of a 10 device identical to that of FIG. 2 where the region 40 device identical to that of FIG. 2 where the region 40 1. These $p(+)$ regions are shown in FIG. 2 as the $p(+)$ has high $n(+)$ conductivity.
regions 30 and 31, respectively, and are similar to those

the present invention is shown in FIGS. 1 and 2 which show a chip of monocrystalline silicon 20 (or some other suitable material), with the device electrodes following the serpentine path 21 best shown in FIG. 1 in 20 By using D-MOS fabrication techniques, two n(+) order to increase the current-carrying area of the de-
order to increase the current-carrying area of the de-
regions order to increase the current-carrying area of the de-
vice. Other geometries could be used. The device illus-
22 and 23, respectively, and define, with the $p(+)$ revice. Other geometries could be used. The device illus-
trated has a reverse voltage of about 400 volts and an gions 30 and 31, n-type channel regions 34 and 35, re**trated has a reverse voltage of about 400 volts and an gions 30 and 31, n-type channel regions 34 and 35, rewidth of 50 centimeters. Devices having reverse volt- 25 beneath the gate oxide 25 and can be inverted by the** ages of from 90 to 400 volts have been made. The 400 appropriate application of a biasing signal to the gate 24 volt devices have carried pulse currents of 30 amperes. in order to permit conduction from the source 22 and The 90 volt devices have had forward on-resistances of the source 23 through the inversion layers into the cenabout 0.1 ohm with a channel width of 50 centimeters tral region disposed beneath the gate 24 and then to the **and have carried pulse currents up to about 100 am- 30 drain dectrode 26. Channels 34 and 35 may each faave a peres. Higher and lower voltage devices can also be length of about I micron.**

Presently known MOSFET devices have much central $n(-)$ region between channels 34 and 35 (and higher on-resistances than the above. For example, a between $p(+)$ regions 30 and 31) should have a high higher on-resistances than the above. For example, a between $p(+)$ regions 30 and 31) should have a high 400 volt MOSFET comparable to that described below 35 resistivity in order to permit the device to withstand 400 volt MOSFET comparable to that described below 35 resistivity in order to permit, the device to withstand but made with prior art techniques would normally high reverse voltages. However, the relatively high but made with prior art techniques would normally high reverse voltages. However, the relatively high have an on-resistance much greater than about 1.5 resistivity $n(-)$ material is also a significant contributhave an on-resistance much greater than about 1.5 resistivity $n(-)$ material is also a significant contribut-
ohms, as compared to an on-resistance less than about ing factor to the high forward on-resistance of the de-0.4 ohm in a device made according to this invention. vice.
Moreover, the MOSFET switching device of the 40 In accordance with the significant feature of the pres-

 \mathcal{O}_2

Moreover, the MOSFET switching device of the 40 present invention will exhibit all of the desirable advantages of the MOSFET device, since it operates as a ducting region is made relatively highly conductive and majority carrier device. These advantages include high consists of an $n(+)$ region 40 disposed immediately majority carrier device. These advantages include high consists of an n(+) region 40 disposed immediately switching speed, high gain and avoidance of the second-
beneath the gate oxide 25. The n(+) region 40 has a **ary breakdown chuacteristics which exist in minority 45 depth of about 4 microns and could range from about 3**

gate electrode 24 which is fixed to but spaced from the semiconductor device surface by a silicon dioxide layer 50 semiconductor device surface by a silicon dioxide layer 50 termined by a total ion implanted dose of from about 25 . The serpentine path followed by gate oxide 25 has a 1×10^{12} to 1×10^{14} phosphorus atoms/cm² length of 50 centimeters and has 667 undulations, but is followed by a diffusion drive at from 1150[°] C. to 1250[°] shown more simply in FIG. 1. Other channel widths C. for from 30 minutes to 240 minutes. It has been found can be used. Source electrodes 22 and 23 can be later- that by making this region 40 relatively highly conducally extended as shown to serve as field plates to help 55 tive n(+) material through a diffusion or other operaspread the depletion region created during reverse volt-
tion, the device characteristics are significantly image conditions. Each of source electrodes 22 and 23 proved and the forward on-resistance of the device is supply current to a common drain electrode 26 which is reduced by a factor greater than two. Moreover, it has fixed to the bottom of the wafer. The relative dimen-
been found that the provision of the high conductivity **sions for the device, particdarly in thickness, faave been 60 region 40 does not interfere with tfae reverse voltage grossly exaggerated m FIG. 2 for purposes of darity. characteristics of the device. Accordingly, by making** The silicon chip or wafer 20 is formed on an n(+) sub-
the region beneath the gate oxide 25 and between chan**strate which may have a thickness of about 14 mils. An nels 34 and 35 more faigfaly conductive, tfae forward** strate which may have a thickness of about 14 mms. And there say and 35 more highly conductive, the forward and t
n(-) epitaxial layer is deposited on substrate 20 and will on-resistance of the ultimate high power switchin **have a thickness and resistivity dependmg on the de- 65 vice has been significantiy reduced and the MOSFET sired reverse voltage. All junctions are formed in this device becomes far more competitive with an equiva**epitaxial layer which can have a relatively high resistiv-

 $\frac{3}{3}$ $\frac{4}{3}$ **second embodiment of the invention.** 20 ohm-centimeters. For a 90 volt device, epitaxial layer FIG. 8 is a cross-sectional view of FIG. 7 taken 20 would be about 10 microns thick and would have a FIG. 8 is a cross-sectional view of FIG. 7 taken 20 would be about 10 microns thick and would have a across the section line 8–8 in FIG. 7.
 resistivity of about 2.5 ohm-centimeters. A channel ross the section line 8—8 in FIG. 7. resistivity of about 2.5 ohm-centimeters. A channel **FIG. 8***a* is a view similar to FIG. 2 and shows a modi- 5 width of 50 centimeters is also used to provide the de-

FIG. 9 shows the shape of forward-current charac- In a preferred embodiment of the invention, there is teristics of a device like that of FIG. 2 where the region an elongated serpentine $p(+)$ conductivity region beteristics of a device like that of FIG. 2 where the region an elongated serpentine $p(+)$ conductivity region be-
40 beneath the oxide is $n(-)$.
40 beneath the oxide is $n(-)$. **heath each of the source electrodes 22 and 23 which thus extends around the serpentine path shown in FIG. has regions 30 and 31, respectively, and are similar to those of the prior art except that the maximum** $p(+)$ **region** DETAILED DESCRIPTION OF THE of the prior att except that the maximum $p(\pm)$ region depth is greatly exaggerated in order to form a large **15 radius of curvature. This dlows the device to withstand** A first embodiment of the novel MOSFET device of higher reverse voltages. By way of example, the depth c present invention is shown in FIGS. 1 and 2 which of regions 30 and 31 is preferably about 4 microns at the dimension X in FIG. 2 and about 3 microns at the di-
mension Y in FIG. 2.

spectively. Channel regions 34 and 35 are disposed

made with varying channel widths. It has previously been thought necessary that the **Presently known MOSFET** devices have much central $n(-)$ region between channels 34 and 35 (and ing factor to the high forward on-resistance of the device.

ent invention, a significant portion of this central conbeneath the gate oxide 25. The $n(+)$ region 40 has a rrier devices.
The device of FIGS. 1 and 2 has two source elec-
ity is not known, and varies with depth, it is high rela-The device of FIGS. 1 and 2 has two source elec-
ity is not known, and varies with depth, it is high rela-
trodes 22 and 23 which are separated by a metalized tive to the $n(-)$ region beneath it. More particularly, tive to the $n(-)$ region beneath it. More particularly, region 40 has a high conductivity which would be de- 1×10^{12} to 1×10^{14} phosphorus atoms/cm² at 50 KV epitaxial layer which can have a relatively high resistiv-
ity. In the embodiment disclosed, the epitaxial layer has advantages of the MOSFET majority carrier operation.

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In the above description of FIGS. 1 and 2, it has been assumed that the conduction channels 34 and 35 are of p(+) materid and are, accordingly, inverted to an ntype conductivity to provide a majority carrier conduction channel from sources 22 and 23 to the central region 40 upon the application of an appropriate gate **voltage. Clearly, however, dl of these conductivity** types could be reversed so that the device could work **as a p-channel device rather than an n-channel device as** a disclosed. 10 **One process by wfaich the device of FIGS. 1 and 2**

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could be constructed is shown in FIGS: 3 to 6. Referring to FIG. 3, the base wafer 20 is shown as an $n(+)$ material having an $n(-)$ epitaxially deposited region on **top thereof. A thick oxide layer 50 is formed on wafer IS 20 and wmdows 51 and 52 are opened therem. The open** windows 51 and 52 are exposed to a beam of boron **atoms in an ion implanting apparatus to form p(+) regions. Thereafter the implanted boron atoms are FIGS. 7 and 8 illustrate a planar configuration which is caused to diffuse deeper into the wafer to form the 20 a simple rectangular arrangement having a ring-shaped** rounded p(+) concentration region shown in FIG. 3 gate 80 which is disposed between a first source election-
which might have a depth of about 4 microns. During trode 81 of ring shape and a central source 82. The this diffusion operation, shallow oxide layers 53 and 54 grow over the windows 51 and 52.

cut in the oxide layer 50 and an $n(+)$ implant takes tance of the various current paths of the device leading place to implant the $n(+)$ regions 63 and 64 into the to the laterally displaced drain electrode 85 which surplace to implant the $n(+)$ regions 63 and 64 into the to the laterally displace 81, $n(-)$ epitaxial layer. This $n(+)$ implantation can be rounds source 81. $n(-)$ epitaxial layer. This $n(+)$ implantation can be carried out with a phosphorus beam. Thereafter, the implanted regions are subjected to a diffusion step to 30 device as shown in FIG. 8 and, in accordance with the cause the regions 63 and 64 to expand and deepen to a present invention, the ring-shaped region 86 is of much **cause the regions 63 and 64 to expand and deepen to a present invention, the ring-shaped region 86 is of much** mined by an implantation dose of 1×10^{12} to 1×10^{14} phosphorus atoms/cm² followed by a drive for 30 minutes to 4 hours at from 1150[°] C. to 1250[°] C. As will be 35 later seen, regions 63 and 64 produce the novel $n(+)$ **region which substantially reduces the on-resistance of the device.**

It should be noted that the $n(+)$ regions 63 and 64 **could, if desired, be epitaxidly deposited and need not 40** be diffused. Similarly, the resulting device being de**scribed herein could be manufactured by any desired** process as would be apparent to those skilled in the art.
The next step in the process is shown in FIG. 5 and is

the channel implantation and diffusion step in which the 45 is widely laterally spaced from source 81 (by greater $p(+)$ regions 71 and 72 are formed through the same than about 90 microns). The drain contact 85 is surwindows 61 and 62 that were used for the $n(+)$ implan-
tation for regions 63 and 64. The $p(+)$ regions 71 and 72 device from other devices on the same chip or wafer. tation for regions 63 and 64. The $p(+)$ regions 71 and 72 device from other devices on the same chip or wafer. are formed by implanting with a boron beam to a dose In the arrangement of FIG. 8, like that of FIG. 2, are formed by implanting with a boron beam to a dose **.** In the arrangement of FIG. 8, like that of FIG. 2, of about 5×10^{13} to 5×10^{14} atoms/cm² followed by a 50 current flow from sources 81 and 82 goes throu of about 5×10^{13} to 5×10^{14} atoms/cm² followed by a 50 diffusion drive for 30 to 120 minutes at 1150° C. to 1250° **C.**

Thereafter, and as shown in FIG. 6, steps are carried out for the source predeposition and the diffusion of the **source regions 32 and 33. This is carried out by a con**ventional and non-critical phosphorus diffusion step where the diffusion proceeds through the windows 61 **and 62 so that the source regicms 32 and 33 are automati-.** cally aligned relative to the other preformed regions. Thus, the wafer is placed in a furnace and exposed to 60 pocl₃ suspended in a carrier gas for from 10 minutes to 50 minutes at a temperature of from 850[°] C, to 1000[°] C.

When this step is completed, the basic junction con-

figuration required in FIG. 2 is formed with short $p(+)$ straight, parallel source elements with respectively inregions disposed beneath the oxide 50 to serve as the 65 terposed gates and the like.

conducting channel for the ultimately constructed de-

The source electrodes 22 and 23 have been shown as conducting channel for the ultimately constructed device and with an $n(+)$ region filling the area between the channels 34 and 35 and between $p(+)$ regions 30

and 31. The manufacturing process then continues from the step of FIG. 6 to the device shown in FIG. 2 wherein the oxide surfaces on top of the chip are suitably stripped and the metalizing patterns for contacts **22,23 and 24 are formed to establish dectricd contacts to the device. The drain contact 26 is applied to the** device in a subsequent metalizing operation. Thereafter, **the entire device may be appropriately coated with a** suitable passivation coating and wire leads are con**nected to the source dectrodes 22 and 23 and the gate 24. The device is then mounted within a suitable protec**tive housing, with the drain electrode fixed to the housing or other conductive support which serves as a drain connection.

The device shown in FIGS. 1 and 2 utilizes a serpen**tine path for each of the source regions and gate regions** and a drain on the surface of the wafer opposite to the **source dectrodes. Other configurations can be used.** trode 81 of ring shape and a central source 82. The device as shown in FIG. 8 is contained within a base **grow over the wmdows 51 and 52. wafer of p(—) monocrystallme silicon 83 which may** have a buried $n(+)$ region 84 to reduce the lateral resistance of the various current paths of the device leading

> A ring-shaped $n(+)$ region 86 is formed within the **higher conductivity than the n(—.) epitaxially deposited region 87 which contains all the junctions of the device.** The ring-shaped region 86 extends from the region beneath the gate oxide 88 and adjoins the ends of the **two conducting, channels, formed between the ring**shaped $p(+)$ region 89 and the central $p(+)$ region 91 disposed beneath the ring-shaped source 81 and central source 82, respectively.

> **It will also be noted in FIG. 8 that the outer periph**ery 90 of the $p(+)$ ring 89 has a large radius to assist the device in withstanding high reverse voltages.

An $n(+)$ region 95 in FIG. 8 is provided to ensure The next step in the process is shown in FIG. 5 and is good contact to drain electrode 85. Drain electrode 85 the channel implantation and diffusion step in which the 45 is widely laterally spaced from source 81 (by greate than about 90 microns). The drain contact 85 is sur-
rounded by a $p(+)$ isolation diffusion 96 to isolate the

> **width of epitaxid regicm 87, through the region 86. The current then flows laterdly outward and then up to the drain ccmtact 85. As m the embodiment of FIG. 2, de**vice resistance is greatly reduced by the relatively **55 highly ccmductive region 86.**

> In carrying out the above invention, it should be **noted that any type of contact materid can be used to make the source and gate ccmtacts. By way of example,** aluminum could be used for the source electrodes while a polysilicon material can be used for the conductive

> **pate 80 in FIG. 8 or the conductive gate 24 in FIG. 2.** Numerous other geometries can be used to make the straight, parallel source elements with respectively in-

> **separate electrodes which can be connected to separate leads. Clearly, the sources 22 and 23 could be directly**

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connected as shown in FIG. 8a where components similar to those of FIG. 2 have been given similar identifying numerals. In FIG. 8a, however, the gate electrode **is a polysiliccm layer 101 (in place of duminum) deposited atop gate oxide 25. The gate 101 is then covered** with oxide layer 102 and a conductive layer 103 con**nects the two sources 22 and 23 together to fbrm a single source conductor which is msulated from gate** 101. Connection is made to the gate at some suitable edge portion of the wafer. **10**

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FIGS. 9 and 10 show the shape of measured curves which demonstrate the reduction in forward resistance when the region 40 is made highly conductive $(n+)$. In FIG. 9, the device tested had a region 40 which had the **n(—) resistivity of the epitaxid region. Thus, the for-IS** ward resistance is characteristically high at different **gate biases as shown in FIG. 9.**

In the device of the invention where region 40 is of $n(+)$ conductivity, there is a dramatic decrease in the on-resistance as shown in FIG. 10 for all gate voltages 20 are applied through said third and fourth windows, are before velocity saturation of the electrons occurs.

each applied by ion implantation. before velocity saturation of the electrons occurs.
Although the present invention has been described in

Although the present invention has been described in 3. The method of claim 1 wherein said chip has an connection with a preferred embodiment thereof, many epitaxial layer thereon which extends to said upper connection with a preferred embodiment thereof, many epitaxial layer thereon which extends to said upper variations and modifications will now become apparent surface and wherein all of said regions are contained to those skilled in the art. It is preferred, therefore, that 25 **the present inventicm be lunited not by the specific** disclosure herein, but only by the appended claims.

Wfaat is claimed is:

1. The method of manufacture of a high power MOS-FET device which comprises the steps of:

- **(a) forming an insdaticm coating on the upper surface of a flat chip of a mcmocrystalline semiccmductor of one of the ccmductivity types;**
- **(b) opening at least fust and second spaced windows** in said insulation coating which have at least first 35 respective portions thereof which are elongated and parallel to one another:
- **(c) applying impurity carriers of a conductivity type** opposite said one conductivity type to said upper surface which is exposed by said first and second 40 windows and heating said chip to cause said carriers to diffuse into said chip to form first and second respective regions of said opposite conductivity type in said chip which have a first depth;
- **(d) opening at least third and fourth spaced windows 45** in any insulation coating on said upper surface which are coextensive with and adjacent to said **first and second wmdows; said third and fourth windows bemg disposed inwardly of the space between said fost and seccmd windows and bemg SO** laterally removed from atop said first and second **regions respectivdy;**
- (e) applying impurity carriers of said opposite conductivity type to said upper surface which is exposed by said third and fourth windows and heat-55 ing said chip to cause said carriers to diffuse into said chip to form third and fourth respective regions of said opposite conductivity type which are continuous with the adjacent sides of said first and second regions respectively but are shallower than 60 said first and second regions; the opposite edges of parallel portions of said third and fourth regions **being laterdly diffused until they are spaced from one another by a given distance by a common neck** region of said one conductivity type of said chip; 65
- **(0 applymg impurity carriers of sdd one ccmductivity** type to said upper surface which is exposed by said third and fourth windows and heating said chip to

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cause sdd carriers from said one conductivity type to diffuse mto sdd third and fourth regions for only a portion of the depth and width of said third and **fourth regions to defme first and second source** regions; said first and second source regions having **facing edges which are spaced from said common nec^ region, thereby to define first and second** channel regions in said third and fourth regions **respectivdy;**

(g) and forming an insulated gate means atop said upper surface and over said first and second chan**nd regions, and forming source electrode means on** said source regions and drain electrode means on the surface of said chip which is opposite said upper surface.

2. The method of claim 1 wherein said impurity carriers of said opposite conductivity type which are applied through said first and second windows, and said impurity carriers of said opposite conductivity type which

surface and wherein all of said regions are contained within said epitaxial layer.

4. The method of manufacture of a high power MOS-FET device which comprises the steps of:

- (a) forming an insulation coating on the upper surface of a flat chip of a monocrystalline semiconductor **of one of the ccmductivity types;**
- **(b) opening at least first and seccmd spaced windows** in said insulation coating which have at least first respective portions thereof which are elongated and parallel to one another;
- **(c) applyuig .impurity carriers of a conductivity type** opposite said one conductivity type to said upper surface which is exposed by said first and second windows: and heating said chip to cause said carriers to diffuse into said chip to form first and second respective regions of said opposite conductivity **type in sdd chip which have a first depth;**
- **(d) opemng at least third and fourtfa spaced windows** in said insulation coating on said upper surface which are coextensive with and adjacent to said first and second-windows respectively; said third and fourth windows being disposed inwardly of the space between said first and second windows and being laterally removed from atop said first and **seccmd regions respectively;**
- (e) applying impurity carriers of said one conductivity type to said upper surface through said third and fourth windows and heating said chip to cause said impurity carriers of said one conductivity type to diffuse into said chip to form relatively highly **doped regions of said one conductivity type which spread laterally until they join one another in a common neck region beneath said insdation coat**ing which is between said third and fourth win**dows;**
- **(f) applying impurity carriers of sdd opposite con**ductivity type to said upper surface which is exposed by said third and fourth windows and heating said chip to cause said carriers to diffuse into said chip to form third and fourth respective re**gions of sdd opposite conductivity type which are** continuous with the adjacent sides of said first and **second regions respectivdy but are shallower than** said first and second regions; the opposite edges of

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9 **9**
parallel portions of said third and fourth regions 5. The method of claim 4 wherein said impurity carri-

- chip to cause said carriers from said one conductiv-
in true to differentiate and fourth and fourth and **6.** The method of claim 4 wherein said chip has an ity type to diffuse into said third and fourth regions 10 6. The method of claim 4 wherein said chip has an epitaxial layer thereon which extends to said upper third and fourth regions to define first and second within said epitaxial layer. for our ce regions; said first and second source regions **for the method** of claim 1, 2 or 3 wherein, following T. The method of claim 1, 2
having facing edges which are spaced from said 16 the stan of forming soid first are
- the surface of said chip which is opposite said **the surface.** The surface of surface of state state sdd chipse solution is opposite solution of $\frac{1}{25}$.

being laterally diffused until they are spaced from ers of said opposite conductivity type which are applied one another by a given distance by said common through said first and second windows, and said impuneck region of said one conductivity type of said rity carriers of said opposite conductivity type which **neck region of sdd one conductivity type of see applied through said first and second windows, and chip;** (g) applying impurity carriers of said one conductiv-

said impurity carriers of said opposite conductivity type (g) applying mipurity carriers of said one conductive- which are applied through said third and fourth win-
ity type to said upper surface which is exposed by **ity type to state upper surface which is exposed by dows, are each applied to said upper surface by ion**
said third and fourth windows and heating said implanation.

for only a portion of the depth and width of said

surface and wherein all of said regions are contained

third and faurth assigns to define first and second

source regions of said and space reduced 15 the step of forming said first and second regions of said
common neck region, thereby to define first and common neck region, thereby to define first and
second channel regions in said third and fourth one conductivity type, impurity carriers of said
one conductivity type are annied to at least selected second channel regions in said third and fourth one conductivity type are applied to at least selected
regions respectively;
regions of said upper surface to cause impurities of said regions respectively;
(h) and forming an insulated gate means atop said one conductivity type to diffuse into said chip to form and forming an insulated gate means atop said one conductivity type to diffuse into said chip to form
unper surface and over said first and second chan, an aslatively lightly doed regions of said and seconductivity l upper surrace and over said first and second chan- 20 relatively lightly doped regions of said one conductivity
hel regions and forming source electrode means on **the to which are dispeced laterally within acid common** nel regions, and forming source electrode means on type which are disposed laterally within said common

said source regions and drain electrode means on heck region and which extend to said upper surface of neck region and which extend to said upper surface of said chip.

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TILIK TENTILI

REEXAMINATION CERTIFICATE (2474th)

United States Patent [19]

Lidow et al.

Case 2:00-cv-06756-R-C

[54] HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN **VOLTAGE**

- [75] Inventors: Alexander Lidow, Manhatta; Thomas Herman, Redondo, both of Calif.
- [73] Assignee: International Rectifier Corporation, Los Angeles, Calif.

Reexamination Request: No. 90/003,141, Jul. 26, 1993

Reexamination Certificate for:

Related U.S. Application Data

- $[60]$ Division of Ser. No. 232,713, Feb. 9, 1981, Pat. No. 4,376,286, which is a continuation of Ser. No. 951,310, Oct. 13, 1978, abandoned.
- [51] Int. Cl.⁶ H01L 21/265; H01L 21/31
- 257/339; 257/341; 257/342; 257/343; 437/30; 437/41; 437/149; 437/150; 437/153; 437/913; 437/931; 437/958; 437/984
- [58] Field of Search 437/29, 30, 41, 149, 437/150, 153, 913, 931, 958, 984; 257/337, 339, 341, 342, 343

$[56]$

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 $[11]$ B1 4,705,759

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OTHER PUBLICATIONS

Plummer et al., "Monolithic 200-V CMOS Analog Switch," IEEE J. Solid-State Circuits, vol. SC-11, No. 6, Dec. 1976.

Tarui et al., "Diffusion Self-Aligned MOST: A New Approach for High Speed Device," J. of Japan Society of Applied Physics, vol. 39, 1970.

Pocha, "High Voltage Double Diffused MOS Transistors for Integrated Circuits," Stanford Electronics Laboratories Technical Report No. 4956-1, Stanford University, Mar. 1976.

Primary Examiner-William G. Saba

ABSTRACT $[57]$

A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective channels in one surface of a semiconductor chip which are controlled by the same gate. The channels lead from the source electrodes to a relatively low resistivity region and from there to a relatively high resistivity epitaxially formed region which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same side as the source regions. The epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type epitaxial layer beneath each of the sources.

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THE PATENT IS HEREBY AMENDED AS ⁵ **INDICATED BELOW.**

Matter endosed in bcavy brackets [] appeared in the patent, but has been deleted and is no longer a part of the ₁₀ **pttent; matter printed in italics indicates additions made** to the patent.

AS A RESULT OF REEXAMINATION. IT HAS REEN DETERMINED THAT: IS

The patentability of claims 4-6 is confirmed.

Claim 1 is detennined to be patentable a; amended.

Claims 2, 3 and 7, dependent on an amended claim, **are determined to be patentdile. 20**

]. The method of manufacture of a high power MOS-FET device which comprises the steps of:

- *(a) forming an insulaticm existing on the upper surface of a flat chip of a monocrystalline semicxmductor* of one *[of the]* conductivity *[types] type*;
- (b) opening at least first and second spaced windows **in sdd insdation coating which have at least iirst 30** respective portions thereof which are elongated and parallel to one another;
- *(c) applying impurity carrieis of a conductivity type opposite sdd one conductivity type to sdd upper* surface which is exposed by said first and second 35 windows and heating said chip to cause said carri*ers to difluse into sdd chip to form first and second respective regicms of sdd opposite conductivity type in sdd chip whicdi have a first depth and a relatively large radius of curvature to allow the derice 40 to withstand higher reverse voltages;*
- **(d) opening at least third and fourth spaced windows** in any insulation coating on said upper surface which are coextensive with and adjacent to said first and second windows; said third and fourth **windows being disposed inwardly of the spac^e** between said first and second windows and being laterally removed from atop said first and second **regions respectively;**
- (e) applying impurity carriers of said opposite con**ductivity type to said upper surface which is ex**posed by said third and fourth windows and heating said chip to cause said carriers to diffuse into said chip to form third and fourth respective re**gions of said opposite conducdvity type which are** continuous with the adjacent sides of said first and second regions respectively but are shallower and **have a smaller radius of curvature than said first and** second regions; the opposite edges of parallel portions of said third and fourth regions being laterally **diffiised until they are spaced from one another by** a given distance by a common neck region of said **one conductivity type of sdd chip;**
- *(f) applying impurity carriers of sdd one conductivity* type to said upper surface which is exposed by said third and fourth windows and heating said chip to *cause sdd carriers from said one c^ndnctivity type to diffuse into saul third and fourth regions for ody a portion of the depth and width of sdd third and fourth regions to define first and second source regions; said first and second source regions having* facing edges which are spaced from said common neck region, thereby to define first and second *channd regions in sdd third and fourth regions respec^tively; and*
- (g) **[and]** forming an insulated gate means atop said upper surface and over said first and:second chan**nd regions, and forming source electrode means on** said source regions and drain electrode means on the surface of the chip which is opposite said upper surface.

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Case 2:00-cv-06756-R-CT

UNITED STATES PATENT AND TRADEMARK OFFICE **CERTIFICATE OF CORRECTION**

PATENT NO. : 4,959,699 **DATED** : September 25, 1990 INVENTOR(S): Alexander Lidow et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below;

Column 12, line 37, please change "19" to -- 20 --.

Signed and Sealed this

Twenty-fifth Day of May, 1993

Michael K. Tick

. MICHAEL K. KIRK Acting Commissioner of Patents and Trademarks

Attesting Officer

Attest:

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