IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

QUICKCOMPILE IP, LLC,	)
	)
Plaintiff,	)
	) Civil Action No. _____
v.	)
	) **JURY TRIAL DEMANDED**
ALTERA CORPORATION,	)
	)
Defendant.	)
	)

COMPLAINT

For its Complaint, Plaintiff QuickCompile IP, LLC ("QuickCompile"), by and through the undersigned counsel, alleges as follows:

THE PARTIES

1. QuickCompile is a Texas limited liability company with a place of business located at 1400 Preston Road, Suite 479, Plano, Texas 75093.

2. Defendant Altera Corporation is a Delaware corporation with, upon information and belief, a place of business located at 5113 Southwest Parkway, Austin, Texas 78735.

3. Upon information and belief, Defendant has registered with the Texas Secretary of State to conduct business in Texas.

JURISDICTION AND VENUE

4. This action arises under the Patent Act, 35 U.S.C. § 1 *et seq.*

5. Subject matter jurisdiction is proper in this Court under 28 U.S.C. §§ 1331 and 1338.

6. Upon information and belief, Defendant conducts substantial business in this forum, directly or through intermediaries, including: (i) at least a portion of the infringements

alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals in this district.

7. Venue is proper in this district pursuant to §§ 1391(b), (c) and 1400(b).

THE PATENTS-IN-SUIT

8. On July 4, 2006, United States Patent No. 7,073,158 (the "'158 patent"), entitled "Automated System For Designing And Developing Field Programmable Gate Arrays" was duly and lawfully issued by the U.S. Patent and Trademark Office. A true and correct copy of the '158 patent is attached hereto as Exhibit A.

9. The claims of the '158 patent provide an inventive concept and do not claim an abstract idea and. The inventive concept of the '158 patent greatly enhances and facilitates the specialized programming of a field-programmable gate array (FPGA), such that source code of high-level programming language designed to process data vectors is mapped onto logic components of an FPGA. The use of high-level programming language to program an FPGA is an improvement over the prior art in that it reduces time and complexity of programming the FPGA.

10. The claims of the '158 patent, moreover, do not merely recite the performance of a longstanding business practice on a computer; rather the claims describe a solution necessarily rooted in computer technology to solve a problem specifically arising in the realm of programming FPGAs. The patent specification, for example, explains how the adoption of FPGAs was slowed by the difficulty in translating desired user-defined algorithms into hardware and the difficulty of updating those algorithms once they are in hardware. The '158 patent overcame these difficulties by simplifying the development of an algorithm or other sequence of

desired operations into the bitstream coding required to program FPGAs.

11. The dependent claims of the '158 patent add additional limitations demonstrating that they also contain inventive concepts, are not directed to any abstract ideas, and do no preempt all ways of programming FPGAs. Claims 4-5 and 7-8, for example, contain specific limitations relating to determining the relative timing between vector processing and identifying the orders and dependencies of vector operands.

12. On September 8, 2009, United States Patent No. 7,587,699 (the "'699 patent"), entitled "Automated System For Designing And Developing Field Programmable Gate Arrays" was duly and lawfully issued by the U.S. Patent and Trademark Office. A true and correct copy of the '699 patent is attached hereto as Exhibit B.

13. The claims of the '699 patent provide an inventive concept and do not claim an abstract idea and. The inventive concept of the '699 patent greatly enhances and facilitates the specialized programming of a FPGA, such that source code of high-level programming language designed to process data vectors is mapped onto logic components of an FPGA. The use of high-level programming language to program an FPGA is an improvement over the prior art in that it reduces time and complexity of programming the FPGA.

14. The claims of the '699 patent, moreover, do not merely recite a computer performing a longstanding business practice; rather the claims describe a solution necessarily rooted in computer technology to solve a problem specifically arising in the realm of programming FPGAs. The patent specification, for example, explains how the adoption of FPGAs was slowed by the difficulty in translating desired user-defined algorithms into hardware and the difficulty of updating those algorithms once they are in hardware. The '699 patent overcame these difficulties by simplifying the development of an algorithm or other sequence of

desired operations into the bitstream coding required to program FPGAs.

15. The dependent claims of the '699 patent add additional limitations demonstrating that they also contain inventive concepts, are not directed to any abstract ideas, and do no preempt all ways of programming FPGAs. Claims 2 and 4-5, for example, contain specific limitations relating to determining the relative timing between vector processing and identifying the orders and dependencies of vector operands.

16. QuickCompile is the assignee and owner of the right, title and interest in and to the '158 and '699 patents, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement of them.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,073,158

17. QuickCompile repeats and realleges the allegations of paragraphs 1 through 16 as if fully set forth herein.

18. Without license or authorization and in violation of 35 U.S.C. § 271(a), Defendant has infringed and continues to infringe at least claims 1, 4-5 and 7-8 of the '158 patent by making, using, importing, offering for sale, and/or selling software for programming field programmable gate arrays ("FPGAs"), including, but not limited to Altera SDK for OpenCL.

19. More specifically and upon information and belief, Altera SDK for OpenCL accepts algorithms specified in source code of high level languages, such as C and C++, *see* https://www.altera.com/en_US/pdfs/literature/wp/wp-01173-opencl.pdf (last accessed May 21, 2015) and it supports processing data vectors. *See* Altera SDK for OpenCL: Best Practices Guide at 1-51 – 1-52 (available at https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/opencl-sdk/aocl_optimization_guide.pdf (last accessed May 21, 2015). The Altera SDK for OpenCL compiler analyzes the input source code and

identifies vector processing operations. *See id.* at 1-50, 1-61. It maps the vector processing operations onto the hardware resources of an FPGA. *See id.* at 1-6. The Altera SDK for OpenCL outputs a hardware design, which is used to program an FPGA with the user's algorithm. *See* https://www.altera.com/products/design-software/embedded-software-developers/opencl/overview.html (last accessed May 21, 2015).

20. QuickCompile is entitled to recover from Defendant the damages sustained by QuickCompile as a result of Defendant's infringement of the '158 patent in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,587,699

21. QuickCompile repeats and realleges the allegations of paragraphs 1 through 20 as if fully set forth herein.

22. Without license or authorization and in violation of 35 U.S.C. § 271(a), Defendant has infringed and continues to infringe at least claims1, 2 and 4-5 of the '699 patent by making, using, importing, offering for sale, and/or selling a system for programming FPGAs, including, but not limited to Altera SDK for OpenCL.

23. More specifically and upon information and belief, Altera SDK for OpenCL accepts algorithms specified in source code of high level languages, such as C and C++, *see* https://www.altera.com/en_US/pdfs/literature/wp/wp-01173-opencl.pdf (last accessed May 21, 2015) and it supports processing data vectors. *See* Altera SDK for OpenCL: Best Practices Guide at 1-51 – 1-52 (available at https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/opencl-sdk/aocl_optimization_guide.pdf (last accessed May 21, 2015). The Altera SDK for OpenCL compiler analyzes the input source code and

identifies vector processing operations. *See id.* at 1-50, 1-61. It maps the vector processing operations onto the hardware resources of an FPGA. *See id.* at 1-6. The Altera SDK for OpenCL outputs a hardware design, which is used to program an FPGA with the user's algorithm. *See* https://www.altera.com/products/design-software/embedded-software-developers/opencl/overview.html (last accessed May 21, 2015).

24. QuickCompile is entitled to recover from Defendant the damages sustained by QuickCompile as a result of Defendant's infringement of the '699 patent in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

QuickCompile hereby demands a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, QuickCompile requests that this Court enter judgment against Defendant as follows:

A. An adjudication that Defendant has infringed the '158 and '699 patents;

B. An award of damages to be paid by Defendant adequate to compensate QuickCompile for Defendant's past infringement of the '158 and '699 patents and any continuing or future infringement through the date such judgment is entered, including interest, costs, expenses and an accounting of all infringing acts including, but not limited to, those acts not presented at trial;

C. A declaration that this case is exceptional under 35 U.S.C. § 285, and an award of QuickCompile's reasonable attorneys' fees; and

D. An award to QuickCompile of such further relief at law or in equity as the Court deems just and proper.

Dated: May 22, 2015

/s/ Andrew W. Spangler

Andrew W. Spangler TX SB #24041960
LOCAL COUNSEL
Spangler Law P.C.
208 N. Green Street, Suite 300
Longview, TX 75601
Telephone: (903) 753-9300
Facsimile: (903) 553-0403
spangler@spanglerlawpc.com

Stamatios Stamoulis DE SB #4606
Richard C. Weinblatt DE SB #5080
LEAD COUNSEL
Stamoulis & Weinblatt LLC
Two Fox Point Centre
6 Denny Road, Suite 307
Wilmington, DE 19809
Telephone: (302) 999-1540
Facsimile: (302) 762-1688
stamoulis@swdelaw.com
weinblatt@swdelaw.com

Attorneys for Plaintiff
QuickCompile IP, LLC