IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ROUND ROCK RESEARCH, LLC, Plaintiff, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA INC., Defendants.	Civil Action No. 14-cv-1491-SLR-SRF **JURY TRIAL DEMANDED**

SECOND AMENDED COMPLAINT

Plaintiff Round Rock Research, LLC ("Round Rock"), for its Second Amended Complaint against Defendants Nintendo Co., Ltd. and Nintendo of America Inc. (collectively, "the Nintendo Defendants"), hereby alleges as follows:

The Parties

1. Plaintiff Round Rock is a Delaware limited liability company with its principal place of business at 2001 Route 46, Waterview Plaza, Suite 310, Parsippany, NJ 07054.

2. Upon information and belief, defendant Nintendo Co., Ltd. ("Nintendo Co.") is a corporation organized and existing under the laws of Japan with its principal place of business at 11-1 Hokotate-cho, Kamitoba, Minami-ku, Kyoto, Japan 601-8501. Nintendo Co. is in the business of researching, designing, developing, manufacturing, and selling video game products including but not limited to consoles, handheld videogame systems, video games, accessories, and components of those products, for importation into the United States and sales in the United States, including in Delaware.

3. Upon information and belief, defendant Nintendo of America Inc. ("Nintendo of America") is a corporation organized under the laws of Washington, having a principal place of business at 4600 150th Avenue NE, in Redmond, Washington 98052. Nintendo of America has appointed The Corporation Trust Company at Corporation Trust Center, 1209 Orange Street in Wilmington, Delaware as its registered agent for service of process in the state of Delaware. Nintendo of America is in the business of importing, marketing, advertising, and selling video game products including consoles, handheld videogame systems, video games, and accessories in the United States, including in Delaware.

4. Nintendo of America is a wholly owned subsidiary of Nintendo Co.

Nature Of The Action

5. This is a civil action for infringement of U.S. Patent Nos. 5,986,347 ("the '347 patent") (attached as Exhibit A), 6,147,405 ("the '405 patent") (attached as Exhibit B), 6,358,801 ("the '801 patent") (attached as Exhibit C), 6,455,935 ("the '935 patent") (attached as Exhibit D), 6,469,336 ("the '336 patent") (attached as Exhibit E), and 6,828,683 ("the '683 patent") (attached as Exhibit F) (collectively, the "Patents-in-Suit") under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq*.

Jurisdiction And Venue

6. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patents laws of the United States, including 35 U.S.C. § 271 *et seq.*

7. This Court has personal jurisdiction over the Nintendo Defendants because, among other things, the Nintendo Defendants have committed, aided, abetted, contributed to,

and/or participated in the commission of patent infringement in violation of 35 U.S.C. § 271 in this judicial district and elsewhere that led to foreseeable harm and injury to Round Rock.

8. This Court also has personal jurisdiction over the Nintendo Defendants because, among other things, the Nintendo Defendants have established minimum contacts within the forum such that the exercise of jurisdiction over the Nintendo Defendants will not offend traditional notions of fair play and substantial justice. For example, the Nintendo Defendants have placed products that practice and/or embody the claimed inventions of the Patents-in-Suit into the stream of commerce with the reasonable expectation and/or knowledge that purchasers and users of such products were located within this district. In addition, the Nintendo Defendants have sold, advertised, marketed, and distributed products in this district that practice the claimed inventions of the Patents-in-Suit. The Nintendo Defendants derive substantial revenue from the sale of infringing products distributed within the district, and/or expect or should reasonably expect their actions to have consequences within the district, and derive substantial revenue from interstate and international commerce.

9. In addition, the Nintendo Defendants knowingly, actively induced and continue to knowingly actively induce infringement of one or more of the Patents-in-Suit within this district by making, using, offering for sale, and selling infringing products, as well as by contracting with others to use, market, sell, and offer to sell infringing products, all with knowledge of the asserted Patents-in-Suit, and their claims, with knowledge that their customers will use, market, sell, and offer to sell infringing products in this district and elsewhere in the United States, and with the knowledge and specific intent to encourage and facilitate infringing sales and use of the products by others within this district and the United States by creating and disseminating

promotional and marketing materials, instructional materials, and product manuals, and technical materials related to the infringing products.

10. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b), because the Nintendo Defendants are subject to personal jurisdiction in this district and have committed acts of infringement in this district.

The Patents-In-Suit

11. United States Patent No. 5,986,347 ("the '347 patent"), titled "Processing Methods Of Forming Contact Openings And Integrated Circuitry," was duly and legally issued by the U.S. Patent and Trademark Office on November 16, 1999. A copy of the '347 patent is attached hereto as Exhibit A. Round Rock is the assignee of all rights, title, and interest in the '347 patent, and it possesses all rights to sue and recover for any current or past infringement of the '347 patent.

12. United States Patent No. 6,147,405 ("the '405 patent"), titled "Asymmetric, Double-Sided Self-Aligned Silicide And Method Of Forming the Same," was duly and legally issued by the U.S. Patent and Trademark Office on November 14, 2000. A copy of the '405 patent is attached hereto as Exhibit B. Round Rock is the assignee of all rights, title, and interest in the '405 patent, and it possesses all rights to sue and recover for any current or past infringement of the '405 patent.

13. United States Patent No. 6,358,801 ("the '801 patent"), titled "Method And Apparatus For Trench Isolation Process With Pad Gate And Trench Edge Spacer Elimination," was duly and legally issued by the U.S. Patent and Trademark Office on March 19, 2002. A copy of the '801 patent is attached hereto as Exhibit C. Round Rock is the assignee of all rights,

title, and interest in the ’801 patent, and it possesses all rights to sue and recover for any current or past infringement of the ’801 patent.

14. United States Patent No. 6,455,935 (“the ’935 patent”), titled “Asymmetric, Double-Sided Self-Aligned Silicide,” was duly and legally issued by the U.S. Patent and Trademark Office on September 24, 2002. A copy of the ’935 patent is attached hereto as Exhibit D. Round Rock is the assignee of all rights, title, and interest in the ’935 patent, and it possesses all rights to sue and recover for any current or past infringement of the ’935 patent.

15. United States Patent No. 6,469,336 (“the ’336 patent”), titled “Structure For Reducing Contact Aspect Ratios,” was duly and legally issued by the U.S. Patent and Trademark Office on October 22, 2002. A copy of the ’336 patent is attached hereto as Exhibit E. Round Rock is the assignee of all rights, title, and interest in the ’336 patent, and it possesses all rights to sue and recover for any current or past infringement of the ’336 patent.

16. United States Patent No. 6,828,683 (“the ’683 patent”), titled “Semiconductor Devices, And Semiconductor Processing Methods,” was duly and legally issued by the U.S. Patent and Trademark Office on December 7, 2004. A copy of the ’683 patent is attached hereto as Exhibit F. Round Rock is the assignee of all rights, title, and interest in the ’683 patent, and it possesses all rights to sue and recover for any current or past infringement of the ’683 patent.

COUNT I

Infringement of U.S. Patent No. 5,986,347

17. Paragraphs 1 through 16 are incorporated by reference as if fully stated herein.

18. The ’347 patent is valid and enforceable.

19. The Nintendo Defendants have infringed, and continue to infringe, one or more claims of the ’347 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of

equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, products encompassed by those claims, including for example, by making, using, selling, offering for sale, and/or importing into the United States all video game products incorporating unlicensed graphical processing units ("GPUs") or any other unlicensed semiconductor component manufactured using a 90nm or later (smaller) process (collectively, the "'347 Infringing Products"). The '347 Infringing Products include, but are not limited to, the Nintendo Wii, the Nintendo Wii U, the Nintendo Wii Mini, and the Nintendo 3DS, consoles, systems, and remotes.

20. The Nintendo Defendants' customers (e.g., distributors, retailers, and online vendors) and Nintendo of America directly infringe one or more claims of the '347 patent under 35 U.S.C. § 271(a) by selling, offering to sell, or importing the '347 Infringing Products in or into the United States. The Nintendo Defendants have actively induced infringement of, and continue to actively induce infringement of, one or more claims of the '347 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by selling, importing, and/or offering for sale the '347 Infringing Products to its customers and/or Nintendo of America with the knowledge of the '347 patent and its claims, with knowledge that its customers and/or Nintendo of America will sell, offer to sell, and/or import into the United States the '347 Infringing Products, and with knowledge and specific intent to encourage and facilitate those infringing sales or imports of the '347 Infringing Products through distributing the products to retailers, distributors, and online vendors and creating and disseminating promotional and marketing materials, instructional manuals, product manuals and other technical materials related to the '347 Infringing Products.

21. The Nintendo Defendants have had knowledge of '347 patent and their infringement of that patent since at least December 11, 2014 through a letter sent by Round Rock concerning that infringement.

22. The Nintendo Defendants have infringed, and continue to infringe, at least claims 1, 2, 3, 4, 5, and/or 6 of the '347 patent.

23. Round Rock has been and continues to be damaged by the Nintendo Defendants' infringement of the '347 patent.

24. The Nintendo Defendants have willfully infringed, and continue to willfully infringe, the '347 patent despite having knowledge of the '347 patent at least through Round Rock's December 11, 2014 letter concerning their infringement.

25. The Nintendo Defendants' conduct in infringing the '347 patent renders this case exceptional within the meaning of 35 U.S.C. § 285.

COUNT II

Infringement of U.S. Patent No. 6,147,405

26. Paragraphs 1 through 25 are incorporated by reference as if fully stated herein.

27. The '405 patent is valid and enforceable.

28. The Nintendo Defendants have infringed, and continue to infringe, one or more claims of the '405 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, products encompassed by those claims, including for example, by making, using, selling, offering for sale, and/or importing into the United States all video game products incorporating unlicensed GPUs or any other unlicensed semiconductor components manufactured using a 90nm or later (smaller) process (collectively, the "'405

Infringing Products"). The '405 Infringing Products include, but are not limited to, the Nintendo Wii, the Nintendo Wii U, and the Nintendo Wii Mini, consoles, systems, and remotes.

29. The Nintendo Defendants' customers (e.g., distributors, retailers, and online vendors) and Nintendo of America directly infringe one or more claims of the '405 patent under 35 U.S.C. § 271(a) by selling, offering to sell, or importing the '405 Infringing Products in or into the United States. The Nintendo Defendants have actively induced infringement of, and continue to actively induce infringement of, one or more claims of the '405 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by selling, importing, and/or offering for sale the '405 Infringing Products to its customers and/or Nintendo of America with the knowledge of the '405 patent and its claims, with knowledge that its customers and/or Nintendo of America will sell, offer to sell, and/or import into the United States the '405 Infringing Products, and with knowledge and specific intent to encourage and facilitate those infringing sales or imports of the '405 Infringing Products through distributing the products to retailers, distributors, and online vendors and creating and disseminating promotional and marketing materials, instructional manuals, product manuals and other technical materials related to the '405 Infringing Products.

30. The Nintendo Defendants have had knowledge of '405 patent and their infringement of that patent since at least April 24, 2012 through a letter sent by Round Rock concerning that infringement.

31. The Nintendo Defendants have infringed, and continue to infringe, at least claims 1, 2, 3, 6, 7, 8, 9, 10 and/or 12 of the '405 patent.

32. Round Rock has been and continues to be damaged by the Nintendo Defendants' infringement of the '405 patent.

33. The Nintendo Defendants have willfully infringed, and continue to willfully infringe, the ’405 patent despite having knowledge of the ’405 patent at least through Round Rock’s April 24, 2012 letter concerning their infringement.

34. The Nintendo Defendants’ conduct in infringing the ’405 patent renders this case exceptional within the meaning of 35 U.S.C. § 285.

COUNT III

Infringement of U.S. Patent No. 6,358,801

35. Paragraphs 1 through 34 are incorporated by reference as if fully stated herein.

36. The ’801 patent is valid and enforceable.

37. The Nintendo Defendants have infringed, and continue to infringe, one or more claims of the ’801 patent under 35 U.S.C. § 271(a) and/or 271(g), either literally and/or under the doctrine of equivalents, by making, selling, offering to sell, using, and/or importing into the United States, products made by a process described in those claims, including for example, by making, using, selling, offering for sale, and/or importing into the United States all video game products incorporating unlicensed GPUs or any other unlicensed semiconductor components manufactured using a 90nm or later (smaller) process (collectively, the “’801 Infringing Products”). The ’801 Infringing Products include, but are not limited to, the Nintendo Wii, the Nintendo Wii U, the Nintendo Wii Mini, and the Nintendo 3DS consoles, systems, and remotes.

38. The Nintendo Defendants’ customers (e.g., distributors, retailers, and online vendors) and Nintendo of America directly infringe one or more claims of the ’801 patent under 35 U.S.C. § 271(a) and/or 271(g) by selling, offering to sell, or importing the ’801 Infringing Products in or into the United States. The Nintendo Defendants have actively induced infringement of, and continue to actively induce infringement of, one or more claims of the ’801

patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by selling, importing, and/or offering for sale the ’801 Infringing Products to its customers and/or Nintendo of America with the knowledge of the ’801 patent and its claims, with knowledge that its customers and/or Nintendo of America will sell, offer to sell, and/or import into the United States the ’801 Infringing Products, and with knowledge and specific intent to encourage and facilitate those infringing sales or imports of the ’801 Infringing Products through distributing the products to retailers, distributors, and online vendors and creating and disseminating promotional and marketing materials, instructional manuals, product manuals and other technical materials related to the ’801 Infringing Products.

39. The Nintendo Defendants have had knowledge of ’801 patent and their infringement of that patent since at least December 11, 2014 through a letter sent by Round Rock concerning that infringement.

40. Round Rock has been and continues to be damaged by the Nintendo Defendants’ infringement of the ’801 patent.

41. The Nintendo Defendants have infringed, and continue to infringe, at least claims 1 and/or 2 of the ’801 patent.

42. The Nintendo Defendants have willfully infringed, and continue to willfully infringe, the ’801 patent despite having knowledge of the ’801 patent at least through Round Rock’s December 11, 2014 letter concerning their infringement.

43. The Nintendo Defendants’ conduct in infringing the ’801 patent renders this case exceptional within the meaning of 35 U.S.C. § 285.

COUNT IV

Infringement of U.S. Patent No. 6,455,935

44. Paragraphs 1 through 43 are incorporated by reference as if fully stated herein.

45. The ’935 patent is valid and enforceable.

46. The Nintendo Defendants have infringed, and continue to infringe, one or more claims of the ’935 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, products encompassed by those claims, including for example, by making, using, selling, offering for sale, and/or importing into the United States all video game consoles incorporating unlicensed GPUs or any other unlicensed semiconductor components manufactured using a 90nm or later (smaller) process (collectively, the “’935 Infringing Products”). The ’935 Infringing Products include, but are not limited to, the Nintendo Wii, the Nintendo Wii U, and the Nintendo Wii Mini consoles, systems, and remotes.

47. The Nintendo Defendants’ customers (e.g., distributors, retailers, and online vendors) and Nintendo of America directly infringe one or more claims of the ’935 patent under 35 U.S.C. § 271(a) by selling, offering to sell, or importing the ’935 Infringing Products in the United States. The Nintendo Defendants have actively induced infringement of, and continue to actively induce infringement of, one or more claims of the ’935 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by selling, importing, and/or offering for sale the ’935 Infringing Products to its customers and/or Nintendo of America with the knowledge of the ’935 patent and its claims, with knowledge that its customers and/or Nintendo of America will sell, offer to sell, and/or import into the United States the ’935 Infringing Products, and with knowledge and specific intent to encourage and facilitate those infringing

sales or imports of the ’935 Infringing Products through distributing the products to retailers, distributors, and online vendors and creating and disseminating promotional and marketing materials, instructional manuals, product manuals and other technical materials related to the ’935 Infringing Products.

48. The Nintendo Defendants have had knowledge of ’935 patent and their infringement of that patent since at least April 24, 2012 through a letter sent by Round Rock concerning that infringement.

49. The Nintendo Defendants have infringed, and continue to infringe, at least claims 1, 2, 3, 4, 6, 8, 9, and/or 10 of the ’935 patent.

50. Round Rock has been and continues to be damaged by the Nintendo Defendants’ infringement of the ’935 patent.

51. The Nintendo Defendants have willfully infringed, and continue to willfully infringe, the ’935 patent despite having knowledge of the ’935 patent at least through Round Rock’s April 24, 2012 letter concerning their infringement.

52. The Nintendo Defendants’ conduct in infringing the ’935 patent renders this case exceptional within the meaning of 35 U.S.C. § 285.

COUNT V

Infringement of U.S. Patent No. 6,469,336

53. Paragraphs 1 through 52 are incorporated by reference as if fully stated herein.

54. The ’336 patent is valid and enforceable.

55. The Nintendo Defendants have infringed, and continue to infringe, one or more claims of the ’336 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or

importing into the United States, products encompassed by those claims, including for example, by making, using, selling, offering for sale, and/or importing into the United States all video game products incorporating the "Hollywood-1" GPU, the "Hollywood-2" GPU (also known as the Renesas D813302 GPU), and/or the "Latte" GPU (also known as the Renesas D813301 GPU), including but not limited to the Nintendo Wii, the Nintendo Wii U, and the Nintendo Wii Mini video game consoles (collectively, the "'336 Infringing Products").

56. The Nintendo Defendants' customers (e.g., distributors, retailers, and online vendors) and Nintendo of America directly infringe one or more claims of the '336 patent under 35 U.S.C. § 271(a) by selling, offering to sell, or importing the '336 Infringing Products in the United States. The Nintendo Defendants have actively induced infringement of, and continue to actively induce infringement of, one or more claims of the '336 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by selling, importing, and/or offering for sale the '336 Infringing Products to its customers and/or Nintendo of America with the knowledge of the '336 patent and its claims, with knowledge that its customers and/or Nintendo of America will sell, offer to sell, and/or import into the United States the '336 Infringing Products, and with knowledge and specific intent to encourage and facilitate those infringing sales or imports of the '336 Infringing Products through distributing the products to retailers, distributors, and online vendors and creating and disseminating promotional and marketing materials, instructional manuals, product manuals and other technical materials related to the '336 Infringing Products.

57. The Nintendo Defendants have had knowledge of the '336 patent and their infringement of that patent since at least August 27, 2013 through email correspondence sent by Round Rock concerning that infringement.

58. The Nintendo Defendants have infringed, and continue to infringe, at least claims 1 and 2 of the ’336 patent.

59. Round Rock has been and continues to be damaged by the Nintendo Defendants’ infringement of the ’336 patent.

60. The Nintendo Defendants have willfully infringed, and continue to willfully infringe, the ’336 patent despite having knowledge of the ’336 patent at least through Round Rock’s August 27, 2013 email correspondence concerning their infringement.

61. The Nintendo Defendants’ conduct in infringing the ’336 patent renders this case exceptional within the meaning of 35 U.S.C. § 285.

COUNT VI

Infringement of U.S. Patent No. 6,828,683

62. Paragraphs 1-61 are incorporated by reference as if fully stated herein.

63. The ’683 patent is valid and enforceable.

64. The Nintendo Defendants have infringed, and continue to infringe, one or more claims of the ’683 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, products encompassed by those claims, including for example, by making, using, selling, offering for sale, and/or importing into the United States all video game products incorporating unlicensed GPUs, processors, or any other unlicensed semiconductor components manufactured using a 90nm or later (smaller) process (collectively, the “’683 Infringing Products”). The ’683 Infringing Products include, but are not limited to, the Nintendo Wii, the Nintendo Wii U, the Nintendo Wii Mini, the Nintendo 3DS XL, and the Nintendo 2DS consoles, systems, and remotes.

65. The Nintendo Defendants' customers (e.g., distributors, retailers, and online vendors) and Nintendo of America directly infringe one or more claims of the '683 patent under 35 U.S.C. § 271(a) by selling, offering to sell, or importing the '683 Infringing Products in the United States. The Nintendo Defendants have actively induced infringement of, and continue to actively induce infringement of, one or more claims of the '683 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by selling, importing, and/or offering for sale the '683 Infringing Products to its customers and/or Nintendo of America with the knowledge of the '683 patent and its claims, with knowledge that its customers and/or Nintendo of America will sell, offer to sell, and/or import into the United States the '683 Infringing Products, and with knowledge and specific intent to encourage and facilitate those infringing sales or imports of the '683 Infringing Products through distributing the products to retailers, distributors, and online vendors and creating and disseminating promotional and marketing materials, instructional manuals, product manuals and other technical materials related to the '683 Infringing Products.

66. The Nintendo Defendants have had knowledge of the '683 patent and their infringement of that patent since at least December 11, 2014 through a letter sent by Round Rock concerning that infringement.

67. The Nintendo Defendants have infringed, and continue to infringe, at least claims 27, 28, 30, 32, 33, 34, and/or 35 of the '683 patent.

68. Round Rock has been and continues to be damaged by the Nintendo Defendants' infringement of the '683 patent.

69. The Nintendo Defendants have willfully infringed, and continue to willfully infringe, the ’683 patent despite having knowledge of the ’683 patent at least through Round Rock’s December 11, 2014 letter concerning their infringement.

70. The Nintendo Defendants’ conduct in infringing the ’683 patent renders this case exceptional within the meaning of 35 U.S.C. § 285.

Prayer For Relief

WHEREFORE, Round Rock prays for judgment as follows:

A. That the Nintendo Defendants have directly and/or indirectly infringed each of the Patents-in-Suit;

B. That the Nintendo Defendants have willfully infringed each of the Patents-in-Suit;

B. That Round Rock be awarded all damages adequate to compensate it for the Nintendo Defendants’ infringement of the Patents-in-Suit, such damages to be determined by a jury and, if necessary to adequately compensate Round Rock for the infringement, an accounting, and that such damages be trebled and awarded to Round Rock with pre-judgment and post-judgment interest;

C. That this case by declared an exceptional case within the meaning of 35 U.S.C. § 285 and that Round Rock be awarded the attorney fees, costs, and expenses that it incurs prosecuting this action; and

D. That Round Rock be awarded such other and further relief as this Court deems just and proper.

Demand For Jury Trial

Plaintiff Round Rock hereby demands a trial by jury on all issues so triable.

Dated: January 14, 2016

Respectfully submitted,

FARNAN LLP

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Counsel for Plaintiff
Round Rock Research, LLC

EXHIBIT A

US005986347A

United States Patent [19]

Donohoe et al.

[11] Patent Number: 5,986,347

[45] Date of Patent: Nov. 16, 1999

[54] **PROCESSING METHODS OF FORMING CONTACT OPENINGS AND INTEGRATED CIRCUITRY**

[75] Inventors: **Kevin G. Donohoe**; **Kirk D. Prall**, both of Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **09/107,930**

[22] Filed: **Jun. 30, 1998**

Related U.S. Application Data

[62] Division of application No. 08/911,311, Aug. 14, 1997.

[51] **Int. Cl.**[6] **H01L 23/48**; H01L 29/46

[52] **U.S. Cl.** **257/774**; 257/758; 257/760; 257/308

[58] **Field of Search** 257/774, 758, 257/760, 308

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,488,166	12/1984	Lehrer	257/774
5,094,900	3/1992	Langley	257/774
5,180,689	1/1993	Liu et al.	437/228
5,408,130	4/1995	Woo et al.	257/774
5,451,819	9/1995	Koyama	257/774
5,468,342	11/1995	Nulty et al.	156/643.1
5,665,623	9/1997	Liang et al.	438/239

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A. Shinohara et al., "A New Self–Aligned Contact Technology for LLD MOS Transistors", Extended Abstracts of the 17th Conference on Solid State Devices and Materials, Tokyo, Japan, 1985, pp. 12–15.

Primary Examiner—Teresa M. Arroyo

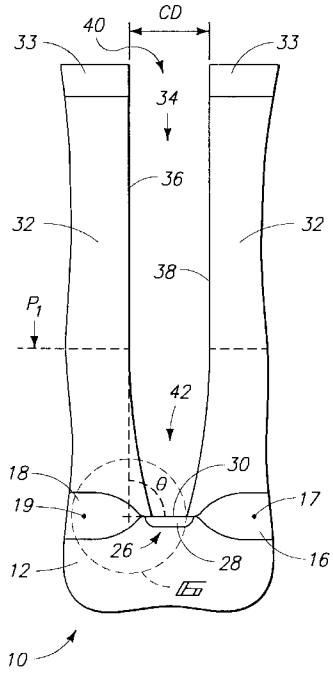
Assistant Examiner—Hung Van Duong

Attorney, Agent, or Firm—Wells, St. John, Roberts, Gregory & Matkin P.S.

[57] **ABSTRACT**

Methods of forming contact openings over a node location and related integrated circuitry are described. In one aspect of the invention, a node location is formed within a semiconductive substrate adjacent an isolation oxide region. A layer of material is formed over the node location and a contact opening is etched through the layer of material to outwardly expose a node location planar upper surface. In one preferred implementation, the contact opening includes an inner surface portion which faces generally transversely away from the isolation oxide region and which defines an angle with the node location upper surface which is greater at a bottom of the contact opening than at a top of the contact opening. In another preferred implementation, the contact opening includes sidewall portions which define a profile which having a non-uniform degree of taper between the contact opening top and bottom. In another preferred implementation, the tapering of the contact opening is effectuated by modifying at least one etching parameter at an intermediate etching point and continuing the etching to outwardly expose the node location.

7 Claims, 5 Drawing Sheets



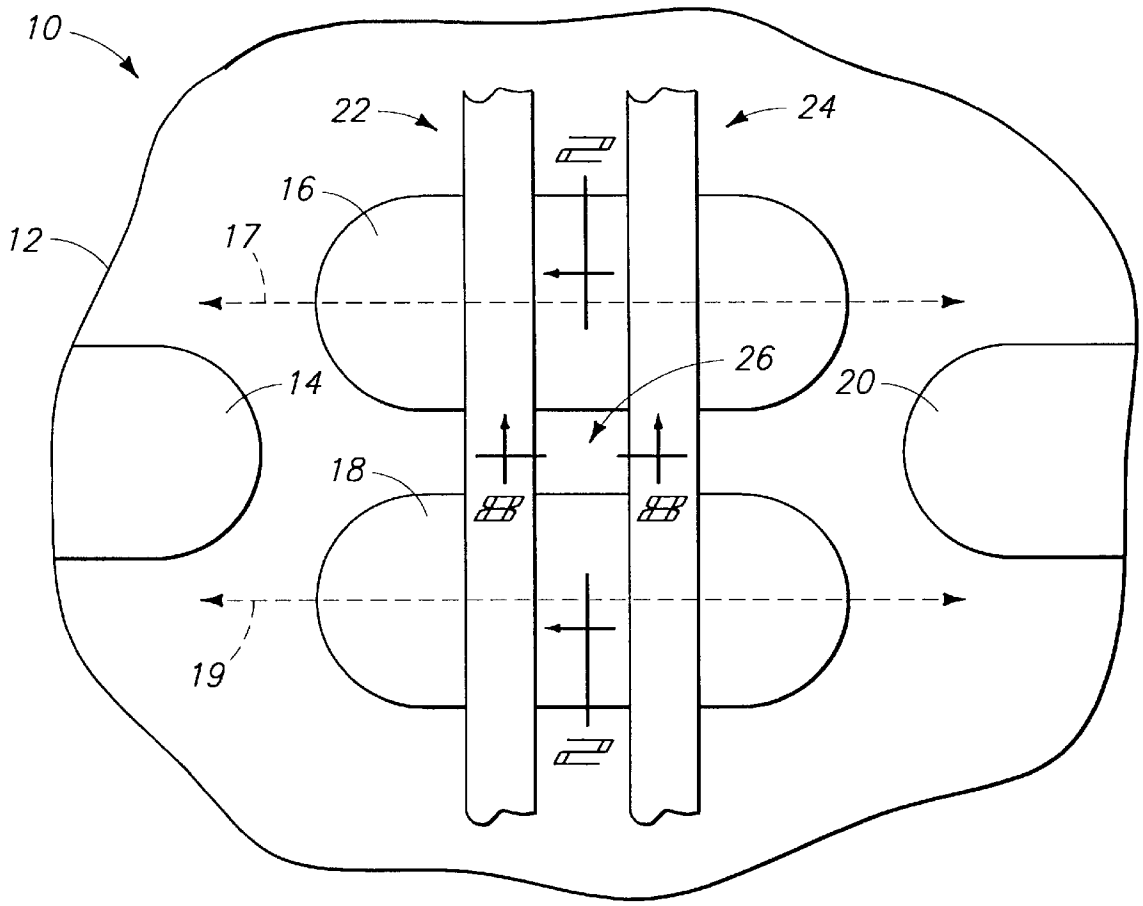


Fig. 1

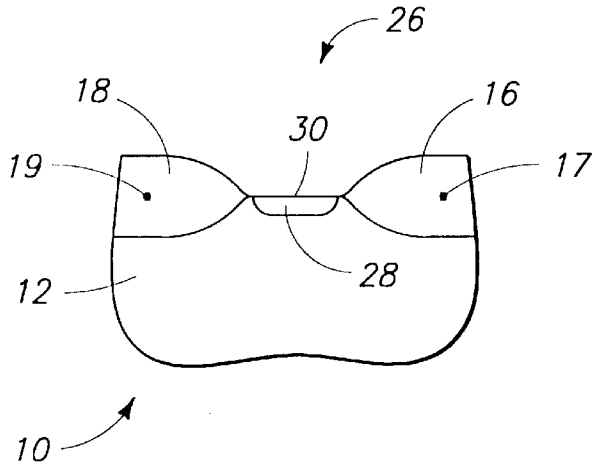


Fig. 2

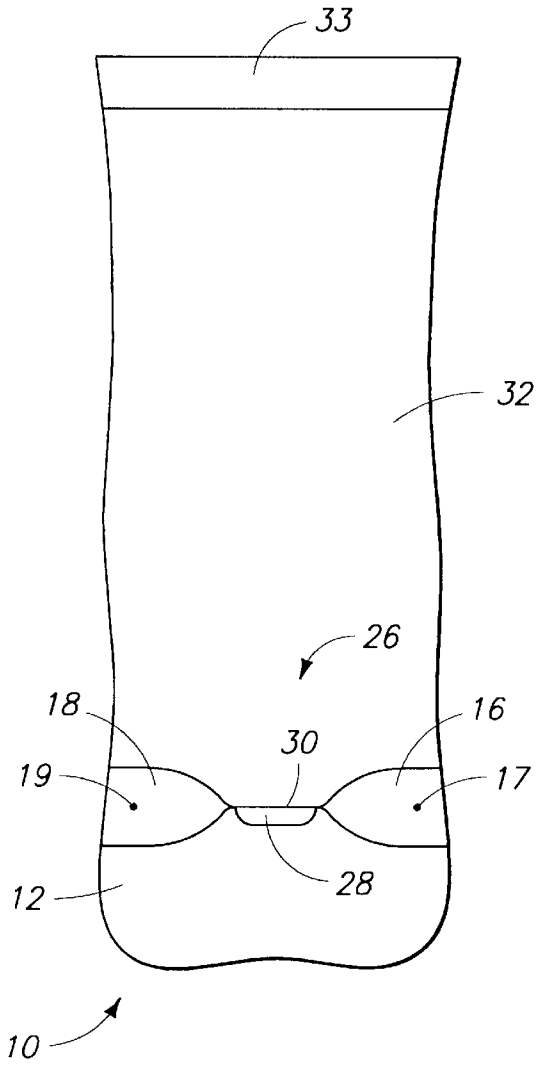

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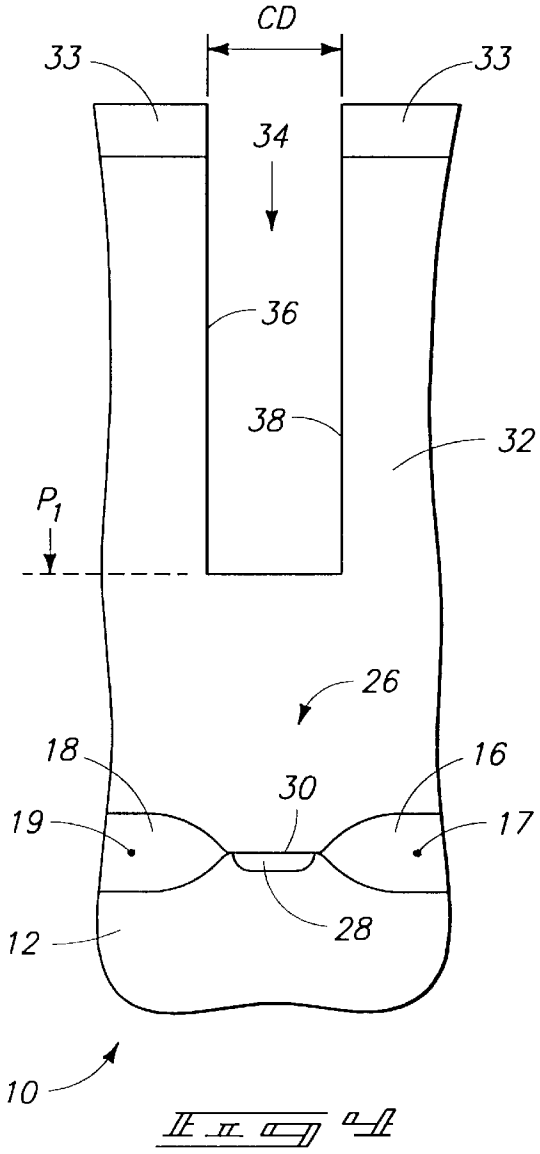
Fig. 3


CD
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10

Fig. 4

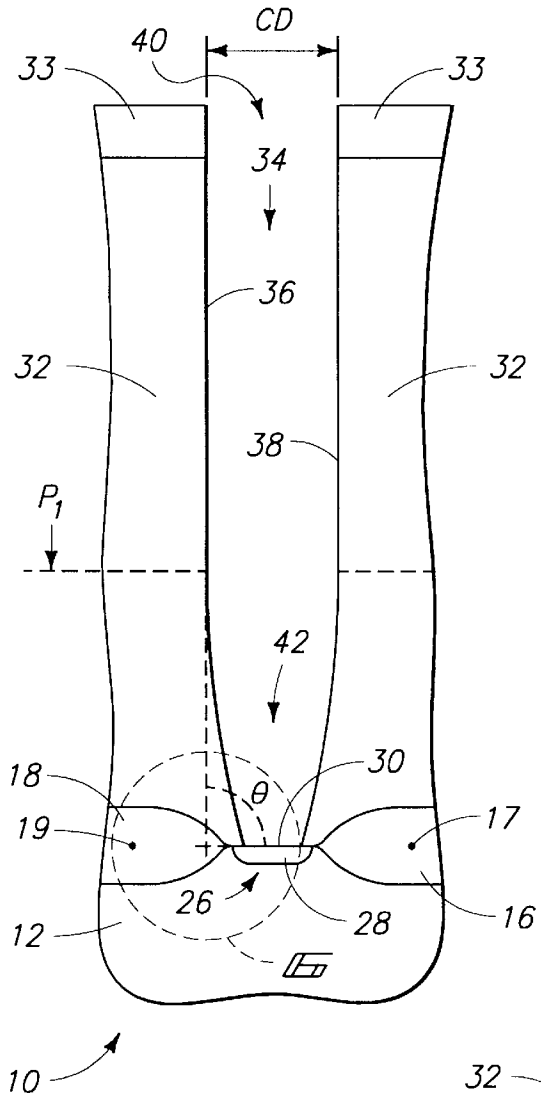
CD
40
33
33
34
36
32
32
38
P_1
42
18
30
θ
19
17
26
28
16
12
10

Fig 5

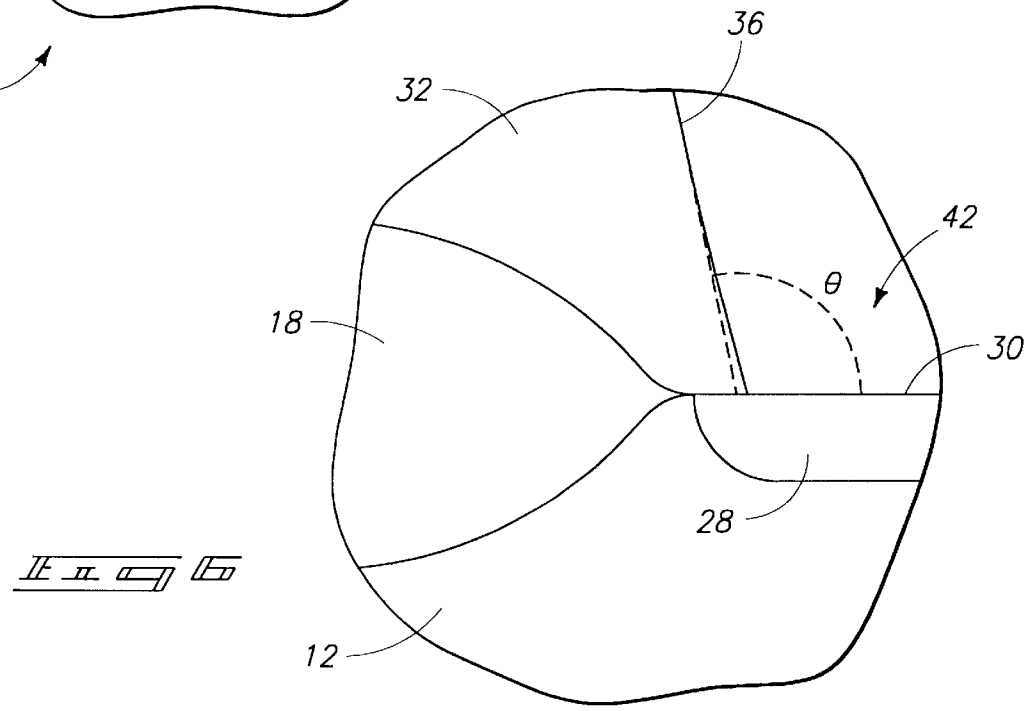
36
32
42
θ
18
30
28
12

Fig 6

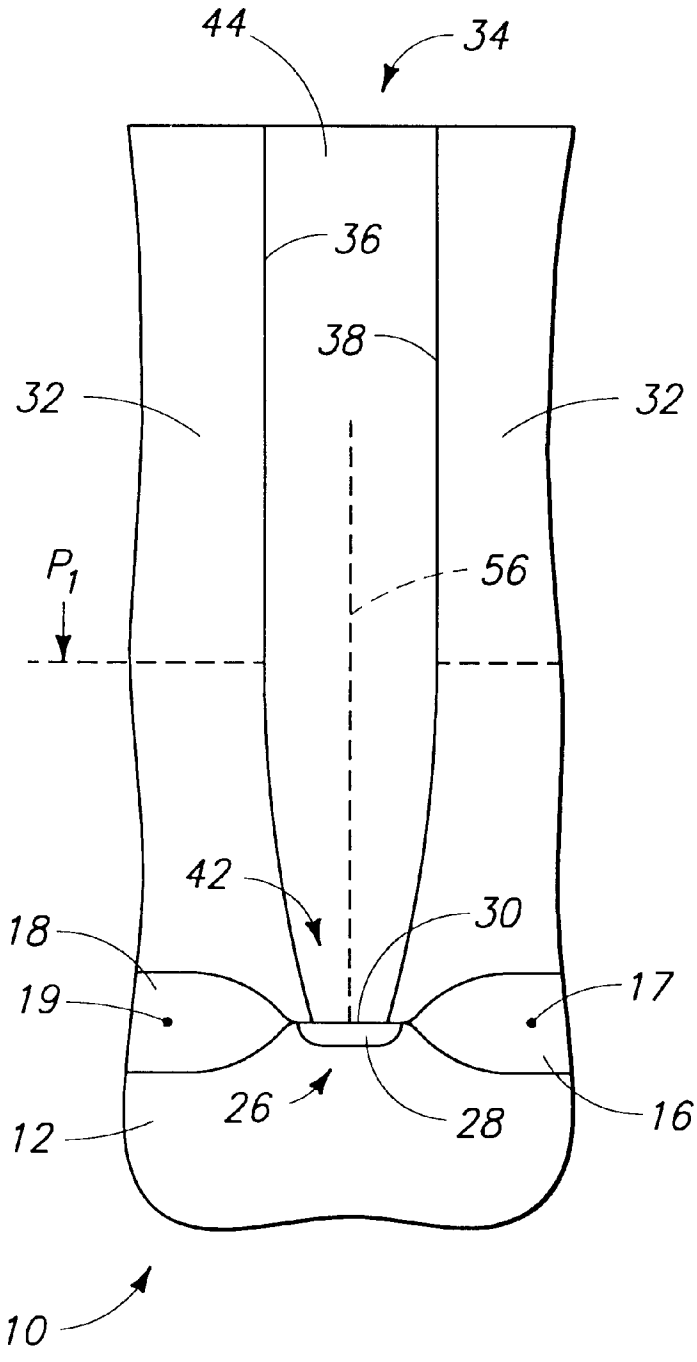

Fig. 2

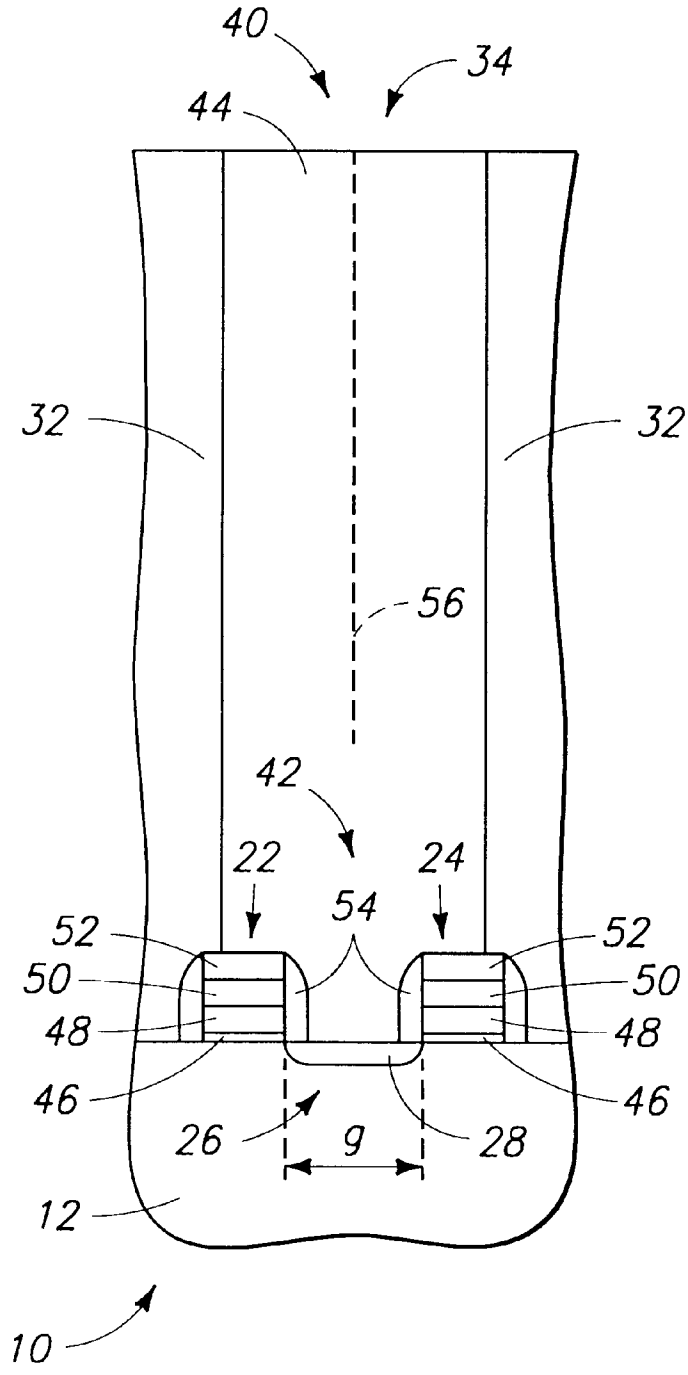

Fig. 8

PROCESSING METHODS OF FORMING CONTACT OPENINGS AND INTEGRATED CIRCUITRY

RELATED PATENT DATA

This patent resulted from a divisional application of U.S. patent application Ser. No. 08/911,311, filed Aug. 14, 1997, entitled "Processing Methods of Forming Contact Openings and Integrated Circuitry", naming Kevin G. Donohoe and Kirk D. Prall as inventors.

TECHNICAL FIELD

This invention relates to methods of forming contact openings and related integrated circuitry.

BACKGROUND OF THE INVENTION

Fabrication of integrated circuitry typically involves forming contact openings through an insulative layer to an elevationally lower substrate node location, such as a diffusion region which constitutes part of a field effect transistor. Typically, field effect transistors are fabricated on a semiconductor wafer, with selected individual transistors being separated by isolation oxide or field oxide regions. As integrated circuitry dimensions grow smaller and smaller, challenges are presented with respect to the formation of contact openings to substrate node locations.

For example, one type of integrated circuitry is a dynamic random access memory device which includes a plurality of isolation oxide regions over which conductive word lines extend. Conductive word lines are usually covered or insulated with protective nitride caps and sidewalls. A thick layer of oxide typically overlies the word lines. A contact opening etch can be conducted selective relative to the protective caps and sidewalls to achieve self-alignment of the contact opening in a direction perpendicular to the line. However, because such word lines typically overlie isolation oxide regions, and because the insulative layer through which the contact opening is etched usually etches in the same manner as the material from which the isolation oxide regions are formed, e.g. when both are oxides, a problem arises insofar as undesirably etching into the isolation oxide region when the contact openings are formed.

This invention arose out of concerns associated with improving the manner in which contact openings are formed in integrated device fabrication.

SUMMARY OF THE INVENTION

Methods of forming contact openings over a node location and related integrated circuitry are described. In one aspect of the invention, a node location -is formed within a semiconductive substrate adjacent an isolation oxide region. A layer of material is formed over the node location and a-contact opening is etched through the layer of material to outwardly expose a node location planar upper surface. In one preferred implementation, the contact opening includes an inner surface portion which faces generally transversely away from the isolation oxide region and which defines an angle with the node location upper surface which is greater at a bottom of the contact opening than at a top of the contact opening. In another preferred implementation, the contact opening includes sidewall portions which define a profile which has a non-uniform degree of taper between the contact opening top and bottom. In another preferred implementation, the tapering of the contact opening is effectuated by modifying at least one etching parameter at an intermediate etching point and continuing the etching to outwardly expose the node location.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

FIG. **1** is a plan view of a semiconductor wafer fragment at one processing step in accordance with the invention.

FIG. **2** is a view of the semiconductor wafer fragment taken along line **2—2** in FIG. **1**.

FIG. **3** is a view of the FIG. **2** wafer fragment at a processing step subsequent to that shown by FIG. **2**.

FIG. **4** is a view of the FIG. **2** wafer fragment at a processing step subsequent to that shown by FIG. **3**.

FIG. **5** is a view of the FIG. **2** wafer fragment at a processing step subsequent to that shown by FIG. **4**.

FIG. **6** is a view of the FIG. **2** wafer fragment at a processing step subsequent to that shown by FIG. **5**.

FIG. **7** is a view of the FIG. **2** wafer fragment at a processing step subsequent to that shown by FIG. **6**.

FIG. **8** is a view of the FIG. **1** wafer fragment taken along line **8—8** in FIG. **1** at a processing step subsequent to that shown by FIG. **6**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to FIGS. **1** and **2**, a semiconductor wafer fragment in process is shown generally at **10** and comprises a semiconductive substrate **12**. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. In the illustrated example, an 8-inch wafer was used as the substrate.

A plurality of isolation oxide regions **14**, **16**, **18**, and **20** are formed within substrate **12**. The isolation oxide regions are preferably formed through suitable oxidation of substrate **12** through LOCOS techniques. In the illustrated example, the isolation oxide regions are spaced apart over substrate **12** and are formed along longitudinal axes, individual respective axes for isolation regions **16**, **18** being indicated at **17**, **19**. Isolation oxide regions **16**, **18** constitute a pair of spaced apart isolation oxide regions whose respective longitudinal axes **17**, **19** are generally or substantially parallel to one another.

Referring to FIGS. **1**, **2**, and **8**, a pair of laterally spaced apart conductive lines **22**, **24** are formed over substrate **12** and oriented generally transversely of longitudinal axes **17**, **19**. In the illustrated example, conductive lines **22**, **24** overlie respective isolation oxide regions **16**, **18**. Such conductive lines typically include, as shown in FIG. **8**, a thin oxide layer **46**, conductive layers **48**, **50** (typically comprising polysilicon and a silicide layer respectively), and a protective cap or capping layer **52**. Sidewall spacers **54** are

also provided. Other conductive line constructions are possible. According to one implementation of the invention, caps **52** and spacers **54** comprise a nitride material which protects the conductive portions of the lines during a subsequent contact opening etch discussed in more detail below. In the illustrated and preferred embodiment, the conductive lines are formed to an elevational thickness of about 2000–3000 Angstroms (not including the elevational thickness of the nitride caps). The preferred nitride caps are formed to an elevational thickness of about 3000 Angstroms so that the total elevational thickness of the individual conductive lines with nitride caps is around about 5000–6000 Angstroms. Additionally, the gap g (FIG. **8**) between lines **22**, **24** is preferably around 2500 Angstroms or less.

A node location **26** is formed within substrate **12** adjacent respective isolation oxide regions **16**, **18** and adjacent respective conductive lines **22**, **24**. In the illustrated and preferred embodiment, node location **26** constitutes a diffusion region **28** (FIG. **2**) having a generally planar upper surface **30**.

Referring to FIG. **3**, a layer of material **32** is formed over substrate **12**. Accordingly, layer **32** is formed over and outwardly of node location **26**, isolation oxide regions **16**, **18**, and conductive lines **22**, **24** (FIG. **1**). A suitable material for layer **32** comprises borophosphosilicate glass (BPSG). An exemplary thickness is about 18,000 Angstroms. Alternately considered and in accordance with one implementation, layer **32** is formed to a thickness over the illustrated conductive lines (FIG. **8**) of at least 3000 Angstroms, and preferably greater than 4000 Angstroms. A masking material layer **33**, preferably comprising photoresist, is subsequently formed over the substrate.

Referring to FIG. **4**, photoresist layer **33** is patterned and an opening **34** which constitutes a portion of a contact opening is etched into layer **32** to an intermediate etching point P_1. The patterning of opening **34** defines an opening lateral width or critical dimension (CD). In the illustrated example, the patterned lateral width of the opening at this point in the etching (i.e. at or adjacent the top of opening **34**) is about 0.4 μm. The lateral width of the contact opening taken in a direction into the page which is transverse to conductive lines **22**, **24** in FIG. **1** is about 0.7 μm. Such a transverse lateral width is shown in FIG. **8**. Intermediate etching point P_1 can be any intermediate etching point between the beginning of the etching which forms the contact opening portion and node location **26**. The etching of opening **34** defines respective contact opening sidewall portions **36**, **38**. In this example, the illustrated sidewall portions **36**, **38** overlie respective isolation oxide regions **18**, **16**. The preferred etching of the contact opening is conducted in a LAM 9100 etcher and an exemplary etch or etching chemistry which is suitable for conducting this etch is one which is conducted in accordance with the following parameters: 1100 Watts (power applied to an external reactor electrode), 1900 Watts (power applied to an internal wafer carrier), 43 CHF_3, 20 C_2HF_5, 1 C_2F_6 (units in sccm), 5 mTorr, and 35 seconds. Such etching parameters permit the illustrated opening to be formed to just proximate the nitride caps covering conductive lines **22**, **24** (FIG. **1**).

Referring to FIG. **5**, and in the illustrated and preferred embodiment, at least one etching parameter is modified at or adjacent etching point P_1 to taper selected individual contact opening sidewall portions **36**, **38** generally transversely away from the nearest respective longitudinal axis **19**, **17** of corresponding isolation oxide regions **18**, **16**. Such etch preferably outwardly exposes node location **26**. An exemplary etch or etching chemistry which is suitable for conducting this etch is one which is conducted in accordance with the following parameters: 1000 Watts (power applied to the external reactor electrode), 2150 Watts (power applied to the internal wafer carrier), 20 CHF_3, 90 C_2HF_5, 5 C_2F_6 (units in sccm), 5 mTorr, and 45 seconds. Such etch is preferably increasingly selective to nitride and results in the illustrated tapering of the contact opening. In the preferred embodiment, the etching of the contact opening constitutes etching the contact opening to taper the illustrated sidewall portions in the absence of individual contact opening sidewall contact with any substrate structure. In addition, the etching of the illustrated contact opening preferably does not meaningfully increase the patterned lateral width or CD of the contact opening at or adjacent the top thereof. Accordingly, the illustrated and preferred contact opening has a lateral width dimension adjacent the contact opening top which is essentially equivalent to the original patterned lateral width dimension. Such etching of the contact opening constitutes etching a contact opening, at least of portion of which gradually tapers, without the etching increasing the patterned lateral width or critical dimension of the contact opening. Alternately considered, the patterned lateral width dimension or CD is generally maintained during the etching of the contact opening. Alternately considered, the contact opening has an initial lateral width dimension adjacent the contact opening top which is generally maintained during the etching of the contact opening. Such is different from known etching regimes in which photoresist erosion is utilized to increase the CD of the upper portion of a contact opening when forming the same.

Another exemplary etch or etching chemistry for the above-mentioned LAM 9100 etcher is a multiple-step process which is conducted in accordance with the following parameters: Step **1**—1100 Watts (power applied to the external reactor electrode), 1900 Watts (power applied to the internal wafer carrier), 61 CHF_3, 11.5 C_2HF_5, 1 CH_2F_2 (units in sccm), 10 mTorr, and 7 seconds; Step 2—1100 Watts (power applied to the external reactor electrode), 900 Watts (power applied to the internal wafer carrier), 61 CHF_3, 11.5 C_2HF_5, 1 CH_2F_2, 10 mTorr, and 18 seconds; Step **3**—1000 Watts (power applied to the external reactor electrode), 1600 Watts (power applied to the internal wafer carrier), 49 CHF_3; 23 C_2HF_5, 5 CH_2F_2, 5 mTorr, and 5 seconds; Step **4**—1000 Watts (power applied to the external reactor electrode), 2150 Watts (power applied to the internal wafer carrier), 49 CHF_3, 23 C_2HF_5, 5 CH_2F_2, 5 mTorr, and 30 seconds; and Step **5**—1000 Watts (power applied to the external reactor electrode), 1500 Watts (power applied to the internal wafer carrier), 49 CHF_3, 34.5 C_2HF_5, 5 CH_2F_2, 2 mTorr, and 49 seconds. Other processes having more or less steps can be utilized. One such exemplary process utilizes two steps and is as follows: Step **1**—1500 Watts (power applied to the external reactor electrode), 1400 Watts (power applied to the internal reactor electrode), 16 C_2HF_5 (units in sccm), 50 CHF_3, 1 CH_2F_2, 120 Argon, 5 mTorr, and 35 seconds; Step **2**—1000 Watts (power applied to the external reactor electrode), 1375 Watts (power applied to the internal reactor electrode), 45 C_2HF_5 (units in sccm), 35 CHF_3, 20 CH_2F_2, 2 mTorr, and 80 seconds. As formed, contact opening **34** has a contact opening top **40** and a contact opening bottom **42** and an aspect ratio (contact opening height-to-width ratio) of from about 5–30, and preferably around 10. The preferred contact opening also has a degree of taper which is defined between contact opening top **40** and contact opening bottom **42**. As shown, the degree of taper is one which varies the width of the contact opening and preferably

results in a contact opening profile with a degree of concavity which is greater nearest contact opening bottom **42** than adjacent contact opening top **40**. In the illustrated and preferred embodiment, the degree of taper arcuately varies, increasing as the contact opening reaches node location **26** proximate the bottom most portion of contact opening bottom **42**. An exemplary contact opening width adjacent contact opening bottom **42** of FIG. **5** is around 0.2 μm.

Alternately considered, contact opening **34** as shown in FIG. **5** defines a profile which lies in or along a plane which is taken through the contact opening and which is both generally transverse the isolation oxide regions' longitudinal axes **17**, **19**, (FIG. **1**) and generally transverse the node location planar upper surface **30**. Such profile is also taken through the contact opening and in a plane which is parallel to either of conductive lines **22**, **24** (FIG. **1**). Such profile, when viewed from top-to-bottom, includes a profile portion which tapers generally arcuately toward node location **26**. The illustrated profile defines a non-uniform degree of taper between contact opening top **40** and contact opening bottom **42**. The contact opening is preferably narrower at or adjacent contact opening bottom **42** than at or adjacent contact opening top **40**. As formed, the contact opening profile is generally bowed arcuately inwardly proximate contact opening bottom **42**.

Alternately considered and with reference to FIGS. **5** and **6**, contact opening **34** includes a pair of inner surface portions which correspond to sidewall portions **36**, **38**. The inner surface portions face generally transversely away from the respective nearest of the isolation oxide regions' longitudinal axes **19**, **17**, and extend between contact opening top **40** and contact opening bottom **42**. Inner surface portions **36**, **38** define an angle with node location upper surface **30**. A representative angle θ is shown for inner surface portion **36** at two different locations relative to the contact opening. A first location is shown in FIG. **5** and corresponds to the angle formed between inner surface portion **36** and node location planar surface **30** adjacent contact opening top **40**. A second location is shown in FIG. **6** and corresponds to the angle formed between inner surface portion **36** and node location planar surface **30** adjacent contact opening bottom **42**. The angle θ is greater adjacent contact opening bottom **42** (FIG. **6**) than at or adjacent contact opening top **40** (FIG. **5**). As shown in FIG. **5**, θ is generally around about 90°. As shown in FIG. **6**, however, θ is generally greater than 90°. Accordingly, the contact opening inner surface portions **36**, **38** generally taper between the contact opening top and bottom and have generally arcuate bottom regions into the direction of node location upper surface **30**. Such tapering effectively minimizes or eliminates etching into isolation regions **16**, **18** when the contact opening is formed.

Referring to FIG. **7**, a plug **44** of conductive material is formed or disposed within contact opening **34** and forms an electrical connection with node location **26**.

Alternately considered, and with reference to FIGS. **1**, **7**, and **8**, a multi-directional, self-aligned contact opening **34** is formed over node location **26**. According to one aspect of the invention, a first material **32** (FIG. **3**) through which a contact opening is to be etched is formed over the substrate. Substrate **12** includes at least one substrate feature which comprises a second material and over which first material **32** is formed. In a preferred implementation, the substrate feature comprises a conductive line such as exemplary line **22**, or exemplary line pairs **22**, **24**. The second material is preferably different from first material **32** and accommodates and facilitates self-alignment of the contact opening in a first alignment direction. An exemplary first alignment direction is illustrated in FIG. **8** and is defined, in part, by the plane of the page upon which FIG. **8** appears, and corresponds to line **8**—**8** in FIG. **1**. Where first material **32** comprises an oxide material such as BPSG, the second material can comprise a nitride material such as the material which is utilized to form spacers **54** and/or caps **52**. Exemplary oxides for first material **32** also include silicon suboxide ($SiO_{<2}$) and SiO_2. Exemplary nitride material for the second material includes $Si_ZO_XN_y$, such as Si_3N_4. Other materials are, of course, possible.

Contact opening **34** is preferably etched through first material **32** to expose node location **26**. As so etched, the contact opening has sidewalls which, in one implementation, include portions in the first alignment direction (FIG. **8**) which comprise the second material from which spacers **54** are formed. FIG. **7** illustrates a second alignment direction which is different from the first alignment direction. The illustrated second alignment direction is defined, in part, by the plane of the page upon which FIG. **7** appears, and corresponds to line **2**—**2** in FIG. **1**. The illustrated second alignment direction is generally transverse the first alignment direction. In accordance with one implementation, the etched contact opening includes a contact opening center **56** and selected portions of the contact opening curve inwardly toward the contact opening center in the second alignment direction of FIG. **7**. In a preferred implementation, the selected portions of the contact opening which curve inwardly do so at an increasing rate as the contact opening reaches contact opening bottom **42**. Bottom portions of the illustrated and preferred inwardly curved portions of FIG. **7** are disposed laterally adjacent the illustrated contact opening second material portions **54** of FIG. **8**. It will be appreciated that contact openings having other profiles in the first and second directions can be formed. For example, referring to FIG. **8**, a contact opening can be formed to have a profile which comprises portions of only one of the illustrated conductive lines. An exemplary contact opening could, accordingly, have one of its sidewalls formed along line **56**.

In accordance with one implementation, the above-described contact opening is etched utilizing a first set of etching parameters which enables at least a portion of the contact opening to be etched. At some point in the etching of the contact opening, at least one of the etching parameters is changed and additional portions of the contact opening are etched. One effect of changing the etching parameters is that the above-described FIG. **7** contact opening selected portions taper or curve inwardly on themselves and toward contact opening center **56**. Exemplary etching parameters are discussed above in more detail. Hence, in accordance with the methodology described immediately above, a self-aligned contact opening which enables alignment in multiple directions is achieved.

The above described methodology has particular application in connection with the fabrication of integrated circuit memory devices, and in particular with 256M DRAM circuitry. In such case, the etching of the illustrated contact opening could constitute etching a bit line contact opening, a capacitor container opening, or some other opening to a substrate node location. Other areas of application are possible.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The

invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

We claim:

1. An integrated circuitry device comprising:

a semiconductive substrate;

a field isolation oxide region received within the substrate and having a longitudinal axis;

a node location received within the substrate adjacent the field isolation oxide region and having a generally planar upper surface;

a layer of insulating material disposed over the substrate;

a contact opening to the node location received within the layer of insulating material, the contact opening having a top and a bottom within the layer of insulating material and a contact opening inner surface portion within the layer of insulating material which faces generally transversely away from the isolation oxide longitudinal axis and which extends between the top and bottom within the layer of insulating material, the contact opening inner surface portion joining with the generally planar upper surface of the node location and defining an angle with the node location generally planar upper surface which is greater at the contact opening bottom within the layer of insulating material than at the contact opening top within the layer of insulating material; and

conductive material disposed within the contact opening and forming an electrical connection with the node location.

2. The integrated circuitry device of claim **1**, wherein the contact opening inner surface portion generally tapers between the contact opening top and bottom.

3. The integrated circuitry device of claim **1**, wherein the contact opening inner surface portion is bowed inwardly proximate the node location upper surface.

4. The integrated circuitry device of claim **1** further comprising:

a second field isolation oxide region received within the substrate and having a longitudinal axis which is generally parallel to the first mentioned longitudinal axis; and

a second contact opening inner surface portion which faces generally away from the longitudinal axis of the second isolation oxide region and toward the first mentioned contact opening inner surface portion, the second contact opening inner surface portion defining an angle with the node location upper surface which is greater at the contact opening bottom than at the contact opening top.

5. The integrated circuitry of claim **1**, wherein there is only insulating material between the entirety of the conductive material within the contact opening and the field isolation oxide region.

6. An integrated circuitry device comprising:

a semiconductive substrate;

a field isolation oxide region received within the substrate and having a longitudinal axis;

a node location received within the substrate adjacent the field isolation oxide region and having a generally planar upper surface;

a single layer of insulating material disposed over the substrate;

a contact opening to the node location received within the single layer of insulating material, the contact opening having a top and a bottom within the single layer of insulating material and a contact opening inner surface portion within the single layer of insulating material which faces generally transversely away from the isolation oxide longitudinal axis and which extends between the top and bottom within the single layer of insulating material, the contact opening inner surface portion joining with the generally planar upper surface of the node location and defining an angle with the node location generally planar upper surface which is greater at the contact opening bottom within the single layer of insulating material than at the contact opening top within the single layer of insulating material; and

conductive material disposed within the contact opening and forming an electrical connection with the node location, and wherein there is no conductive line disposed between the entirety of the conductive material within the contact opening and the field isolation oxide region.

7. The integrated circuitry device of claim **6** further comprising a second field isolation oxide region received within the substrate and having a longitudinal axis and being spaced from the first-mentioned field isolation oxide region, and wherein there is no conductive material disposed between the entirety of the conductive material within the contact opening and the second field isolation oxide region.

* * * * *

EXHIBIT B

US006147405A

United States Patent [19]

Hu

[11] Patent Number: 6,147,405

[45] Date of Patent: Nov. 14, 2000

[54] **ASYMMETRIC, DOUBLE-SIDED SELF-ALIGNED SILICIDE AND METHOD OF FORMING THE SAME**

[75] Inventor: **Yongjun Jeff Hu**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **09/026,104**

[22] Filed: **Feb. 19, 1998**

[51] **Int. Cl.**[7] **H01L 23/58**; B32B 15/04

[52] **U.S. Cl.** **257/755**; 257/756; 257/757; 257/412; 257/413; 428/472; 428/450; 428/704

[58] **Field of Search** 438/FOR 360, 438/364, 365, 583, 655, 664, 682; 428/446, 448, 450, 469, 472, 689, 699, 704; 257/755, 756, 757, 412, 413, 763, 764

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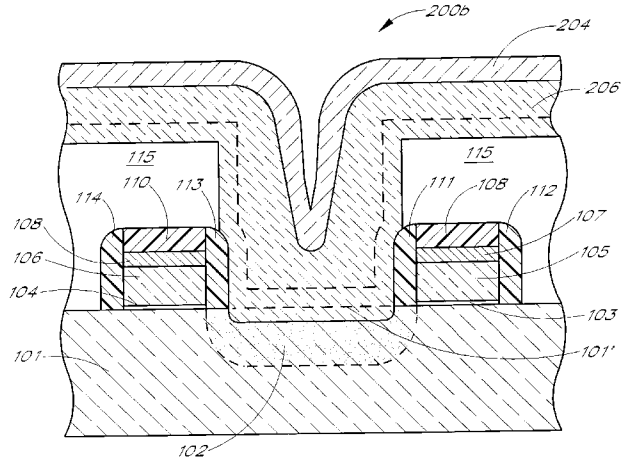
Primary Examiner—Deborah Jones
Assistant Examiner—Stephen Stein
Attorney, Agent, or Firm—Knobbe, Martens, Olson & Bear, LLP.

[57] **ABSTRACT**

Disclosed are structures and processes which are related to asymmetric, self-aligned silicidation in the fabrication of integrated circuits. A pre-anneal contact stack includes a silicon substrate, a metal source layer such as titanium-rich titanium nitride (TiN_x), and a silicon layer. The metal nitride layer is deposited on the substrate by sputtering a target metal reactively in nitrogen and argon ambient. A N:Ar ratio is selected to deposit a uniform distribution of the metal nitride in an unsaturated mode (x<1) over the silicon substrate. The intermediate substrate structure is sintered to form a metal silicide. The silicidation of metal asymmetrically consumes less of the underlying silicon than the overlying silicon layer. The resulting structure is a mixed metal silicide/nitride layer which has a sufficient thickness to provide low sheet resistance without excessively consuming the underlying substrate. A metal nitride of maximum bulk resistivity within the unsaturated (metal-rich) realm is chosen for maximizing asymmetry in the silicidation.

13 Claims, 10 Drawing Sheets



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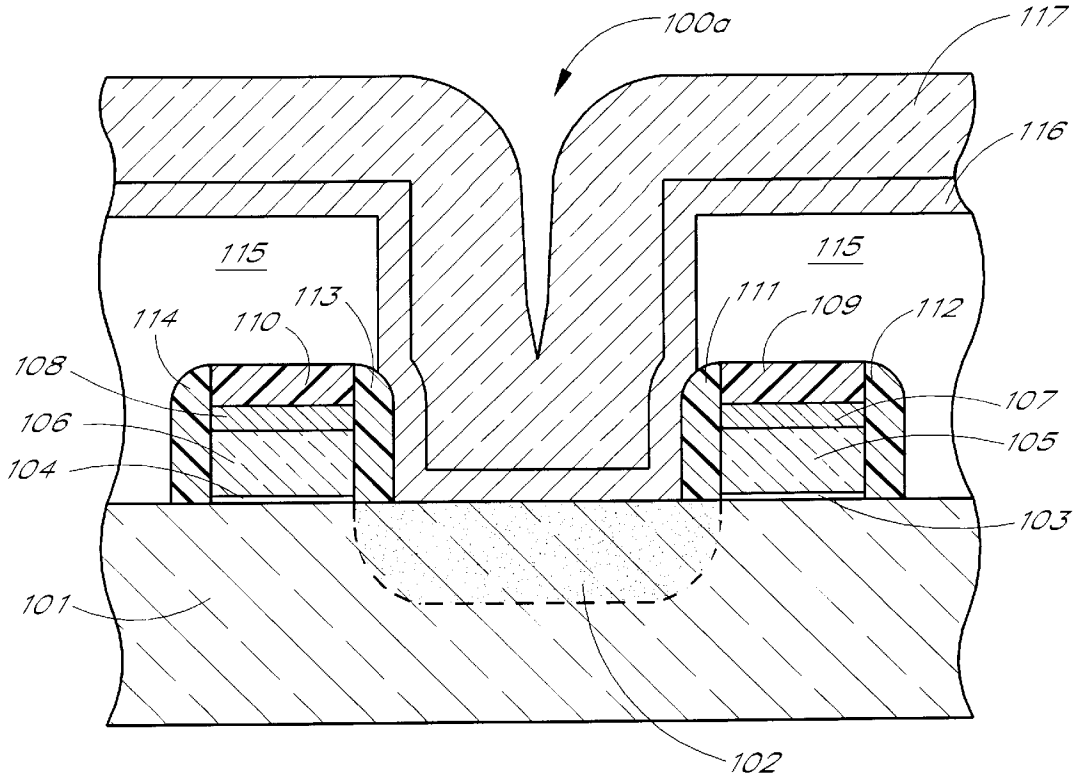
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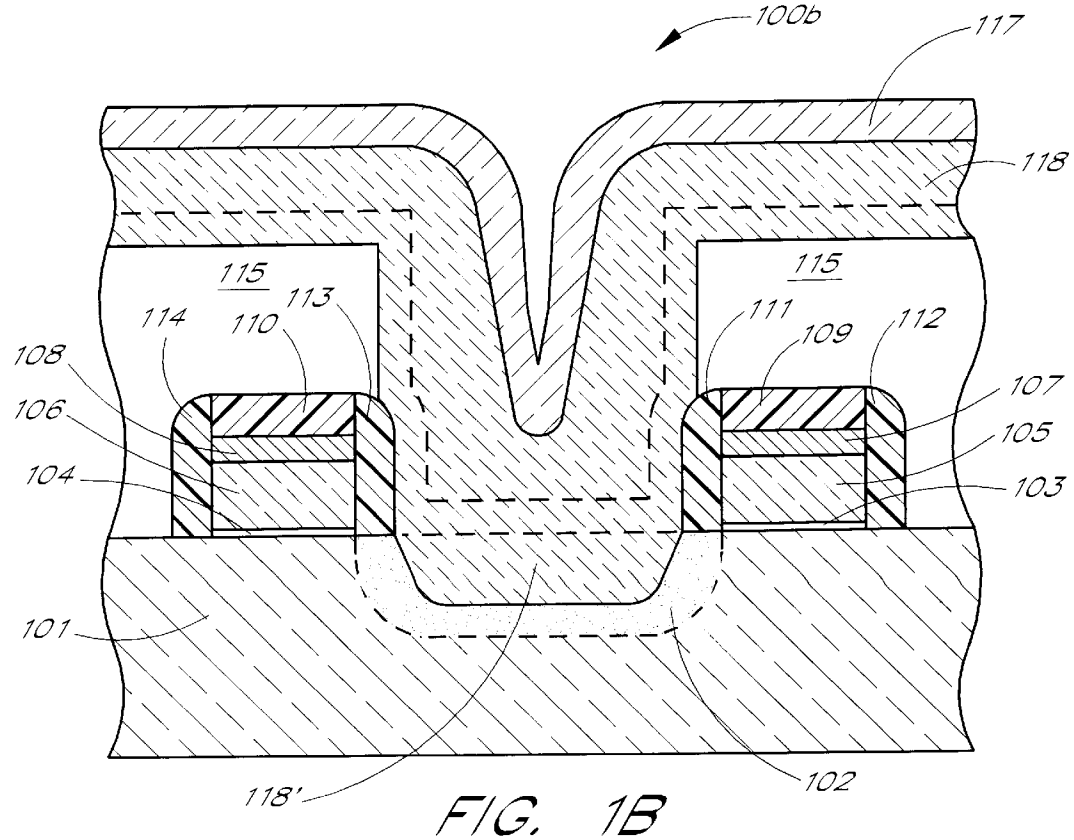
FIG. 1A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112
108
106
104
107
105
103
101
118'
102

FIG. 1B

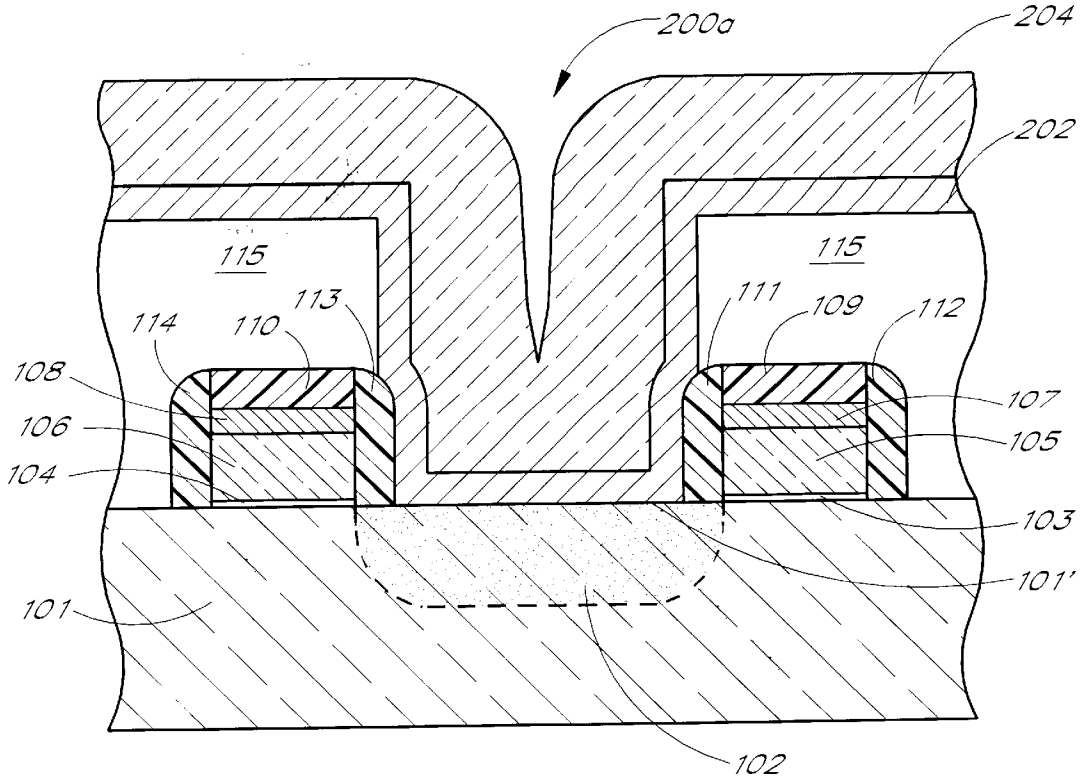
200a
204
202
115
115
113
111
114
110
109
112
108
107
106
105
104
103
101'
101
102

FIG. 2A

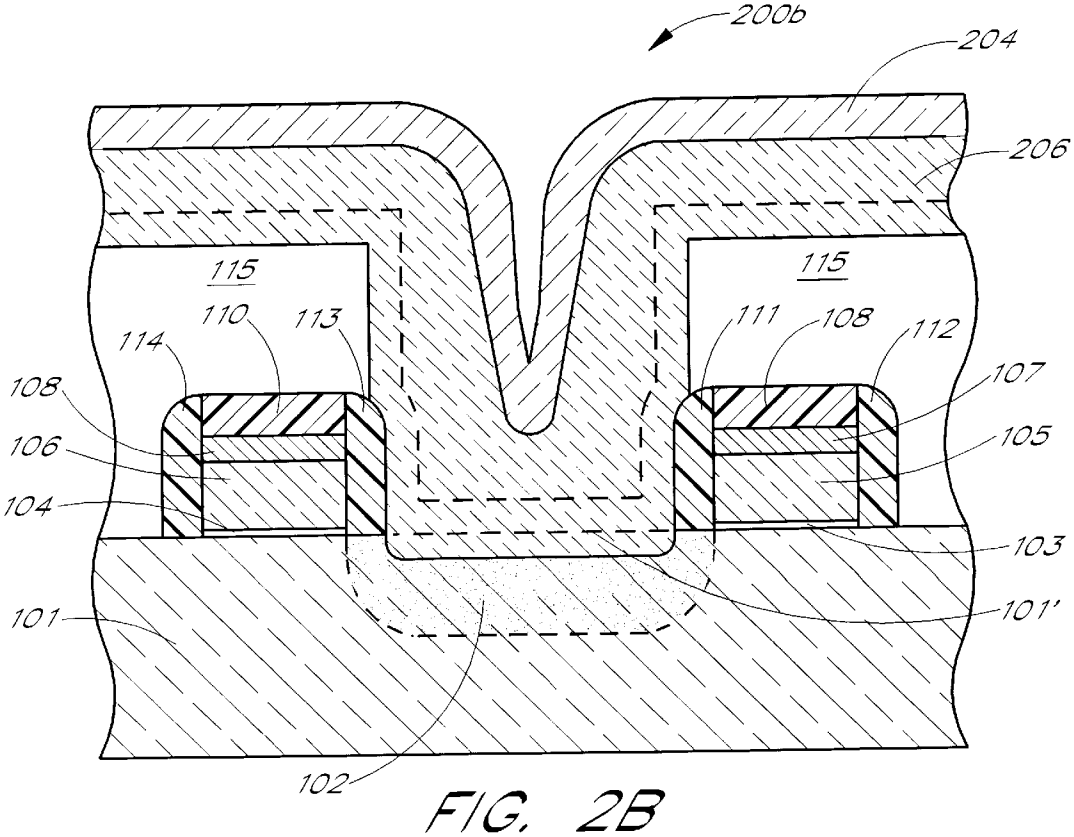
200b
204
206
115
115
110
113
111
108
114
112
108
107
106
105
104
103
101'
101
102

FIG. 2B

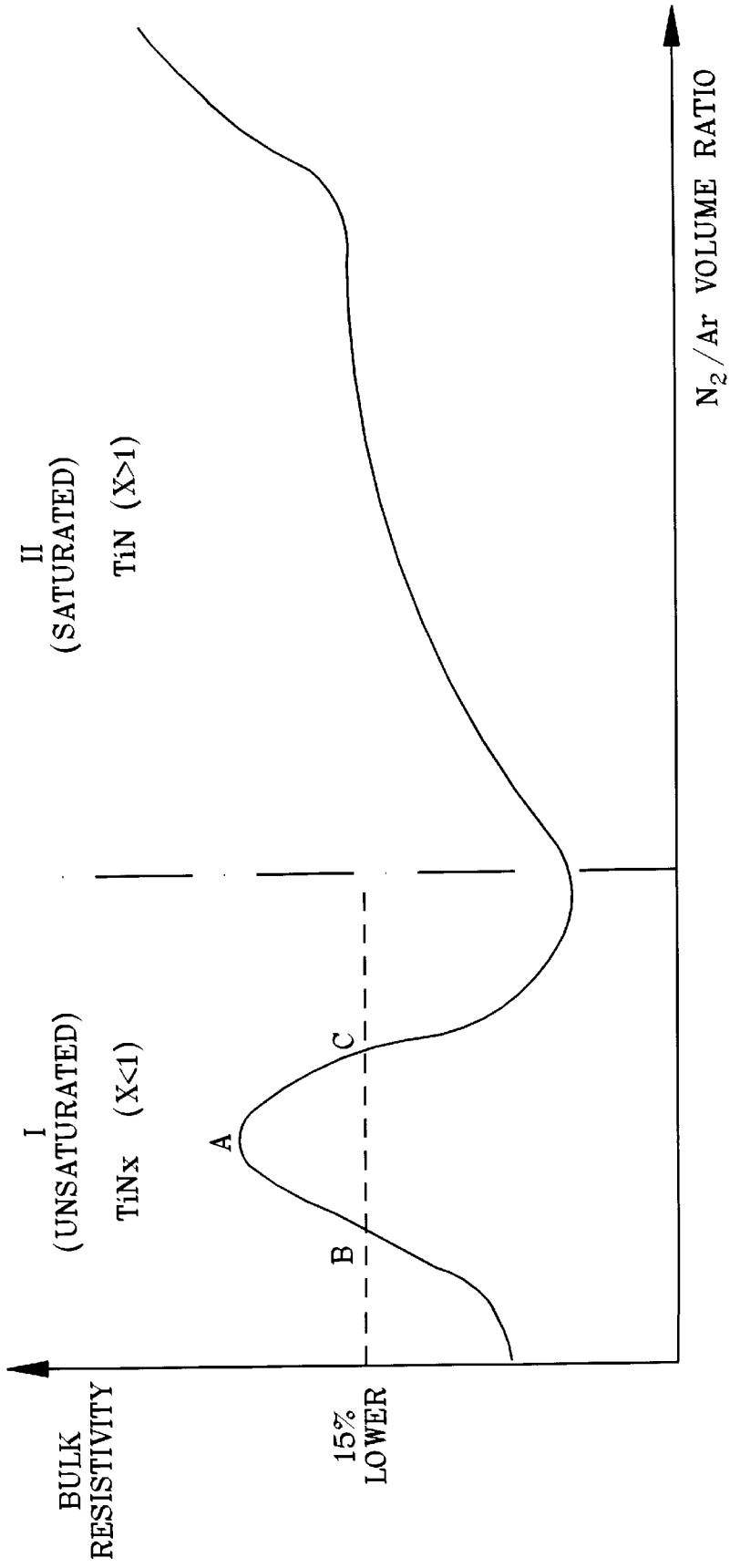
BULK RESISTIVITY
15% LOWER
I (UNSATURATED) TiNx (X<1)
II (SATURATED) TiN (X>1)
A
B
C
N_2/Ar VOLUME RATIO

FIG. 3

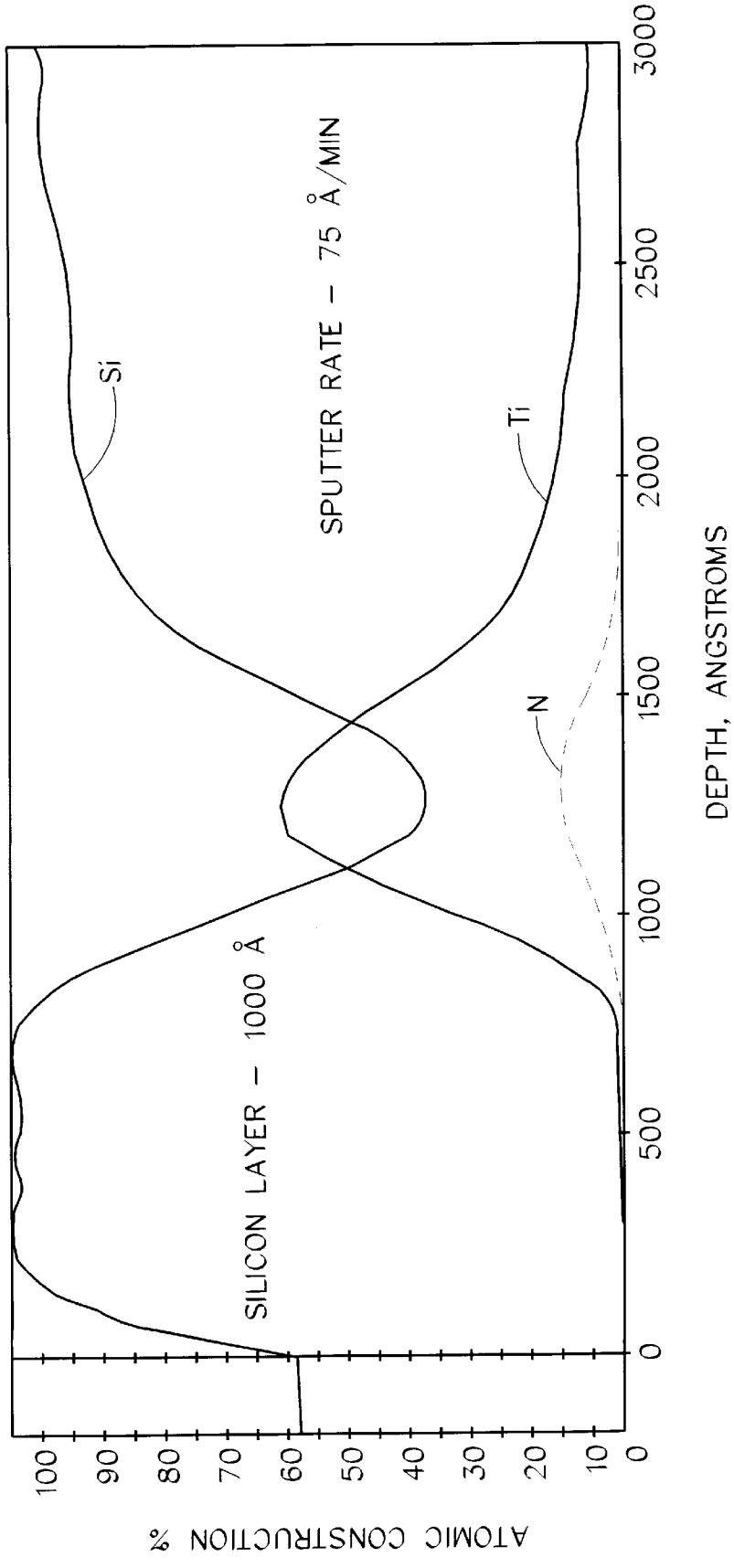
ATOMIC CONSTRUCTION %
100
90
80
70
60
50
40
30
20
10
0
0
500
1000
1500
2000
2500
3000
DEPTH, ANGSTROMS
SILICON LAYER – 1000 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N

FIG. 4A

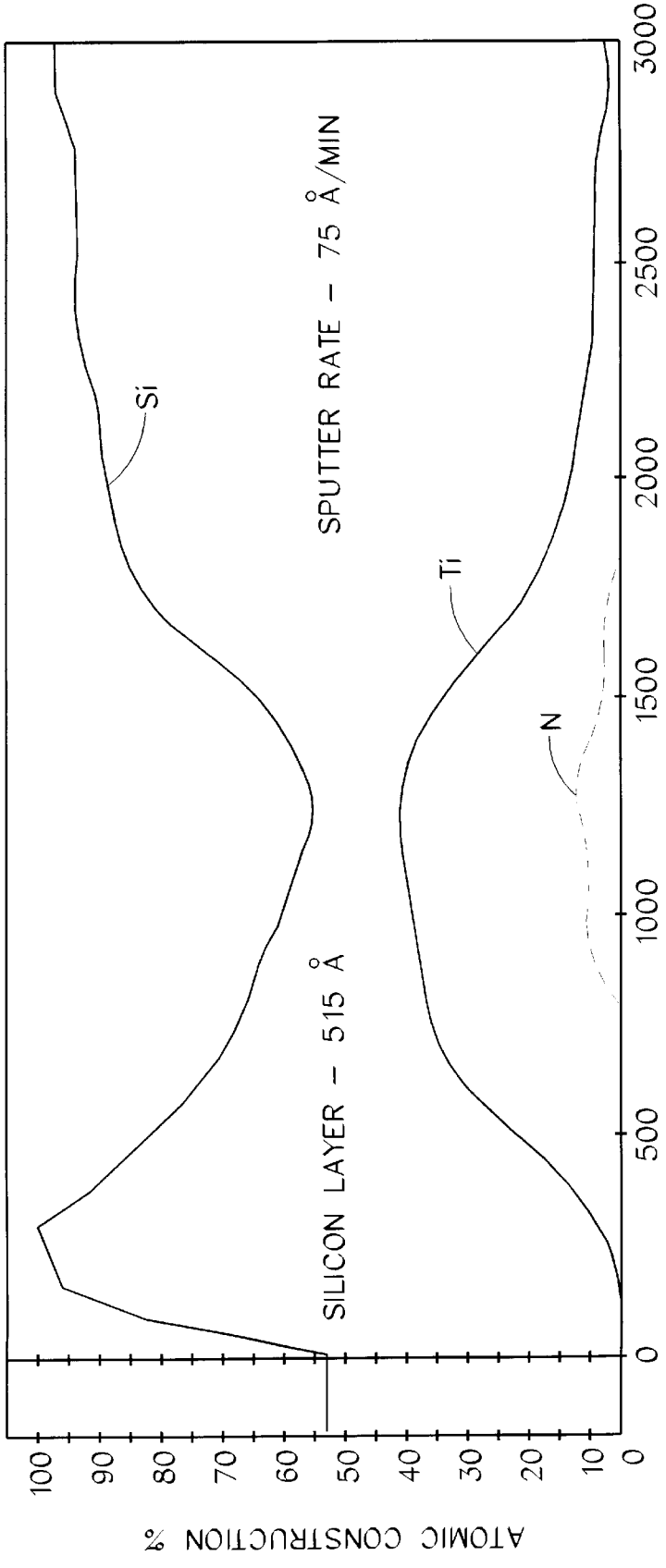
SILICON LAYER – 515 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N
ATOMIC CONSTRUCTION %
DEPTH, ANGSTROMS
0
10
20
30
40
50
60
70
80
90
100
0
500
1000
1500
2000
2500
3000

FIG. 4B

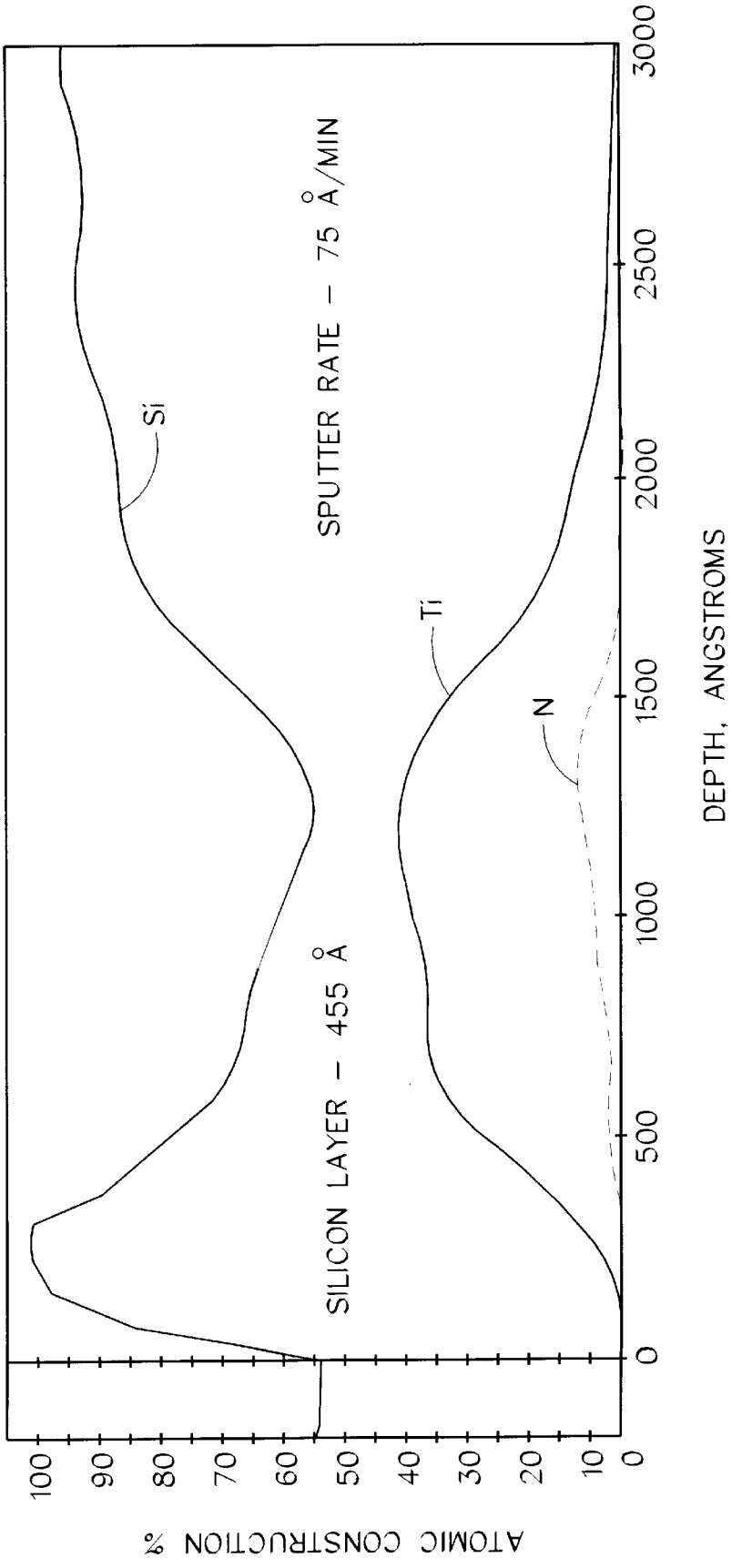
SPUTTER RATE – 75 Å/MIN
SILICON LAYER – 455 Å
Si
Ti
N
ATOMIC CONSTRUCTION %
DEPTH, ANGSTROMS
0
10
20
30
40
50
60
70
80
90
100
500
1000
1500
2000
2500
3000

FIG. 4C

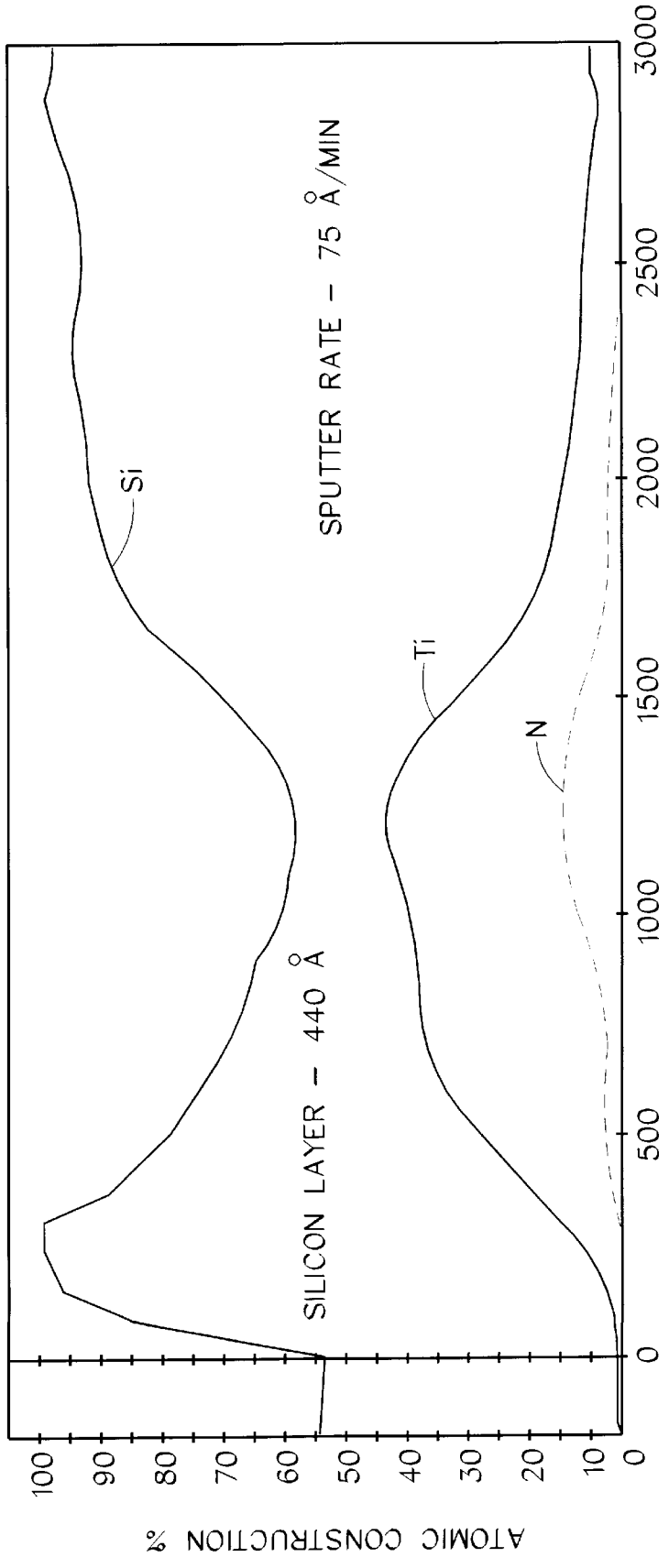
ATOMIC CONSTRUCTION %
100
90
80
70
60
50
40
30
20
10
0
0
500
1000
1500
2000
2500
3000
DEPTH, ANGSTROMS
SILICON LAYER – 440 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N

FIG. 4D

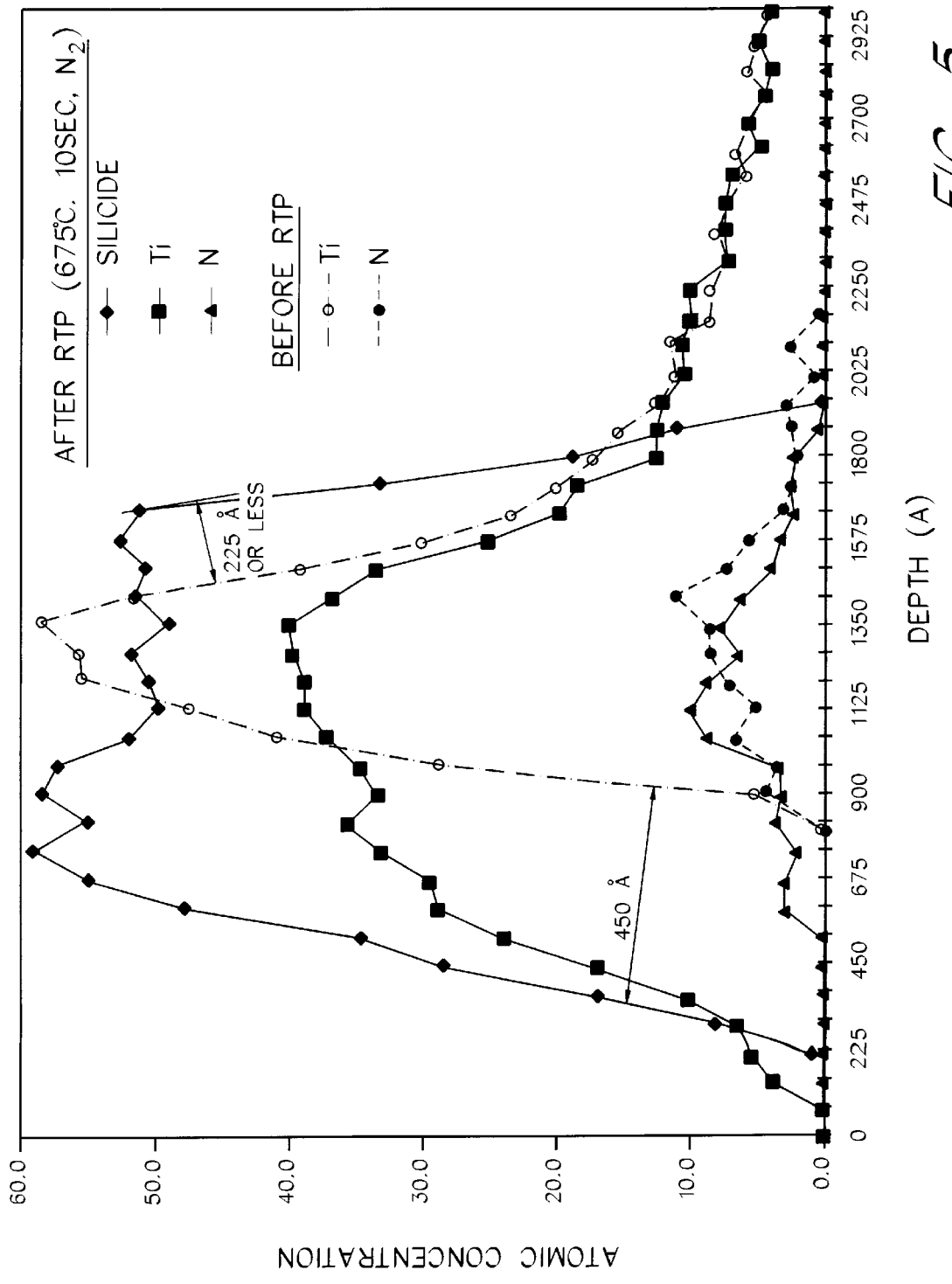
AFTER RTP (675C. 10SEC, N2)
SILICIDE
Ti
N
BEFORE RTP
Ti
N
225 Å OR LESS
450 Å
ATOMIC CONCENTRATION
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0
225
450
675
900
1125
1350
1575
1800
2025
2250
2475
2700
2925
DEPTH (A)

FIG. 5

FIG. 6A

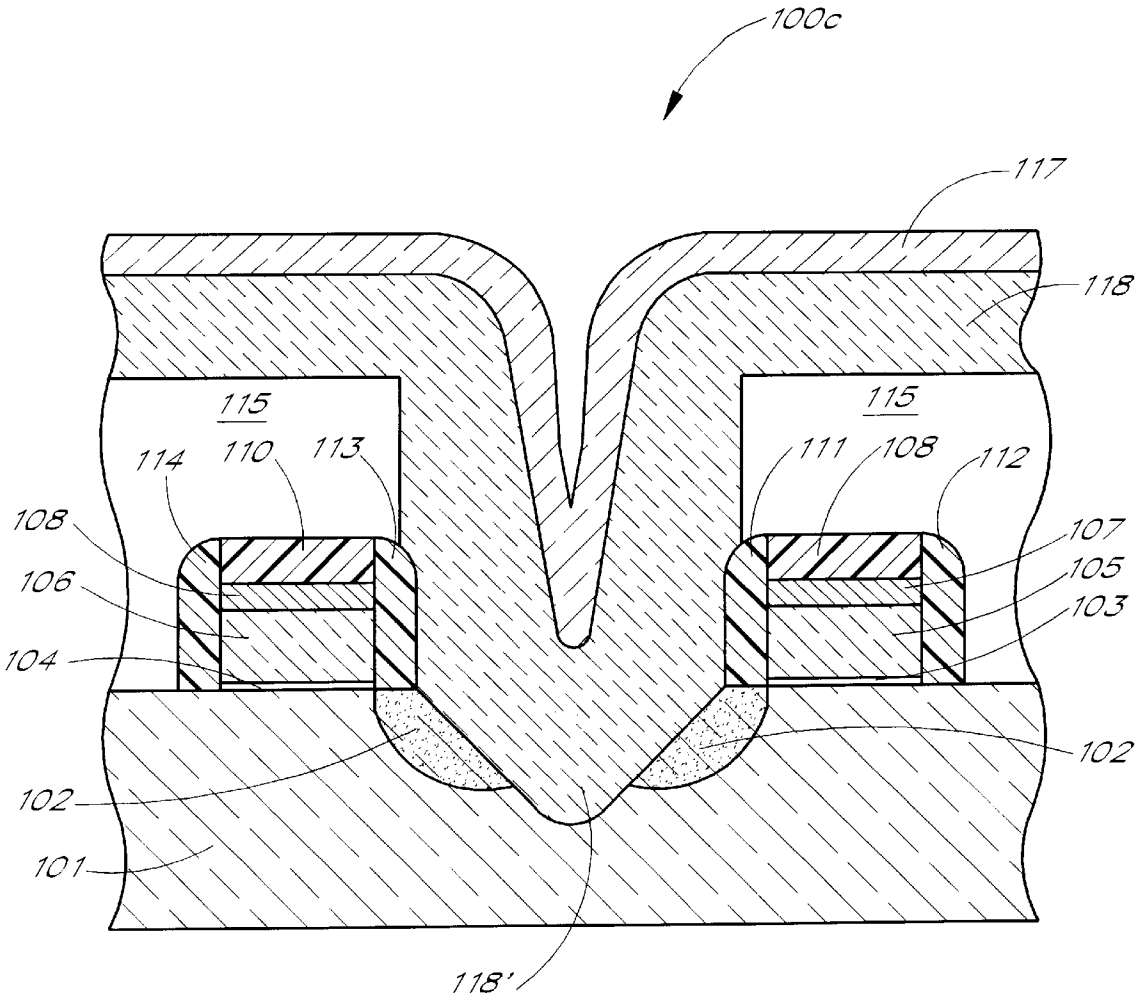
100c
117
118
115
115
114
110
113
111
108
112
108
106
104
107
105
103
102
102
101
118'

FIG. 6B

ASYMMETRIC, DOUBLE-SIDED SELF-ALIGNED SILICIDE AND METHOD OF FORMING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to fabrication of semiconductor circuit devices. More particularly, the present invention is directed to self-aligned silicide structures and methods of forming the same without excessive consumption of underlying silicon.

2. Description of Related Art

As is well known in processing integrated circuits, electrical contacts must be made among circuit nodes, such as isolated device active regions formed within a single-crystal silicon substrate. As the contact dimensions of devices become smaller, the contact resistance and the sheet resistance of the contacts increase. In this regard, refractory metal suicides have been used for local interconnections to provide low resistance electrical contacts between device active regions within the silicon substrate.

One common method of forming metal silicides is a self-aligned silicide process, often referred to as salicidation. A thin layer of refractory metal, such as titanium, is deposited over a dielectric area and through contact openings formed on the dielectric area to contact underlying silicon circuit elements, such as source and drain active regions formed within a silicon substrate. The structure is generally annealed to form a silicide, such as titanium silicide (predominantly $TiSi_2$) at a high temperature. During the anneal, the deposited titanium reacts with the silicon in the contact to form $TiSi_2$ at the contact openings. Titanium which overlies the dielectric area does not form $TiSi_2$, as the titanium does not contact any silicon. The process is referred to as "self-aligned" because the silicide is formed only where the metal layer contacts silicon, for example, through the contact openings. After the first annealing, the unreacted titanium may be removed in a wet etch, and a post-silicidation anneal is performed to lower the sheet resistance of the silicide to acceptable levels. The final annealing converts titanium silicide from the C49 phase to the lower resistance C54 phase. This self-aligned silicide is often referred to by the short form "salicide."

In the salicidation process, silicon from the contact regions of the substrate diffuses upward into the titanium layer. Similarly, titanium diffuses into the underlying active areas of the silicon substrate. Titanium and silicon react with each other to form a silicide thick enough to provide low sheet resistance. As a result, the doped active area of the silicon substrate becomes thinner due to the consumption of silicon during the reaction. The resultant silicide is said to intrude or sink into the substrate. Over-consumption of the underlying silicon can be problematic for any silicon circuit element, tending to cause voids, and thus device failures. Where contact is made to a shallow junction active area of a silicon substrate, salicide contacts of sufficient thickness cannot be formed without completely destroying a junction.

A need, therefore, exists for an interconnect and method of fabricating the same, which provides the advantages of salicide interconnects without excessive consumption of underlying silicon to which contact is made.

SUMMARY OF THE INVENTION

The aforementioned needs are satisfied by several aspects of the present invention.

In accordance with one aspect of the present invention, a method is provided for forming a self-aligned silicide contact on a silicon substrate. The method includes forming a contact window through an insulating layer over the silicon substrate, thereby exposing a portion of the silicon substrate. A metal nitride layer is deposited over the exposed portion of the silicon substrate. A silicon layer is formed over the metal nitride layer.

In accordance with another aspect of the present invention, a method is provided for forming a metal source layer, which incorporates a uniform distribution of an impurity and a metal, between silicon structures in an integrated circuit. The method includes selecting a sputtering ambient to maximize bulk resistivity for a metal-rich class of layers incorporating the impurity and the metal. A metallic target is sputtered in the selected ambient.

In accordance with another aspect of the present invention, a method is provided for forming a silicide interconnect over a silicon substrate. The method includes selecting a metal layer incorporating an impurity to a level below saturation. The metal layer has a bulk resistivity within about 15% of the maximal resistivity for unsaturated metal layers having the same metal and impurity. The selected layer is deposited over the silicon substrate, and the selected layer and the substrate ire sintered.

In accordance with another aspect of the present invention, a method is provided for forming a self-aligned silicide contact to a semiconductor substrate. The method includes opening a contact in an insulating layer to expose an active region of the substrate. A refractory metal source layer is deposited into the contact directly over the active region of the substrate. A silicon source layer is deposited directly over the refractory metal source layer. A silicidation is then performed to form the self-aligned silicide contact. The silicidation preferentially consumes silicon from the silicon source layer as compared to silicon from the substrate in a ratio of greater than about 1.2:1.

In accordance with another aspect of the present invention, an intermediate substrate assembly is provided. The assembly includes a silicon substrate, a metal nitride layer directly over the silicon substrate, and a silicon layer directly over the metal nitride layer. In accordance with a preferred embodiment, this intermediate assembly is sintered to form a silicide contact.

In accordance with another aspect of the present invention, an integrated circuit is provided, including a silicon substrate, an insulating layer formed over the silicon substrate with a contact opening formed in the insulating layer, and a conductive contact directly contacting the silicon substrate within the contact opening. The contact includes metal silicide uniformly interspersed with metal nitride.

In accordance with another aspect of the present invention, an integrated circuit includes a silicon substrate and a self-aligned contact. The contact includes a metal silicide, and the extends into the substrate below the upper surface of the substrate by an amount less than about 30% of the contact thickness.

In accordance with another aspect of the present invention, a self-aligned silicide contact is provided. The contact extends below a substrate surface into a shallow junction transistor active area, which has a junction depth of no more than about 1,000 Å. The contact extends below the substrate surface by no more than about 30% of the junction depth.

These and other features of the present invention will become more fully apparent from the following description and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A and **1**B are partial schematic sectional views of an integrated circuit, illustrating a double-sided salicidation. FIGS. **1**A and **1**B respectively show silicon substrate sub-assemblies before annealing and after annealing.

FIGS. **2**A and **2**B are partial schematic sectional views of an integrated circuit, illustrating self-aligned salicidation in accordance with a preferred embodiment of the present invention. FIGS. **2**A and **2**B, respectively, show silicon substrate assembly structures before annealing and after annealing.

FIG. **3** shows the bulk resistivity of a titanium nitride layer as a function of N_2/Ar volume ratio in a reactive sputtering of Ti to form TiN_x at a given target power.

FIG. **4** shows X-ray photoelectron spectroscopic ("XPS") profiles of integrated circuits constructed in accordance with the preferred embodiment. FIG. **4**A is a profile of an integrated circuit prior to annealing. FIGS. **4**B, **4**C, and **4**D are profiles of integrated circuits annealed at different temperatures.

FIG. **5** shows XPS curve-fitting results of FIGS. **4**A and **4**B.

FIG. **6**A shows a bit-line contact X-SEM result on an actual device which was run though furnace reflow. FIG. **6**B is a schematic sectional view of the integrated circuit of FIG. **1**B after furnace reflow.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the preferred embodiments are illustrated in the context of self-alignied silicide (or "salicide") contacts to active regions in silicon substrates, it will be recognized by one of skill in the art of semiconductor fabrication that the invention will have application whenever electrical contact to silicon elements is desirable. For example, salicide can be used in forming contact to silicon interconnects, gate electrodes or plugs. Furthermore, the term "substrate," as used in the present application, refers to one or more semiconductor layers or structures which include active or operable portions of semiconductor devices.

In general, one method of reducing substrate (or "silicon electrical element") consumption in forming self-aligned silicide wiring is to supply additional silicon to the process. For example, an intermediate silicon layer can be introduced between the silicon substrate and the titanium layer. The intermediate silicon layer provides the titanium layer with some or all of the silicon required in the salicidation.

With intermediate silicon, however, the titanium layer should be thick enough to consume all of the intermediate silicon in order for the silicide to be in contact with the underlying active area of the silicon substrate. Alternatively, the intermediate silicon layer must be doped to match the doping type of the contacted active region in order to ensure ohmic contact, forming "raised" source/drain regions. Such doping can require an additional mask and all the attendant processing steps. In the fabrication of CMOS circuits, which utilize complementary n-channel and p-channel devices, contacts require two marks for doping the different regions which contact p+ drains and n+ drains, respectively. Each of these masks is expensive both to create for different chip designs and to use in production.

Supplemental silicon can also be introduced over a metallic layer to provide silicon required to form silicide. FIG. **1**A, for example, illustrates a schematic sectional view of such a structure **100***a* formed on a silicon substrate **101**. A

highly doped silicon active area **102** is defined below a substrate surface **101'**. In the illustrated embodiment, the active area **102**, which may comprise a transistor source or drain, has an ultrashallow junction of no more than about 1,000 Å.

Two structures, such as gate structures in MOS devices, lie over silicon substrate **101** adjacent the active area **102**. Each of the gate structures has a thin gate oxide layer **103**, **104**, a polysilicon gate electrode layer **105**, **106**, a metallic layer **107**, **108**, and a protective cap layer **109**, **110**. Sidewall spacers **111**, **112**, **113**, **114** protect the gate stacks, and an insulating layer **115** (e.g., BPSG) covers the gate structures and the silicon substrate **101**. A window is opened onto the active area **102** through the insulating layer **115** in order to provide contact to the active area **102**. The contact window thus is defined by the insulating layer **115**, inner sidewall spacers **111**, **113**, and the active area **102**. A titanium layer **116** and a polysilicon layer **117** are deposited, in that order, into the contact window and over the insulating layer **115**. The deposition of polysilicon over titanium forms a sandwich-like structure inside the window, in which the metal layer **116** is interposed between the supplemental silicon (i.e., the polysilicon layer **117**) and the active area **102** of the silicon substrate **101**. This structure **100***a* allows titanium in the titanium layer **116** to diffuse into and consume silicon from both the underlying active area **102** and the overlying polysilicon layer **117** when it is annealed. This process can be referred to as "double-sided salicidation."

FIG. **1**B, for example, shows a structure **100***b* which is the result of annealing the structure **100***a* of FIG. **1**A. Over the insulating layer **115**, only the overlying polysilicon **117** provides silicon for the reaction. Inside the contact window, on the other hand, the reaction proceeds in both directions. Titanium consumes silicon from both the overlying polysilicon layer **117** and the underlying active area **102** to form a silicon-rich titanium silicide **118'** thick enough to present a low sheet resistance. While the titanium may diffuse at about a 10% higher rate in polysilicon than in monocrystalline silicon, the salicidation reaction is substantially symmetrical, consuming about the same amount of silicon from the substrate as from the overlying silicon **117**.

While the double-sided salicidation reaction described above is preferable to conventional salicide, double-sided salicide is not without its problems. For example, chemical vapor deposition ("CVD"), the most conmnon process for depositing polysilicon, does not easily form silicon over metallic layers, such as the titanium layer **116**. This is due to the fact that the silicon does not easily nucleate on metal surfaces. Even if a silicon layer of suitable thickness can be formed over the titanium layer **116**, double-sided salicidation may still consume too much of the silicon substrate **101**, or result in too thin a silicide to provide a low enough sheet resistance.

FIG. **2** depicts schematic sectional views of a silicon substrate assembly structure in accordance with a preferred embodiment of the present invention. Referring to FIG. **2**A, an intermediate structure **200***a* is illustrated, in which a contact window is opened through an insulating layer **115** to expose an active area **102** of a silicon substrate **101**. As the gates structures and insulating layer can be similar to those of FIG. **1**A, like reference numerals will be used to refer to like parts.

A metal source layer **202**, having an impurity therein, is deposited over the insulating layer **115** and the active area **102** through the contact window. Preferably, the impurity comprises nitrogen, and the metal source layer **202** com-

prises a metal-rich nitride. Most preferably, the metal source layer **202** comprises titanium-rich titanium nitride of the form TiN_x (x<1). Preferably x is between about 0.2 and 0.8, and most preferably between about 0.5 and 0.6. Methods of forming the preferred TiN_x layer **202** will be discussed in greater detail below. The metal layer **202** is preferably between about 50 Å and 800 Å, more preferably between about 300 Å and 400 Å. While the layer **202** is not pure metal, it may be referred to as a metal layer for convenience.

A silicon source layer **204** is deposited over the metal source layer **202**. As a result, the TiN_x layer **202** is interposed between the active area **102** of the silicon substrate **101** and the silicon source layer **204**, forming a sandwich structure. The silicon source layer **204**, which may comprise amorphous or polycrystalline silicon, is preferably between about 100 Å and 10,000 Å, more preferably about 1,000 Å. While in other arrangements the silicon source layer need not be purely silicon, the preferred layer **204** simply consists of polysilicon.

After forming the silicon layer **204** over the metal source layer **202**, the silicon **204** is preferably patterned, by conventional photolithography and silicon etch, in accordance with circuit design for the interconnect layer. Silicon **204** is thus left over the metal source layer **202** only where silicide interconnect is desired.

The structure **200***a* is then subjected to an anneal, preferably at between about 500° C. and 850° C., and more preferably between about 650° C. and 750° C., in a nitrogen ambient. During the annealing, metal and impurity atoms in the metal source layer **202** diffuse into the underlying active area **102** of the silicon substrate **101** and the overlying silicon layer **204**. Likewise, silicon diffuses into the metal source layer **202** from the underlying active area **102** and the overlying silicon layer **204**. Elementary titanium reacts with silicon from both sides and forms a titanium silicide, such that the process is a double-sided salicidation.

FIG. **2**B shows a structure **200***b* which is formed by annealing the structure **200***a* of FIG. **2**A. A silicide **206** is formed, comprising titanium nitride and titanium silicide. The resulting salicide layer **206** has sufficient thickness to provide low sheet resistance, preferably less than about 200 $\mu\Omega$.cm. The titanium silicide layer **206** preferably has a thickness greater than about 200 Å, more preferably greater than about 300 Å, and most preferably greater than about 500 Å.

After silicide formation, unreacted metal can be removed in a selective metal wet etch, as will be reorganized by one of ordinary skill in the art. Thus, where silicon had been removed in the pre-silicidation patterning, described above, unreact metal can be washed away.

Significantly, the salicidation does not consume the same amount of silicon from the underlying active area **102** and the overlying silicon layer **204**. The consumption of the underlying silicon area **102** is less than that of the overlying silicon layer **204**. In particular, salicidation of the preferred TiN_x layer **202** preferentially consumes overlying silicon relative to underlying silicon in a ratio of greater than about 1.2:1, more preferably greater than 2:1, and most preferably about 3:1. The salicidation occurs asymmetrically and thus does not destroy a shallow junction formed within the silicon substrate **101**. Accordingly, the portion of the self-aligned silicide **206** sinking below the surface of the substrate **102** represents less than about 30% of the total silicide thickness within the contact, preferably less than about 20%.

Preferably, the silicide **206** extends or intrudes below the original surface **101**' of the active area **102** by less than about 30% of the ultrashallow junction depth (e.g., less than about 300 Å of a 1,000 Å junction is consumed), more preferably less than about 25%, such that the transistor remains operable. It will be understood that, in other arrangements, the substrate surface from which the contact intrusion is measured can be that of a raised source/drain surface, and need not be coincident with the surface of a single crystal silicon wafer as shown.

It has been found that maximizing the bulk resistivity of the metal source layer **202** maximizes the asymmetry of silicide growth from the structure **200***a* of FIG. **2**A. In turn, the salicide method discussed above results in the maximum silicide thickness for a given amount of substrate consumption.

The metal source layer **202** can be formed by any of a number of techniques. For example, a metal layer can be doped with impurities after deposition, by diffusion or implantation techniques. Preferably, however, the metal source layer **202** is formed incorporating impurities during formation and most preferably during sputtering, although one of skill in the art can apply CVD methods in light of the present disclosure.

FIG. **3** relates to a preferred method for choosing an optimal region for sputtering of Ti in a N_2 and Ar ambient, thereby forming a TiN_x layer. Bulk resistivity of a titanium nitride layer is plotted as a function of N_2/Ar volume ratio in the reactive sputtering of Ti to form TiN_x at a given target power. As FIG. **3** illustrates, reactive sputtering of Ti falls into two main regions or realms. Sputtering with N_2/Ar ratio within Region I results in an unsaturated or titanium-rich titanium nitride of the form, TiN_x (x<1), while sputtering within Region II results in a saturated or standard TiN. Point A thus represents the flow ratio for which the highest bulk resistivity titanium-rich TiN_x is achieved, which, in turn, reflects a highly uniform distribution of nitride nuclei throughout Ti film. Beyond this point, nuclei begin to grow and eventually contact one another, causing bulk resistivity to drop. Then the saturated region or Region II begins, wherein no titanium is available for salicidation. Resistivity again rises within this region as excess nitrogen interferes with conductivity. Points B and C represent lower and higher flow ratios, respectively, which result in a TiN_x film of about 15% lower bulk resistivity than a film formed at peak A. This range of ratios represents a preferred processing window.

Absolute ratios in FIG. **3** depend upon the sputtering power. For example, with 2.0 kW sputtering power, 35 sccm of Ar and 7–8 sccm of N_2 result in a maximum Region I resistivity of about 270 $\mu\Omega$-cm. The TiN_x resulting from this N_2/Ar ratio has x approximately equal to 0.6. Increasing sputtering power gives smaller TiN_x nucleates, and reducing power gives larger TiN_x nucleates. Higher sputtering power thus flattens out the peak A. It will be understood, in light of the present disclosure, that at higher sputter power, a larger window of preferred N_2/Ar ratios is available. In general, sputtering with a ratio closer to point A results in a better the TiN_x distribution uniformity, which in turn results in greater salicide thickness uniformity after silicidation. Typically, x is around 0.5 or 0.6 at point A. It can be 0.2 to 0.8 between point B to point C when higher or lower sputtering power is used.

FIGS. **4**A to **4**D illustrate X-ray photoelectron spectroscopic profiles of integrated circuits of the present invention, illustrating the consumption of silicon from the active area **102** of the silicon substrate **101** and the overlying silicon layer **204**. Wafers of silicon assembly structures having 1,000 Å α-Si/400 Å TiN_x/Si substrate and 1,000 Å α-Si/300

Å TiN_x/Si substrate were subjected to rapid thermal processing ("RTP") at different temperatures. The metal source layers **202** of the wafers were deposited by reactively sputtering a titanium target at the N_2/Ar ratio of point A, as described above. X-ray photoelectron spectroscopic ("XPS") profiles for 1000 Å α-Si/400 Å TiN_x/Si substrate structures are shown.

FIG. **4**A is a profile of the sandwich structure prior to annealing. At the center of FIG. **2**A, titanium and nitrogen atoms forming the preferred metal source layer **202** are shown between silicon-rich areas. Trace elements are omitted.

FIG. **4**B is a profile for the structure annealed at 675° C. for 10 seconds. About 515 Å of silicon remains after the RTP. FIG. **4**C and **4**D are profiles of similar structures annealed at 710° C. and 790° C., respectively, for 20 seconds each. As can be seen in the FIGS. **4**B to **4**D, titanium is found asymmetrically toward Lhe left of the profile (representing points above the substrate) after the anneal. Total atomic percentage analysis results reveal asymmetric characteristic of double-sidled salicide formation at temperatures from 675° C. to 790° C. Clearly, salicide formation consumes more of the silicon source layer (α-Si or poly-Si) deposited over the metal source layer than silicon substrate below the metal source layer. The titanium salicide profiles remain stable between 675° C. and 790° C. The profiles of a sandwich structure using 300 Å of TiN_x as the metal source layer are similar to the profiles shown in FIGS. **4**A to **4**D, except that they consume even less (about 20% less) of the silicon substrate.

FIG. **5** shows curve-fitting results of the X-ray photoelectron spectroscopy profiles of FIGS. **4**A and **4**B to quantitatively analyze the degree of asymmetry of the preferred double-sided salicidation. As can be seen, the salicidation of titanium consumes the overlying silicon layer **204** at least twice as much as it consumes the silicon substrate **101**. A comparison of the titanium profile prior to anneal with the silicide profile after anneal shows consumption of less than 225 Å of the silicon substrate **101** (represented by a shift to the right), whereas about 450 Å of the overlying silicon layer **204** (represented by a shift to the left) is consumed. For the process using 300 Å of TiN_x, not shown, consumption of the substrate is down to 180 Å. This low consumption (representing less than 25% and even less than 20% with use of 300 Å of TiN_x layer) is very important for ultrashallow junction applications. For 750–1,000 Å junctions, the source/drain contact should preferably consume less than about 300 Å, more preferably less than about 250 Å, of silicon substrate to reduce leakage. At the same time, the salicide total thickness is preferably at least about 300 Å, more preferably at least about 500 Å, to form sufficiently low contact resistance, thermally and dynamically stable in the face of post-silicidation anneal (converting the grain to C54 orientation) and other high temperature processes.

As also apparent from FIGS. **4** and **5**, the resultant metal silicide contact contains the impurity which was incorporated into the metal source layer. In particular, nitrogen is present in the titanium silicide layer, preferably comprising between about 5% and 80% of the silicide layer **206** (FIG. **2**B), more preferably comprising about 10% to 30%, and most preferably in the range of about 15% to 20%. The XPS profiles of FIG. **4** indicate a slightly lower percentage of nitrogen than actual, due to preferential readings by the measuring apparatus.

Referring to FIGS. **6**A and **6**B, a conventionally-formed self-aligned silicide contact is shown after a high temperature glass reflow, typically conducted at about 750° C. for about 10 minutes. FIG. **6**A shows an X-SEM of an actual device after furnace reflow, where the contact was formal by sintering a sandwich structure with 300 Å pure titanium between a silicon substrate and a 1,000 Å polysilicon layer. The wafer was run through the entire device fabrication process flow, including furnace reflow at 750° C., after forming the salicide contact. As can be seen in FIG. **6**A, a silicide crater can be found after reflow at 750° C. The crater is more than 1,000 Å deep, such that an ultrashallow junction would be destroyed. FIG. **6**B schematically illustrates the structural deformation. The structure **100***b* of FIG. **1**B is shown after furnace reflow. The structure **100***c* of FIG. **6**B shows that a part of silicide **118'** extends even further into the active area **102** after reflow.

In contrast, actual devices were constructed in accordance with the preferre d embodiment, and put through furnace reflow at different temperatures. X-SEM results showed no such crater on wafers processed with either 300 Å TiN_x or **400** Å TiN_x layers. The $TiSi_x$/Si interface remained smooth and intact. The crater in salicide contacts formed conventionally is believed to be associated with tendency of $TiSi_x$ large grain formation to reduce surface energy and effect of agglomeration at high temperature. Formation of excessively large grains is drastically suppressed by the preferred embodiments, however, by incorporating TiN_x nuclei into $TiSi_x$ film.

The intermediate assembly structure having a TiN_x ($x<1$) layer and a silicon layer (see FIG. **2**A) over the silicon substrate enables asymmetric salicidation (FIG. **2**B). The asymmetric salicidation enables self-aligned formation of silicides thick enough to provide low contact resistance, while consuming less than about 300 Å, more preferably less than 250 Å, of the silicon substrate. The process preferably consumes greater than 1.2, more preferably greater than 2 times more silicon from the overlying silicon layer than from silicon substrate. This asymmetric salicidation facilitates self-aligned contact metallization for an ultrashallow junction (<1,000 Å), consuming less than 30% and preferably less than about 20% of the junction while providing adequately low resistivity contacts. This unique titanium silicide contact also has a much higher thermal stability than conventionally-formed self-aligned silicide.

Although the foregoing invention has been described in terms of certain preferred embodiments, other embodiments will become apparent to those of ordinary skill in the art, in view of the disclosure herein. Accordingly, the present invention is not intended to be limited by the recitation of preferred embodiments, but is instead intended to be defined solely by reference to the appended claims.

I claim:

1. An integrated circuit comprising:

a silicon substrate;

an insulating layer formed over the silicon substrate with a contact opening formed in the insulating layer; and

a conductive contact directly contacting the silicon substrate within the contact opening, the contact comprising metal silicide interspersed with metal nitride throughout the metal silicide, including at a substrate-silicide interface.

2. The integrated circuit as defined in claim **1**, wherein the contact comprises titanium.

3. The integrated circuit as defined in claim **1**, wherein a nitrogen content of the contact is between about 5% and 80%.

4. The integrated circuit as defined in claim **3**, wherein a nitrogen content of the contact is between about 10% and 30%.

5. The integrated circuit as defined in claim 4, wherein a nitrogen content of the contact is between about 15% and 20%.

6. The integrated circuit as defined in claim 1, wherein the contact intrudes into the substrate by an amount representing less than about 20% of the total contact thickness.

7. The integrated circuit as defined in claim 3, further comprising a metal silicide interconnect formed over the insulating layer, the interconnect continuous with the metal silicide contact.

8. An integrated circuit comprising:

a silicon substrate having an upper surface; and

a self-aligned contact comprising a metal silicide layer, having a metal silicide thickness,

the metal silicide layer extending into the substrate below the upper surface of the substrate by an amount less than about 30% of the metal silicide thickness, wherein the metal silicide layer includes a metal nitride interspersed therein.

9. The integrated circuit of claim 8, wherein the metal silicide layer extends into the substrate below the upper surface of the substrate by an amount less than about 20% of the metal silicide thickness.

10. The integrated circuit of claim 8, wherein the metal silicide layer extends into the substrate below the upper surface of the substrate by less than about 250 Å.

11. The integrated circuit of claim 8, wherein the nitrogen content of the metal silicide layer is between about 10% and 30%.

12. The integrated circuit of claim 8, wherein the silicon surface overlies a source/drain active area having a junction depth of no more than about 1,000 Å, and the contact extends into the active area to a depth less than about 30% of the junction.

13. The integrated circuit of claim 8, wherein the metal silicide layer has a sheet resistance of less than about 200 $\mu\Omega$.cm.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,147,405
DATED : November 14, 2000
INVENTOR(S) : Yongjun Jeff Hu

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2,
Line 24, please replace "ire" with -- are --.

Column 8,
Line 16, please replace "preferre d" with -- preferred --.

Signed and Sealed this

Eleventh Day of March, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

EXHIBIT C

US006358801B1

(12) **United States Patent**
Fazan et al.

(10) **Patent No.: US 6,358,801 B1**
(45) **Date of Patent: *Mar. 19, 2002**

(54) **METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/644,282**

(22) Filed: **Aug. 22, 2000**

Related U.S. Application Data

(62) Division of application No. 09/032,231, filed on Feb. 27, 1998, now Pat. No. 6,107,157.

(51) **Int. Cl.**[7] **H01L 21/336**; H01L 21/76
(52) **U.S. Cl.** **438/270**; 438/296; 438/424
(58) **Field of Search** 438/270, 296, 438/424

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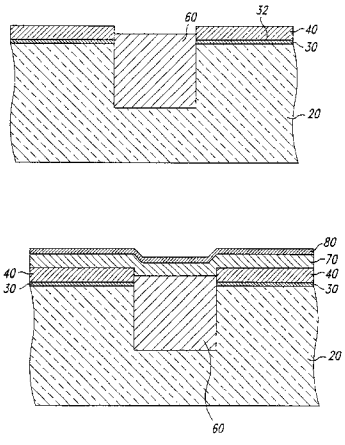
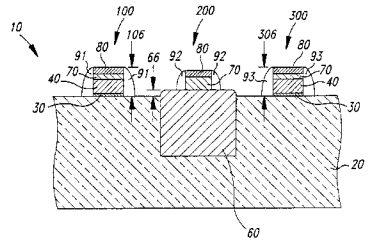
Assistant Examiner—Josetta I. Jones
(74) *Attorney, Agent, or Firm*—Dorsey & Whitney LLP

(57) **ABSTRACT**

A microelectronic device includes a field oxide isolation pad which extends from a trench formed in a microelectronic substrate by a height which is less than approximately two times the height of a gate structure formed on the microelectronic substrate. Spacers are formed around the gate structures, although little or no spacer forms around the isolation pad. The microelectronic device is fabricated by forming a gate oxide layer on a microelectronic substrate, depositing a first gate layer on the gate oxide layer, forming a trench extending through the gate layer, the gate oxide layer and into the substrate, filling the trench with a field oxide, planarizing the field oxide, recessing the field oxide to a level above the microelectronic substrate and below an upper level of the first gate layer, forming a second gate layer over the recessed field oxide and the first gate layer, forming a conductive layer over the second gate layer, forming gate structures in the conductive layer, the first and second gate layers, and the gate oxide layer, and forming spacers adjacent the gate structures.

38 Claims, 5 Drawing Sheets





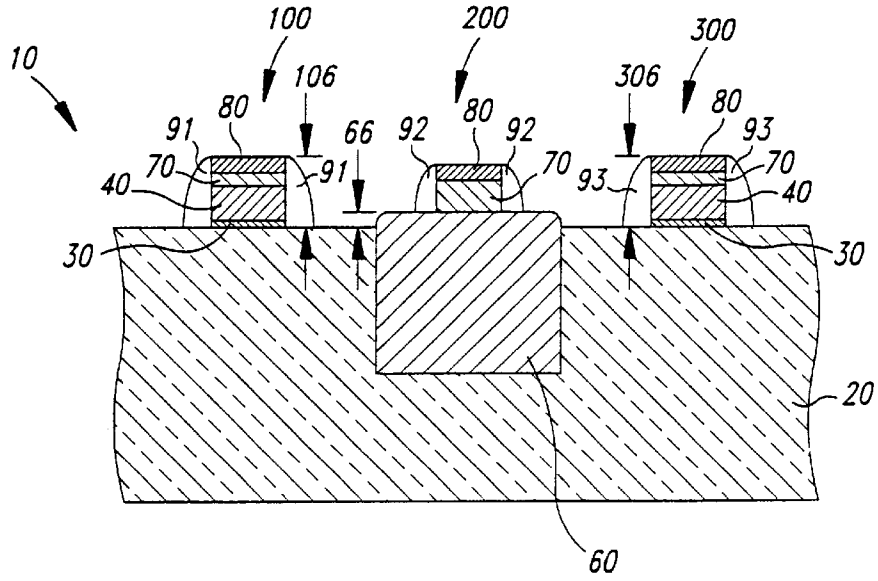


Fig. 2H

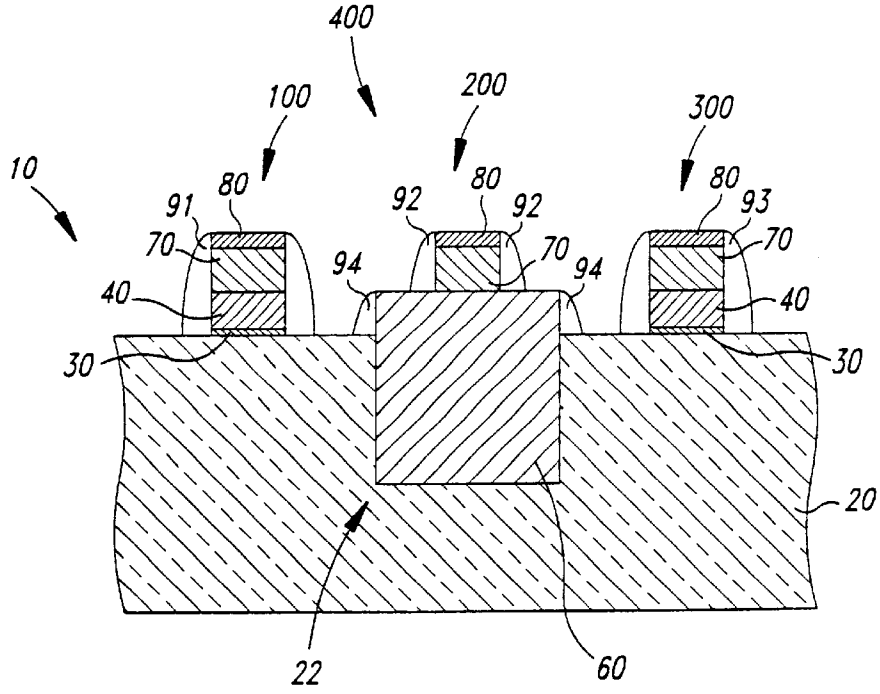


Fig. 1
(PRIOR ART)

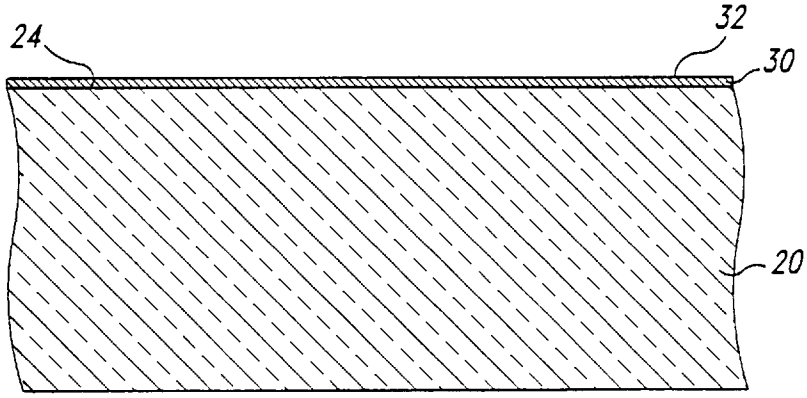


Fig. 2A

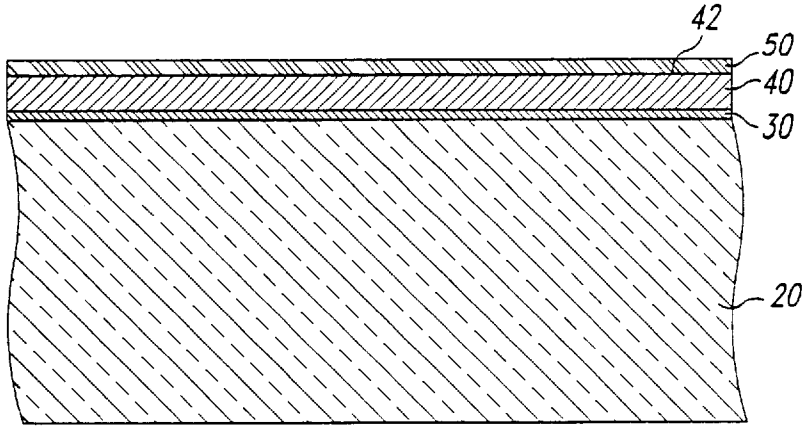


Fig. 2B

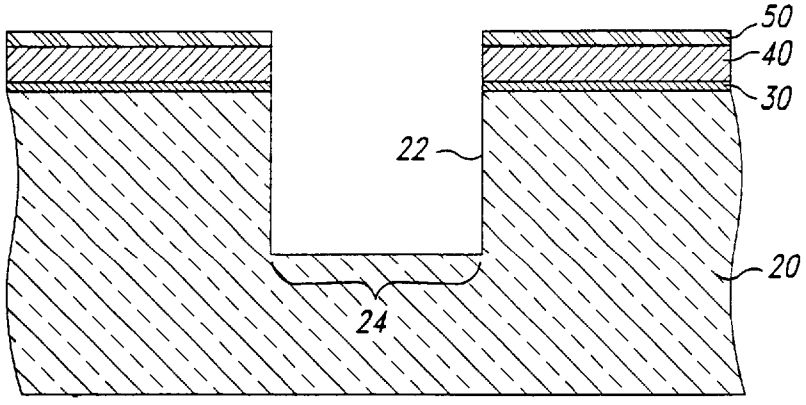


Fig. 2C

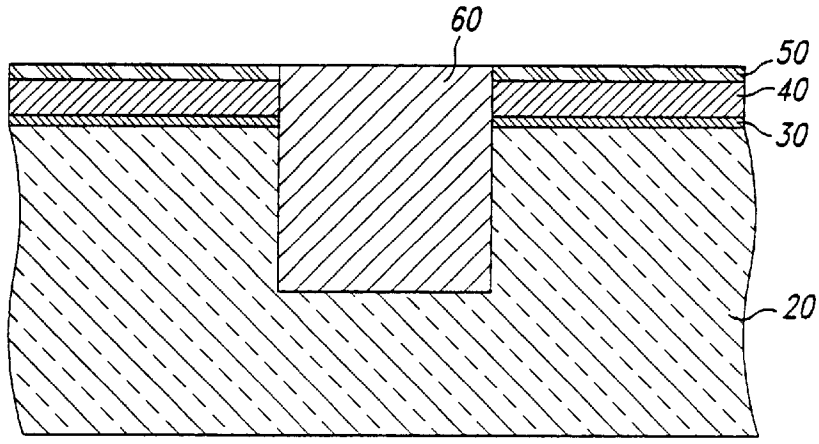


Fig. 2D

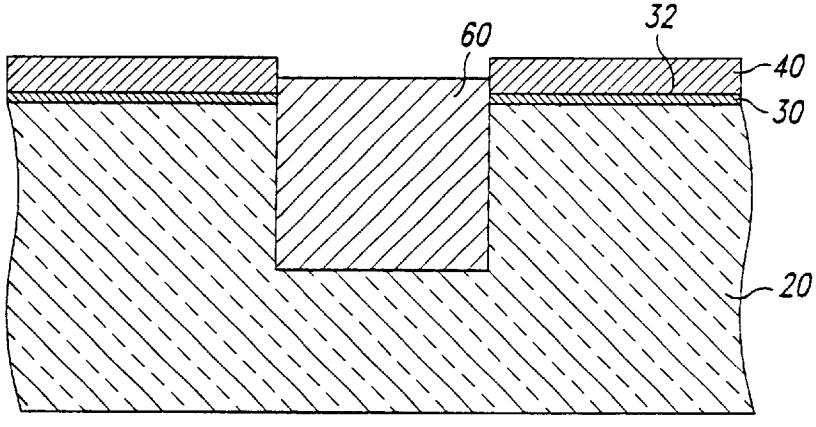


Fig. 2E

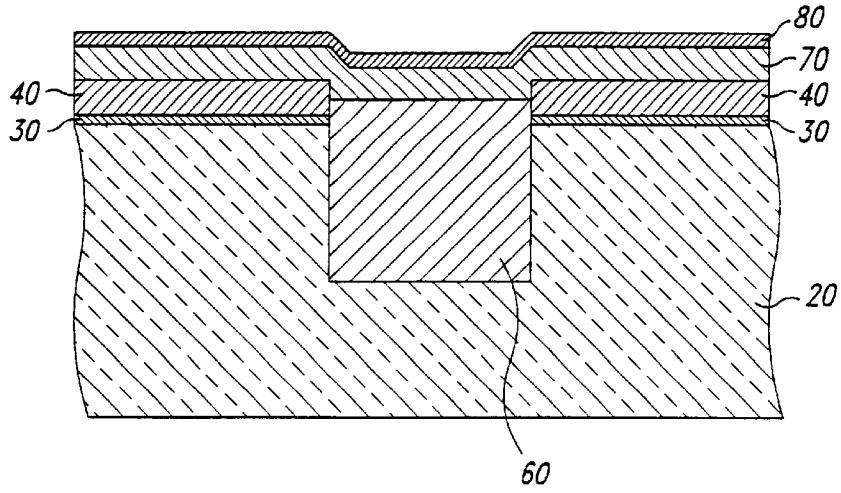

80
70
40
30
40
30
20
60

Fig. 2F

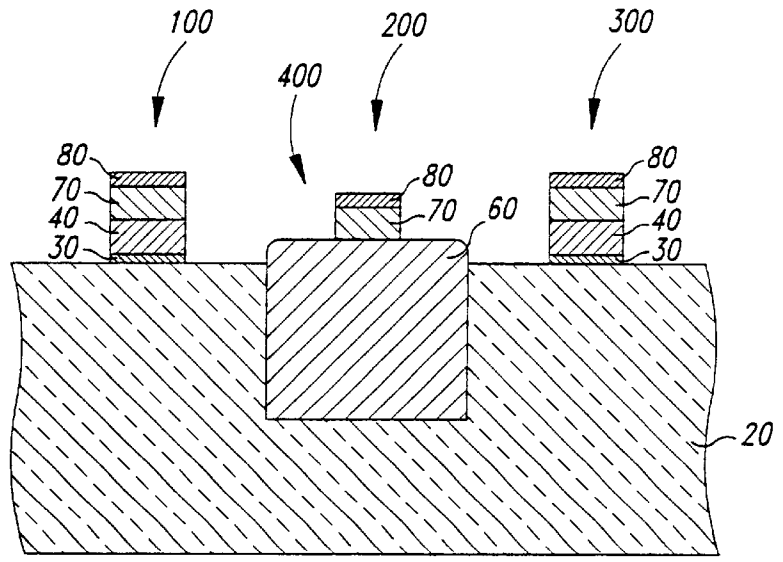

100
200
300
400
80
70
40
30
80
70
60
80
70
40
30
20

Fig. 2G

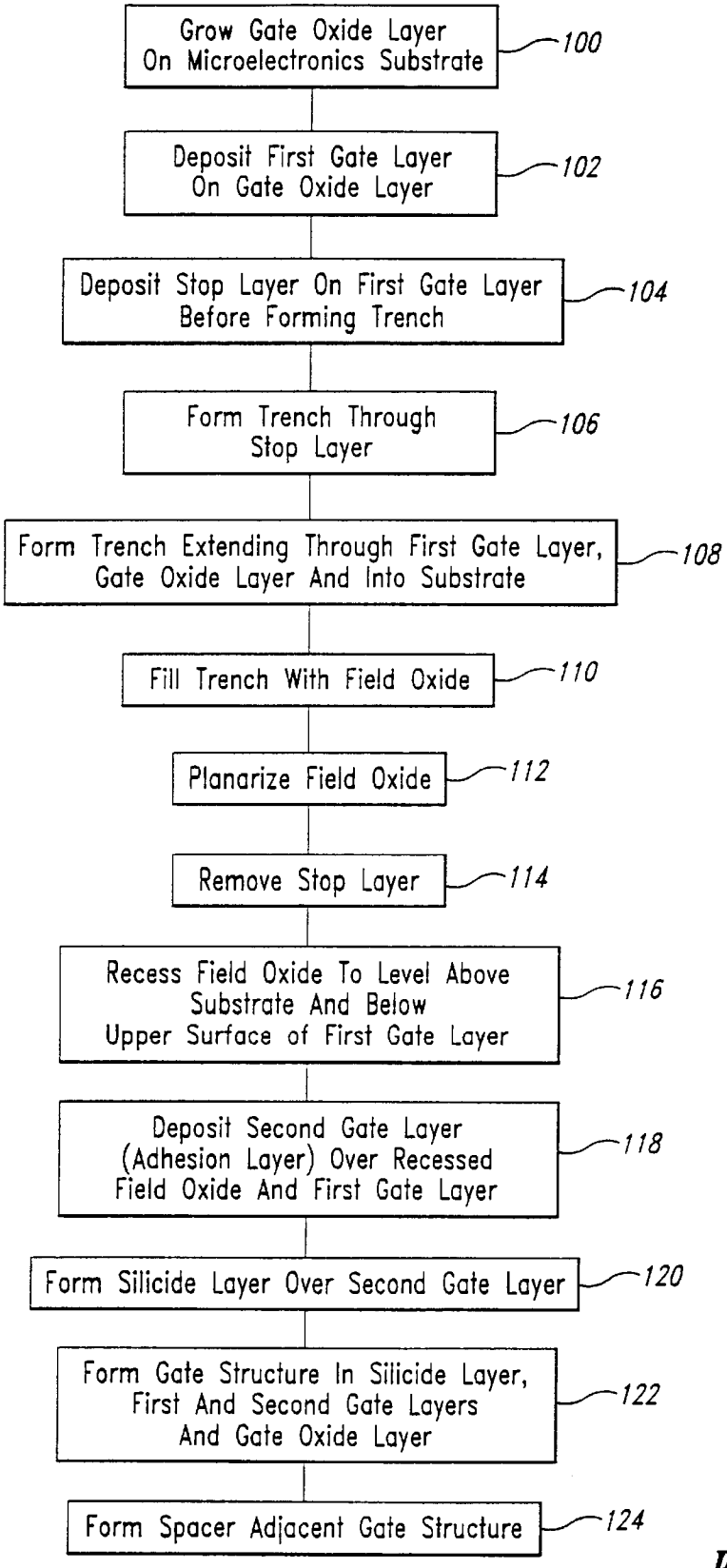

Grow Gate Oxide Layer On Microelectronics Substrate
100
Deposit First Gate Layer On Gate Oxide Layer
102
Deposit Stop Layer On First Gate Layer Before Forming Trench
104
Form Trench Through Stop Layer
106
Form Trench Extending Through First Gate Layer, Gate Oxide Layer And Into Substrate
108
Fill Trench With Field Oxide
110
Planarize Field Oxide
112
Remove Stop Layer
114
Recess Field Oxide To Level Above Substrate And Below Upper Surface of First Gate Layer
116
Deposit Second Gate Layer (Adhesion Layer) Over Recessed Field Oxide And First Gate Layer
118
Form Silicide Layer Over Second Gate Layer
120
Form Gate Structure In Silicide Layer, First And Second Gate Layers And Gate Oxide Layer
122
Form Spacer Adjacent Gate Structure
124

Fig. 3

METHOD AND APPARATUS FOR TRENCH ISOLATION PROCESS WITH PAD GATE AND TRENCH EDGE SPACER ELIMINATION

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of ending U.S. patent application Ser. No. 09/032,231, filed Feb. 27, 1998, now U.S. Pat. No. 6,107,157.

TECHNICAL FIELD

The present invention relates generally to trench isolation structures on microelectronic devices and methods for forming the same, and more specifically to oxide spacers which are formed about trench isolation structures.

BACKGROUND OF THE INVENTION

Microelectronic devices are used in computers, communications equipment, televisions and many other products. Typical microelectronic devices include processors, memory devices, field emission displays and other devices that have circuits with small, complex components. In current manufacturing processes, the components of such circuits are generally formed on a microelectronic substrate or wafer with conductive, insulative and semiconductive materials. Fifty to several hundred microelectronic devices are typically formed on each microelectronic substrate, and each microelectronic device may have several million components.

Because fabricating microelectronic devices generally involves forming electrical components at a number of layers and locations, microelectronic devices generally have many conductive features to couple the various components together.

The method by which the components of an integrated circuit are interconnected involves the fabrication of metal strips that run across an oxide layer in the regions between rows of transistors. However, the strips, together with the oxide beneath the strips, form gates of parasitic MOS transistors and diffused regions adjacent the strips form sources and drain regions, respectively, of the parasitic MOS transistors. The threshold voltage of such parasitic transistors must be kept higher than any possible operating voltage so that spurious channels will not be inadvertently formed between the devices. In order to isolate MOS transistors, then, it is necessary to prevent the formation of channels in the field regions, implying that a large value of VT is needed in the field regions.

Implementing electronic circuits involves connecting isolated devices through specific electrical paths. When fabricating silicon integrated circuits it must therefore be possible to isolate devices built into the silicon from one another. These devices can subsequently be interconnected to create the specific circuit configurations desired. Isolation technology is one of the most critical aspects of fabricating integrated circuits. Hence, a variety of techniques have been developed to isolate devices in integrated circuits. These techniques balance competing requirements, such as minimum isolation spacing, area of footprint, surface planarity, process complexity, and density of defects generated during fabrication of the isolation structure.

One of the most important techniques developed is termed LOCOS isolation (for LOCal Oxidation of Silicon), which involves the formation of a semi-recessed oxide in the nonactive (or field) areas of the substrate for use with PMOS and NMOS integrated circuits. Conventional LOCOS isolation technologies reach the limits of their effectiveness as device geometries reach submicron size. Modified LOCOS processes such as trench isolation have had to be developed to deal with these smaller geometries.

Refilled trench structures have been used as a replacement for conventional LOCOS isolation techniques. Trench/refill approaches for isolation applications generally fall into the following three categorie: shallow trenches (less than 1 micron); moderate depth trenches (1–3 micron); and deep, narrow trenches (greater than 3 micron deep, less than 2 micron wide). Shallow, refilled trenches are used primarily for isolating devices of the same type, and hence they can be considered as replacements for LOCOS isolation. An example of a shallow trench isolation structure is shown in FIG. **1**.

The conventional shallow trench isolation structure **10** shown in FIG. **1** is fabricated on a microelectronic substrate **20**. Gate structures **100** and **300** are formed on the substrate **20** from a pad/gate oxide layer **30**, a first gate layer **40**, a second gate layer **70** and a silicide layer **80**. A trench **22** formed in the substrate **20** is filled with a silicon oxide **60**, to form the shallow trench isolation structure or isolation pad **400**. An isolated component **200** is fabricated on the isolation pad **400**, the isolated component **200** comprising the second gate layer **70** and the silicide layer **80**. Oxide spacers **91–94** are then formed about the gate structures **100** and **300**, the isolated component **200** and the isolation pad **400**. The oxide spacers **91–94** protect the components from contact with other conductive components, as well as, providing gentle slopes to improve step coverage when applying additional layers. Generally, the less severe the slope, the better the coverage.

Due to the need to define gentle slopes from the relatively tall gate structures **100**, **300**, the isolated component **200**, and the isolation pad **400**, the spacers **91–94** take up a large amount of area on the microelectronic substrate **20**. Continued progress in microelectronic fabrication requires that isolation structures be as small as possible and take up a minimum of area on the microelectronic substrate. Any reduction in the size of the isolation structures will provide great benefits in semiconductor manufacture.

SUMMARY OF THE INVENTION

A reduction in the size of isolation shallow trench structures and associated gates is achieved by the elimination of spacers about the isolation pad and the reduction in the area occupied by spacers around the associated gate structures and the isolation component. The elimination of the spacer around the isolation pad, and the reduction in size of the other spacers is achieved by controlling the height by which the isolation pad extends from the substrate.

In a first exemplary embodiment, the isolation pad is recessed to a level which is between an upper level of the first gate layer and an upper level of the substrate of the microelectronic substrate.

In a second embodiment, the height of the isolation pad is controlled relative to the height of the gate structure by ensuring that the gate structure is at least approximately twice the height of the height by which the isolation pad extends beyond the substrate. Likewise, spacer size can be controlled by ensuring that the isolation pad extends beyond the substrate by a height which is less than approximately one half of the height of the gate structure.

Controlling the relative heights of the isolation pad relative to the gate structures or the isolated component is

accomplished by recessing the isolation pad during the fabrication process.

In one exemplary embodiment of the fabrication process, the gate oxide layer is grown on the microelectronic substrate. The first gate layer is deposited on the gate oxide layer and the trench is formed through the gate layer and the gate oxide layer and into the substrate. The trench is then filled with the silicon oxide, and the structure is planarized through chemical-mechanical planarization (CMP). The field oxide is then recessed to an appropriate depth. It is this recess step which controls the later spacer formation. After recessing, the second gate layer is deposited over the recessed field oxide and the first gate layer. The silicide layer is then formed over the second gate layer and gate structures and the isolated component are formed in the silicide layer, the first and second gate layers, and the gate oxide layer. Spacers are formed about the resulting gate structures and the isolated component.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view showing a conventional method for the fabrication of a shallow trench isolation structure having spacers.

FIGS. **2**A–**2**H are cross-sectional views showing respective steps of a method for the fabrication of a shallow trench isolation structure in a microelectronic substrate, according to an exemplary embodiment of the present invention.

FIG. **3** is a flow chart of the method steps in the exemplary embodiment of FIGS. **2**A–**2**G.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of various embodiments of the present invention. However, one skilled in the art will understand that the present invention may be practiced without these details. In other instances, well-known structures associated with microelectronic devices and with the fabrication of microelectronic devices, and isolation structures in microelectronic devices, have not been shown in detail in order to avoid unnecessarily obscuring the description of the embodiments of the invention.

With reference to FIGS. **2**A and **3**, a pad oxide or gate oxide layer **30** is formed on a surface **24** of a microelectronic substrate **20** in step **100**. The gate oxide layer **30** has an exposed upper surface **32**. The substrate **20** may be formed of glass or other suitable material, but is preferably formed of silicon. The gate oxide layer **30** may be formed by first cleaning a bare silicon surface of substrate **20** and then thermally growing a SiO_2 layer thereupon. Other techniques for forming the gate oxide layer **30** may be used, such as CVD SiO_2 deposition.

With reference to FIGS. **2**B and **3**, a first gate layer **40** is deposited over the gate oxide layer **30** in step **102**. The first gate layer **40** has an upper surface **42**. The first gate layer **40** preferably consists of polysilicon. A nitride stop layer **50** may optionally be formed over the first gate layer **40** in step **104**. The stop layer **50** may be CVD silicon nitride which functions as an oxidation mask.

With reference to FIGS. **2**C and **3**, in steps **106** and **108**, a trench **22** is formed, the trench **22** extending through the stop layer **50**, the first gate layer **40**, the gate oxide layer **30** and into the substrate **20**. The trench **22** defines a field area **24** in the substrate **20**. A thin layer (100–200 Å) of silicon dioxide (SiO_2) is then thermally grown on the exposed silicon (Si).

With reference to FIGS. **2**D and **3**, the trench **22** is filled with silicon oxide to form a field oxide **60** in step **110**. Silicon oxide can be deposited using conventional techniques such as LPCVD, HDPCVD (high density plasma CVD), etc. Conventional processes may be used to reduce or eliminate the birds beak which often results from field oxide growth. Chemical-mechanical planarization (CMP) is then used to planarize the field oxide **60** in step **112**. In general, CMP involves holding or rotating a wafer of semiconductor material against a wetted polishing surface under controlled chemical slurry, pressure, and temperature conditions. A chemical slurry containing a polishing agent such as alumina or silica may be utilized as the abrasive medium. Additionally, the chemical slurry may contain chemical etchants. This procedure may be used to produce a surface with a desired endpoint or thickness, which also has a polished and planarized surface. If the optional stop layer **50** is formed, the stop layer **50** will normally determine the endpoint of the CMP step **112**. The stop layer **50** is then removed in step **114** by conventional means.

With reference to FIGS. **2**E and **3**, the field oxide **60** is recessed in step **116** such that the surface of the field oxide **60** is at a level between the level of the upper surface **42** of the first gate layer **40** and the surface **24** of substrate **20**. In the exemplary embodiment, the field oxide level is between the upper surface **42** of the first gate layer **40** and the upper surface **32** of the gate oxide layer **30**.

With reference to FIGS. **2**F and **3**, a second gate layer **70** may be formed on the recessed field oxide **60** and the first gate layer **40** in step **118**. The second gate layer **70** serves as an adhesion layer. The second gate layer **70** is preferably composed of polysilicon. The second gate layer **70** can be formed by conventional deposition methods.

A conductive layer **80** is then formed over the second gate layer **70** in step **120**. The conductive layer **80** may be formed by chemical vapor deposition of tungsten silicide (WSi_x). Other refracting metal suicides may be used, including, but not limited to $TiSi_2$, $TaSi_2$, $MoSi_2$, PtSi. A thin layer of oxide may optionally be formed on the silicide layer **80**.

Gate structures **100**, **300** are next formed in the silicide conductive layer **80**, the first and second gate layers **40**, **70** and the gate oxide layer **30** in step **122** as shown in FIG. **2**G. The shallow trench isolation structure **400** may also be uncovered at this point. The gates **100**, **300** are formed through conventional patterning and etching processes. The isolated component **200** may also be formed at this point.

With reference to FIGS. **2**H and **3**, spacers **91** and **92** are formed about the gate structures **100** and **300**, respectively, and spacer **92** is formed about the isolated component **200** in step **124**. Formation of the spacers may be carried out in a number of ways including deposition of LPCVD-SiO_2. The spacers **91–93** are grown until an adequate reduction of step size is achieved. Due to the relatively low profile of the isolation pad **400**, little or no spacer will form adjacent to the isolation pad **60**. To achieve this, the field oxide isolation pad height **66** should be approximately one half of the height of the gate structure **106**, **306**, an approximately two-to-one ratio.

Although specific embodiments of the shallow trench isolation structure and method of the present invention have been described above for illustrative purposes, various equivalent modifications may be made without departing from the spirit and scope of the invention, as will be recognized by those skilled in the relevant art. The teachings provided herein of the present invention can be applied to other isolation structures, not necessarily the exemplary

shallow trench isolation structure generally described above. For example, additional layers may be formed or the order of forming layers may be changed. The substrate may be composed of silicon, glass or some combination of other materials or layers of materials. Alternatively, different materials may be employed, and different methods of forming or depositing the layers may be used.

These and other changes can be made to the invention in light of the above detailed description. In general, in the following claims, the terms should not be construed to limit the invention to the specific embodiments disclosed in the specification claims, but should be construed to include all apparatus and methods for forming trench isolation structures with reduced and eliminated spacers. Accordingly, the invention is not limited by the disclosure, but instead its scope is to be determined entirely by the following claims.

What is claimed is:

1. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

forming a trench in the microelectronic substrate;

depositing a field oxide in the trench extending from the trench to a height which is less than half of a height of a gate structure to be formed on the substrate;

forming the gate structure on the substrate; and

forming a spacer adjacent the gate structure.

2. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

depositing a field oxide isolation pad extending from a recess in the substrate to a field oxide isolation pad height;

forming a gate structure on the substrate having a height which is at least twice the height of the field oxide isolation pad height; and

forming a spacer adjacent the gate structure.

3. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

forming a trench in the microelectronic substrate;

depositing a field oxide isolation pad extending from the trench by height which is less than half of a height of a component to be formed on the field oxide isolation pad;

forming the component on the field oxide isolation pad; and

forming a spacer adjacent the component.

4. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

depositing a field oxide isolation pad extending from a recess in the substrate to a field oxide isolation pad height;

forming a component on the field isolation pad having a height which is at least twice the height of the field oxide isolation pad height; and

forming a spacer adjacent the component.

5. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

growing a gate oxide layer on the microelectronic substrate;

depositing a first gate layer on the gate oxide layer;

forming a trench, the trench extending through the first gate layer, the gate oxide layer and into the substrate;

filling the trench with a field oxide;

planarizing the field oxide;

recessing the field oxide;

depositing a second gate layer over the recessed field oxide and the first gate layer;

forming a silicide layer over the second gate layer;

forming at least one gate structure in the silicide layer, the first and the second gate layers and the gate oxide layer; and

forming a spacer adjacent the gate structure.

6. The method of claim **5** wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is below an upper surface of the first gate layer.

7. The method of claim **5** wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is above an upper surface of the substrate.

8. The method of claim **5** wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is between an upper level of the first gate layer and an upper level of the substrate.

9. The method of claim **5** wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is below an upper level of the first gate layer and that is at least even with an upper level of the substrate.

10. The method of claim **5** wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a level which extends beyond an upper level of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure.

11. The method of claim **10**, further comprising the step of depositing a stop layer on the first gate layer before forming the trench.

12. The method of claim **11**, wherein the step of forming a trench includes the step of

etching through the stop layer, the first gate layer, the gate oxide layer; and etching into the substrate.

13. The method of claim **12**, further comprising the step of removing the stop layer after planarizing the field oxide.

14. The method of claim **5** wherein the step of depositing a first gate layer includes the step of

depositing a layer of polysilicon on the gate oxide layer.

15. The method of claim **5** wherein the step of depositing a second gate layer includes the step of

depositing a layer of polysilicon on the recessed field oxide and the first gate layer.

16. The method of claim **5** wherein the step of forming a silicide layer includes the step of

depositing a layer of tungsten silicide on the second gate layer by chemical vapor deposition.

17. The method of claim **5**, wherein the step of forming the silicide layer includes the step of:

depositing a conductor by chemical vapor deposition on at least one of the first and the second gate layers; and

reacting the metal with the at least one of the first and the second gate layers to form a silicide.

18. A method of forming a trench isolation structure on a microelectronic substrate, comprising:

growing a gate oxide layer on the microelectronic substrate;

depositing a first gate layer on the gate oxide layer;

forming a trench, the trench extending through the first gate layer, the gate oxide layer and into the substrate;

filling the trench with a field oxide;

planarizing the field oxide;

recessing the field oxide to a depth that is below an upper surface of the first gate layer;

depositing a second gate layer over the recessed field oxide and the first gate layer;

forming a silicide layer over the second gate layer;

forming at least one gate structure in the silicide layer, the first and the second gate layers and the gate oxide layer; and

forming a spacer adjacent the gate structure.

19. The method of claim **18** wherein recessing the field oxide includes recessing the field oxide to a depth that is above an upper surface of the substrate.

20. The method of claim **18** wherein recessing the field oxide includes recessing the field oxide to a depth that is between an upper level of the first gate layer and an upper level of the substrate.

21. The method of claim **18** wherein recessing the field oxide includes recessing the field oxide to a depth that is at least even with an upper level of the substrate.

22. The method of claim **18** wherein recessing the field oxide includes recessing the field oxide to a level which extends beyond an upper level of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure.

23. The method of claim **18**, further comprising depositing a stop layer on the first gate layer before forming the trench.

24. The method of claim **23**, wherein forming a trench includes etching through the stop layer, the first gate layer, the gate oxide layer; and etching into the substrate.

25. The method of claim **24**, further comprising removing the stop layer after planarizing the field oxide.

26. The method of claim **18** wherein depositing a first gate layer includes depositing a layer of polysilicon on the gate oxide layer.

27. The method of claim **18** wherein depositing a second gate layer includes depositing a layer of polysilicon on the recessed field oxide and the first gate layer.

28. The method of claim **18** wherein forming a silicide layer includes depositing a layer of tungsten silicide on the second gate layer by chemical vapor deposition.

29. A method of forming a trench isolation structure on a microelectronic substrate, comprising:

growing a gate oxide layer on the microelectronic substrate;

depositing a first gate layer on the gate oxide layer;

depositing a stop layer on the first gate layer before forming a trench;

forming the trench, the trench extending through the stop layer, the first gate layer, the gate oxide layer and into the substrate;

filling the trench with a field oxide;

planarizing the field oxide;

recessing the field oxide;

depositing a second gate layer over the recessed field oxide and the first gate layer;

forming a silicide layer over the second gate layer;

forming at least one gate structure in the silicide layer, the first and the second gate layers and the gate oxide layer; and

forming a spacer adjacent the gate structure.

30. The method of claim **29** wherein recessing the field oxide includes recessing the field oxide to a depth that is below an upper surface of the first gate layer.

31. The method of claim **29** wherein recessing the field oxide includes recessing the field oxide to a depth that is below an upper level of the first gate layer and greater than or equal to a level of the substrate.

32. The method of claim **29**, wherein forming a trench includes etching through the stop layer, the first gate layer, the gate oxide layer; and etching into the substrate.

33. The method of claim **29**, further comprising removing the stop layer after planarizing the field oxide.

34. A method of forming a trench isolation structure on a microelectronic substrate, comprising:

growing a gate oxide layer on the microelectronic substrate;

depositing a first gate layer on the gate oxide layer;

forming a trench, the trench extending through the first gate layer, the gate oxide layer and into the substrate;

filling the trench with a field oxide;

planarizing the field oxide;

recessing the field oxide;

depositing a second gate layer over the recessed field oxide and the first gate layer;

forming a silicide layer over at least one of the first and second gate layers including depositing a conductor by chemical vapor deposition on the at least one of the first and second gate layers, and reacting the conductor with the at least one of the first and second gate layers;

forming at least one gate structure in the silicide layer, the at least one of the first and the second gate layers and the gate oxide layer; and

forming a spacer adjacent the gate structure.

35. The method of claim **34** wherein recessing the field oxide includes recessing the field oxide to a depth that is below an upper surface of the first gate layer.

36. The method of claim **34** wherein recessing the field oxide includes recessing the field oxide to a depth that is below an upper level of the first gate layer and greater than or equal to a level of the substrate.

37. The method of claim **34**, further comprising depositing a stop layer on the first gate layer before forming the trench.

38. The method of claim **34** wherein depositing a first gate layer includes depositing a layer of polysilicon on the gate oxide layer.

* * * * *

EXHIBIT D

US006455935B1

(12) **United States Patent**
Hu

(10) **Patent No.: US 6,455,935 B1**
(45) **Date of Patent: *Sep. 24, 2002**

(54) **ASYMMETRIC, DOUBLE-SIDED SELF-ALIGNED SILICIDE**

(75) Inventor: **Yongjun Jeff Hu**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 122 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/658,780**

(22) Filed: **Sep. 11, 2000**

Related U.S. Application Data

(63) Continuation of application No. 09/026,104, filed on Feb. 19, 1998, now Pat. No. 6,147,405.

(51) **Int. Cl.**[7] **H01L 23/48**

(52) **U.S. Cl.** **257/755**; 257/412; 257/413; 257/756; 257/757

(58) **Field of Search** 257/755, 412, 257/413, 756, 757, 763, 764; 438/649, 682, 683, 655, 660, 664, 583

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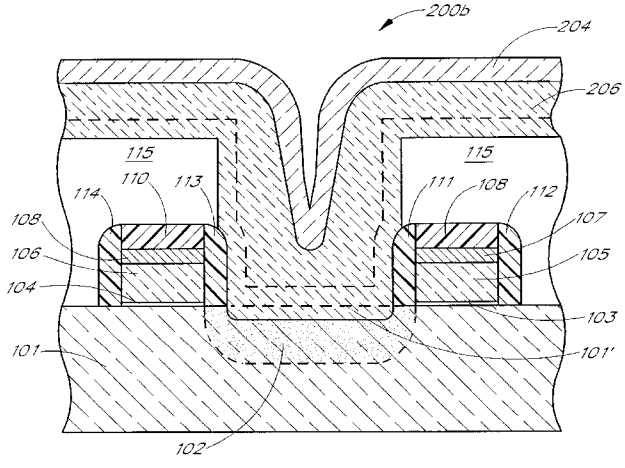
(74) *Attorney, Agent, or Firm*—Knobbe, Martens, Olson & Bear, LLP.

(57) **ABSTRACT**

Disclosed are structures and processes which are related to asymmetric, self-aligned silicidation in the fabrication of integrated circuits. A pre-anneal contact stack includes a silicon substrate, a metal source layer such as titanium-rich titanium nitride (TiN_x), and a silicon layer. The metal nitride layer is deposited on the substrate by sputtering a target metal reactively in nitrogen and argon ambient. A N:Ar ratio is selected to deposit a uniform distribution of the metal nitride in an unsaturated mode (x<1) over the silicon substrate. The intermediate substrate structure is sintered to form a metal silicide. The silicidation of metal asymmetrically consumes less of the underlying silicon than the overlying silicon layer. The resulting structure is a mixed metal silicide/nitride layer which has a sufficient thickness to provide low sheet resistance without excessively consuming the underlying substrate. A metal nitride of maximum bulk resistivity within the unsaturated (metal-rich) realm is chosen for maximizing asymmetry in the silicidation.

10 Claims, 10 Drawing Sheets



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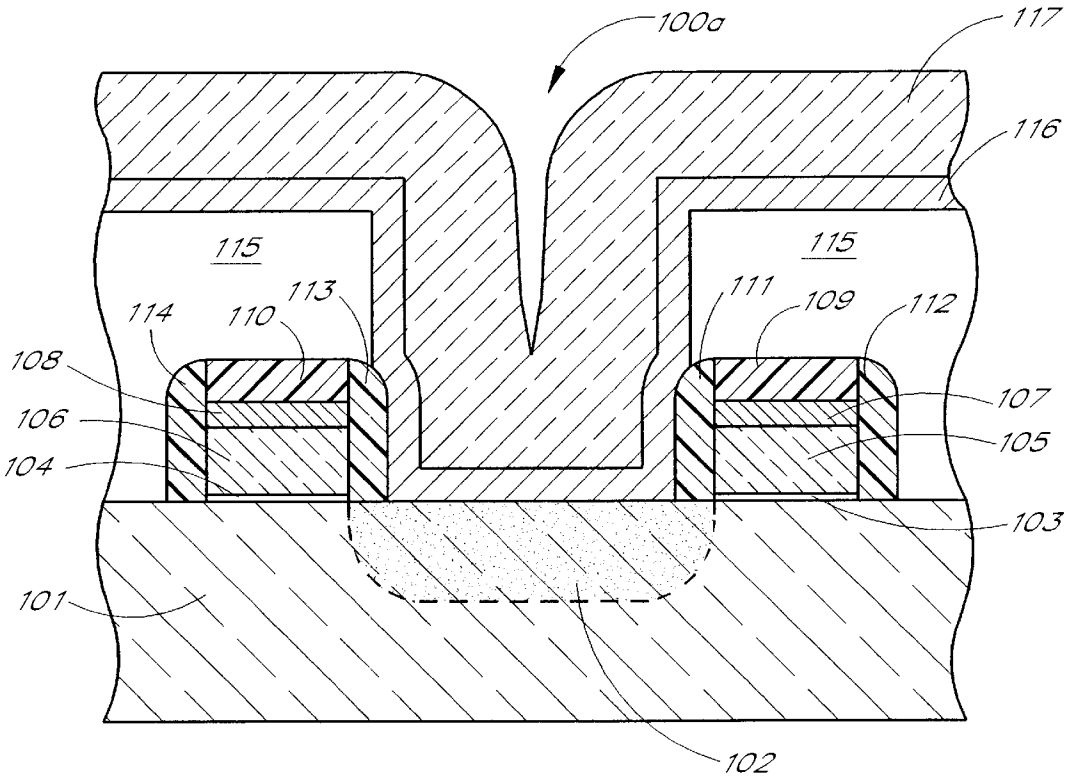

100a
117
116
115
115
114
110
113
111
109
112
108
106
104
107
105
103
101
102

FIG. 1A

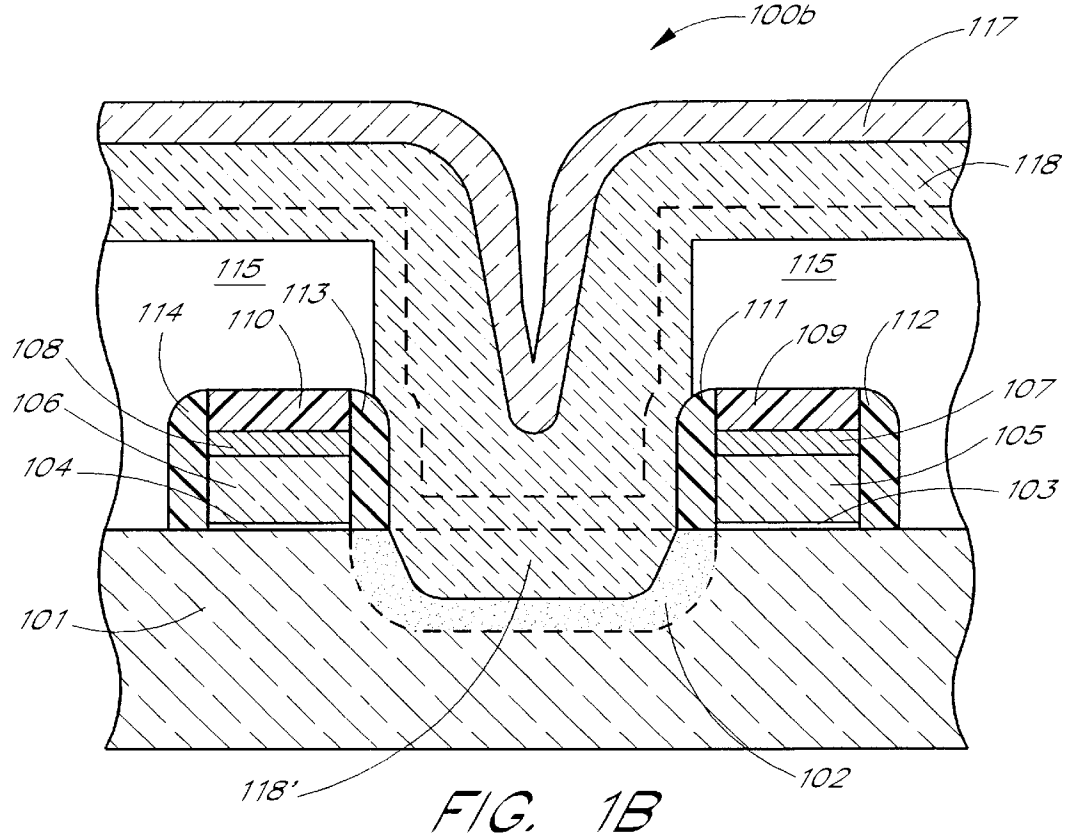

100b
117
118
115
115
114
110
113
111
109
112
108
106
104
107
105
103
101
118'
102

FIG. 1B

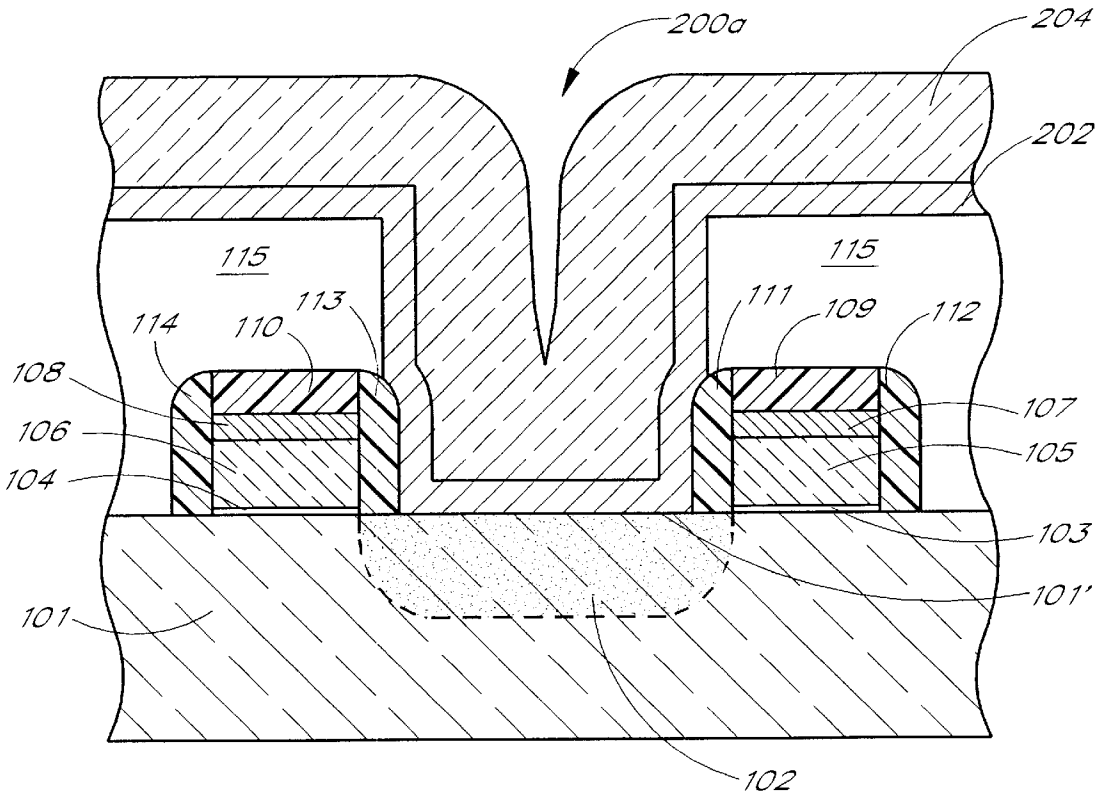

200a
204
202
115
115
114
110
113
111
109
112
108
106
104
107
105
103
101'
101
102

FIG. 2A

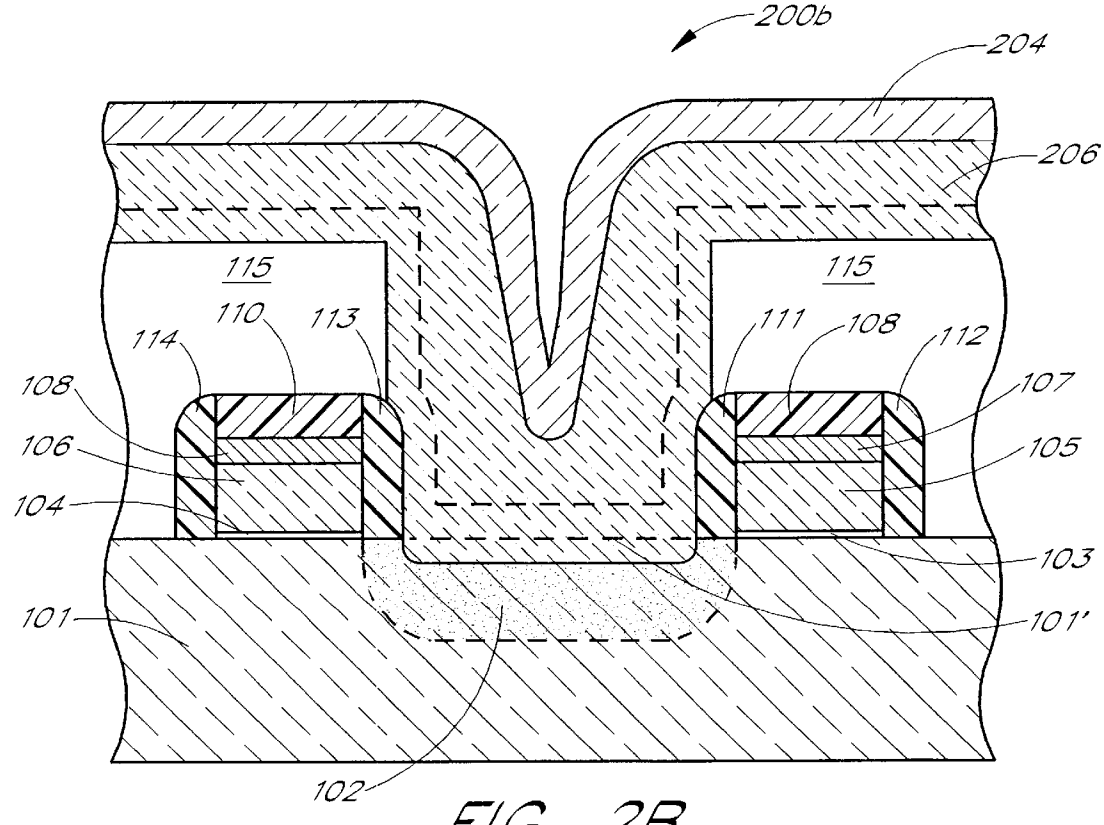

200b
204
206
115
115
110
113
114
111
108
112
108
106
104
107
105
103
101'
101
102

FIG. 2B

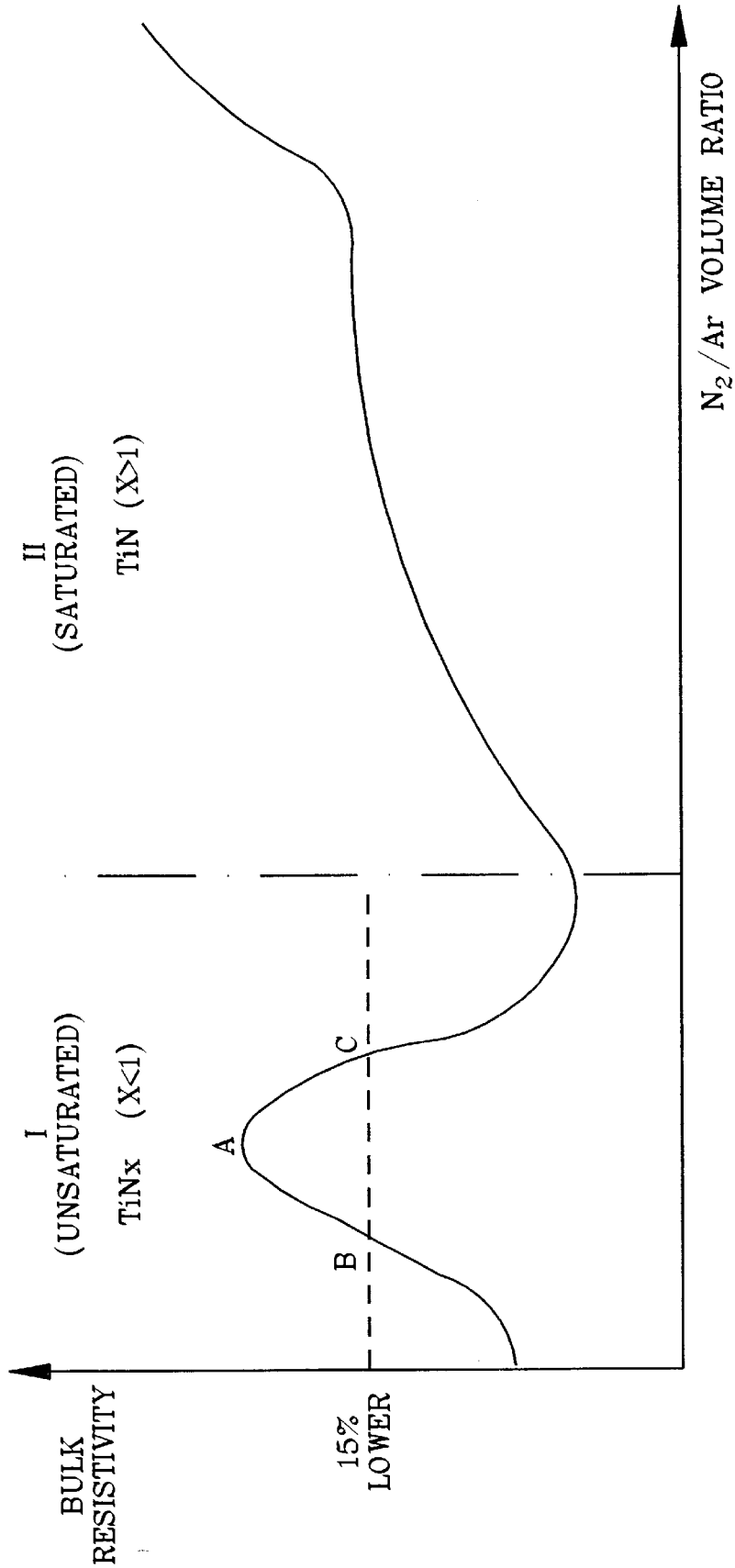

BULK RESISTIVITY
15% LOWER
I (UNSATURATED) TiNx (X<1)
II (SATURATED) TiN (X>1)
A
B
C
N_2/Ar VOLUME RATIO

FIG. 3

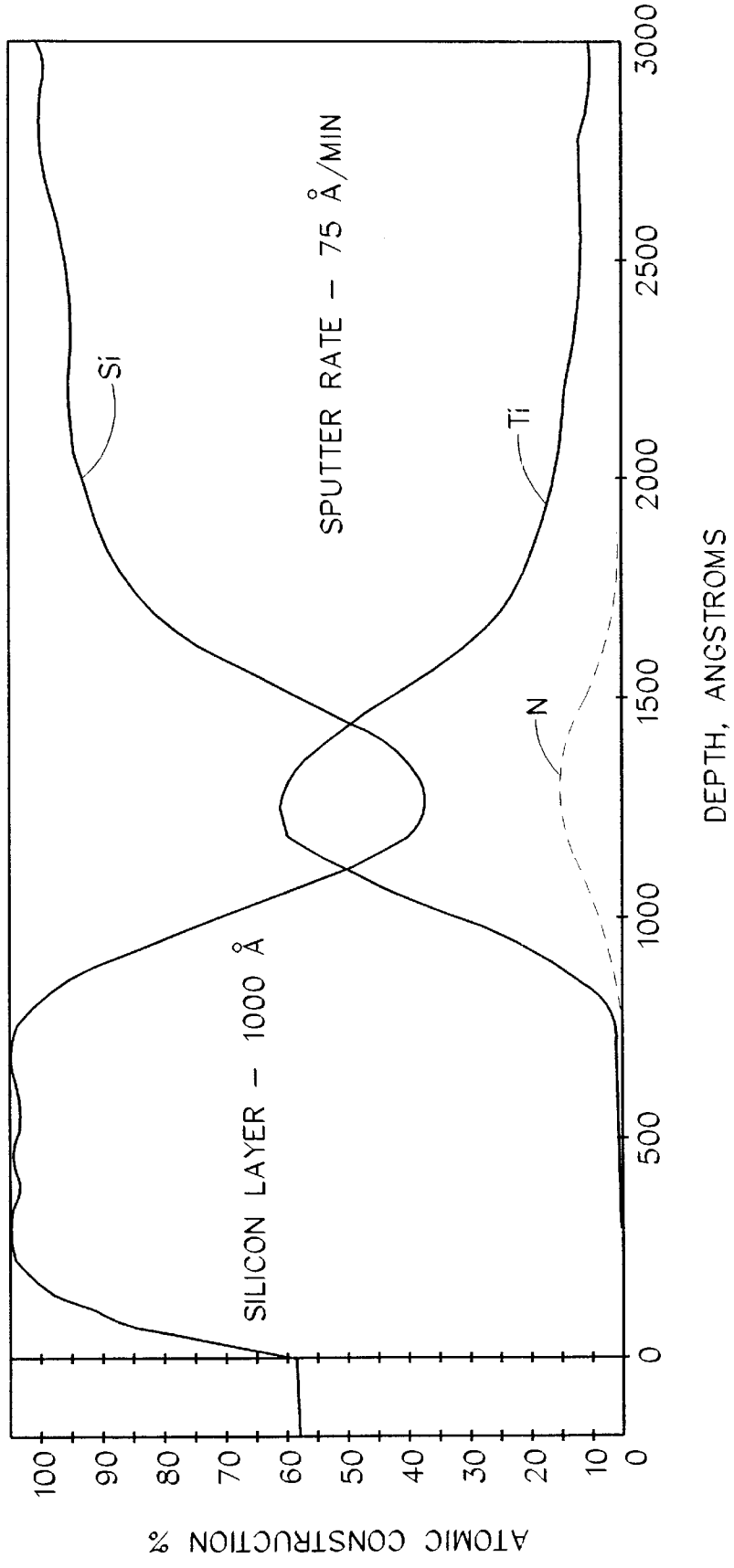

ATOMIC CONSTRUCTION %
100
90
80
70
60
50
40
30
20
10
0
0
500
1000
1500
2000
2500
3000
DEPTH, ANGSTROMS
SILICON LAYER – 1000 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N

FIG. 4A

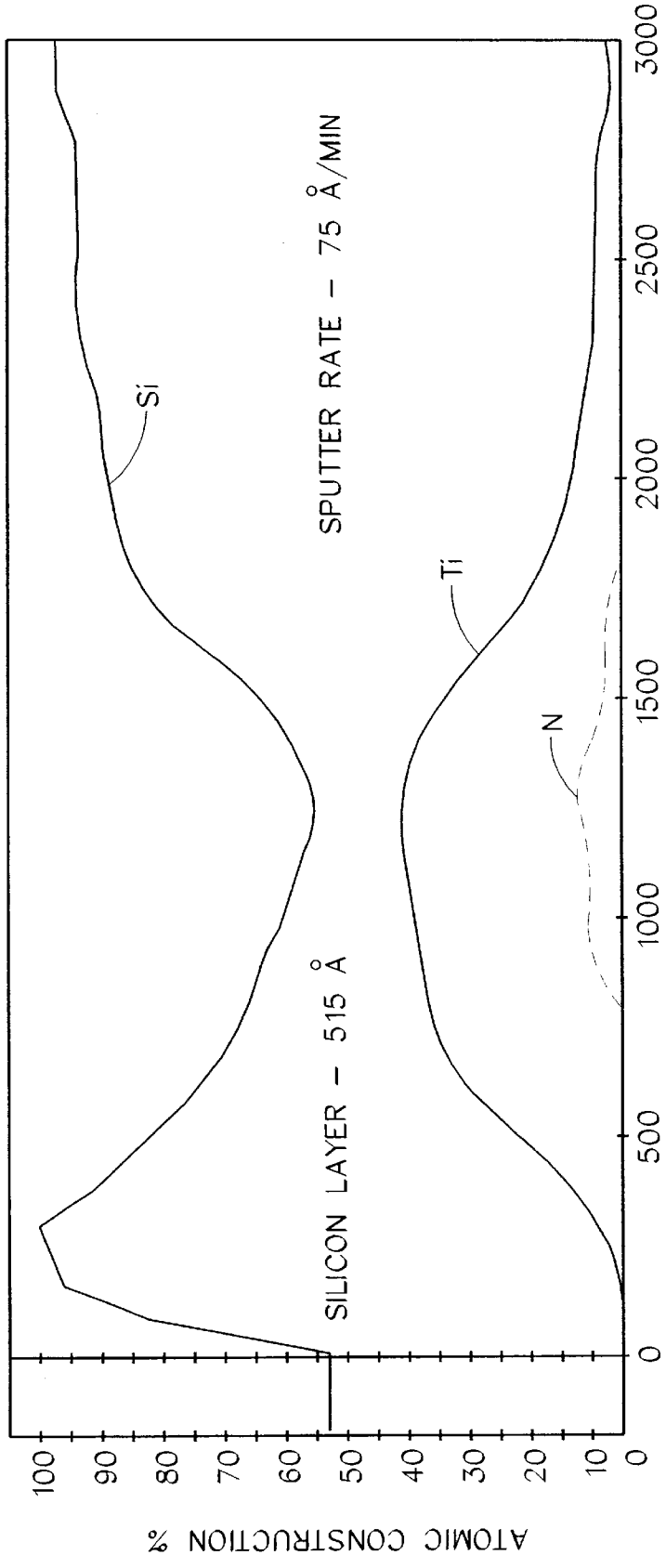

ATOMIC CONSTRUCTION %
100
90
80
70
60
50
40
30
20
10
0
0
500
1000
1500
2000
2500
3000
DEPTH, ANGSTROMS
SILICON LAYER – 515 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N

FIG. 4B

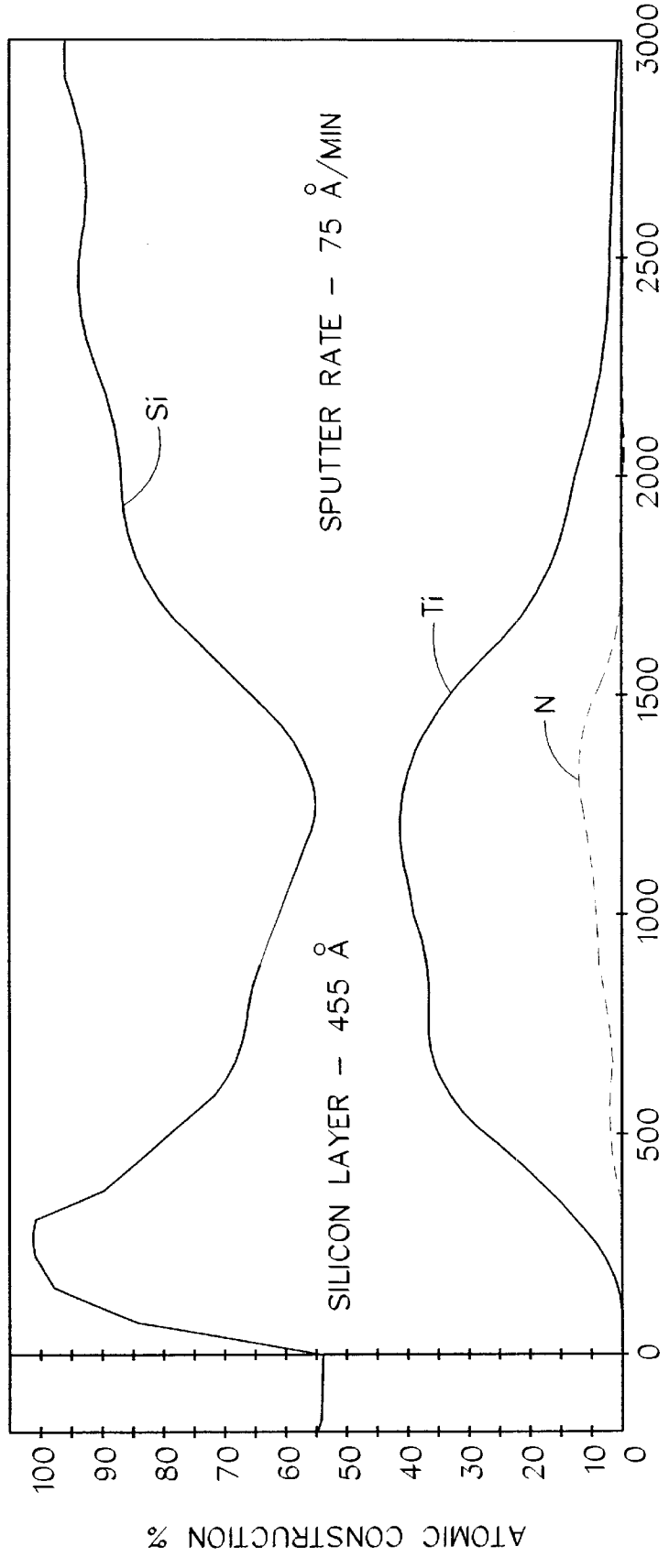

ATOMIC CONSTRUCTION %
100
90
80
70
60
50
40
30
20
10
0
0
500
1000
1500
2000
2500
3000
DEPTH, ANGSTROMS
SILICON LAYER – 455 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N

FIG. 4C

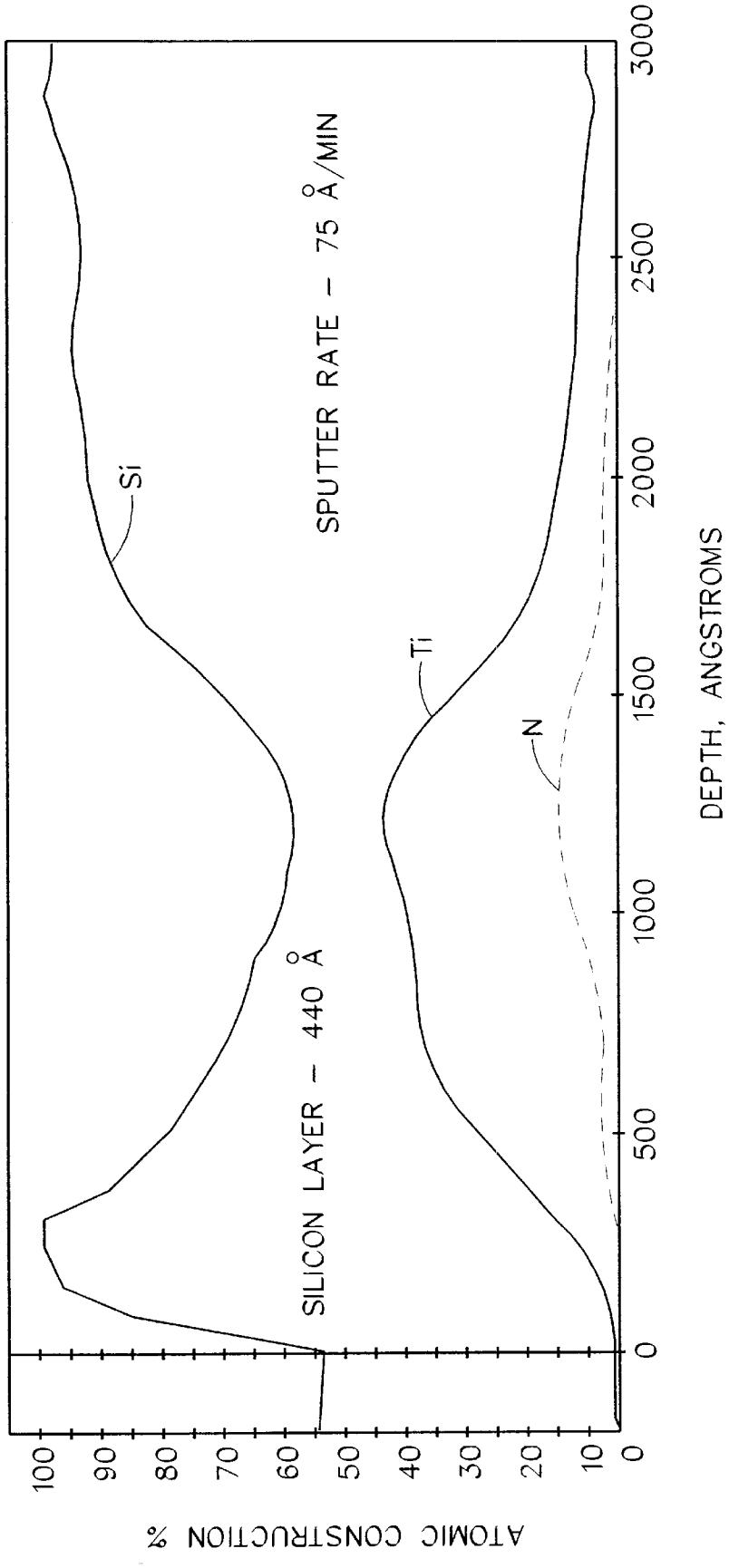

ATOMIC CONSTRUCTION %
100
90
80
70
60
50
40
30
20
10
0
0
500
1000
1500
2000
2500
3000
DEPTH, ANGSTROMS
SILICON LAYER – 440 Å
SPUTTER RATE – 75 Å/MIN
Si
Ti
N

FIG. 4D

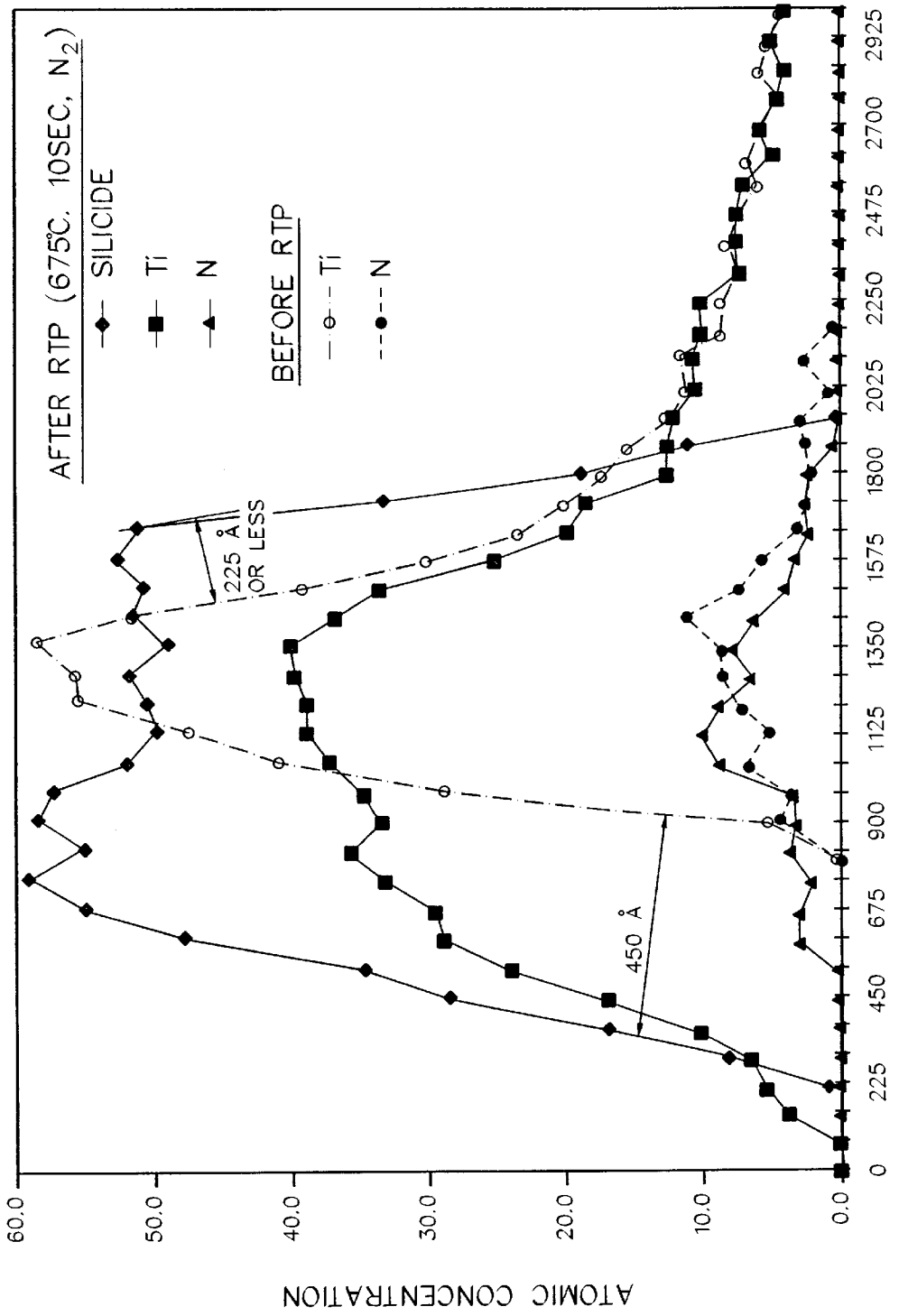
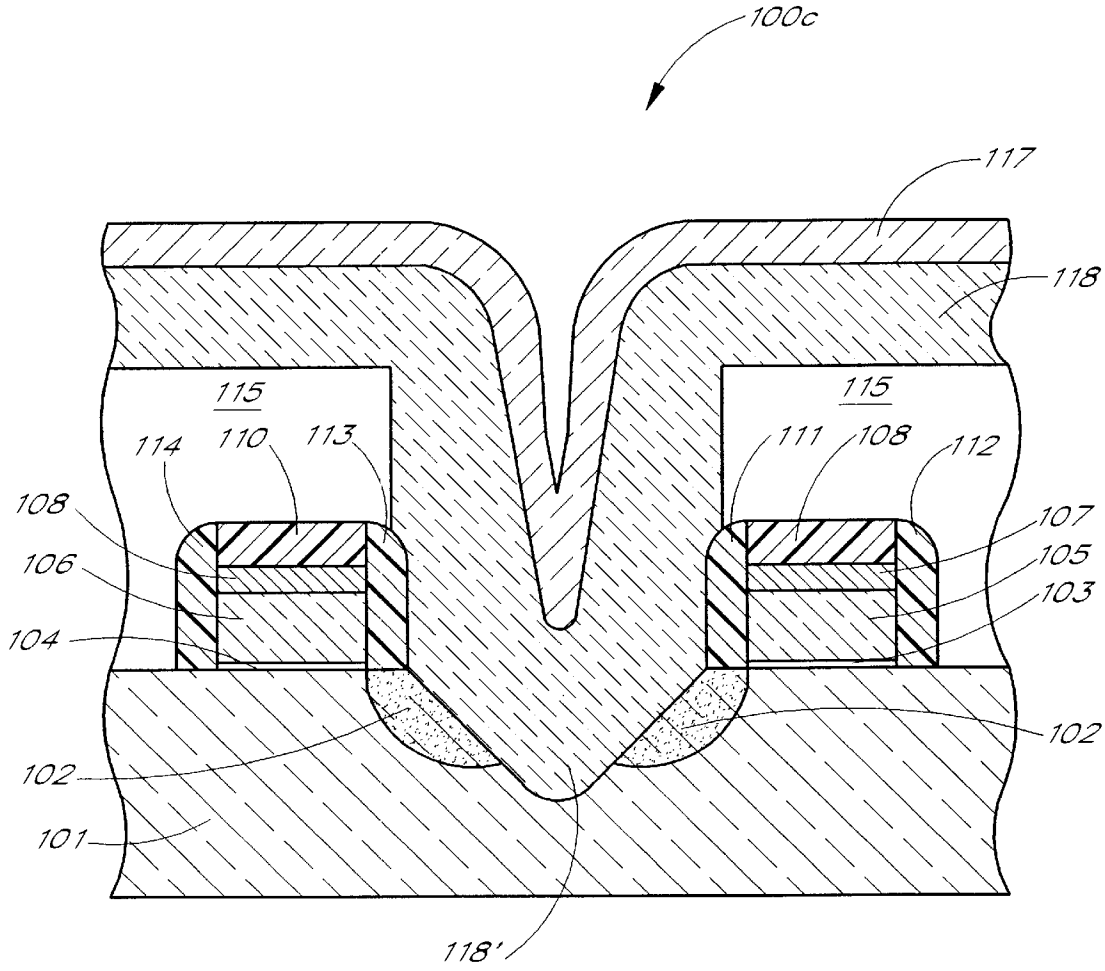

AFTER RTP (675°C. 10SEC, N_2)
SILICIDE
Ti
N
BEFORE RTP
Ti
N
225 Å OR LESS
450 Å
ATOMIC CONCENTRATION
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0
225
450
675
900
1125
1350
1575
1800
2025
2250
2475
2700
2925
DEPTH (A)

FIG. 5

FIG. 6A


100c
117
118
115
115
114
110
113
111
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112
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106
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107
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103
102
102
101
118'

FIG. 6B

ASYMMETRIC, DOUBLE-SIDED SELF-ALIGNED SILICIDE

REFERENCE TO RELATED APPLICATION

The present application is a continuation of U.S. application Ser. No. 09/026,104, filed Feb. 19, 1998 now U.S. Pat. No. 6,147,405.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to fabrication of semiconductor circuit devices. More particularly, the present invention is directed to self-aligned silicide structures and methods of forming the same without excessive consumption of underlying silicon.

2. Description of Related Art

As is well known in processing integrated circuits, electrical contacts must be made among circuit nodes, such as isolated device active regions formed within a single-crystal silicon substrate. As the contact dimensions of devices become smaller, the contact resistance and the sheet resistance of the contacts increase. In this regard, refractory metal silicides have been used for local interconnections to provide low resistance electrical contacts between device active regions within the silicon substrate.

One common method of forming metal silicides is a self-aligned silicide process, often referred to as salicidation. A thin layer of refractory metal, such as titanium, is deposited over a dielectric area and through contact openings formed on the dielectric area to contact underlying silicon circuit elements, such as source and drain active regions formed within a silicon substrate. The structure is generally annealed to form a silicide, such as titanium silicide (predominantly $TiSi_2$) at a high temperature. During the anneal, the deposited titanium reacts with the silicon in the contact to form $TiSi_2$ at the contact openings. Titanium which overlies the dielectric area does not form $TiSi_2$, as the titanium does not contact any silicon. The process is referred to as "self-aligned" because the silicide is formed only where the metal layer contacts silicon, for example, through the contact openings. After the first annealing, the unreacted titanium may be removed in a wet etch, and a post-silicidation anneal is performed to lower the sheet resistance of the silicide to acceptable levels. The final annealing converts titanium silicide from the C49 phase to the lower resistance C54 phase. This self-aligned silicide is often referred to by the short form "salicide."

In the salicidation process, silicon from the contact regions of the substrate diffuses upward into the titanium layer. Similarly, titanium diffuses into the underlying active areas of the silicon substrate. Titanium and silicon react with each other to form a silicide thick enough to provide low sheet resistance. As a result, the doped active area of the silicon substrate becomes thinner due to the consumption of silicon during the reaction. The resultant silicide is said to intrude or sink into the substrate. Over-consumption of the underlying silicon can be problematic for any silicon circuit element, tending to cause voids, and thus device failures. Where contact is made to a shallow junction active area of a silicon substrate, salicide contacts of sufficient thickness cannot be formed without completely destroying a junction.

A need, therefore, exists for an interconnect and method of fabricating the same, which provides the advantages of salicide interconnects without excessive consumption of underlying silicon to which contact is made.

SUMMARY OF THE INVENTION

The aforementioned needs are satisfied by several aspects of the present invention.

In accordance with one aspect of the present invention, a method is provided for forming a self-aligned silicide contact on a silicon substrate. The method includes forming a contact window through an insulating layer over the silicon substrate, thereby exposing a portion of the silicon substrate. A metal nitride layer is deposited over the exposed portion of the silicon substrate. A silicon layer is formed over the metal nitride layer.

In accordance with another aspect of the present invention, a method is provided for forming a metal source layer, which incorporates a uniform distribution of an impurity and a metal, between silicon structures in an integrated circuit. The method includes selecting a sputtering ambient to maximize bulk resistivity for a metal-rich class of layers incorporating the impurity and the metal. A metallic target is sputtered in the selected ambient.

In accordance with another aspect of the present invention, a method is provided for forming a silicide interconnect over a silicon substrate. The method includes selecting a metal layer incorporating an impurity to a level below saturation. The metal layer has a bulk resistivity within about 15% of the maximal resistivity for unsaturated metal layers having the same metal and impurity. The selected layer is deposited over the silicon substrate, and the selected layer and the substrate are sintered.

In accordance with another aspect of the present invention, a method is provided for forming a self-aligned silicide contact to a semiconductor substrate. The method includes opening a contact in an insulating layer to expose an active region of the substrate. A refractory metal source layer is deposited into the contact directly over the active region of the substrate. A silicon source layer is deposited directly over the refractory metal source layer. A silicidation is then performed to form the self-aligned silicide contact. The silicidation preferentially consumes silicon from the silicon source layer as compared to silicon from the substrate in a ratio of greater than about 1.2:1.

In accordance with another aspect of the present invention, an intermediate substrate assembly is provided. The assembly includes a silicon substrate, a metal nitride layer directly over the silicon substrate, and a silicon layer directly over the metal nitride layer. In accordance with a preferred embodiment, this intermediate assembly is sintered to form a silicide contact.

In accordance with another aspect of the present invention, an integrated circuit is provided, including a silicon substrate, an insulating layer formed over the silicon substrate with a contact opening formed in the insulating layer, and a conductive contact directly contacting the silicon substrate within the contact opening. The contact includes metal silicide uniformly interspersed with metal nitride.

In accordance with another aspect of the present invention, an integrated circuit includes a silicon substrate and a self-aligned contact. The contact includes a metal silicide, and the extends into the substrate below the upper surface of the substrate by an amount less than about 30% of the contact thickness.

In accordance with another aspect of the present invention, a self-aligned silicide contact is provided. The contact extends below a substrate surface into a shallow junction transistor active area, which has a junction depth of

no more than about 1,000 Å. The contact extends below the substrate surface by no more than about 30% of the junction depth.

These and other features of the present invention will become more fully apparent from the following description and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A and **1**B are partial schematic sectional views of an integrated circuit, illustrating a double-sided salicidation. FIGS. **1**A and **1**B respectively show silicon substrate subassemblies before annealing and after annealing.

FIGS. **2**A and **2**B are partial schematic sectional views of an integrated circuit, illustrating self-aligned salicidation in accordance with a preferred embodiment of the present invention. FIGS. **2**A and **2**B, respectively, show silicon substrate assembly structures before annealing and after annealing.

FIG. **3** shows the bulk resistivity of a titanium nitride layer as a function of N_2/Ar volume ratio in a reactive sputtering of Ti to form TiN_x at a given target power.

FIGS. **4**A–**4**D show X-ray photoelectron spectroscopic ("XPS") profiles of integrated circuits constructed in accordance with the preferred embodiment. FIG. **4**A is a profile of an integrated circuit prior to annealing. FIGS. **4**B, **4**C, and **4**D are profiles of integrated circuits annealed at different temperatures.

FIG. **5** shows XPS curve-fitting results of FIGS. **4**A and **4**B.

FIG. **6**A shows a bit-line contact X-SEM result on an actual device which was run though furnace reflow. FIG. **6**B is a schematic sectional view of the integrated circuit of FIG. **1**B after furnace reflow.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the preferred embodiments are illustrated in the context of self-aligned silicide (or "salicide") contacts to active regions in silicon substrates, it will be recognized by one of skill in the art of semiconductor fabrication that the invention will have application whenever electrical contact to silicon elements is desirable. For example, salicide can be used in forming contact to silicon interconnects, gate electrodes or plugs. Furthermore, the term "substrate," as used in the present application, refers to one or more semiconductor layers or structures which include active or operable portions of semiconductor devices.

In general, one method of reducing substrate (or "silicon electrical element") consumption in forming self-aligned silicide wiring is to supply additional silicon to the process. For example, an intermediate silicon layer can be introduced between the silicon substrate and the titanium layer. The intermediate silicon layer provides the titanium layer with some or all of the silicon required in the salicidation.

With intermediate silicon, however, the titanium layer should be thick enough to consume all of the intermediate silicon in order for the silicide to be in contact with the underlying active area of the silicon substrate. Alternatively, the intermediate silicon layer must be doped to match the doping type of the contacted active region in order to ensure ohmic contact, forming "raised" source/drain regions. Such doping can require an additional mask and all the attendant processing steps. In the fabrication of CMOS circuits, which utilize complementary n-channel and p-channel devices, contacts require two marks for doping the different regions which contact p+ drains and n+ drains, respectively. Each of these masks is expensive both to create for different chip designs and to use in production.

Supplemental silicon can also be introduced over a metallic layer to provide silicon required to form silicide. FIG. **1**A, for example, illustrates a schematic sectional view of such a structure **100***a* formed on a silicon substrate **101**. A highly doped silicon active area **102** is defined below a substrate surface **101**'. In the illustrated embodiment, the active area **102**, which may comprise a transistor source or drain, has an ultrashallow junction of no more than about 1,000 Å.

Two structures, such as gate structures in MOS devices, lie over silicon substrate **101** adjacent the active area **102**. Each of the gate structures has a thin gate oxide layer **103**, **104**, a polysilicon gate electrode layer **105**, **106**, a metallic layer **107**, **108**, and a protective cap layer **109**, **110**. Sidewall spacers **111**, **112**, **113**, **114** protect the gate stacks, and an insulating layer **115** (e.g., BPSG) covers the gate structures and the silicon substrate **101**. A window is opened onto the active area **102** through the insulating layer **115** in order to provide contact to the active area **102**. The contact window thus is defined by the insulating layer **115**, inner sidewall spacers **111**, **113**, and the active area **102**. A titanium layer **116** and a polysilicon layer **117** are deposited, in that order, into the contact window and over the insulating layer **115**. The deposition of polysilicon over titanium forms a sandwich-like structure inside the window, in which the metal layer **116** is interposed between the supplemental silicon (i.e., the polysilicon layer **117**) and the active area **102** of the silicon substrate **101**. This structure **100***a* allows titanium in the titanium layer **116** to diffuse into and consume silicon from both the underlying active area **102** and the overlying polysilicon layer **117** when it is annealed. This process can be referred to as "double-sided salicidation."

FIG. **1**B, for example, shows a structure **100***b* which is the result of annealing the structure **100***a* of FIG. **1**A. Over the insulating layer **115**, only the overlying polysilicon **117** provides silicon for the reaction. Inside the contact window, on the other hand, the reaction proceeds in both directions. Titanium consumes silicon from both the overlying polysilicon layer **117** and the underlying active area **102** to form a silicon-rich titanium silicide **118**' thick enough to present a low sheet resistance. While the titanium may diffuse at about a 10% higher rate in polysilicon than in monocrystalline silicon, the salicidation reaction is substantially symmetrical, consuming about the same amount of silicon from the substrate as from the overlying silicon **117**.

While the double-sided salicidation reaction described above is preferable to conventional salicide, double-sided salicide is not without its problems. For example, chemical vapor deposition ("CVD"), the most common process for depositing polysilicon, does not easily form silicon over metallic layers, such as the titanium layer **116**. This is due to the fact that the silicon does not easily nucleate on metal surfaces. Even if a silicon layer of suitable thickness can be formed over the titanium layer **116**, double-sided salicidation may still consume too much of the silicon substrate **101**, or result in too thin a silicide to provide a low enough sheet resistance.

FIG. **2** depicts schematic sectional views of a silicon substrate assembly structure in accordance with a preferred embodiment of the present invention. Referring to FIG. **2**A, an intermediate structure **200***a* is illustrated, in which a contact window is opened through an insulating layer **115** to expose an active area **102** of a silicon substrate **101**. As the

gates structures and insulating layer can be similar to those of FIG. **1**A, like reference numerals will be used to refer to like parts.

A metal source layer **202**, having an impurity therein, is deposited over the insulating layer **115** and the active area **102** through the contact window. Preferably, the impurity comprises nitrogen, and the metal source layer **202** comprises a metal-rich nitride. Most preferably, the metal source layer **202** comprises titanium-rich titanium nitride of the form TiN_x (x<1). Preferably x is between about 0.2 and 0.8, and most preferably between about 0.5 and 0.6. Methods of forming the preferred TiN_x layer **202** will be discussed in greater detail below. The metal layer **202** is preferably between about 50 Å and 800 Å, more preferably between about 300 Å and 400 Å. While the layer **202** is not pure metal, it may be referred to as a metal layer for convenience.

A silicon source layer **204** is deposited over the metal source layer **202**. As a result, the TiN_x layer **202** is interposed between the active area **102** of the silicon substrate **101** and the silicon source layer **204**, forming a sandwich structure. The silicon source layer **204**, which may comprise amorphous or polycrystalline silicon, is preferably between about 100 Å and 10,000 Å, more preferably about 1,000 Å. While in other arrangements the silicon source layer need not be purely silicon, the preferred layer **204** simply consists of polysilicon.

After forming the silicon layer **204** over the metal source layer **202**, the silicon **204** is preferably patterned, by conventional photolithography and silicon etch, in accordance with circuit design for the interconnect layer. Silicon **204** is thus left over the metal source layer **202** only where silicide interconnect is desired.

The structure **200***a* is then subjected to an anneal, preferably at between about 500° C. and 850° C., and more preferably between about 650° C. and 750° C., in a nitrogen ambient. During the annealing, metal and impurity atoms in the metal source layer **202** diffuse into the underlying active area **102** of the silicon substrate **101** and the overlying silicon layer **204**. Likewise, silicon diffuses into the metal source layer **202** from the underlying active area **102** and the overlying silicon layer **204**. Elementary titanium reacts with silicon from both sides and forms a titanium silicide, such that the process is a double-sided salicidation.

FIG. **2**B shows a structure **200***b* which is formed by annealing the structure **200***a* of FIG. **2**A. A silicide **206** is formed, comprising titanium nitride and titanium silicide. The resulting salicide layer **206** has sufficient thickness to provide low sheet resistance, preferably less than about 200 μΩ·cm. The titanium silicide layer **206** preferably has a thickness greater than about 200 Å, more preferably greater than about 300 Å, and most preferably greater than about 500 Å.

After silicide formation, unreacted metal can be removed in a selective metal wet etch, as will be reorganized by one of ordinary skill in the art. Thus, where silicon had been removed in the pre-silicidation patterning, described above, unreacted metal can be washed away.

Significantly, the salicidation does not consume the same amount of silicon from the underlying active area **102** and the overlying silicon layer **204**. The consumption of the underlying silicon area **102** is less than that of the overlying silicon layer **204**. In particular, salicidation of the preferred TiN_x layer **202** preferentially consumes overlying silicon relative to underlying silicon in a ratio of greater than about 1.2:1, more preferably greater than 2:1, and most preferably about 3:1. The salicidation occurs asymmetrically and thus does not destroy a shallow junction formed within the silicon substrate **101**. Accordingly, the portion of the self-aligned silicide **206** sinking below the surface of the substrate **102** represents less than about 30% of the total silicide thickness within the contact, preferably less than about 20%.

Preferably, the silicide **206** extends or intrudes below the original surface **101**' of the active area **102** by less than about 30% of the ultrashallow junction depth (e.g., less than about 300 Å of a 1,000 Å junction is consumed), more preferably less than about 25%, such that the transistor remains operable. It will be understood that, in other arrangements, the substrate surface from which the contact intrusion is measured can be that of a raised source/drain surface, and need not be coincident with the surface of a single crystal silicon wafer as shown.

It has been found that maximizing the bulk resistivity of the metal source layer **202** maximizes the asymmetry of silicide growth from the structure **200***a* of FIG. **2**A. In turn, the salicide method discussed above results in the maximum silicide thickness for a given amount of substrate consumption.

The metal source layer **202** can be formed by any of a number of techniques. For example, a metal layer can be doped with impurities after deposition, by diffusion or implantation techniques. Preferably, however, the metal source layer **202** is formed incorporating impurities during formation and most preferably during sputtering, although one of skill in the art can apply CVD methods in light of the present disclosure.

FIG. **3** relates to a preferred method for choosing an optimal region for sputtering of Ti in a N_2 and Ar ambient, thereby forming a TiN_x layer. Bulk resistivity of a titanium nitride layer is plotted as a function of N_2/Ar volume ratio in the reactive sputtering of Ti to form TiN_x at a given target power. As FIG. **3** illustrates, reactive sputtering of Ti falls into two main regions or realms. Sputtering with N_2/Ar ratio within Region I results in an unsaturated or titanium-rich titanium nitride of the form, TiN_x (x<1), while sputtering within Region II results in a saturated or standard TiN. Point A thus represents the flow ratio for which the highest bulk resistivity titanium-rich TiN_x is achieved, which, in turn, reflects a highly uniform distribution of nitride nuclei throughout Ti film. Beyond this point, nuclei begin to grow and eventually contact one another, causing bulk resistivity to drop. Then the saturated region or Region II begins, wherein no titanium is available for salicidation. Resistivity again rises within this region as excess nitrogen interferes with conductivity. Points B and C represent lower and higher flow ratios, respectively, which result in a TiN_x film of about 15% lower bulk resistivity than a film formed at peak A. This range of ratios represents a preferred processing window.

Absolute ratios in FIG. **3** depend upon the sputtering power. For example, with 2.0 kW sputtering power, 35 sccm of Ar and 7–8 sccm of N_2 result in a maximum Region I resistivity of about 270 μΩ-cm. The TiN_x resulting from this N_2/Ar ratio has x approximately equal to 0.6. Increasing sputtering power gives smaller TiN_x nucleates, and reducing power gives larger TiN_x nucleates. Higher sputtering power thus flattens out the peak A. It will be understood, in light of the present disclosure, that at higher sputter power, a larger window of preferred N_2/Ar ratios is available. In general, sputtering with a ratio closer to point A results in a better the TiN_x distribution uniformity, which in turn results in greater salicide thickness uniformity after silicidation. Typically, x is around 0.5 or 0.6 at point A. It can be 0.2 to 0.8 between point B to point C when higher or lower sputtering power is used.

FIGS. **4**A to **4**D illustrate X-ray photoelectron spectroscopic profiles of integrated circuits of the present invention, illustrating the consumption of silicon from the active area **102** of the silicon substrate **101** and the overlying silicon layer **204**. Wafers of silicon assembly structures having 1,000 Å α-Si/400 Å TiN_x/Si substrate and 1,000 Å α-Si/300 Å TiN_x/Si substrate were subjected to rapid thermal processing ("RTP") at different temperatures. The metal source layers **202** of the wafers were deposited by reactively sputtering a titanium target at the N_2/Ar ratio of point A, as described above. X-ray photoelectron spectroscopic ("XPS") profiles for 1000 Å α-Si/400 Å TiN_x/Si substrate structures are shown.

FIG. **4**A is a profile of the sandwich structure prior to annealing. At the center of FIG. **2**A, titanium and nitrogen atoms forming the preferred metal source layer **202** are shown between silicon-rich areas. Trace elements are omitted.

FIG. **4**B is a profile for the structure annealed at 675° C. for 10 seconds. About 515 Å of silicon remains after the RTP. FIGS. **4**C and **4**D are profiles of similar structures annealed at 710° C. and 790° C., respectively, for 20 seconds each. As can be seen in the FIGS. **4**B to **4**D, titanium is found asymmetrically toward the left of the profile (representing points above the substrate) after the anneal. Total atomic percentage analysis results reveal asymmetric characteristic of double-sided salicide formation at temperatures from 675° C. to 790° C. Clearly, salicide formation consumes more of the silicon source layer (α-Si or poly-Si) deposited over the metal source layer than silicon substrate below the metal source layer. The titanium salicide profiles remain stable between 675° C. and 790° C. The profiles of a sandwich structure using 300 Å of TiN_x as the metal source layer are similar to the profiles shown in FIGS. **4**A to **4**D, except that they consume even less (about 20% less) of the silicon substrate.

FIG. **5** shows curve-fitting results of the X-ray photoelectron spectroscopy profiles of FIGS. **4**A and **4**B to quantitatively analyze the degree of asymmetry of the preferred double-sided salicidation. As can be seen, the salicidation of titanium consumes the overlying silicon layer **204** at least twice as much as it consumes the silicon substrate **101**. A comparison of the titanium profile prior to anneal with the silicide profile after anneal shows consumption of less than 225 Å of the silicon substrate **101** (represented by a shift to the right), whereas about 450 Å of the overlying silicon layer **204** (represented by a shift to the left) is consumed. For the process using 300 Å of TiN_x, not shown, consumption of the substrate is down to 180 Å. This low consumption (representing less than 25% and even less than 20% with use of 300 Å TiN_x layer) is very important for ultrashallow junction applications. For 750–1,000 Å junctions, the source/drain contact should preferably consume less than about 300 Å, more preferably less than about 250 Å, of silicon substrate to reduce leakage. At the same time, the salicide total thickness is preferably at least about 300 Å, more preferably at least about 500 Å, to form sufficiently low contact resistance, thermally and dynamically stable in the face of post-silicidation anneal (converting the grain to C54 orientation) and other high temperature processes.

As also apparent from FIGS. **4** and **5**, the resultant metal silicide contact contains the impurity which was incorporated into the metal source layer. In particular, nitrogen is present in the titanium silicide layer, preferably comprising between about 5% and 80% of the silicide layer **206** (FIG. **2**B), more preferably comprising about 10% to 30%, and most preferably in the range of about 15% to 20%. The XPS profiles of FIG. **4** indicate a slightly lower percentage of nitrogen than actual, due to preferential readings by the measuring apparatus.

Referring to FIGS. **6**A and **6**B, a conventionally-formed self-aligned silicide contact is shown after a high temperature glass reflow, typically conducted at about 750° C. for about 10 minutes. FIG. **6**A shows an X-SEM of an actual device after furnace reflow, where the contact was formal by sintering a sandwich structure with 300 Å pure titanium between a silicon substrate and a 1,000 Å polysilicon layer. The wafer was run through the entire device fabrication process flow, including furnace reflow at 750° C., after forming the salicide contact. As can be seen in FIG. **6**A, a silicide crater can be found after reflow at 750° C. The crater is more than 1,000 Å deep, such that an ultrashallow junction would be destroyed. FIG. **6**B schematically illustrates the structural deformation. The structure **100***b* of FIG. **1**B is shown after furnace reflow. The structure **100***c* of FIG. **6**B shows that a part of silicide **118'** extends even further into the active area **102** after reflow.

In contrast, actual devices were constructed in accordance with the preferred embodiment, and put through furnace reflow at different temperatures. X-SEM results showed no such crater on wafers processed with either 300 Å TiN_x or 400 Å TiN_x layers. The $TiSi_x$/Si interface remained smooth and intact. The crater in salicide contacts formed conventionally is believed to be associated with tendency of $TiSi_x$ large grain formation to reduce surface energy and effect of agglomeration at high temperature. Formation of excessively large grains is drastically suppressed by the preferred embodiments, however, by incorporating TiN_x nuclei into $TiSi_x$ film.

The intermediate assembly structure having a TiN_x (x<1) layer and a silicon layer (see FIG. **2**A) over the silicon substrate enables asymmetric salicidation (FIG. **2**B). The asymmetric salicidation enables self-aligned formation of suicides thick enough to provide low contact resistance, while consuming less than about 300 Å, more preferably less than 250 Å, of the silicon substrate. The process preferably consumes greater than 1.2, more preferably greater than 2 times more silicon from the overlying silicon layer than from silicon substrate. This asymmetric salicidation facilitates self-aligned contact metallization for an ultrashallow junction (<1,000 Å), consuming less than 30% and preferably less than about 20% of the junction while providing adequately low resistivity contacts. This unique titanium silicide contact also has a much higher thermal stability than conventionally-formed self-aligned silicide.

Although the foregoing invention has been described in terms of certain preferred embodiments, other embodiments will become apparent to those of ordinary skill in the art, in view of the disclosure herein. Accordingly, the present invention is not intended to be limited by the recitation of preferred embodiments, but is instead intended to be defined solely by reference to the appended claims.

I claim:

1. An integrated circuit comprising:

a silicon substrate having an upper surface; and

a self-aligned contact comprising a metal silicide layer, having a metal silicide thickness, the metal silicide layer extending into the substrate below the upper surface of the substrate by an amount less than about 30% of the metal silicide thickness.

2. The integrated circuit of claim **1**, wherein the metal silicide layer extends into the substrate below the upper surface of the substrate by an amount less than about 20% of metal silicide thickness.

3. The integrated circuit of claim 1, wherein the metal silicide layer extends into the substrate below the upper surface of the substrate by less than about 250 Å.

4. The integrated circuit of claim 1, wherein the metal silicide layer includes metal nitride interspersed therein.

5. The integrated circuit of claim 4, wherein a nitrogen content of the metal silicide layer is between about 10% and 30%.

6. The integrated circuit of claim 1, wherein the silicon surface overlies a source/drain active area having a junction depth of no more than about 1,000 Å, and the metal silicide layer extends into the active area to a depth less than about 30% of the junction depth.

7. The integrated circuit of claim 1, wherein the metal silicide layer has a sheet resistance of less than about 200 $\mu\Omega$cm.

8. A self-aligned silicide contact extending below a substrate surface into a shallow junction transistor active area, the active area having a junction depth of no more than about 1,000 Å, the contact extending below the substrate surface into the active area by no more than about 30% of the junction depth.

9. The self-aligned silicide contact of claim 8, wherein the contact extends below the substrate surface into the active area by no more than about 25% of the junction depth.

10. The self-aligned silicide contact of claim 9, wherein the contact extends below the substrate surface into the active area by no more than about 20% of the junction depth.

* * * * *

EXHIBIT E

US006469336B2

(12) **United States Patent**
Deboer et al.

(10) **Patent No.: US 6,469,336 B2**
(45) **Date of Patent: Oct. 22, 2002**

(54) **STRUCTURE FOR REDUCING CONTACT ASPECT RATIOS**

(75) Inventors: **Scott J. Deboer**, Boise, ID (US); **Vishnu K. Agarwal**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/912,649**

(22) Filed: **Jul. 23, 2001**

(65) **Prior Publication Data**

US 2001/0045658 A1 Nov. 29, 2001

Related U.S. Application Data

(62) Division of application No. 09/334,842, filed on Jun. 16, 1999, now Pat. No. 6,365,453.

(51) **Int. Cl.**[7] **H01L 27/108**
(52) **U.S. Cl.** **257/301**; 438/253
(58) **Field of Search** 432/253, 396, 432/656, 303–305; 257/301–306, 309

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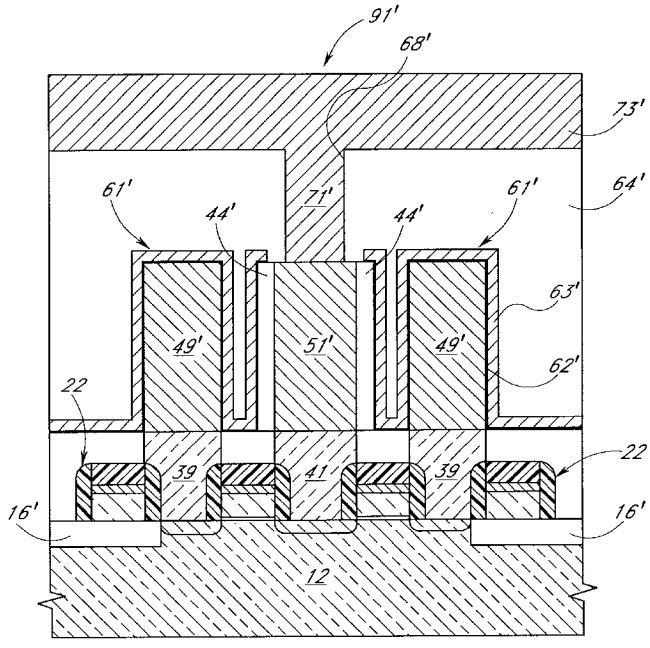
Assistant Examiner—Dung A Le
(74) *Attorney, Agent, or Firm*—Knobbe, Martens, Olson & Bear LLP

(57) **ABSTRACT**

An intermediate metal plug is used to raise the platform to which contact is to be made. In the illustrated process, a partial bit line plug is formed adjacent a stacked capacitor, and an interlevel dielectric formed over the capacitor. The bit line contact is completed by extending a via from the bit line, formed above the interlevel dielectric, down to the level of the intermediate plug, and the via is filled with metal. The height of the via to be filled is thus reduced by the height of the intermediate plug. In one embodiment, the intermediate plug is slightly shorter than an adjacent container-shaped capacitor. In another embodiment, the intermediate plug is about as high as an adjacent stud capacitor.

12 Claims, 9 Drawing Sheets



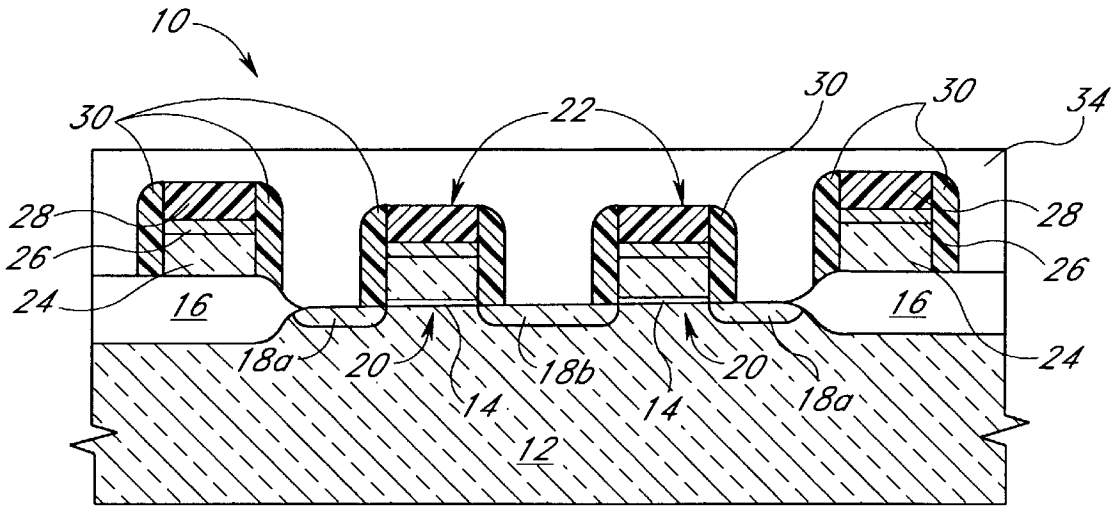

10
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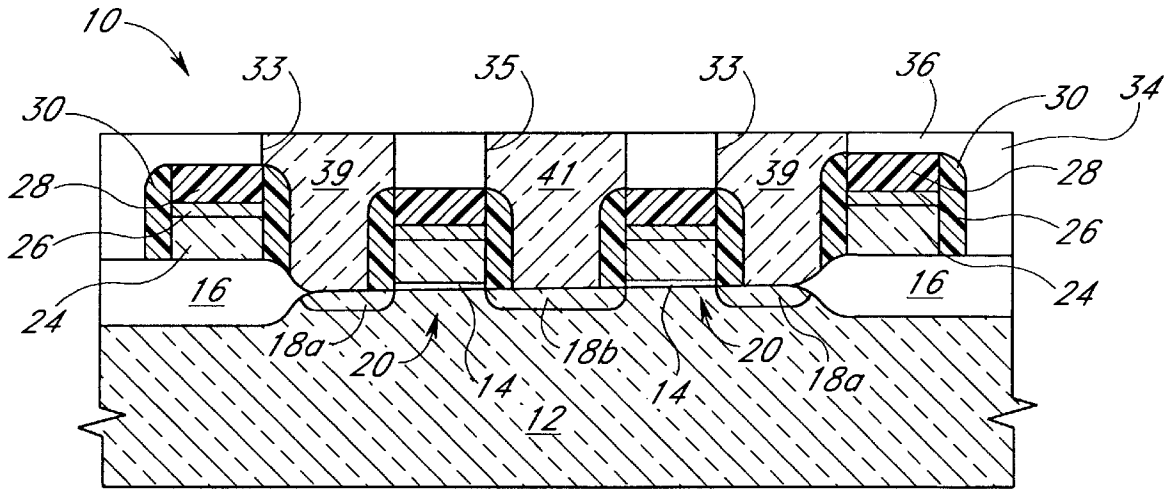
FIG. 1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14
18b
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18a
16
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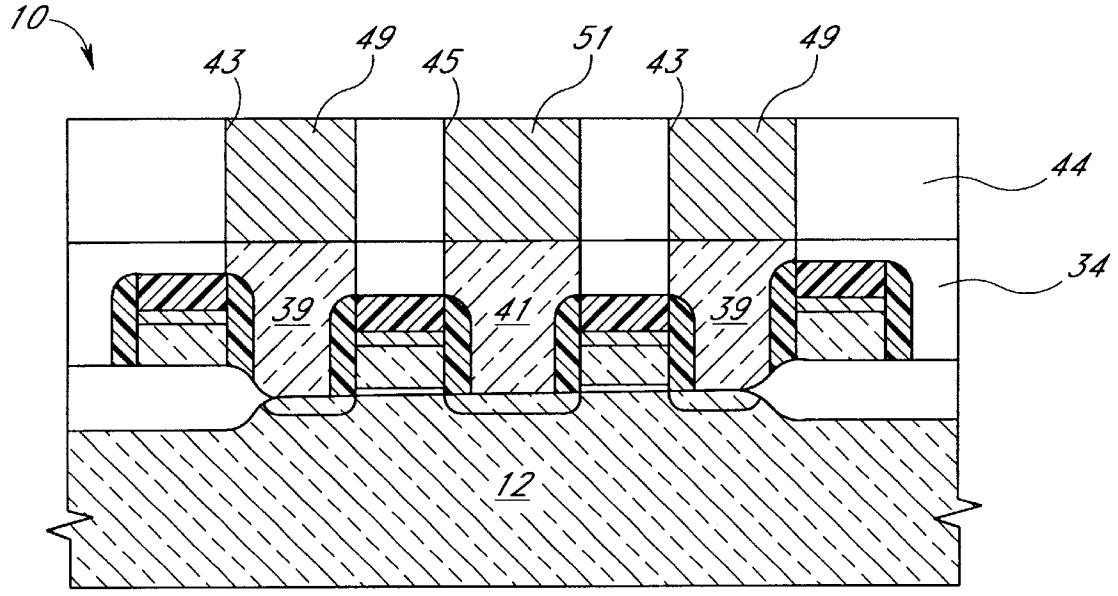
FIG. 2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49
45
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34
39
41
39
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FIG. 3A

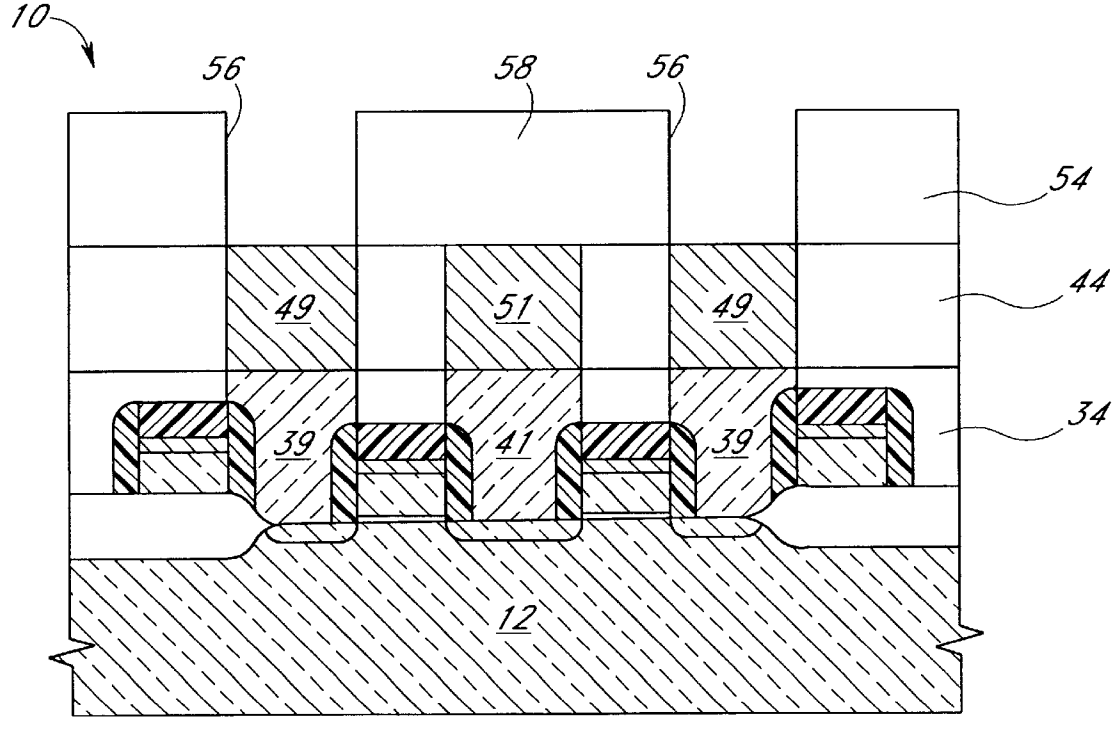
10
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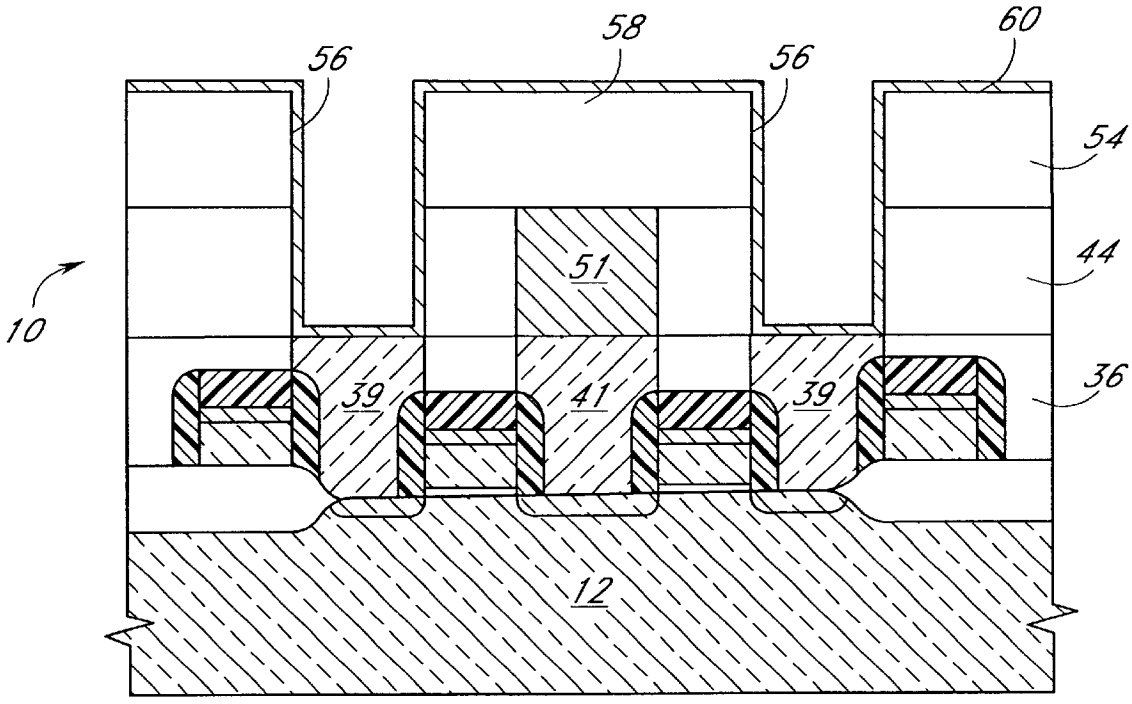
FIG. 3B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60
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10
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FIG. 4

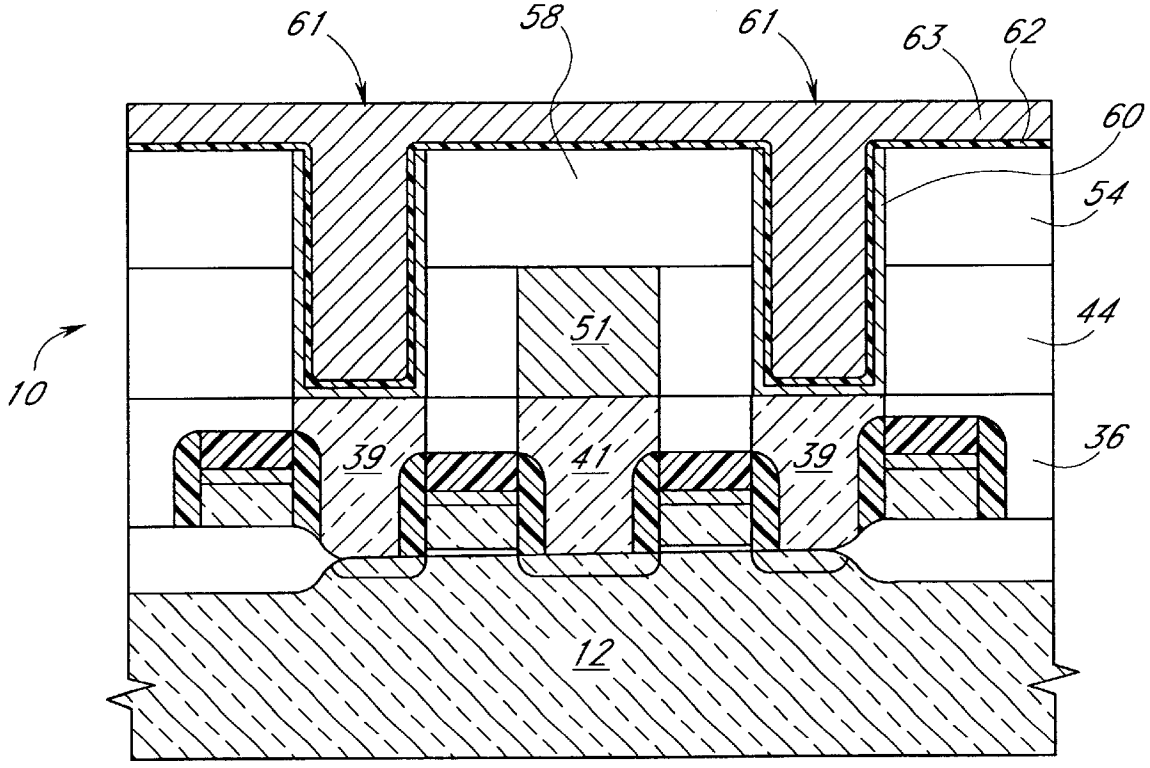
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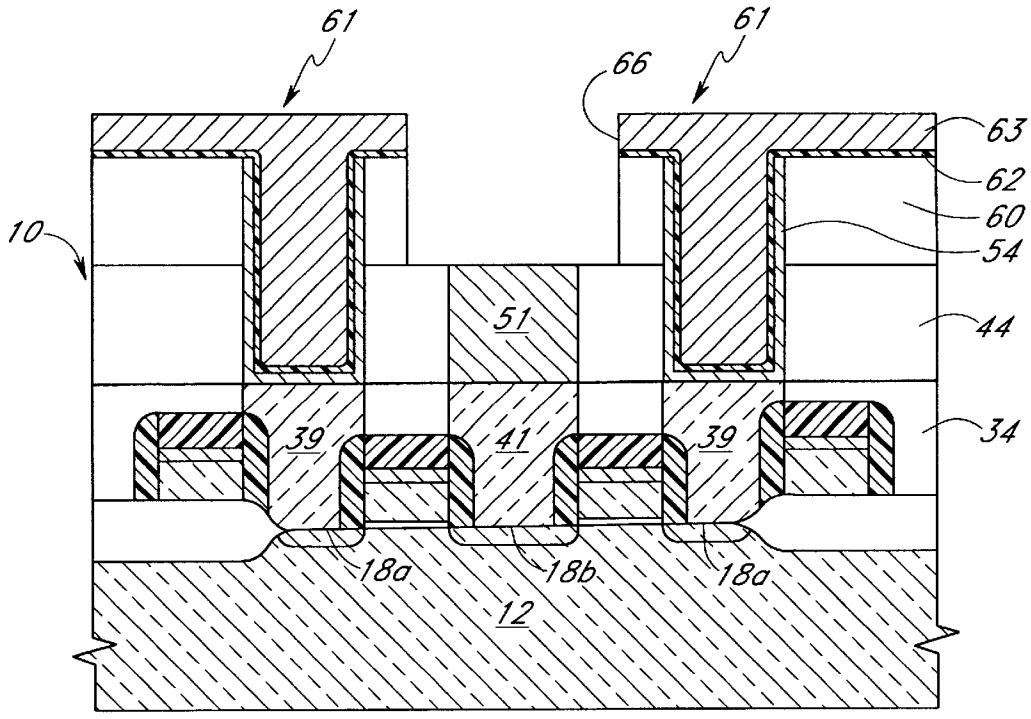
FIG. 5


61
61
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63
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41
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34
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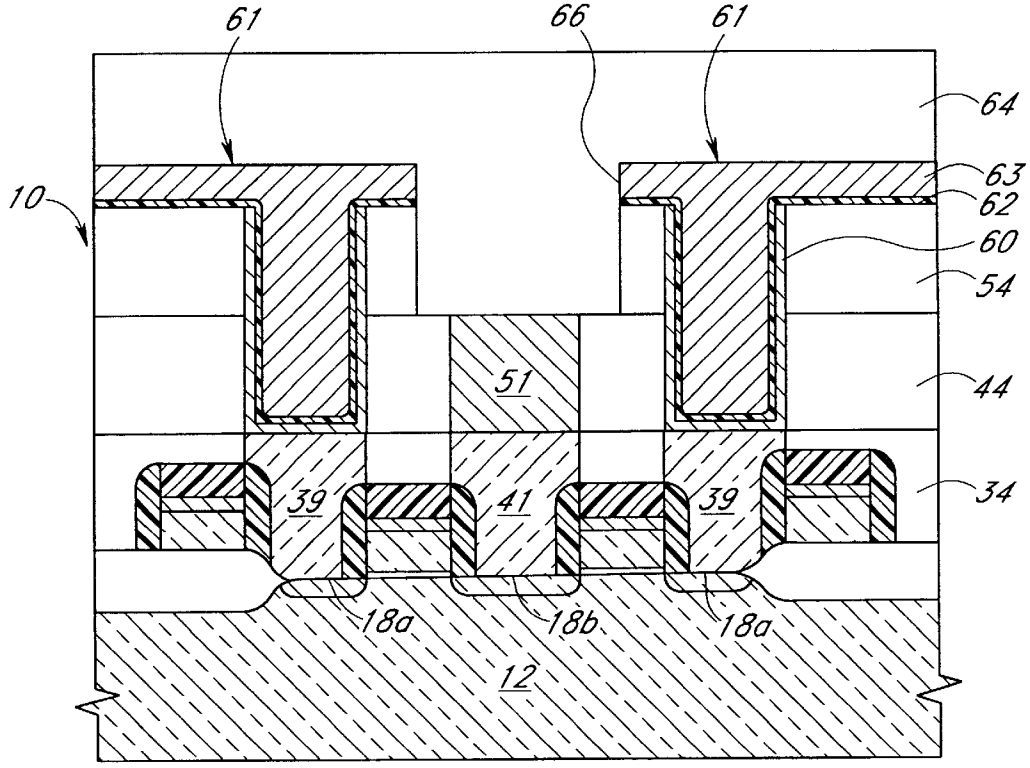
FIG. 6


61
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63
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18b
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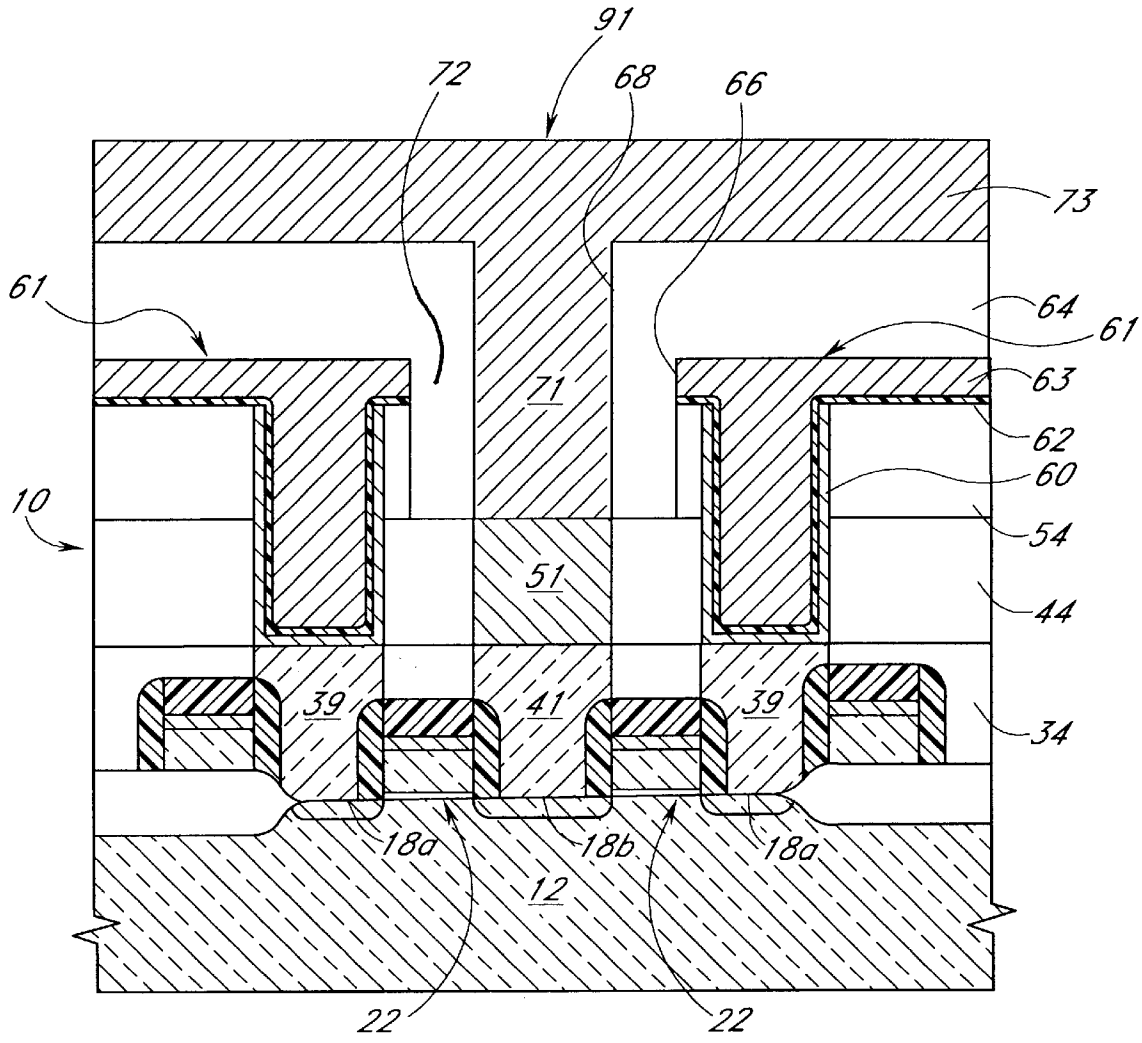
FIG. 7


91
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10
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34
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FIG. 8

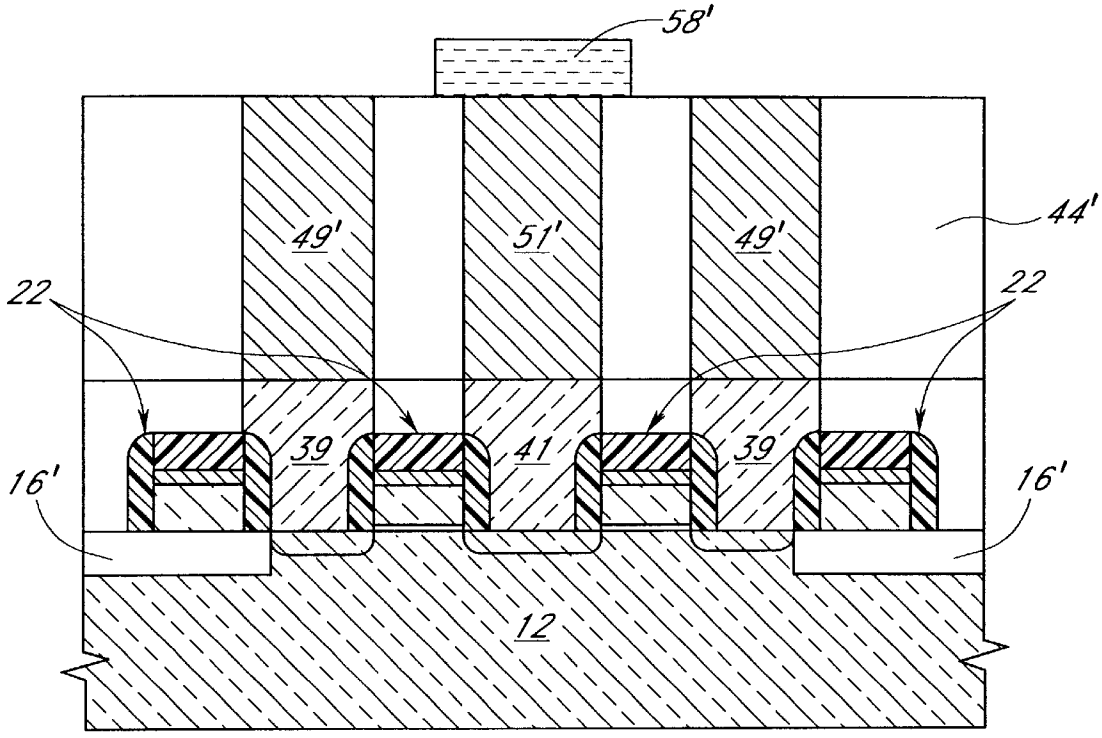
58'
49'
51'
49'
44'
22
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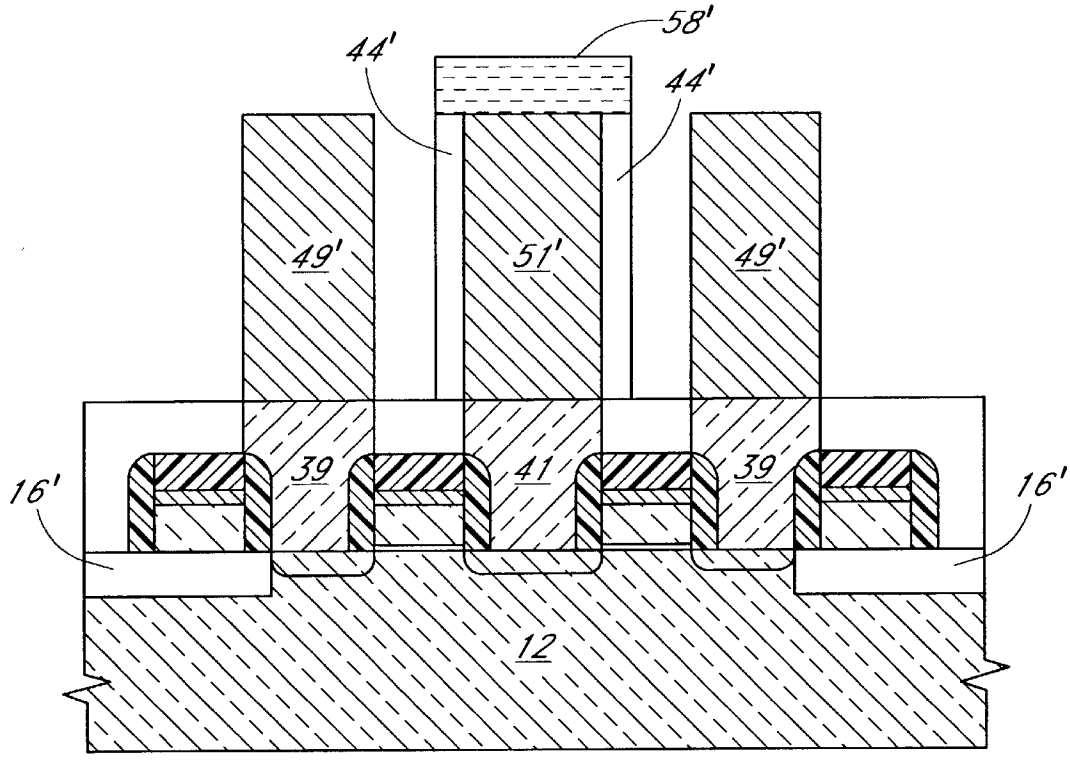
FIG. 9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12

FIG. 10

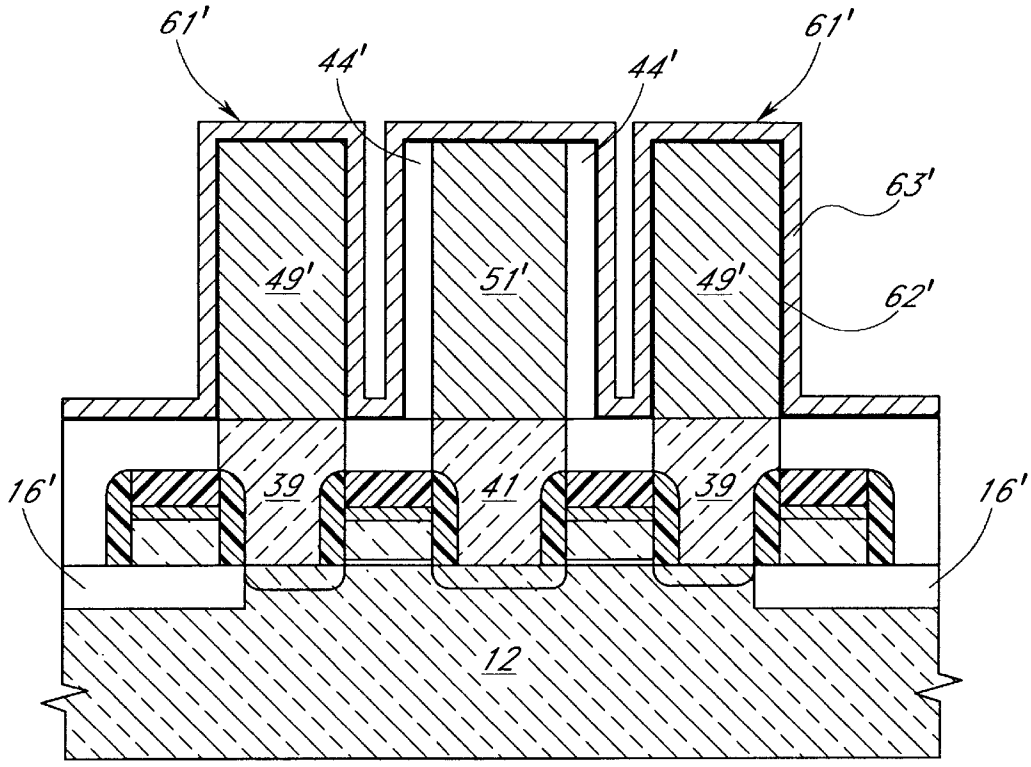
61'
44'
44'
61'
63'
49'
51'
49'
62'
16'
39
41
39
16'
12

FIG. 11

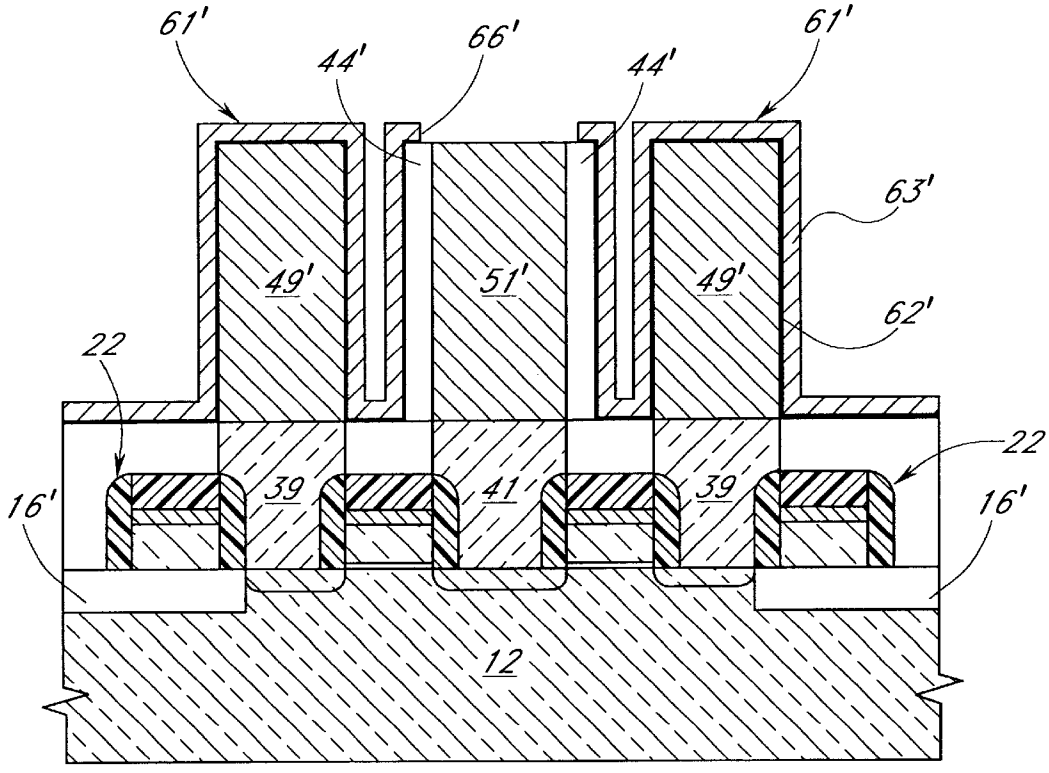
61'
44'
66'
44'
61'
63'
49'
51'
49'
62'
22
22
16'
39
41
39
16'
12

FIG. 12

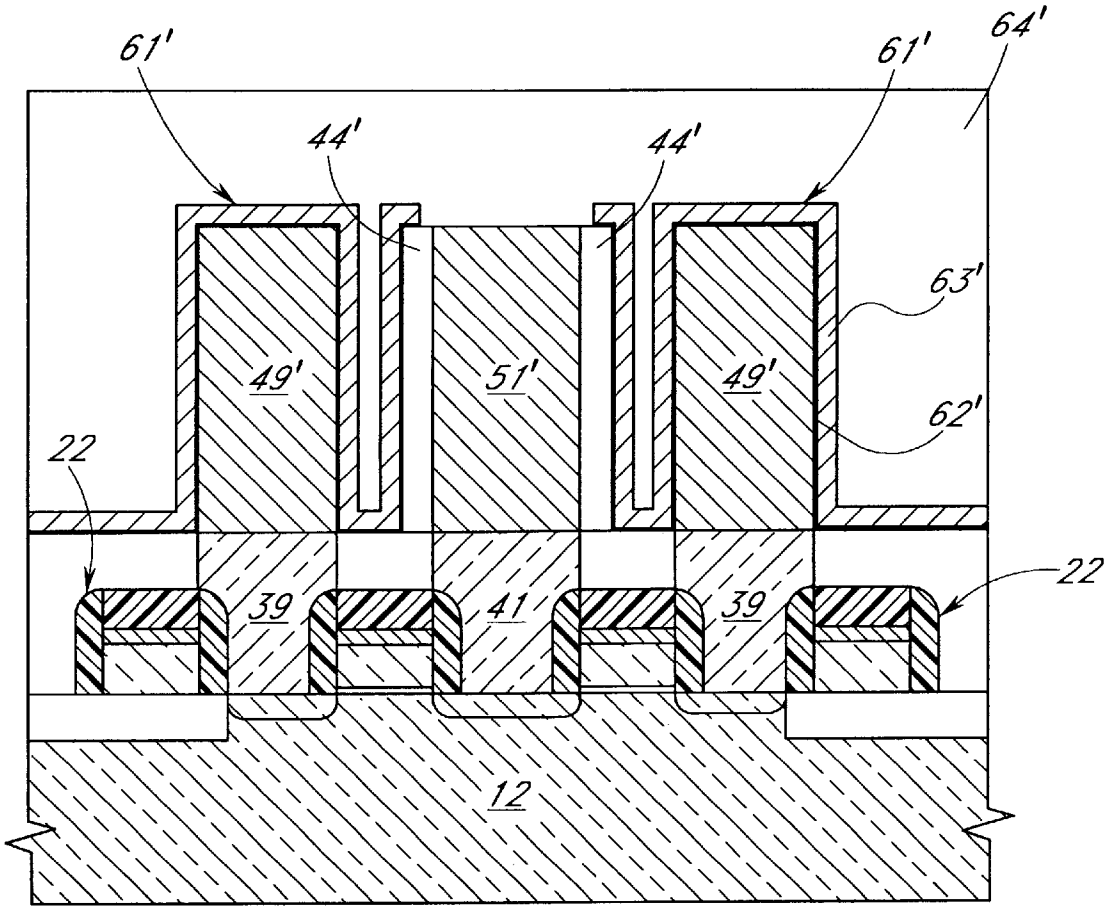

FIG. 13

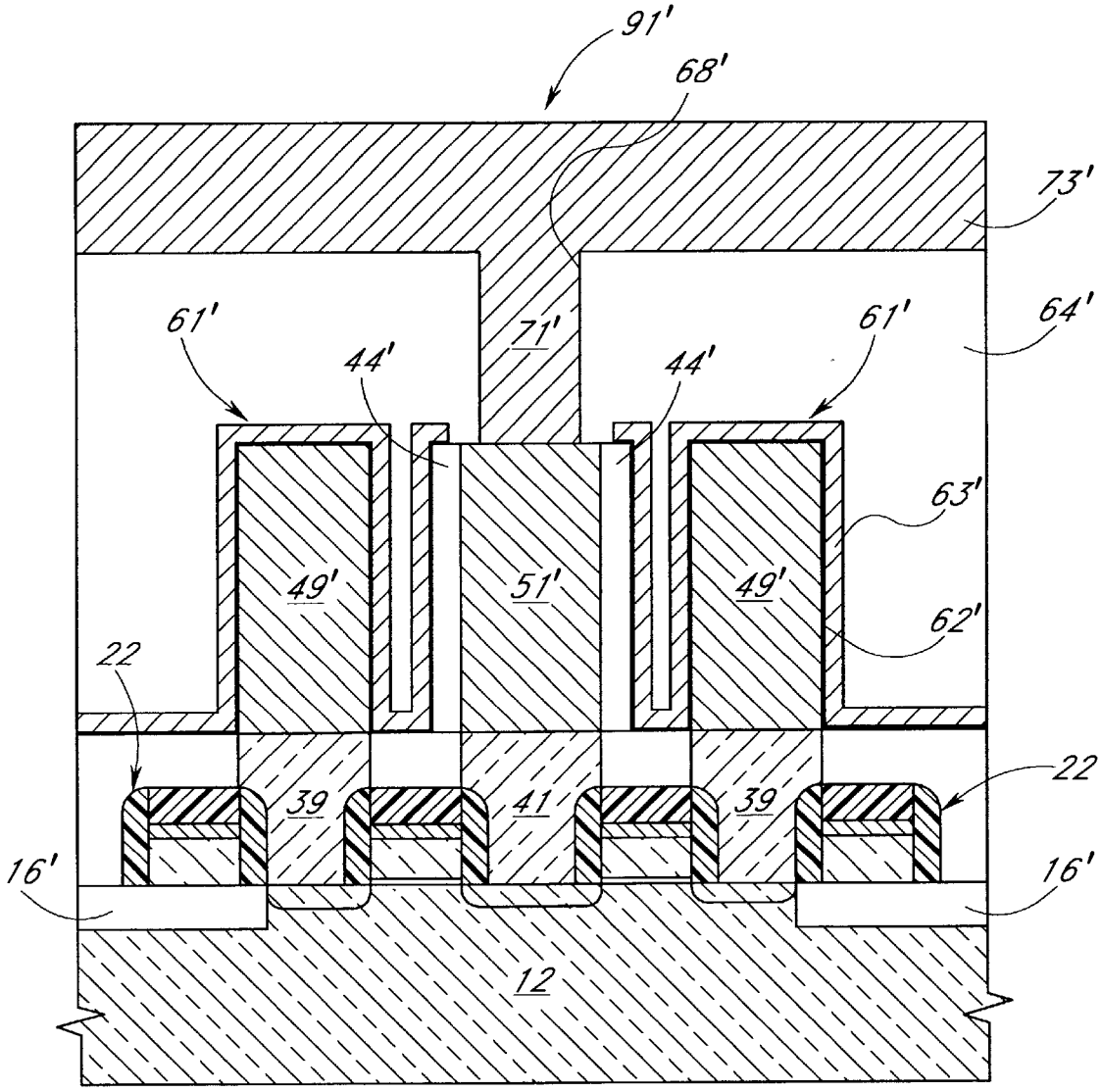

FIG. 14

STRUCTURE FOR REDUCING CONTACT ASPECT RATIOS

Reference to Related Application

The present application is a divisional of U.S. patent application Ser. No. 09/334,842, by deBoer et al., filed Jun. 16, 1999 now U.S. Pat. No. 6,365,453 and assigned to Micron Technology Inc., the assignee of the present application.

FIELD OF THE INVENTION

The present invention relates generally to the formation of contacts in integrated circuits, and more particularly to a method of forming bit line contacts in dynamic random access memory chips.

BACKGROUND OF THE INVENTION

Integrated circuits, also commonly referred to as semiconductor devices, are formed of various electrically conducting, semiconducting and insulating materials. Silicon, in single crystal, amorphous or polycrystalline form, is the most commonly used semiconductor material. Silicon can be made electrically conductive by adding impurities, commonly referred to as doping. Through a series of doping, deposition and etch steps, electrical devices are formed and interconnected to produce the integrated circuits.

Dynamic random access memory (DRAM) circuits include arrays of memory cells, each of which includes two basic components: a field effect transistor (FET) and a storage capacitor. Typically, a semiconducting substrate is doped to produce active areas of an access transistor, one of which is connected to the lower or storage electrode of the capacitor. The other active area and the transistor gate electrode are connected to external connection lines, namely digit or bit lines and word lines or rows. The top or reference electrode of the capacitor is connected to a reference voltage. DRAM arrays thus include a transistors, capacitors and contacts to interconnecting lines.

It is advantageous to form integrated circuits with smaller individual elements so that as many elements as possible may be formed in a single chip. In this way, electronic equipment becomes smaller and more reliable, assembly and packaging costs are minimized and circuit performance is improved. In particular, denser device packing leads to faster and more efficient circuit operation. Despite the focus on continued miniaturization, the storage capacity of the cell capacitor must generally remain above a minimum level to ensure reliable operation (low error rates). Consequently, the development of faster and more powerful DRAM chips focuses in large part on maintaining capacitance despite shrinking available chip area for each memory cell.

One way in which capacitance has been increased has been to increase the surface area of the capacitor electrodes by creating three-dimensional folding structures to which the electrodes conform. When the capacitor is formed above the transistors, they are known in the industry as "stacked" capacitors. Stacked capacitors advantageously demonstrate high capacitance per unit of occupied chip area ("footprint"), high reliability and simple process integration relative to other capacitor designs.

As noted, in the process of fabricating a DRAM chip, electrical connections must be made to the transistor active areas. The active areas, which are also known as source and drain regions, are discrete doped regions in the surface of the semiconductor substrate. As the size of the DRAM is

reduced, the size of the active areas and the corridors available for contacts to reach the active areas are also reduced. At the same time, insulating materials must be maintained to effectively isolate the contacts from the transistor and capacitor components. Accordingly, the width of bit line contacts, and other integrated contacts generally, must shrink as device packing density increases.

Unfortunately, while contact width continually decreases, contact height cannot decrease proportionately. Rather, the contact height is defined by the thickness of the interlevel dielectric (ILD) which separates the two levels in the circuit, such as the substrate and higher wiring levels. The ILD thickness, in turn, must be maintained to minimize the risk of short circuits, as well as to prevent interlevel capacitance, which can tie up electrical carriers and slow signal propagation.

Relative increases in contact height is particularly acute in DRAM circuit designs which incorporate stacked capacitors. As noted, capacitance is proportional to the surface area, which depends on both height and width. In order to maintain the same or higher level of capacitance from generation to generation, the capacitor height must remain the same or even increase as device spacing decreases. In bit-over-capacitor (BOC) designs, the bit line contact increases in height along with the capacitor.

While contact width decreases and contact height is essentially maintained, the aspect ratio (defined as the ratio of height to width of a contact) of contacts continues to increase. In general, therefore, each successive generation of integrated circuits contacts of higher aspect ratios, and this is particularly true for certain DRAM circuit designs. As is well known in the art of integrated circuit fabrication, high aspect ratio contact vias are very difficult to fill without forming keyholes.

One partial solution to this problem is to reduce the dielectric constant of the ILD. A lowered dielectric constant enables thinning ILDs for a given tolerable parasitic capacitance, and consequently lowers the aspect ratio. This solution, however, can only be carried so far before the dielectric loses its insulating qualities, or the risk of short circuits through the thinned ILD becomes too high. Moreover, this solution does not address the high aspect ratios of bit line contacts necessitated by high stacked capacitors in bit-over-capacitor DRAM circuit designs.

Accordingly, a need exists for more effective methods of forming contacts between levels in integrated circuits.

SUMMARY OF THE INVENTION

In accordance with a disclosed embodiment, intermediate conductive plugs raise the platform from which a contact extends. In DRAM fabrication, for example, a partial bit line plug is formed adjacent a stacked capacitor, and an interlevel dielectric formed over the capacitor. The bit line contact is completed by extending a via from the bit line, formed above the interlevel dielectric, down to the level of the intermediate plug, and the via is filled with metal. The height of the via to be filled is thus reduced by the height of the intermediate plug.

In one embodiment, sacrificial plugs are simultaneously formed adjacent the intermediate metal plugs. The sacrificial plugs can be selectively removed, while the intermediate plugs are shielded from etch, and the capacitors formed in the resulting container. In another embodiment, the bottom electrodes for stud capacitors are simultaneously formed adjacent the intermediate metal plugs.

In accordance with one aspect of the invention, therefore, an integrated circuit contact is provided. The integrated

circuit includes an electronic device formed above a semiconductor substrate, extending from a first level to a second level. A conducting line overlies the electronic device, electrically insulated by an interlevel dielectric. A contact plug extends downwardly through the interlevel dielectric to an intermediate level above the first level, while remaining electrically insulated from the direct contact with the electronic device.

In accordance with another aspect of the invention, a method is provided for forming electrical contact between levels in an integrated circuit. A conductive plug is formed and covered with a shield. While the plug remains covered, an electrical device is at least partially formed adjacent the conductive plug. After the shield is opened, a contact is then extended to directly contact the conductive plug.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will be readily apparent from the attached detailed description, claims and drawings, wherein like numerals will be used to refer to like parts, and in which:

FIG. **1** is a partial, schematic, sectional view of a partially fabricated integrated circuit, constructed in accordance with a preferred embodiment of the present invention, having a plurality of transistors formed therein and a first interlevel dielectric covering the transistors;

FIG. **2** shows the integrated circuit of FIG. **1** after a plurality of conductive plugs are formed through the first interlevel dielectric to contact the transistor active areas;

FIG. **3**A shows the integrated circuit of FIG. **2** after a second interlevel dielectric layer is formed and conductive plugs formed therethrough to electrically contact the underlying plugs;

FIG. **3**B shows the integrated circuit of FIG. **3**A after a third interlevel dielectric layer has been deposited and etched to expose certain of the underlying conductive plugs, while shielding other conductive plugs;

FIG. **4** illustrates the integrated circuit of FIG. **3**B after the exposed conductive plugs have been removed, and a conformal conductive layer deposited over the wafer;

FIG. **5** illustrates the integrated circuit of FIG. **4** after the conformal conductive layer has been patterned to define capacitor bottom electrodes, and capacitor dielectric and top electrode layers deposited thereover;

FIG. **6** illustrates the integrated circuit of FIG. **5** after a window has been formed through the top electrode;

FIG. **7** illustrates the integrated circuit of FIG. **6** after a fourth interlevel dielectric has been deposited;

FIG. **8** shows the integrated circuit of FIG. **7** after formation of a bit line contact through the window;

FIG. **9** is a partial, schematic, sectional view of a partially fabricated integrated circuit, constructed in accordance with another embodiment of the invention, having a plurality of aligned conductive plugs formed through two interlevel dielectric layers that cover the transistors;

FIG. **10** shows the integrated circuit of FIG. **10** after the second interlevel dielectric has been substantially removed, except for sidewall spacers surrounding a partial bit line plug;

FIG. **11** shows the integrated circuit of FIG. **10** after formation of capacitor dielectric and top electrode layers;

FIG. **12** shows the integrated circuit of FIG. **11** after a window has been opened in the top electrode and capacitor dielectric over the partial bit line plug;

FIG. **13** shows the integrated circuit of FIG. **12** after a third interlevel dielectric has been deposited; and

FIG. **14** shows the integrated circuit of FIG. **13** after extension of the bit line plug and formation of a bit line.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the preferred embodiment is described in the context of a bit line contact in a dynamic random access memory array, the skilled artisan will find application for the described invention in a variety of other contexts. The process and structures described herein have particular utility for forming electrical contacts through intermediate levels in integrated circuits.

Referring to FIG. **1**, a partially fabricated integrated circuit will be referred to as a wafer **10** for convenience. The wafer **10** includes a semiconductor substrate **12**, gate insulating layers **14** and field isolation regions **16**, as will be understood by the skilled artisan. The illustrated isolation regions **16** comprise field oxide grown by local oxidation of silicon, or LOCOS, though other isolation techniques are also contemplated (e.g., shallow trench isolation, or STI). While the illustrated substrate **12** comprises the upper portions of a single-crystal silicon wafer, the skilled artisan will appreciate that the substrate will generally comprise a semiconductor layer or structure in which active or operable portions of electronic devices are formed.

Impurities are diffused or implanted in the surface of substrate **12** to form source/drain regions **18***a* and **18***b* for access transistors **20**. Transistor gate electrodes **22** of the illustrated embodiment include a polysilicon layer **24**, a tungsten silicide layer **26** and a protective cap layer **28**. Insulating spacers **30** are formed on either side of the transistor gate electrodes **22**. The cap layer **28** and insulating spacers **30** are preferably made of silicon nitride. The skilled artisan will understand, however, that the compositions of the gate stacks and other lower device elements are not central to the invention and can take a variety of forms. Further details are omitted for simplicity.

A first interlevel dielectric (ILD) layer **34** is then deposited over the transistors **20** and is preferably planarized. The illustrated first ILD **34** comprises borophosphosilicate glass (BPSG), although the skilled artisan will readily appreciate that many other materials are suitable for use as an ILD, such as TEOS, spin-on glass (SOG), and polyamide. The first ILD **34** is deposited to a thickness adequate to electrically isolate the underlying transistors **20**, preferably between about 0.2 μm and 0.8 μm.

Referring to FIG. **2**, the lower insulating layer **34** is patterned and etched to define contact vias **33** and **35**, exposing the substrate **12** at the active areas **18***a* and **18***b*, respectively. This etch is preferably an anisotropic reactive ion etch (RE), which advantageously produces vertical sidewalls, allowing for tighter packing densities. The contact vias **33**, **35** are filled with conductive material and recessed or planarized to form capacitor contact plugs **39** (over which cell capacitors are to be formed) and first bit line contact plugs **41** (over which the bit line contacts are to be formed). Typically, such plugs are formed by chemical vapor deposition (CVD) of conductive materials such as tungsten or polysilicon into the vias **33**, **35**, for good step coverage into the tight confines between the gate electrodes **22**. In the illustrated embodiment, the plugs **39**, **41** are formed of polysilicon, which advantageously integrates well with the active areas **18** of the substrate **12**.

Referring to FIG. **3**A, a second ILD **44**, also preferably comprising BPSG, is deposited over the first ILD **34** and

plugs **39**, **41**. The thickness of the second ILD **44** is determined by design and operational considerations, such as the desired overall height of the cell capacitors. As will be understood in view of the entirety of the disclosed process, the second ILD **44** defines the amount by which the contact height is reduced. Preferably, the second ILD **44** is greater than about 20% of the overall desired height of the adjacent electrical devices (cell capacitors), and more preferably greater than about 50% of the overall desired height. In the illustrated embodiment, the second ILD **44** has a preferred thickness between about 0.8 μm and 2.0 μm, and more preferably between about 1.0 μm and 1.5 μm.

The second ILD **44** is patterned and etched to define vias **43**, **45** over the plugs **39**, **41**, which vias are then filled and recessed or planarized to form sacrificial capacitor plugs **49** and second bit line plugs **51** (one shown). The same mask may be employed as was used for the first vias **33**, **35**, as illustrated, thereby aligning the plugs **49** with the underlying capacitor contact plugs **39**, and saving the costs of an additional mask design. Preferably, however, the sacrificial capacitor plugs **49** are made wider than the underlying contact plugs **49**, since more space exists above the tightly packed gate electrodes. A greater width for these plugs will allow for greater capacitance, as will be understood in light of the disclosure hereinbelow. The sacrificial plugs **49** are preferably elliptical, where one dimension is between about 0.25 μm and 0.60 μm and a second dimension is between about 0.10 μm and 0.40 μm. The elliptical configuration advantageously maximizes use of available space for the cell capacitor.

It will also be understood that the second bit line contact plug **51** need not have the same width as the sacrificial capacitor plugs **49**, and similarly for the underlying plugs **39**, **41**. The width of the second bit line plug **51** is preferably between about 0.10 μm and 0.30 μm and more preferably between about 0.15 μm and 0.25 μm.

While not individually illustrated, the plugs **49**, **51** formed in the second ILD **44** preferably include a plurality of layers. For example, a first lining layer of refractive metal (e.g., titanium, tanatalum, cobalt, nickel) is preferably first deposited into the vias, to form a silicide with the polysilicon of the underlying plugs **39**, **41** and to assist adhesion to the BPSG sidewalls of the vias. A layer of metal nitride (e.g., TiN) preferably follows, to form a diffusion barrier. Such liners for metal plugs are well known and need not be detailed here. Furthermore, additional features, such as etch stop layers, may be incorporated into the process flow to facilitate alignment of the plugs, as will be appreciated by the skilled artisan.

A conductive filler material is then deposited into the lined vias and recessed or planarized to complete the plugs **49**, **51**. The filler preferably comprises CVD tungsten, but may also comprise other materials such as force-fill aluminum, hot aluminum, or any other suitable conductive material. In other arrangements, particularly where high dielectric constant materials are employed, non-oxidizing conductors such as Ru, RuO_x, Pt, Ir, IrO_x, etc. are preferred.

With reference now to FIG. **3**B, a third ILD **54**, also preferably comprising BPSG, is formed over the second ILD **44** and the plugs **49**, **51**. In the illustrated embodiment, the thickness of the third ILD **54** is selected, in combination with the thickness of the second ILD **44**, to complete the desired height of the cell capacitor. The illustrated third ILD **54** is thus preferably between about 0.8 μm and 2.0 μm, and more preferably between about 0.8 μm and 1.3 μm.

Vias **56** are then formed in the third ILD **54** to expose only the sacrificial capacitor plugs **49**, while a shield portion **58** of the third ELD **54** remains over the second bit line plug **51**. Desirably, the vias **56** are aligned and of mating cross-sectional configuration with the underlying sacrificial capacitor plugs **49**, which are elliptical in the illustrated embodiment.

Referring to FIG. **4**, the sacrificial capacitor plugs **49** are then selectively etched, relative to the surrounding insulators **54**, **44**, with the etch preferably stopping on the underlying capacitor contact plugs **39**. In the illustrated embodiment, where the sacrificial plugs **49** comprise metal, a selective metal etch such as HCl can be employed to remove the plugs **49**, as well as any metallic lining layers. As shown, the second bit line contact plug **51** remains protected from this etch by the mask (not shown) and shield portion **58** while the vias **56** are extended down to the capacitor contact plugs **39** by the removal of the sacrificial plugs.

In an alternative arrangement, one or two of the lining layers within the sacrificial plugs may be left by the selective etch and can serve as the bottom electrodes of the capacitors to be formed. As will be understood by the skilled artisan, such an arrangement would save electrode formation steps, as well as isolation steps.

In accordance with the illustrated embodiment, however, FIG. **4** shows the sacrificial plugs to have been completely removed and a conformal conductive layer **60** deposited into the extended vias **56** and over the remaining portions of the third ILD **54**. Desirably, this conductive layer **60** is thin, and represents the bottom or storage electrode of the cell capacitor. An exemplary conductive layer comprises doped polysilicon, though metal and other conductive materials are suitable. As is known in the art, the conductive layer **60** may also include micro-texturing (e.g., hemispherical grained or HSG polysilicon) to further increase the plate surface area and thus increase cell capacitance. The conductive layer **60** has a thickness sufficient to provide conductivity, but thin enough to avoid crowding the interior of the container.

With reference to FIG. **5**, cell capacitors **61** are completed by patterning the conductive layer **60**, such as by planarization, leaving container-shaped bottom electrodes. In some arrangements, portions of the third ILD can be removed at this stage to expose outer surfaces of the container, further increasing surface area. Bottom electrode isolation is followed by formation of the capacitor dielectric **62** and top or reference electrode **63**. The capacitor dielectric **62** can comprise conventional materials, such silicon oxide, silicon nitride, oxynitride, and oxide-nitride-oxide (ONO), or it can comprise high permittivity materials such as barium strontium tantalate (BST), strontium bismuth tantalate (SBT), tantalum oxide, etc.

In the illustrated embodiment, both the capacitor dielectric **62** and the top electrode **63** are commonly formed across all cells in an array. In other arrangements, it will be understood that either or both layers **62**, **63** can be isolated for each cell.

With reference now to FIGS. **6** and **7**, a window **66** is formed through the common reference electrode **63** to permit formation of the bit line contact therethrough without shorting to electrode **63**. Accordingly, the window **66** is formed wider than the desired bit line contact, such that the bit line contact can be isolated from the capacitors **61** by deposition of a fourth ILD layer **64** into the window **66**, as shown in FIG. **7**. The fourth ILD **64** is deposited to a thickness sufficient to isolate the capacitors **61** from the overlying bit line to be formed, and is preferably between about 0.2 μm and 0.6 μm, then planarized above the capacitors **61**.

In the illustrated embodiment, the window **66** also extends through the capacitor dielectric **62** and the underlying shield portion **58** (see FIG. **5**) of the third ILD layer **54**, to expose the underlying second bit line contact plug **51**. It will be understood, however, that the window could stop on either the capacitor dielectric or the third ELD layer, if desired, without requiring additional mask or etch steps. In any case, filling the window with the fourth ILD or forming insulative spacers over the exposed sidewalls of the capacitor electrode will serve to isolate the electrode from the bit line contact to be completed.

With reference to FIG. **8**, a third bit line contact via **68** is then etched through the fourth ILD **64**, and a third bit line contact plug **71** formed therein. The third bit line via **68** is more narrow than the window **66** in the reference electrode **63**. Accordingly, a portion of the fourth ELD **64** remains to serve as a spacer **72** surrounding the plug **71** and preventing the third bit line contact plug **71** from shorting to the electrode **63**.

In the illustrated embodiment, the third bit line "plug" **71** is not truly a plug, as that term is conventionally used in the art to refer to a contact isolated a via only. Rather, the "plug" **71** is formed simultaneously with a bit line **73** above the fourth ILD **64**, in accordance with known damascene or dual damascene process flows. While CVD processes can be used to facilitate good step coverage, the conductive material forming the bit line **73** and the third bit line contact plug **71** is preferably highly conductive compared to tungsten. Highly conductive metals are typically deposited by physical vapor deposition (e.g., sputtered aluminum alloy with 0.5% copper). Because the illustrated bit line contact plug **71** has a reduced height, compared to conventional processes, the designer has more flexibility in choosing such PVD metals for the plug **71**, despite highly dense device packing.

Nevertheless, the illustrated embodiment also takes advantage of more recently developed metal fill processes, such as hot metal processes, involving high temperature deposition or reflow, or force-fill processes, involving extremely high pressure conditions. In accordance with such aggressive fill techniques, it is desirable to first line the via **68** prior to deposition of the metal, for better contact resistivity, adhesion and barrier protection. For example, the via **68** may be lined with a metal nitride, such as TiN, TaN, WN prior to forming the plug **71** and bit line **73**. Preferably, Ti/TiN/ W layers are deposited sequentially by CVD techniques.

While the overall height of the bit line contact **91** is preferably between about 2.5 μm and 5.0 μm (e.g., about 3.0 μm), the final deposition to form the third contact plug **71** is essentially defined by the thickness of the third and fourth ILDs **54**, **64**. Preferably, the third plug has a height between about 0.8 μm and 2.5 μm, and preferably between about 1.0 μm and 2.0 μm.

With reference to FIGS. **9–14**, an elevated bit line plug is illustrated in accordance with another embodiment of the present invention. In the illustrated embodiment, the second bit line plug is constructed as high as the adjacent capacitors, and a separate shield formed to protect the plug during formation of the capacitors. In the drawings, elements which are similar to elements of FIGS. **1–8** shall be referred to by like reference numerals. Corresponding similar parts, which are different in significant ways, are referred to by like reference numerals with the addition of a prime (') symbol thereafter.

Referring initially to FIG. **9**, capacitor contact plugs **39** and first bit line plugs **41** have been formed between transistor gate electrodes **22** in a semiconductor substrate **12**. Additionally, capacitor plugs **49'** and second bit line plugs **51'** have been formed within a second ILD **44'**. Unlike the first embodiment, however, the transistors are isolated from one another by shallow trench isolation **16'**, rather than by local oxidation. Moreover, the each of the plugs **49'**, **51'** are constructed to the full intended height of the capacitors to be formed. As also shown in FIG. **9**, a photoresist shield **58'** covers the second bit line plug **51'**, and extends laterally beyond the edges thereof.

As shown in FIG. **10**, the shield **58'** serves to protect a portion of the second ILD **44'** as the remainder of the second ILD **44'** is removed. A sidewall spacer of the ILD **44'** material is thus left surrounding the second bit line plug **51'**, while the capacitor plugs **49'** are exposed.

In contrast to the previous embodiment, the capacitor plugs **49'** are not sacrificial, but rather will serve as the bottom electrode of the capacitors to be formed. Advantageously, the electrodes for such "stud capacitors" are non-oxidizing conductors, facilitating use of high dielectric materials for the cell dielectric. For example, the capacitor plugs can comprise Ru, RuO_x, Pt, Ir, IrO_x, etc.

With reference to FIG. **11**, after the shield has been removed, the capacitor dielectric **62'** and the top electrode **63'** are deposited. Desirably, the capacitor dielectric **62'** is characterized by a high effective dielectric constant, such as Ta_2O_5, BST, SBT, ST, BT, PZT, and other ceramics, complex oxides, ferroelectric materials and the like. Capacitors **61'** are thereby completed.

With reference to FIG. **12**, a window **66'** is then opened through the electrode layer **63'** and dielectric layer **62'**, exposing the second bit line plug **51'**. Desirably, the window **66'** is wider than the second bit line plug **51'**, as shown. FIG. **13** shows the structure of FIG. **12** after deposition of a third ILD **64'** over the capacitors **61'** and the second bit line contact.

FIG. **14** then shows the structure after a contact via **68'** is etched through the third ILD **64'**, and filled to form a third bit line plug **71'**, thereby completing the bit line contact **91'**. Note that, in comparison to the previous process, the depth of the third bit line plug **71'** is further reduced, and need only extend down to approximately the level of the capacitors **61'**.

Advantageously, the disclosed processes reduce the aspect ratio of the bit line contact via **68** or **68'** to be filled at the end of the process. A bit line contact **91**, **91'**, from the bit line **73**, **73'** to the substrate **12**, is thus made in three stages: the first bit line contact plug **41**, **41'**, the second bit line contact plug **51**, **51'**, and the third bit line contact plug **71**, **71'**. In other arrangements, the lower plugs **39**, **41** or **39'**, **41'** can be omitted, and the capacitors **61**, **61'** and bit line plugs **51**, **51'** can be formed in direct contact with the substrate **12**.

Each of these contact plugs **41**, **51**, **71** or **41'**, **51'**, **71'** are aligned with one another. It will be understood that "aligned," as used herein, does not imply complete overlap nor identical widths of the plugs. Rather, alignment refers to the arrangement such that the plugs define a single electrical path from the substrate **12** to the bit line **73**, **73'**. Thus, in application, the multiple levels of the bit line contact **91**, **91'** can exhibit slight misalignment and variation in widths. The skilled artisan will understand that the use of etch stop layers between ILDs can reduce the risk of shorting due to slight mask misalignment.

From another viewpoint, the bit line contact plug **71**, **71'** is raised, relative to conventional processes, to a level above the bottom of adjacent cell capacitors. Thus, where conven-

tional bit line contacts must extend the full height of the stacked capacitors in addition to the height of the ILD separating the capacitors from the bit line, the final stage **71** of the bit line contact **91** of FIG. **8** extends only partway down the height of the capacitors. The final stage **71'** of the bit line contact **91'** of FIG. **14** extends upwardly from approximately the top of the capacitors **61'**. As will be recognized by the skilled artisan, the reduced aspect ratio via is thus more readily filled with fewer voids and consequently better yield. Moreover, the process enables further scaling and may be extended to include multiple stages between the lower plug **41**, **41'** and the upper plug **71**, **71'**.

As will be understood by the skilled artisan, the processes and structures disclosed herein are applicable to forming interlevel contact through vias of high-aspect ratio, in general. The process has particular utility in the context of contacts through intermediate levels of device fabrication, such as the illustrated DRAM circuits with the bit line formed over stacked cell capacitors.

Thus, although, the invention has been described in terms of certain preferred embodiments and suggested possible modifications thereto, other embodiments and modifications will suggest themselves and be apparent to those of ordinary skill in the art. Such modifications are intended to also fall within the spirit and scope of the present invention, which should accordingly be defined by reference to the appended claims.

We claim:

1. An integrated circuit contact extending from a lower level to an upper level, the contact comprising:

a first plug in direct contact with the lower level;

a second conductive plug in direct contact with the first plug; and

a third conductive plug in direct contact with the second conductive plug and the upper level.

2. The integrated circuit contact of claim **1**, wherein the upper level comprises a metal wiring layer and the lower level comprises a semiconductor substrate.

3. The integrated circuit contact of claim **2**, wherein the metal wiring layer comprises a bit line in a memory array.

4. The integrated circuit contact of claim **3**, wherein the bit line extends over a plurality of cell capacitors in the memory array.

5. The integrated circuit contact of claim **4**, wherein the first plug extends from the substrate to a bottom level of the cell capacitors.

6. The integrated circuit contact of claim **5**, wherein the second plug extends from the first plug to a level below a top level of the cell capacitors.

7. The integrated circuit contact of claim **5**, wherein the second plug extends from the first plug to approximately a top level of the cell capacitors.

8. The integrated circuit contact of claim **1**, wherein the first plug comprises polysilicon, the second plug comprises metal, and the third plug comprises metal.

9. The integrated circuit contact of claim **8**, wherein the second plug comprises elemental tungsten.

10. The integrated circuit contact of claim **8**, wherein the second plug further comprises a conformal via liner.

11. The integrated circuit contact of claim **8**, wherein the third plug comprises aluminium.

12. An integrated circuit contact extending from a lower level to an upper level, the contact comprising:

a first plug in direct contact with the lower level;

a second plug in direct contact with the first plug, wherein the first and second plugs have a combined height of between about 1.0 μm and 2.3 μm; and

a third plug in direct contact with the second plug and the upper level, wherein the overall height of the contact is between about 2.0 μm and 5.5 μm.

* * * * *

EXHIBIT F

US006828683B2

(12) **United States Patent**
Li et al.

(10) **Patent No.: US 6,828,683 B2**
(45) **Date of Patent: *Dec. 7, 2004**

(54) **SEMICONDUCTOR DEVICES, AND SEMICONDUCTOR PROCESSING METHODS**

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(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/219,041**

(22) Filed: **Dec. 23, 1998**

(65) **Prior Publication Data**

US 2002/0020919 A1 Feb. 21, 2002

(51) **Int. Cl.**[7] **H01L 23/48**

(52) **U.S. Cl.** **257/759**; 257/751; 257/762; 257/642; 438/687; 438/623; 438/794; 438/627

(58) **Field of Search** 257/759, 751, 257/762, 642, 386; 438/687, 623, 793, 794, 624, 627

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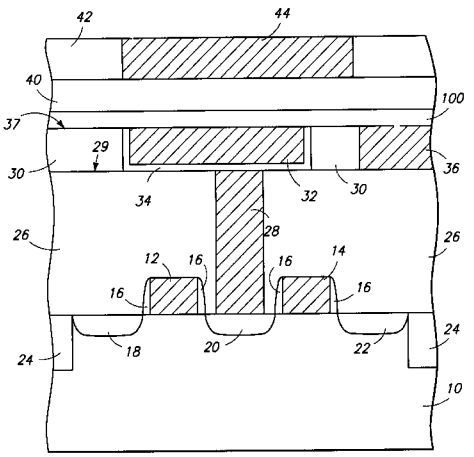
(57) **ABSTRACT**

In one aspect, the invention encompasses a semiconductor processing method wherein a conductive copper-containing material is formed over a semiconductive substrate and a second material is formed proximate the conductive material. A barrier layer is formed between the conductive material and the second material. The barrier layer comprises a compound having silicon chemically bonded to both nitrogen and an organic material. In another aspect, the invention encompasses a composition of matter comprising silicon chemically bonded to both nitrogen and an organic material. The nitrogen is not bonded to carbon. In yet another aspect, the invention encompasses a semiconductor processing method. A semiconductive substrate is provided and a layer is formed over the semiconductive substrate. The layer comprises a compound having silicon chemically bonded to both nitrogen and an organic material.

38 Claims, 3 Drawing Sheets



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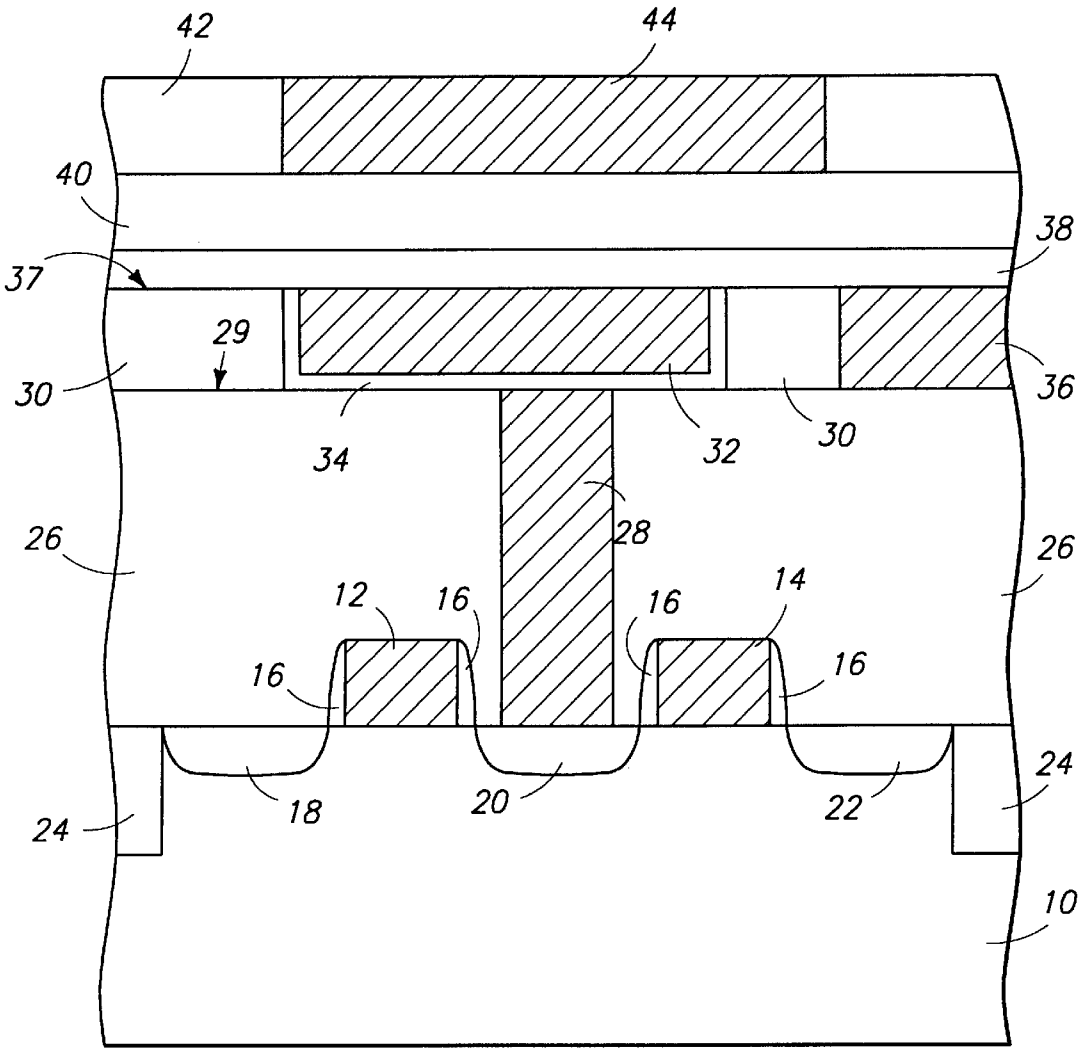

Fig 1
PRIOR ART

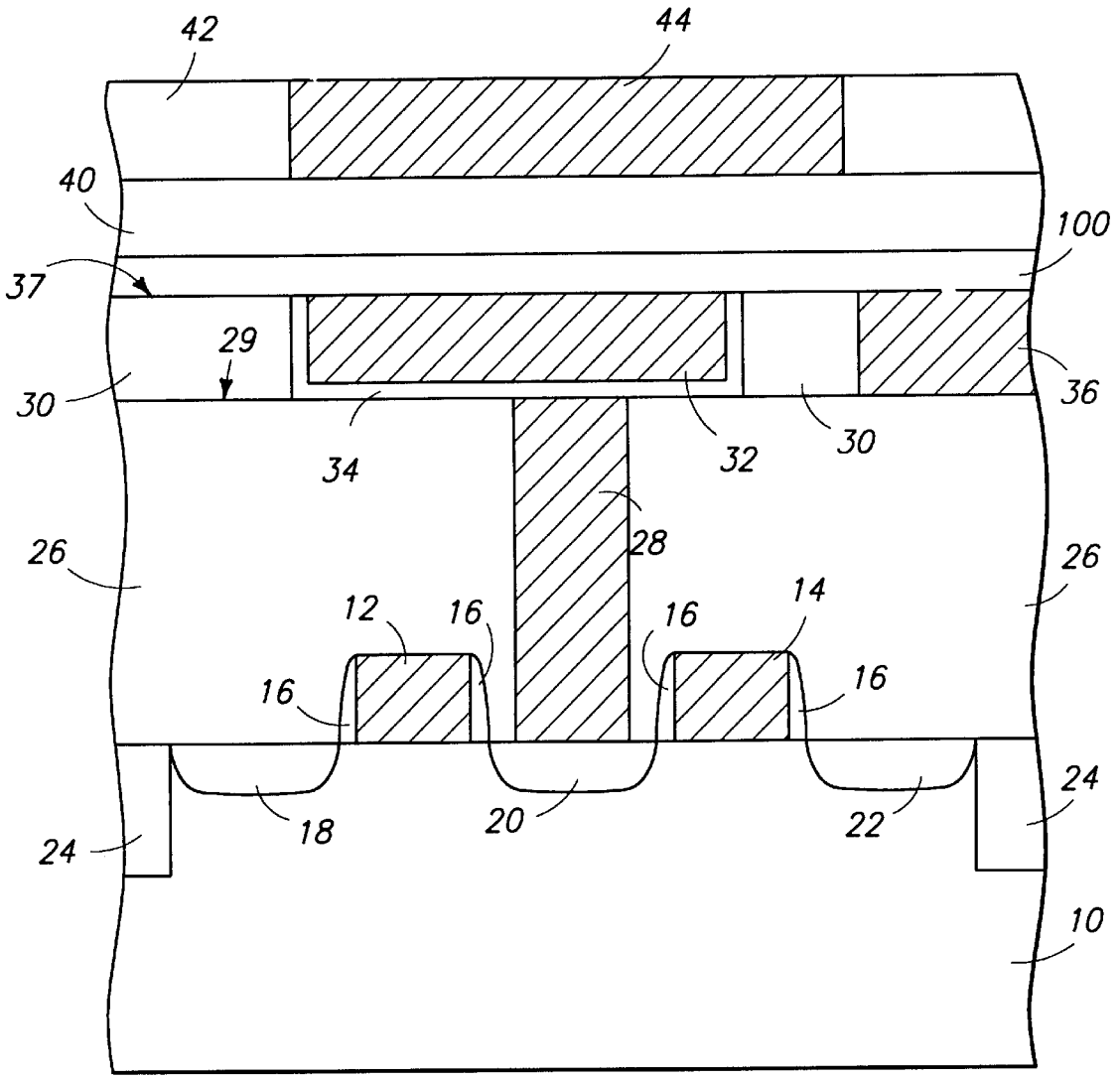
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Fig 2

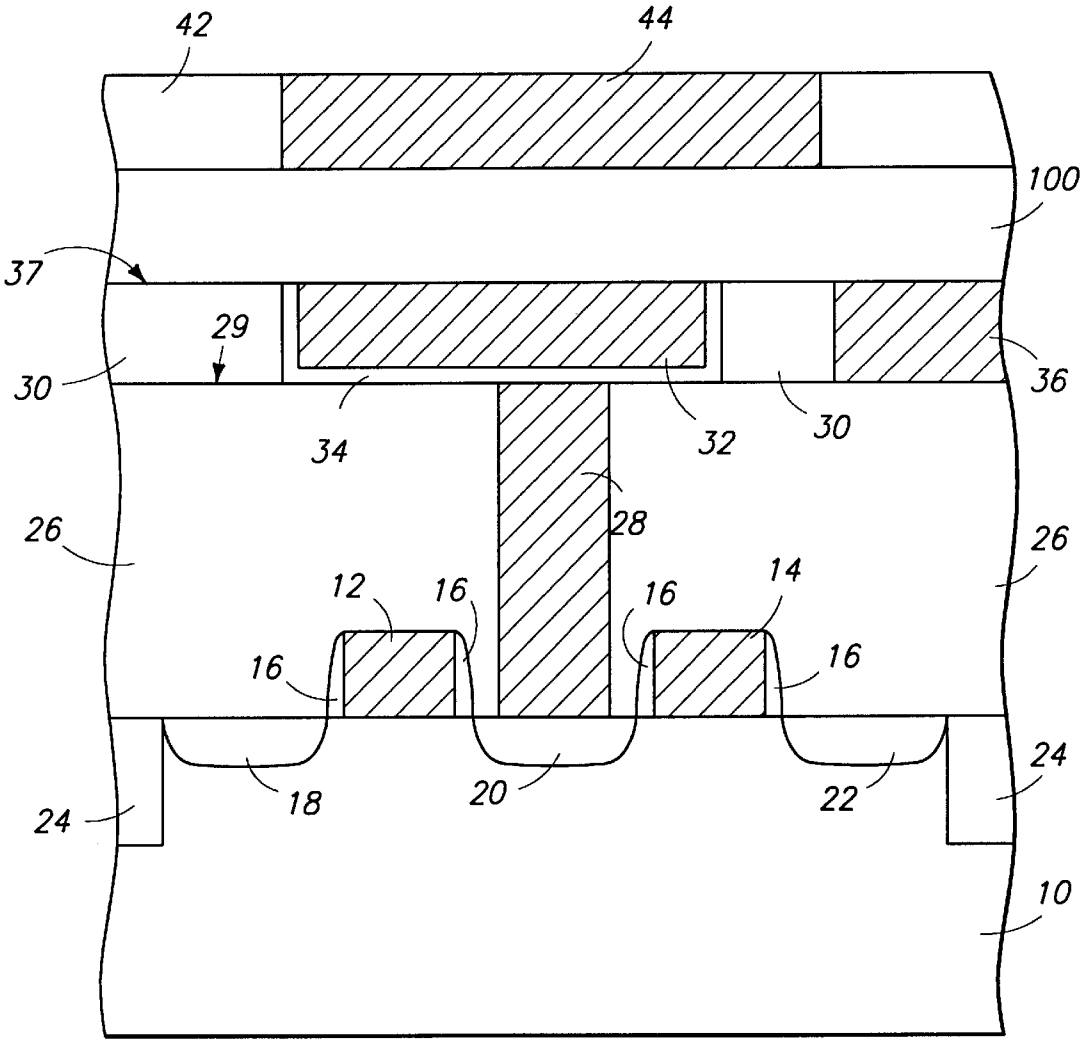
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Fig 3

SEMICONDUCTOR DEVICES, AND SEMICONDUCTOR PROCESSING METHODS

TECHNICAL FIELD

The invention pertains to compositions of matter comprising silicon bonded to both nitrogen and an organic material. The invention further pertains to semiconductor devices incorporating the above-described compositions of matter, and to methods of forming semiconductor devices. In particular aspects, the invention pertains to semiconductor devices incorporating copper-containing materials, and to methods of forming such devices.

BACKGROUND OF THE INVENTION

It would be desirable to employ copper-containing materials in semiconductor devices. Copper has conductive properties that are superior to those of many of the conductive materials presently utilized in semiconductor devices. Unfortunately, copper has a drawback associated with it that it cannot generally be placed against oxide-comprising insulative materials (such as, for example, silicon dioxide). If copper-containing materials are placed adjacent oxide-comprising insulative materials, oxygen can diffuse into the copper-containing material and react to reduce conductivity of the material. Also, copper can diffuse into the oxide-containing material to reduce the insulative properties of the oxide-containing material. Additionally, copper can diffuse through oxide insulative material to device regions and cause degradation of device (e.g., transistor) performance. The problems associated with copper are occasionally addressed by providing nitride containing barrier layers adjacent the copper-containing materials, but such can result in problems associated with parasitic capacitance, as illustrated in FIG. **1**. Specifically, FIG. **1** illustrates a fragment of a prior art integrated circuit, and illustrates regions where parasitic capacitance can occur.

The structure of FIG. **1** comprises a substrate **10**, and transistor gates **12** and **14** overlying substrate **10**. Substrate **10** can comprise, for example, monocrystalline silicon lightly doped with a p-type background conductivity-enhancing dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Transistor gates **12** and **14** can comprise conventional constructions such as overlying layers of gate oxide, polysilicon and silicide. Insulative spacers **16** are formed adjacent transistor gates **12** and **14**, and conductively doped diffusion regions **18**, **20** and **22** are formed within substrate **10** and proximate gates **12** and **14**. Also, isolation regions **24** (shown as shallow trench isolation regions) are formed within substrate **10** and electrically isolate diffusion regions **18** and **22** from other circuitry (not shown) provided within and over substrate **10**.

An insulative material **26** extends over substrate **10**, and over transistor gates **12** and **14**. A conductive plug **28** extends through insulative material **26** to contact conductive diffusion region **20**. Conductive plug **28** can comprise, for example, conductively doped polysilicon. Insulative material **26** can comprise, for example, silicon dioxide or borophosphosilicate glass (BPSG). Insulative material **26** and plug **28** together comprise a planarized upper surface **29**. Planarized surface **29** can be formed by, for example, chemical-mechanical polishing.

A second insulative material **30** is formed over insulative material **26** and on planarized upper surface **29**. Second insulative material **30** can comprise, for example, borophosphosilicate glass or silicon dioxide. A conductive material **32** is formed within an opening in insulative material **30** and over conductive plug **28**. Conductive material **32** comprises copper. The copper can be, for example, in the form of elemental copper, or in the form of an alloy. Conductive material **32** is separated from conductive plug **28** by an intervening barrier layer **34**. Barrier layer **34** typically comprises a conductive material, such as titanium nitride (TiN) or tantalum nitride (TaN), and is provided to prevent out-diffusion of copper from conductive material **32** into either insulative material **26** or the polysilicon of conductive plug **28**. Barrier layer **34** can also prevent diffusion of silicon or oxygen from layers **26**, **28** and **30** into the copper of conductive material **32**. It is desired to prevent diffusion of oxygen to the copper of material **32**, as such oxygen could otherwise reduce conductance of material **32**. Also, it is desired to prevent copper diffusion from material **32** into insulative layer **26**, as such copper could reduce the insulative properties of the material of layer **26**. Additionally, diffusion through layer **26** and into one or more of regions **18**, **20** and **22** can reduce the performance of transistor devices.

A second conductive material **36** is provided over insulative material **26** and spaced from first conductive material **32**. Second conductive material **36** can comprise, for example, conductively doped polysilicon or a conductive metal, or a combination of two or more conductive materials (such as copper and TiN). Second conductive material **36** is spaced from first conductive material **32** by an intervening region of insulative material **30** and barrier layer **34**.

Insulative material **30**, barrier layer **34**, first conductive material **32** and second conductive material **36** share a common planarized upper surface **37**. Planarized upper surface **37** can be formed by, for example, chemical-mechanical polishing.

An insulative barrier layer **38** is provided over planarized upper surface **37**. Insulative barrier layer **38** can comprise, for example, silicon nitride.

An insulative layer **40** is provided over insulative barrier layer **38**. Insulative layer **40** can comprise, for example, silicon dioxide or BPSG. Insulative barrier layer **38** inhibits diffusion of copper from first conductive material **32** into insulative layer **40**, and inhibits diffusion of oxygen from insulative layer **40** into first conductive material **32**.

Another insulative layer **42** is provided over insulative layer **40**, and a third conductive material **44** is provided within insulative material **42** and over first conductive material **32**. Insulative material **42** can comprise, for example, BPSG or silicon dioxide, and third conductive material **44** can comprise, for example, conductively doped polysilicon or a metal, or a combination of two or more conductive materials (such as copper and TiN).

Conductive materials **32**, **36** and **44** can be conductive interconnects between electrical devices, or portions of electrical devices. The function of materials **32**, **36** and **44** within a semiconductor circuit is not germane to this discussion. Instead, it is the orientation of conductive materials

32, **36** and **44** relative to one another that is of interest to the present discussion. Specifically, each of materials **32**, **36** and **44** is separated from the other materials by intervening insulative (or dielectric) materials. Accordingly, parasitic capacitance can occur between the conductive materials **32**, **36** and **44**. A method of reducing the parasitic capacitance is to utilize insulative materials that have relatively low dielectric constants ("k"). For instance, as silicon dioxide has a lower dielectric constant that silicon nitride, it is generally preferable to utilize silicon dioxide between adjacent conductive components, rather than silicon nitride. However, as discussed previously, copper-containing materials are preferably not provided against silicon dioxide due to diffusion problems that can occur. Accordingly, when copper is utilized as a conductive material in a structure, it must generally be spaced from silicon dioxide-comprising insulative materials to prevent diffusion of oxygen into the copper structure, as well as to prevent diffusion of copper into the oxygen-comprising insulative material. Accordingly, the copper materials are generally surrounded by nitride-comprising materials (such as the shown is barrier layers **34** and **38**) to prevent diffusion from the copper materials, or into the copper materials. Unfortunately, this creates the disadvantage of having relatively high dielectric constant nitride materials (for example, the material of layer **38**) separating conductive materials. Accordingly, the requirement of nitride-comprising barrier layers can take away some of the fundamental advantage of utilizing copper-comprising materials in integrated circuit constructions.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a semiconductor processing method wherein a conductive copper-containing material is formed over a semiconductive substrate and a second material is formed proximate the conductive material. A barrier layer is formed between the conductive material and the second material. The barrier layer comprises a compound having silicon chemically bonded to both nitrogen and an organic material.

In another aspect, the invention encompasses a composition of matter comprising silicon chemically bonded to both nitrogen and an organic material.

In yet another aspect, the invention encompasses a semiconductor processing method. A semiconductive substrate is provided and a layer is formed over the semiconductive substrate. The layer comprises a compound having silicon chemically bonded to both nitrogen and an organic material.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

FIG. **1** is a diagrammatic, cross-sectional, fragmentary view of a prior art integrated circuit construction.

FIG. **2** is a diagrammatic, cross-sectional, fragmentary view of an integrated circuit construction encompassed by the present invention.

FIG. **3** is a diagrammatic, cross-sectional, fragmentary view of another embodiment integrated circuit construction encompassed by the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the present invention, a novel composition of matter has been developed which comprises silicon chemically bonded to both nitrogen and an organic material, and wherein the nitrogen is not bonded to carbon. More specifically, the silicon is chemically bonded to both nitrogen and carbon. The carbon can be, for example, in the form of a hydrocarbon. In a preferred aspect, the carbon is comprised by a methyl group and the composition of matter consists essentially of $(CH_3)_xSi_3N_{(4-x)}$, wherein x is greater than 0 and no greater than about 4.

A composition of the present invention can be formed by, for example, reacting inorganic silane with one or more of ammonia (NH_3), hydrazine (N_2H_4), or a combination of nitrogen (N_2) and hydrogen (H_2). The reaction can occur with or without a plasma. However, if the reaction comprises an organic silane in combination with dinitrogen and dihydrogen, the reaction preferably occurs in the presence of plasma.

An exemplary reaction is to combine methylsilane (CH_3SiH_3) with ammonia (NH_3) in the presence of a plasma to form $(CH_3)_xSi_3N_{4-x}$. The exemplary reaction can occur, for example, under the following conditions. A substrate is placed within a reaction chamber of a reactor, and a surface of the substrate is maintained at a temperature of from about 0° C. to about 600° C. Ammonia and methylsilane are flowed into the reaction chamber, and a pressure within the chamber is maintained at from about 300 m Torr to about 30 Torr, with a plasma at radio frequency (RF) power of from about 50 watts to about 500 watts. A product comprising $(CH_3)_xSi_3N_{(4-x)}$ is then formed and deposited on the substrate. The reactor can comprise, for example, a cold wall plasma reactor.

It is found that the product deposited from the described reaction consists essentially of Si_3N_y and $(CH_3)_xSi_3N_{(4-x)}$, (wherein y is generally about 4/3, and x is also generally about 4/3). The $(CH_3)_xSi_3N_{(4-x)}$ is present in the product to a concentration of from greater than 0% to about 50% (mole percent), and is preferably from about 10% to about 20%. The amount of $(CH_3)_xSi_3N_{(4-x)}$ present in the product can be adjusted by providing a feed gas of SiH_4 in the reactor in addition to the CH_3SiH_3, and by varying a ratio of the SiH_4 to the CH_3SiH_3, and/or by adjusting RF power.

The compositions of matter encompassed by the present invention are found to be insulative, and to have lower dielectric constants than silicon nitride. Accordingly, compositions of the present invention can be substituted for silicon nitride in barrier layers to reduce parasitic capacitance between adjacent conductive components. FIG. **2** illustrates a fragment of an integrated circuit incorporating a composition of the present invention. In referring to FIG. **2**, similar numbering to that utilized above in describing the prior art structure of FIG. **1** will be used, with differences indicated by different numerals.

The structure of FIG. **2** differs from the prior art structure of FIG. **1** in that FIG. **2** illustrates a barrier layer **100** in place of the silicon nitride barrier layer **38** of FIG. **1**. Layer **100** can comprise, for example, an above-described novel composition of the present invention, such as, for example, $(CH_3)_xSi_3N_{(4-x)}$. Alternatively, layer **100** can comprise a composition which includes carbon, silicon and nitrogen, and wherein the nitrogen is bonded to carbon. Layer **100** is proximate conductive material **32** (actually against conductive material **32**) and separates second conductive material **44** from first conductive material **32**. In the construction shown in FIG. **2**, barrier layer **100** separates conductive material **32** from an insulative material **40** to impede migra-

tion of oxide from insulative material **40** into copper of a preferred conductive material **32**, as well as to impede migration of copper from preferred material **32** into insulative material **40**.

FIG. **3** illustrates an alternate embodiment semiconductor construction of the present invention (with numbering identical to that utilized in FIG. **2**), wherein insulative material **40** (FIG. **2**) is eliminated. Barrier layer **100** is thus the only material between first conductive material **32** and second conductive material **44**, and is against both conductive material **32** and conductive material **44**.

In exemplary embodiments of the present invention, barrier layer **100** comprises $(CH_3)_xSi_3N_{(4-x)}$ (wherein "X" is from about 1 to about 4, and preferably wherein "X" is about 0.7). Such barrier layer **100** can be formed by the methods discussed above, and can, for example, consist essentially of Si_3N_y and $(CH_3)_xSi_3N_{(4-x)}$. Also, an amount of $(CH_3)_xSi_3N_{(4-x)}$ within barrier layer **100** can be adjusted by the above-discussed methods of adjusting a ratio of SiH_4 and CH_3SiH_3 during formation of the layer. An exemplary concentration of $(CH_3)_xSi_3N_{(4-x)}$ within barrier layer **100** is from greater than 0% to about 20% (mole percent).

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

What is claimed is:

1. A semiconductor processing method, comprising:

forming a conductive copper-containing material over a semiconductive substrate;

forming a second material proximate the conductive material; and

forming a barrier layer between the conductive material and the second material, the barrier layer comprising $(CH_3)_xSi_3N_{(4-x)}$, with x being greater than 0 and no greater than 4.

2. The method of claim **1** wherein conductive material consist essentially of copper.

3. The method of claim **1** wherein the barrier layer is against the conductive material.

4. The method of claim **1** wherein the barrier layer is against both the conductive material and the second material.

5. The method of claim **1** wherein the second material is an insulative material.

6. A semiconductor processing method, comprising:

forming a conductive copper-containing material over a semiconductive substrate;

forming a second material proximate the conductive material;

forming a barrier layer between the conductive material and the second material, the barrier layer comprising a compound having silicon chemically bonded to both nitrogen and an organic material, the barrier layer being in physically contact with the second material; and

wherein the second material comprises silicon dioxide.

7. The method of claim **1** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein y is greater than 0 and no greater than about 4.

8. The method of claim **1** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, wherein y is greater than 0 and no greater than about 4, and wherein the $(CH_3)_xSi_3N_{(4-x)}$ is present in the barrier layer to a concentration of from greater than 0% to about 20% (mole percent).

9. The method of claim **1** wherein the forming the barrier layer occurs in a reaction chamber and comprises combining CH_3SiH_3 and NH_3 in the chamber to deposit the $(CH_3)_xSi_3N_{(4-x)}$ over the substrate.

10. The method of claim **1** wherein the forming the barrier layer occurs in a reaction chamber and comprises combining CH_3SiH_3 and NH_3 in the chamber with a plasma to deposit the $(CH_3)_xSi_3N_{(4-x)}$ over the substrate.

11. The method of claim **1** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein the forming the barrier layer occurs in a reaction chamber and comprises combining CH_3SiH_3, SiH_4 and NH_3 in the chamber with a plasma to deposit the $(CH_3)_xSi_3N_{(4-x)}$ over the substrate, and wherein y is greater than 0 and no greater than about 4.

12. A semiconductor processing method, comprising:

providing a semiconductive substrate;

forming a first material over the semiconductive substrate;

forming a barrier layer proximate the first material, the barrier layer comprising $(CH_3)_xSi_3N_{(4-x)}$, with x being greater than 0 and no greater than 4; and

forming a second material separated from the first material by the barrier layer.

13. The method of claim **12** wherein the barrier layer is formed against the first material.

14. The method of claim **12** wherein the barrier layer is formed against the first material, and wherein the second material is formed against the barrier layer.

15. The method of claim **12** wherein at least one of the first and second materials is conductive.

16. The method of claim **12** wherein at least one of the first and second materials is insulative.

17. The method of claim **12** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein y is greater than 0 and no greater than about 4.

18. A semiconductor processing method, comprising:

providing a semiconductive substrate; and

forming a layer over the semiconductive substrate, the layer comprising $(CH_3)_xSi_3N_{(4-x)}$, with x being greater than 0 and no greater than 4.

19. The method of claim **18** wherein the layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein y is greater than 0 and no greater than about 4.

20. The method of claim **18** wherein the layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, wherein the $(CH_3)_xSi_3N_{(4-x)}$ is present in the layer to a concentration of from greater than 0% to about 20% (mole percent), and wherein y is greater than 0 and no greater than about 4.

21. The method of claim **18** wherein the forming occurs in a reaction chamber and comprises combining CH_3SiH_3 and NH_3 in the chamber to deposit the $(CH_3)_xSi_3N_{(4-x)}$ over the substrate.

22. The method of claim **18** wherein the forming occurs in a reaction chamber and comprises combining CH_3SiH_3 and NH_3 in the chamber with a plasma to deposit the $(CH_3)_xSi_3N_{(4-x)}$ over the substrate.

23. The method of claim **18** wherein the layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein the forming occurs in a reaction chamber and comprises combining CH_3SiH_3, SiH_4 and NH_3 in the chamber with a plasma to deposit the $(CH_3)_xSi_3N_{(4-x)}$ over the substrate.

24. A semiconductor device, comprising:

a semiconductive substrate; and

a layer over the semiconductive substrate, the layer comprising $(CH_3)_xSi_3N_{(4-x)}$, with x being greater than 0 and no greater than 4.

25. The device of claim **24** wherein the layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein y is greater than 0 and no greater than about 4.

26. The device of claim **24** wherein the layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, wherein the $(CH_3)_xSi_3N_{(4-x)}$ is present in the layer to a concentration of from greater than 0% to about 50% (mole percent), and wherein y is no greater than about 4.

27. A semiconductor device, comprising:

a semiconductive substrate;

a first material over the semiconductive substrate;

a second material proximate the first material; and

a barrier layer separating the second material from the first material, the barrier layer comprising $(CH_3)_xSi_3N_{(4-x)}$, with x being greater than 0 and no greater than 4.

28. The device of claim **27** wherein at least one of the first and second materials is conductive.

29. The device of claim **27** wherein the nitrogen is not bonded to carbon.

30. The device of claim **27** wherein at least one of the first and second materials is insulative.

31. The device of claim **27** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein y is no greater than about 4.

32. A semiconductor device, comprising:

a semiconductive substrate;

a conductive copper-containing material over the semiconductive substrate;

a second material proximate the conductive material; and

a barrier layer between the conductive material and the second material, the barrier layer comprising $(CH_3)_xSi_3N_{(4-x)}$, with x being greater than 0 and no greater than 4.

33. The device of claim **32** wherein the barrier layer is against the conductive material.

34. The device of claim **32** wherein the barrier layer is against both the conductive material and the second material.

35. The device of claim **32** wherein the second material is an insulative material.

36. A semiconductor device, comprising:

a semiconductive substrate;

a conductive copper-containing material over the semiconductive substrate;

a second material proximate the conductive material;

a barrier layer between the conductive material and the second material, the barrier layer comprising a compound having silicon chemically bonded to both nitrogen and an organic material, the barrier layer being in physical contact with the second material; and

wherein the second material comprises silicon dioxide.

37. The device of claim **32** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, and wherein y is no greater than about 4.

38. The device of claim **32** wherein the barrier layer consists essentially of Si_3N_y and the $(CH_3)_xSi_3N_{(4-x)}$, wherein the $(CH_3)_xSi_3N_{(4-x)}$, is present in the layer to a concentration of from greater than 0% to about 50% (mole percent), and wherein y is no greater than about 4.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,828,683 B2
APPLICATION NO. : 09/219041
DATED : December 7, 2004
INVENTOR(S) : Li et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item (56) Refereces Cited, Page 3, Other Publications – Replace "Weidman T. et al., "-Nc~" with --Weidman T. et al., "New--.

Item (56) References Cited, Page 3, Other Publications – Replace "TEXT: Jenkins, F. et al., Fundaments" with --TEXT: Jenkins, F. et al., Fundamentals--.

Item (56) References Cited, Page 3, Other Publications – Replace "Laxlhan, R. et al." with --Laxman et al.--.

Item (56) References Cited, Page 3, Other Publications – Replace "Hackn's Chemical Dictionary" with --Hackh's Chemical Dictionary--.

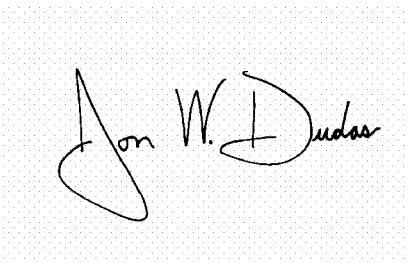
Column 3, Line 21 – Replace "the shown in barrier layers **34**" with --the shown barrier layers **34**--.

Column 4, Line 22 – Replace "$(CH_3)_xSi_3N_{4-x}$" with --$(CH_3)_xSi_3N_{(4-x)}$--.

Column 5, Line 63, Claim 6 – Replace "in physically contact" with --in physical contact--.

Signed and Sealed this

Fourth Day of September, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office