IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

NORTH STAR INNOVATIONS INC., Plaintiff, v. TOSHIBA CORPORATION, TOSHIBA AMERICA, INC. AND TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC. Defendants.	C.A. No. 16-cv-115-LPS-CJB **JURY DEMANDED**

FIRST AMENDED COMPLAINT

Under Fed. R. Civ. P. 15(a)(1), Plaintiff North Star Innovations Inc. ("North Star") files this First Amended Complaint. North Star complains of Defendants Toshiba Corporation, Toshiba America, Inc. and Toshiba America Electronic Components, Inc. (collectively, "Toshiba") as follows:

JURISDICTION AND VENUE

1. Title 28 of the United States Code Section 1338(a) confers subject matter jurisdiction on this Court because Defendants have infringed Plaintiff's patent. The Patent Act of 1952, as amended, 35 U.S.C. § 271, *et seq.*, makes patent infringement actionable through a private cause of action.

2. Defendants have transacted business in the State of Delaware, and in this judicial district by making, using, selling, offering to sell and distributing products in this judicial district that violate North Star's patents. Accordingly, this Court has personal jurisdiction over Defendant.

3. Venue is proper in the District of Delaware under the general federal venue statute, 28 U.S.C. § 1391(d), and under the specific venue provision relating to patent-infringement cases, 28 U.S.C. § 1400(b).

PARTIES

4. North Star is a Delaware corporation with its principal place of business at Plaza Tower, 600 Anton Boulevard, Suite 1350, Costa Mesa, CA 92626. North Star is a subsidiary of Wi-LAN Technologies Inc. North Star is the assignee of and owns all right, title and interest in and has standing to sue for infringement of United States Patent No. 6,909,320 ("the '320 Patent"), attached as Exhibit A, entitled Method and Apparatus for Dual Output Voltage Regulation, United States Patent No. 6,917,555 ("the '555 Patent"), attached as Exhibit B, entitled Integrated Circuit Power Management for Reducing Leakage Current In Circuit Arrays and Method Therefor, United States Patent No. 6,108,263 ("the '263 Patent"), attached as Exhibit C, entitled Memory System, Method For Verifying Data Stored In A Memory System After A Write Cycle And Method For Writing To A Memory System, and United States Patent No. 6,127,875 ("the '875 Patent"), attached as Exhibit D, entitled Complimentary Double Pumping Voltage Boost Converter. The '320 Patent issued June 21, 2005, the '555 Patent issued July 12, 2005, the '263 Patent issued August 22, 2000, and the '875 Patent issued October 3, 2000.

5. Toshiba Corporation is a Japanese multinational company with its principal place of business at 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan. Toshiba Corporation has previously and is presently making, using, selling, offering for sale, and/or importing into the United States memory controller products that infringe one or more claims of the '320 Patent, one or more claims of the '555 Patent, one or more claims of the '263 Patent, and one or more claims of the '875 Patent.

6. Toshiba America, Inc. is a subsidiary of Toshiba Corporation with its principal place of business at 1251 Avenue of the Americas, Suite 4110, New York, NY 10020. Toshiba America, Inc. has previously and is presently making, using, selling, offering for sale, and/or importing into the United States memory controller products that infringe one or more claims of the '320 Patent, one or more claims of the '555 Patent, one or more claims of the '263 Patent, and one or more claims of the '875 Patent.

7. Toshiba America Electronic Components, Inc. is an independent operating company owned by Toshiba America, Inc. with its principal place of business at 9740 Irvine Boulevard, Irvine, CA 92618. Toshiba America Electronic Components, Inc. has previously and is presently making, using, selling, offering for sale, and/or importing into the United States memory controller products that infringe one or more claims of the ’320 Patent, one or more claims of the ’555 Patent, one or more claims of the ’263 Patent, and one or more claims of the ’875 Patent.

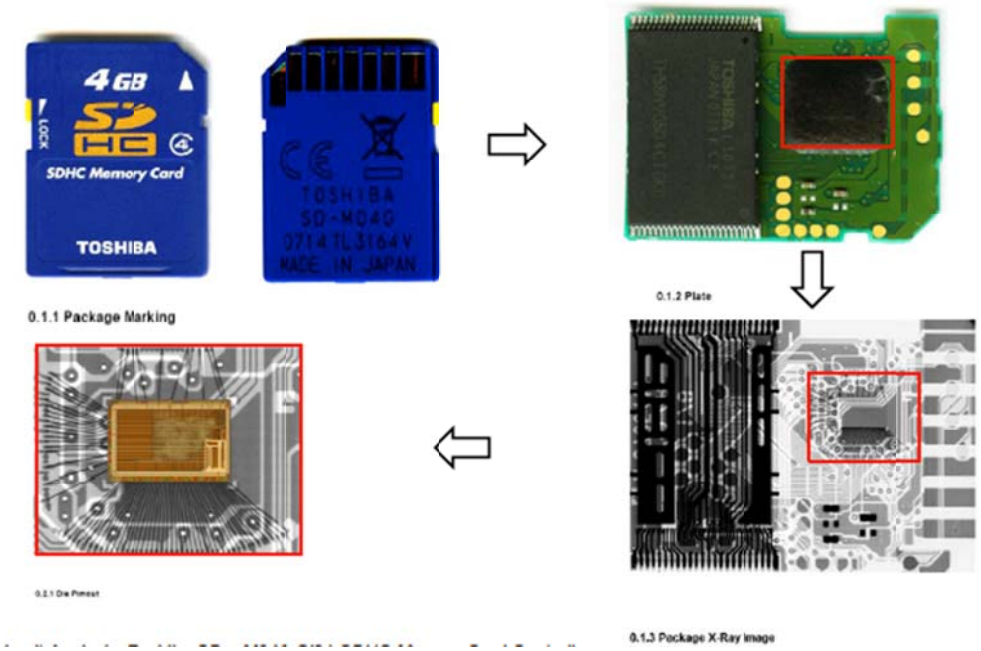
BACKGROUND

8. North Star is the owner of patent rights, which cover commercially significant technologies related to voltage regulation circuits and integrated circuit power management. The ’320 Patent covers a dual output voltage regulator circuit to prevent leakage, the ’555 Patent covers an integrated circuit having power management to eliminate leakage current in circuit arrays, the ’263 Patent covers erasable non-volatile memory systems, and the ‘875 Patent covers a double pumping voltage boosting circuit for providing an output voltage greater than a supplied input voltage and which is suited to be manufactured in integrated circuit form.

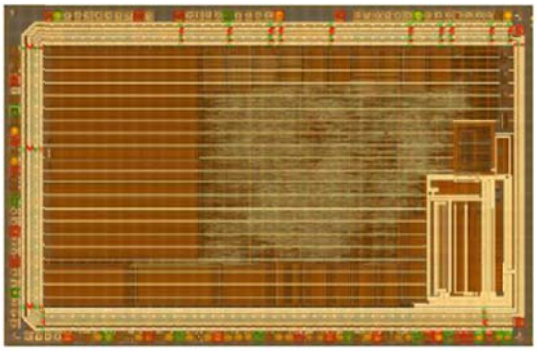
9. Defendants design, manufacture, and sell memory controller products that that infringe the ’320 Patent, the ’555 Patent, the ’263 Patent, and the ’875 Patent.

COUNT I - PATENT INFRINGEMENT OF THE ’320 PATENT

10. Defendants have infringed and continue to infringe at least claims 1-4, and 6 of the ’320 Patent, in violation of 35 U.S.C. § 271 through, among other activities, making, using, offering to sell, and/or selling the Toshiba SDHC Memory Card, and Toshiba SD – M04G GI91 SDHC Memory Card Controller. Photos of the Toshiba SDHC Memory Card are depicted below, including Package Marking (top-left), Plate (top-right), Die Pinout (bottom-left) and Package X-Ray Image (bottom-right) (Source: ISS, Circuit Analysis Toshiba SD – M04G Gl91 SDHC Memory Card Controller):



Photos of the Toshiba SD – M04G GI91 SDHC Memory Card Controller are shown below, including a Die Photograph (left) and Die Marking (right) (Source: ISS, Circuit Analysis Toshiba SD – M04G Gl91 SDHC Memory Card Controller):



0.2.3 Die Photograph

0.2.2 Die Marking

11. Defendants' infringing technology and products include without limitation their memory controller products, including, for example, the Toshiba SDHC Memory Card, Toshiba SD – M04G GI91 SDHC Memory Card Controller and other memory controller products. Defendants' infringement may include additional products and technologies (to be determined in discovery) marketed or used by Defendants.

12. Claim 1 is an exemplary infringed claim. Its preamble states: "A dual output voltage regulator circuit, comprising." Toshiba's products, such as its SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller, have a dual output voltage regulator circuit. The SD – M04G GI91 SDHC Memory Card Controller circuit has two regulators and a voltage divider.

13. After the preamble, the first limitation of claim 1 states: "a first voltage regulator section including a first pass device, and having a first regulated voltage output with a first current capacity." Toshiba's products, such as its SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller contain this first limitation, because they have a first voltage regulator section including a first pass device, and having a first regulated voltage output with a first current capacity. One model of the SD – M04G GI91 SDHC Memory Card Controller has a "Regulator 1" with a first current capacity of 4000, where the first current capacity is given by $W * M / L$, where $W = 10.0$ is the width of the first pass device, $L = 0.4$ is the length of the first pass device, and $M = 160$ which, as discussed in the '320 patent at 5:22:25, "may be chosen as a function of the reference voltage 107 and the desired output voltage in terminals 211, 212, and the current flowing through divider 405, 410."

14. The first pass device of the SD – M04G GI91 SDHC Memory Card Controller is a transistor, which is a type of first pass device contemplated by the '320 Patent. The '320 Patent indicates that "[i]n practice, the first and second pass devices 325, 330 may be, for example, positive channel metal oxide semiconductor (PMOS) transistors." '320 3:36-38. The '320 Patent also refers to the first pass device 325 as a "transistor" at 4:8 and 5:9.

15. After the first limitation, the second limitation of claim 1 states: "a second voltage regulator section coupled to the first voltage regulator section, the second voltage regulator section including a second pass device, having a second regulated voltage output with a second current capacity less than the first current capacity, a width to a length ratio of the first pass device relative to a width to a length ratio of the second pass

device being in the range of approximately 10 to 1000." Toshiba's products, such as its SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller contain this second limitation. In one model, a "Regulator 2" of the SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller is coupled to the "Regulator 1." The "Regulator 2" includes a second pass device, having a second regulated voltage output with a second current capacity less than the first current capacity. In this model, the second current capacity is 66.7, where the second current capacity is given by $W * M / L$, where $W = 5.0$ is the width of the second pass device, $L = 0.6$ is the length of the second pass device, and $M = 8$ which, as discussed in the '320 patent at 5:22:25, "may be chosen as a function of the reference voltage 107 and the desired output voltage in terminals 211, 212, and the current flowing through divider 405, 410." The second current capacity 66.7 of the second regulated voltage output is less than the first current capacity 4000 of the first regulated voltage output.

16. The second pass device of the SD – M04G GI91 SDHC Memory Card Controller is a transistor, which is a type of second pass device contemplated by the '320 Patent. The '320 Patent indicates that "[i]n practice, the first and second pass devices 325, 330 may be, for example, positive channel metal oxide semiconductor (PMOS) transistors." '320 3:36-38.

17. As stated above, the second limitation of claim 1 also states: "a width to a length ratio of the first pass device relative to a width to a length ratio of the second pass device being in the range of approximately 10 to 1000." Toshiba's products, such as its SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller contain this part of the second limitation as its products exhibit this property. For Toshiba's SD – M04G GI91 SDHC Memory Card Controller product, the width to a length ratio of the first pass device (taking into consideration the factor *M*), is 4000, and the width to a length ratio of the second pass device (taking into consideration the factor *M*), is 66.7. One embodiment of relativeness of the width to length ratio of the first and second pass devices, discussed in the '320 Patent at '320 5:6-13, is the ratio of the two computations.

Here, the ratio of 4000 to 66.7 is 60. 60 is in the range of approximately 10 to 1000. Without taking into consideration the factor *M*, the ratio of the width to length ratio of the first pass device is 25 (W = 10.0 / L = 0.4), and the ratio of the width to length ratio of the second pass device is 8.33 (W = 5 / L = 0.6). The ratio of these two computations is 3. 3 is also in the range of approximately 10 to 1000. Another consideration of relativeness is the difference (with or without the factor *M*) between the width to length ratio of the first pass device and the width to length ratio of the second pass device.

18. The first regulated voltage output and the second regulated voltage output correspond to items 211 and items 212 of FIGS. 2 and 3 of the '320 Patent. FIG. 2 is reproduced below:

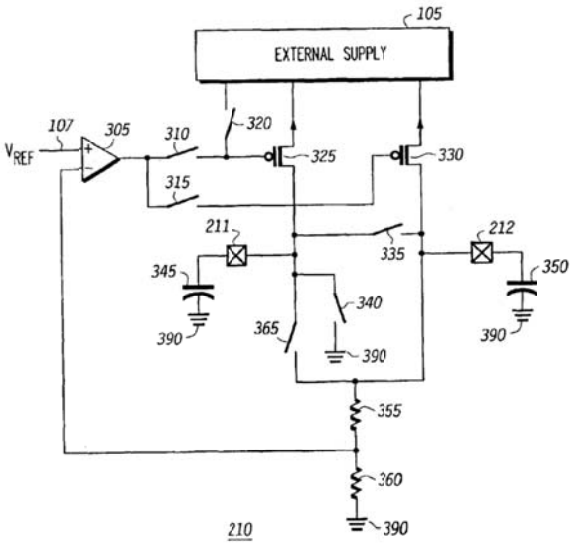


FIG.2

19. After the second limitation, the third and final limitation of claim 1 states: "and a switching circuit coupled to the first voltage regulator section and to the second voltage regulator section, the switching circuit operating the first voltage regulator section together with the second voltage regulator section in a normal mode, and operating only the second voltage regulator section in a power gating mode." Toshiba's products, such as its SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller contain this third limitation. For example, the SD – M04G GI91 SDHC Memory Card Controller has an AND-OR-NOT gate switching circuit that is coupled to

the "Regulator 1" – the first voltage regulator section and "Regulator 2" – the second voltage regulator section. The SDHC Memory Card and SD – M04G GI91 SDHC Memory Card Controller's switching circuit operates the first voltage regulator section together with the second voltage regulator section in a normal mode, and operates only the second voltage regulator section in a power gating mode. The section of the '320 Patent that discusses this is at '320 3:44-59, 4:61-5:5, and 5:47-57 ("The voltage across the fourth switch 365 changes back to 3.0V sometime after the regulator 210 returns to normal mode, in order to avoid bleeding the voltage at the first terminal 211 too early.").

20. As a direct and proximate consequence of Defendants' infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

21. Defendant's infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further manufacture, use, sale and/or offer for sale of products that come within the scope of the '320 Patent.

COUNT II - PATENT INFRINGEMENT OF THE '555 PATENT

22. North Star hereby incorporates paragraphs 1-21 above by reference.

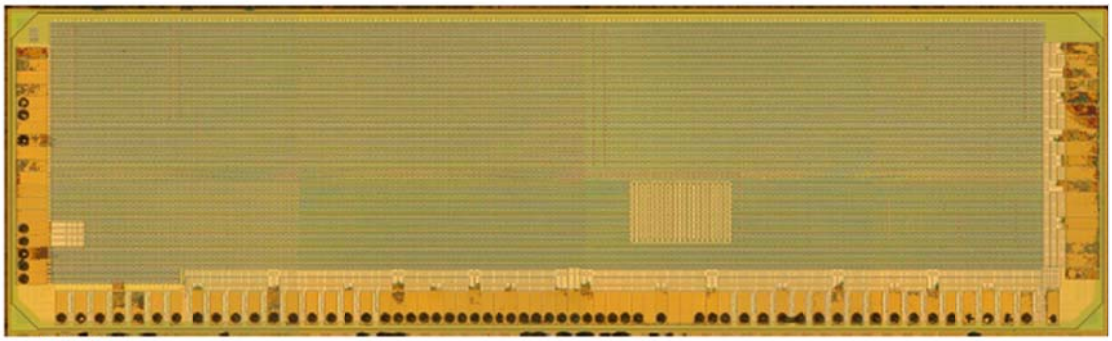
23. Defendants have infringed and continue to infringe at least claim 1 of the '555 Patent, in violation of 35 U.S.C. § 271 through, among other activities, making, using (for example by testing), offering to sell, and/or selling the Toshiba THGBM4G7D2GBAIE Flash Memory Controller.

24. Defendants' infringing products include without limitation their memory controller products, including, for example, the Toshiba THGBM4G7D2GBAIE Flash Memory Controller and other memory controller products. Defendants' infringement may include additional products and technologies (to be determined in discovery)

marketed or used by Defendants. Photos of the THGBM4G7D2GBAIE Flash Memory Controller are shown below, including a Package Top View (top-left), Die Marking (top-right), and Die View (bottom) (Source: ISS Report, "Toshiba THGBM4G7D2GBAIE Flash Memory Controller).

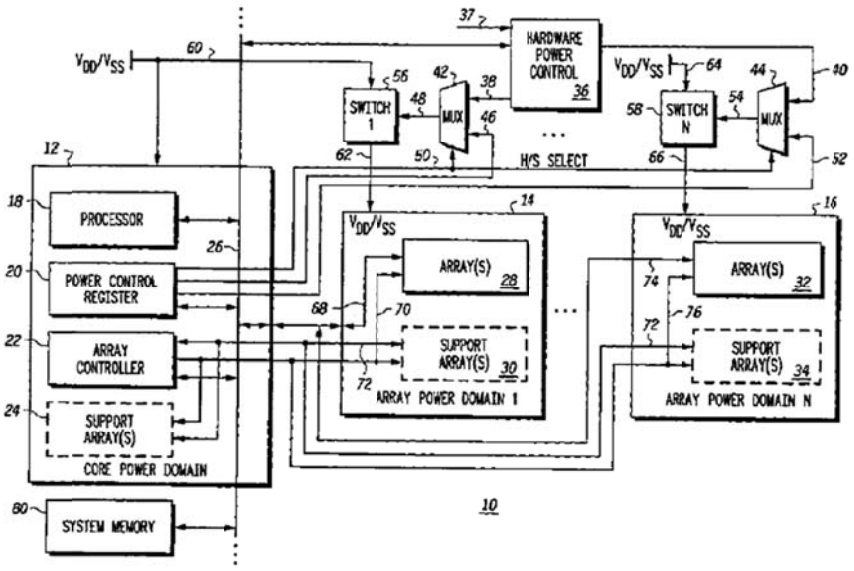
0.1.1 Package Top View

0.2.1 Die Marking



0.2.2 Die View

25. Claim 1 is an exemplary infringed claim. Its preamble states: "An integrated circuit having power management comprising". Toshiba's THGBM4G7D2GBAIE Flash Memory Controller is an integrated circuit having power management. The integrated circuit of the THGBM4G7D2GBAIE Flash Memory Controller contains an MMC I/O Block, a Regulator, Core Logic, and a NAND I/O block. FIG. 1 of the '555 Patent, shown below, is a block diagram view of an integrated circuit with power management for reducing leakage current in circuit arrays.



26. After the preamble, the first limitation of claim 1 states: "processing circuitry for executing instructions." Toshiba's products such as the THGBM4G7D2GBAIE Flash Memory Controller contain this limitation. The THGBM4G7D2GBAIE Flash Memory Controller's processing circuitry is the Core Logic within its integrated circuit, corresponding to processor 18 of the '555 Patent.

27. After the first limitation, the second limitation states: "at least one memory array coupled to the processing circuitry for providing data to the processing circuitry." Toshiba's products such as the THGBM4G7D2GBAIE Flash Memory Controller contain this limitation. The THGBM4G7D2GBAIE Flash Memory Controller has a 6.0 SRAM3 memory array, which is coupled to the processing circuitry and provides data to the processing circuitry via a D[31..0] 32-bit port, and a Q[31..0] 32-bit port.

28. After the second limitation, the third and final limitation states: "and control circuitry coupled to the at least one memory array, the control circuitry removing electrical connectivity of the at least one memory array to a supply voltage terminal by firstly disabling all accesses to the at least one memory array and secondly removing electrical power to all of the at least one memory array to reduce leakage current in the at least one memory array." Toshiba's products such as the THGBM4G7D2GBAIE Flash Memory Controller contain this limitation.

29. The THGBM4G7D2GBAIE Flash Memory Controller has control circuitry coupled to the 6.0 SRAM3 memory array. Components of the control circuitry include 6.7 PWR_SUP_CTR (power supply control) and 6.6 CTR (control) modules.

30. Further, the control circuitry of the THGBM4G7D2GBAIE Flash Memory Controller removes electrical connectivity of the 6.0 SRAM3 memory array to a supply voltage terminal. It does this via a 6.7.5 VDDI_SW module (a VDDI switch) within the 6.7 PWR_SUP_CTR (power supply control). The VDDI switch removes electrical connectivity to a set of VDDI supply voltage terminals (by setting an nSWE port of the VDDI switch).

31. In the THGBM4G7D2GBAIE Flash Memory Controller, the electrical connectivity is removed by firstly disabling all accesses to the at least one memory array. This is accomplished by setting parameters of a 6.7.1 DRV module within the 6.7 PWR_SUP_CTR (power supply control), such that INb is equal to 1 and OU is equal to 0. This results in CTRb (output of the Power Supply Control) equal to 0, and then ACCE of the 6.6 CTR Control Logic equal to 0. With ACCE equal to 0, then WCAD3 [1..0] and RCAD3 [1..0] of a 6.5 CA_DEC (Column Address Decoder) are both equal to 0. When port LE of 6.1.1 LATCHa (Latch (Type A)) is equal to 0, then Q and nQ of 6.1.1 LATCHa (Latch (Type A)) are equal to 0. When port WCAD3 of 6.3.1 WRT_DRV (Write Driver) is equal to 1, then N20 and N23 of 6.3.1 WRT_DRV (Write Driver) are equal to 0. Finally, when port RCAD3 of 6.4.1 S_AMP (Sence Amplifier) is equal to 0, then nDL and DL of 6.4.1 S_AMP are both equal to 0. These parameters disable all access to the 6.0 SRAM3 memory array.

32. In the THGBM4G7D2GBAIE Flash Memory Controller, the electrical connectivity is removed by secondly removing all electrical power to the 6.0 SRAM3 memory array to reduce leakage current in the 6.0 SRAM3 memory array. This is accomplished by the 6.7.5 VDDI_SW module (VDDI switch) of 6.7 PWR_SUP_CTR (Power Supply Control). When nSWE of 6.7.5 VDDI_SW (VDDI Switch) is equal to 1,

then N3 is equal to 0 even though all of VDDI supply voltage terminals are equal to 1 (and N1 and C1 are also equal to 1).

33. As a direct and proximate consequence of Defendants' infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

34. Defendant's infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further manufacture, use, sale and/or offer for sale of products that come within the scope of the '555 Patent.

COUNT III - PATENT INFRINGEMENT OF THE '263 PATENT

35. North Star hereby incorporates paragraphs 1-34 above by reference.

36. Defendants have infringed and continue to infringe at least claims 1-5, and 7 of the '263 Patent, in violation of 35 U.S.C. § 271 through, among other activities, making, using (for example by testing), offering to sell, and/or selling the Toshiba TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash.

37. Defendants' infringing products include without limitation their memory products, including, for example, the Toshiba TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash and other memory products. Defendants' infringement may include additional products and technologies (to be determined in discovery) marketed or used by Defendants.

38. Claim 1 is an exemplary infringed claim. Its preamble states: "A memory system comprising". Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash are memory systems. FIG. 2 of the '263 Patent, shown below, is a block schematic diagram of a memory system in accordance with a preferred embodiment of the '263 Patent.

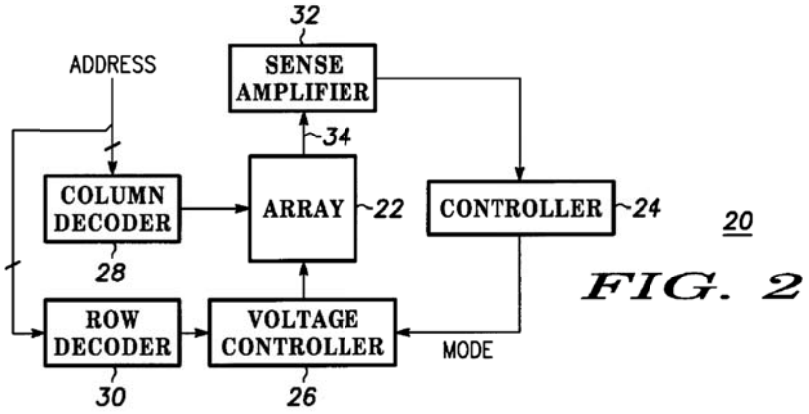
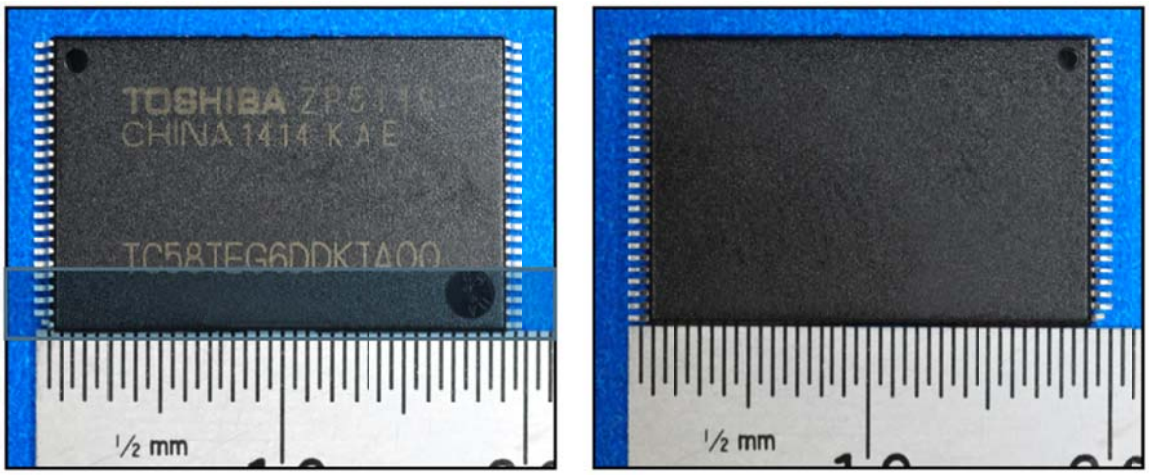
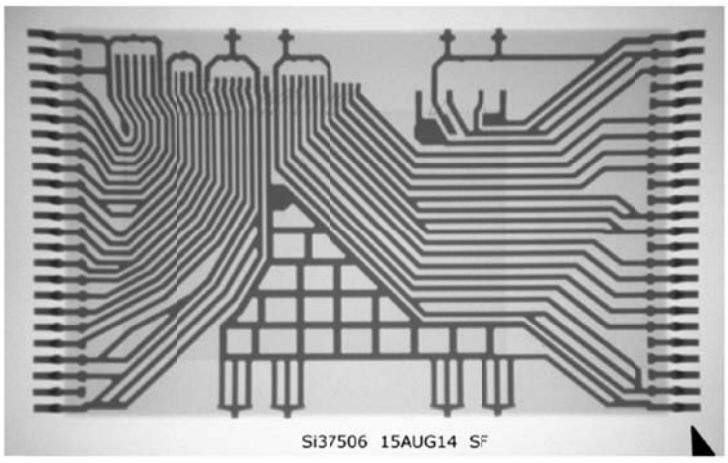


FIG. 2

Package markings of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash are shown below:



A package X-Ray of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash is shown below:



A die photograph of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash is shown below:

Die markings of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash is shown below.

39. After the preamble, the first limitation of claim 1 states: "a memory array having a plurality of memory cells arranged in rows and columns (A), wherein each memory cell has a control terminal (B)." Sublimitations are labeled (A) and (B) for analysis purposes. Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contain this limitation. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains Sublimitation (A) by virtue of its "Memory Array & Wordline Switches" (Source: Figures 3.1 & 3.3.1, report ID#: 0614-36824-O-

5CV-101) shown in a simplified block diagram view of the voltage generator path, as well as a memory array and a plurality of blocks and additional blocks within the memory array. It contains sublimitation (B) by virtue of a flash memory cell within the memory array, as well as 128-bit port WLE[127:0].

40. After the first limitation, the second limitation states: "a voltage controller for providing to the control terminal of a memory cell (C) a first verify voltage signal (D) during a first verify cycle (E) or a second verify voltage signal (F) during a second verify cycle (G), the first verify voltage signal having a predetermined voltage level that corresponds substantially to a threshold voltage level of a memory cell in the array in a first state (H) and the second verify voltage signal having a predetermined voltage level that corresponds substantially to a threshold voltage level of a memory cell in the array in a second state (I)." Sublimitations are labeled (C) – (I) for analysis purposes. Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contain this limitation.

41. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (C), a voltage controller for providing to the control terminal of a memory cell, by virtue of its voltage generator path, including a Bandgap Voltage Reference 1 (BGVR3), Bandgap Voltage Reference 2 (GVREF1), Voltage Pump (VPUMP4B and VPUMP4A), Voltage Regulator (VREG_11), Voltage Generators, Global Wordline Switches 2 (V_WVS), Global Wordline Switches 1 (V1GWL[24:0]), Global Wordline Selectors (GWLE[127:0] and V1GWL[9]), and MVBG between the Main Bandgap Voltage Reference and GVREF1 Voltage Generator. The generated erase verify and program verify voltages on output signal VREG_11 are determined by the configurable output of the resistor divider circuit on a node between VPUMP4B and VPUMP4A. The VREG_11 signal is the verify signal for providing the erase verify signal with a first value during the erase verify cycle and for also providing the program verify signal with a second value during the program verify cycle. See Global Wordline Switches & Selectors (Source: Figure 7.5, report ID#: 0614-36824-O-5CV-101), Global

Wordline Switches & Selectors (Source: Figures 7.5.2, 7.5.1.2.3 & 7.5.1.1, report ID#: 0614-36824-O-5CV-101), Voltage Regulator (Source: Figure 7.6.11.2, report ID#: 0614-36824-O-5CV-101), Bandgap Voltage Reference 1 (Source: Figure 7.6.11.1, report ID#: 0614-36824-O-5CV-101), Voltage Pump (Source: Figure 7.8.4, report ID#: 0614-36824-O-5CV-101), and Bandgap Voltage Reference 2 (Source: Figures 7.4.4 & 7.4.5, report ID#: 0614-36824-O-5CV-101).

42. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (D), a first verify voltage signal, by virtue of an Erase Verify Pulse: 0.4V. At the end of the erase pulse, the erase cycle is complete (no more erase pulses applied) indicating an erase memory cell. See Erase after program for one Block (Source: Figure 2.1.g, report ID#: IP_2909-37506).

43. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (E), during a first verify cycle, by virtue of tracking the 1) CH1 500 mV 10 us GWLE[57], 2) CH2 500 mV 10 us V1GWL[9], 3) CH3 500 mV 10 us V_WVS, and 4) CH4 500 mV 10 us VREG_11, as well as the Erase Verify Pulse: 0.4V. See Erase after program for one Block (Source: Figure 2.1.g, report ID#: IP_2909-37506).

44. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (F), or a second verify voltage signal, by virtue of Wordline Program Verify Select Pulse 0.6V (of 0.6, 2.2 & 3.8 V). At that marking, the program state 1 cycle is now complete (no more program verify pulses of 0.6 V is applied) indicating the memory cell has reached its first intermediate threshold voltage (state 1). See Program Data “random”– GWLE[57] Selected (Source: Figure 2.1.c, report ID#: IP_2909-37506).

45. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (G), during a second verify cycle, by virtue of Wordline Program Verify Select Pulses 0.6, 2.2 & 3.8 V. See Program Data “random”– GWLE[57] Selected (Source: Figure 2.1.c, report ID#: IP_2909-37506).

46. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (H), the first verify voltage signal having a predetermined voltage level that corresponds substantially to a threshold voltage level of a memory cell in the array in a first state, by virtue of an Erase State. The voltage level of the erase verify voltage (0.4 volts) is sufficient to determine if the memory cell is conductive or not (checking for low threshold voltage). See Simplified Memory States Diagram (Source: Figure 2.2, report ID#: IP_2909-37506).

47. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (I), and the second verify voltage signal having a predetermined voltage level that corresponds substantially to a threshold voltage level of a memory cell in the array in a second state, by virtue of a Program State 1. The voltage level of the program verify voltage (0.6 volts) is sufficient to determine if the memory cell is non-conductive (checking for high threshold voltage). See Simplified Memory States Diagram (Source: Figure 2.2, report ID#: IP_2909-37506).

48. As a direct and proximate consequence of Defendants' infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

49. Defendant's infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further manufacture, use, sale and/or offer for sale of products that come within the scope of the '263 Patent.

COUNT IV - PATENT INFRINGEMENT OF THE '875 PATENT

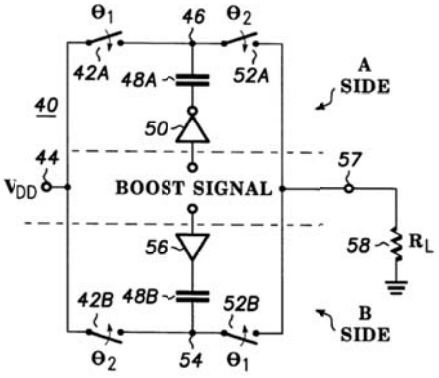
50. North Star hereby incorporates paragraphs 1-49 above by reference.

51. Defendants have infringed and continue to infringe at least claims 1-3 of the '875 Patent, in violation of 35 U.S.C. § 271 through, among other activities, making,

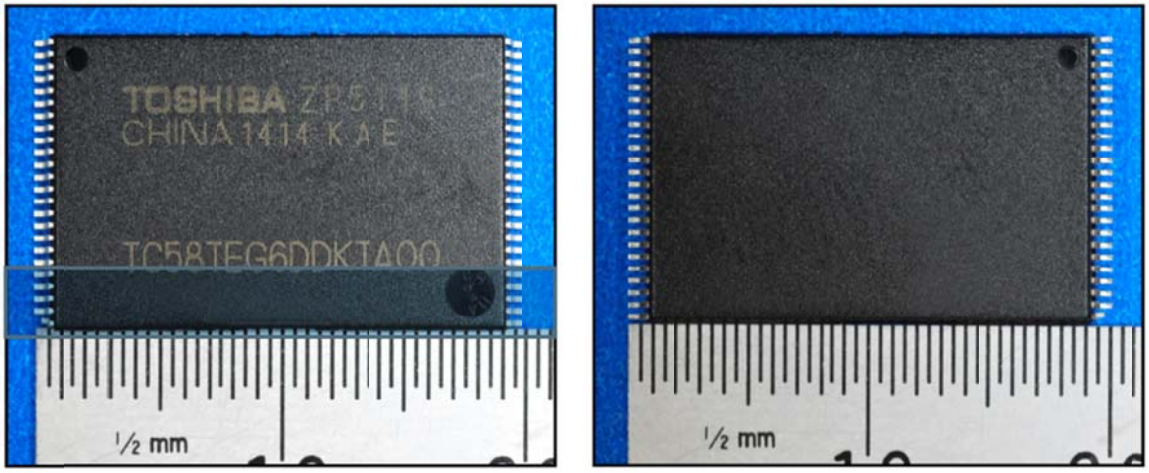
using (for example by testing), offering to sell, and/or selling the Toshiba TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash.

52. Defendants' infringing products include without limitation their memory products, including, for example, the Toshiba TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash and other memory products. Defendants' infringement may include additional products and technologies (to be determined in discovery) marketed or used by Defendants.

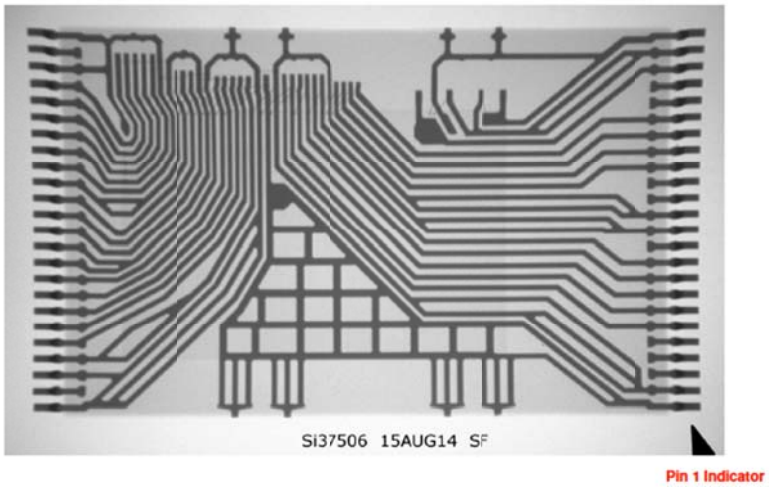
53. Claim 1 is an exemplary infringed claim. Its preamble states: "A boost circuit having an input terminal and an output terminal (A), comprising". The preamble and sublimitations of claim 1 are labeled (A) – (G) for analysis purposes. Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash comprise a boost circuit having an input terminal and an output terminal (A) by virtue of a Pump Cell 1of a Voltage Pump Block. See Voltage Pump Block (Source: Figure 7.8.3.2, report ID#: 0614-36824-O-5CV-101). Pump Cell 1 has an input terminal VIN and output terminal VOUT. See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101). FIG. 3 of the '875 Patent, shown below, is a schematic diagram of an embodiment of the boost circuit of the invention, showing input terminal 44 and output terminal 57.



Package markings of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash are shown below:



A package X-Ray of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash is shown below:



A die photograph of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash is shown below:

Die markings of the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash is shown below.

54. After the preamble, the first limitation of claim 1 states: "a first switch coupled between the input terminal and the output terminal (B) and operated by a first phase signal (C)." The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (B), a first switch coupled between the input terminal and the output terminal, by virtue of a switch within the Pump Cell 1 where the switch has properties HV W = 13.0U*2, and L = 1.5U. See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101).

55. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (C), and operated by a first phase signal, by virtue of a CK_BST port on capacitor (block CAP 6) on the Pump Cell 1 (VH2CK1BST = 1 out of Local

Clock Booster). See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101) and Clock Divider Selector & Generator (Source: Figures 7.8.3.2.9 & 7.8.3.2.10, report ID#: 0614-36824-O-5CV-101).

56. After the first limitation, the second limitation states: "a second switch coupled between the input terminal and the output terminal (D) and operated by a second phase signal that is opposite to the first phase signal (E)." Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contain this limitation. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (D), a second switch coupled between the input terminal and the output terminal, by virtue of another switch within the Pump Cell 1 where the switch has properties HV W = 13.0U*2, and L = 1.5. See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101).

57. The TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contains sublimitation (E), and operated by a second phase signal that is opposite to the first phase signal, by virtue of another CK_BST port on capacitor (CAP 6) on the Pump Cell 1 (VH2CK1BST~). See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101). Also, by virtue of VH2CK1BST = "0" out of the Local Clock Booster. See Clock Divider Selector & Generator (Source: Figures 7.8.3.2.9 & 7.8.3.2.10, report ID#: 0614-36824-O-5CV-101).

58. After the second limitation, the third limitation states: "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal (F)." Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contain this limitation, by virtue of a capacitor (CAP 5) and ports CK and NOT(CK) (for receiving a boost signal) on a Level Shifter (VH2CKDEL1 and VH2CKDEL1~). The first terminal is terminal C2 on the CAP 5 block. The second terminal is between the Level Shifter and the CAP 5 block. See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101). Also, by virtue of terminal CK_IN into a Clock Buffer with outputs VH2CKD1 And VH2CKD1~, as well

as inputs VH2CKD1 and VH2CKD1~ into non-overlapping Clock Generator, and VH2CKDEL1~ and VH2CKDEL1 for receiving a boot signal. See Clock Divider Selector & Generator (Source: Figures 7.8.3.2.9 & 7.8.3.2.10, report ID#: 0614-36824-O-5CV-101). Also, by virtue of CK_IN = "1", LEVEL SHIFTER B4 = "1", and outputs VH2CKD1 = "1" and VH2CKD1~ = 0 out of Clock Buffer, and VH2CKD2 = "1" and VH2CKD2~ = "0" into a non-overlapping clock generator, as well as VH2CKDEL1~ = "0" and VH2CKDEL1 for receiving a boost signal. See Clock Buffer & Non-overlapping Clock Generator (Source: Figures 7.8.3.2.10.2 & 7.8.3.2.9.2, report ID#: 0614-36824-O-5CV-101).

59. After the third limitation, the fourth limitation states: "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal (G)." Toshiba's products such as the TC58TEG6DDKTA00 19 nm (Advanced) MLC NAND Flash contain this limitation, by virtue of another capacitor (CAP 5 block) on Pump Cell 1. The first terminal is a terminal (C2) on the other CAP 5, and the second terminal is terminal (C1) on the other CAP 5. See Pump Cell 1 (Source: Figure 7.8.3.2.5, report ID#: 0614-36824-O-5CV-101).

60. As a direct and proximate consequence of Defendants' infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

61. Defendant's infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further manufacture, use, sale and/or offer for sale of products that come within the scope of the '875 Patent.

JURY DEMAND

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, North Star demands a trial by jury on all issues presented that can properly be tried to a jury.

REQUEST FOR RELIEF

THEREFORE, North Star asks this Court to enter judgment against Defendants and against their subsidiaries, affiliates, agents, servants, employees and all persons in active concert or participation with Defendants, granting the following relief:

A. An award of damages adequate to compensate North Star for the infringement that has occurred, together with prejudgment interest from the date infringement began and postjudgment interest;

B. All other damages permitted by 35 U.S.C. § 284;

C. A permanent injunction prohibiting further infringement, inducement and contributory infringement of the ’320 Patent, the’555 Patent, the ’263 Patent, and the ’875 Patent; and

D. Such other and further relief as this Court or a jury may deem proper and just.

Dated: May 26, 2016

Respectfully submitted,

FARNAN LLP

/s/ Brian Farnan

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