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NORTH STAR INNOVATIONS INC.

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

NORTH STAR INNOVATIONS INC.,

Plaintiff,

vs.

ELITE SEMICONDUCTOR MEMORY TECHNOLOGY INC. d/b/a ESMT, and KAGA ELECTRONICS (USA) INC. d/b/a TAXAN,

Defendants.

CASE NO. 8:16-cv-00600-SJO-FFM

FIRST AMENDED COMPLAINT

JURY TRIAL DEMANDED

Plaintiff North Star Innovations Inc. ("Plaintiff" or "North Star"), by and through its attorneys, files this First Amended Complaint for Patent Infringement against Defendant Elite Semiconductor Memory Technology Inc. d/b/a ESMT ("ESMT") and Defendant Kaga Electronics (USA) Inc. d/b/a TAXAN ("Kaga"), and alleges as follows:

PARTIES

1. North Star is a corporation organized and existing under the laws of the State of Delaware, with a principal place of business at 600 Anton Blvd., Costa Mesa, California 92626.

2. North Star is the owner of seminal patents in the fields of integrated circuits, semiconductor memory architecture, and semiconductor memory devices, including patents that address volatile memory, such as DRAM and SRAM. Plaintiff's portfolio includes patents that teach valuable innovations and improvements related to – among other things – speed, power consumption, density, reliability, and cost. Plaintiff is actively engaged in licensing efforts with respect to such technologies.

3. On information and belief, Defendant ESMT is a Taiwanese corporation organized and existing under the laws of Taiwan, with a principal place of business at: Elite Technology Building, No.23, Industry East Rd. IV Science-Based Industrial Park, Hsinchu 300, Taiwan. Upon information and belief, ESMT may be served with process in Taiwan as follows: by way of letters rogatory; pursuant to the foreign country's laws governing domestic service of process, i.e., through service by the clerk of Taiwan's court; or, with ESMT's consent, through service upon ESMT's U.S. counsel, Dr. Christian E. Mammen, Hogan Lovells, 3 Embarcadero Center, Suite 1500, San Francisco, CA 94111, U.S.A.

4. According to the websites of ESMT and Kaga, ESMT is a provider of various memory ICs. In contrast to main memory products, such as DRAM used for PCs, servers, and workstations, ESMT focuses its design and manufacturing

efforts on specialty legacy memory ICs, including DRAM products for such markets as PC peripherals, IA products, consumer products, optical devices, and communication devices. ESMT markets a full range of densities, from 1MB to 256MB, and a wide variety of specialty DRAM products, including EDO, SDRAM, and DDR. On information and belief, ESMT, through its own website and through U.S. suppliers and distributors of electronic components such as Kaga, markets or has marketed its products throughout the U.S. For example, at the time of the filing of the Original Complaint, Kaga's website stated: "KAGA and ESMT want to be your specialty memory partner."

5. Kaga is a corporation organized and existing under the law of the State of California, with its principal place of business at 780 Montague Expressway Suite #403, San Jose, CA 95131-1318. Kaga may be served by serving its registered agent for services of process, Jeffrey Joseph Demello, 780 Montague Expressway Suite #403, San Jose, CA 95131-1318. Alternatively, Kaga may be served by serving its counsel of record, John F. Ward, at: Kelly Drye & Warren LLP, Attn: John F. Ward, Esq., 101 Park Ave., New York, NY 10178, or at: jward@kelleydrye.com.

6. According to its website, Kaga, a wholly-owned subsidiary of Japan-based Kaga Electronics Co., Ltd., is and/or was a distributor of electronic components, including semiconductors and memory products. According to its website, Kaga serves and/or served U.S. customers in various markets, including "consumer electronics, industrial automation, automotive, medical equipment, network/telecom, semi-infrastructural area, and gaming/amusement," and it functions as a sales agency for PC … peripherals made by [various] worldwide brands," including, at least as of the time the Original Complaint was filed, ESMT products. At the time the Original Complaint was filed, Kaga's website specifically advertised that "KAGA and ESMT want to be your specialty memory partner."

JURISDICTION AND VENUE

7. This action arises under the patent laws of the United States, 35 U.S.C. § 1 *et seq.*, including §§ 271, 281, 282, 283, 284, and 285. This Court has subject matter jurisdiction over this patent infringement action pursuant to 28 U.S.C. §§ 1331, and 1338(a).

8. This Court has personal jurisdiction over ESMT. Upon information and belief, ESMT, directly or indirectly through its agents or suppliers, has regularly conducted and continues to conduct business in the U.S., in the State of California, and in this judicial district. Further, upon information and belief, ESMT has, through its actions, purposely availed itself of this forum, and such actions give rise to the claims described in this Complaint, such that this Court's exercise of jurisdiction would be reasonable and fair. On information and belief, Defendant, directly or indirectly through its current and/or former suppliers or agents (such as, for example, Kaga), has committed infringing activities in this judicial district by using, marketing, offering for sale, selling, and/or importing products and systems that infringe the Patents-In-Suit (as defined below) or by placing such infringing products and systems into the stream of commerce with the awareness, knowledge, and intent that they would be used, offered for sale, or sold by others in this judicial district and/or purchased by consumers in this judicial district.

9. This Court has personal jurisdiction over Kaga. Upon information and belief, Kaga has regularly conducted and continues to conduct business in the U.S., in the State of California, and in this judicial district. On information and belief, Kaga has committed infringing activities in California and in this judicial district by using, marketing, offering for sale, selling, and/or importing products and systems that infringe the Patents-In-Suit (as defined below) or by placing such infringing products and systems into the stream of commerce with the awareness, knowledge, and intent that they would be used, offered for sale, or sold by others in this judicial district and/or purchased by consumers in this judicial district. Further, this Court has personal jurisdiction over Kaga because Kaga is incorporated under the laws of

the State of California. Kaga has thereby availed itself of the privileges of conducting business in the State of California and has sought protection and benefit from the laws of the State of California. This Court's exercise of personal jurisdiction over Kaga would therefore comport with due process.

10. Venue is proper pursuant to 28 U.S.C. §§ 1391(b) and 1400(b).

THE PATENTS-IN-SUIT

11. On February 23, 1999, U.S. Patent No. 5,875,143 ("the '143 Patent") – entitled "Dynamic Memory Device with Refresh Circuit and Refresh Method" – was lawfully and properly issued by the United States Patent and Trademark Office ("USPTO"), after a full and fair examination. The named inventor on the '143 Patent is Jacob Ben-Svi of Austin, Texas. A true and correct copy of the '143 Patent is attached hereto as Exhibit A and incorporated by reference.

12. Generally speaking, the '143 Patent teaches, among other things, an optimized, flexible, programmable refresh circuit that reduces size and power consumption in a DRAM or SDRAM memory device by allowing for partial refresh of a memory array.

13. On October 3, 2000, U.S. Patent No. 6,127,875 ("the '875 Patent") – entitled "Complimentary Double Pumping Voltage Boost Converter" – was lawfully and properly issued by the United States Patent and Trademark Office ("USPTO"), after a full and fair examination. The named inventors on the '875 Patent are Steven Peter Allen, Ahmad H. Atriss, Gerald Lee Walcott, and Walter C. Seelbach, all of Arizona. A true and correct copy of the '875 Patent is attached hereto as Exhibit B and incorporated by reference.

14. Generally speaking, the '875 Patent teaches, among other things, an efficient and compact voltage boosting circuit that boosts the available supply voltage and limits output distortion.

15. On July 12, 2005, U.S. Patent No. 6,917,555 ("the '555 Patent") – entitled "Integrated Circuit Power Management for Reducing Leakage Current in

Circuit Arrays and Method Therefor" – was lawfully and properly issued by the United States Patent and Trademark Office ("USPTO"), after a full and fair examination. The named inventors on the '555 Patent are Ryan D. Bedwell, Christopher K.Y. Chun, Qadeer A. Qureshi, and John J. Vaglica, all of Texas. A true and correct copy of the '555 Patent is attached hereto as Exhibit C and incorporated by reference.

16. Generally speaking, the '555 Patent teaches, among other things, a novel design for an integrated circuit with power management capabilities, where, in certain embodiments, multiple, independent power planes are used to eliminate or reduce leakage current.

17. The '143 Patent, the '875 Patent, and the '555 Patent may be referred to individually as a "Patent-in-Suit" or collectively as the "Patents-in-Suit."

18. By way of assignment, Plaintiff is the owner of all right, title, and interest in and to the Patents-in-Suit, including the rights to prosecute this action and to collect and receive damages for all past, present, and future infringements.

COUNT ONE: INFRINGEMENT OF THE '143 PATENT

19. Plaintiff incorporates the above allegations as if set forth here in full.

20. The '143 Patent is valid and enforceable. Defendants do not have a license to practice the patented inventions of the '143 Patent.

21. Defendants, individually or through their agents or suppliers, have infringed and are currently infringing, either literally or under the doctrine of equivalents, the '143 Patent by, among other things, making, using, offering for sale, selling, and/or importing within this judicial district and elsewhere in the United States – without license or authority – products, devices, or systems falling within the scope of one or more claims of the '143 Patent. For example, ESMT's 256Mb Mobile DDR SDRAM, ESMT Part Number M53D256328A ("ESMT's Mobile DDR SDRAM"), which, by way of example and upon information and

belief, is and/or has been imported, offered for sale, and/or sold by Kaga, directly infringes at least Claim 2 of the '143 Patent, either literally or under the doctrine of equivalents.

22. More specifically, ESMT's Mobile DDR SDRAM infringes at least Claim 2 because it meets each and every limitation of Claim 2, either literally or under the doctrine of equivalents. For example, the referenced product includes, among other things, "a reference register for storing a reference address and control logic coupled to said reference register, to said address generator, and to said decoder, wherein said control logic uses said addresses generated by said address generator and said reference address to determine which storage elements are in said first sub-set and which storage elements are in said second sub-set."

23. On information and belief, additional, similar models of ESMT's memory products are believed to infringe one or more claims of the '143 Patent. Plaintiff expressly reserves the right to assert additional claims and to identify additional infringing products in accordance with the Court's scheduling order and local rules.

24. Plaintiff has been damaged by Defendants' infringing conduct and will continue to be damaged unless Defendants are enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringers, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendants from committing the infringing acts.

COUNT TWO: INFRINGEMENT OF THE '875 PATENT

25. Plaintiff incorporates the above allegations as if set forth here in full.

26. The '875 Patent is valid and enforceable. Defendants do not have a license to practice the patented inventions of the '875 Patent.

27. Defendants have infringed and are currently infringing the '875 Patent by, among other things, making, using, offering for sale, selling, and/or importing within this judicial district and elsewhere in the United States – without license or authority – products, devices, and/or systems falling within the scope of one or more claims of the '875 Patent. For example, ESMT's 128 Mb DDR SDRAM, ESMT Part Number M13S128168A-5T ("ESMT's DDR SDRAM"), which, by way of example and upon information and belief, is and/or has been imported, offered for sale, and/or sold by Kaga, directly infringes at least Claim 1 of the '875 Patent, either literally or under the doctrine of equivalents.

28. More specifically, the referenced product infringes at least Claim 1 because it meets each and every limitation of Claim 1, either literally or under the doctrine of equivalents. For example, the referenced product includes, among other things, a boost circuit that includes "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal; a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal; a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal."

29. On information and belief, additional, similar models of ESMT's memory products are believed to infringe one or more claims of the '875 Patent. Plaintiff expressly reserves the right to assert additional claims and to identify additional infringing products in accordance with the Court's scheduling order and local rules.

30. Plaintiff has been damaged by Defendants' infringing conduct and will continue to be damaged unless Defendants are enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be

determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringers, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendants from committing the infringing acts.

COUNT THREE: INFRINGEMENT OF THE '555 PATENT

31. Plaintiff incorporates the above allegations as if set forth here in full.

32. The '555 Patent is valid and enforceable. Defendants do not have a license to practice the patented inventions of the '555 Patent.

33. Defendants have infringed and are currently infringing the '555 Patent by, among other things, making, using, offering for sale, selling, and/or importing within this judicial district and elsewhere in the United States – without license or authority – products, devices, and/or systems falling within the scope of one or more claims of the '555 Patent. For example, ESMT's DDR SDRAM, which, by way of example and upon information and belief, is and/or has been imported, offered for sale, and/or sold by Kaga, directly infringes at least Claim 15 of the '555 Patent, either literally or under the doctrine of equivalents.

34. More specifically, the referenced product infringes at least Claim 15 because it meets each and every limitation of Claim 15, either literally or under the doctrine of equivalents. For example, the above-referenced accused product is: "An integrated circuit having power management comprising:[1] processing circuitry for executing instructions; a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane; memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the memory array peripheral circuitry being selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane; and control circuitry coupled to the

[1] Plaintiff does not hereby suggest or concede that the preamble of this or any other asserted claim constitutes a substantive limitation. That issue is expressly reserved for the claim construction stage.

memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the control circuitry selectively removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells."

35. On information and belief, additional, similar models of ESMT's memory products are believed to infringe one or more claims of the '555 Patent. Plaintiff expressly reserves the right to assert additional claims and to identify additional infringing products in accordance with the Court's scheduling order and local rules.

36. Plaintiff has been damaged by Defendants' infringing conduct and will continue to be damaged unless Defendants are enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringers, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendants from committing the infringing acts.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully prays for entry of judgment as follows:

1. That Defendants have directly infringed, either literally or under the doctrine of equivalents, one or more claims of each of the Patents-In-Suit;

2. That Plaintiff is entitled to, and should recover, all damages to which Plaintiff is entitled under 35 U.S.C. § 284, but in no event less than a reasonable royalty;

3. That Defendants be ordered to provide an accounting;

4. That Plaintiff, as the prevailing party, shall recover from Defendants all taxable costs of court;

5. That Plaintiff shall recover from Defendants all pre- and post-judgment interest on the damages award, calculated at the highest interest rates allowed by law;

6. That Plaintiff is entitled to enhanced damages from ESMT of up to three times the amount found by the jury or ordered by the Court, pursuant to 35 U.S.C. § 284;

7. That this case is exceptional and that Plaintiff therefore shall recover its attorney's fees and other recoverable expenses, under 35 U.S.C. § 285; and

8. That Plaintiff shall recover from Defendants such other and further relief as the Court may deem appropriate.

Dated: July 11, 2016

/s/ Brandon C. Fernald

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Attorneys for Plaintiff
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DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury on all issues properly triable by jury.

Dated: July 11, 2016

/s/ Brandon C. Fernald

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Attorneys for Plaintiff
NORTH STAR INNOVATIONS INC.

EXHIBIT A

US005875143A

United States Patent [19]

Ben-Zvi

[11] Patent Number: 5,875,143

[45] Date of Patent: Feb. 23, 1999

[54] **DYNAMIC MEMORY DEVICE WITH REFRESH CIRCUIT AND REFRESH METHOD**

[75] Inventor: **Jacob Ben-Zvi**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **976,835**

[22] Filed: **Nov. 24, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 683,642, Jul. 15, 1996, abandoned.

[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/222**; 365/185.11; 365/185.22; 365/230.03

[58] **Field of Search** 365/222, 230.03, 365/185.11, 185.22

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,914,630 4/1990 Fujisthima et al. 365/222

5,247,655 9/1993 Khan et al. 395/550

FOREIGN PATENT DOCUMENTS

0488593 6/1992 European Pat. Off. .

0609577 8/1994 European Pat. Off. .

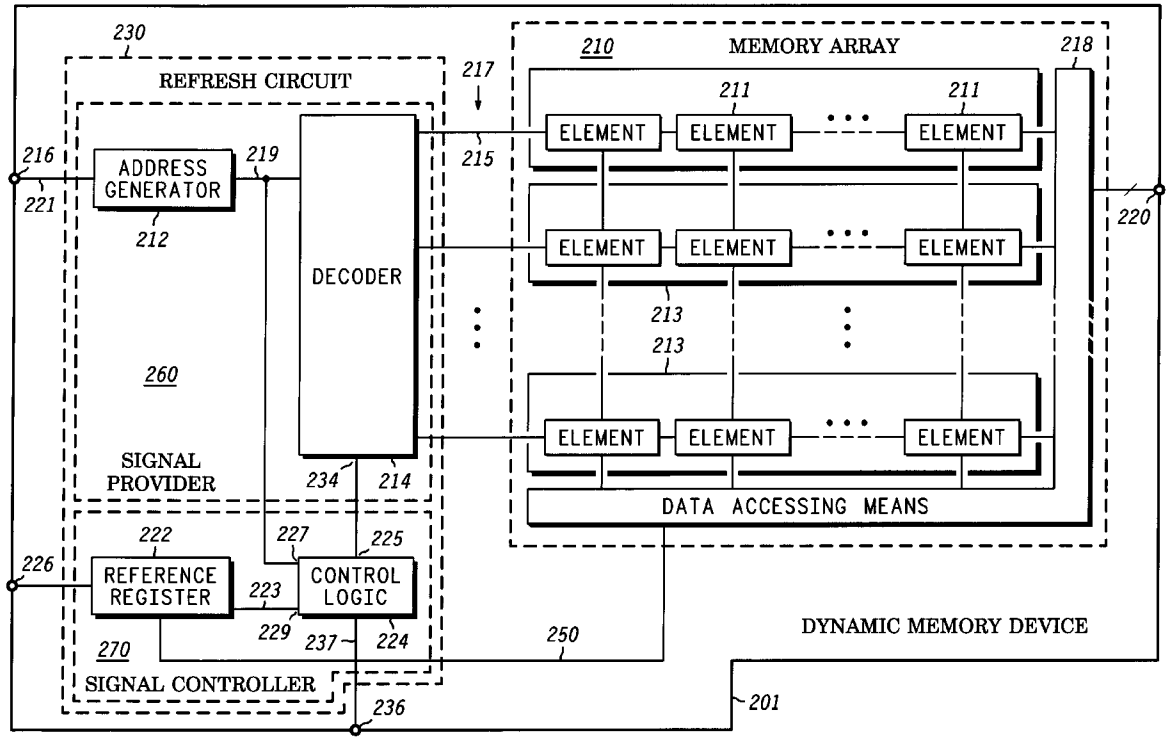
Primary Examiner—David Nelms

Assistant Examiner—Hoai V. Ho

[57] **ABSTRACT**

A refresh circuit (**230**) and a method for the refresh of dynamic memory devices (**201**) are described where the rows to be refreshed are determined by a logical function and by a reference address (**223**). The availability of refresh signals (**215**) for the rows at the outputs (**217**) of a decoder (**214**) is determined by control logic (**224**) which is connected to an address generator (**212**) and to a reference register (**222**) which contains a reference address (**223**). By supplying the reference address (**223**) to the refresh circuit (**230**) it is possible to determine which rows are to be refreshed. The memory array (**210**) of the dynamic memory device (**201**) can be refreshed partially and energy consumption for the refresh can be reduced.

13 Claims, 2 Drawing Sheets



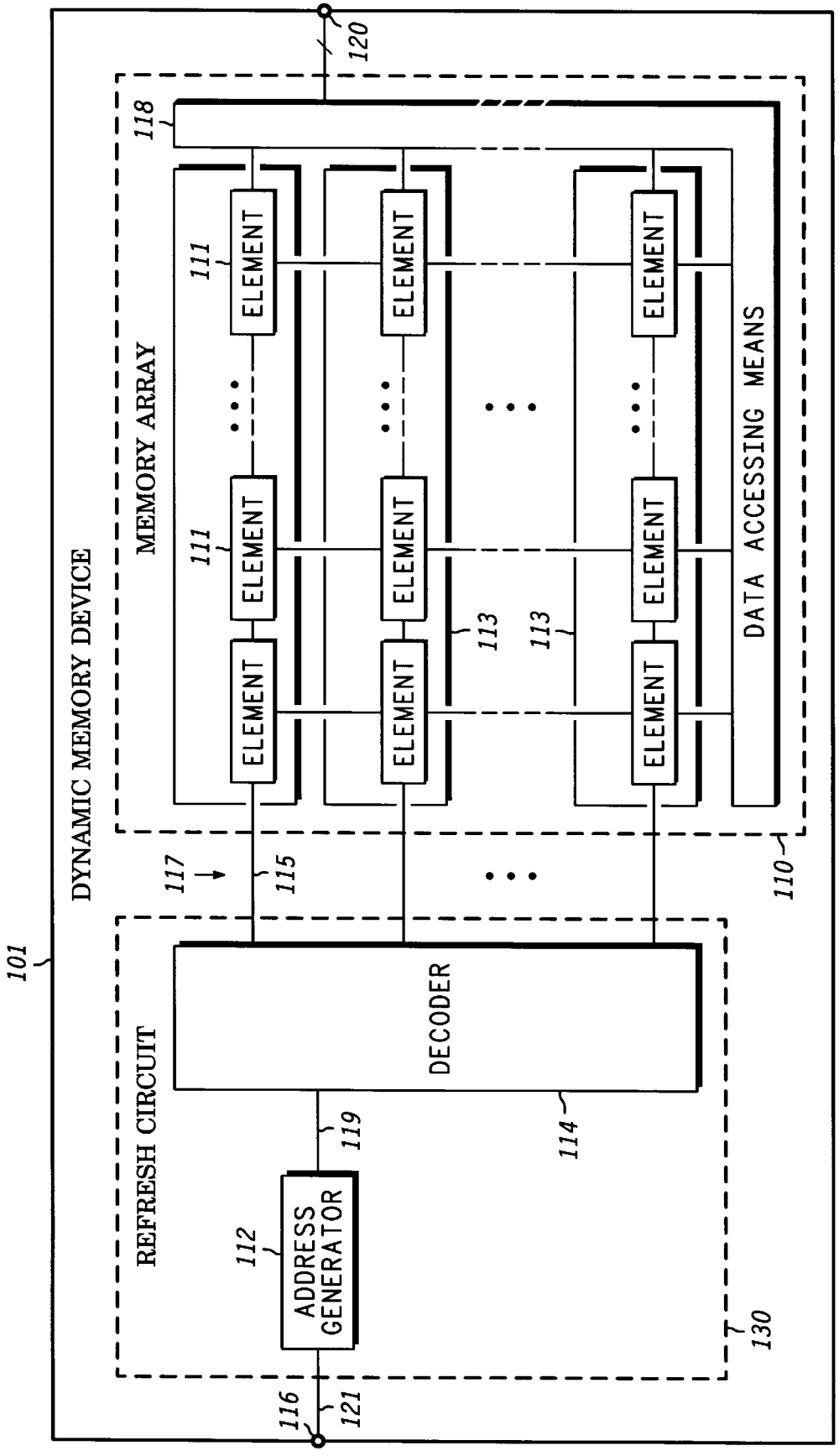


FIG. 1 -PRIOR ART-

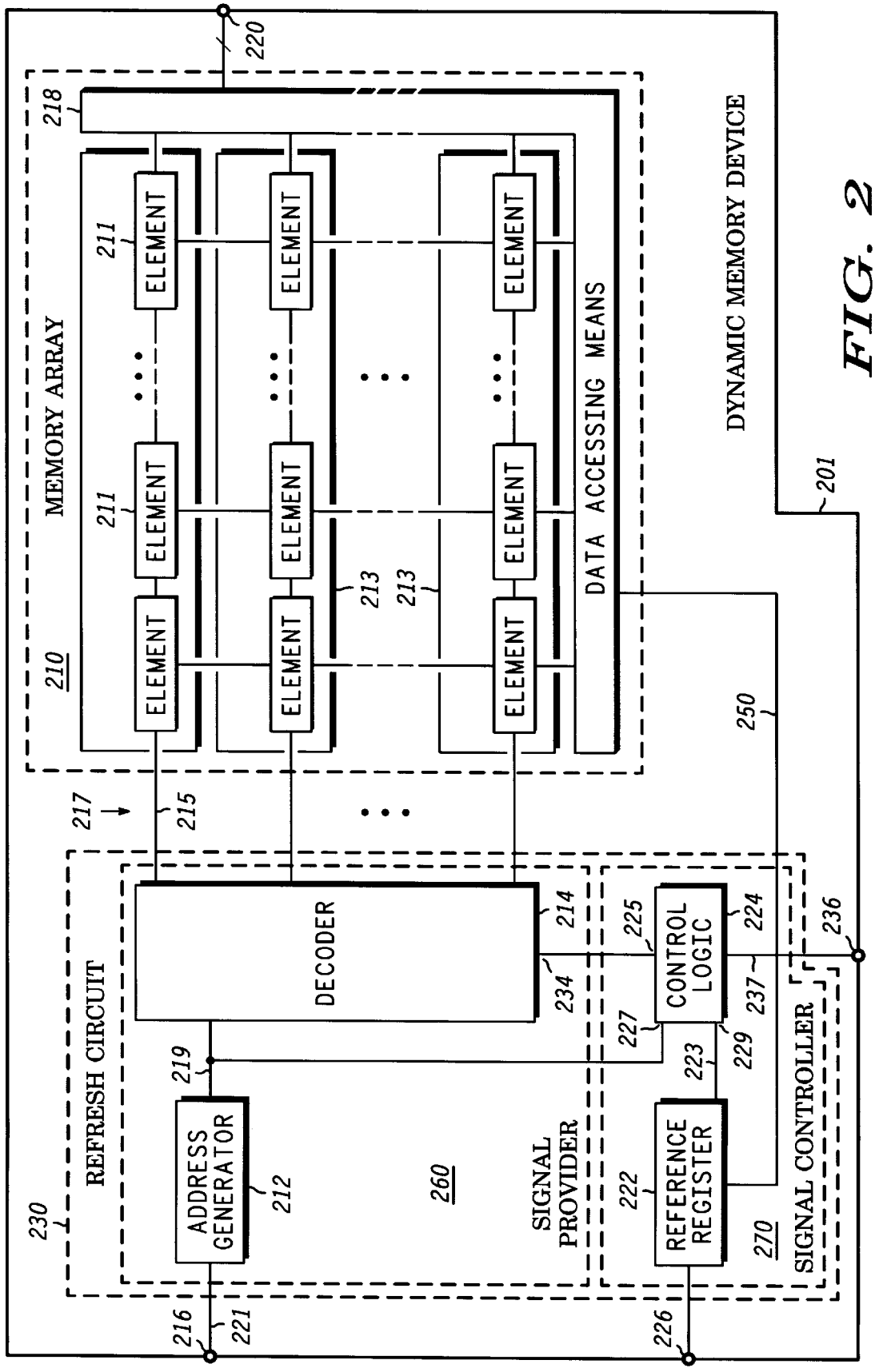

DYNAMIC MEMORY DEVICE
MEMORY ARRAY
ELEMENT
DATA ACCESSING MEANS
DECODER
CONTROL LOGIC
REFRESH CIRCUIT
ADDRESS GENERATOR
SIGNAL PROVIDER
REFERENCE REGISTER
SIGNAL CONTROLLER
220
218
211
213
210
201
250
217
215
214
225
224
236
234
237
227
219
223
229
212
260
222
270
230
216
221
226

FIG. 2

DYNAMIC MEMORY DEVICE WITH REFRESH CIRCUIT AND REFRESH METHOD

This application is a continuation of prior patent application Ser. No. 08/683,642 filed Jul. 15, 1996 now abandoned.

FIELD OF THE INVENTION

The present invention relates to a dynamic memory device, and a method to refresh dynamic memory devices, as for example but not limited to a Dynamic Random Access Memory (DRAM).

BACKGROUND OF THE INVENTION

Dynamic memory devices such as DRAM need to be refreshed. This consumes energy. In many systems energy consumption is very crucial for performance, and the power used for refreshing should be reduced.

Energy consumption can be reduced by using a memory that consists not only of a DRAM but also of a less power consuming static memory (SRAM). During standby mode critical data can be stored in the SRAM, and the DRAM can be switched off and not refreshed. Providing an SRAM leads to additional cost and space. Moreover, two different memory access cycles are required.

U.S. Pat. No. 5,331,601 describes a memory device that alters the input refresh addresses to access fewer memory cells to save power, or to address more memory cells to decrease the refresh time. The circuit contains a simple transistor configuration that blocks certain address bits, then substitutes active bits in their place to the address decoder. The circuit also includes a controller that is responsive to the memory device entering the refresh mode. When the device is used in refresh mode, the address bits may be passed unblocked to the address decoder for full user control.

Another prior art reference, European patent application 488 593, relates to the stability of the refresh in case the power supply fails.

FIG. **1** shows a schematic block diagram of prior art dynamic memory device **101**.

Dynamic memory device **101** comprises memory array **110**, address generator **112** and decoder **114**. The combination of address generator **112** and decoder **114** is referred to as refresh circuit **130**. As shown in FIG. **1**, dynamic memory device **101** also comprises data terminal **120** and optional terminal **116**. Memory array **110** comprises a multitude of storage elements **111** and data accessing means **118**. Data accessing means **118** is provided to write, read and update data which is stored in storage elements **111**. Data accessing means **118** is connected to storage elements **111** and to data terminal **120**.

A physical group of storage elements **111** in memory array **110** is referred to as block **113**. Blocks **113** are logically designated by A_1, A_i . . . A_n. In memory array **110**, the number of blocks **113** is n. Block addresses a_1, a_i . . . a_n are logically assigned to blocks A_1, A_i . . . A_n. There is one block address a_i for one block A_i.

Outputs **117** of decoder **114** are connected to storage elements **111** of corresponding blocks **113**. Address generator **112** is connected to decoder **114** and generates block addresses **119** (a_1, a_i . . . a_n) corresponding to blocks **113** (A_1, A_i . . . A_n).

Dynamic memory device **101** can be connected to other components via data terminal **120** or optional terminal **116**.

Optional terminal **116** can provide control signal **121** for address generator **112**. For example, control signal **121** can be a clock signal.

In one refresh cycle, address generator **112** generates block addresses **119** (a_1, a_i . . . a_n) for all blocks **113** (A_1, A_i . . . A_n) of memory array **110**. Block addresses a_1, a_i . . . a_n can have, for example, ascending or descending values. Block addresses a_1, a_i . . . a_n are supplied to decoder **114**. Decoder **114** sends refresh signals **115** to corresponding blocks **113** on memory array **110**. Upon receiving refresh signal **115** the information of all storage elements **111** of one block **113** is updated by data accessing means **118**, thus each block **113** is refreshed. At the end of each refresh cycle, address generator **112** resets automatically and the cycle can start again when a clock signal is available. The clock signal can be supplied as control signal **121** via optional terminal **116**. It can also be generated by address generator **112** itself.

It is frequently the case with a DRAM, that data is stored in an array comprising memory cells which are arranged for example in rows. In such a case the memory cells correspond to storage elements **111**, the rows to blocks **113**, a counter to address generator **112**, a row decoder to decoder **114**, and data accessing means **118** comprises charge detection circuits for reading the information. Row addresses are generated in the counter and supplied to the row decoder. The row decoder is connected to each row via outputs **117**. The signals at the outputs of the row decoder are the above mentioned refresh signals **115**. When refresh signal **115** is applied to a particular row, the information of every single memory cell of that particular row is read and the capacitor of that memory cell is recharged if required, thus that row is refreshed.

For convenience of explanation and not intended to be limiting the following example is given:

In a DRAM having an array of 1024×1024 memory cells for storing 1 Mbit data, the memory cells are arranged in 1024 rows designated as A_1 . . . A_{1024}. The row decoder is connected to each row and supplies above mentioned refresh signals **115** to the rows. The counter produces increasing addresses a_i which are integer numbers from a_1=1 to a_{1024}=1024. When, for example, the address a_{256}=256 is supplied to the input of the row decoder then all 1024 memory cells of row A_{256} are refreshed one after another. The charge of each memory cell is detected by a charge detection circuit which is part of data accessing means **118**. If the memory cell is charged, than it is recharged. That means that all memory cells with charged capacitors (e.g., representing the bit "1") are recharged, and these with uncharged capacitors (e.g., representing the bit "0") are not recharged.

A DRAM usually also includes data accessing means **118** to read the information of each memory cell. Additional addresses such as, for example, column addresses are required to access each memory cell. That additional addresses can be supplied via data terminal **120**.

In dynamic memory device **101** of FIG. **1**, all blocks **113** of memory array **110** are refreshed in every refresh cycle, thus consuming energy.

The invention provides an improved refresh circuit for dynamic memory devices and a method for refreshing such devices that reduces or overcomes the above mentioned problems of prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a schematic diagram of a dynamic memory device as known in prior art; and

FIG. **2** shows a schematic diagram of a dynamic memory device with modified refresh circuit according to a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **2** shows a schematic diagram of dynamic memory device **201** with modified refresh circuit **230** according to a preferred embodiment of the invention.

As in the prior art, dynamic memory device **201** comprises memory array **210**, address generator **212** and decoder **214**. Additionally, dynamic memory device **201** comprises reference register **222** or other storage means and control logic **224**. Dynamic memory device **201** also comprises data terminal **220** and optional terminals **216**, **226**, **236**.

The combination of address generator **212** and decoder **214** is referred to as signal provider **260**. The combination of reference register **222** and control logic **224** is referred to as signal controller **270**. Signal provider **260** and signal controller **270** form refresh circuit **230**.

As in the prior art, memory array **210** comprises a multitude of storage elements **211** and data accessing means **218**. Data accessing means **218** is provided to write, read and update data which is stored in storage elements **211**. Data accessing means **218** is connected to storage elements **211** and to data terminal **220**. Optional terminal **216** can provide control signal **221** for address generator **212**. For example, control signal **221** can be a clock signal.

A physical group of storage elements **211** in memory array **210** is referred to as block **213**. Each block **213** is logically designated by $A_1, A_i \ldots A_n$. In memory array **210**, the number of blocks **213** is n. Block addresses **219** $a_1, a_i \ldots a_n$ are logically assigned to blocks $A_1, A_i \ldots A_n$. There is one address a_i for one block A_i. Outputs **217** of decoder **214** are connected to storage elements **211** of corresponding blocks **213**.

In FIG. **1** and FIG. **2** the reference numbers **101/201**, **110/210**, **111/211**, **112/212**, **113/213**, **114/214**, **115/215**, **116/216**, **117/217**, **118/218**, **119/219**, **120/220**, **121/221**, **130/230** stand for analogous components or signals. However, their operation or function is different as a consequence of the embodiment which will be explained in detail referring to FIG. **2**.

Reference register **222** is used to store a reference address a_r. In FIG. **2**, reference address a_r is indicated by number **223**. The reference address a_r can be provided to reference register **222** by optional terminal **226**. Control logic **224** is connected at input **227** to address generator **212** and at input **229** to reference register **222**. Decoder **214** is equipped with ENABLE-input **234** connected to output **225** of control logic **224**. Optional link **250** can be provided between memory array **210** and reference register **222**. Optional terminal **236** can be provided for feeding signals to control logic **224**.

Address generator **212** continually supplies block addresses **219** ($a_1, a_i \ldots a_n$) to decoder **214**.

The constant reference address a_r appears at input **229** of control logic **224**. At input **227** of control logic **224** an address a_i of the changing addresses $a_1, a_i \ldots a_n$ from address generator **212** is present. Control logic **224** compares this address a_i with the reference address a_r and switches decoder **214** ON and OFF according to a logical function $f(a_i, a_r)$ implemented in control logic **224**. The logical function $f(a_i, a_r)$ can be expressed by terms such as greater or smaller than, odd or even, modulo, etc. In that way, decoder **214** sends refresh signals **215** to memory array **210** only when it is enabled by control logic **224** at ENABLE-input **234**.

The reference address a_r or information to produce it can be supplied to reference register **222** via optional terminal **226** or it can be stored internally. The logical function can be implemented in control logic **224**, but any means for supplying the logical function $f(a_i, a_r)$ to control logic **224** can also be used. For example, the logical function $f(a_i, a_r)$ can be supplied to control logic **224** via optional terminal **236** or it can be supplied via optional terminal **226** or optional terminal **216** or a combination thereof, or it can be stored within dynamic memory device **201**.

In the preferred embodiment for a DRAM, control logic **224** is a comparator. For example, control logic **224** enables decoder **214** for $a_i<a_r$ and for $a_i=a_r$. It disables decoder **214** for $a_i>a_r$. For example, assume there are n=1024 rows from A_1 to A_{1024} which have addresses from a_1=1 to a_{1024}=1024, and that reference register **222** has the value of $a_r=a_{512}$=512. Address generator **212** generates addresses a_i which are in this example numbers from 1 to 1024 and returns to 1. When these addresses are smaller or equal to 512 than decoder **214** is enabled and rows A_1 to A_{512} are refreshed. Then address generator **212** counts further from 513 to 1024, but decoder **214** is disabled and rows $A_{513}, A_{514} \ldots A_{1024}$ are not refreshed. In that example, refreshed rows $A_1, A_2 \ldots A_{512}$ are contiguous. This is convenient but not essential. Rows $A_{513}, A_{514} \ldots A_{1024}$ which are not refreshed can also be contiguous.

In another example for a DRAM, control logic **224** has a different logical function $f(a_i, a_r)$. For example, when a_r=1, control logic **224** can enable decoder **214** for even block addresses a_i and disable decoder for odd block addresses a_i. For a_r=0, control logic **224** can always enable decoder **214**, independently of whether block address a_i is even or odd. In that case a_r can have only one bit.

In all cases, the operation of address generator **212** with the generation of all block addresses $a_1, a_i \ldots a_n$ in one cycle can be the same as in prior art. Address generator **212** and reference register **222** are independent. The number of blocks **213** in memory array **210** to be refreshed depends only on the reference address a_r of reference register **222** and of the logical function $f(a_i, a_r)$ which commands control logic **224**.

In comparison to the prior art, where all blocks **113** and therefore all storage elements **111** are refreshed, the present invention of FIG. **2** allows one to divide the total number of storage elements **211** into two sets: a first set of storage elements **211** to be refreshed, and a second set of storage elements **211** not to be refreshed. The term "set" is also applicable to blocks **213**: storage elements **211** of the first set of blocks **213** are to be refreshed, and storage elements **211** of the second set of blocks **213** are not to be refreshed. In other words, refresh circuit **130** of prior art allows only full refresh of an array; and refresh circuit **230** of the present invention allows not only full but also partial refresh of an memory array of storage elements. It is also included in the present invention that reference address a_r and logical function $f(a_i, a_r)$ can be supplied from outside dynamic memory device **201**.

When a system which uses dynamic memory device **201** requires full memory capacity, reference register **222** can be set to a certain value a_{r0}, preferably equal to but not excluding the lowest address a_1 or the highest address a_n of address generator **212**. Then, memory array **210** can store the maximum amount of data because it will be refreshed completely on each refresh cycle. The above mentioned first set contains all blocks **213** and the second set is empty.

The present invention is not limited merely to the use of one address generator **212**, reference register **222** or control logic **224**. Additional units can be used and combined in order to specify blocks **213** to be refreshed more flexibly.

This is especially important if dynamic memory device **201** is a Content Addressable Memory in which the blocks to be refreshed need to be controlled by the system in which dynamic memory device **201** is used.

By optimizing refresh circuit **230** it can be guaranteed that critical data is stored even if a reference register **222** fails. Memory array **210** is refreshed completely and failure of reference register **222** only influences the power consumption and not the security of data, thus providing fail-safe operation.

The reference address a_r as well as the logical function $f(a_i, a_r)$ and therefore blocks **213** to be refreshed can be determined by software and adjusted to the requirements of the system and of each application.

In a further embodiment of the invention, reference register **222** can be set to a certain value $a_{r\,fix}$. That value can not be changed from outside dynamic memory device **201**. In such a configuration, control signal **237** is provided at optional terminal **236**. Depending on control signal **237** memory array **210** is refreshed fully or only partially refreshed.

In a still further embodiment of the invention, reference register **222** is coupled by optional link **250** directly to data accessing means **218**. The reference address a_r is part of the data stored in the DRAM.

Applications for the inventions can be found for a wide range of battery powered portable systems, as for example, lap top computers, portable computer games, cellular telephones, pagers, hearing aides, etc.

The above mentioned communication and other systems often operate for a significant period of time in standby mode when only a certain amount of data needs to be stored. When activated to full operation, the system requires full memory capacity available within very short time. The present invention makes such operation possible without use of static memory.

The applications are not limited to such systems. There are many other stationary and remote systems where the power source is difficult to maintain or even impossible to replace as, for example, in solar or wind powered transmitters, remote earthquake or temperature sensors, emergency beacons, and in satellites. For example, reducing size and power consumption of an implantable medical device has an appreciable advantage for the patient, since the battery needs to be exchanged less often or not at all. With further reduction of energy consumption, dynamic memory devices can be used in applications from which they had been previously excluded.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art based on the teachings herein without departing from the scope of the present invention.

The space which the hardware of the inventive refresh circuit requires is very small compared to the other elements. As the improved hardware is compatible with existing software, there is no need to modify software at the same time as introducing the present invention. Compared to the prior art solution of combining static and dynamic devices, the use of expensive hardware such as for static memory devices can be significantly reduced or avoided, thus increasing reliability and cost saving.

I claim:

1. A dynamic memory device comprising:

(a) a plurality of storage elements;

(b) a signal provider for sending refresh signals to said storage elements and for providing addresses of substantially all storage elements; and

(c) a programmable signal controller coupled to said signal provider for receiving said addresses and for comparing magnitudes of said addresses to a magnitude of a reference address, said programmable signal controller for controlling said signal provider so that, during a particular refresh cycle in which addresses for substantially all storage elements are generated, only a first sub-set of storage elements with addresses in a first magnitude relation to said reference address are refreshed and a second sub-set of storage elements with addresses in a second magnitude relation to said reference address are not refreshed.

2. A dynamic memory device comprising:

(a) a plurality of storage elements;

(b) a signal provider for sending refresh signals to said storage elements; and

(c) a programmable signal controller coupled to said signal provider for controlling said signal provider so that, during a particular refresh cycle, only a first sub-set of storage elements are refreshed and a second sub-set of storage elements are not refreshed, said signal provider having

(i) an address generator for providing addresses for said storage elements; and

(ii) a decoder for receiving said addresses from said address generator and, in response to a control signal received from said signal controller, sending refresh signals to said first sub-set of storage elements but not to said second sub-set of storage elements,

said signal controller having a reference register for storing a reference address and control logic coupled to said reference register, to said address generator, and to said decoder, wherein said control logic uses said addresses generated by said address generator and said reference address to determine which storage elements are in said first sub-set and which storage elements are in said second sub-set.

3. The dynamic memory device of claim **2** wherein the reference address is supplied to said reference register by an external terminal.

4. The dynamic memory device of claim **2** wherein said control logic is controllable by a signal applied to an external terminal.

5. A method for the refresh of dynamic memory devices having a plurality of rows with storage elements, comprising the steps of:

a) storing a reference address;

b) generating an address for one of said rows;

c) relating said row address and said reference address by a logical function, thereby determining if a magnitude of said row address belongs to a first sub-set or a second sub-set of magnitudes of row addresses;

d) sending refresh signals to said row only if said row address belongs to said first sub-set; and

e) repeating said steps b) to d) for substantially all rows.

6. A memory comprising:

an array of rows;

a generator which continuously generates row addresses; and

a filter coupled between said generator and said array, said filter consecutively relating substantially all of said row addresses to a reference address and depending on a

comparison between said reference address and said row addresses sending refresh signals to some of said rows and not sending refresh signals to the other rows.

7. A memory comprising:

an array of rows;

a generator which continuously generates row addresses; and

a filter coupled between said generator and said array, said filter consecutively relating substantially all of said row addresses to a reference address and sending refresh signals to some of said rows and not sending refresh signals to the other rows said filter having

(a) a decoder receiving said row addresses and sending refresh signals, and

(b) a comparator receiving said reference address once and said row addresses consecutively, said comparator enabling said decoder or disabling said decoder.

8. An apparatus comprising:

a plurality of n blocks A_i (i=1 to n), each block A_i being accessible by a single address a_i;

a generator which in a single refresh cycle provides addresses a_i from i=1 to i=n in any order;

a register for storing a reference address; and

a comparator

receiving an address a_i;

every time said comparator has received an address a_i, comparing said address a_i with said reference address, and

every time said comparator has compared, selectively forwarding said address a_i to A_i so that a refresh operation is executed in some of said n blocks, but not in all blocks A_i.

9. The apparatus of claim **8** wherein said reference address is constant during a single refresh cycle.

10. The apparatus of claim **8** wherein said reference address is provided from an external terminal.

11. A dynamic memory comprising:

a plurality of n rows A_i (i=1 to i=n) each having storage cells;

a generator which cyclically generates addresses a_i for i=1 to i=n;

a decoder receiving one address a_i at a time, said decoder being either enabled or disabled, said decoder when enabled sending a refresh signal to said storage cells of row A_i which is identified by said address a_i; and

a control logic cyclically receiving addresses a_i, and enabling or disabling said decoder depending on a logical relation between and a reference address a_r.

12. A dynamic memory comprising:

a plurality of n rows A_i (i=1 to i=n) each having storage cells;

a generator which cyclically generates addresses a_i for i=1 to i=n;

a decoder receiving one address a_i at a time, said decoder being either enabled or disabled, said decoder when enabled sending a refresh signal to said storage cells of row A_i which is identified by said address a_i; and

a control logic cyclically receiving addresses a_i and enabling or disabling said decoder depending on a logical relation between a_i and a reference address a_i, said control logic enabling the decoder for $a_i<a_r$ and $a_i=a_r$ and disabling said decoder for $a_i>a_r$ wherein r is a predetermined integer between from 0 to n.

13. The dynamic memory of claim **11** which receives said reference address from an external terminal.

* * * * *

EXHIBIT B

US006127875A

United States Patent [19]

Allen et al.

[11] **Patent Number: 6,127,875**

[45] **Date of Patent: Oct. 3, 2000**

[54] **COMPLIMENTARY DOUBLE PUMPING VOLTAGE BOOST CONVERTER**

[75] Inventors: **Steven Peter Allen**, Mesa; **Ahmad H. Atriss**, Chandler; **Gerald Lee Walcott**, Mesa; **Walter C. Seelbach**, Fountain Hills, all of Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **09/130,343**

[22] Filed: **Aug. 13, 1998**

[51] **Int. Cl.**[7] **H03L 5/00**

[52] **U.S. Cl.** **327/306**; 327/536; 327/537; 327/589

[58] **Field of Search** 327/534, 536, 327/530, 537, 390, 306, 331, 589; 365/185.23

[56] **References Cited**

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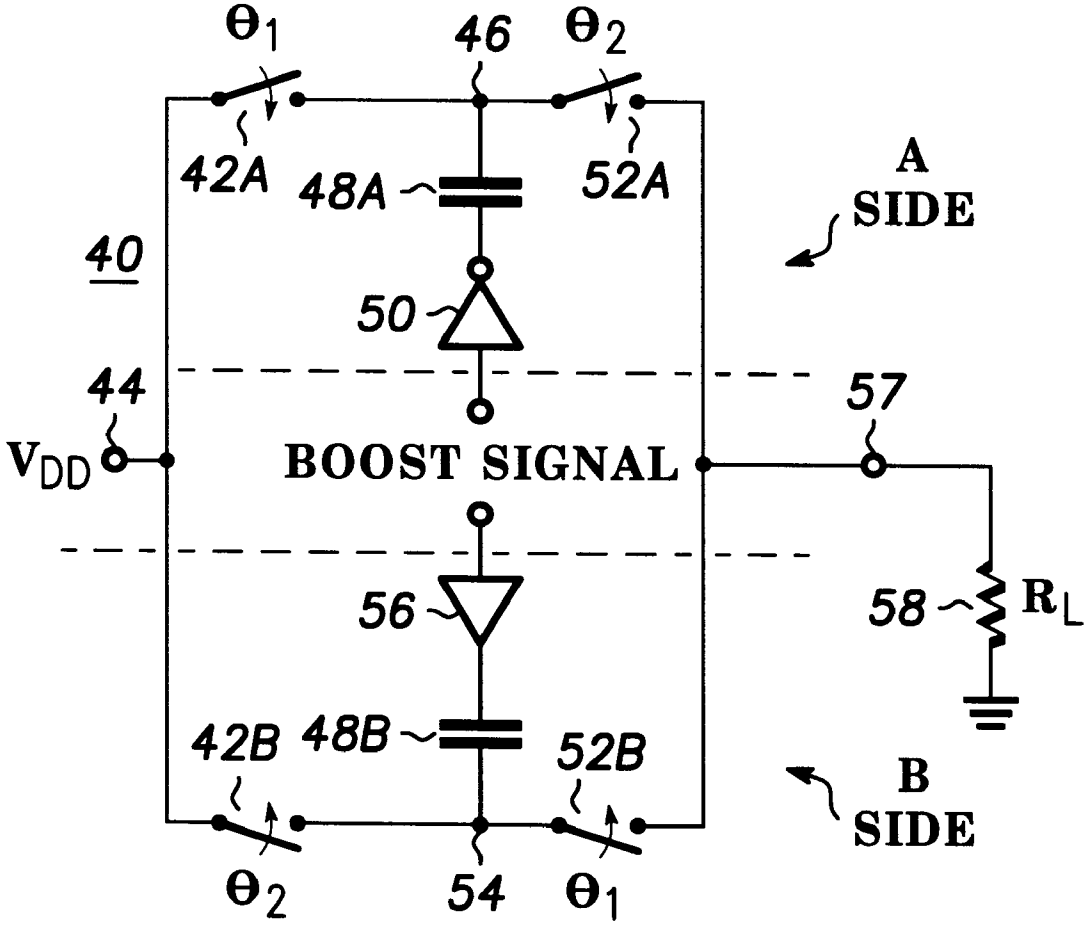
Primary Examiner—Tuan T. Lam
Assistant Examiner—Hiep Nguyen
Attorney, Agent, or Firm—Lanny L. Parker; A. Kate Huffman

[57] **ABSTRACT**

A voltage boosting circuit which derives an output voltage than is substantially twice the magnitude of a supply voltage applied thereto. The voltage boosting circuit consists of complementary acting boost circuits each having a pair of switches (**42**A, **52**A; **42**B, **52**B) connected between an input of the voltage boosting circuit, at which is applied the supply voltage, and an output at which the output voltage is produced. Boost capacitors (**48**A, **48**B) are connected between the respective switches of the complementary boost circuits and the switches of the these circuits are opened and closed out of phase with respect to each other in response to clocking signals being applied thereto such that a boosted output voltage is produced during each half cycle of the clocking signals.

3 Claims, 2 Drawing Sheets



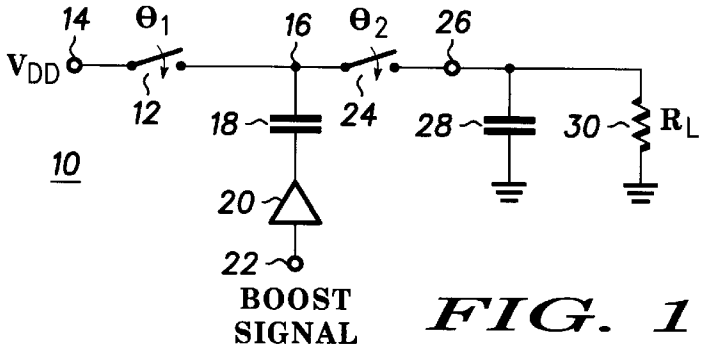


FIG. 1

- PRIOR ART -

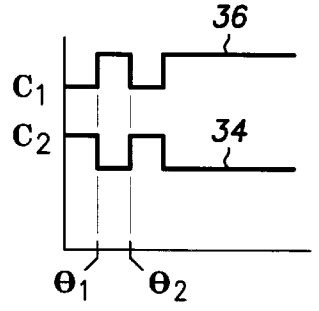


FIG. 2A

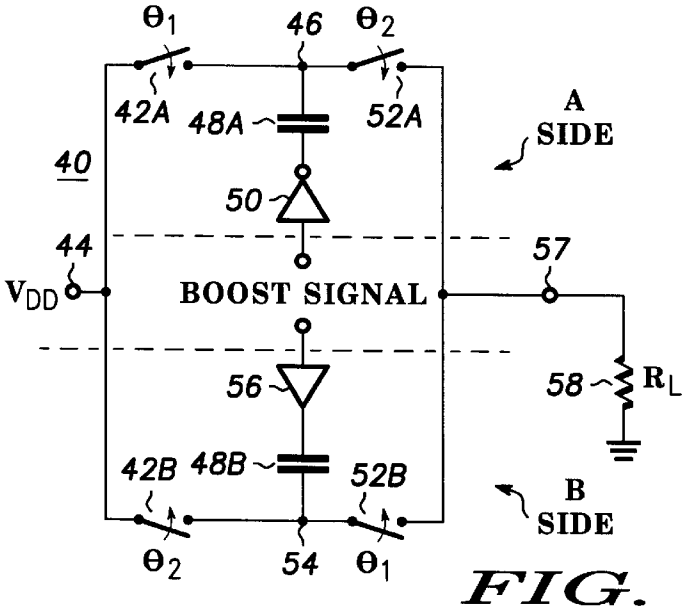


FIG. 3

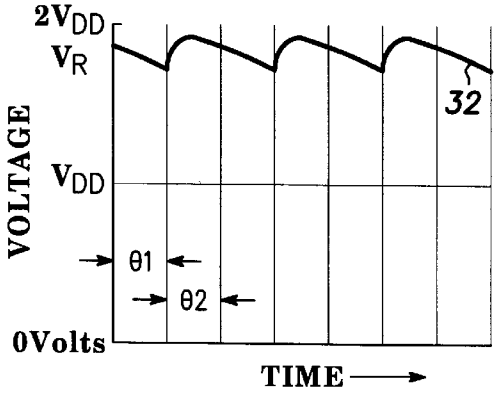


FIG. 2

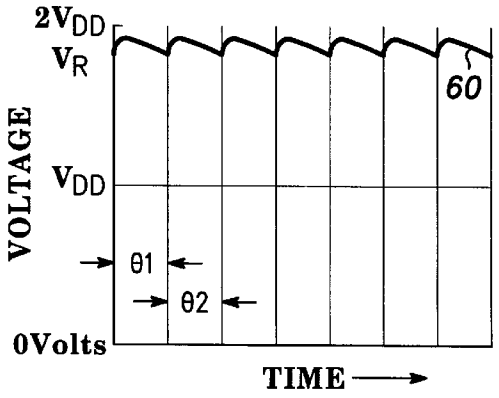


FIG. 4

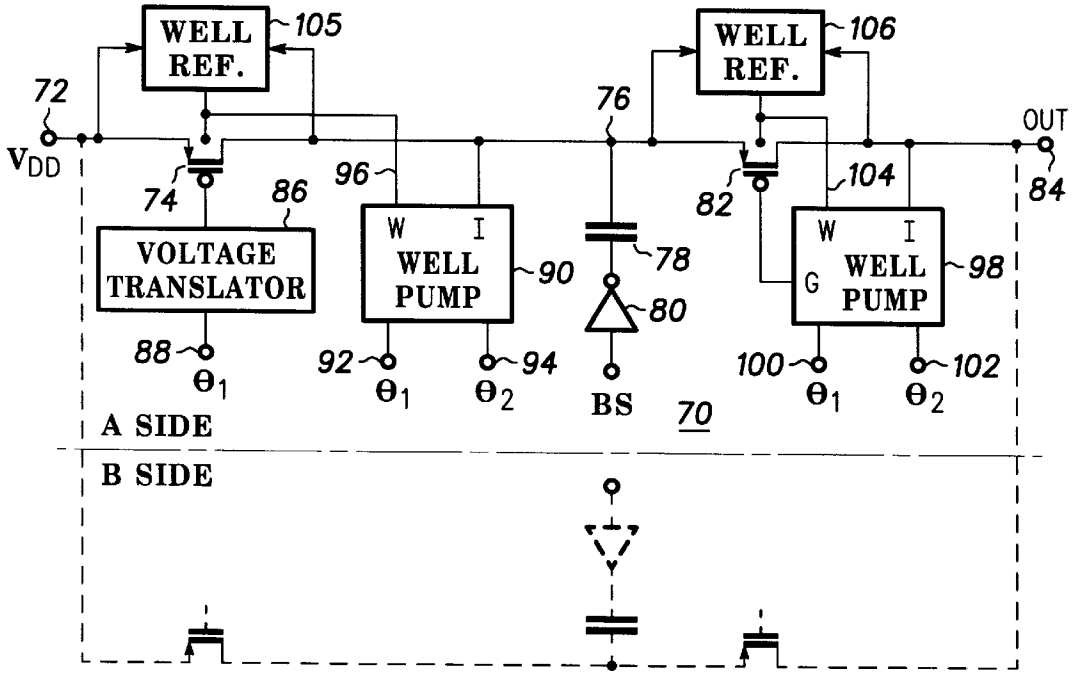


FIG. 5

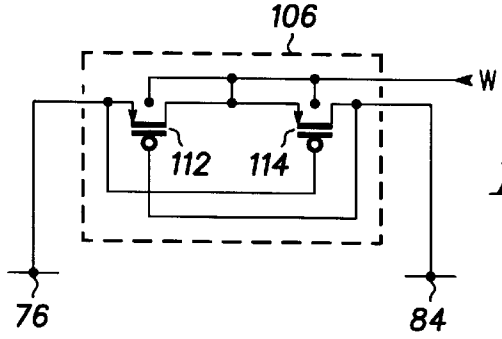


FIG. 6

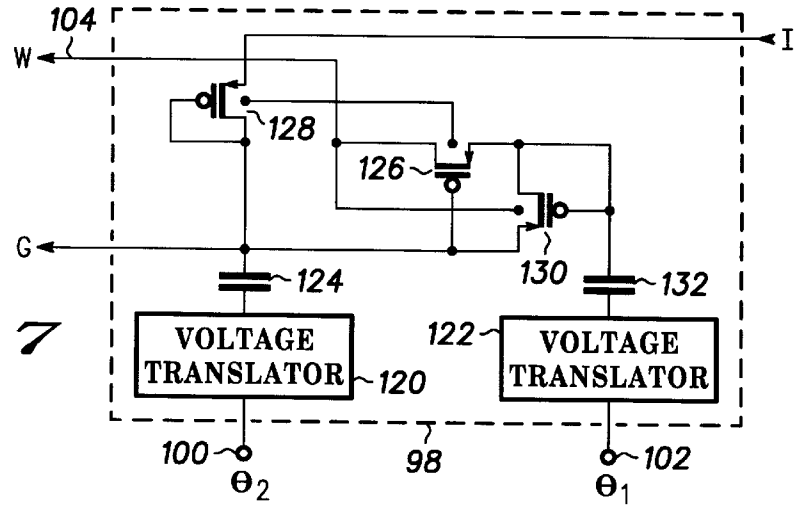


FIG. 7

COMPLIMENTARY DOUBLE PUMPING VOLTAGE BOOST CONVERTER

BACKGROUND OF THE INVENTION

The present invention relates to voltage boosting converters and, more particularly to a double pumping voltage boosting circuit for providing an output voltage greater than a supplied input voltage and which is suited to be manufactured in integrated circuit form.

The evolution of integrated circuit technology has provided for ever smaller device geometry's with lower operating supply voltages. The lower supply voltage has resulted in advantages and disadvantages with the primary advantage being a significant reduction in power consumption. A significant disadvantage is the inability of some of the more complex functions to operate at the lower supply voltage. To facilitate these functions, a localized voltage boosting circuit is needed to supply an increased operating voltage. The voltage boosting circuit should be efficient in terms of power consumption, component count and die area while delivering an increased supply voltage with minimal amounts of ripple or distortion.

A basic voltage boosting circuit **10**, that is well understood in the art, is illustrated in FIGS. **1**, **2**, and **2**A. Circuit **10** uses two switches **12** and **24** for controlling the current flow and two capacitors **18** and **28** for boosting and storing an output voltage applied across a load resistor **30** which is derived from a supply voltage V_{DD} supplied at an input **14**. The circuit operation begins by first referencing the boosting capacitor **18** to the supply voltage and ground reference potential by having switch **12** closed during the first half cycle, η_1, in response to a pair of non-overlapping clock signals C**1** and C**2**, which are 180 degrees out of phase with respect to one another, while the output of buffer **20** is in a low voltage level state due to a boost signal applied thereto. This connects the top of capacitor **18** to V_{DD} while the bottom is at ground reference potential. In the second half cycle, Θ_2, switch **12** opens and buffer driver output drives from a low voltage level state to a high voltage level state boosting the potential at the top of capacitor **18** to substantially twice the supply voltage V_{DD}. Simultaneously, switch **24** closes so that the boosted charge on capacitor **18** can be distributed between itself and storing load capacitor **28**. The resulting output voltage V_R, depicted in FIG. **2**, shows the boosted voltage on capacitor **28** decaying as current is delivered in the load R_L, during the first half of the clock cycle, Θ_1. During the second half of the clock cycle, Θ_2, the output voltage first builds toward $2V_{DD}$, due to the boosted charge on capacitor **18** being redistributed across capacitors **18** and **28**, and then decays as current is delivered to the load. The resulting output voltage contains a significant amount of distortion due to the discrete charge and decay times. Furthermore, it typically takes 1600 pF of capacitance for both capacitors to deliver 1.2 ma of current while boosting the voltage from 0.9 volts to 1.4 volts, at a 10 MHz clock rate.

Hence, a need exists for an improved voltage boosting circuit suitable for fabrication in integrated circuit form for boosting a supply voltage while requiring less capacitance and output voltage distortion than known prior art voltage boosting circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a prior art voltage boosting circuit;

FIG. **2** shows the output voltage produced by the prior art circuit of FIG. **1**;

FIG. **2**A shows the clocking signals useful for explaining the operation of the present invention;

FIG. **3** is a schematic diagram of one embodiment of the present invention;

FIG. **4** shows the output voltage produced by the embodiment of the present invention;

FIG. **5** is a partial block and schematic diagram of the voltage boosting circuit of the present invention shown in FIG. **3**;

FIG. **6** is a schematic diagram of the well reference circuit shown in FIG. **5**; and

FIG. **7** is a schematic diagram illustrating a well pump circuit disclosed in FIG. **5**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now to FIG. **3** there is shown double pumping voltage boosting converter **40** of the preferred embodiment of the present invention. Voltage boosting circuit **40** comprises an A side voltage boost circuit portion similar to the prior art circuit of FIG. **1** and a complementary (B side) voltage boost circuit portion. Thus, the complementary pumping architecture of FIG. **3** includes first switches **42**A and **42**B connecting a supply voltage V_{DD}, applied to terminal **44**, to respective terminals **46** and **54** when the switches are closed and disconnecting terminal **44** from terminals **46** and **54** when opened. The A side circuit portion further includes capacitive device **48**A connected between terminal **46** and the output of inverting buffer driver **50**. Likewise, B side circuit portion includes capacitive device **48**B coupled between terminal **54** and non-inverting buffer driver **56**. Terminals **46** and **54** are coupled respectively via a pair of switches **52**A and **52**B to output **57** of voltage boosting circuit **40** which is, in turn, connected to load device **58**, shown here as a resistor R_L. A voltage boost signal is applied to the inputs of buffer drivers **50** and **56**.

Thus, in operation, during the first half cycle, Θ_1, of the clocking signals **34** and **36**, switches **42**A and **52**B are closed while switches **42**B and **52**A are opened. If it is assumed that the capacitive device **48**B has been charged to V_{DD} during a previous half cycle, and at the same time switch **52**B is closed, the boost signal is in a high level state, as previously described, the voltage across capacitive device **48**B will be boosted to nearly $2V_{DD}$ as illustrated in FIG. **4**, to drive into load **58**. As current flows in load **58** the charge across capacitive device **56** begins to decrease but to a much less degree than for prior art circuit **10**. Simultaneously, the boost signal applied to inverting buffer **50** is driving its output to a low level state, is referencing capacitive device **48**A between V_{DD} and ground potential as switch **42**A is closed while terminals **46** and **54** are disconnected from output terminal **57** and input terminal **44** respectively as the switches are open. Thus, as capacitive device **48**B is delivering the boosted voltage into load **58**, capacitive device **48**A is being charged to V_{DD}. Conversely, during the second half cycle, Θ_2, switches **42**B and **52**A are closed while switches **42**A and **52**B are opened. Boost signal also changes states from a high level to a low level. Hence, the A side of voltage boosting circuit **40** drives load **58** with a voltage nearly equal to $2V_{DD}$ as the voltage across capacitive device **48**A is boosted to the higher voltage level while V_{DD} is applied across capacitive device **48**B. Thus, during initiation of both half cycles Θ_1 and Θ_2, as illustrated in FIG. **4**, the voltage drive into load **58** is raised to nearly $2V_{DD}$.

The output voltage V_R, wave form **60**, is shown to have much less distortion as boost capacitors **48**A and **48**B deliver

charge into load **58** during both phases of the clocking pulses which reducing the discharge time that V_R decreases which is a significant advantage over the prior art. Additionally, the need for an added load capacitance, capacitor **28**, is eliminated by voltage boosting circuit **40** since either capacitive device **48**A or capacitive device **48**B is driving load **58** at all times. Hence, not only is the need for one capacitive device eliminated by the present invention but the individual capacitance value of the two driving capacitive devices thereof are significantly reduced. Therefore, the die area needed for fabricating voltage boosting circuit **40** in integrated circuit form compared to circuit **10** is significantly reduced.

In one example, a voltage boosting circuit of the present architecture has been found to use 400 pF of capacitance for capacitive devices **48**A and **48**B to deliver 1.2 ma of current to a load while boosting the voltage applied thereto from 0.9 volts to 1.4 volts, at a 10 Mhz clock rate while reducing the output voltage distortion when compared to the voltage boost circuit of the prior art. The prior art boost circuit required 3200 pF of capacitance to achieve the same performance. This represents a significant savings in die area.

Turning now to the remaining figures, the voltage boosting circuit architecture of the present invention is shown in more detail. For brevity, FIG. **5** illustrates only the A side portion **70** of the voltage boosting circuit **40** described in FIG. **3**, it being understood that the B side portion is identical thereto.

Switches **42**A, **52**A (as well as **42**B and **52**B) are illustrated as being realized by PMOS transistors. PMOS transistor **74**, switch **42**A, is shown as having its source electrode coupled to input **72** to which is applied supply voltage while its drain is coupled to terminal **76** at one side of capacitor **78**. The other side of capacitor **78** is coupled to the output of inverting buffer driver **80** the latter of which has an input to which the boost signal is applied. Switch **52**A is shown as being realized by PMOS transistor **82** having its source electrode coupled to terminal **76** and its drain electrode coupled to output **84**. Output **84** would be connected a to load which, not shown, would be similar to load **58** of FIG. **3**. A voltage translator **86** which has an input **88** for receiving the clock pulse C**1** provides a translated voltage, as is understood to those skilled in the art, to drive the gate electrode of transistor **74** such that the gate potential is of sufficient magnitude to insure that the transistor remains off whenever its gate is driven high. Similarly, a voltage translator is provided, as will be discussed, for driving the gate electrode of transistor **82** in a complementary phase with respect to transistor **74**. All translators receive their supply voltage from the converter output, node **84**.

The switch transistors **74** and **82**, as well as the corresponding switch transistors (shown in phantom) of the B side portion of the voltage boosting circuit **40**, are floating well P-channel transistors who's well biasing is driven by pumping structures **90** and **98** respectively. The well pumping structures provide a continuous boosting drive at the W outputs thereof to each floating well of the switch transistors during every phase Θ_1 and Θ_2 of the clocking signals C**1** and C**2** applied at the inputs (**92**, **94**; **100**, **102**) so that the well is quickly boosted and maintained at a higher potential than the source or drain of the switch transistor. This is critical in preventing charge injection, particularly during start up of voltage boosting circuit **40**. In addition, clamping circuits or well reference circuits **105** and **106**, which are coupled between the drain and source of transistors **74** and **82**, prevent the wells of these floating well transistors from being boosted to too high of a potential at which gain degradation due to body effect may occur.

Turning to FIG. **6**, the clamping circuit **106** will be described, it being understood that clamping circuit **105** is substantially identical therewith. Clamping circuit **106** is illustrated as including a pair of floating well PMOS transistors **112** and **114** the floating wells of which are coupled to the well driving output of well pump **98**. The source electrode of transistor **112** is coupled at terminal **76** while its gate electrode is coupled with the drain electrode of transistor **114** at output **84**. Transistor **114** has its source electrode coupled to the drain electrode of transistor **112** and to the interconnected wells of the two transistors while its gate electrode is coupled at the source electrode of transistor **112** at terminal **76**. Clamping circuit **106** references the well potential of transistor **82** to within one threshold of the highest potential at either its source or drain. At start up, where the output voltage at node **84** is low and the voltage at the top of boost capacitor **78** is high, during the boost cycle, transistor **112** turns on whenever the potential of the well of transistor **82** exceeds the potential on capacitor **78** at node **76**. Conversely, when the output voltage at output **84** is high and boost capacitor **78** is driven low, transistor **114** turns on whenever well of transistor **82** exceeds one threshold of the output voltage. As a result, clamping circuit **106** or **105** keeps the well of the switch transistors **74** and **82** closely coupled to the highest potential of there surrounding nodes so that the highest possible gain of the respective switch transistor can be achieved without the possibility of incurring charge injection.

Turning now to FIG. **7**, well pumping circuit **98** will be described which provides a continuous boost drive to the well of switch transistor **82**. As shown, the pair of clocking signals (FIG. **1**A) are supplied to respective inputs **100** and **102** which drive voltage translators **120** and **122**. The outputs of the voltage translators **120** and **122** are coupled to the bottoms respectively of capacitors **124** and **132**. As illustrated, an output of voltage translator **120** is coupled through capacitor **124** to drive the gate of transistor **82**. Continuing, the top side of capacitor **124** is also coupled to the drain of transistor **128** the source of which is coupled to node **84** while its gate is connected to the drain thereof. The top side of capacitor **132** is connected to both the gate and drain of transistor **130** while the source of transistor **130** is connected both to the gate of transistor **126** and the top side of capacitor **124**. Transistor **126** is further shown as having its source connected to the drain of transistor **130** while its drain is connected to the floating well of switch transistor **82** and to the well of transistor **130**. Transistor **134** has its gate connected to its drain and to node **84**. The only difference between well pump circuit **98** and **90** is that the former has an output G connected to the gate of its related switch transistor while the latter does not since the gate of its related switch transistor **74** is driven directly by a separate voltage translator, **86**.

The well pumps **90** and **98** work by first having capacitor **124** being driven high from translator **120** for driving the gate of transistor **126** while capacitor **132** is driven low by translator **122**. Transistor **126** will thus be turned off while transistor **130** is turned on. This results in the potential at the top of capacitor **132** being driven to a voltage threshold below the potential at the top of capacitor **124**. Clock signals C**1** and C**2** then change phase during the next half cycle of operation resulting in capacitor **124** being driven low while capacitor **132** is driven high. Transistor **126** will thus be turned on while transistor **130** is turned off. With transistor **126** now on, the increased potential at the top of capacitor **132** is transferred across the source and drain of transistor **126** to the well of the respective switch transistor that is connected to the output W of the well pump circuit.

Hence, what has been described is a novel improved voltage boosting circuit for providing an output voltage that is substantially twice the magnitude of a supply voltage applied thereto. For localized voltage boosting the voltage boosting circuit disclosed herein provides maximum voltage boosting while requiring less total circuit capacitance and less output distortion than equivalent prior circuits.

What is claimed is:

1. A boost circuit having an input terminal and an output terminal, comprising:

a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;

a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;

a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and

a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.

2. The boost circuit of claim **1**, further including:

an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and

a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.

3. The boost circuit of claim **1**, further including:

a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and

a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal.

* * * * *

EXHIBIT C

US006917555B2

(12) **United States Patent**
Bedwell et al.

(10) **Patent No.: US 6,917,555 B2**
(45) **Date of Patent: Jul. 12, 2005**

(54) **INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR**

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(73) Assignee: **Freescale Semiconductor, Inc.**, Austin, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 92 days.

(21) Appl. No.: **10/675,005**

(22) Filed: **Sep. 30, 2003**

(65) **Prior Publication Data**

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(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/226**; 365/227
(58) **Field of Search** 365/226, 227; 326/121

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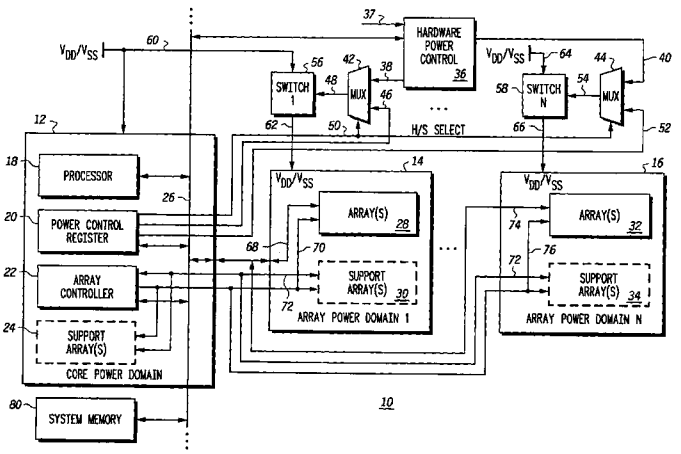
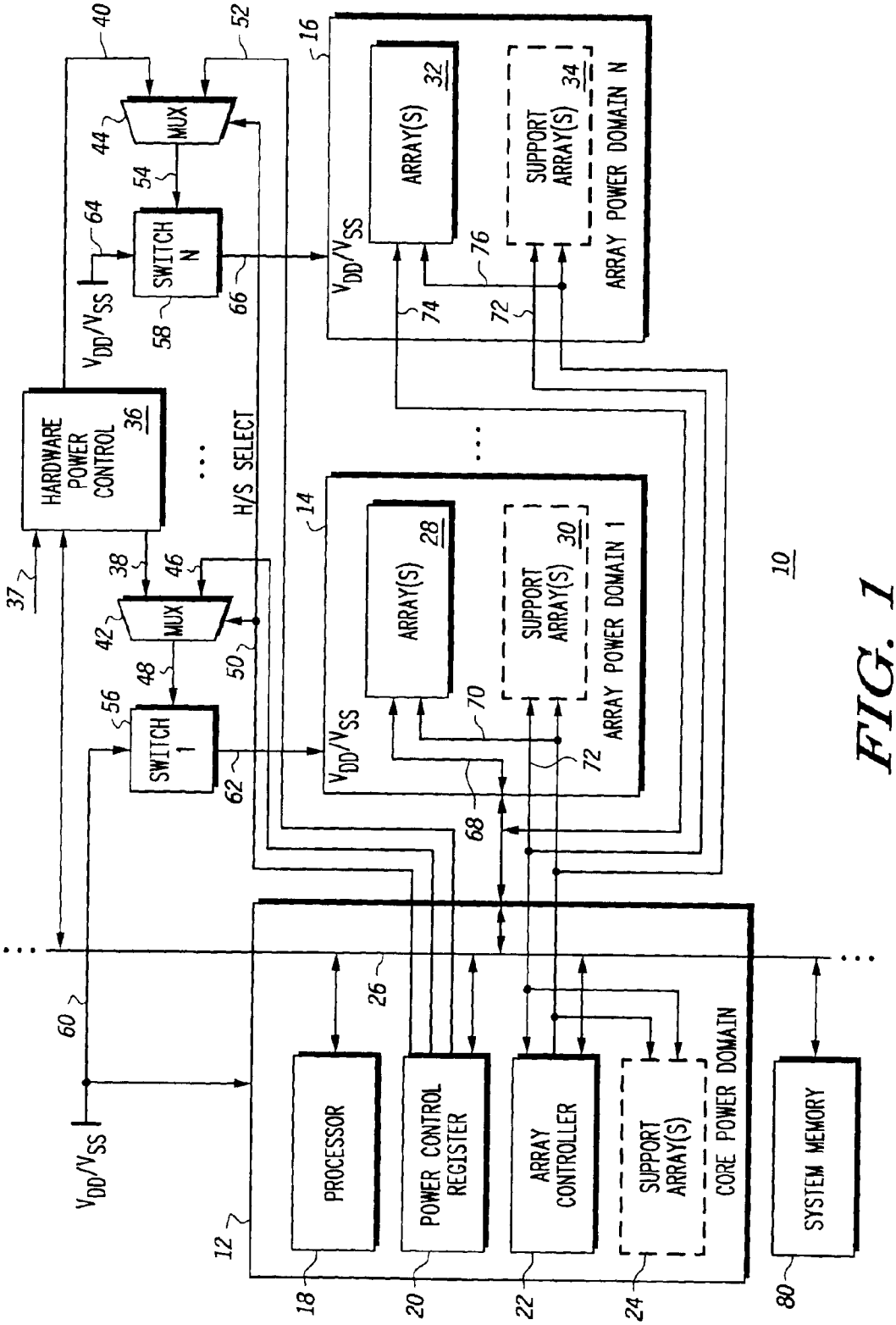
(74) *Attorney, Agent, or Firm*—Michael J. Balconi-Lamica

(57) **ABSTRACT**

Leakage current is eliminated in a memory array during a low power mode of a processing system having a processor that interfaces with the memory array. Because two power planes are created, the processor may continue executing instructions using a system memory while bypassing the memory array when the array is powered down. A switch selectively removes electrical connectivity to a supply voltage terminal in response to either processor-initiated control resulting from execution of an instruction or from a source originating in the system somewhere else than the processor. Upon restoration of power to the memory array, data may or may not need to be marked as unusable depending upon which of the two power planes supporting arrays to the memory array are located. Predetermined criteria may be used to control the timing of the restoration of power. Multiple arrays may be implemented to independently reduce leakage current.

26 Claims, 3 Drawing Sheets




HARDWARE POWER CONTROL
36
H/S SELECT
MUX
SWITCH N
SWITCH 1
ARRAY(S)
SUPPORT ARRAY(S)
ARRAY POWER DOMAIN N
ARRAY POWER DOMAIN 1
V_{DD}/V_{SS}
PROCESSOR
POWER CONTROL REGISTER
ARRAY CONTROLLER
SUPPORT ARRAY(S)
CORE POWER DOMAIN
SYSTEM MEMORY
10
12
14
16
18
20
22
24
26
28
30
32
34
36
37
38
40
42
44
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68
70
72
74
76
80

FIG. 1

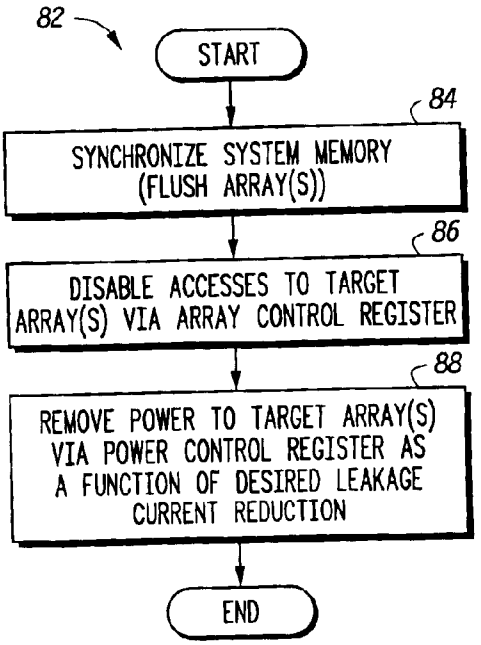


FIG. 2

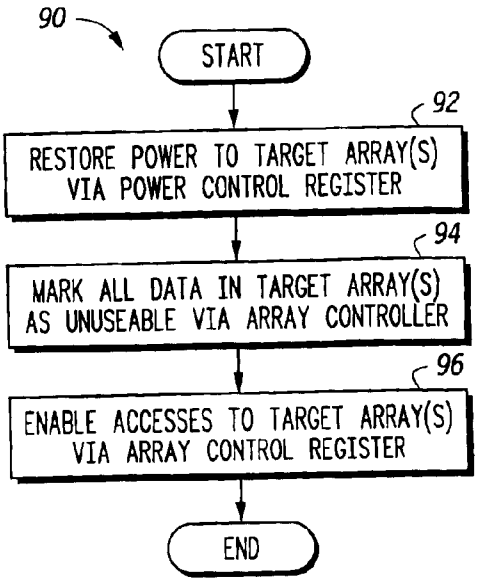


FIG. 3

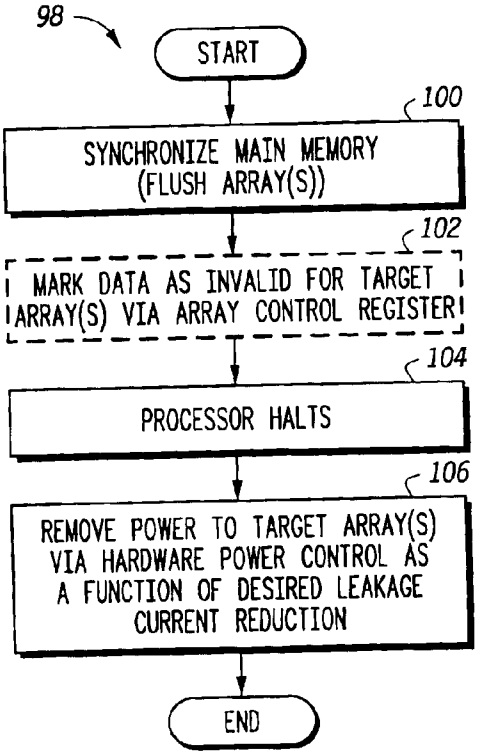


FIG. 4

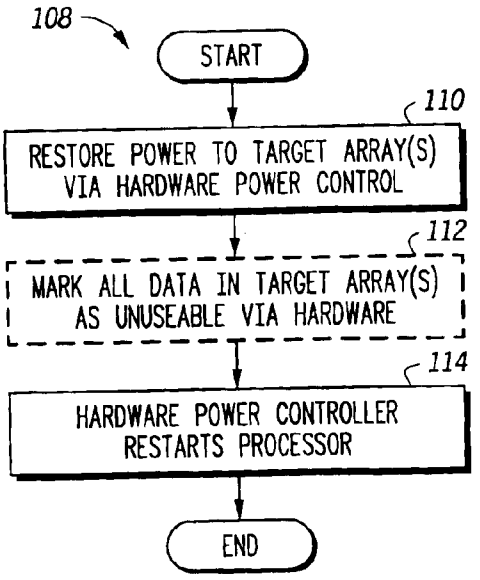


FIG. 5

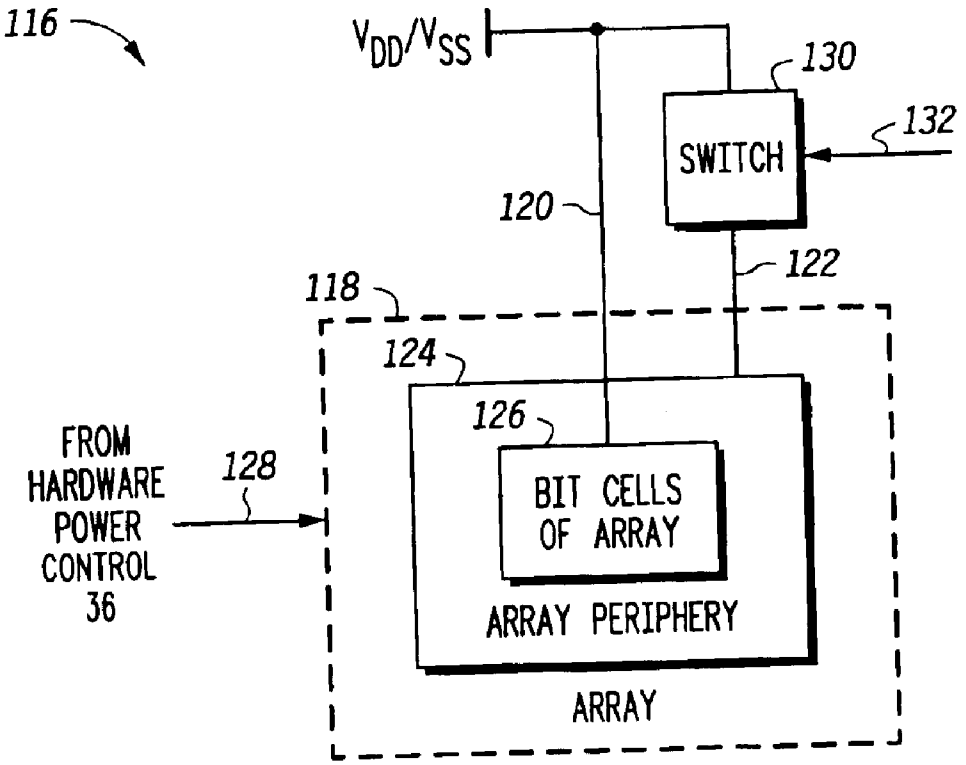

116
V_{DD}/V_{SS}
130
SWITCH
132
120
122
118
124
126
FROM HARDWARE POWER CONTROL 36
128
BIT CELLS OF ARRAY
ARRAY PERIPHERY
ARRAY

FIG. 6

INTEGRATED CIRCUIT POWER MANAGEMENT FOR REDUCING LEAKAGE CURRENT IN CIRCUIT ARRAYS AND METHOD THEREFOR

BACKGROUND

1. Field of the Invention

The present invention relates generally to integrated circuits and method of making the same, and more particularly, to integrated circuit power management for reducing leakage current in circuit arrays and method therefor.

2. Related Art

Battery-powered devices that incorporate integrated circuits, such as cell phones, personal digital assistants, handheld computing devices, and other similar type wireless and/or mobile electronic devices, are very sensitive to power consumption. As technology moves to the 90 nm process technology node and beyond, static leakage current within the integrated circuit of a battery-powered device becomes a major concern with respect to times when the device is powered but not actively used.

Accordingly, an improved integrated circuit and method of making the same is desired.

SUMMARY

According to one embodiment, an integrated circuit includes processing circuitry, at least one memory array, and control circuitry. The processing circuitry executes instructions. The at least one memory array couples to the processing circuitry for providing data to the processing circuitry. Lastly, the control circuitry couples to the at least one memory array, wherein the control circuitry removes electrical connectivity of the at least one memory array to a supply voltage terminal by firstly disabling all accesses to the at least one memory array and secondly removing electrical power to all of the at least one memory array to reduce leakage current in the at least one memory array.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the present disclosure are illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

FIG. **1** is a block diagram view of an integrated circuit with power management for reducing leakage current in circuit arrays according to an embodiment of the present disclosure;

FIG. **2** is a flow diagram view of an array(s) power-down sequence under software control according to another embodiment of the present disclosure;

FIG. **3** is a flow diagram view of an array(s) power-up sequence under software control according to the embodiment corresponding to FIG. **2**;

FIG. **4** is a flow diagram view of an array(s) power-down sequence under hardware control according to yet another embodiment of the present disclosure;

FIG. **5** is a flow diagram view of an array(s) power-up sequence under hardware control according to the embodiment corresponding to FIG. **4**; and

FIG. **6** is a block diagram view of a portion of the integrated circuit of FIG. **1** in greater detail according to yet another embodiment of the present disclosure.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve an understanding of the embodiments of the present disclosure.

DETAILED DESCRIPTION

Powering off of memory arrays of an integrated circuit during low-power modes according to the embodiments of the present disclosure can save significant leakage current. One example of an application of the present disclosure is the powering off of the data arrays of on-chip cache memories and other memory arrays. According to the embodiments of the present disclosure, powering off of memory arrays results in no loss of functionality. The powering off of memory arrays produces only some performance degradation. Performance degradation is due to one or more of the following: the need to flush the memory array prior to powering the memory array off; the need to ensure that all entries are invalid when the memory array is powered back up; and re-population of the memory array after power-up to a level similar to that before power-down.

The embodiments of the present disclosure include details for hardware and software requirements of methods for accomplishing a power-down sequence for a memory array, such as a cache memory array. The methods are equally applicable to any level of cache. However the methods differ in the point of control; one is software-controlled, the other is hardware-controlled. Furthermore, the methods can be simultaneously supported to allow a maximum flexibility.

In one embodiment, the method allows cache data arrays to be powered off during low-power modes or during long periods of extremely low processing requirements, inactivity, or limited inactivity. An example of an extremely low processing requirement for a device could include processing requirements for an idle cell phone. Uniqueness of the embodiments of the present disclosure resides partially in the fact that the cache arrays are powered off without having power to the corresponding processing core powered off, with the accompanying savings and restoring of states. In one embodiment, the method includes a whole-cache bypass and array power control using a single transistor. In one embodiment, the whole-cache power control provides for optimizing leakage reduction, with very little hardware overhead, and furthermore still allowing deterministic behavior by allowing explicit software control.

Referring now to FIG. **1**, the figure illustrates a block diagram view of an integrated circuit **10** with power management for reducing leakage current in circuit arrays according to an embodiment of the present disclosure. Integrated circuit **10** includes a core power domain **12** and one or more array power domains (**1** to N, where N is an integer), for example, as indicated in FIG. **1** by reference numerals **14** and **16**. The core power domain **12** includes processor (or processing circuitry) **18**, power control register **20**, and array controller **22**. Core power domain **12** may also include one or more support arrays **24**, for example, a tag array, a dirty array, a valid array, or combination(s) thereof. A system bus **26** couples processor **18**, power control register **20**, array controller **22**, and other system devices or functions, such as, hardware power control **36**, system memory **80**, or others (not shown).

Array power domain **14** includes one or more array(s) **28** and may also include one or more support array(s) **30**, for example, a tag array, a dirty array, a valid array, or combination(s) thereof. Array power domain **16** includes one or more array(s) **32** and may also include one or more

support array(s) **34**, for example, a tag array, a dirty array, a valid array, or combination(s) thereof.

Integrated circuit **10** further includes hardware power control **36**. Hardware power control **36** provides at least up to N hardware power control outputs, for example, hardware power control outputs **38** and **40**. Hardware power control **36** also includes a control input **37** configured to receive one or more power control signal(s).

In addition, integrated circuit **10** includes at least up to N power switch control multiplexers (MUXs), for example, MUX **42** and MUX **44**. In one embodiment, MUX **42** includes a 2:1 multiplexer having inputs **38** and **46** and an output **48**. A select input **50** driven by an output of power control register **20** controls which of the inputs **38** or **46** is passed to the MUX **42** output **48**. In one embodiment, input **38** corresponds to one output of hardware power control **36** and input **46** corresponds to one output of power control register **20**. MUX **44** includes a 2:1 multiplexer having inputs **40** and **52** and an output **54**. A select input **50** driven by an output of power control register **20** controls which of the inputs **40** or **52** is passed to the MUX **44** output **54**. In one embodiment, input **40** corresponds to another output of hardware power control **36** and input **52** corresponds to another output of power control register **20**.

Still further, integrated circuit **10** also includes at least up to N switches, for example, switch **56** and switch **58**. In one embodiment, switches **56** and **58** can comprise PFETs, NFETs, or other suitable transistor switching devices. Switch **56** has an input **60** and an output **62**, wherein connectivity from input to output is controlled by the output **48** of MUX **42**. Similarly, switch **58** has an input **64** and an output **66**, wherein connectivity from input to output is controlled by the output **54** of MUX **44**. A supply voltage terminal provides a voltage V_{DD} or V_{SS} to core power domain **12** and to the N switches, for example, corresponding to input **60** of switch **56** and input **64** of switch **58**. The switch output **62** of switch **56** is coupled to a power plane terminal V_{DD}/V_{SS} of array power domain **14**. Similarly, the switch output **66** is coupled to a power plane terminal V_{DD}/V_{SS} of array power domain **16**.

For clarity of illustration, the core power domain **12** has been shown as including the processor **18**, power control register **20**, array controller **22** and support array(s) **24**. However, the hardware power control **36**, MUXs (**42**,**44**), switches (**56**,**58**), and system memory **80** may also or may not also be included within the core power domain **12**.

Referring still to FIG. **1**, array(s) **28** of array power domain **14** receives and/or sends data across the system bus **26** via data lines **68**. Array controller **22** provides address and control signals for the array(s) **28** and/or support array(s) **30** via signal lines **70**. In addition, support array(s) **30** receives and/or sends data from/to array controller **22** via signal lines **72**. Signal lines **72** include one or more buses as may be required for a particular integrated circuit implementation. Furthermore, array(s) **32** of array power domain **16** receives and/or sends data across the system bus **26** via data lines **74**. Array controller **22** provides address and control signals for the array(s) **32** and/or support array(s) **34** via signal lines **76**. Furthermore, support array(s) **34** receives and/or sends data from/to array controller **22** via signal lines **72**.

FIG. **2** is a flow diagram view of an array(s) power-down sequence **82** under software control according to one embodiment of the present disclosure. The array(s) power-down sequence **82** can be executed at any time in which processor **18** is able to execute instructions during operation of integrated circuit **10**. The target array or arrays are those array/arrays to be powered down for achieving a desired reduction in overall leakage current of integrated circuit **10**. The target array or arrays can include one or more of arrays **28** and **32**, one or more support arrays **30** and **34**, or any combinations thereof. The actual selection of the target array(s) is based upon selection criteria relating to leakage savings and performance impact of the array(s) in a particular integrated circuit implementation. At step **84** of sequence **82**, processor **18** synchronizes system memory **80** with contents of the target array(s). In one embodiment, synchronizing system memory may entail the flushing of a cache memory. Cache memory may include an L1, L2, L3, or other similar type memory. Subsequent to synchronizing system memory, at step **86**, processor **18** disables access to the target array(s) via array control register **22**. In an embodiment using a cache array, disabling access can include placing the cache array in a by-pass mode, wherein all subsequent cache memory requests are passed to a next level of memory.

Finally, in step **88**, processor **18** removes power to the target array(s) as a function of the desired leakage current reduction by writing to the power control register **20**, instructing power control register **20** to de-assert one or more corresponding software power control signals of the target array(s). As a result, connectivity of one or more corresponding switches is interrupted. For example, in FIG. **1**, if the target array includes one or more of array(s) within array power domain **14**, then processor **18** would instruct power control register **20** to de-assert software power control signal **46** while driving hardware/software select line **50** to the software select state, thus causing connectivity between the input and output of switch **56** to be interrupted.

FIG. **3** is a flow diagram view of an array(s) power-up sequence **90** under software control according to the embodiment corresponding to FIG. **2**. The array(s) power-up sequence **90** can be executed at any time in which processor **18** is able to execute instructions during operation of integrated circuit **10**. For the power-up sequence **90**, the target array or arrays are those array/arrays to be powered up to an active operating mode. The target array or arrays can include one or more of arrays **28** and **32**, one or more support arrays **30** and **34**, or any combinations thereof.

In step **92**, processor **18** restores power to the target array(s) by writing to the power control register **20**, instructing power control register **20** to assert one or more corresponding software power control signals of the target array(s). As a result, connectivity of one or more corresponding switches is established. For example, in FIG. **1**, if the target array includes one or more of array(s) within array power domain **14**, then processor **18** would instruct power control register **20** to assert software power control signal **46** while driving hardware/software select line **50** to the software select state, thus causing connectivity between the input and output of switch **56** to be established.

At step **94** of sequence **90**, processor **18** marks all data in the target array(s) as unusable via array controller **22**, because the contents of the target array would be unknown, and hence, unusable. In one embodiment, marking all data in the target array(s) as unusable may entail invalidating the contents of a cache memory. As indicated above, cache memory may include an L1, L2, L3, or other similar type memory. Subsequent to marking the data as unusable, at step **96**, processor **18** enables access to the target array(s) via array control register **22**. In an embodiment using a cache array, enabling access can include placing the cache array in an operational mode, wherein all subsequent cache memory requests are evaluated by the cache memory for servicing according to the then current contents of the cache memory.

FIG. **4** is a flow diagram view of an array(s) power-down sequence **98** under hardware control according to yet another embodiment of the present disclosure. Prior to execution of sequence **98**, processor **18** configures the corresponding power control MUXs for hardware power control. For example, in FIG. **1**, if the target array(s) were part of array power domain **14**, then processor **18** would instruct power control register **20** to drive the hardware/software select line **50** to the hardware select state. Accordingly, input **38** is passed to output **48** of MUX **42**.

The array(s) power-down sequence **98** is executed as part of an integrated circuit system wide, or sub-system wide, low-power mode entry sequence for causing the integrated circuit system or sub-system to enter a power savings mode which is outside the scope of the present embodiments. The target array or arrays are those array/arrays to be powered down for achieving a desired reduction in overall leakage current of integrated circuit **10**. The target array or arrays can include one or more of arrays **28** and **32**, one or more support arrays **30** and **34**, or any combinations thereof. The selection criteria for the target array(s) is similar to that as mentioned herein above.

At step **100** of sequence **98**, processor **18** synchronizes system memory **80** with contents of the target array(s). In one embodiment, synchronizing system memory may entail the flushing of a cache memory. Cache memory may include an L1, L2, L3, or other similar type memory. Subsequent to synchronizing system memory, at step **102**, processor **18** optionally marks all data in the target array(s) as unusable via array controller **22**. In one embodiment, marking all data in the target array(s) as unusable may entail invalidating the contents of a cache memory. As indicated above, cache memory may include an L1, L2, L3, or other similar type memory. At some period of time subsequent to marking the data as unusable, at step **104**, processor **18** halts by execution of an appropriate instruction.

At step **106**, power hardware control **36** removes power to the target array(s) as a function of the desired leakage current reduction by de-asserting one or more corresponding hardware power control signals of the target array(s). As a result, connectivity of one or more corresponding switches is interrupted. For example, in FIG. **1**, if the target array includes one or more of array(s) within array power domain **14**, then hardware power control **36** would de-assert hardware power control signal **38**, thus causing connectivity between the input and output of switch **56** to be interrupted. This array(s) power-down sequence portion of the system or sub-system power savings mode entry sequence is then ended.

FIG. **5** is a flow diagram view of an array(s) power-up sequence **108** under hardware control according to the embodiment corresponding to FIG. **4**. Prior to execution of sequence **108**, processor **18** configures the corresponding power control MUXs for hardware power control. For example, in FIG. **1**, if the target array(s) were part of array power domain **14**, then processor **18** would instruct power control register **20** to drive the hardware/software select line **50** to the hardware select state. Accordingly, input **38** is passed to output **48** of MUX **42**.

The array(s) power-up sequence **108** is executed at as part of an integrated circuit system wide, or sub-system wide, low-power mode exit sequence for causing the integrated circuit system or sub-system to exit a power savings mode which is outside the scope of the present embodiments. For the power-up sequence **108**, the target array or arrays are those array/arrays to be powered up to an active operating mode. The target array or arrays can include one or more of arrays **28** and **32**, one or more support arrays **30** and **34**, or any combinations thereof.

In step **110**, hardware power control **36** restores power to the target array(s) by asserting one or more corresponding hardware power control signals of the target array(s). As a result, connectivity of one or more corresponding switches is established. For example, in FIG. **1**, if the target array includes one or more of array(s) within array power domain **14**, then hardware power control **36** would assert hardware power control signal **38**, thus causing connectivity between the input and output of switch **56** to be established.

Subsequent to restoration of power to the target array(s), at step **112** of sequence **108**, invalidation hardware optionally marks all data in the target array(s) as unusable. In one embodiment, the invalidation hardware comprises a support array, such as a cache valid array, having a zero-ize input as discussed hereafter with respect to FIG. **6**. The zero-ize input operates to reset the state of all bits in the corresponding support array to a known value, wherein the hardware power control **36** drives the zero-ize input.

Subsequent to marking the data as unusable, at step **114**, hardware power control **36**, or a different hardware power control element not specifically disclosed herein, restarts processor **18**. In an embodiment using a cache array, all subsequent accesses by processor **18** are evaluated by the cache memory for servicing according to the then current contents of the cache memory.

FIG. **6** is a block diagram view of a portion of the integrated circuit **10** of FIG. **1** in greater detail according to yet another embodiment of the present disclosure. For example, one or more of array(s) **28**, **30**, **32**, or **34** could include a configuration **116** having an array **118** with separate power terminals (**120**,**122**) respectively for a corresponding array periphery **124** and for the corresponding bit cells **126**, and/or a zero-ize input **128**. In this configuration, the bit cells **126** remain powered while power for the array periphery **124** is switched by switch **130**, further as controlled by signal **132** from a corresponding power switch control MUX, such as, MUX **42**, **44**, or other power switch control MUX.

Further to the above discussion, in one embodiment an integrated circuit having power management includes processing circuitry, at least one memory array, and control circuitry. The processing circuitry executes instructions. The at least one memory array couples to the processing circuitry for providing data to the processing circuitry. Lastly, the control circuitry couples to the at least one memory array, wherein the control circuitry removes electrical connectivity of the at least one memory array to a supply voltage terminal by firstly disabling all accesses to the at least one memory array and secondly removing electrical power to all of the at least one memory array to reduce leakage current in the at least one memory array.

The integrated circuit may further include one or more supporting memory arrays coupled to the at least one memory array. The one or more supporting memory arrays provide a support function to operate a corresponding one of the at least one memory array. In addition, according to one embodiment, the control circuitry keeps the one or more supporting memory arrays selectively powered up when electrical power is removed to all of the at least one memory array depending upon whether all data in the at least one memory array must be marked as unusable upon restoring power to the at least one memory array.

In another embodiment, the integrated circuit is similar as that as described above, wherein the control circuitry further

includes a switch having a first terminal coupled to the supply voltage terminal and a second terminal coupled to a power plane terminal of the at least one memory array. The switch also includes a control terminal for receiving a control signal that determines when the switch is conductive. The control signal can be provided in response to either execution of at least one instruction by the processing circuitry or in response to receipt by the processing circuitry of a power down signal. In addition, a configuration register stores a control value that determines whether the control signal is provided in response to execution of the at least one instruction or in response to the power down signal.

In yet another embodiment, the integrated circuit is similar as that as described above, wherein the integrated circuit further includes a plurality of memory arrays, each of the plurality of memory arrays being coupled to the control circuitry and being able to be independently entirely powered off to reduce transistor leakage current.

In still yet another embodiment, the integrated circuit is similar as that as described above, wherein the integrated circuit further includes a system memory coupled to the processing circuitry, wherein the control circuitry synchronizes the system memory by flushing the at least one memory array of stored data and physically halts the processing circuitry prior to removing power to the at least one memory array.

In another additional embodiment, the integrated circuit is similar as that as described above, wherein the integrated circuit further includes a system memory coupled to the processing circuitry, wherein contents of the at least one memory array are synchronized with the system memory and wherein the at least one memory array comprises a copy-back cache that is configured as a write-through cache so that the contents of the at least one memory array are always synchronized with the system memory.

In yet another additional embodiment, the integrated circuit is similar as that as described above, wherein the integrated circuit further includes a system memory coupled to the processing circuitry, wherein the control circuitry synchronizes the system memory by flushing the at least one memory array of stored data prior to disabling accesses to the at least one memory array under control of the processing circuitry for executing instructions and removing power to the at least one memory array. Furthermore, the integrated circuit further includes a control register coupled to the at least one memory array. The control register is configured for storing a command signal provided by the processing circuitry. The command signal disables accesses to the at least one memory array.

In still yet another embodiment, the integrated circuit is similar as that as described above, wherein the integrated circuit further includes a control register within the control circuitry. The control register receives and stores a command signal from the processing circuitry that functions to restore power to the at least one memory array. The control circuitry further comprises an array controller that marks all data entries in the at least one memory array with a predetermined bit value prior to the array controller enabling accesses to the at least one memory array.

In another embodiment, the integrated circuit is similar as that as described above, wherein the control circuitry restores power to the at least one memory array in response to a power up signal and marks all data entries in the at least one memory array as unusable prior to restarting the circuitry for executing instructions.

The control circuitry may further include monitoring logic that observes memory accesses of the at least one memory array during removing electrical power to all of the at least one memory array. The monitoring logic limits powering up of the at least one memory array in response to one or more memory requests until a predetermined criteria is met. In addition, the monitoring logic is configured to use differing predetermined criteria depending upon a sequence of instructions executed by the processing circuitry.

According to another embodiment, an integrated circuit having power management includes processing circuitry, a plurality of memory bit cells contained within a memory array, memory array peripheral circuitry, and control circuitry. The processing circuitry is configured to execute instructions. The plurality of memory bit cells contained within the memory array are coupled to a power supply terminal for creating a first power plane. The memory array peripheral circuitry is peripheral to the plurality of memory bit cells, wherein the memory array peripheral circuitry is selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane. Lastly, the control circuitry is coupled to the memory array circuitry peripheral to the plurality of memory bit cells, wherein the control circuitry is configured to selectively remove electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

In another embodiment, the control circuitry provides a control signal to selectively remove electrical connectivity, the control signal being provided in response to either execution of at least one instruction by the processing circuitry or in response to receipt by the processing circuitry of a power down signal. In another embodiment, the control circuitry halts the processing circuitry prior to removing power from the power supply terminal. Still further, in yet another embodiment, the control circuitry disables access to the plurality of memory bit cells prior to removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

In another embodiment, the integrated circuit is similar as that as described above, wherein the integrated circuit further comprises monitoring logic. The monitoring logic is configured to observe memory accesses of the memory array during removing electrical power to all of the memory array. The monitoring logic is further configured to limit powering up of the memory array in response to one or more memory requests until a predetermined criteria is met. In addition, the monitoring logic uses differing predetermined criteria depending upon a sequence of instructions executed by the processing circuitry.

According to yet another embodiment, a method for reducing leakage current in an integrated circuit includes providing a first power plane of circuitry, the first power plane of circuitry comprising an array of memory cells, and providing a second power plane of circuitry, the second power plane of circuitry comprising a processor and control circuitry. The control circuitry removes electrical connectivity of the array of memory cells to a supply voltage terminal by firstly disabling all accesses to the array of memory cells and secondly removing electrical power to all of the array of memory cells to reduce leakage current in the array of memory cells.

The method can also include providing at least one supporting array of memory cells in either the first power plane of circuitry or the second power plane of circuitry for providing support functions to the array of memory cells. In one embodiment, when the at least one supporting array of

memory cells is in the first power plane of circuitry, the supporting array of memory cells is not powered down when the second power plane of circuitry is powered down thereby keeping a record of validity status of bits in the array of memory cells.

The method may further include providing one or more additional power planes of circuitry coupled to the first power plane of circuitry. The one or more additional power planes of circuitry can comprise additional arrays of memory cells in which each additional array may be separately and completely powered down independently of whether the second power plane of circuitry is powered.

According to yet another embodiment, a method of power management in an integrated circuit includes executing instructions with a processor and providing a plurality of memory bit cells contained within a memory array. The plurality of memory bit cells are coupled to a power supply terminal for creating a first power plane. The method further includes providing memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, selectively coupling the memory array peripheral circuitry to the power supply terminal for creating a second power plane that is independent of the first power plane. The method further includes coupling control circuitry to the memory array peripheral circuitry to the plurality of memory bit cells. Lastly, the method includes selectively removing electrical connectivity to the power supply voltage terminal of the memory array peripheral circuitry to the plurality of memory bit cells.

The method can further comprise observing memory accesses of the plurality of memory bit cells during removing of electrical power to all of the plurality of memory bit cells. In addition, the method includes limiting powering up of the plurality of memory bit cells in response to one or more memory requests until a predetermined criteria is met. Differing predetermined criteria can be used depending upon a sequence of instructions executed by the processor.

Programming of instructions to be processed by the processor or processing circuitry for carrying out the various functions and/or functionalities of the methods as discussed herein above can be performed using programming techniques well known in the art. For example, programming includes software modifications to a low-power mode entry/exit routine of a device incorporating an integrated circuit of the present embodiments and/or addition of software control code to the same.

In the foregoing specification, the disclosure has been described with reference to various embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present embodiments as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present embodiments.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the term "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements by may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

We claim:

1. An integrated circuit having power management comprising:

processing circuitry for executing instructions;

at least one memory array coupled to the processing circuitry for providing data to the processing circuitry; and

control circuitry coupled to the at least one memory array, the control circuitry removing electrical connectivity of the at least one memory array to a supply voltage terminal by firstly disabling all accesses to the at least one memory array and secondly removing electrical power to all of the at least one memory array to reduce leakage current in the at least one memory array.

2. The integrated circuit of claim **1** further comprising:

one or more supporting memory arrays coupled to the at least one memory array, the one or more supporting memory arrays providing a support function to operate the at least one memory array, the control circuitry keeping the one or more supporting memory arrays selectively powered up when electrical power is removed to all of the at least one memory array depending upon whether all data in the at least one memory array must be marked as unusable upon restoring power to the at least one memory array.

3. The integrated circuit of claim **1** wherein the control circuitry further comprises:

a switch having a first terminal coupled to the supply voltage terminal and a second terminal coupled to a power plane terminal of the at least one memory array, the switch further comprising a control terminal for receiving a control signal that determines when the switch is conductive.

4. The integrated circuit of claim **3** wherein the control signal is provided in response to either execution of at least one instruction by the processing circuitry or in response to receipt by the processing circuitry of a power down signal.

5. The integrated circuit of claim **4** further comprising:

a configuration register for storing a control value that determines whether the control signal is provided in response to execution of the at least one instruction or in response to the power down signal.

6. The integrated circuit of claim **1** further comprising:

a plurality of memory arrays, each of the plurality of memory arrays being coupled to the control circuitry and being able to be independently entirely powered off to reduce transistor leakage current.

7. The integrated circuit of claim **1** further comprising:

a system memory coupled to the processing circuitry, wherein the control circuitry synchronizes the system memory by flushing the at least one memory array of stored data and physically halts the processing circuitry prior to removing power to the at least one memory array.

8. The integrated circuit of claim **1** further comprising:

a system memory coupled to the processing circuitry, wherein contents of the at least one memory array are synchronized with the system memory and wherein the at least one memory array comprises a copy-back cache that is configured as a write-through cache so that the contents of the at least one memory array are always synchronized with the system memory.

9. The integrated circuit of claim **1** further comprising:

a system memory coupled to the processing circuitry, wherein the control circuitry synchronizes the system

memory by flushing the at least one memory array of stored data prior to disabling accesses to the at least one memory array under control of the processing circuitry for executing instructions and removing power to the at least one memory array.

10. The integrated circuit of claim **9** further comprising:

a control register coupled to the at least one memory array, the control register storing a command signal provided by the processing circuitry for executing instructions, the command signal disabling accesses to the at least one memory array.

11. The integrated circuit of claim **1** further comprising:

a control register within the control circuitry, the control register receiving and storing a command signal from the processing circuitry for executing instructions that functions to restore power to the at least one memory array, the control circuitry further comprising an array controller that marks all data entries in the at least one memory array with a predetermined bit value prior to the array controller enabling accesses to the at least one memory array.

12. The integrated circuit of claim **1** wherein the control circuitry restores power to the at least one memory array in response to a power up signal and marks all data entries in the at least one memory array as unusable prior to restarting the circuitry for executing instructions.

13. The integrated circuit of claim **1** wherein the control circuitry further comprises monitoring logic that observes memory accesses of the at least one memory array during removing electrical power to all of the at least one memory array, the monitoring logic limiting powering up of the at least one memory array in response to one or more memory requests until a predetermined criteria is met.

14. The integrated circuit of claim **13** wherein the monitoring logic uses differing predetermined criteria depending upon a sequence of instructions executed by the processing circuitry.

15. An integrated circuit having power management comprising:

processing circuitry for executing instructions;

a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane;

memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the memory array peripheral circuitry being selectively coupled to the power supply terminal for creating a second power plane that is independent of the first power plane; and

control circuitry coupled to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the control circuitry selectively removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

16. The integrated circuit of claim **15** wherein the control circuitry provides a control signal to selectively remove electrical connectivity, the control signal being provided in response to either execution of at least one instruction by the processing circuitry or in response to receipt by the processing circuitry of a power down signal.

17. The integrated circuit of claim **15** wherein the control circuitry halts the processing circuitry prior to removing power from the power supply terminal.

18. The integrated circuit of claim **15** wherein the control circuitry disables access to the plurality of memory bit cells prior to removing electrical connectivity to the power supply terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

19. The integrated circuit of claim **15** further comprising monitoring logic that observes memory accesses of the memory array during removing electrical power to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells, the monitoring logic limiting powering up of the memory array peripheral circuitry in response to one or more memory requests until a predetermined criteria is met.

20. The integrated circuit of claim **19** wherein the monitoring logic uses differing predetermined criteria depending upon a sequence of instructions executed by the processing circuitry.

21. A method for reducing leakage current in an integrated circuit comprising:

providing a first power plane of circuitry, the first power plane of circuitry comprising an array of memory cells; and

providing a second power plane of circuitry, the second power plan of circuitry comprising a processor and control circuitry, the control circuitry removing electrical connectivity of the array of memory cells to a supply voltage terminal by firstly disabling all accesses to the array of memory cells and secondly removing electrical power to all of the array of memory cells to reduce leakage current in the array of memory cells.

22. The method of claim **21** further comprising:

providing at least one supporting array of memory cells in either the first power plane of circuitry or the second power plane of circuitry for providing support functions to the array of memory cells, wherein when the at least one supporting array of memory cells is in the first power plane of circuitry, the supporting array of memory cells is not powered down when the second power plane of circuitry is powered down thereby keeping a record of validity status of bits in the array of memory cells.

23. The method of claim **21** further comprising:

one or more additional power planes of circuitry coupled to the first power plane of circuitry, the one or more additional power planes of circuitry comprising additional arrays of memory cells in which each additional array may be separately and completely powered down independently of whether the second power plane of circuitry is powered.

24. A method of power management in an integrated circuit comprising:

executing instructions with a processor;

providing a plurality of memory bit cells contained within a memory array, the plurality of memory bit cells being coupled to a power supply terminal for creating a first power plane;

providing memory array peripheral circuitry that is peripheral to the plurality of memory bit cells;

selectively coupling the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells to the power supply terminal for creating a second power plane that is independent of the first power plane;

coupling control circuitry to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells; and

selectively removing electrical connectivity to the power supply voltage terminal of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells.

25. The method of claim **24** further comprising:

observing memory accesses of the plurality of memory bit cells during removing of electrical power to the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells; and

limiting powering up of the memory array peripheral circuitry that is peripheral to the plurality of memory bit cells in response to one or more memory requests until a predetermined criteria is met.

26. The method of claim **25** further comprising:

using differing predetermined criteria depending upon a sequence of instructions executed by the processor.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,917,555 B2
APPLICATION NO. : 10/675005
DATED : July 12, 2005
INVENTOR(S) : Ryan D. Bedwell et al.

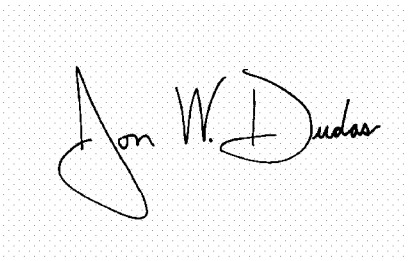
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 12, Line 21, Claim No. 21:

Change "plan" to --plane--.

Signed and Sealed this

Third Day of April, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office