

**IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE**

NORTH STAR INNOVATIONS INC.,

Plaintiff,

vs.

NIKON CORPORATION, NIKON INC.,

Defendants.

C.A. No.

**JURY DEMANDED**

**COMPLAINT**

Plaintiff North Star Innovations Inc. (“North Star”) complains of Defendants Nikon Corporation and Nikon Inc. (collectively, “Nikon”) as follows:

**JURISDICTION AND VENUE**

1. Title 28 of the United States Code Section 1338(a) confers subject matter jurisdiction on this Court because Defendants have infringed Plaintiff’s patent. The Patent Act of 1952, as amended, 35 U.S.C. § 271, *et seq.*, makes patent infringement actionable through a private cause of action.

2. Defendants have transacted business in the State of Delaware, and in this judicial district by making, using, selling, offering to sell and distributing products in this judicial district that violate North Star’s patent. Accordingly, this Court has personal jurisdiction over Defendants.

3. Venue is proper in the District of Delaware under the general federal venue statute, 28 U.S.C. § 1391(d), and under the specific venue provision relating to patent infringement cases, 28 U.S.C. § 1400(b).

**PARTIES**

4. North Star is a Delaware corporation with its principal place of business at Plaza Tower, 600 Anton Boulevard, Suite 1350, Costa Mesa, CA 92626. North Star is a subsidiary of Wi-LAN Technologies Inc. North Star is the assignee of and owns all right, title and interest in and has standing to sue for infringement of United States Patent No.

5,892,777 (“the ’777 Patent”), entitled Apparatus and Method for Observing the Mode of a Memory Device. The ’777 Patent issued April 6, 1999 and claims priority to May 5, 1997 and is attached as Exhibit A.

5. Nikon Corporation is a Japanese multinational corporation with its principal place of business at Shinagawa Intercity Tower C, 2-15-3, Konan, Minato-ku, Tokyo 108-6290. Nikon Corporation has previously and is presently making, using, selling, offering for sale, and/or importing into the United States imaging products (containing memory devices) that infringe one or more claims of the ’777 Patent.

6. Nikon Inc. is a New York corporation with its principal place of business at 1300 Walt Whitman Road, Melville, NY 11747-3064. Nikon Inc. has previously and is presently making, using, selling, offering for sale, and/or importing into the United States imaging products (containing memory devices) that infringe one or more claims of the ’777 Patent.

#### BACKGROUND

7. North Star is the owner of patent rights, which cover commercially significant technologies related to observing the mode of a memory device. In particular, the ’777 Patent covers a method and apparatus to observe a mode register in a synchronous memory device.

8. Defendants design, manufacture, and sell imaging products (containing memory devices) that infringe the ’777 Patent.

#### PATENT INFRINGEMENT OF THE ’777 PATENT

9. Defendants have infringed and continue to infringe at least claim 1 of the ’777 Patent, in violation of 35 U.S.C. § 271 through, among other activities, making, using, offering to sell, and/or selling their Nikon DSLR Camera (Model: D7200). Photos of the Nikon DSLR Camera are depicted below, including a package photo – top view (left) and package photo – bottom view (right):

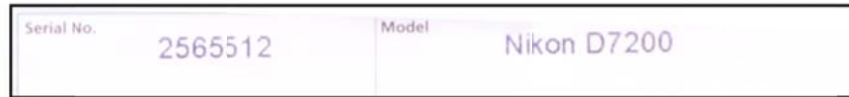


Package Photo – Top View



Package Photo – Bottom View

Package label photos of the Nikon DSLR Camera is shown below:

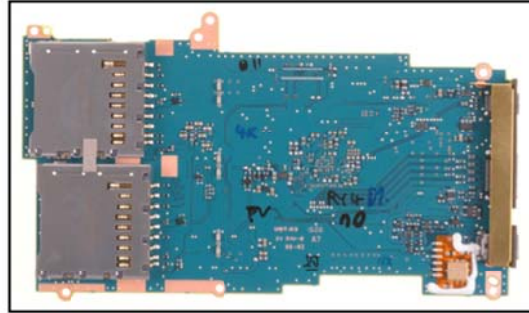


Package Label Photos

Board photos of the Nikon DSLR Camera are shown below, including a board photo – top view (left) and board photo – bottom view (right):

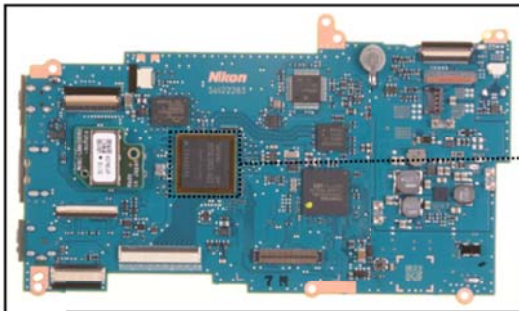


**Board Photo – Top View**

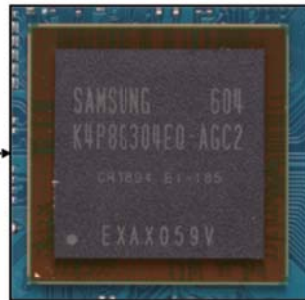


**Board Photo – Bottom View**

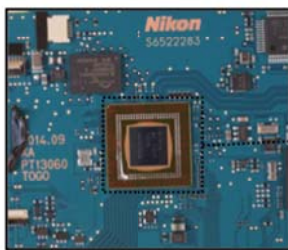
More board photos of the Nikon DSLR Camera are shown below, with larger views of two of its components, the Samsung 8Gb LPDDR2 SDRAM Part#: K4P8G304EQ-AGC2 (top), and Nikon Image Processor Part#: M2-1321 (bottom):



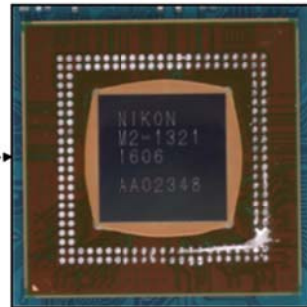
**Board Photo – Top View**



**Samsung 8Gb LPDDR2 SDRAM**  
Part #: K4P8G304EQ-AGC2  
Date Code: 604  
IPRG#: IP-3256-2



**Board Photo – Top View  
(with memory removed)**



**Nikon Image Processor**  
Part#: M2-1321  
Date Code: 1606  
IPRG#: IP-3256-1

**Nikon DSLR Camera**  
Model No.: D7200  
Date Code: N/A  
IPRG#: IP-3254

10. Defendants' infringing technology and products include without limitation their imaging products (containing memory devices), including, for example, the Nikon DSLR Camera and other imaging products. Defendants' infringement may include

additional products and technologies (to be determined in discovery) marketed or used by Defendants.

11. Claim 1 is an exemplary infringed claim. Its preamble states: “A method for observing a control register (A) in a memory device (B), the control register defining an operation of the memory device (C), the control register not observable from the memory device (D), the method comprising the steps of.” Subparts of the preamble are labeled (A) through (D) for analysis purposes. Defendants’ products, such as their Nikon DSLR Camera, perform a method for observing a control register (A) in a memory device (B), the control register defining an operation of the memory device (C), the control register not observable from the memory device (D).

12. The Nikon DSLR Camera contains subpart (A) of the preamble, a control register, by virtue of a mode register of the LPDDR2 SDRAM. Section 3.5.1 of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 30 defines the Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM. Table 17 – Mode Register Assignment in LPDDR2 SDRAM/NVM(Common Part) shows the mode registers for LPDDR2 SDRAM. The control register is MR# 4.

13. The Nikon DSLR Camera contains subpart (B) of the preamble, in a memory device, by virtue of the LPDDR2 SDRAM which it contains. The memory device is the Samsung 8Gb LPDDR2 SDRAM Part#: K4P8G304EQ-AGC2.

14. The Nikon DSLR Camera contains subpart (C) of the preamble, the control register defining an operation of the memory device, by virtue of the contents of the control (mode) register MR# 4, including SDRAM Refr. R. for Function, R for Access, TUF for OP[7], (RFU) for OP[6]-OP[3], and Refresh Rate for OP[2]-OP[0]. Section 5.12.1, Temperature Sensor, of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 126 indicates that “LPDDR2-SX and LPDDR2-N devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate (SDRAM).”

15. The Nikon DSLR Camera contains subpart (D) of the preamble, the control register not observable from the memory device, by virtue of clock synchronization and the Mode Register Read Command of the LPDDR2. Section 5.12, Mode Register Read Command, of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 124 indicates that “The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7,  $RL * t_{CK} + t_{DQSCK} + t_{DQSQ}$  after the rising edge of the clock where the Mode Register Read Command is issued.”

16. After the preamble, the first limitation of claim 1 states: “storing a received value in the control register responsive to a first signal (E) (F).” This limitation is labeled (E) (F) for analysis purposes.

17. The Nikon DSLR Camera contains limitation (E), storing a received value in the control register responsive to a first signal, by virtue of internal updates of MR4. Page 126 of LPDDR2 JEDEC Standard JESD209-2B, February 2010 indicates that “TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.” The graph shown as Figure 81 – Temp Sensor Timing of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 127 shows storing a received value in the control register responsive to a first signal along the Time axis at MR4 = 0x03, MR4=0x86, MR4=0x86, MR4=0x86, MR4=0x86, and MR4=0x06.

18. The Nikon DSLR Camera contains sublimitation (F), a first signal, by virtue of the Temperature Sensor Update, which is shown in the graph in Figure 81 – Temp Sensor Timing of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 127.

19. After the first limitation, the second limitation of claim 1 states: “outputting the received value responsive to a second control signal (G) when no output

is expected from the memory device (H).” This limitation is labeled (G) and (H) for analysis purposes. The Nikon DSLR Camera contains this limitation.

20. The Nikon DSLR Camera contains sublimitation (G), a second control signal, by virtue of the Mode Register Read (MRR) command. This command is the Host MR4 Read, shown in Figure 81 – Temp Sensor Timing on page 127 in LPDDR2 JEDEC Standard JESD209-2B, February 2010. Section 5.12, Mode Register Read Command, of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 124 indicates that “The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM.” The MRR command is shown in Figure 78 – Mode Register Read timing example:  $RL = 3$ ,  $t_{MRR} = 2$  on page 124 of LPDDR2 JEDEC Standard JESD209-2B, February 2010. The second control signal is also represented as symbols CA3, CA2, CA0, CA1, CS1\_n, CS0\_n, CK\_t, and CK\_c, sent between the memory and processor.

21. The Nikon DSLR Camera contains limitation (H), outputting the received value responsive to a second control signal when no output is expected from the memory device, by virtue of the MRR MR4 reads from the system. These reads are shown in the graph in Figure 81 of LPDDR2 JEDEC Standard JESD209-2B, February 2010 at MRR MR4 = 0x03 and MRR MR4 = 0x86. Section 5.12.1 Temperature Sensor on page 126 indicates that “ReadInterval is the time period between MR4 reads from the system”, and “SysRespDelay is the maximum time between a read of MR4 and the response by the system.” Additionally, Section 5.12, Mode Register Read Command, of LPDDR2 JEDEC Standard JESD209-2B, February 2010 on page 124 states “The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS\_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock.” and “The mode register contents are available on the first data beat of DQ0-DQ7,  $RL * t_{CK} + t_{DQSK} + t_{DQSQ}$  after the rising edge of the clock where the Mode Register Read Command is issued.” Moreover, DOUT A on the DQ[0-7] signal, shown in Figure

78 – Mode Register Read timing example:  $RL = 3$ ,  $t_{MRR} = 2$  on page 124 of LPDDR2 JEDEC Standard JESD209-2B, February 2010 shows this limitation, “outputting the received value responsive to a second control signal when no output is expected from the memory device” as NOTE 3 states that “Mode Register data is valid only on DQ[0-7] on the first beat.” This is further represented as symbols DQ6, DQ7, DQ5, DQ4, DQ3, DQ0, DQ1, and DQ2 sent between the memory and processor.

22. After the second limitation, the third and final limitation of claim 1 states, “disabling the operation of the memory device responsive to the second control signal subsequent to the step of outputting (I).” This limitation is labeled (I) for analysis purposes. The The Nikon DSLR Camera contains this limitation (I), because the “The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period ( $t_{MRR}$ ) is 2 clock cycles.” as indicated in Section 5.12 Mode Register Read Command of LPDDR2 JEDEC Standard JESD209-2B, February 2010. This is further indicated in Figure 78 – Mode Register Read timing example:  $RL = 3$ ,  $t_{MRR} = 2$  of LPDDR2 JEDEC Standard JESD209-2B, February 2010, as NOTE 2 indicates that “Mode Register Read operation shall not be interrupted” and NOTE 4 indicates that “The Mode Register Command period is  $t_{MRR}$ . No command (other than Nop) is allowed during this period.”

23. As a direct and proximate consequence of Defendants’ infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

24. Defendants’ infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further manufacture, use, sale and/or offer for sale of products that come within the scope of the ’777 Patent.



JURY DEMAND

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, North Star demands a trial by jury on all issues presented that can properly be tried to a jury.

REQUEST FOR RELIEF

THEREFORE, North Star asks this Court to enter judgment against Defendants and against their subsidiaries, affiliates, agents, servants, employees and all persons in active concert or participation with Defendants, granting the following relief:

- A. An award of damages adequate to compensate North Star for the infringement that has occurred, together with prejudgment interest from the date infringement began and postjudgment interest;
- B. All other damages permitted by 35 U.S.C. § 284;
- C. A finding that this case is exceptional and an award to North Star of its attorneys' fees and costs as provided by 35 U.S.C. § 285;
- D. A permanent injunction prohibiting further infringement, inducement and contributory infringement of the '777 Patent; and
- E. Such other and further relief as this Court or a jury may deem proper and just.

Dated: August 19, 2016

Respectfully submitted,

FARNAN LLP

Of Counsel:

William W. Flachsbart  
Robert P. Greenspoon  
Michael R. La Porte  
FLACHSBART & GREENSPOON, LLC  
333 North Michigan Avenue, Suite 2700  
Chicago, IL 60601  
T: 312-551-9500  
F: 312-551-9501

/s/ Brian Farnan  
Brian E. Farnan (Bar No. 4089)  
Michael J. Farnan (Bar No. 5165)  
919 N. Market St., 12<sup>th</sup> Floor  
Wilmington, DE 19801  
(302) 777-0300  
(302) 777-0301  
bfarnan@farnanlaw.com  
mfarnan@farnanlaw.com

*Attorneys for Plaintiff  
North Star Innovations Inc.*