

2. Defendant ASE (U.S.) Inc. (“ASE”) is a California corporation organized and existing under the laws of the State of California, with a principal place of business at 1255 E. Arques Avenue, Sunnyvale, CA 94085. It may be served with process by serving its registered agent, Jon Howard at 1255 E. Arques Ave., Sunnyvale, CA 94085.

3. ASE has multiple U.S. sales offices, including offices in Dallas and Austin, Texas. *See, e.g.*, <http://www.aseglobal.com/en/About/ASEContact.asp#na-07>.

4. On information and belief, ASE is the U.S. sales arm for, and a wholly-owned subsidiary of, Advanced Semiconductor Engineering, Inc. (“The ASE Group”), a Taiwanese company that manufactures and sells semiconductor products throughout the world. According to its website: “The ASE Group is the world’s largest provider of independent semiconductor manufacturing services in assembly and test. The group develops and offers complete turnkey solutions covering IC packaging, design and production of interconnect materials, front-end engineering test, wafer probing and final test As [the] global leader, ASE provides a complete scope of services for the semiconductor market, driven by superior technologies, breakthrough innovations, and advanced development programs.”

JURISDICTION AND VENUE

5. This action arises under the patent laws of the United States, 35 U.S.C. § 1 *et seq.*, including §§ 271, 281, 282(a), 283, 284, 285, and 295. This Court has subject matter jurisdiction over this patent infringement action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Defendant. Defendant has regularly conducted and continues to conduct business in the State of Texas and in this judicial district. On information and belief, Defendant has committed infringing activities in the United States, in Texas, and in this judicial district by, at a minimum, importing, using, offering for sale and/or

selling products that infringe the Patents-In-Suit (as defined below); by placing such infringing products into the stream of commerce with the awareness, knowledge, and intent that they would be used, offered for sale, and/or sold by others in this judicial district and/or purchased by consumers in this judicial district; and/or by importing into the U.S. and/or offering for sale and/or selling in this judicial district one or more products made by a process patented in the U.S..

7. Venue is proper pursuant to 28 U.S.C. §§ 1391(b) and 1400(b).

THE PATENTS-IN-SUIT

8. On April 20, 1999, U.S. Patent No. 5,895,229 (“the ’229 Patent”) – entitled “Microelectronic Package Including a Polymer Encapsulated Die, and Method for Forming Same” – was lawfully and properly issued by the United States Patent and Trademark Office (“USPTO”), after a full and fair examination. The named inventors on the ’229 Patent are: Francis J. Carney and Donald H. Klosterman of Gilbert, Arizona; George Amos Carson of Elk Grove Village, Illinois; Phillip C. Celaya, Frank Tim Jones, and James Howard Knapp of Chandler, Arizona; Harry Fuerhaupter of Lombard, Illinois; Cynthia M. Melton of Bolingbrook, Illinois; and Keith E. Nelson of Tempe, Arizona. A true and correct copy of the ’229 Patent is attached hereto as Exhibit A and incorporated by reference.

9. Generally speaking, the ’229 Patent teaches, among other things, a method for forming a microelectronic package in which the integrated circuit die is completely encapsulated within a molded polymeric material. The novel process leads to enhanced reliability and reinforcement to the solder bump interconnections and also provides protection for the back side of the integrated circuit die using a single, less complex manufacturing process that, in certain embodiments, minimizes the footprint of the package.

10. On January 11, 2000, U.S. Patent No. 6,013,571 (“the ’571 Patent”) – entitled “Microelectronic Assembly Including Columnar Interconnections and Method for Forming Same” – was lawfully and properly issued by the USPTO, after a full and fair examination. The named inventor on the ’571 Patent is Michelle J. Morell of Glen Ellyn, Illinois. A true and correct copy of the ’571 Patent is attached hereto as Exhibit B and incorporated by reference.

11. Generally speaking, the ’571 Patent teaches, among other things, an integrated circuit component that is connected to a substrate by metallic columnar interconnections that have a predetermined standoff between the component and the substrate. The novel invention provides for a more reliable assembly. Specifically, in a preferred embodiment, the invention helps control the width of the interconnection and thereby controls the lateral dimensions between interconnections to avoid shorting, to reduce stress in the interconnections, and to maintain an adequate height between component and substrate so as to allow for consistent disposal of polymeric precursor into the gaps.

12. On July 25, 2000, U.S. Patent No. 6,093,972 (“the ’972 Patent”) – entitled “Microelectronic Package Including a Polymer Encapsulated Die” – was lawfully and properly issued by the USPTO, after a full and fair examination. The named inventors on the ’972 Patent are: Francis J. Carney and Donald H. Klosterman of Gilbert, Arizona; George Amos Carson of Elk Grove Village, Illinois; Phillip C. Celaya, Frank Tim Jones, and James Howard Knapp of Chandler, Arizona; Harry Fuerhaupter of Lombard, Illinois; Cynthia M. Melton of Bolingbrook, Illinois; and Keith E. Nelson of Tempe, Arizona.. A true and correct copy of the ’972 Patent is attached hereto as Exhibit C and incorporated by reference.

13. Generally speaking, the ’972 Patent teaches, among other things, a microelectronic package in which the integrated circuit die is completely encapsulated within a

molded polymeric material. The novel invention provides a package with enhanced reliability and reinforcement to the solder bump interconnections and also provides protection for the back side of the integrated circuit die using a single, less complex manufacturing process that, in certain embodiments, minimizes the footprint of the package.

14. On October 15, 2002, U.S. Patent No. 6,465,743 (“the ’743 Patent”) – entitled “Multi-Strand Substrate for Ball-Grid Array Assemblies and Method” – was lawfully and properly issued by the USPTO, after a full and fair examination. The named inventor on the ’743 Patent is Norman Lee Owens of Chandler, Arizona. A true and correct copy of the ’743 Patent is attached hereto as Exhibit D and incorporated by reference.

15. Generally speaking, the ’743 Patent teaches, among other things, a novel method for assembling ball-grid array (BGA) packages in an “N by M” array having multiple rows and multiple columns, where the method produces -- in a way that is cost effective and conducive to large-scale automated assembly -- multiple substrates that are resistant to warping.

16. The ’229, ’571, ’972, and ’743 Patents may be referred to individually as a “Patent-in-Suit” or collectively as the “Patents-in-Suit.”

17. Plaintiff acquired the Patents-in-Suit from the company formerly known as Freescale Semiconductor, Inc. in Austin, Texas. By way of assignment, Plaintiff is the owner of all right, title, and interest in and to the Patents-in-Suit, including the rights to prosecute this action and to collect and receive damages for all past, present, and future infringements.

THE ACCUSED PRODUCTS

18. ASE’s infringing acts, as described in this Complaint, relate to its assembly and packaging of certain semiconductor products, including, in particular, the Qualcomm Snapdragon 410 (MSM8916) Processor (“Qualcomm Snapdragon Processor”), which can be

found in many different smartphones and tablets, including the ZTE Speed smartphone. The specifications for the ZTE Speed phone, including its Qualcomm Snapdragon Processor, are described on various publicly available websites, including: http://www.phonearena.com/phones/ZTE-Speed_id9075/fullspecs and http://www.gsmarena.com/zte_speed-6898.php.

19. Qualcomm Incorporated is a Delaware corporation with headquarters at 5775 Morehouse Drive, San Diego, CA 92121. Qualcomm has multiple offices in Texas, including at 2100 Lakeside Blvd., Suite 475, Richardson, TX 75082.

20. ZTE (USA), Inc. is a New Jersey corporation with its principal place of business at 2425 N. Central Expressway, Richardson, TX, 75080, which is located in the Eastern District of Texas. Also, ZTE (TX), Inc. is a Texas corporation having a principal place of business at 2500 Dallas Parkway, Plano, Texas 75093, which is located in the Eastern District of Texas.

COUNT ONE: INFRINGEMENT OF THE '229 PATENT

21. Plaintiff incorporates the above allegations as if set forth here in full.

22. The '229 Patent is valid and enforceable. Defendant does not have a license to practice the patented inventions of the '229 Patent.

23. On information and belief, and in violation of 35 U.S.C. §271(g), Defendant infringes at least Claims 1, 2, and 4 of the '229 Patent. For example, on information and belief, ASE imports, offers for sale, sells, and/or uses products made (by The ASE Group) according to a process that meets each and every limitation in Claim 1 of the '229 Patent, which recites: "A method for forming a microelectronic package comprising:¹ attaching an integrated circuit die to a substrate by a plurality of solder bump interconnections to form a preassembly, said integrated

¹ Plaintiff does not hereby suggest or concede that the preamble of this or any other asserted claim constitutes a substantive limitation. That issue is expressly reserved for the claim construction stage.

circuit die having an active face facing the substrate and spaced apart therefrom by a gap and a back face opposite the active face, said substrate including a die attach region and a surrounding region about the integrated circuit die, said plurality of solder bump interconnections extending across the gap and connecting the integrated circuit die and the substrate; disposing a mold onto the preassembly such that the mold cooperates with the substrate to define a mold cavity that encloses the integrated circuit die, said mold having a molding surface that includes said surrounding region and an inner face facing the back face and spaced apart therefrom; dispensing a polymeric precursor into the mold cavity, whereupon said polymeric precursor is formed against the molding surface and the back face; and curing the polymeric precursor to form a polymeric encapsulant that encapsulates the integrated circuit die.”

24. Stated another way, there is a one-to-one correspondence between (i) the method steps of Claim 1 and (ii) the process used to make the Qualcomm Snapdragon Processor, as shown in the chart below. The column on the right describes *how* the Qualcomm Snapdragon Processor is assembled:

Claim limitations (i.e., method steps):	Factual assertions: the Qualcomm Snapdragon Processor is assembled according to ...
A method for forming a microelectronic package comprising:	a method for forming a microelectronic package comprising:
attaching an integrated circuit die to a substrate by a plurality of solder bump interconnections to form a preassembly, said integrated circuit die having an active face facing the substrate and spaced apart therefrom by a gap and a back face opposite the active face, said substrate including a die attach region and a surrounding region about the integrated circuit die, said plurality of solder bump interconnections extending across the gap and connecting the integrated circuit die and the substrate;	attaching an integrated circuit die to a substrate by a plurality of solder bump interconnections to form a preassembly, said integrated circuit die having an active face facing the substrate and spaced apart therefrom by a gap and a back face opposite the active face, said substrate including a die attach region and a surrounding region about the integrated circuit die, said plurality of solder bump interconnections extending across the gap and connecting the integrated circuit die and the substrate;

disposing a mold onto the preassembly such that the mold cooperates with the substrate to define a mold cavity that encloses the integrated circuit die, said mold having a molding surface that includes said surrounding region and an inner face facing the back face and spaced apart therefrom;	disposing a mold onto the preassembly such that the mold cooperates with the substrate to define a mold cavity that encloses the integrated circuit die, said mold having a molding surface that includes said surrounding region and an inner face facing the back face and spaced apart therefrom;
dispensing a polymeric precursor into the mold cavity, whereupon said polymeric precursor is formed against the molding surface and the back face; and	dispensing a polymeric precursor into the mold cavity, whereupon said polymeric precursor is formed against the molding surface and the back face; and
curing the polymeric precursor to form a polymeric encapsulant that encapsulates the integrated circuit die.	curing the polymeric precursor to form a polymeric encapsulant that encapsulates the integrated circuit die.

25. These factual assertions, made on information and belief, are made to satisfy the pleadings standards of Fed. R. Civ. P. 8(a), as applied and interpreted by *Twombly*, *Iqbal*, and their progeny. In accordance with Fed. R. Civ. P. 11, Plaintiff states, without waiving any applicable privileges or protections, that such assertions are based upon Plaintiff's pre-suit investigation and due diligence, in reliance on publicly available information, documents, and products and analysis derived therefrom. Plaintiff will provide infringement contentions in accordance with this Court's local rules and will supplement those contentions when Defendant provides the technical documentation required by the Court's local patent rules and as may be requested or subpoenaed in discovery requests made pursuant to the Federal Rules of Civil Procedure.

26. On information and belief, many of the products assembled and packaged by The ASE Group, including products that are offered for sale and/or sold by ASE in the U.S., are assembled and/or packaged, in whole or in part, using the patented processes recited in one or more claims of the '229 Patent. Such offers for sale and sales violate 35 U.S.C. § 271(g). Plaintiff expressly reserves the right to assert additional patents and additional claims and to identify

additional infringing products and additional entities who operate in concert with Defendant, in accordance with the Federal Rules of Civil Procedure, the Court's scheduling order and the Court's local rules.

27. Plaintiff has been damaged by Defendant's infringing conduct and will continue to be damaged unless Defendant is enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringer, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendant from committing the infringing acts.

COUNT TWO: INFRINGEMENT OF THE '571 PATENT

28. Plaintiff incorporates the above allegations as if set forth here in full.

29. The '571 Patent is valid and enforceable. Defendant does not have a license to practice the patented inventions of the '571 Patent.

30. On information and belief, and in violation of 35 U.S.C. §271(g), Defendant infringes at least Claims 1, 2, and 3 of the '571 Patent. For example, on information and belief, ASE imports, offers for sale, sells, and/or uses products made (by The ASE Group) according to a process that meets each and every limitation in Claim 1 of the '571 Patent, which recites: "A method for forming a microelectronic assembly including an integrated circuit component attached to a substrate by columnar interconnections, the method comprising: depositing metallic columns onto component bond pads disposed on an integrated circuit component, each said metallic column comprising a solder attachment surface remote from the component bond pad and a peripheral surface intermediate the solder attachment surface and the component bond pad,

each said metallic column formed of a first metal having a first melting temperature; depositing a solder plate onto each solder attachment surface, said solder plate being formed of a solder having a second melting temperature lower than the first melting temperature; oxidizing the peripheral surfaces of the metallic columns to inhibit wetting by solder during reflow; superposing the integrated circuit component onto a substrate such that each solder plate contacts a corresponding substrate bond pad on the substrate; and reflowing the solder by heating at a temperature above the second melting temperature and below the first melting temperature to bond the metallic column to the substrate bond pad and thereby attach the integrated circuit component to the substrate.”

31. Stated another way, there is a one-to-one correspondence between (i) the method steps of Claim 1 and (ii) the process used to make the Qualcomm Snapdragon Processor, as shown in the chart below. The column on the right describes *how* the Qualcomm Snapdragon Processor is assembled:

Claim limitations (i.e., method steps):	Factual assertions: the Qualcomm Snapdragon Processor is formed according to ...
A method for forming a microelectronic assembly including an integrated circuit component attached to a substrate by columnar interconnections, the method comprising:	a method for forming a microelectronic assembly including an integrated circuit component attached to a substrate by columnar interconnections, the method comprising:
depositing metallic columns onto component bond pads disposed on an integrated circuit component, each said metallic column comprising a solder attachment surface remote from the component bond pad and a peripheral surface intermediate the solder attachment surface and the component bond pad, each said metallic column formed of a first metal having a first melting temperature;	depositing metallic columns onto component bond pads disposed on an integrated circuit component, each said metallic column comprising a solder attachment surface remote from the component bond pad and a peripheral surface intermediate the solder attachment surface and the component bond pad, each said metallic column formed of a first metal having a first melting temperature;
depositing a solder plate onto each solder attachment surface, said solder plate being formed of a solder having a second melting	depositing a solder plate onto each solder attachment surface, said solder plate being formed of a solder having a second melting

temperature lower than the first melting temperature;	temperature lower than the first melting temperature;
oxidizing the peripheral surfaces of the metallic columns to inhibit wetting by solder during reflow;	oxidizing the peripheral surfaces of the metallic columns to inhibit wetting by solder during reflow;
superposing the integrated circuit component onto a substrate such that each solder plate contacts a corresponding substrate bond pad on the substrate; and	superposing the integrated circuit component onto a substrate such that each solder plate contacts a corresponding substrate bond pad on the substrate; and
reflowing the solder by heating at a temperature above the second melting temperature and below the first melting temperature to bond the metallic column to the substrate bond pad and thereby attach the integrated circuit component to the substrate.	reflowing the solder by heating at a temperature above the second melting temperature and below the first melting temperature to bond the metallic column to the substrate bond pad and thereby attach the integrated circuit component to the substrate.

32. These factual assertions, made on information and belief, are made to satisfy the pleadings standards of Fed. R. Civ. P. 8(a), as applied and interpreted by *Twombly*, *Iqbal*, and their progeny. In accordance with Fed. R. Civ. P. 11, Plaintiff states, without waiving any applicable privileges or protections, that such assertions are based upon Plaintiff's pre-suit investigation and due diligence, in reliance on publicly available information, documents, and products and analysis derived therefrom. Plaintiff will provide infringement contentions in accordance with this Court's local rules and will supplement those contentions when Defendant provides the technical documentation required by the Court's local patent rules and as may be requested or subpoenaed in discovery requests made pursuant to the Federal Rules of Civil Procedure.

33. On information and belief, many of the products made by The ASE Group, including products that are offered for sale and/or sold by ASE in the U.S., are made and/or assembled, in whole or in part, using the patented processes recited in one or more claims of the '571 Patent. Such offers for sale and sales violate 35 U.S.C. § 271(g). Plaintiff expressly reserves the right to assert additional patents and additional claims and to identify additional infringing

products and additional entities who operate in concert with Defendant, in accordance with the Federal Rules of Civil Procedure, the Court's scheduling order and the Court's local rules.

34. Plaintiff has been damaged by Defendant's infringing conduct and will continue to be damaged unless Defendant is enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringer, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendant from committing the infringing acts.

COUNT THREE: INFRINGEMENT OF THE '972 PATENT

35. Plaintiff incorporates the above allegations as if set forth here in full.

36. The '972 Patent is valid and enforceable. Defendant does not have a license to practice the patented inventions of the '972 Patent.

37. On information and belief, and in violation of 35 U.S.C. §271(a), Defendant infringes at least Claims 1, 2, and 5 of the '972 Patent. For example, on information and belief, ASE uses, offers for sale, and/or sells in the U.S. products that meet each and every limitation in Claim 1 of the '972 Patent, which recites: "A microelectronic package comprising: a carrier substrate that includes a die attachment face and carrier sides about the die attachment face, said die attachment face comprising a die attach region and a surrounding region about the die attach region; an integrated circuit die overlying the die attach region and spaced apart therefrom by a gap, said integrated circuit die including an active face facing the die attach region and a back face opposite the active face; a plurality of solder bump interconnections that extend across the gap and connect the integrated circuit die to the die attach region; and an encapsulant formed of

a singular polymeric body overlying the back face and molded against the surrounding region so as to encapsulate the die therein, said body comprising sides coextensive with said carrier sides.”

38. Stated another way, there is a one-to-one correspondence between (i) the patented apparatus of Claim 1 and (ii) the Qualcomm Snapdragon Processor offered for sale and sold by Defendant, as shown in the chart below. The column on the right describes *how* the Qualcomm Snapdragon Processor infringes, namely, by virtue of having each and every component recited in Claim 1, and by virtue of the fact that those components are connected and assembled in the configuration recited by Claim 1:

Claim limitations (for apparatus claims, these are sometimes referred to as “structural limitations):	Factual assertions about the Qualcomm Snapdragon Processor:
A microelectronic package comprising:	It is a microelectronic package that includes:
a carrier substrate that includes a die attachment face and carrier sides about the die attachment face, said die attachment face comprising a die attach region and a surrounding region about the die attach region;	a carrier substrate that includes a die attachment face and carrier sides about the die attachment face, said die attachment face comprising a die attach region and a surrounding region about the die attach region;
an integrated circuit die overlying the die attach region and spaced apart therefrom by a gap, said integrated circuit die including an active face facing the die attach region and a back face opposite the active face;	an integrated circuit die overlying the die attach region and spaced apart therefrom by a gap, said integrated circuit die including an active face facing the die attach region and a back face opposite the active face;
a plurality of solder bump interconnections that extend across the gap and connect the integrated circuit die to the die attach region; and	a plurality of solder bump interconnections that extend across the gap and connect the integrated circuit die to the die attach region; and
an encapsulant formed of a singular polymeric body overlying the back face and molded against the surrounding region so as to encapsulate the die therein, said body comprising sides coextensive with said carrier sides.	an encapsulant formed of a singular polymeric body overlying the back face and molded against the surrounding region so as to encapsulate the die therein, said body comprising sides coextensive with said carrier sides.

39. These factual assertions, made on information and belief, are made to satisfy the pleadings standards of Fed. R. Civ. P. 8(a), as applied and interpreted by *Twombly*, *Iqbal*, and

their progeny. In accordance with Fed. R. Civ. P. 11, Plaintiff states, without waiving any applicable privileges or protections, that such assertions are based upon Plaintiff's pre-suit investigation and due diligence, in reliance on publicly available information, documents, and products and analysis derived therefrom. Plaintiff will provide infringement contentions in accordance with this Court's local rules and will supplement those contentions when Defendant provides the technical documentation required by the Court's local patent rules and as may be requested or subpoenaed in discovery requests made pursuant to the Federal Rules of Civil Procedure.

40. On information and belief, numerous additional products offered for sale and/or sold by ASE in the U.S. infringe one or more claims of the '972 Patent. Such offers for sale and sales violate 35 U.S.C. § 271(a). Plaintiff expressly reserves the right to assert additional patents and additional claims and to identify additional infringing products and additional entities who operate in concert with Defendant, in accordance with the Federal Rules of Civil Procedure, the Court's scheduling order and the Court's local rules.

41. Plaintiff has been damaged by Defendant's infringing conduct and will continue to be damaged unless Defendant is enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringer, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendant from committing the infringing acts.

COUNT FOUR: INFRINGEMENT OF THE '743 PATENT

42. Plaintiff incorporates the above allegations as if set forth here in full.

43. The '743 Patent is valid and enforceable. Defendant does not have a license to practice the patented inventions of the '743 Patent.

44. On information and belief, and in violation of 35 U.S.C. §271(g), Defendant infringes at least Claims 1, 2, and 8 of the '743 Patent. For example, on information and belief, ASE imports, offers for sale, sells, and/or uses products made (by The ASE Group) according to a process that meets each and every limitation in Claim 1 of the '743 Patent, which recites: “A method for assembling ball-grid array (BGA) packages, comprising the steps of: providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board having a thickness, wherein N and M are greater than or equal to 2, each of the plurality of BGA substrates having a plurality of bond posts on one side and a plurality of contact pads on an opposite side; attaching a semiconductor die to each of the plurality of BGA substrates, the semiconductor die having a plurality of bond pads; encapsulating the semiconductor die with an encapsulant; curing the encapsulant; attaching conductive solder balls to each of the plurality of contact pads; and dividing the N by M array into separate BGA packages, and wherein each of the separate BGA packages is substantially planar.”

45. Stated another way, there is a one-to-one correspondence between (i) the method steps of Claim 1 and (ii) the process used to assemble the Qualcomm Snapdragon Processor, as shown in the chart below. The column on the right describes *how* the Qualcomm Snapdragon Processor is assembled:

Claim limitations (i.e., method steps):	Factual assertions: the Qualcomm Snapdragon Processor is assembled according to ...
A method for assembling ball-grid array (BGA) packages, comprising the steps of:	a method for assembling ball-grid array (BGA) packages, comprising the steps of:
providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board having a thickness, wherein N	providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board having a thickness, wherein N

and M are greater than or equal to 2, each of the plurality of BGA substrates having a plurality of bond posts on one side and a plurality of contact pads on an opposite side;	and M are greater than or equal to 2, each of the plurality of BGA substrates having a plurality of bond posts on one side and a plurality of contact pads on an opposite side;
attaching a semiconductor die to each of the plurality of BGA substrates, the semiconductor die having a plurality of bond pads;	attaching a semiconductor die to each of the plurality of BGA substrates, the semiconductor die having a plurality of bond pads;
encapsulating the semiconductor die with an encapsulant;	encapsulating the semiconductor die with an encapsulant;
curing the encapsulant;	curing the encapsulant;
attaching conductive solder balls to each of the plurality of contact pads; and	attaching conductive solder balls to each of the plurality of contact pads; and
dividing the N by M array into separate BGA packages, and wherein each of the separate BGA packages is substantially planar.	dividing the N by M array into separate BGA packages, and wherein each of the separate BGA packages is substantially planar.

46. These factual assertions, made on information and belief, are made to satisfy the pleadings standards of Fed. R. Civ. P. 8(a), as applied and interpreted by *Twombly*, *Iqbal*, and their progeny. In accordance with Fed. R. Civ. P. 11, Plaintiff states, without waiving any applicable privileges or protections, that such assertions are based upon Plaintiff's pre-suit investigation and due diligence, in reliance on publicly available information, documents, and products and analysis derived therefrom. Plaintiff will provide infringement contentions in accordance with this Court's local rules and will supplement those contentions when Defendant provides the technical documentation required by the Court's local patent rules and as may be requested or subpoenaed in discovery requests made pursuant to the Federal Rules of Civil Procedure.

47. On information and belief, many of the products assembled and packaged by The ASE Group, including products that are offered for sale and/or sold by ASE in the U.S., are assembled and/or packaged, in whole or in part, using the patented processes recited in one or more claims of the '743 Patent. Such offers for sale and sales violate 35 U.S.C. § 271(g). Plaintiff

expressly reserves the right to assert additional patents and additional claims and to identify additional infringing products and additional entities who operate in concert with Defendant, in accordance with the Federal Rules of Civil Procedure, the Court's scheduling order and the Court's local rules.

48. Plaintiff has been damaged by Defendant's infringing conduct and will continue to be damaged unless Defendant is enjoined from further infringement. Accordingly, upon finding for Plaintiff, the Court should award to Plaintiff damages adequate to compensate for the infringement, in an amount to be determined at trial, but in no event less than a reasonable royalty for the use made of the invention by the infringer, together with interest and costs as fixed by the Court. Further, upon judgment in favor of Plaintiff, the Court should permanently enjoin Defendant from committing the infringing acts.

DEMAND FOR JURY TRIAL

49. Plaintiff hereby demands a trial by jury on all issues.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully prays for entry of judgment as follows:

50. That Defendant has infringed one or more claims of the Patents-in-Suit.

51. That Plaintiff is entitled to, and should recover, all damages to which Plaintiff is entitled under 35 U.S.C. § 284, but in no event less than a reasonable royalty;

52. That Defendant be permanently enjoined from further infringement of the Patents-in-Suit;

53. That Defendant be ordered to provide an accounting;

54. That Plaintiff, as the prevailing party, shall recover from Defendant all taxable costs of court;

55. That Plaintiff shall recover from Defendant all pre- and post-judgment interest on the damages award, calculated at the highest interest rates allowed by law;

56. That this case is exceptional and that Plaintiff therefore shall recover its attorney's fees and other recoverable expenses, under 35 U.S.C. § 285; and

57. That Plaintiff shall recover from Defendant such other and further relief as the Court may deem appropriate.

Dated: October 28, 2016

WHITAKER CHALK SWINDLE
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