**UNITED STATES DISTRICT COURT**
**FOR THE SOUTHERN DISTRICT OF TEXAS**

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| JAMES B. GOODMAN,<br>Plaintiff,<br>vs.<br>ASUS COMPUTER INTERNATIONAL<br>Defendant. | **Civil Action No.**<br><br>**COMPLAINT FOR PATENT INFRINGEMENT AND**<br><br>**DEMAND FOR JURY TRIAL** |

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NOW COMES Plaintiff, JAMES B. GOODMAN ("Goodman" herein), through his attorney, and files this Complaint for Patent Infringement and Demand for Jury Trial against ASUS Computer International ("ACI" herein).

**PARTIES**

1. Goodman is an individual residing in the State of Texas.
2. On information and belief, the corporate office of ACI is located at 800 Corporate Way, Fremont, CA 94539.

## JURISDICTION AND VENUE

3. This is an action for patent infringement of United States Patent No. 6,243,315 (hereinafter "the '315 Patent") pursuant to the laws of the United States of America as set forth in Title 35 Sections 271 and 281 of the United States Code. This court has subject matter jurisdiction over this action pursuant to 28 U.S.C. Sec. 1338(a) and 28 U.S.C. Sec. 1331. Venue is proper in this judicial district under 28 U.S.C. § 1391(d) and 1400(b).

4. On information and belief, ACI has substantial sales and presence in this Federal Jurisdiction through offering to sell, and sales online through the internet, and through a multitude of local stores.

5. On information and belief, ACI is subject to this Court's specific and general personal jurisdiction, pursuant to due process and/or the Texas Long Arm Statute, due to at least its business presence in this Federal Judicial District, including substantial infringement in this Federal Judicial District.

6. On information and belief, ACI, directly and/or through intermediaries, advertise at least through web sites and other web sites, offers to sell, sold and/or distributed its products, and/or has induced the sale and use of infringing products in this Federal Judicial District.

7. In addition, and on information and belief, ACI is subject to the Court's general jurisdiction, including from regularly doing business, or soliciting business, or engaging in other persistent courses of conduct, and/or deriving substantial revenue from goods and services provided to individuals and businesses in this Federal Judicial District.

## BACKGROUND

8. ACI offers for sale directly through its web site and through a multitude of local stores in Houston, TX many computer related products, including desktop computers, laptop computers, servers, and the like.

9. Many of the ACI computer related products sold in this Federal Judicial District incorporate memory products known in the industry as DDR3, DDR3L, DDR4, and LPDDR4 memory products. Variations of these memory products such as the DDR3 memory product include DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600, and DDR3-1666 as well as DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1666. The use of the terms “DDR3", “DDR3L”, “DDR4", and “LPDDR4" to include in the designation of a memory product requires the performance of the memory product to comply with the respective industry standards for performance, and operations.

10. The standards published by the Joint Electron Device Engineering Council Solid State Technology Association (“JEDEC”) state for the respective DDR3, DDR3L, DDR4, and LPDDR4 memory products and their variation: "No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met."

11. On information and belief, the use of the terms “DDR3", “DDR3L”, “DDR4", and “LPDDR4" and variations thereof implies that the respective memory products complies with the corresponding JEDEC Standards.

12. Therefore, the DDR3, DDR3L, DDR4, and LPDDR4 memory products and their variations must operate in compliance with the respective standards established by the JEDEC Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201.

13. Any memory product identified as being a DDR3 memory product or a variation thereof including the term “DDR3" must comply with JEDEC Standard JESD79-3F.

14. Any memory product identified as being a DDR3L memory product or a variation thereof including the term “DDR3L" must comply with both JEDEC Standard JESD79-3F and JESD79-3-1A.01.

15. Any memory product identified as being a DDR4 memory product or a variation thereof including the term “DDR4" must comply with JEDEC Standard JESD79-4A.

16. Any memory product identified as being a LPDDR4 memory product or a variation thereof including the term “LPDDR4" must comply with JEDEC Standard JESD209-4A.

17. On information and belief, the JEDEC Standards for DDR3, DDR3L, DDR4, and LPDDR4 memory products have several relevant operating capabilities in common when installed in an ACI computer related product, for example: (a) Each memory product has at least two banks of volatile memory, and this is the equivalent of a plurality of volatile solid state memory devices under the doctrine of equivalents; (b) A first external device (supplied by ACI computer related product) connected to the memory product can provide signals for selectively electrically isolating the address and control lines so that signals on the address and control lines do not reach the memory devices; and (c) A second external device (supplied by ACI computer related product) connected to the memory product can determine when the memory system is not being accessed and can initiate a low power for the memory system wherein the first external device isolates the memory devices and places the memory devices in self refresh mode, thereby reducing the electrical energy drawn from the electrical power supply of the ACI computer related product.

18. On information and belief, the aforementioned ACI computer related products incorporating a DDR3, DDR3L, DDR4, or LPDDR4 provide the aforementioned first and second external devices in order to take advantage of the respective operating specification of the memory products, including the low power mode which saves electrical energy while protecting the memory product against potential signals which could damage or corrupt the stored data.

19. The following is a Claim Chart for Claim 1 of the '315 Patent for the DDR3 memory product:

**CLAIM CHART AND ASSOCIATED CONSTRUCTION**

| **U.S. Patent No. 6,243,315** | **ACI COMPUTER RELATED SYSTEM HAVING AN INSTALLED DDR3 MEMORY PRODUCT AND PROVIDING THE AFOREMENTIONED FIRST AND SECOND EXTERNAL DEVICES** |
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| Claim 1. A memory system for use in a computer system, said memory system comprising: | A "memory system" can be construed to be "**a system capable of retaining data**". The JEDEC Standard JESD79-3F specification at p. 18, Sec. 3.2, "The DDR3 SDRAM is a high-speed dynamic random-access memory ...". On the same page, "an interface designed to transfer two data words per clock cycle". The DDR3 memory product retains data.<br><br>Thus, this memory product is within the preamble description. |

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| a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and | A "memory device" can be construed to be an "**integrated circuit or chip**"; and "a plurality of volatile solid state memory devices" can be construed to be "**two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while a electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information**".<br><br>The JEDEC Standard JESD79-3F at p. 109, Sec. 6.1 states the absolute maximum DC Ratings. P. 111, Sec. 7.1 shows the recommended DC Operating Conditions with a minimum and maximum for the DC voltages.<br><br>The JEDEC Standard JESD79-3F in at p. 77 refers to the memory module as being a "chip". See Sec. 4.15.<br><br>The JEDEC Standard JESD79-3F at p. 18, Sec. 3.2 states, "The DDR3 SDRAM is a high-speed dynamic random-access internally configured a an eight-bank DRAM." The second paragraph describes how a bank can be selected. See the Command Truth Table at p. 33, Sec. 4.1, and NOTE 3 explains that "BA" is for the selection of a bank being operated upon. Hence, the DDR3 has eight memory banks and the equivalents of a plurality of solid state memory devices.<br><br>On information and belief, a DRAM is volatile memory and that means a voltage in a specific range must be applied to operate acceptably as pointed out above. |
| capable of being placed in a self refresh mode; | The JEDEC Standard JESD79-3F shows that the DDR3 is capable of being refreshed at p. 13, Sec. 2.10 for CKE, (CKE0), (CKE1) "Self-Refresh operations (all banks idle)"; p. 17, Sec. 3.1 on the diagram; p. 31, Sec. 3.4.4.1 entitled "Partial Array Self-Refresh (PASR)"; p. 35, Sec. 4.2 shows an entry for "Self-Refresh"; p. 46, Sec. 4.9.0.1 entitled, "Auto Self-Refresh"; and |
| said memory devices having address lines and control lines; | |

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| | and p. 79, Sec. 4.16 entitled "Self-Refresh Operation". |
| a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and | JEDEC Standard JESD79-3F at p. 81, Sec. 4.17.1 entitled "Power-Down Entry and Exit" discloses a power-down operation. The description states, "Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cylce(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and receivers after tCPDED has expired. The text also states, "In power-down mode, CKE low, RESET# high, and stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are "Don't Care." The input signals are address and control signals are related to the CK# input noted at p. 13, Sec. 2.10, where it is stated, "All Address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. |
| a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system. | The power-down is due to an input signal from the second external device as pointed out at P. 13, Sec. 2.10. The device generating the input signal for the power-down functions like the claimed memory access enable control device.<br>JEDEC Standard JESD79-3F , Sec. 4.17.1 states, " Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operations are in progress. |

20. The respective DDR3, DDR3L, DDR4, and LPDDR4 memory products are typically incorporated into the ACI computer related product on what is known in the industry as a "motherboard", and other components on the motherboard provide subsystems to monitor activity in the mounted memory product, initiate the reduced power down mode, to inhibit responses in the memory products on the motherboard, and other requirements of the respective JEDEC standard.

21. Goodman has granted limited, non-exclusive licenses to the following companies: Patriot Memory, LLC, Nan Ya Technology Corporation USA, ON Semiconductor Corporation, Intel Corporation, Numonyx B.V., Atmel Corporation, Spansion, Inc., Hynix Semiconductor America Inc., NanoAmp Solutions, Inc., Integrated Silicon Solutions Inc., Fujitsu, Samsung, Sharp Electronics Corporation, Toshiba Corporation, Elpida, Micron Technology, Inc., Infineon Technologies North America Corp, and Smart Modular Technologies Inc.

**COUNT ONE**
**(DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,243,315)**

22. Plaintiff Goodman repeats and incorporates herein the allegations contained in paragraphs 1 through 24 above.

23. On June 5, 2001, the ‘315 Patent entitled "COMPUTER MEMORY SYSTEM WITH A LOW POWER MODE", was duly and legally issued to James B. Goodman, as the sole patentee.

24. Plaintiff Goodman is the sole owner of the ‘315 Patent, and has standing to bring this action.

25. All of the limitations of Claim 1 of the ‘315 Patent are present in ACI related computer products incorporating at least one DDR3, DDR3L, DDR4, or LPDDR4 memory product offered for sale, and being sold directly or indirectly by ACI in this Federal Judicial District.

26. All of the limitations of claim 1 of the ‘315 Patent are present in ACI computer related products including offered for offered for sale, and sold directly or indirectly by ACI.

27. ACI is infringing at least claim 1 of the ‘315 Patent literally, or under the doctrine of equivalents in this Federal Judicial District.

**JURY DEMAND**

Pursuant to Fed. R. Civ. P. 38(b), Plaintiff hereby demands a jury trial as to all issues in this lawsuit.

**PRAYER FOR RELIEF**

THEREFORE, Plaintiff respectfully requests this Court to:

a. enter judgment for Plaintiff on Claim 1 of the '315 Patent for patent infringement, either literally, and/or under the doctrine of equivalents;

b. order that an accounting be had for the damages caused to the Plaintiff by the infringing activities of the ACI;

c. enter an injunction to prohibit ACI directly or indirectly from offering for sale, or selling infringing products;

d. award Plaintiff interest and costs; and

e. award Plaintiff such other and further relief as this Court may deem just and equitable.

THE PLAINTIFF

JAMES B. GOODMAN

Date: November 2, 2016

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