IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

NORTH STAR INNOVATIONS INC., Plaintiff, v. TOSHIBA CORPORATION AND TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC. Defendants.	C.A. No. **JURY DEMANDED**

COMPLAINT

Under Fed. R. Civ. P. 15(a)(1), Plaintiff North Star Innovations Inc. ("North Star") complains of Defendants Toshiba Corporation and Toshiba America Electronic Components, Inc. (collectively, "Toshiba") as follows:

JURISDICTION AND VENUE

1. Title 28 of the United States Code Section 1338(a) confers subject matter jurisdiction on this Court because Defendants have infringed Plaintiff's patents. The Patent Act of 1952, as amended, 35 U.S.C. § 271, *et seq.*, makes patent infringement actionable through a private cause of action.

2. Defendants have transacted business in the State of Delaware, and in this judicial district by making, using, selling, offering to sell and distributing products in this judicial district that violate North Star's patents. Accordingly, this Court has personal jurisdiction over Defendants.

3. Venue is proper in the District of Delaware under the general federal venue statute, 28 U.S.C. § 1391(d), and under the specific venue provision relating to patent infringement cases, 28 U.S.C. § 1400(b).

PARTIES

4. North Star is a Delaware corporation with its principal place of business at Plaza Tower, 600 Anton Boulevard, Suite 1350, Costa Mesa, CA 92626. North Star is a

subsidiary of Wi-LAN Technologies Inc. North Star is the assignee of and owns all right, title and interest in and has standing to sue for infringement of United States Patent No. 7,171,526 ("the '526 Patent") (attached as Exhibit A), entitled Memory Controller Useable in a Data Processing System, and United States Patent No. 7,573,416 ("the '416 Patent") (attached as Exhibit B), entitled Analog to Digital Converter with Low Power Control. The '526 Patent issued January 30, 2007, and the '416 Patent issued August 11, 2009.

5. Toshiba Corporation is a Japanese multinational company with its principal place of business at 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan. Toshiba Corporation has previously and is presently selling and importing into the United States laptops and memory products that infringe one or more claims of the '526 Patent, and one or more claims of the '416 Patent.

6. Toshiba America Electronic Components, Inc. is an independent operating company with its principal place of business at 9740 Irvine Boulevard, Irvine, CA 92618. Toshiba America Electronic Components, Inc. has previously and is presently using, selling, offering for sale, and importing into the United States laptops and memory products that infringe one or more claims of the '526 Patent, and one or more claims of the '416 Patent. Defendants have also infringed the '526 Patent and '416 Patent through acts of inducement in violation of 35 U.S.C. § 271.

BACKGROUND

7. North Star is the owner of patent rights, which cover commercially significant technologies related to memory controllers and analog to digital converters. The'526 Patent covers a memory controller useable within a data processing system, and the '416 Patent covers analog to digital converters with low power control.

8. Toshiba Corporation designs, manufacture, sells and imports into the United States products that infringe the '526 Patent and the '416 Patent. Toshiba's primary customer is Toshiba America Electronic Components, Inc., which then distributes the products throughout the United States.

9. Toshiba America Electronic Components, Inc. imports, sells, offers for sale and uses products that infringe the ’526 Patent and the ’416 Patent. Toshiba imports products

INFRINGEMENT OF THE ’526 PATENT

10. Defendants have infringed and continue to infringe at least claims 15 and 17 of the ’526 Patent, in violation of 35 U.S.C. § 271 through, among other activities, Toshiba Corporation’s importing and selling of, and Toshiba America Electronic Components, Inc.’s importing, using, offering to sell, and selling the Toshiba Protégé Z30 Ultrabook Laptop, a representative infringing product. A marketing photo with technical specifications of the Toshiba Z30 Ultrabook Laptop is shown below.

Source: http://us.toshiba.com/computers/laptops/portege/Z30/Z30-001011 (last visited November 14, 2016)

A photo showing all the items provided in a purchased Toshiba Protégé Z30 Ultrabook Laptop is shown below.

All Items

Source: TechInsights product teardown

Different views of the Toshiba Protégé Z30 Ultrabook Laptop are shown below, including a Front, Top, Bottom, and ID Tag.

Front

Top

Bottom

ID Tag

Source: TechInsights product teardown

11. Defendants' infringing technology and products include without limitation their laptop computers which have memory controllers usable within a data processing system, including, for example, the Toshiba Protégé Z30 Ultrabook Laptop. Defendants'

infringement may include additional products and technologies (to be determined in discovery) marketed or used by Defendants.

12. Claim 15 is an exemplary infringed claim. Its preamble states: "A data processing system, comprising." Toshiba's products, such as its Protégé Z30 Ultrabook Laptop, comprise a circuit with a data processing system. FIG. 1 of the '526 Patent is shown below. The data processing circuit of Toshiba's Protégé Z30 Ultrabook Laptop closely resembles that of FIG. 1.

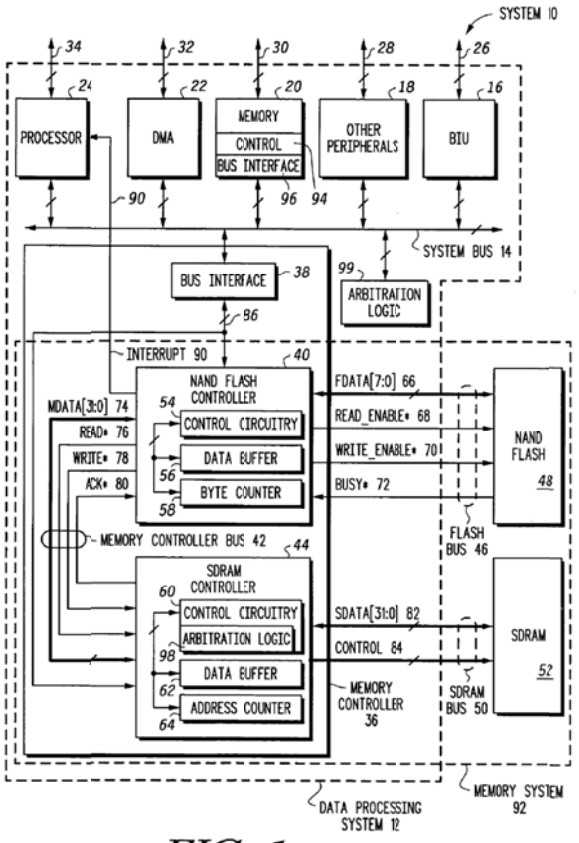
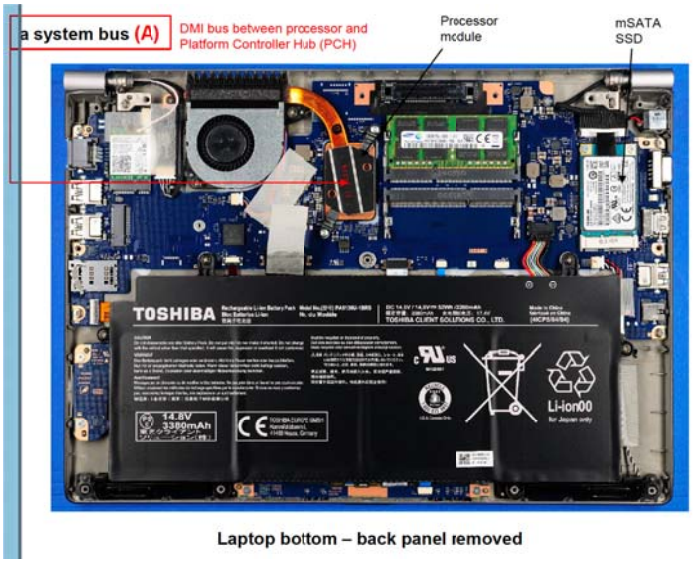


FIG. 1

13. After the preamble, the first limitation of claim 15 states: "a system bus (A)." The limitations and sublimitations of claim 15 are labeled (A) through (G) for analysis purposes. Toshiba's products, such as its Toshiba Protégé Z30 Ultrabook Laptop contain this first limitation. Shown below is a photo of the Z30 laptop bottom

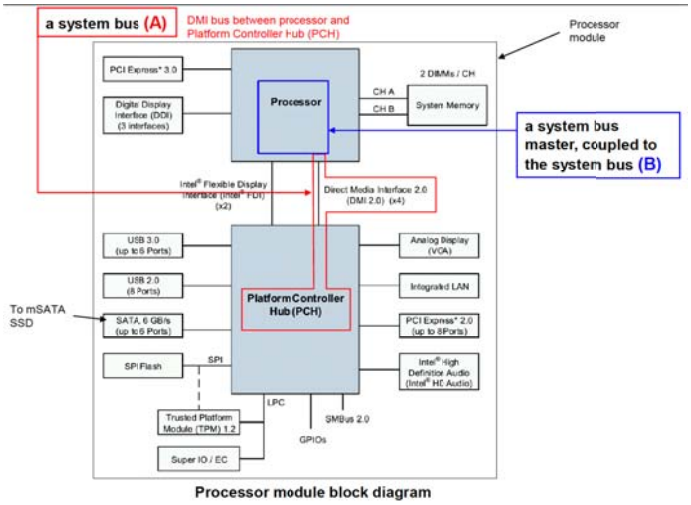
with back panel removed. The system bus is shown as the Direct Media Interface (DMI) bus between the processor and the platform controller hub (PCH).



Laptop bottom – back panel removed

Source: TechInsights product teardown

The DMI system bus is also depicted in the below processor module block diagram. As shown, the Direct Media Interface 2.0 (DMI 2.0) (x4) system bus is shown between the processor and Platform Controller Hub (PCH):

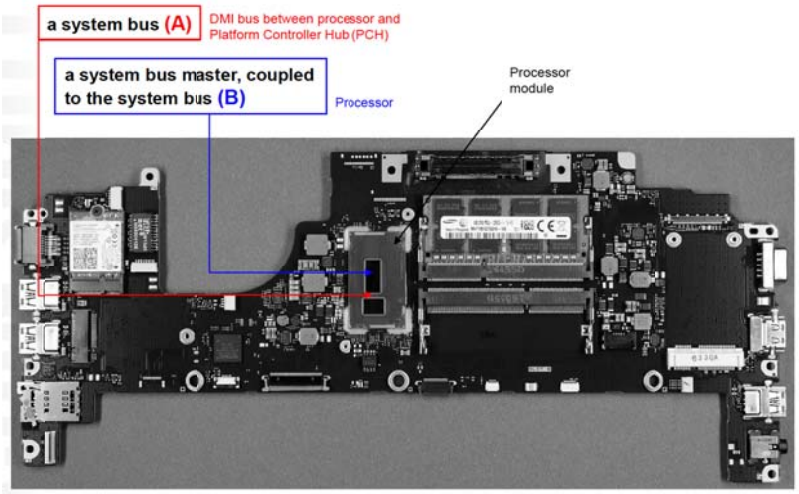


Processor module block diagram

Source: Desktop 5th Generation Intel Core Processor Family Datasheet – Volume 1 of 2, June 2015.

14. After the first limitation, the second limitation of claim 15 states: "a system bus master, coupled to the system bus (B)." Toshiba's products, such as its

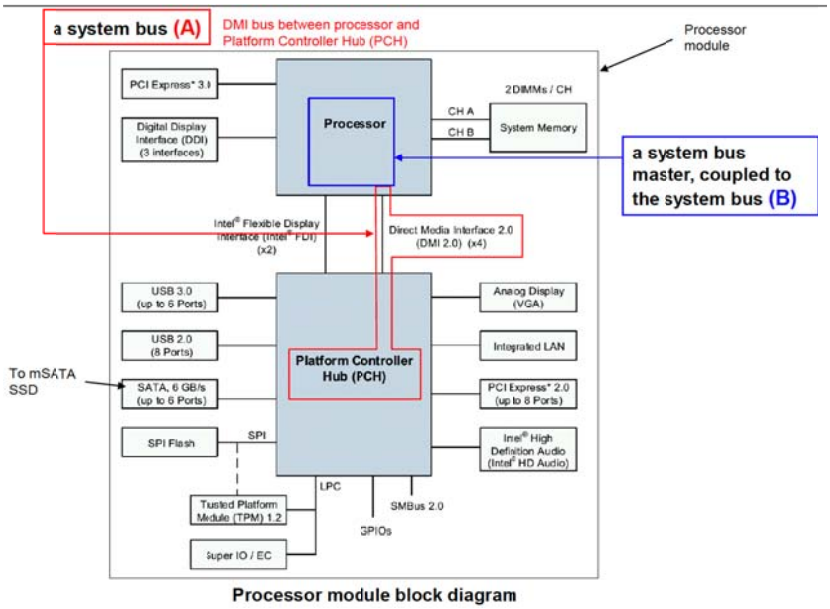
Toshiba Protégé Z30 Ultrabook Laptop contain this second limitation. A processor is the system bus master. The processor is depicted in the below photo of the main board top with the cooling module and SSD removed.



Main board top – cooling module and SSD removed

Source: TechInsights product teardown

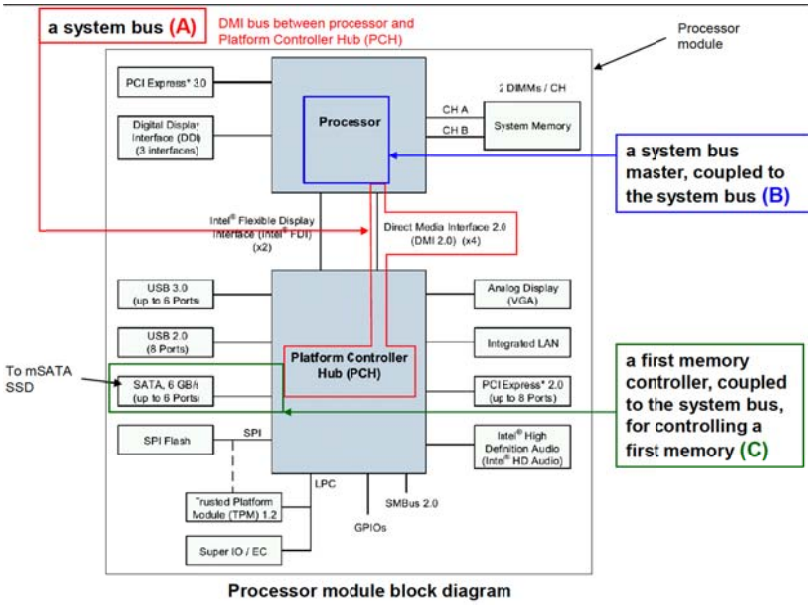
The processor is also shown in the below processor module block diagram:



Processor module block diagram

Source: Desktop 5th Generation Intel Core Processor Family Datasheet – Volume 1 of 2, June 2015.

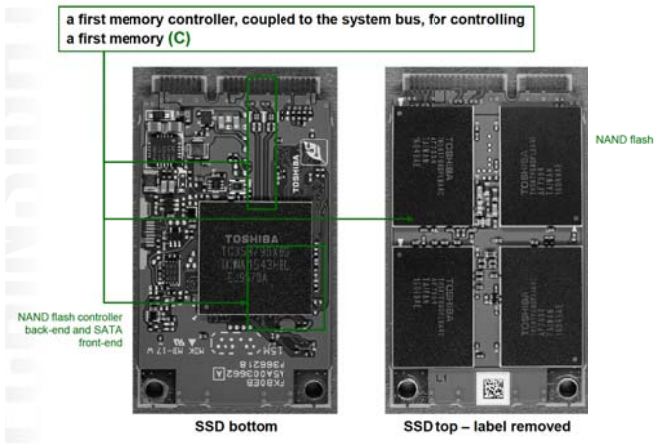
15. After the second limitation, the third limitation of claim 15 states: "a first memory controller, coupled to the system bus, for controlling a first memory (C)." Toshiba's products, such as its Toshiba Protégé Z30 Ultrabook Laptop contain this third limitation. In the diagram below, the first memory controller is the "SATA, 6 GB/s (up to 6 Ports)," which is coupled to the system bus and controls a first memory of the laptop. The acronym SATA stand for Serial Advanced Technology Attachment.



Processor module block diagram

Source: Desktop 5th Generation Intel Core Processor Family Datasheet – Volume 1 of 2, June 2015.

The NAND flash controller back-end and SATA front-end memory controller are depicted in the below solid state drive (SSD) diagrams, both on SSD bottom (left) and SSD top – label removed (right).



Source: TechInsights product teardown

The NAND controller and NAND memory control the first memory:

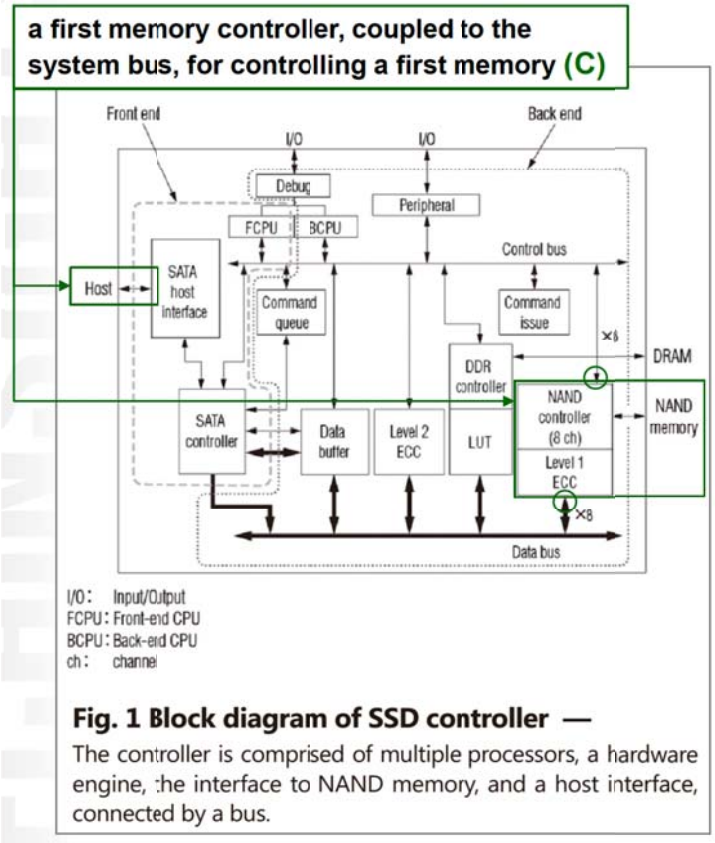
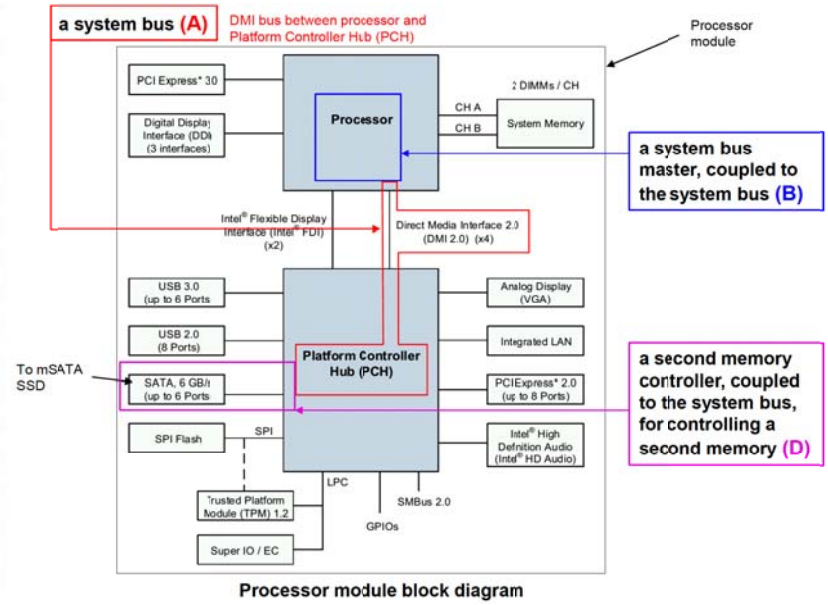


Fig. 1 Block diagram of SSD controller —
The controller is comprised of multiple processors, a hardware engine, the interface to NAND memory, and a host interface, connected by a bus.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

16. After the third limitation, the fourth limitation of claim 15 states: "a second memory controller, coupled to the system bus, for controlling a second memory (D)." Toshiba's products, such as its Toshiba Protégé Z30 Ultrabook Laptop contain this

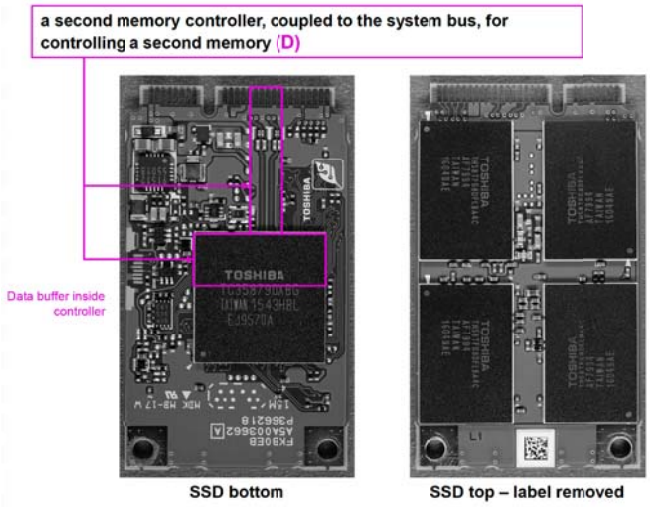
fourth limitation. In the diagram below, the second memory controller is the "SATA, 6 GB/s (up to 6 Ports)," which is coupled to the system bus and controls a second memory of the laptop.



Processor module block diagram

Source: Desktop 5th Generation Intel Core Processor Family Datasheet – Volume 1 of 2, June 2015

In particular, the second memory controller is the data buffer inside the controller. This is shown below, in the SSD bottom photo on the left.



SSD bottom SSD top – label removed

Source: TechInsights product teardown

The second memory controller is further illustrated in the below diagram as being the "Data buffer" and "Host":

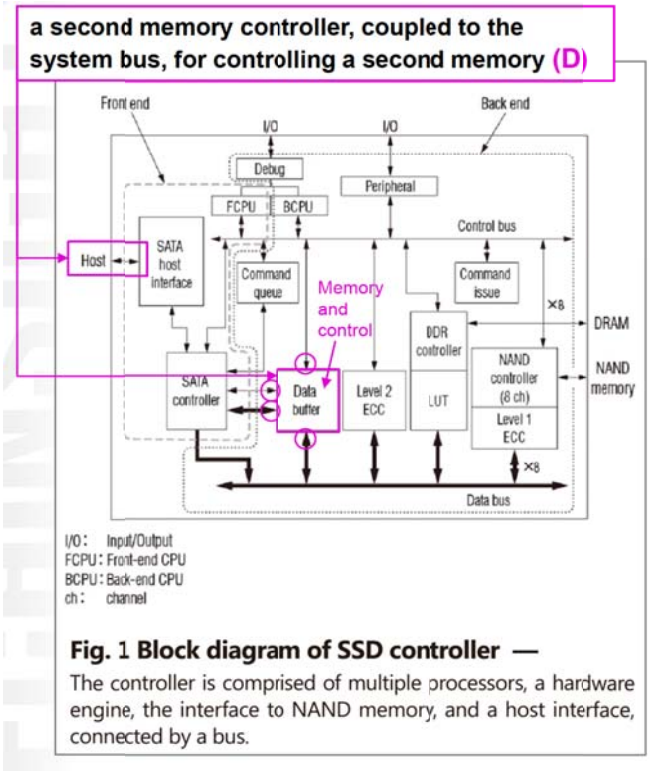


Fig. 1 Block diagram of SSD controller —
The controller is comprised of multiple processors, a hardware engine, the interface to NAND memory, and a host interface, connected by a bus.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

The basic processing flow for read and write operations are described below (highlighted portions describing the second memory controller):

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Next, we describe the basic processing flow for read and write operations. A SATA read command from the host passes through the front end of the controller to the command queue. A read command that has entered the command queue is sent to the LUT to get the mapping between the LBA specified read address and the NAND memory physical address. Then the read command is sent to the appropriate NAND controller channel corresponding to the physical address, and the data is read out. The data read is transferred to the data buffer, and then sent to the host through the front end.

A write command from the host passes through the front end, and the write data, LBA, and data attributes are sent to the data buffer. Next, the LUT provides the mapping between LBA and NAND memory physical address, and data is written from the data buffer to the NAND memory location pointed by the physical address. Level 1 and level 2 error-correcting codes are generated and written with the write data to NAND memory.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

17. After the fourth limitation, the fifth limitation of claim 15 states: "arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory (E)." Toshiba's products, such as its Toshiba Protégé Z30 Ultrabook Laptop contain this fifth limitation. The arbitration logic is depicted in the diagram below as being, in combination, the Host, the Back-end CPU (BCPU), the SATA controller, the Data Buffer, the NAND controller (8 ch), and Level 1 FCC.

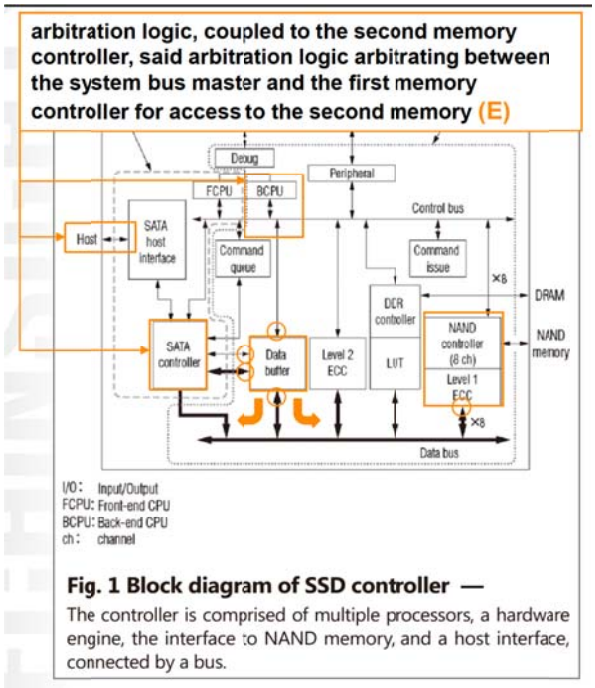
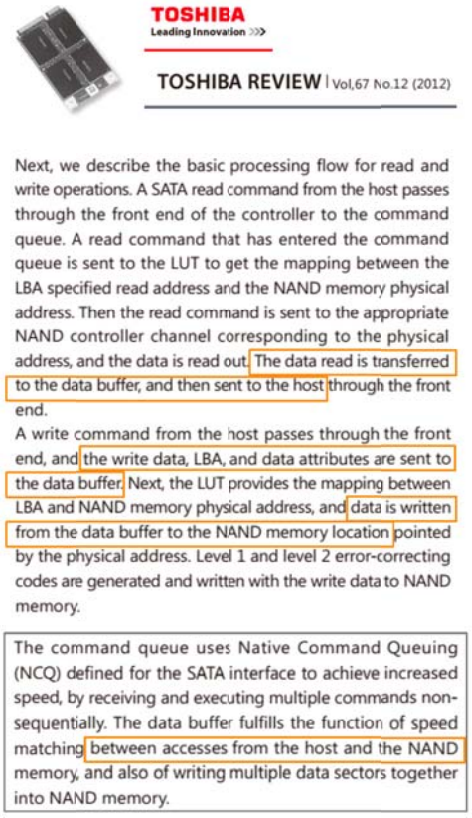


Fig. 1 Block diagram of SSD controller —
The controller is comprised of multiple processors, a hardware engine, the interface to NAND memory, and a host interface, connected by a bus.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

The basic processing flow for read and write operations are described below (highlighted portions describing the arbitration logic):



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A write command from the host passes through the front end, and the write data, LBA, and data attributes are sent to the data buffer. Next, the LUT provides the mapping between LBA and NAND memory physical address, and data is written from the data buffer to the NAND memory location pointed by the physical address. Level 1 and level 2 error-correcting codes are generated and written with the write data to NAND memory.

The command queue uses Native Command Queuing (NCQ) defined for the SATA interface to achieve increased speed, by receiving and executing multiple commands non-sequentially. The data buffer fulfills the function of speed matching between accesses from the host and the NAND memory, and also of writing multiple data sectors together into NAND memory.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

18. After the fifth limitation, the sixth and final limitation of claim 15 states: "and a memory controller bus operating independent of the system bus, said memory controller bus being coupled to the first memory controller and to the second memory controller (F), said memory controller bus transferring data between the first memory controller and the second memory controller (G)." Toshiba's products, such as its Toshiba Protégé Z30 Ultrabook Laptop contain this sixth limitation as shown by the "Data bus" in the diagram below.

a memory controller bus operating independent of the system bus, said memory controller bus being coupled to the first memory controller and to the second memory controller (F)

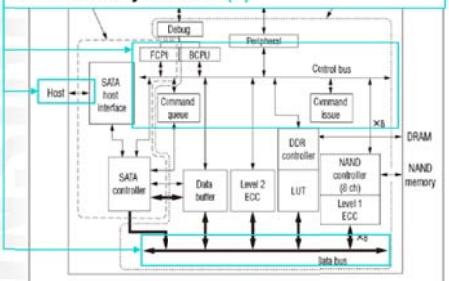

Fig. 1 Block diagram of SSD controller —
The controller is comprised of multiple processors, a hardware engine, the interface to NAND memory, and a host interface, connected by a bus.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

The discussion of pipelined command processing as meeting sublimitation (F) is discussed below (emphasis by highlighting):

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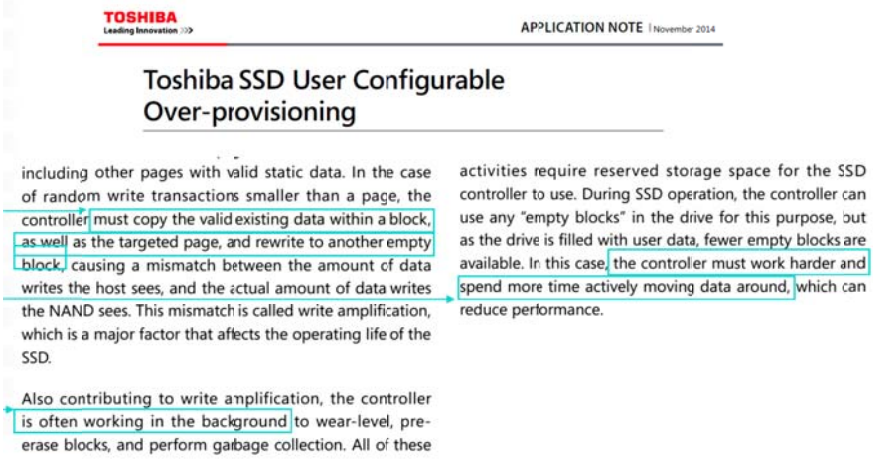
The command queue uses Native Command Queuing (NCQ) defined for the SATA interface to achieve increased speed, by receiving and executing multiple commands non-sequentially. The data buffer fulfills the function of speed matching between accesses from the host and the NAND memory, and also of writing multiple data sectors together into NAND memory.

To achieve high data transfer rates, Toshiba's controller implements pipelined command processing. In other words, the controller processing is internally divided into a progression of blocks, through which each command is passed.. At this point, the amount of processing allocated to each block is approximately equal. The input/output units of each block are provided with internal buffers so that when the processing of a command completes in a block, it is passed to the following block and another command passed from the preceding block can start processing.
This means that the blocks can simultaneously process different commands and that the overall system can process multiple commands in parallel. In Fig. 2, the pipeline concept is shown with an example of how multiple read commands are processed continuously.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

Further documentation discussing sublimitation (F) includes a discussion of Toshiba SSD User Configurable Over-provisioning (relevant portions highlighted):



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APPLICATION NOTE November 2014

Toshiba SSD User Configurable Over-provisioning

including other pages with valid static data. In the case of random write transactions smaller than a page, the controller must copy the valid existing data within a block, as well as the targeted page, and rewrite to another empty block, causing a mismatch between the amount of data writes the host sees, and the actual amount of data writes the NAND sees. This mismatch is called write amplification, which is a major factor that affects the operating life of the SSD.

Also contributing to write amplification, the controller is often working in the background to wear-level, pre-erase blocks, and perform garbage collection. All of these activities require reserved storage space for the SSD controller to use. During SSD operation, the controller can use any "empty blocks" in the drive for this purpose, but as the drive is filled with user data, fewer empty blocks are available. In this case, the controller must work harder and spend more time actively moving data around, which can reduce performance.

Source: Toshiba SSD User Configurable Over-provisioning, Application Note, November 2014

19. The Toshiba Protégé Z30 Ultrabook Laptop contains sublimitation (G), said memory controller bus transferring data between the first memory controller and the second memory controller, as illustrated below as data being transferred between the NAND controller and the Data buffer.

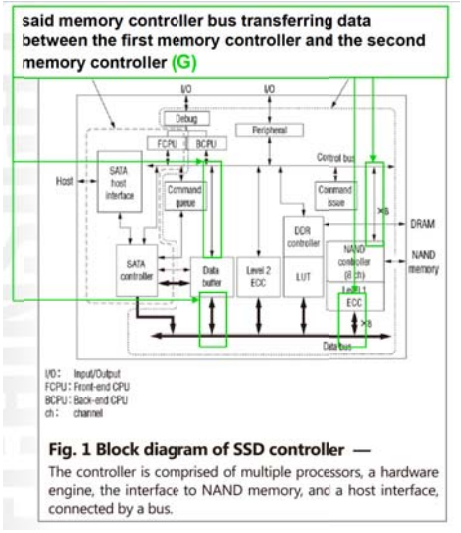
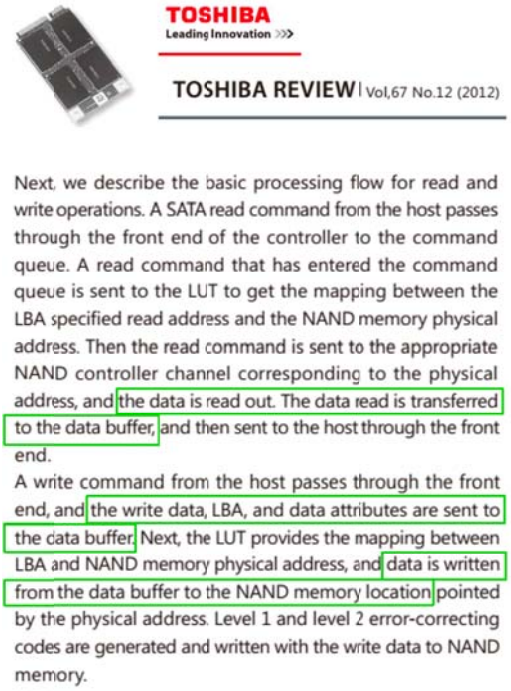


Fig. 1 Block diagram of SSD controller —
The controller is comprised of multiple processors, a hardware engine, the interface to NAND memory, and a host interface, connected by a bus.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

A description of the data being transferred between the data buffer and the NAND is provided in Toshiba product documentation:



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Next, we describe the basic processing flow for read and write operations. A SATA read command from the host passes through the front end of the controller to the command queue. A read command that has entered the command queue is sent to the LUT to get the mapping between the LBA specified read address and the NAND memory physical address. Then the read command is sent to the appropriate NAND controller channel corresponding to the physical address, and the data is read out. The data read is transferred to the data buffer, and then sent to the host through the front end.

A write command from the host passes through the front end, and the write data, LBA, and data attributes are sent to the data buffer. Next, the LUT provides the mapping between LBA and NAND memory physical address, and data is written from the data buffer to the NAND memory location pointed by the physical address. Level 1 and level 2 error-correcting codes are generated and written with the write data to NAND memory.

Source: High-Performance Control Technologies for SSDs Using 19 nm Generation NAND Flash Memory for PC Market, Toshiba Review Vol,67 No.12 (2012)

20. As a direct and proximate consequence of Defendants' infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

21. Defendants' infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further importation, use, sale and/or offer for sale of products that come within the scope of the '526 Patent.

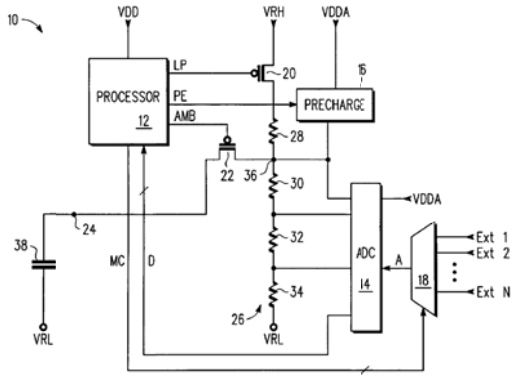
PATENT INFRINGEMENT OF THE '416 PATENT

22. North Star hereby incorporates paragraphs 1-21 above by reference.

23. Defendants have infringed and continue to infringe at least claims 1, 3, and 5 of the ’416 Patent, in violation of 35 U.S.C. § 271 through, among other activities, Toshiba Corporation’s importing and selling, and Toshiba America Electronic Components, Inc.’s importing, using, offering to sell, and selling the Toshiba THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash.

24. Defendants’ infringing products include without limitation their memory products, including, for example, the Toshiba THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash and other memory products. Defendants’ infringement may include additional products and technologies (to be determined in discovery) marketed or used by Defendants.

25. Claim 1 is an exemplary infringed claim. Its preamble states: “A circuit comprising”. Toshiba’s THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash is a circuit. The circuit of the THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contains all the elements of claim 1, as discussed below. The FIGURE of the ’416 Patent, shown below, is a block diagram view of a circuit representing an analog to digital converter with low power control. The circuit of Toshiba’s THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash closely resembles the circuit shown in the FIGURE of the ’416 Patent.



FIGURE

26. After the preamble, the first limitation of claim 1 states: "a reference voltage generating circuit (A) having an input and an output terminal for providing a reference voltage (B)." Sublimitations of claim 1 are labeled (A) through (M) for analysis purposes. Toshiba's products such as the THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contain this limitation. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contains sublimitation (A), a reference voltage generation circuit, by virtue of the series of transistors and resistors located in the middle portion of the VG_VR3A (the VREG3 Voltage Regulator), including the RES 25 represented as FIG. 7.2.11.2. *See* Figure 3: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contains sublimitation (B), an input and an output terminal for providing a reference voltage (B), through the terminal by which the VG_VR3A port is connected to the reference voltage generation circuit. *See* Figure 3: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101.

27. After the first limitation, the second limitation of claim 1 states: "a first switch (C) having a first terminal coupled to a first power supply voltage terminal (D), a second terminal coupled to the input and the output terminal (E) of the reference voltage

generating circuit, and a control terminal for receiving a first control signal (F)." Toshiba's products such as the THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contain this limitation.

28. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash has a first switch (C), the VH3A switch of the VREG3 Voltage Regulator. *See* Figure 3: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. The first switch has a first terminal coupled to a first power supply voltage terminal (D) through the IREF5 port of the VREG3 Voltage Regulator. *See* Figure 3: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. The first terminal coupled to a first power supply voltage terminal (D) is also shown via the VH3A and IREF5 ports. *See* Figure 4: Current Source, Source: Figure 7.2.18, report ID# 0615-39600-O-5CV-101; *see also* Figure 5: Charge Pumps Block, Source: Figure 7.1.4.3, report ID#: 0615-39600-O-5CV-101. The first switch has a second terminal coupled to the input and the output terminal (E) through the terminal connecting the VH3A block and the reference voltage generation circuit. *See* Figure 3: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. The first switch has a control terminal for receiving a first control signal (F) through the OUT line signal on the LEVEL SHIFTER 2 circuit, corresponding to FIG. 8.178. *See* Figure 3: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101.

29. After the second limitation, the third limitation of claim 1 states: "a second switch (G) having a first terminal coupled to the input and the output terminal (H) of the reference voltage generating circuit, a second terminal (I), and a control terminal for receiving a second control signal (J)." Toshiba's products such as the THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contain this limitation.

30. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash has a second switch (G) as the transistor on the line signal connecting the reference voltage generation circuit and the VG_VR3A port of the VREG3 Voltage Regulator. *See* Figure 6: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-

101. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash has a first terminal coupled to the input and the output terminal (H) via the line signal connecting the input and output terminal for providing a reference voltage (B) and the second switch (G). *See* Figure 6: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash has a second terminal (I) via the line signal between second switch (G) and the VG_VR3A port. *See* Figure 6: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash has a control terminal for receiving a second control signal (J) via the line signal between the Level Shifter 2 represented in FIG. 8.178 and the second switch (G). *See* Figure 6: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101.

31. After the third limitation, the fourth and final limitation of claim 1 states: "and a capacitive element (K) having a first plate electrode coupled to the second terminal of the second switch (L), and a second plate electrode coupled to a second power supply voltage terminal (M)". Toshiba's products such as the THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash contain this limitation.

32. The THGBX6T0T8LLFXF 15 nm TLC 128 Gbit NAND Flash has a capacitive element (K) between the line signal connecting the input and output terminal for providing a reference voltage (B), the second switch (G), and the VG_VR3A port. *See* Figure 7: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. This capacitive element (K) has a first plate electrode coupled to the second terminal of the second switch (L) via the line signal connecting the second switch (G) and the capacitive element (K). *See* Figure 7: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101. This capacitive element (K) has a second plate electrode coupled to a second power supply voltage terminal (M) via the VSS of the capacitive element (K). *See* Figure 7: VREG3 Voltage Regulator, Source: Figure 7.2.11, report ID#: 0615-39600-O-5CV-101.

33. As a direct and proximate consequence of Defendants' infringement, North Star has been, is being and, unless such acts and practices are enjoined by the Court, will continue to be injured in its business and property rights, and has suffered, is suffering, and will continue to suffer injury and damages for which it is entitled to relief under 35 U.S.C. § 284 adequate to compensate for such infringement, but in no event less than a reasonable royalty.

34. Defendants' infringement will continue to injure North Star, unless and until this Court enters an injunction, which prohibits further infringement and specifically enjoins further importation, use, sale and/or offer for sale of products that come within the scope of the '416 Patent.

JURY DEMAND

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, North Star demands a trial by jury on all issues presented that can properly be tried to a jury.

REQUEST FOR RELIEF

THEREFORE, North Star asks this Court to enter judgment against Defendants and against their subsidiaries, affiliates, agents, servants, employees and all persons in active concert or participation with Defendants, granting the following relief:

A. An award of damages adequate to compensate North Star for the infringement that has occurred, together with prejudgment interest from the date infringement began and postjudgment interest;

B. All other damages permitted by 35 U.S.C. § 284;

C. A finding that this case is exceptional and an award to North Star of its attorneys' fees and costs as provided by 35 U.S.C. § 285;

D. A permanent injunction prohibiting further infringement of the '526 Patent and the '416 Patent; and

E. Such other and further relief as this Court or a jury may deem proper and just.

Dated: November 30, 2016

Respectfully submitted,

FARNAN LLP

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