IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

JANUS SEMICONDUCTOR RESEARCH, LLC, ***Plaintiff,*** **v.** **SK HYNIX, INC., SK HYNIX AMERICA INC., AND SK HYNIX MEMORY SOLUTIONS INC.,** ***Defendants*.**	**Civil Action No. 2:16-cv-1410** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Janus Semiconductor Research, LLC ("Janus"), by and through its attorneys, brings this action and makes the following allegations of patent infringement relating to U.S. Patent No. 5,987,620 ("the '620 patent" or "the patent-in-suit"). Defendants SK Hynix, Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. (collectively, "SK Hynix") infringe the patent-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq*., and Janus seeks compensation for this unauthorized use.

THE PARTIES

1. Janus is a Texas limited liability company with its principal place of business at 911 NW Loop 281, Suite 211-27, Longview, TX 75604.

2. Janus is a small, Texas-based company with an employee in Longview, Texas. Like many technology-focused companies, Janus depends on patent protection to effectively license its innovative technologies and build its business.

3. On information and belief, Defendant SK Hynix, Inc. is a Korean corporation with its principal office at 2091, Gyeongchung-daero, Bubal-eup, Icheon-si, Gyeonggi, Republic of Korea.

4. On information and belief, Defendant SK Hynix America Inc. is a California corporation with its principal office at 3101 North First Street, San Jose, CA 95134. SK Hynix

America Inc. can be served through its registered agent, The Prentice-Hall Corporation System, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

5. On information and belief, SK Hynix America Inc. maintains major offices in Austin, Texas and Houston, Texas and is registered with the Texas Secretary of State to do business in Texas.

6. On information and belief, Defendant SK Hynix Memory Solutions Inc. is a Delaware corporation with its principal office at 3101 North First Street, San Jose, CA 95134. SK Hynix Memory Solutions Inc. can be served through its registered agent, Sang Soo Son, at 3101 North First Street, San Jose, CA 95134.

7. On information and belief, SK Hynix offers infringing products for sale throughout the United States and Canada, including in the Eastern District of Texas. Further, SK Hynix advertises its infringing products throughout the Eastern District of Texas and claims financial benefits through its conducting of business in Texas.

JURISDICTION AND VENUE

8. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

9. On information and belief, this Court has personal jurisdiction over SK Hynix, Inc. in this action because SK Hynix, Inc. has committed acts within the Eastern District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over SK Hynix, Inc. would not offend traditional notions of fair play and substantial justice. Defendant SK Hynix, Inc., directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patent-in-suit.

10. On information and belief, this Court has personal jurisdiction over SK Hynix America Inc. in this action because SK Hynix America Inc. has committed acts within the Eastern District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over SK Hynix America Inc. would not offend traditional notions of fair play and substantial justice. Defendant SK Hynix America Inc., directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patent-in-suit. Moreover, SK Hynix America Inc. maintains major offices in Austin, Texas and Houston, Texas and is registered to do business in the State of Texas.

11. On information and belief, this Court has personal jurisdiction over SK Hynix Memory Solutions Inc. in this action because SK Hynix Memory Solutions Inc. has committed acts within the Eastern District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over SK Hynix Memory Solutions Inc. would not offend traditional notions of fair play and substantial justice. Defendant SK Hynix Memory Solutions Inc., directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patent-in-suit.

12. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Defendant SK Hynix, Inc., upon information and belief, has transacted business in the Eastern District of Texas and has committed acts of direct and indirect infringement in the Eastern District of Texas. Defendant SK Hynix America Inc. is registered to do business in Texas, has several offices in Texas, and, upon information and belief, has transacted business in the Eastern District of Texas and has committed acts of direct and indirect infringement in the Eastern District of Texas. Defendant SK Hynix Memory Solutions, Inc., upon information and belief,

has transacted business in the Eastern District of Texas and has committed acts of direct and indirect infringement in the Eastern District of Texas.

HISTORY

13. Janus is the owner and assignee of the patent-in-suit.

14. The sole named inventor of the '620 patent, Dr. Thang Tran, is a prolific inventor and an electrical engineer with many years of industry experience.

15. Dr. Tran's professional career began in 1980. After graduating with a Bachelor's Degree in Electrical Engineering from the University of Texas at Austin ("UT Austin"), Dr. Tran joined Motorola, Inc. in Austin, Texas as an engineer.

16. While working full-time at Motorola, Dr. Tran earned his Master's Degree in Electrical Engineering with a focus on solid-state electronics from UT Austin.

17. Dr. Tran left Motorola in 1985 to join Advanced Micro Devices, Inc. ("AMD"). While working at AMD, he decided to shift his focus from solid-state electronics to the emerging field of semiconductor design, which he has continued to pursue for the past 30 years.

18. To further his education in semiconductor design, Dr. Tran earned a PhD in Electrical Engineering from UT Austin, with a focus on superscalar processor design, while still working full-time at AMD.

19. During his twelve years at AMD, Dr. Tran worked almost exclusively on microprocessor architecture and design.

20. Dr. Tran's work had an astounding impact on AMD. In addition to being a key architect on AMD's Athlon processor, Dr. Tran's work at AMD generated 80 issued United States patents, which have themselves been cited as prior art in more than 2,200 United States patents and published applications.

21. During the remainder of his nearly 40-year career, Dr. Tran has also worked for a number of other semiconductor-design companies, including Intel, Analog Devices, MediaTek, Centaur Technology, Texas Instruments, Freescale Semiconductor, and Synopsis.

22. For example, after spending several years developing and patenting microprocessor technology on his own, Dr. Tran joined Intel in 1999 as a Principal Engineer, a senior title in Intel's technical career track intended only for those few who have "a deep technical expertise with significant impact in [their] technology area."[1]

23. As another example, Dr. Tran spent more than seven years at Texas Instruments, working at a newly opened microprocessor design center in Austin, Texas, as a Design Manager and Senior Member of the Technical Staff. During his time at the design center, which was a collaboration between Texas Instruments and ARM, Dr. Tran designed the ARM Cortex-A8 microprocessor that would come to power the Apple iPhone 4 and Samsung Galaxy S smartphones.

24. Dr. Tran has spent his entire professional career designing microprocessor technology and is a named inventor on over 110 issued United States patents, which have themselves been cited as prior art in more than 3,100 United States patents and published applications.

25. In addition, Dr. Tran will be serving as an adjunct professor at Santa Clara University teaching microprocessor design beginning next year.

TECHNOLOGY OVERVIEW

26. Integrated circuits have become ubiquitous in today's world and continue to become smaller, more powerful, and more complex. Modern integrated circuits, such as processors, systems on a chip ("SoCs"), digital memory, application-specific integrated circuits ("ASICs"), and field-programmable gate arrays ("FPGAs"), are used in virtually all of today's electronic devices.

27. At the time of the application that led to the '620 patent, however, integrated circuits were much simpler than they are today. For example, microprocessors at that time were generally classic RISC ("reduced instruction set computer") processors with a single clock and

[1] Kelli Gizzi, *Setting a Deliberate Path to Principal Engineer*, INTEL IT PEER NETWORK (August 19, 2014).

relatively few pipeline stages (e.g., five stages) with limited parallel-processing capabilities, multi-threading capabilities, pipeline depth, and issue width. External memory was similarly limited, having lower clock speeds, slower memory accesses, and smaller storage capacities.

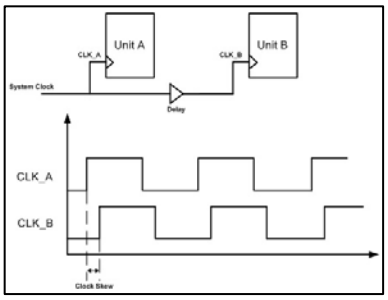
I. Fundamentals of Circuit Design

28. Data is represented in digital circuits using binary signals that are either high (i.e., a "1") or low (i.e., a "0"). The data is stored in storage devices, such as registers or arrays, which are made up of multiple storage elements, such as flip-flops, that store the individual 1s and 0s.

29. In a circuit with a synchronous processing design, in which the circuit relies on a clock signal to control the circuit's timing, the storage devices capture the data values on either a rising edge and/or a falling edge of the clock signal and store those values until a later rising/falling edge. The outputs of the storage elements change state and are read at certain points in time, based on the clock signal, to ensure an accurate reading. Ideally, the clock signal should reach all the storage elements at the same time, causing all of them to change state simultaneously.

30. The clock signal, although necessary in a synchronous processing design, can cause additional problems and concerns—such as clock skew (i.e., the difference in arrival times of clock edges at different parts of the circuit), clock jitter (i.e., the amount the clock signal deviates from an ideal clock signal), increased power consumption, and excess noise—that chip designers must address.

31. For example, clock skew can occur when a single global clock signal is used to synchronize an entire circuit because the clock signal can be affected by a variety of factors as it travels through the circuit to various functional blocks. As a result, the same clock signal can arrive at the different functional blocks within the same circuit at different times, potentially causing problems. An exemplary depiction of clock skew is illustrated in the figure below.



Yasen Stoyanov, *Clock Skew Removal (Clock Deskewing) using PLL and DLL*, OPEN4TECH TECHNOLOGY ARTICLE (September 13, 2016), available at http://open4tech.com/clock-skew-removal-pll-dll/.

32. As clock rates have increased and the size of the components on a chip has decreased, the negative effects of clock skew and jitter have become more pronounced, taking up more and more of the available clock cycle period.

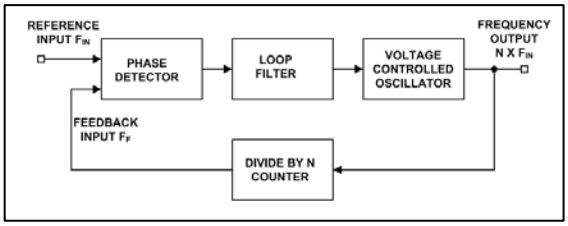
33. In contrast to the more commonly used synchronous processing design, circuits using asynchronous processing design are not governed by a clock. Instead, the state of the circuit changes when the input changes. Because they do not have to wait for the next clock pulse to begin processing data, circuits using asynchronous processing design are theoretically faster than circuits using synchronous processing designs as their speed is theoretically limited only by the propagation delay of the gates.

34. Circuits using asynchronous processing offer some advantages over those using synchronous processing. For example, because there is no clock, neither clock skew nor clock jitter is a concern. Additionally, circuits using asynchronous processing use less power because their asynchronous nature allows them to activate or enable processing units only as they are needed during an operation.

35. Because modern integrated circuits are very complex and require precise timing, they often use phase-locked loop ("PLL") circuits and delay-locked loop ("DLL") circuits to generate and manage multiple clocks that are distributed to the various components within the circuit. These multiple, distributed clocks allow different functional blocks within the circuit to operate at unique frequencies.

36. In a PLL, a voltage-controlled oscillator is adjusted in a negative feedback loop, which causes the frequency and phase of the output clock signal to match the frequency and phase of the reference clock. By adding a frequency divider to the feedback loop of the PLL, the PLL can be used to generate an output frequency that is a multiple of the input frequency.

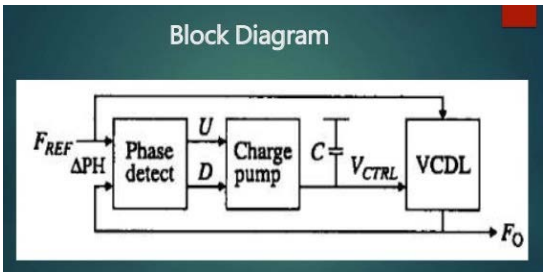
37. The figure below shows an exemplary conceptual block diagram of a PLL.



See, e.g., *Dynamic Measurements of Phase Lock Loop Transient Response*, TELEDYNE LECROY TECHNICAL BRIEF, at 1 (June 25, 2013).

38. In a DLL, an adjustable delay-line element delays an incoming clock signal such that the output clock signal is delayed by one or more clock cycles. A DLL is used to bring a voltage-controlled delay line into phase alignment with a reference signal. This can be beneficial for maintaining the timing relationship between a clock signal and an output data signal. A DLL's phase detector detects the phase difference between the clock and output data, and then sends control information through a low-pass filter to a variable delay line that adjusts the timing of the internal clock to maintain the desired timing relationship.

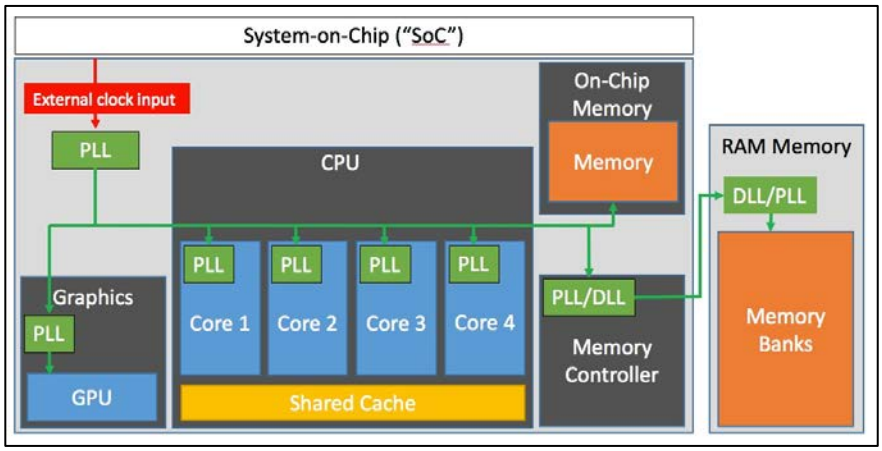
39. The figure below shows an exemplary conceptual block diagram of a DLL.



See, e.g., Kartik Pal, *Design and Simulation of PLL & DLL Using Matlab Simulink*, at Slide 26, available at http://www.slideshare.net/kartikpal/pll-dll-design-in-simulink-matlab (visited Oct. 17, 2016).

II. Complex Modern Integrated Circuits

40. In contrast to the simple RISC microprocessors that were common at the time of the ’620 patent application, modern processors are much more complex, with deep superpipelined, superscalar architectures and larger instruction sets. Modern multi-core processors are often implemented as SoCs that include a variety of functional blocks, such as, for example: multiple cores for processing instructions and data; various levels of cache memory; on-chip memory; one or more on-chip memory controllers; and one or more peripheral interfaces. These modern multi-core processors generally connect to an external clock and use a PLL to generate a global system clock that is then distributed within the processor to each of the cores and the various controllers. At each of the cores and the various controllers, additional PLLs and/or DLLs generate a separate local clock for use within each of those cores and controllers. The following figure shows a stylized version of some of the various functional blocks and clocks that can be found in modern SoC processors.



41. Modern SoC processors often also use additional system memory, which is provided as an external memory chip or module and interfaces with the processor through the processor’s on-chip memory controller. The stylized figure above also shows an exemplary external memory module. Although there are many kinds of external memory that may be used, depending on the particular application, synchronous dynamic random access memory (or “SDRAM”) is perhaps the most prevalent type.

42. To ensure SDRAM technology is interchangeable, JEDEC, the industry body for semiconductor standards, defines the specifications for SDRAM memory. These specifications define, for example, the "features, functionalities, AC and DC characteristics, packages, and ball/signal assignments" for the various DDR standards. *See, e.g.*, DDR3 SDRAM, JEDEC Standard No. 79-3C, at 1.

43. JEDEC adopted its first SDRAM standard in 1993 with the introduction of single data rate ("SDR") SDRAM. Since then, each new version of SDRAM has been developed to make it faster and more effective. The first major improvement to SDRAM occurred with the creation of double data rate ("DDR") SDRAM in 2000, and DDR SDRAM remains popular today, with most modern SDRAM being DDR SDRAM.

44. JEDEC released the first specification for DDR SDRAM, Standard No. 79C, in June of 2000. Since then, as technology has evolved, JEDEC has defined newer versions of the DDR specification, such as DDR2, DDR3, DDR4, GDDR5, and GDDR5X.

45. Each new generation of DDR SDRAM offers increased data rates and operates at higher clock speeds. While these changes have improved the overall performance of SDRAM, the increased clock speeds have exacerbated the effects of clock skew, clock jitter, and the other design considerations discussed above.

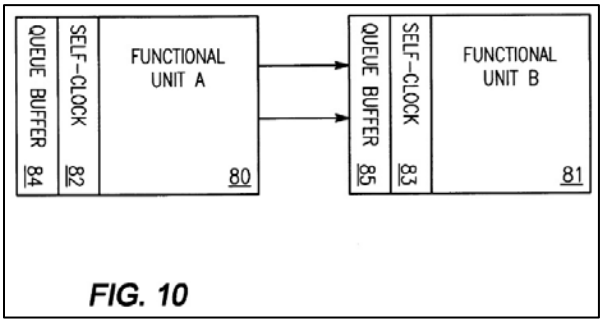
OVERVIEW OF THE PATENT-IN-SUIT

46. Recognizing the above-discussed problems associated with synchronous and asynchronous processing designs, Dr. Tran observed the need for an "asynchronous clock design having the heretofore typically mutually exclusive advantages of low power dissipation, and an easily verifiable output where all components start together and generate output in a predetermined and predictable fashion." '620 Patent, at 2:63-67. To solve these problems, he designed a "distributed self-timed and self-enabled clock design" that can be used at the system level and that is "adaptable for use in any digital circuit clock design." *Id.* at 3:3-7.

47. This distributed clock design described in the ’620 patent is covered by the ’620 patent’s four independent claims (along with their corresponding dependent claims), which generally recite either: (1) a clock system for a digital circuit (i.e., claims 1 and 16); or (2) functional blocks in a processor and/or digital system that include clock modules (i.e., claims 33 and 46). The ’620 patent “contemplates a use with any processing unit” and “provides a method to distribute the self-enabled and self-timed clock to individual functional units within a pipeline processing unit,” such as an SDRAM module. ’620 Patent, at 20:10-14.

48. In contrast to using a single, centralized clock signal, which was common at the time of the application that led to the ’620 patent, the ’620 patent describes clock modules (referred to in the patent as “self-clocks”) that are distributed to various functional blocks of a processor and are each activated by an enable signal. These distributed self-clock modules can match the frequency of an external clock signal (*id*. at 3:50-52), ensuring the proper timing of each functional block. Using these distributed self-clock modules in a processor, SDRAM module, or other digital circuit allows different functional blocks within the processor to operate using their own separate, local clocks.

49. For example, Figure 10 of the ’620 patent, shown below, depicts an embodiment of the ’620 patent with two functional blocks, each of which includes its own self-clock. These functional blocks each process data in different amounts of times using the local clock signal provided by their respective self-clocks.



’620 Patent, Fig. 10.

50. The distributed self-clock modules described in the ’620 patent offer a number of benefits, such as flexibility in the circuit design; reduction of power dissipation, noise, and clock skew; and improvement of the overall instruction-per-cycle performance of the processor. For example, the ’620 patent describes the flexibility to enable each self-clock only as needed and the ability of each self-clock to synchronize with an external clock as well as the self-clocks of other functional blocks to ensure proper operation of the circuit and to minimize clock skew.

COUNT I
INFRINGEMENT OF U.S. PATENT NO. 5,987,620

51. Janus restates and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

52. U.S. Patent No. 5,987,620 (“the ’620 patent”), entitled “Method and Apparatus for a Self-Timed and Self-Enabled Distributed Clock,” was filed on November 14, 1997. The named inventor on the face of the ’620 patent is Dr. Thang Tran, of Austin, Texas. Janus is the owner by assignment of the ’620 patent. A true and correct copy of the ’620 patent is attached hereto as Exhibit A.

53. The ’620 patent has been cited by at least 92 United States patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ’620 patent as relevant prior art:

- Facebook, Inc.;
- Globalfoundries, Inc.;
- Intel Corporation;
- International Business Machines, Inc.;
- Lockheed Martin Corporation;
- Micron Technology, Inc.;
- Rambus, Inc.;
- Renesas Electronics Corporation;
- STMicroelectronics, Inc.;
- Sun Microsystems, Inc.; and
- Texas Instruments, Inc.

54. On information and belief, SK Hynix makes, uses, sells, offers to sell, and/or imports DDR4 SDRAM Modules, including but not limited to all products with a part number beginning with "HMA"; DDR4 SDRAM Components, including but not limited to all products with a part number beginning with "H5A"; DDR3 SDRAM Modules, including but not limited to all products with a part number beginning with "HMT"; and DDR3 SDRAM Components, including but not limited to all products with a part number beginning with "H5T" (collectively, "the SK Hynix Accused Products").

55. On information and belief, to the extent the preamble is limiting, the SK Hynix Accused Products comprise a self-timed and self-enabled clock circuit for synchronizing operation of a digital circuit. For example, the SK Hynix Accused Products include a DLL, which is used to generate an internal clock in SDRAM memory and to synchronize the operation of the memory.

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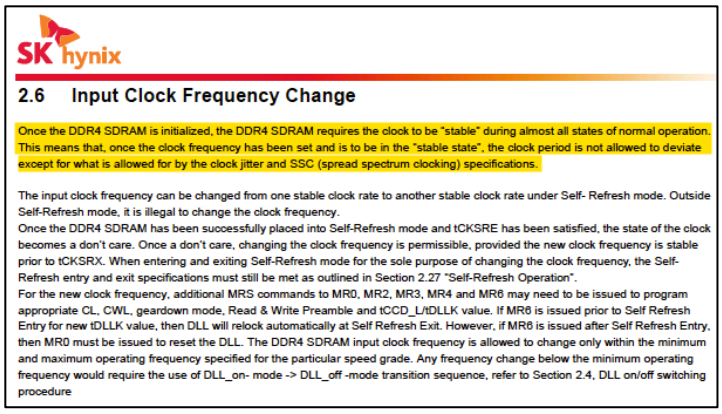
MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 4)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency	00 = 0(AL disabled) 01 = CL-1 10 = CL-2 11 = Resrved
A2, A1	Output Driver Impedance Control	(see Table 5)
A0	DLL Enable	0 = Disable[2] 1 = Enable

SK Hynix DDR4 SDRAM Device Operation Manual, SK HYNIX TECHNICAL DOCUMENTATION (June 2013), at 15 (highlighting added).

56. On information and belief, the SK Hynix Accused Products comprise a control circuit that detects input clock pulses. For example, the SK Hynix Accused Products receive and are able to detect input clock pulses from an external clock through the CK input.



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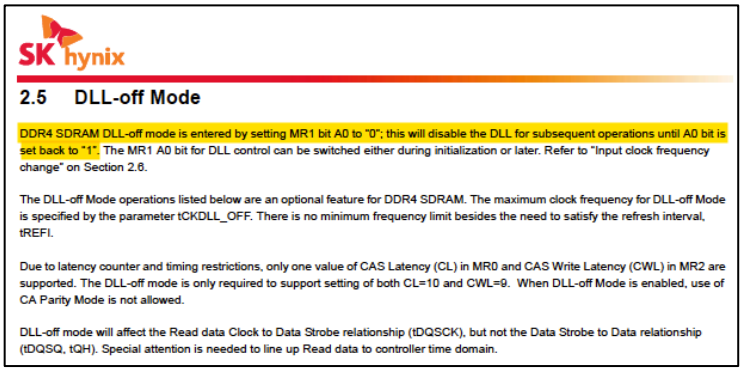
2.6 Input Clock Frequency Change

Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under Self- Refresh mode. Outside Self-Refresh mode, it is illegal to change the clock frequency.
Once the DDR4 SDRAM has been successfully placed into Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Section 2.27 "Self-Refresh Operation".
For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4 and MR6 may need to be issued to program appropriate CL, CWL, geardown mode, Read & Write Preamble and tCCD_L/tDLLK value. If MR6 is issued prior to Self Refresh Entry for new tDLLK value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL. The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to Section 2.4, DLL on/off switching procedure

SK Hynix DDR4 SDRAM Device Operation Manual, SK HYNIX TECHNICAL DOCUMENTATION (June 2013), at 31 (highlighting added).

57. On information and belief, the SK Hynix Accused Products comprise a control circuit that provides an enable signal while the input clock pulses are provided. For example, Mode Register MR1 in the SK Hynix Accused Products stores settings that are used to, among other things, enable/disable the DLL within the SK Hynix Accused Products. The SK Hynix Accused Products include a control circuit that enables/disables the DLL in response to the settings in MR1.



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2.5 DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to "0"; this will disable the DLL for subsequent operations until A0 bit is set back to "1". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on Section 2.6.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

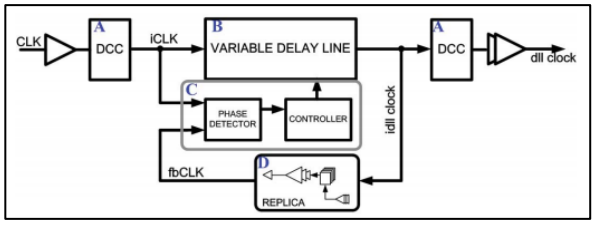
Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

SK Hynix DDR4 SDRAM Device Operation Manual, SK HYNIX TECHNICAL DOCUMENTATION (June 2013), at 30 (highlighting added).

58. On information and belief, the SK Hynix Accused Products comprise a clock delay device, coupled to the control circuit, that has a plurality of inputs and an output that provides an output clock pulse when the clock delay device is enabled. For example, the DLL in the SK Hynix Accused Products contains multiple inputs, including inputs for both a feedback

clock and an input clock, and an output that provides an output clock pulse when the DLL is enabled.



Hyun-Woo Lee and Chulwoo Kim, *Survey and Analysis of Delay-Locked Loops Used in DRAM Interfaces*, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 4 (April 2014) at 707.

59. On information and belief, the inputs to the clock delay device in the SK Hynix Accused Products include a feedback clock input that is coupled to the output of the clock delay device. For example, the DLL in the SK Hynix Accused Products includes a feedback loop wherein the output of the DLL is fed back into the DLL as an input, which is used to adjust the edges of the DLL's output clock (i.e., the internal clock) so that the memory's output data signal will be aligned with the input clock signal.

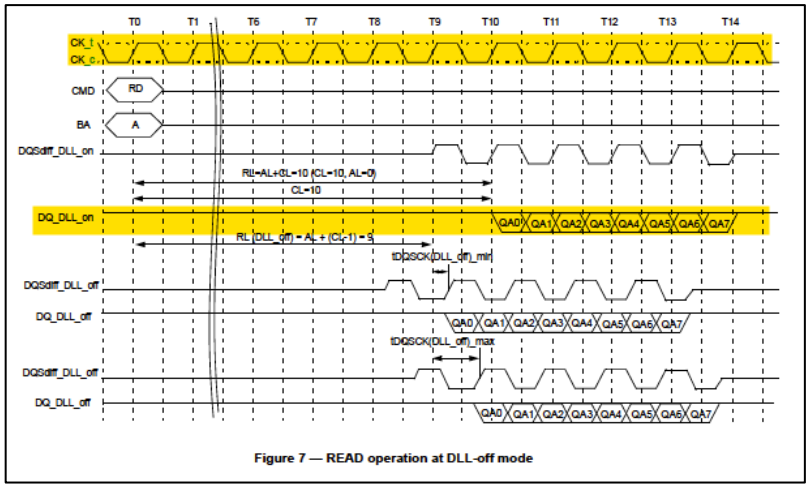


Figure 7 — READ operation at DLL-off mode

SK Hynix DDR4 SDRAM Device Operation Manual, SK HYNIX TECHNICAL DOCUMENTATION (June 2013), at 30 (highlighting added).

60. On information and belief, the inputs to the clock delay device in the SK Hynix Accused Products include a clock input for receiving the input clock pulses. For example, as

explained above, the DLL in the SK Hynix Accused Products includes a clock input (i.e., CK) for receiving input clock pulses.

61. On information and belief, the inputs to the clock delay device in the SK Hynix Accused Products include an enable input that receives the enable signal to enable the clock delay device. For example, as explained above, the DLL in the SK Hynix Accused Products includes an enable input for receiving an enable signal in response to the settings in the Mode Register MR1.

62. On information and belief, when enabled by the enable signal, the clock delay device in the SK Hynix Accused Products provides output clock pulses that are synchronized with the input clock pulses. For example, when enabled, the DLL in the SK Hynix Accused Products provides output clock pulses that are synchronized with the input clock pulses so that the memory's output data signal will be aligned with the input clock signal.

63. By making, using, testing, offering for sale, selling, and/or importing integrated circuits, including but not limited to the SK Hynix Accused Products, SK Hynix has injured Janus and is liable to Janus for directly infringing one or more claims of the '620 patent, including at least claim 1, pursuant to 35 U.S.C. § 271(a).

64. On information and belief, SK Hynix also indirectly infringes the '620 patent by actively inducing infringement under 35 U.S.C. § 271(b).

65. On information and belief, SK Hynix has had knowledge of the '620 patent since at least the date of service of this Complaint or shortly thereafter, and on information and belief, SK Hynix knew of the '620 patent and knew of its infringement, including by way of this lawsuit.

66. On information and belief, SK Hynix intended to induce patent infringement by third-party customers and users of the SK Hynix Accused Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. SK Hynix specifically intended and was aware that the normal and customary use of the accused products would infringe the '620 patent. SK Hynix performed

the acts that constitute induced infringement, and would induce actual infringement, with the knowledge of the ’620 patent and with the knowledge that the induced acts would constitute infringement. For example, SK Hynix provides the SK Hynix Accused Products, which are capable of operating in a manner that infringes one or more claims of the ’620 patent, including at least claim 1, and SK Hynix further provides documentation and training materials that cause customers of the SK Hynix Accused Products to utilize the products and services in a manner that directly infringes one or more claims of the ’620 patent. By providing instruction and training to customers on how to use the SK Hynix Accused Products, SK Hynix specifically intended to induce infringement of the ’620 patent, including at least claim 1. On information and belief, SK Hynix engaged in such inducement to promote the sales of the SK Hynix Accused Products and to actively induce its customers to infringe the ’620 patent. Accordingly, SK Hynix has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the ’620 patent, knowing that such use constitutes infringement of the ’620 patent.

67. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’620 patent.

68. As a result of SK Hynix’s infringement of the ’620 patent, Janus has suffered monetary damages, and seeks recovery in an amount adequate to compensate for SK Hynix’s infringement, but in no event less than a reasonable royalty for the use made of the invention by SK Hynix together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Janus respectfully requests that this Court enter:

A. A judgment in favor of Plaintiff Janus that SK Hynix has infringed the ’620 patent, either literally and/or under the doctrine of equivalents;

B. An award of damages resulting from SK Hynix’s acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order requiring SK Hynix to provide accountings and to pay supplemental damages to Janus, including, without limitation, prejudgment and post-judgment interest; and

D. Any and all other relief to which Janus may show itself to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Janus requests a trial by jury of any issues so triable by right.

Dated: December 14, 2016

Respectfully submitted,

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