IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

JANUS SEMICONDUCTOR RESEARCH, LLC, ***Plaintiff,*** **v.** **INTEL CORPORATION AND ALTERA CORPORATION,** ***Defendants.***	**Civil Action No. 2:17-cv-109** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Janus Semiconductor Research, LLC ("Janus"), by and through its attorneys, brings this action and makes the following allegations of patent infringement relating to U.S. Patent No. 5,987,620 ("the '620 patent" or "the patent-in-suit"). Defendants Intel Corporation ("Intel") and Altera Corporation ("Altera") infringe the patent-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*, and Janus seeks compensation for this unauthorized use.

THE PARTIES

1. Janus is a Texas limited liability company with its principal place of business at 911 NW Loop 281, Suite 211-27, Longview, TX 75604.

2. Janus is a small, Texas-based company with an employee in Longview, Texas. Like many technology-focused companies, Janus depends on patent protection to effectively license its innovative technologies and build its business.

3. On information and belief, Defendant Intel is a Delaware corporation with its principal place of business at 2200 Mission College Blvd., Santa Clara, California 95054. Intel can be served through its registered agent, CT Corporation System, 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136.

4. On information and belief, Defendant Altera is a Delaware corporation with its principal place of business at 101 Innovation Drive, San Jose, CA 95134. Altera can be served

through its registered agent, CT Corporation System, 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136.

5. On information and belief, Defendant Intel has approximately 2,300 employees in Texas and maintains substantial offices in Austin, Texas; Plano, Texas; and Richardson, Texas, where it engages in sales, marketing, and research and development of its System on a Chip and microprocessor components.[1]

6. On information and belief, Defendant Altera also maintains a substantial workforce in Texas with offices in both Austin, Texas and Richardson, Texas, where it engages in sales, marketing, and research and development of its FPGA products.

7. On information and belief, Intel purchased Altera for approximately $16.7 billion on December 28, 2015, and since that time, Altera has continued to operate as a wholly-owned subsidiary of Intel.

8. On information and belief, Intel and Altera offer infringing products for sale throughout the United States, including in the Eastern District of Texas. Further, Intel and Altera advertise their infringing products throughout the Eastern District of Texas and claim financial benefits through their conducting of business in Texas.

JURISDICTION AND VENUE

9. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

10. Upon information and belief, this Court has personal jurisdiction over Intel in this action because Intel has committed acts within the Eastern District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over Intel would not offend traditional notions of fair play and substantial justice. Defendant Intel, directly and/or through subsidiaries or intermediaries (including distributors,

[1] *Intel in Texas*, INTEL WEBPAGE, available at http://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html (accessed Sept. 6, 2016).

retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patent-in-suit. Moreover, Intel maintains substantial offices in Austin, Plano, and Richardson (all in Texas); is registered to do business in the State of Texas; and has appointed CT Corporation System, 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136, as its agent for service of process.

11. Upon information and belief, this Court has personal jurisdiction over Altera in this action because Altera has committed acts within the Eastern District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over Altera would not offend traditional notions of fair play and substantial justice. Defendant Altera, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patent-in-suit. Moreover, Altera maintains substantial offices in Austin, Texas and Richardson, Texas; is registered to do business in the State of Texas; and has appointed CT Corporation System, 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136, as its agent for service of process.

12. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Defendant Intel is registered to do business in Texas, has three substantial offices in Texas, and, upon information and belief, has transacted business in the Eastern District of Texas and has committed acts of direct and indirect infringement in the Eastern District of Texas. Defendant Altera is registered to do business in Texas, has two substantial offices in Texas, and, upon information and belief, has transacted business in the Eastern District of Texas and has committed acts of direct and indirect infringement in the Eastern District of Texas.

HISTORY

13. Janus is the owner and assignee of the patent-in-suit.

14. The sole named inventor of the ’620 patent, Dr. Thang Tran, is a prolific inventor and an electrical engineer with many years of industry experience.

15. Dr. Tran’s professional career began in 1980. After graduating with a Bachelor’s Degree in Electrical Engineering from the University of Texas at Austin (“UT Austin”), Dr. Tran joined Motorola, Inc. in Austin, Texas as an engineer.

16. While working full-time at Motorola, Dr. Tran earned his Master’s Degree in Electrical Engineering with a focus on solid-state electronics from UT Austin.

17. Dr. Tran left Motorola in 1985 to join Advanced Micro Devices, Inc. (“AMD”). While working at AMD, he decided to shift his focus from solid-state electronics to the emerging field of semiconductor design, which he has continued to pursue for the past 30 years.

18. To further his education in semiconductor design, Dr. Tran earned a PhD in Electrical Engineering from UT Austin, with a focus on superscalar processor design, while still working full-time at AMD.

19. During his twelve years at AMD, Dr. Tran worked almost exclusively on microprocessor architecture and design.

20. Dr. Tran’s work had an astounding impact on AMD. In addition to being a key architect on AMD’s Athlon processor, Dr. Tran’s work at AMD generated 80 issued United States patents, which have themselves been cited as prior art in more than 2,200 United States patents and published applications.

21. During the remainder of his nearly 40-year career, Dr. Tran also worked for a number of other semiconductor-design companies, including Intel, Analog Devices, MediaTek, Centaur Technology, Texas Instruments, Freescale Semiconductor, and Synopsis.

22. For example, after spending several years developing and patenting microprocessor technology on his own, Dr. Tran joined Intel in 1999 as a Principal Engineer, a

senior title in Intel's technical career track intended only for those few who have "a deep technical expertise with significant impact in [their] technology area."[2]

23. As another example, Dr. Tran spent more than seven years at Texas Instruments, working at a newly opened microprocessor design center in Austin, Texas, as a Design Manager and Senior Member of the Technical Staff. During his time at the design center, which was a collaboration between Texas Instruments and ARM, Dr. Tran designed the ARM Cortex-A8 microprocessor that would come to power the Apple iPhone 4 and Samsung Galaxy S smartphones.

24. Dr. Tran has spent his entire professional career designing microprocessor technology and is a named inventor on over 110 issued United States patents, which have themselves been cited as prior art in more than 3,100 United States patents and published applications.

TECHNOLOGY OVERVIEW

25. Integrated circuits have become ubiquitous in today's world and continue to become smaller, more powerful, and more complex. Modern integrated circuits, such as processors, systems on a chip ("SoCs"), digital memory, application-specific integrated circuits ("ASICs"), and field-programmable gate arrays ("FPGAs"), are used in virtually all of today's electronic devices.

26. At the time of the application that led to the '620 patent, however, integrated circuits were much simpler than they are today. For example, microprocessors at that time were generally classic RISC ("reduced instruction set computer") processors with a single clock and relatively few pipeline stages (e.g., five stages) with limited parallel-processing capabilities, multi-threading capabilities, pipeline depth, and issue width. External memory was similarly limited, having lower clock speeds, slower memory accesses, and smaller storage capacities.

[2] Kelli Gizzi, *Setting a Deliberate Path to Principal Engineer*, INTEL IT PEER NETWORK (August 19, 2014).

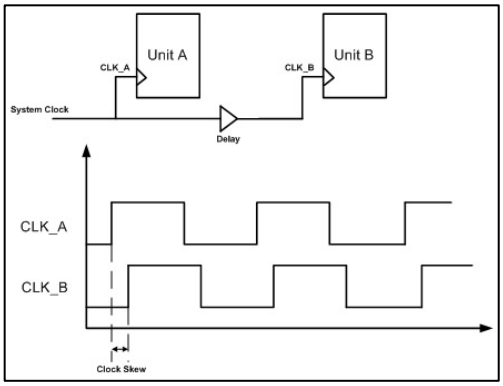
I. Fundamentals of Circuit Design

27. Data is represented in digital circuits using binary signals that are either high (i.e., a "1") or low (i.e., a "0"). The data is stored in storage devices, such as registers or arrays, which are made up of multiple storage elements, such as flip-flops, that store the individual 1s and 0s.

28. In a circuit with a synchronous processing design, in which the circuit relies on a clock signal to control the circuit's timing, the storage devices capture the data values on either a rising edge and/or a falling edge of the clock signal and store those values until a later rising/falling edge. The outputs of the storage elements change state and are read at certain points in time, based on the clock signal, to ensure an accurate reading. Ideally, the clock signal should reach all the storage elements at the same time, causing all of them to change state simultaneously.

29. The clock signal, although necessary in a synchronous processing design, can cause additional problems and concerns—such as clock skew (i.e., the difference in arrival times of clock edges at different parts of the circuit), clock jitter (i.e., the amount the clock signal deviates from an ideal clock signal), increased power consumption, and excess noise—that chip designers must address.

30. For example, clock skew can occur when a single global clock signal is used to synchronize an entire circuit because the clock signal can be affected by a variety of factors as it travels through the circuit to various functional blocks. As a result, the same clock signal can arrive at the different functional blocks within the same circuit at different times, potentially causing problems. An exemplary depiction of clock skew is illustrated in the figure below.



Yasen Stoyanov, *Clock Skew Removal (Clock Deskewing) using PLL and DLL*, OPEN4TECH TECHNOLOGY ARTICLE (September 13, 2016), available at http://open4tech.com/clock-skew-removal-pll-dll/.

31. As clock rates have increased and the size of the components on a chip has decreased, the negative effects of clock skew and jitter have become more pronounced, taking up more and more of the available clock cycle period.

32. In contrast to the more commonly used synchronous processing design, circuits using asynchronous processing design are not governed by a clock. Instead, the state of the circuit changes when the input changes. Because they do not have to wait for the next clock pulse to begin processing data, circuits using asynchronous processing design are theoretically faster than circuits using synchronous processing designs as their speed is theoretically limited only by the propagation delay of the gates.

33. Circuits using asynchronous processing offer some advantages over those using synchronous processing. For example, because there is no clock, neither clock skew nor clock jitter is a concern. Additionally, circuits using asynchronous processing use less power because their asynchronous nature allows them to activate or enable processing units only as they are needed during an operation.

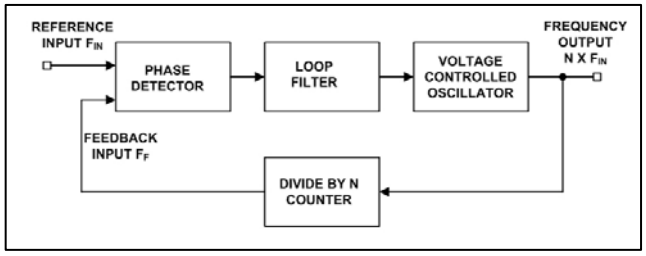
34. Because modern integrated circuits are very complex and require precise timing, they often use phase-locked loop ("PLL") circuits and delay-locked loop ("DLL") circuits to generate and manage multiple clocks that are distributed to the various components within the

circuit. These multiple, distributed clocks allow different functional blocks within the circuit to operate at unique frequencies.

35. In a PLL, a voltage-controlled oscillator is adjusted in a negative feedback loop, which causes the frequency and phase of the output clock signal to match the frequency and phase of the reference clock. By adding a frequency divider to the feedback loop of the PLL, the PLL can be used to generate an output frequency that is a multiple of the input frequency.

36. In a PLL, a voltage-controlled oscillator is adjusted in a negative feedback loop, which causes the frequency and phase of the output clock signal to match the frequency and phase of the reference clock. By adding a frequency divider to the feedback loop of the PLL, the PLL can be used to generate an output frequency that is a multiple of the input frequency.

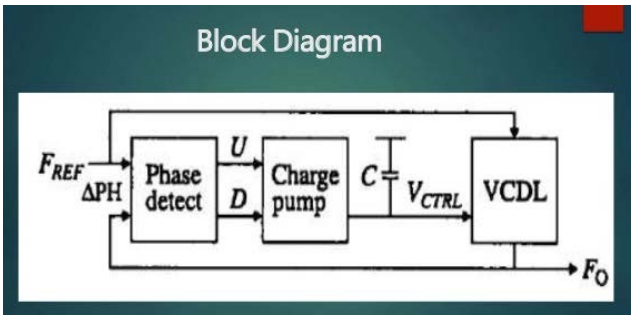
37. The figure below shows an exemplary conceptual block diagram of a PLL.



See, e.g., *Dynamic Measurements of Phase Lock Loop Transient Response*, TELEDYNE LECROY TECHNICAL BRIEF, at 1 (June 25, 2013).

38. In a DLL, an adjustable delay-line element delays an incoming clock signal such that the output clock signal is delayed by one or more clock cycles. A DLL is used to bring a voltage-controlled delay line into phase alignment with a reference signal. This can be beneficial for maintaining the timing relationship between a clock signal and an output data signal. A DLL's phase detector detects the phase difference between the clock and output data, and then sends control information through a low-pass filter to a variable delay line that adjusts the timing of the internal clock to maintain the desired timing relationship.

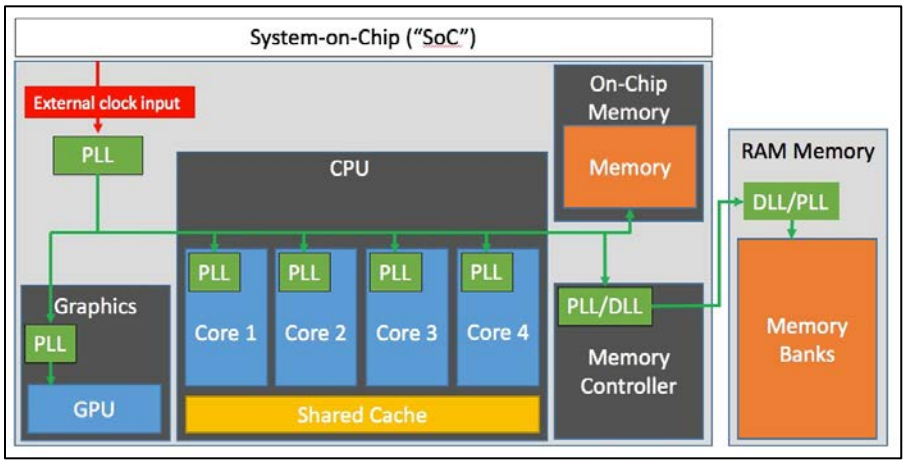
39. The figure below shows an exemplary conceptual block diagram of a DLL.



See, e.g., Kartik Pal, *Design and Simulation of PLL & DLL Using Matlab Simulink*, at Slide 26, available at http://www.slideshare.net/kartikpal/pll-dll-design-in-simulink-matlab (visited Oct. 17, 2016).

II. Complex Modern Processors

40. In contrast to the simple RISC microprocessors that were common at the time of the ’620 patent application, modern processors are much more complex, with deep superpipelined, superscalar architectures and larger instruction sets. Modern multi-core processors are often implemented as SoCs that include a variety of functional blocks, such as, for example: multiple cores for processing instructions and data; various levels of cache memory; on-chip memory; one or more on-chip memory controllers; and one or more peripheral interfaces. These modern multi-core processors generally connect to an external clock and use a PLL to generate a global system clock that is then distributed within the processor to each of the cores and the various controllers. At each of the cores and the various controllers, additional PLLs and/or DLLs generate a separate local clock for use within each of those cores and controllers. The following figure shows a stylized version of some of the various functional blocks and clocks that can be found in modern SoC processors.



OVERVIEW OF THE PATENT-IN-SUIT

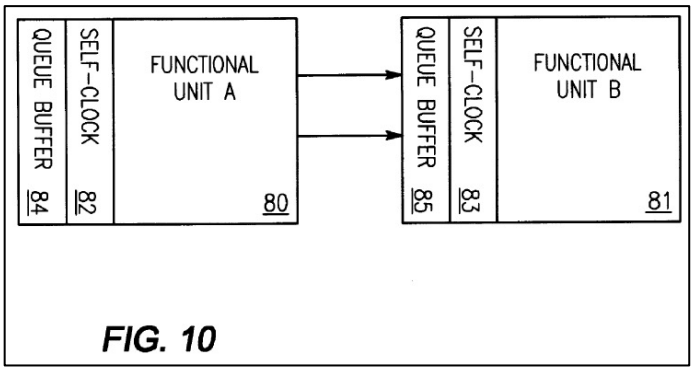
41. Recognizing the above-discussed problems associated with synchronous and asynchronous processing designs, Dr. Tran observed the need for an "asynchronous clock design having the heretofore typically mutually exclusive advantages of low power dissipation, and an easily verifiable output where all components start together and generate output in a predetermined and predictable fashion." '620 Patent, at 2:63-67. To solve these problems, he designed a "distributed self-timed and self-enabled clock design" that can be used at the system level and that is "adaptable for use in any digital circuit clock design." *Id.* at 3:3-7.

42. This distributed clock design described in the '620 patent is covered by the '620 patent's four independent claims (along with their corresponding dependent claims), which generally recite either: (1) a clock system for a digital circuit (i.e., claims 1 and 16); or (2) functional blocks in a processor and/or digital system that include clock modules (i.e., claims 33 and 46). The '620 patent "contemplates a use with any processing unit" and "provides a method to distribute the self-enabled and self-timed clock to individual functional units within a pipeline processing unit," such as a processor or FPGA. '620 Patent, at 20:10-14.

43. In contrast to using a single, centralized clock signal, which was common at the time of the application that led to the '620 patent, the '620 patent describes clock modules (referred to in the patent as "self-clocks") that are distributed to various functional blocks of an integrated circuit and are each activated by an enable signal. These distributed self-clock

modules can match the frequency of an external clock signal (*id*. at 3:50-52), ensuring the proper timing of each functional block. Using these distributed self-clock modules in a processor, FPGA, SDRAM module, or other digital circuit allows different functional blocks within the processor to operate using their own separate, local clocks.

44. For example, Figure 10 of the ’620 patent, shown below, depicts an embodiment of the ’620 patent with two functional blocks, each of which includes its own self-clock. These functional blocks each process data in different amounts of times using the local clock signal provided by their respective self-clocks.



’620 Patent, Fig. 10.

45. The distributed self-clock modules described in the ’620 patent offer a number of benefits, such as flexibility in the circuit design, reduction of power dissipation, noise, and clock skew, and improvement of the overall instruction-per-cycle performance of the processor. For example, the ’620 patent describes the flexibility to enable each self-clock only as needed and the ability of each self-clock to synchronize with an external clock as well as the self-clocks of other functional blocks to ensure proper operation of the circuit and to minimize clock skew.

COUNT I
INFRINGEMENT OF U.S. PATENT NO. 5,987,620
(AGAINST INTEL)

46. Janus restates and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

47. U.S. Patent No. 5,987,620 ("the '620 patent"), entitled "Method and Apparatus for a Self-Timed and Self-Enabled Distributed Clock," was filed on November 14, 1997. The named inventor on the face of the '620 patent is Dr. Thang Tran, of Austin, Texas. Janus is the owner by assignment of the '620 patent. A true and correct copy of the '620 patent is attached hereto as Exhibit A.

48. The '620 patent has been cited by at least 94 United States patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '620 patent as relevant prior art:

- Facebook, Inc.;
- Globalfoundries, Inc.;
- Intel Corporation;
- International Business Machines, Inc.;
- Lockheed Martin Corporation;
- Micron Technology, Inc.;
- Rambus, Inc.;
- Renesas Electronics Corporation;
- STMicroelectronics, Inc.;
- Sun Microsystems, Inc.; and
- Texas Instruments, Inc.

49. On information and belief, Intel makes, uses, sells, offers to sell, and/or imports the Intel Core i3 series of processors based upon Intel's Westmere, Clarkdale, Sandy Bridge, Ivy Bridge, Haswell, Broadwell, Skylake, and Kaby Lake architectures, including but not limited to those with Model Nos. beginning with i3-530, i3-540, i3-550, i3-560, i3-2100, i3-2102, i3-2105, i3-2120, i3-2130, i3- 3210, i3- 3220, i3- 3225, i3- 3240, i3- 3245, i3- 3250, i3-4130, i3-4150, i3-4160, i3-4170, i3-4330, i3-4340, i3-4350, i3-4360, i3-4370, i3-6098, i3-6100, i3-6300, i3-6320, i3-7100, i3-7101, i3-7300, i3-7320, i3-7350, i3-7100, and i3-7100 (collectively, "the Intel Core i3 Processors").

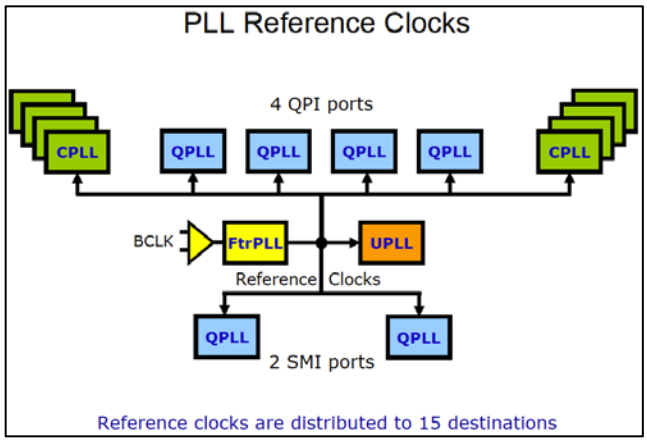
50. On information and belief, Intel makes, uses, sells, offers to sell, and/or imports the Intel Core i5 series of processors based upon Intel's Nehalem, Westmere, Clarkdale, Sandy Bridge, Ivy Bridge, Haswell, Broadwell, Skylake, and Kaby Lake architectures, including but not

limited to those with Model Nos. beginning with i5-650, i5-655, i5-660, i5-661, i5-670, i5-680, i5-750, i5-760, i5-2300, i5-2310, i5-2320, i5-2380, i5-2390, i5-2400, i5-2405, i5-2500, i5-2550, i5-3300, i5-3330, i5-3340, i5-3350, i5-3450, i5-3470, i5-3475, i5-3550, i5-3570, i5-4430, i5-4440, i5-4460, i5-4570, i5-4590, i5-4670, i5-4690, i5-5575, i5-5675, i5-6400, i5-6402, i5-6500, i5-6585, i5-6600, i5-6685, i5-7400, i5-7500, and i5-7600 (collectively, "the Intel Core i5 Processors").

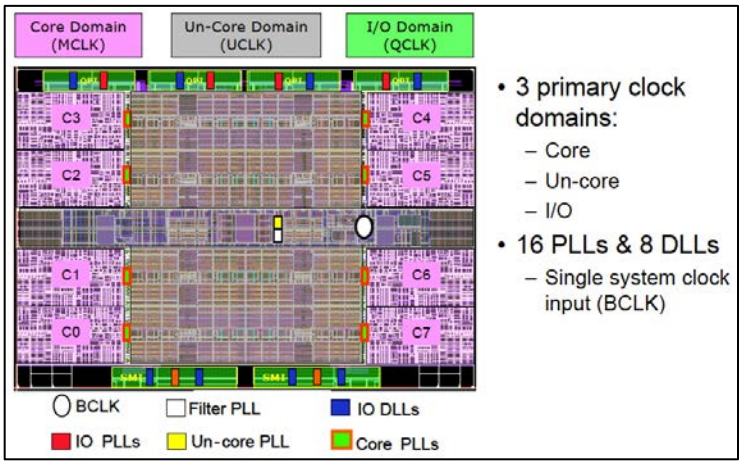
51. On information and belief, Intel makes, uses, sells, offers to sell, and/or imports the Intel Core i7 series of processors based upon Intel's Nehalem, Westmere, Clarkdale, Sandy Bridge, Ivy Bridge, Haswell, Broadwell, Skylake, and Kaby Lake architectures, including but not limited to those with Model Nos. beginning with i7-860, i7-870, i7-875, i7-880, i7-920, i7-930, i7-940, i7-950, i7-960, i7-970, i7-980, i7-2600, i7-2700, i7-3770, i7-4765, i7-4770, i7-4771, i7-4785, i7-4790, i7-5775, i7-6700, i7-6785, and i7-7700 (collectively, "the Intel Core i7 Processors").

52. On information and belief, Intel makes, uses, sells, offers to sell, and/or imports the Intel Core i3 Processors, the Intel Core i5 Processors, and the Intel Core i7 Processors (collectively, "the Intel Accused Products").

53. On information and belief, to the extent the preamble of claim 1 of the '620 patent is limiting, the Intel Accused Products comprise a self-timed and self-enabled clock circuit for synchronizing operation of a digital circuit. For example, the Intel Accused Products use three primary clock domains. These clock domains include multiple distributed PLLs, which are used for the various functional blocks within the clock domain, along with their own clock distribution.

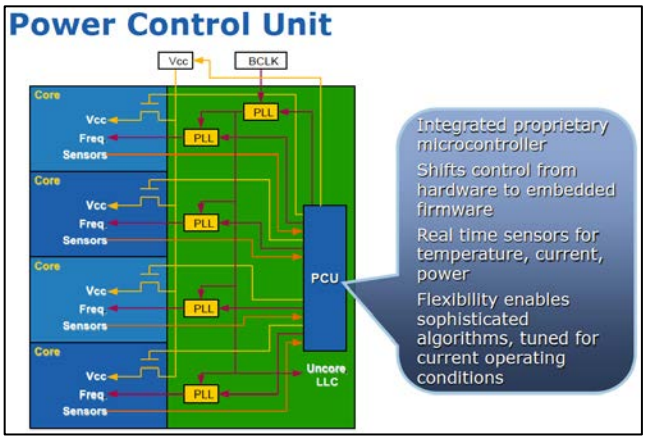


Stefan Rusu, *Nehalem-EX: a 45nm, 8-core Enterprise Processor*, INTEL TECHNICAL PRESENTATION (2009), at Slide 11, available at http://www.ewh.ieee.org/r6/scv/ssc/Oct2009.pdf.



Stefan Rusu, *Nehalem-EX: a 45nm, 8-core Enterprise Processor*, INTEL TECHNICAL PRESENTATION (2009), at Slide 10, available at http://www.ewh.ieee.org/r6/scv/ssc/Oct2009.pdf.

54. On information and belief, the Intel Accused Products comprise a control circuit that detects input clock pulses. For example, the Intel Accused Products include a Power Control Unit that receives and detects input clock pulses and that manages aspects of the operation of the distributed PLLs for each of the various functional blocks.



Glenn Hinton, *Key Nehalem Choices*, INTEL TECHNICAL PRESENTATION (February 17, 2010) at Slide 16.

55. On information and belief, the Intel Accused Products comprise a control circuit that provides an enable signal while the input clock pulses are provided. For example, the Intel Accused Products use core-level, low-power idle states called "C-states" to save power. The C0 state is the normal operating state of a core. When a core is operating normally (e.g., while the input clock pulses are provided) in the C0 state, the PLL is enabled. The C3 state is a low-power idle state in which all core clocks (e.g., the PLL for that core) are stopped. To stop the PLL for the C3 state, the control circuit turns off the enable signal to disable the PLL of that core.

4.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

Intel Datasheet, *Desktop 3rd Generation Intel Core Processor Family, Desktop Intel Pentium Processor Family, and Desktop Intel Celeron Processor Family*, Volume 1 of 2 (Nov. 2013), at 53.

56. On information and belief, the Intel Accused Products comprise a clock delay device, coupled to the control circuit, that has a plurality of inputs and an output that provides an output clock pulse when the clock delay device is enabled. For example, one or more of the distributed PLLs in the Intel Accused Products includes a clock delay device with multiple

inputs, including inputs for both a feedback clock and an input clock, and an output that provides an output clock pulse when the PLL is enabled.

57. On information and belief, the inputs to the clock delay device in the Intel Accused Products include a feedback clock input that is coupled to the output of the clock delay device. For example, one or more of the distributed PLLs in the Intel Accused Products includes a feedback loop wherein the output of the PLL is fed back into the PLL as an input, which is used to maintain phase alignment.

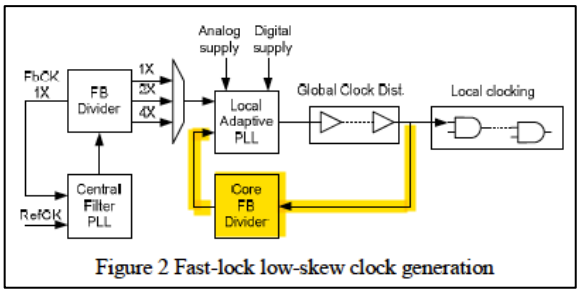


Figure 2 Fast-lock low-skew clock generation

Nasser Kurd et al., *Next Generation Intel Micro-architecture (Nehalem) Clocking Architecture*, IEEE SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS (2008), at 62 (highlighting added).

58. On information and belief, the inputs to the clock delay device in the Intel Accused Products include a clock input for receiving the input clock pulses. For example, one or more of the distributed PLLs in the Intel Accused Products includes a reference clock input for receiving input clock pulses from elsewhere in the circuit, such as the global clock reference signal.

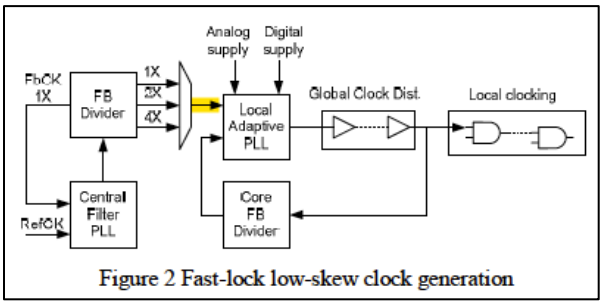
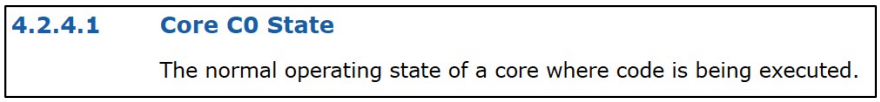


Figure 2 Fast-lock low-skew clock generation

Nasser Kurd et al., *Next Generation Intel Micro-architecture (Nehalem) Clocking Architecture*, IEEE SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS (2008), at 62 (highlighting added).

59. On information and belief, the inputs to the clock delay device in the Intel Accused Products include an enable input that receives the enable signal to enable the clock delay device. For example, one or more of the distributed PLLs in the Intel Accused Products includes an enable input for receiving an enable signal from the Power Control Unit to enable the PLL, such as when the core is operating normally in the C0 state.

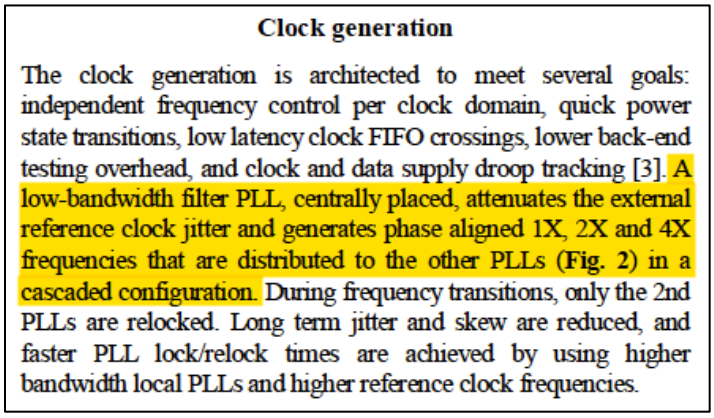


4.2.4.1 Core C0 State

The normal operating state of a core where code is being executed.

Intel Datasheet, *Desktop 3rd Generation Intel Core Processor Family, Desktop Intel Pentium Processor Family, and Desktop Intel Celeron Processor Family*, Volume 1 of 2 (Nov. 2013), at 52.

60. On information and belief, when enabled by the enable signal, the clock delay device in the Intel Accused Products provides output clock pulses that are synchronized with the input clock pulses. For example, when the one or more distributed PLLs in the Intel Accused Products is enabled, it provides output clock pulses that are synchronized with the input clock pulses.



Clock generation

The clock generation is architected to meet several goals: independent frequency control per clock domain, quick power state transitions, low latency clock FIFO crossings, lower back-end testing overhead, and clock and data supply droop tracking [3]. A low-bandwidth filter PLL, centrally placed, attenuates the external reference clock jitter and generates phase aligned 1X, 2X and 4X frequencies that are distributed to the other PLLs (**Fig. 2**) in a cascaded configuration. During frequency transitions, only the 2nd PLLs are relocked. Long term jitter and skew are reduced, and faster PLL lock/relock times are achieved by using higher bandwidth local PLLs and higher reference clock frequencies.

Nasser Kurd et al., *Next Generation Intel Micro-architecture (Nehalem) Clocking Architecture*, IEEE SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS (2008), at 62 (highlighting added).

61. By making, using, testing, offering for sale, selling, and/or importing integrated circuits, including but not limited to the Intel Accused Products, Intel has injured Janus and is

liable to Janus for directly infringing one or more claims of the ’620 patent, including at least claim 1, pursuant to 35 U.S.C. § 271(a).

62. On information and belief, Intel also indirectly infringes the ’620 patent by actively inducing infringement under 35 U.S.C. § 271(b).

63. On information and belief, Intel has had knowledge of the ’620 patent since at least May 15, 2001, when the USPTO issued Intel’s U.S Patent No. 6,233,690. During prosecution of the ’690 patent, the USPTO cited the ’620 patent as relevant prior art and the ’620 patent appears on the face of the ‘690 patent as one of the references considered.

64. In the alternative, on information and belief, Intel has had knowledge of the ’620 patent since at least the date of service of this Complaint or shortly thereafter, and on information and belief, Intel knew of the ’620 patent and knew of its infringement, including by way of this lawsuit.

65. On information and belief, Intel intended to induce patent infringement by third-party customers and users of the Intel Accused Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. Intel specifically intended and was aware that the normal and customary use of the accused products would infringe the ’620 patent. Intel performed the acts that constitute induced infringement, and would induce actual infringement, with the knowledge of the ’620 patent and with the knowledge that the induced acts would constitute infringement. For example, Intel provides the Intel Accused Products, which are capable of operating in a manner that infringes one or more claims of the ’620 patent, including at least claim 1, and Intel further provides documentation and training materials that cause customers of the Intel Accused Products to utilize the products and services in a manner that directly infringes one or more claims of the ’620 patent. By providing instruction and training to customers on how to use the Intel Accused Products, Intel specifically intended to induce infringement of the ’620 patent, including at least claim 1. On information and belief, Intel engaged in such inducement to promote the sales of the Intel Accused Products and to actively induce its customers to infringe

the ’620 patent. Accordingly, Intel has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the ’620 patent, knowing that such use constitutes infringement of the ’620 patent.

66. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’620 patent.

67. As a result of Intel’s infringement of the ’620 patent, Janus has suffered monetary damages, and seeks recovery in an amount adequate to compensate for Intel’s infringement, but in no event less than a reasonable royalty for the use made of the invention by Intel together with interest and costs as fixed by the Court.

COUNT II
INFRINGEMENT OF U.S. PATENT NO. 5,987,620
(AGAINST ALTERA AND INTEL)

68. Janus restates and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

69. U.S. Patent No. 5,987,620 (“the ’620 patent”), entitled “Method and Apparatus for a Self-Timed and Self-Enabled Distributed Clock,” was filed on November 14, 1997. The named inventor on the face of the ’620 patent is Dr. Thang Tran, of Austin, Texas. Janus is the owner by assignment of the ’620 patent. A true and correct copy of the ’620 patent is attached hereto as Exhibit A.

70. The ’620 patent has been cited by at least 94 United States patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ’620 patent as relevant prior art:

- Facebook, Inc.;
- Globalfoundries, Inc.;
- Intel Corporation;
- International Business Machines, Inc.;
- Lockheed Martin Corporation;
- Micron Technology, Inc.;
- Rambus, Inc.;
- Renesas Electronics Corporation;

- STMicroelectronics, Inc.;
- Sun Microsystems, Inc.; and
- Texas Instruments, Inc.

71. On information and belief, Intel and Altera make, use, sell, offer to sell, and/or import the Cyclone V FPGAs and SoCs, the Stratix IV FPGAs and SoCs, the Stratix V FPGAs and SoCs, the Stratix 10 FPGAs and SoCs, the Arria V FPGAs and SoCs, and the Arria 10 FPGAs and SoCs (collectively, "the Altera Accused Products").

72. On information and belief, to the extent the preamble of claim 16 of the '620 patent is limiting, the Altera Accused Products comprise a distributed clock system for a digital circuit. For example, the Altera Accused Products contain global clock networks, regional clock networks, and periphery clock networks, all of which are organized into a hierarchical structure.

Global Clock Networks

Cyclone V devices provide GCLKs that can drive throughout the device. The GCLKs serve as low-skew clock sources for functional blocks, such as adaptive logic modules (ALMs), digital signal processing (DSP), embedded memory, and PLLs. Cyclone V I/O elements (IOEs) and internal logic can also drive GCLKs to create internally-generated global clocks and other high fan-out control signals, such as synchronous or asynchronous clear and clock enable signals.

Regional Clock Networks

RCLK networks are only applicable to the quadrant they drive into. RCLK networks provide the lowest clock insertion delay and skew for logic contained within a single device quadrant. The Cyclone V IOEs and internal logic within a given quadrant can also drive RCLKs to create internally generated regional clocks and other high fan-out control signals.

Periphery Clock Networks

Cyclone V devices provide only horizontal PCLKs from the left periphery.

Clock outputs from the programmable logic device (PLD)-transceiver interface clocks, horizontal I/O pins, and internal logic can drive the PCLK networks.

PCLKs have higher skew when compared with GCLK and RCLK networks. You can use PCLKs for general purpose routing to drive signals into and out of the Cyclone V device.

Altera Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration, ALTERA TECHNICAL DOCUMENTATION, at 4-4, 4-6, and 4-8 (2016).

73. On information and belief, the Altera Accused Products comprise a first self clock that provides first output clock pulses when enabled.

Internal Logic

You can drive each GCLK, RCLK, and horizontal PCLK network using LAB-routing and row clock to enable internal logic to drive a high fan-out, low-skew signal.

Note: Internally-generated GCLKs, RCLKs, or PCLKs cannot drive the Cyclone V PLLs. The input clock to the PLL has to come from dedicated clock input pins, PLL-fed GCLKs, or PLL-fed RCLKs.

Altera Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration, ALTERA TECHNICAL DOCUMENTATION, at 4-12 (2016).

74. On information and belief, the first self clock of the Altera Accused Products comprises an output, a first input coupled to the output and a second input. For example, the first self clock of the Altera Accused Products comprises a clock input, a plurality of outputs, and a feedback input (i.e., an input coupled to the output).

Clock Sources Per Quadrant

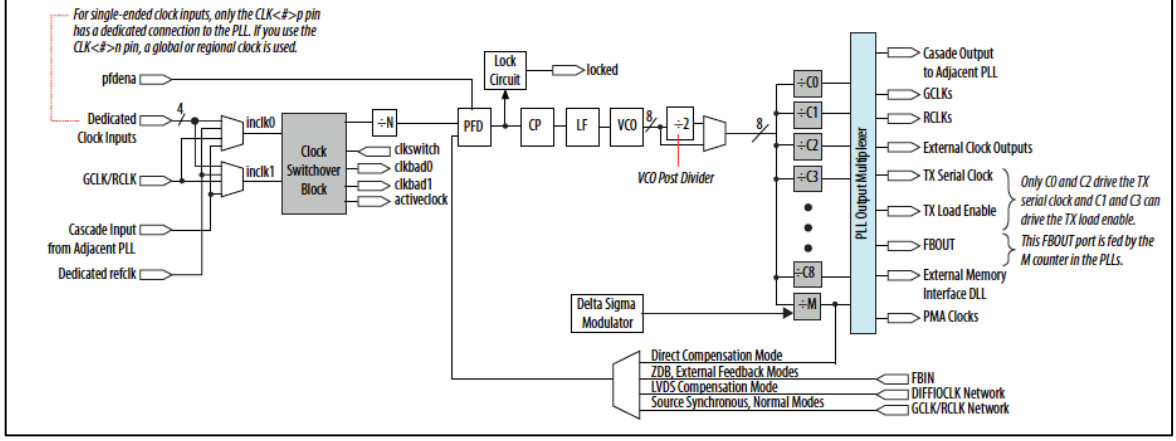
The Cyclone V devices provide 30 section clock (SCLK) networks in each spine clock per quadrant. The SCLK networks can drive six row clocks in each logic array block (LAB) row, nine column I/O clocks, and two core reference clocks. The SCLKs are the clock resources to the core functional blocks, PLLs, and I/O interfaces of the device.

A spine clock is another layer of routing between the GCLK, RCLK, and PCLK networks before each clock is connected to the clock routing for each LAB row. The settings for spine clocks are transparent. The Quartus Prime software automatically routes the spine clock based on the GCLK, RCLK, and PCLK networks.

The following figure shows SCLKs driven by the GCLK, RCLK, PCLK, or the PLL feedback clock networks in each spine clock per quadrant. The GCLK, RCLK, PCLK, and PLL feedback clocks share the same routing to the SCLKs. To ensure successful design fitting in the Quartus Prime software, the total number of clock resources must not exceed the SCLK limits in each region.

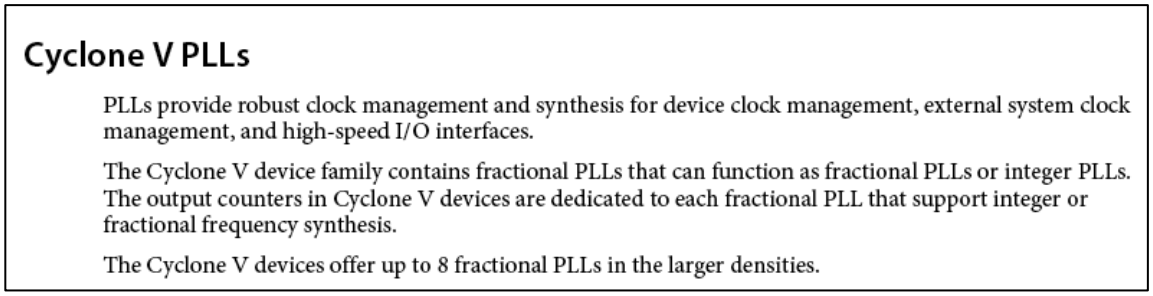
Altera Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration, ALTERA TECHNICAL DOCUMENTATION, at 4-10 (2016).

Figure 4-23: Fractional PLL High-Level Block Diagram for Cyclone V Devices



Altera Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration, ALTERA TECHNICAL DOCUMENTATION, at 4-28 (2016).

75. On information and belief, the first self clock of the Altera Accused Products is enabled by each clock pulse received at the second input and synchronizes the first output clock pulses with respective clock signals received at the second input.



Cyclone V PLLs

PLLs provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.

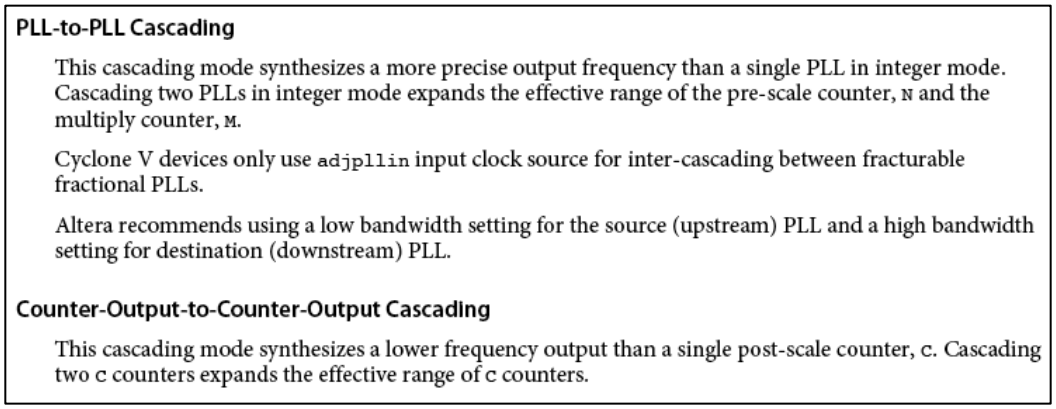
The Cyclone V device family contains fractional PLLs that can function as fractional PLLs or integer PLLs. The output counters in Cyclone V devices are dedicated to each fractional PLL that support integer or fractional frequency synthesis.

The Cyclone V devices offer up to 8 fractional PLLs in the larger densities.

Altera Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration, ALTERA TECHNICAL DOCUMENTATION, at 4-19 (2016).

76. On information and belief, the Altera Accused Products comprise a second self clock that provides second output clock pulses when enabled.

77. On information and belief, the second self clock of the Altera Accused Products comprises an output, a first input coupled to the output of the second self clock, and a second input coupled to the output of the first self clock. For example, the second self clock of the Altera Accused Products comprises a clock input from an earlier, cascaded PLL (i.e., a second input coupled to the output of the first self clock), a plurality of outputs, and a feedback input (i.e., a first input coupled to the output of the second self clock).



PLL-to-PLL Cascading

This cascading mode synthesizes a more precise output frequency than a single PLL in integer mode. Cascading two PLLs in integer mode expands the effective range of the pre-scale counter, N and the multiply counter, M.

Cyclone V devices only use `adjpllin` input clock source for inter-cascading between fracturable fractional PLLs.

Altera recommends using a low bandwidth setting for the source (upstream) PLL and a high bandwidth setting for destination (downstream) PLL.

Counter-Output-to-Counter-Output Cascading

This cascading mode synthesizes a lower frequency output than a single post-scale counter, C. Cascading two C counters expands the effective range of C counters.

Altera Cyclone V Device Handbook, Volume 1: Device Interfaces and Integration, ALTERA TECHNICAL DOCUMENTATION, at 4-29 (2016).

78. On information and belief, the second self clock of the Altera Accused Products is enabled by each clock pulse received at the second input and synchronizes the second output clock pulse with respective clock signals received at the second input of the second self clock.

79. By making, using, testing, offering for sale, selling, and/or importing integrated circuits, including but not limited to the Altera Accused Products, Intel and Altera have injured Janus and are liable to Janus for directly infringing one or more claims of the ’620 patent, including at least claim 16, pursuant to 35 U.S.C. § 271(a).

80. On information and belief, Intel and Altera also indirectly infringe the ’620 patent by actively inducing infringement under 35 U.S.C. § 271(b).

81. On information and belief, Intel and Altera have had knowledge of the ’620 patent since at least May 15, 2001, when the USPTO issued Intel’s U.S Patent No. 6,233,690. During prosecution of the ’690 patent, the USPTO cited the ’620 patent as relevant prior art and the ’620 patent appears on the face of the ‘690 patent as one of the references considered.

82. In the alternative, on information and belief, Intel and Altera have had knowledge of the ’620 patent since at least the date of service of this Complaint or shortly thereafter, and on information and belief, Intel and Altera knew of the ’620 patent and knew of their infringement, including by way of this lawsuit.

83. On information and belief, Intel and Altera intended to induce patent infringement by third-party customers and users of the Altera Accused Products and had knowledge that the inducing acts would cause infringement or were willfully blind to the possibility that their inducing acts would cause infringement. Intel and Altera specifically intended and were aware that the normal and customary use of the accused products would infringe the ’620 patent. Intel and Altera performed the acts that constitute induced infringement, and would induce actual infringement, with the knowledge of the ’620 patent and with the knowledge that the induced acts would constitute infringement. For example, Intel and Altera provide the Altera Accused Products, which are capable of operating in a manner that infringes one or more claims of the ’620 patent, including at least claim 16, and Intel and Altera further provide documentation and

training materials that cause customers of the Altera Accused Products to utilize the products and services in a manner that directly infringes one or more claims of the ’620 patent. By providing instruction and training to customers on how to use the Altera Accused Products, Intel and Altera specifically intended to induce infringement of the ’620 patent, including at least claim 16. On information and belief, Intel and Altera engaged in such inducement to promote the sales of the Altera Accused Products and to actively induce their customers to infringe the ’620 patent. Accordingly, Intel and Altera have induced and continue to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the ’620 patent, knowing that such use constitutes infringement of the ’620 patent.

84. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’620 patent.

85. As a result of Intel’s and Altera’s infringement of the ’620 patent, Janus has suffered monetary damages, and seeks recovery in an amount adequate to compensate for Intel’s and Altera’s infringement, but in no event less than a reasonable royalty for the use made of the invention by Intel and Altera together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Janus respectfully requests that this Court enter:

A. A judgment in favor of Plaintiff Janus that Intel and Altera have infringed the '620 patent, either literally and/or under the doctrine of equivalents;

B. An award of damages resulting from Intel's and Altera's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order requiring Intel and Altera to provide accountings and to pay supplemental damages to Janus, including, without limitation, prejudgment and post-judgment interest; and

D. Any and all other relief to which Janus may show itself to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Janus requests a trial by jury of any issues so triable by right.

Dated: February 3, 2017

Respectfully submitted,

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