IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SMART SEMICONDUCTOR, LLC, Plaintiff, v. MICRON TECHNOLOGY, INC., Defendants.	**Civil Action No. _____** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Smart Semiconductor, LLC ("Smart Semiconductor" or "Plaintiff"), for its Complaint against Defendant Micron Technology, Inc. ("Defendant" or "Micron") alleges the following:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq*.

THE PARTIES

2. Plaintiff is a limited liability company organized under the laws of the State of Delaware and can be served through its registered agent at 717 North Union Street, Wilmington, Delaware 19805.

3. Upon information and belief, Micron is a corporation organized and existing under the laws of Delaware, with a place of business at 8000 S. Federal Way, P.O. Box 6, Boise, Idaho 83707-0006, and can be served through its registered agent, Corporation Service Company, 2711 Centerville Road, Suite 400, Wilmington, Delaware 19808. Upon information and belief, Micron sells and offers to sell products and services throughout the United States,

including in this judicial district, and introduces products and services that into the stream of commerce and that incorporate infringing technology knowing that they would be sold in this judicial district and elsewhere in the United States.

JURISDICTION AND VENUE

4. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code.

5. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

6. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b), (c), (d) and/or 1400(b). On information and belief, Defendant conducts business in this District, the claims alleged in this Complaint arise in this District, and the acts of infringement have taken place and are continuing to take place in this District.

7. On information and belief, Defendant is subject to this Court's general and specific personal jurisdiction because Defendant has sufficient minimum contacts within the State of Delaware, pursuant to due process and/or the Del. Code. Ann. Tit. 3, § 3104 because Defendant purposefully availed itself of the privileges of conducting business in the State of Delaware, because Defendant regularly conducts and solicits business within the State of Delaware, and because Plaintiff's causes of action arise directly from Defendant's business contacts and other activities in the State of Delaware. Further, this Court has personal jurisdiction over Defendant because Defendant is incorporated in Delaware and purposely availed itself of the privileges and benefits of the laws of the State of Delaware.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,242,254

8. The allegations set forth in the foregoing paragraphs 1 through 7 are incorporated into this First Claim for Relief.

9. On July 10, 2007, U.S. Patent No. 7,242,254 ("the '254 patent"), entitled "Adjustable Lock-In Circuit for Phase-Locked Loops," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '254 patent is attached as Exhibit 1.

10. Plaintiff is the assignee and owner of the right, title and interest in and to the '254 patent, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement of them.

11. Upon information and belief, Defendant has and continues to directly infringe at least claims 1, 8, 9, 10, 14, 18, and 19 of the '254 patent by making, using, selling, importing and/or providing and causing to be used adjustable lock-in circuits that fall within the scope of claims 1, 8, 9, 10, 14, 18, and 19 of the '254 patent, including, but not limited to, the products with the following designations or trade names: DDR4 SDRAM (Part # MT40xx), DDR3 SDRAM (Part # MT41xx), DDR2 SDRAM (Part # MT47xx), DDR SDRAM (Part # MT46xx) (the "Infringing Instrumentalities").

12. Claim 1 of the '254 patent generally recites an adjustable lock-in circuit for enabling any phase-locked loop to become locked according to a targeted lock-in time, comprising: a feedback line connected with the output of the adjustable lock-in circuit and also coupled to the output of a filter; a sensor for comparing a feedback voltage with a reference voltage and providing its output; two stacked PMOS transistors connected between power supply and the output; and two stacked NMOS transistors connected between the output and ground.

13. On information and belief, the Infringing Instrumentalities infringe claim 1 of the '254 patent because they comprise an adjustable lock-in circuit for enabling any phase-locked loop to become locked according to a targeted lock-in time, the adjustable lock-in circuit

comprising: two stacked PMOS transistors connected between power supply and the output, two stacked NMOS transistors connected between the output and the ground, and a feedback line. Based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, the feedback line, and the fact that, on information and belief, the Infringing Instrumentalities are capable of a substantial increase in acquisition time compared to phase-locked loops using conventional charge pump configurations, on information and belief the feedback line is connected with the output of the adjustable lock-in circuit and also coupled to the output of a filter, and the circuit comprises a sensor for comparing a feedback voltage with a reference voltage and providing its output.

14. Claim 8 of the ’254 patent generally recites the circuit as recited in claim 1 wherein the sensor is an operational amplifier.

15. On information and belief, the Infringing Instrumentalities infringe claim 8 of the ’254 patent because they infringe claim 1 for the reasons set forth in paragraph 13 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the sensor is an operational amplifier.

16. Claim 9 of the ’254 patent generally recites the circuit as recited in claim 1 wherein the sensor is an amplifier with a reference voltage.

17. On information and belief, the Infringing Instrumentalities infringe claim 9 of the ’254 patent because they infringe claim 1 for the reasons set forth in paragraph 13 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the sensor is an amplifier with a reference voltage.

18. Claim 10 of the ’254 patent generally recites the circuit as recited in claim 1 wherein the sensor is a comparator with a reference voltage.

19. On information and belief, the Infringing Instrumentalities infringe claim 10 of the ’254 patent because they infringe claim 1 for the reasons set forth in paragraph 13 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the sensor is a comparator with a reference voltage.

20. Claim 14 of the ’254 patent generally recites the circuit as recited in claim 1 further comprising a power-down PMOS transistor and a power-down inverter so that no current flows into the circuit during power-down mode.

21. On information and belief, the Infringing Instrumentalities infringe claim 14 of the ’254 patent because they infringe claim 1 for the reasons set forth in paragraph 13 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the Infringing Instrumentalities further comprise a power-down PMOS transistor and a power-down inverter so that no current flows into the circuit during power-down mode.

22. Claim 18 of the ’254 patent generally recites the circuit as recited in claim 1 wherein the reference voltage is based on selecting tap of a segmented resistor string by a digital circuit that is coupled to the segmented resistor string.

23. On information and belief, the Infringing Instrumentalities infringe claim 18 of the ’254 patent because they infringe claim 1 for the reasons set forth in paragraph 13 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the reference voltage is

based on selecting tap of a segmented resistor string by a digital circuit that is coupled to the segmented resistor string.

24. Claim 19 of the ’254 patent generally recites the circuit as recited in claim 1 wherein the adjustable lock-in circuit is applied to all phase-locked loops without regard to architectures, topologies, and schematics.

25. On information and belief, the Infringing Instrumentalities infringe claim 19 of the ’254 patent because they infringe claim 1 for the reasons set forth in paragraph 13 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the adjustable lock-in circuit is applied to all phase-locked loops without regard to architectures, topologies, and schematics.

26. Plaintiff has been harmed by Defendant’s infringing activities.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,224,233

27. The allegations set forth in the foregoing paragraphs 1 through 26 are incorporated into this Second Claim for Relief.

28. On May 29, 2007, U.S. Patent No. 7,224,233 (“the ’233 patent”), entitled “Smart Lock-In Circuit for Phase-Locked Loops,” was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the ’233 patent is attached as Exhibit 2.

29. Plaintiff is the assignee and owner of the right, title and interest in and to the ’233 patent, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement of them.

30. Upon information and belief, Defendant has and continues to directly infringe at least claims 1, 2, 4, 6, 12, 15, and 19 of the ’233 patent by making, using, selling, importing and/or providing and causing to be used smart lock-in circuits that fall within the scope of claims 1, 2, 4, 6, 12, 15, and 19 of the ’233 patent, including, but not limited to, the products with the

following designations or trade names: DDR4 SDRAM (Part # MT40xx), DDR3 SDRAM (Part # MT41xx), DDR2 SDRAM (Part # MT47xx), DDR SDRAM (Part # MT46xx) (the "Infringing Instrumentalities").

31. Claim 1 of the '233 patent generally recites a smart lock-in circuit for enabling any phase-locked loop including at least a filter to become locked according to schedule, comprising: a feedback line connected to an output and input of the smart lock-in circuit and also coupled to an output of a filter; a sensor for sensing a voltage at the filter output, comparing with a midpoint voltage decided by device aspect ratios of the sensor, and providing its response; two stacked PMOS transistors connected between power supply and the output; and two stacked NMOS transistors connected between the output and ground.

32. On information and belief, the Infringing Instrumentalities infringe claim 1 of the '233 patent because they comprise a smart lock-in circuit for enabling any phase-locked loop including at least a filter to become locked according to schedule, comprising: two stacked PMOS transistors connected between power supply and the output, two stacked NMOS transistors connected between the output and the ground, and a feedback line. Based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, the feedback line, and the fact that, on information and belief, the Infringing Instrumentalities are capable of a substantial increase in acquisition time compared to phase-locked loops using conventional charge pump configurations, on information and belief the feedback line is connected to an output and input of the smart lock-in circuit and also coupled to an output of a filter, and the circuit comprises a sensor for sensing a voltage at the filter input, comparing with a midpoint voltage decided by device aspect ratios of the sensor, and providing its response.

33. Claim 2 of the ’233 patent generally recites the circuit as recited in claim 1 wherein the sensor is a lower-voltage sensor whose device aspect ratios determine a lower midpoint voltage.

34. On information and belief, the Infringing Instrumentalities infringe claim 2 of the ’233 patent because they infringe claim 1 for the reasons set forth in paragraph 32 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the sensor is a lower-voltage sensor whose device aspect ratios determine a lower midpoint voltage.

35. Claim 4 of the ’233 patent generally recites the circuit as recited in claim 1 wherein the sensor is a higher-voltage sensor whose device aspect ratios determine a higher midpoint voltage.

36. On information and belief, the Infringing Instrumentalities infringe claim 4 of the ’233 patent because they infringe claim 1 for the reasons set forth in paragraph 32 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the sensor is a higher-voltage sensor whose device aspect ratios determine a higher midpoint voltage.

37. Claim 6 of the ’233 patent generally recites the circuit as recited in claim 1 wherein the sensor is both a lower-voltage sensor and a higher voltage sensor.

38. On information and belief, the Infringing Instrumentalities infringe claim 6 of the ’233 patent because they infringe claim 1 for the reasons set forth in paragraph 32 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the sensor is both a lower-voltage sensor and a higher voltage sensor.

39. Claim 12 of the ’233 patent generally recites the circuit as recited in claim 1 further comprising a power-down NMOS transistor so that no current flows into the circuit during power-down mode.

40. On information and belief, the Infringing Instrumentalities infringe claim 12 of the ’233 patent because they infringe claim 1 for the reasons set forth in paragraph 32 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the Infringing Instrumentalities further comprise a power-down a power-down NMOS transistor so that no current flows into the circuit during power-down mode.

41. Claim 15 of the ’233 patent generally recites the circuit as recited in claim 1 further comprising a power-down PMOS transistor and a power-down inverter so that no current flows into the circuit during power-down mode.

42. On information and belief, the Infringing Instrumentalities infringe claim 15 of the ’233 patent because they infringe claim 1 for the reasons set forth in paragraph 32 above, and because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the Infringing Instrumentalities further comprise a power-down PMOS transistor and a power-down inverter so that no current flows into the circuit during power-down mode.

43. Claim 19 of the ’233 patent generally recites the circuit as recited in claim 1 wherein the smart lock-in circuit is applied to all phase-locked loops including at least a filter without regard to architectures, topologies, and schematics.

44. On information and belief, the Infringing Instrumentalities infringe claim 19 of the ’233 patent because they infringe claim 1 for the reasons set forth in paragraph 32 above, and

because, based on at least the presence of the two stacked PMOS transistors, the two stacked NMOS transistors, and the feedback line, on information and belief the smart lock-in circuit is applied to all phase-locked loops including at least a filter without regard to architectures, topologies, and schematics.

45. Plaintiff has been harmed by Defendant's infringing activities.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 7,515,003

46. The allegations set forth in the foregoing paragraphs 1 through 45 are incorporated into this Third Claim for Relief.

47. On April 7, 2009, U.S. Patent No. 7,515,003 ("the '003 patent"), entitled "Filter-Based Lock-In Circuits for PLL and Fast System Startup," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '003 patent is attached as Exhibit 3.

48. Plaintiff is the assignee and owner of the right, title and interest in and to the '003 patent, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement of them.

49. Upon information and belief, Defendant has and continues to directly infringe at least claims 1, 2, 6, 11, 15, and 20 of the '003 patent by making, using, selling, importing and/or providing and causing to be used smart lock-in circuits that fall within the scope of 1, 2, 6, 11, 15, and 20 of the '003 patent, including, but not limited to, the products with the following designations or trade names: DDR4 SDRAM (Part # MT40xx), DDR3 SDRAM (Part # MT41xx), DDR2 SDRAM (Part # MT47xx), DDR SDRAM (Part # MT46xx) (the "Infringing Instrumentalities").

50. Claim 1 of the '003 patent generally recites a filter-based lock-in circuit used in a system for reducing system startup time and system latency time, comprising: an upper transistor

and a lower transistor connected in series between a power supply and a ground having a shared terminal which becomes a single bidirectional node, wherein the shared terminal is defined by a junction between the upper transistor and the lower transistor; a sensing inverter for sensing a voltage at the single bidirectional node and comparing it with an input transition voltage of the sensing inverter which causes an output of the sensing inverter to be centered at half the power supply voltage wherein an input terminal of the sensing inverter is connected to the single bidirectional node; a logic gate coupled between an output terminal of the sensing inverter and a gate terminal of the upper transistor; and wherein an initial voltage at the single bidirectional node of the filter-based lock-in circuit is almost the same as the input transition voltage of the sensing inverter.

51. On information and belief, the Infringing Instrumentalities infringe claim 1 of the ’003 patent because they comprise a filter-based lock-in circuit used in a system for reducing system startup time and system latency time, comprising: an upper PMOS transistor and a lower NMOS transistor connected in series between power supply and having a shared terminal which, on information and belief, becomes a single bidirectional node, wherein the shared terminal is defined by a junction between the upper PMOS transistor and the lower NMOS transistor; and a feedback line. Based on at least the presence of the upper PMOS transistor, the lower NMOS transistor, the bidirectional node, the feedback line, and the fact that, on information and belief, the Infringing Instrumentalities are capable of a substantial increase in acquisition time compared to phase-locked loops using conventional charge pump configurations, on information and belief the filter-based lock-in circuit of the Infringing Instrumentalities comprises: a sensing inverter for sensing a voltage at the single bidirectional node and comparing it with an input transition voltage of the sensing inverter to be centered at half the power supply voltage wherein an input

terminal of the sensing inverter is connected to the singe bidirectional node; a logic gate coupled between an output terminal of the sensing inverter and a gate terminal of the upper PMOS transistor; and wherein an initial voltage at the single bidirectional node of the filter-based lock-in circuit is almost the same as the input transition voltage of the sensing inverter.

52. Claim 2 of the ’003 patent generally recites the circuit as recited in claim 1 wherein the upper transistor and the lower transistor are a PMOS transistor and an NMOS transistor, respectively, the shared terminal is a drain terminal that the PMOS transistor and the NMOS transistor have, and the logic gate comprises an odd number of inverters, wherein the NMOS transistor has a gate terminal which is connected to ground.

53. On information and belief, the Infringing Instrumentalities infringe claim 2 of the ’003 patent because they infringe claim 1 for the reasons set forth in paragraph 51 above, and because, based on at least the presence of the upper PMOS transistor, the lower NMOS transistor, the bidirectional node, and the feedback line, on information and belief the shared terminal is a drain terminal that the PMOS transistor and the NMOS transistor have, and the logic gate comprises an odd number of inverters, wherein the NMOS transistor has a gate terminal which is connected to ground.

54. Claim 6 of the ’003 patent generally recites the circuit as recited in claim 1 wherein the single bidirectional node of the filter-based lock-in circuit is also connected to a terminal, which is defined by a junction between a resistor and a capacitor in a low-pass filter of a phase-locked loop.

55. On information and belief, the Infringing Instrumentalities infringe claim 6 of the ’003 patent because they infringe claim 1 for the reasons set forth in paragraph 51 above, and because, based on at least the presence of the upper PMOS transistor, the lower NMOS

transistor, the bidirectional node, and the feedback line, on information and belief the single bidirectional node of the filter-based lock-in circuit is also connected to a terminal, which is defined by a junction between a resistor and a capacitor in a low-pass filter of a phase-locked loop.

56. Claim 11 of the ’003 patent generally recites the circuit as recited in claim 1 wherein the system is a consumer electronics system.

57. On information and belief, the Infringing Instrumentalities infringe claim 11 of the ’003 patent because they infringe claim 1 for the reasons set forth in paragraph 51 above, and because, on information and belief, the system is a consumer electronics system.

58. Claim 15 of the ’003 patent generally recites the circuit as recited in claim 1 wherein the system is a cellular phone system.

59. On information and belief, the Infringing Instrumentalities infringe claim 15 of the ’003 patent because they infringe claim 1 for the reasons set forth in paragraph 51 above, and because, on information and belief, the system is a cellular phone system.

60. Claim 20 of the ’003 patent generally recites the circuit as recited in claim 1 wherein the filter-based lock-in circuit is developed for use in all types of systems containing at least a phase-locked loop without regard to architecture and topology.

61. On information and belief, the Infringing Instrumentalities infringe claim 20 of the ’003 patent because they infringe claim 1 for the reasons set forth in paragraph 51 above, and because, on information and belief, the filter-based lock-in circuit is developed for use in all types of systems containing at least a phase-locked loop without regard to architecture and topology.

62. Plaintiff has been harmed by Defendant’s infringing activities.

JURY DEMAND

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiff demands a trial by jury on all issues triable as such.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff demands judgment for itself and against Defendant as follows:

A. An adjudication that Defendant has infringed the ’254, ’233, and ’003 patents;

B. An award of damages to be paid by Defendant adequate to compensate Plaintiff for Defendant’s past infringement of the ’254, ’233, and ’003 patents, and any continuing or future infringement through the date such judgment is entered, including interest, costs, expenses and an accounting of all infringing acts including, but not limited to, those acts not presented at trial;

C. A declaration that this case is exceptional under 35 U.S.C. § 285, and an award of Plaintiff’s reasonable attorneys’ fees; and

D. An award to Plaintiff of such further relief at law or in equity as the Court deems just and proper.

Dated: April 21, 2017

DEVLIN LAW FIRM LLC

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