IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLORADO

Civil Action No.: 1:17-cv-687

Anza Technology, Inc.,

Plaintiff,

v.

Xilinx, Inc.,

Defendant.

FIRST AMENDED COMPLAINT

Plaintiff Anza Technology, Inc. ("Anza" or "Plaintiff"), by and through its undersigned counsel complains and alleges against Defendant Xilinx, Inc. ("Defendant") as follows:

NATURE OF THE ACTION

1. This is a civil action for infringement of a patent arising under the laws of the United States relating to patents, 35 U.S.C. § 101, *et seq.*, including, without limitation, 35 U.S.C. §§ 271, 281. Plaintiff Anza seeks monetary damages for patent infringement.

JURISDICTION AND VENUE

2. This court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a) and pursuant to the patent laws of the United States of America, 35 U.S.C. § 101, *et seq.*

3. Plaintiff is informed, believes and thereon alleges that Defendant conducts substantial business directly and/or through third parties or agents in this judicial district by selling and/or offering to sell the Accused Products and/or by conducting other business in this judicial district. Defendant maintains an office at 3100 Logic Drive, Longmont, Colorado, and therefore also engages in business in this district. Accordingly, venue properly lies within the District of Colorado pursuant to the provisions of 28 U.S.C. §§ 1391(b), (c), and (d) and 1400(b).

4. This Court also has personal jurisdiction over the Defendant because its infringing

activities (which includes, without limitation, using, selling and/or offering for sale the infringing products) occur in the State of Colorado and the District of Colorado. This Court also has personal jurisdiction over Defendant because it maintains an office in Longmont, Colorado, and contracts Luscombe Engineering, Inc., a company that is located in Broomfield, Colorado, as its sales representative. Plaintiff is also informed and believes that Defendant transacts continuous and systematic business within the State and the District of Colorado by placing infringing products in the stream of interstate commerce with the expectation that they would be used, sold and/or offered for sale within the State of Colorado and the District of Colorado.

PARTIES

5. Plaintiff Anza is a corporation organized and existing under the laws of the State of California with an office and principal place of business at 4121 Citrus Avenue, Suite 4, Rocklin, California 95677. Anza is a designer, manufacturer and seller of products directed to the manufacture and assembly of electronics including the bonding of electrostatic-discharge-sensitive devices.

6. Defendant is a corporation organized and existing under the laws of the State of Delaware, with a principal place of business at 2100 Logic Drive, San Jose, CA. In addition, Defendant maintains an office at 3100 Logic Drive, Longmont, Colorado.

BACKGROUND

7. Defendant designs, imports, sells, offers for sale, and/or uses products with electrostatic-discharge-sensitive integrated circuit ("IC") chips that are assembled utilizing techniques and methods to guard against damage from electrostatic discharge in a manner that infringes the Asserted Patents.

8. Electrostatic Discharge ("ESD") failure is a major concern in the assembly of ICs and products containing them. ESD damage is a well-known phenomenon in the electronics industry and certain standards have been developed by industry-recognized standards setting organizations (JEDEC, the IEC and/or the ESDA) to identify risks and recommend protocols to minimize the risk of damage ESD sensitive devices during assembly and manufacture. An ESD

event can change structures in ESD sensitive devices, potentially damaging them.

9. Complementary Metal-Oxide Semiconductors ("CMOS") are a type of IC commonly used in microprocessors, microcontrollers, static RAM and other digital logic circuits. CMOS ICs are known to be ESD sensitive and are highly susceptible to damage from electrostatic events. CMOS chips (known as "dies") are typically cut into individual pieces from a larger wafer of silicon. They are picked up and placed on a substrate or in a package for transport and placement on a Printed Circuit Board (PCB). An example of a packaged device is a ball grid array or "BGA" IC (pictured at right).

10. A ball grid array is a type of surface-mount packaging (a chip carrier) used for integrated circuits. BGA packages are used to permanently mount devices such as microprocessors. A BGA can provide more interconnection pins than a dual in-line or flat package.

11. A ball grid array mounting system (or a variation thereof, *e.g.*, FBGA, TBGA, PBGA etc.) (collectively referred to herein as "BGA") is a commonly-used method of packaging CMOS ICs in modern electronics. A BGA IC package is fabricated when individual CMOS IC dies are inserted in a package or case. The package uses "solder balls" as conduits of electrical connectivity. Thereafter, BGA IC packages are surface mounted to PCBs *via* another array of solder balls.

12. In the process of bonding the die into a BGA package or mounting the finished BGA IC to a PCB, heat is applied, causing the solder balls to melt and bind the CMOS IC die to the BGA package or, alternatively, to bind the packaged BGA IC to a PCB.

13. Naturally-occurring electrostatic charges (of varying degrees) build up whenever anything, including but not limited to mounting tools, come in contact with the die during placement in the package. Electrostatic charges also build-up when the fabricated BGA package is placed in a tray or on a tape for transport. Similarly, charges build up when a BGA package is removed from a transport vessel and placed on a PCB for bonding.

14. Every time an ESD sensitive device is handled, electrostatic charges to one degree or another are generated. Simple movements of an ESD sensitive device can create an electrical charge (commonly referred to as "tribocharging"). Tribocharging is a contact electrification process that enables buildup of static electricity due to touching or rubbing of surfaces in specific combinations of two dissimilar materials.

15. It is well-known in the industry that tribocharging occurs in all automated assembly processes with, *e.g.*, the rubbing of conveyor belts or the touching of ICs and product parts with carrier trays or tapes. Electrostatic charges are also created at several places in an automated production line where ICs are made, transported, touched or handled.

16. Since automated production line processes naturally generate electrostatic charges, caution must be taken to avoid damaging ESD sensitive components when they are moved, picked up and placed in contact with one another.

17. As early as February 1999, the inventors of the Asserted Patents began developing methods of making and using dissipative bonding tools that avoid or reduce damage to ICs from ESD events.

18. Since then, broadly-accepted standards have been promulgated by standards-setting organizations, such as the ESD Association and JEDEC, for the proper handling of ESD sensitive devices.

19. By way of example, and not limitation, the ANSI/ESD S20.20 standard (also referred to herein as the "ANSI Standard"), as promulgated by the ESD Association (ESDA), outlines some of the requirements for the design, implementation and testing of ESD Control Programs related to the manufacture, assembly, processing, installation, packaging, labeling, servicing, testing and any other handling of electrical or electronic parts, assemblies and equipment susceptible to ESD damage.

20. Among other things, ANSI/ESD S4.1, which is expressly incorporated into the ANSI Standard, recommends that work surfaces, have a resistance in the range of between 1×10^6 ohms and 1×10^9 ohms.

21. ANSI S20.20 at Section 8.1 provides that conductors in "Grounding/Equipotential Bonding Systems" that come into contact with ESD sensitive devices have the same electrical potential. ANSI/ESD S6.1, also expressly incorporated in the ANSI Standard, further specifies that during "Grounding" and "Equipotential Bonding" the maximum resistance between any ESD sensitive devices and a common connection point, be less than 1.0×10^9 ohms.

22. Other materials published by the ESDA, including the "Fundamentals of Electrostatic Discharge, Part 3," supplement and explain the ANSI Standard and make clear that an effective ESD Control Program requires equipment, work surfaces, workstations, or anything that may come into contact with ESD-sensitive devices be made of "static dissipative materials."

23. ANSI/ESD ADV1.0, which is expressly incorporated into the ANSI Standard, defines "static dissipative" and "dissipative materials" as having a surface volume resistance of between 1.0×10^4 and 1.0×10^{11} ohms.

24. Xilinx requires its manufacturers to comply with ANSI S20.20. Xilinx's manufacturers further hold themselves out to the public to be ANSI S20.20 certified. Plaintiff is further informed, believes, and thereon alleges, that it is common practice for electronics manufacturers to comply with the ASNI Standard.

25. In addition, the JESD625B standard promulgated by JEDEC (the "JEDEC Standard") specifies "[r]equirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices." The JEDEC Standard incorporates significant portions of the ANSI Standard and the ANSI Standard expressly refers to the JESD625B standard as an "Industry Standard" the ESDA reviewed during its preparation of the ANSI Standard.

26. JESD625B also specifically requires the use of dissipative materials in the handling of ESD-sensitive devices. By way of example and not limitation, the JESD625B standard requires that ESD work surfaces and workstations utilize static dissipative materials having a surface or volume resistance between 1×10^4 ohms and 1×10^{11} ohms.

27. Plaintiff is informed, believes, and thereon alleges, that it is industry-wide practice for electronics manufacturers to comply with the ASNI Standard and/or the JEDEC

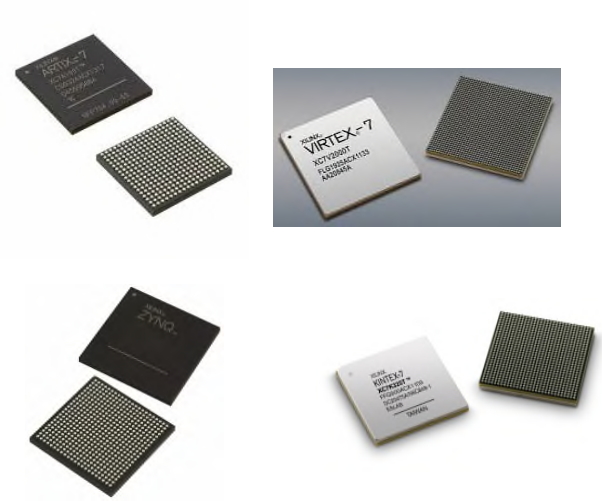
Standard.

28. Xilinx is an active member of JEDEC and is therefore obligated to comply with the JEDEC Standard and to require its contractors and subcontractors to comply with the JEDEC Standard. Plaintiff is further informed, believes, and thereon alleges, that it is common practice for electronics manufacturers to comply with the JEDEC Standard.

ACCUSED PRODUCTS

29. The Accused Products for purposes of the asserted patents include, but are not limited to, Defendant's BGA packaged IC products that are packaged utilizing flip chip or wire bonding techniques as well as PCB products sold by Defendant to which BGA packaged ICs are mounted. The Accused Products therefore include, but are not limited to, BGA packaged ICs that are made, sold or used by the Defendant such as the Spartan, Virtex, Kintex, Artix, and Zynq families of ICs. The Accused Products also include PCBs sold by Defendant that are bonded with the aforementioned BGA packaged ICs, such as Xilinx's "Evaluation Kit," "Connectivity Kit," "Characterization Kit," "DSP Kit," "System on Module (SoM)," "Module," "Base Board," and/or "Development Board" products and all other "kits," "modules," "PCIe," "PXIe," "boards," and/or other PCB products sold by Xilinx that include embedded Spartan, Virtex, Kintex, Artix, and Zynq family ICs.

30. Exemplars of some of the Accused Products are pictured below:



THE ASSERTED PATENTS

31. On June 24, 2008, the USPTO duly and legally issued United States Patent No. 7,389,905 B2 entitled "FLIP CHIP BONDING TOOL TIP" ("the '905 patent"). Steven F. Reiber is the patent's sole named inventor and Plaintiff is owner, by assignment, of the entire right, title and interest in and to the '905 patent and vested with the right to bring this suit for damages and other relief. A true and correct copy of the '905 patent is attached hereto as Exhibit "A."

32. On August 30, 2005, the United States Patent and Trademark Office ("USPTO") duly and legally issued United States Patent No. 6,935,548 B2 entitled "DISSIPATIVE CERAMIC BONDING TOOL TIP" ("the '548 patent"). Steven F. Reiber and Mary Louise Reiber are the patent's sole named inventors and Plaintiff is owner, by assignment, of the entire right, title and interest in and to the '548 patent and vested with the right to bring this suit for damages and other relief. A true and correct copy of the '548 patent is attached hereto as Exhibit "B."

33. On March 12, 2002, the United States Patent and Trademark Office ("USPTO") duly and legally issued United States Patent No. 6,354,479 B1 entitled "DISSIPATIVE CERAMIC BONDING TOOL TIP" ("the '479 patent"). Steven F. Reiber and Mary Louise Reiber are the patent's sole named inventors and Plaintiff is owner, by assignment, of the entire right, title and interest in and to the '479 patent and vested with the right to bring this suit for damages and other relief. A true and correct copy of the '479 patent is attached hereto as Exhibit "C."

COUNT ONE

INFRINGEMENT OF THE '905 PATENT BY DEFENDANT

(All Accused Products Except The Spartan Family Of Products)

34. Plaintiff re-alleges and incorporates by reference each of the allegations set forth in paragraphs 1 through 33 above.

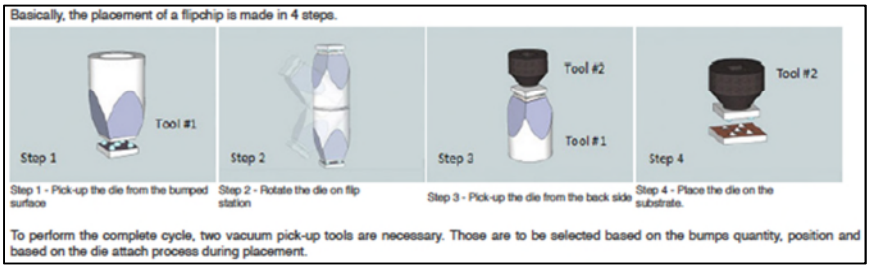
35. The Accused Products, alone or in combination with other products, directly or

alternatively under the doctrine of equivalents infringe each of the limitations of independent claims 53 and 55 of the '905 patent in violation of 35 U.S.C. § 271 (g) when Defendant imports into the United States or offers to sell, sells, or uses within the United States a product which is made by the processes described herein.

36. The Accused Products, include the Xilinx 7 Series FPGAs comprising Artix-7, Kintex-7 and Virtex-7 and ZYNQ-7000 series FPGA, which are packaged using a flip chip bonding process. The Accused Products also include PCBs to which the Defendant's BGA ICs are bonded.

37. The Accused Products have a low threshold for current as disclosed in data sheets supplied by the Defendant. They include BGA-mounted chips for which the Defendant recommends current tolerances of I/O pins at 10mA (*see, e.g.*, p. 3, Table 2 of the ZYNQ programmable SoCs[1] and 7-series FPGAs datasheets). They are therefore extremely susceptible to damage from an ESD event and are commonly referred to as ESD-sensitive devices.

38. Flip chip bonding techniques are commonly used in fabricating BGA packaged ICs and in placing BGA components on Printed Circuit Boards. The process involves the use of bonding tools that come in contact with the Accused Products as shown above.



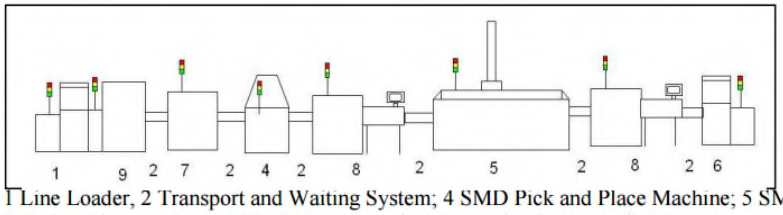
39. Generically speaking, flip chip microelectronic assembly involves the direct electronic connection of facedown electronic components onto substrates, circuit boards, or carriers by means of conductive bumps on an IC's bond pads. In the fabrication or manufacturing process, the Accused Products come in contact with tools and machines that pick them up and place them on surfaces where they are bonded to allow for the interconnection of

[1] https://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

circuits. The risk of an ESD event or discharge exists when the Accused Product(s) come(s) in contact with any tool or surface. ESD events or discharges from this interaction are likely to irreparably damage the Accused Product(s).

40. In bonding an IC to a substrate, the industry-wide practice is to utilize a bonding machine equipped with a flip chip bonding tool.

41. Defendant is a large-scale purveyor of ICs. As a result, manual assembly of the Accused Products would be too time-consuming to meet Defendant's large-scale customer demand. Accordingly, Plaintiff is informed, believes and thereon alleges that Defendant's OEMs utilize bonding machines (like the system pictured above) that are equipped with flip chip bonding tools. These tools utilize a "tip," to bond ESD-sensitive ICs to substrates as described herein and as taught by claims 53 and 55 of the '905 patent.



1 Line Loader, 2 Transport and Waiting System; 4 SMD Pick and Place Machine; 5 SMD Oven; 6 End of Line Loader; 7 AOI; 8 Manual Optical Inspection Systems; 9 Printers

Figure 3 SMD production line (sample)

42. Current industry standards, including ANSI S20.20 and JESD 625B, specify that, during manufacture of products with ESD-sensitive ICs, materials that contact an ESD-sensitive device should be made of dissipative materials to neutralize electrostatic charges and have a resistance value between conductors and insulators of at least between 1×10^4 and 1×10^{11} ohms surface or volume resistance. These resistance ranges are low enough to prevent a discharge of a charge to an ESD-sensitive device such as the Accused Products, but high enough to avoid current flows that may damage the device.

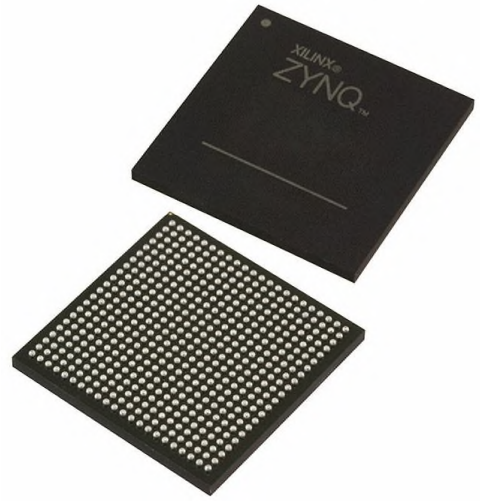
43. Sound manufacturing processes therefore require that dissipative materials must be used in the manufacturing process to ensure controlled electrostatic discharges and avoid abrupt electrostatic discharges that may damage an ESD-sensitive device (such as Xilinx's 7 series FPGAs and ZYNQ SoCs). Defendant specifies and/or directs that the Accused Products be assembled or manufactured in ways that meet or exceed widely accepted industry standards

for ESD-sensitive devices, such as ANSI S20.20 and/or JESD625B, to reduce the risk of damage to the Accused Products.

44. Based on the foregoing, Defendant's OEMs use flip chip bonding machines that are capable of being equipped and are equipped with flip chip bonding tools in the fabrication and manufacture of the Accused Products.

45. Defendant requires its OEMs to equip their bonding machines with tool tips made with dissipative materials having a resistance within the range required by the ANSI and/or JEDEC Standards, which range is low enough to prevent a discharge of a charge to the Accused Products but high enough to avoid current flows that may damage the Accused Products as taught by claim 53 of the '905 Patent.

46. The Accused Products are bonded to substrates using materials that are thermally and electrically conductive as taught by claim 53 of the '905 patent. Shown at right is a typical example of the Defendant's Accused Products (ZYNQ), which uses solder balls. Solder is known to be thermally and electrically conductive. The solder balls are also melted so as to become substantially spherical in shape as taught by claim 53 of the '905 Patent.



47. Further, when the Accused Products are fabricated or used in the manufacture of other products, a flip chip bonding tool tip is used to electrically connect the Accused Products to a substrate by applying pressure to the Accused Product causing the solder balls to form an electrically conductive bump as taught by claim 53 of the '905 Patent.

48. Defendant requires, and its OEMs follow, industry standards in the fabrication and manufacture of the Accused Products and therefore require that tool tips that come in contact with the Accused Products be dissipative in the range of at least 1×10^4 and 1×10^{11} ohms surface or volume resistance (the ANSI and JEDEC standards), which is within the range of $1 \times$

10^2 and 1×10^{12} ohms that is taught by claim 55 of the ’905 Patent.

49. A surface or volume resistance value between 1×10^4 and 1×10^{11} ohms is further “low enough to prevent a discharge of a charge to a device being bonded and high enough to avoid current flow large enough to damage the device being bonded” as taught by claims 53 and 55 of the ’905 Patent.

50. Further, during the process of fabrication or manufacture of the Accused Products, a potential is established between the tool and the Accused Product that involve grounding leads coupled to the Accused Products as taught by claim 55 of the ’905 patent. A potential can occur whenever anything contacts the Accused Product, including during bonding. Triboelectric charging occurs naturally with movement and/or touching and can build with the simple movement of the bonding tool in an automated machine. It also occurs when the Accused Products are placed or removed from packaging material or when they come in contact with a substrate. The charge built up during the fabrication and manufacture process, or potential, is destructive and must be, and is, dissipated smoothly without affecting the Accused Product’s electrical characteristics as taught by claim 55 of the ’905 patent. Defendant accomplishes this by using digital and analog grounding pins on the IC, which are connected to the device’s ground.

51. Defendant has had knowledge of infringement of the ’905 patent since at least the filing of this complaint.

COUNT TWO

INFRINGEMENT OF THE ’548 PATENT BY DEFENDANT

52. Plaintiff re-alleges and incorporates by reference each of the allegations set forth in paragraphs 1 through 51 above.

53. Defendant infringes each of the limitations of independent claim 3 of the ’548 Patent in violation of 35 U.S.C. §271(g) by importing the Accused Products, alone or in combination with other products, directly or alternatively, under the doctrine of equivalents, and offering to sell, selling, or using the Accused Products within the United States.

54. The Accused Products include the Xilinx 7 Series FPGAs comprising Spartan-7, Artix-7, Kintex-7, Virtex-7 and ZYNQ-7000 series FPGA, which are packaged using a flip chip bonding process. The Accused Products also include PCBs to which the Defendant's BGA ICs are bonded.

55. The Accused Products have a low threshold for current as disclosed in data sheets supplied by the Defendant. They include BGA-mounted chips for which the Defendant recommends current tolerances of I/O pins at 10mA (*see, e.g.*, p. 3, Table 2 of the ZYNQ programmable SoCs and 7-series FPGAs datasheets). They are therefore extremely susceptible to damage from an ESD event and are commonly referred to as ESD-sensitive devices.

56. As set forth above, current industry standards that are expressly required by Defendant and followed by its OEMs, including the standards issued by the ESDA and JEDEC, specify that, during manufacture of products with ESD-sensitive ICs, materials that contact an ESD-sensitive device should be made of dissipative materials to neutralize electrostatic charges and have a resistance value between conductors and insulators of between $1 \times 10^4 < 1 \times 10^{11}$ ohms surface or volume resistance. These resistance ranges are low enough to prevent a discharge of a charge to an ESD-sensitive device such as the Accused Products, but high enough to avoid current flows that may damage the device.

57. Sound manufacturing processes therefore require that dissipative materials must be used in the manufacturing process to ensure controlled electrostatic discharges and avoid abrupt electrostatic discharges that may damage an ESD-sensitive device (such as the Xilinx 7 series FPGAs and ZYNQ SoCs). Defendant specifies and/or directs that the Accused Products be assembled or manufactured in ways that meet or exceed widely-accepted industry standards for ESD-sensitive devices, such as ANSI S20.20 and JEDEC 625B, to reduce the risk of damage to the Accused Products.

58. The Defendant specifies electrical current tolerances for each of the Accused Products. For example, the ZYNQ programmable SoCs product line specification provides the maximum allowed current for I/O pins at 10mA making it extremely susceptible to damage from

an ESD event. Plaintiff is informed, believes and alleges that the Defendant, in recognizing the susceptibility of the Accused Products to ESD damage, requires its OEMs to utilize and follow, and its OEMS do utilize and follow, best industry standard practices in the fabricating or manufacturing of the Accused Products, including the ANSI and/or JEDEC Standards.

59. During the process of bonding silicon dies into BGA packages or in bonding BGA packaged ICs to PCBs, the Defendant's contract manufacturer(s) use bonding tools with tips that are electrically dissipative in compliance with the ANSI and JEDEC Standards cited herein above and as taught by claim 3 of the '548 patent.

60. In addition, the ICs are bonded to the BGA packages and/or BGA packages are bonded to PCBs using conductive adhesive such as solder, which is used as packaging interconnects.

61. The tool tips used by Defendant's manufacturers are composed of materials within the resistance ranges cited above, allow for the controlled dissipation of current in a manner that does not cause damage to the Accused Products during bonding, while allowing the current to flow at a high enough rate to avoid a buildup of current to avoid a damaging discharge to the Accused Products during bonding.

62. Defendant has, since at least the filing of this complaint, had knowledge of infringement of the '548 patent.

COUNT THREE

INFRINGEMENT OF THE '479 PATENT BY DEFENDANT

63. Plaintiff re-alleges and incorporates by reference each of the allegations set forth in paragraphs 1 through 62 above.

64. Defendant infringes each of the limitations of independent claim 37, dependent claim 38 and independent claim 50 of the '479 Patent in violation of 35 U.S.C. §271(g) by importing the Accused Products, alone or in combination with other products, directly or alternatively, under the doctrine of equivalents, and offering to sell, selling, or using the Accused Products within the United States.

65. The Accused Products include the Xilinx 7 Series FPGAs comprising Spartan-7, Artix-7, Kintex-7, Virtex-7 and ZYNQ-7000 series FPGA, which are packaged using a flip chip bonding process. The Accused Products also include PCBs to which the Defendant's BGA ICs are bonded.

66. The Accused Products have a low threshold for current as disclosed in data sheets supplied by the Defendant. They include BGA-mounted chips for which the Defendant recommends current tolerances of I/O pins at 10mA (*see, e.g.*, p. 3, Table 2 of the ZYNQ programmable SoCs and 7-series FPGAs datasheets). They are therefore extremely susceptible to damage from an ESD event and are commonly referred to as ESD-sensitive devices.

67. As stated above, current industry standards, including those issued by the ESDA and JEDEC, specify that, during manufacture of products with ESD-sensitive ICs, materials that contact an ESD-sensitive device should be made of dissipative materials to neutralize electrostatic charges and have a resistance value between conductors and insulators of between at least 1×10^4 and 1×10^{11} ohms surface or volume resistance. These resistance ranges are low enough to prevent a discharge of a charge to an ESD-sensitive device such as the Accused Products, but high enough to avoid current flows that may damage the device.

68. Sound manufacturing processes therefore require that dissipative materials must be used in the manufacturing process to ensure controlled electrostatic discharges and avoid abrupt electrostatic discharges that may damage an ESD-sensitive device (such as the Xilinx's 7 series FPGAs and ZYNQ SoCs). Defendant specifies and/or directs that the Accused Products be assembled or manufactured in ways that meet or exceed widely-accepted industry standards for ESD-sensitive devices, such as ANSI S20.20 and JESD 625B, to reduce the risk of damage to the Accused Products.

69. The Defendant specifies electrical current tolerances for each of the Accused Products. For example, the ZYNQ programmable SoCs product line specification provides the maximum allowed current for I/O pins at 10mA making it extremely susceptible to damage from and ESD event. Plaintiff is informed, believes and alleges that the Defendant, in recognizing the

susceptibility of the Accused Products to ESD damage, requires its manufacturers to utilize and follow, and its manufacturers do utilize and follow, best industry standard practices in the fabricating or manufacturing of the Accused Products.

70. During the process of bonding silicon dies into BGA packages or in bonding BGA packaged ICs to PCBs, the Defendant's manufacturer(s) use bonding tools with tips that are electrically dissipative in compliance with the industry standards described herein above. Recognizing their susceptibility to ESD damage, the Defendant requires the use of bonding tools, and does use bonding tools, equipped with tips made of static dissipative materials as required by claims 37, 38 and 50 of the '479 Patent to avoid any abrupt electrostatic discharge.

71. Defendant requires, and its manufacturers follow, current industry standards requirements that tool tips have dissipative qualities in the range of at least 1×10^4 and 1×10^{11} ohms surface or volume resistance. Further Plaintiff is informed and believes that the Defendant's manufacturer(s) use bonding tool tips in the process of fabricating or manufacturing the Accused Products that are within the range taught by claim 38 of the '479 Patent of between 1×10^5 and 1×10^{12} ohms. These resistance ranges are low enough to prevent a discharge of a charge to an ESD-sensitive device such as the Accused Products, but high enough to avoid current flows that may damage the device as taught by claims 37 and 50 of the '479 patent.

72. Further, in the process of making the Accused Products, the bonding tool tips used by Defendant's manufacturer(s) must and do couple with the ICs of Accused Products during the bonding process forming a bond or connection that allows for static electrical charges that arise as a result of bonding to flow between the tool tip and the Accused Product as taught by claim 50 of the '479 patent.

73. Defendant has had knowledge of infringement of the '479 patent since at least the filing of this complaint.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for relief and judgment as follows:

1. That Defendant has infringed the Patents-in-Suit;

2. Compensation for all damages caused by Defendant's infringement of the Patents-in-Suit to be determined at trial;

3. A finding that this case is exceptional and an award of reasonable attorney's fees pursuant to 35 U.S.C. § 285;

4. Granting Plaintiff pre-and post-judgment interest on its damages, together with all costs and expenses; and,

5. Awarding such other relief as this Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury on all claims.

Dated: May 9, 2017 By: /s/ Anton N. Handal

Anton N. Handal (Bar No. 113812)
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the foregoing document has been served on this date to all counsel of record, if any to date, who are deemed to have consented to electronic service via the Court's CM/ECF system per Fed. R. Civ. P. 5 and D.C.COLO.LCivR. 5.1(d). Any other counsel of record will be served by electronic mail, facsimile and/or overnight delivery upon their appearance in this matter.

I declare under penalty of perjury of the laws of the United States that the foregoing is true and correct. Executed this 9th day of May 2017 at San Diego, California.

By: */s/Anton N. Handal*
Anton N. Handal