IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

UPF Innovations, LLC, ***Plaintiff,*** **v.** **MICROSEMI CORPORATION,** ***Defendant.***	**Civil Action No._____** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff UPF Innovations, LLC ("UPF"), by and through its attorneys, brings this action and makes the following allegations of patent infringement relating to U.S. Patent No. RE40,188 ("the '188 patent" or "the patent-in-suit"). Defendant Microsemi Corporation ("Microsemi") infringes the patent-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*, and UPF seeks compensation for this infringement.

PARTIES

1. Plaintiff UPF Innovations, LLC is a Texas Limited Liability Corporation with its principal place of business located at 3800 N. Lamar Blvd., Suite 200, Austin, TX 78756.

2. On information and belief, Defendant Microsemi Corporation is a Delaware corporation with its principal place of business at One Enterprise, Aliso Viejo, CA, USA 92656. Microsemi can be served through its registered agent, The Prentice Hall Corporation, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

3. On information and belief, Defendant Mirosemi has approximately 4,800 employees globally, including offices in in Addison, Austin, Houston, and Plano, Texas.[1]

[1] MICROSEMI WEBPAGE, available at https://www.microsemi.com/locations (accessed June 26, 2017).

4. On information and belief, Microsemi conducts engineering, research and development, sales and administration activities at its locations in the United States, including in Plano, Texas.[2]

5. On information and belief, Microsemi offers infringing products for sale throughout the United States, including in the Eastern District of Texas.

JURISDICTION AND VENUE

6. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

7. Upon information and belief, this Court has personal jurisdiction over Microsemi in this action because Microsemi has committed acts within the Eastern District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over Microsemi would not offend traditional notions of fair play and substantial justice. Defendant Microsemi, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patent-in-suit. Moreover, Microsemi maintains substantial offices in Addison, Austin, Houston, and Plano, Texas[3]; is registered to do business in the State of Texas[4]; and has appointed The Prentice Hall Corporation, 211 E. 7th Street, Suite 620, Austin, TX 78701, as its agent for service of process.

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[2] MICROSEMI 2016 ANNUAL REPORT at page 28, available at https://investor.microsemi.com/download/Microsemi+Annual+Report+2016+FINAL.pdf (accessed June 26, 2017)

[3] *See* note 1, *supra*.

[4] *See* TEXAS COMPTROLLER OF PUBLIC ACCOUNTS WEBPAGE, Texas Taxpayer Number: 19521103713, Texas OS File Number: 0010390906, available at https://mycpa.cpa.state.tx.us/ (last accessed June 27, 2016)

8. Venue is proper in this district under 28 U.S.C. § 1400(b). Defendant Microsemi has a regular and established place of business in the Eastern District of Texas, in Plano, Texas, at 2805 North Dallas Tollway, Plano, TX. Consistent with its physical presence in Plano, Texas, Defendant Microsemi advertises its presence in the Eastern District of Texas on its website.[5] Further, upon information and belief, Microsemi has transacted business in the Eastern District of Texas and has committed acts of direct and indirect infringement in the Eastern District of Texas.

TECHNOLOGY OVERVIEW

9. Integrated circuits have become ubiquitous in today's world and continue to become smaller, more powerful, and more complex. Modern integrated circuits, such as processors, systems on a chip ("SoCs"), digital memory, application-specific integrated circuits ("ASICs"), and field-programmable gate arrays ("FPGAs"), are used in virtually all of today's electronic devices.

10. Integrated circuits are often manufactured in batch processes intended to make all integrated circuit chips identical, thereby lowering manufacturing costs and improving quality. However, it is useful to be able to distinguish each individual integrated circuit from all others, for example, to track its source of manufacture, or to identify a system employing the integrated circuit, which are both useful strategies for avoiding counterfeiting.

11. While it takes incredible ingenuity to design advanced integrated circuits, and the electronic devices that run by them, such circuitry is nevertheless susceptible to counterfeit.

12. In general, a counterfeit electronic part is any unlawful or unauthorized reproduction, substitution, or alteration that has been knowingly mismarked, misidentified, or otherwise misrepresented to be an authentic, unmodified electronic part from the original manufacturer, or a source with the express written authority of the original manufacturer or

[5] *See* note 1, *supra* (Microsemi office located at "2805 North Dallas Tollway, Plano, TX, USA 75093")

current design activity, including an authorized aftermarket manufacturer. Unlawful or unauthorized substitution may include used electronic parts represented as new, or the false identification of grade, serial number, lot number, date code, or performance characteristics.[6]

13. Counterfeit electronic parts cost American companies billions of dollars a year.[7] But economic risk is not the only risk of counterfeit parts; rather, counterfeit parts create significant health and safety risks as well due to their ubiquity in electronic devices of all sorts, including health and safety equipment.

14. As a result of the risks posed by counterfeit electronic parts, the U.S. government has enacted many laws to eliminate the introduction of counterfeit parts into the stream of commerce—especially where government contracts are concerned. For example, in 2012 the U.S. Government enacted laws requiring regulations for contractor responsibilities for detection and avoidance of the use of counterfeit electronic parts.[8]

15. Many technological solutions for preventing and detecting counterfeit parts have been developed, including, for example, integrating RFID tags into electronic parts, creating hardware "fingerprints," "watermarking" electronic parts, and others. Many of these technologies are referred to as "intrinsic security" measures because they are built into the electronic parts.

16. One intrinsic security technique is based on Physical Unclonable Functions (PUFs). PUFs allow an electronic part to be uniquely identified based on the unique properties of its microstructure, which depends on random physical factors introduced during manufacturing. PUFs are extremely useful for electronic devices because they are easy to produce, often

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[6] *See, e.g.*, U.S. Defense Federal Acquisition Regulation 202.101; SAE Int'l AS5553A and AS6081A

[7] *See, e.g.*, The 'Ticking Time Bomb' of Counterfeit Electronic Parts, available at http://www.industryweek.com/procurement/ticking-time-bomb-counterfeit-electronic-parts (last accessed July 3, 2017).

[8] See 48 CFR 252.246-7007 "Contractor Counterfeit Electronic Part Detection and Avoidance System" available at https://www.gpo.gov/fdsys/pkg/CFR-2014-title48-vol3/pdf/CFR-2014-title48-vol3-sec252-246-7007.pdf (last accessed July 3, 2017).

requiring no special manufacturing steps, but very difficult if not impossible to duplicate, even if the exact manufacturing process that produced the PUF is known. PUFs are frequently implemented in electronic parts with high security requirements.

OVERVIEW OF U.S. PATENT NO. RE40,188

17. U.S. Patent Application No. 09/251,692 (‘692 Application) was filed on February 17, 1999 and subsequently issued as U.S. Patent No. 6,161,213 (‘213 Patent), entitled “System and Method for Providing Integrated Circuit with a Unique Identification,” on December 12, 2000.

18. On December 12, 2002, the assignee of the ‘213 Patent filed U.S. Patent Reissue Application 10/318,583 (‘583 Application), entitled “System and Method for Providing Integrated Circuit with a Unique Identification,” based on the ‘213 Patent. The ‘583 Application was subsequently reissued as RE40,188 (‘188 Patent) on March 25, 2008. The ‘188 Patent includes 164 claims total, of which 10 are independent claims.

19. The ‘188 Patent recognizes that while many methods exist for uniquely identifying an electronic part, those existing methods require special steps during the manufacturing process that add cost and time to the manufacturing process. To solve this problem, the ‘188 Patent teaches a novel method for reliably and easily identifying and authenticating individual integrated circuits that does not require any additional manufacturing steps or equipment. Ex. 1 [‘188 Patent] at 2:36-44.

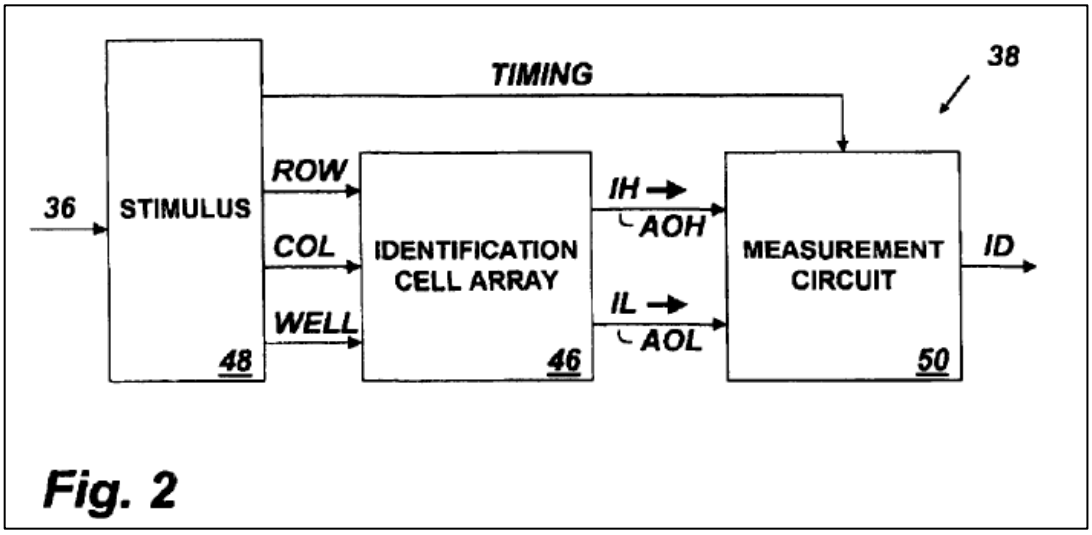
20. In particular, the ‘188 Patent teaches a method of producing integrated circuit identification (ICID) circuits, which produces a unique identification number or record (ID) for each chip in which the ICID is included, even though the ICID circuit is fabricated on all chips using identical masks. Ex. 1 [‘188 Patent] at 2:46-50.

21. Embodiments of ICID circuits include a set of cells that produce an output ID based on measurements of outputs of those cells, and the outputs of those cells are functions of random parametric variations that naturally occur when fabricating the ICID circuit. Ex. 1 [‘188

Patent] at 2:50-54. Embodiments of ICID circuits include arrays of cells and a circuit for selecting each cell of the array, measuring that cell's output, and producing the chip ID based on the pattern of measured outputs of all cells in the array. Ex. 1 ['188 Patent] at 2:57-62. The chip ID is thus a unique "fingerprint" for the chip. Ex. 1 ['188 Patent] at 3:1-4.

22. The '188 Patent teaches that when the number of ICID circuit cells is sufficiently large, then millions of chips can be provided with a unique identifying ID without having to customize each chip using costly and time-consuming additional processing steps during or after chip fabrication. Ex. 1 ['188 Patent] at 2:54-56; 3:13:17.

23. Figure 2 of the '188 Patent depicts a functional block diagram of an embodiment of an ICID device:



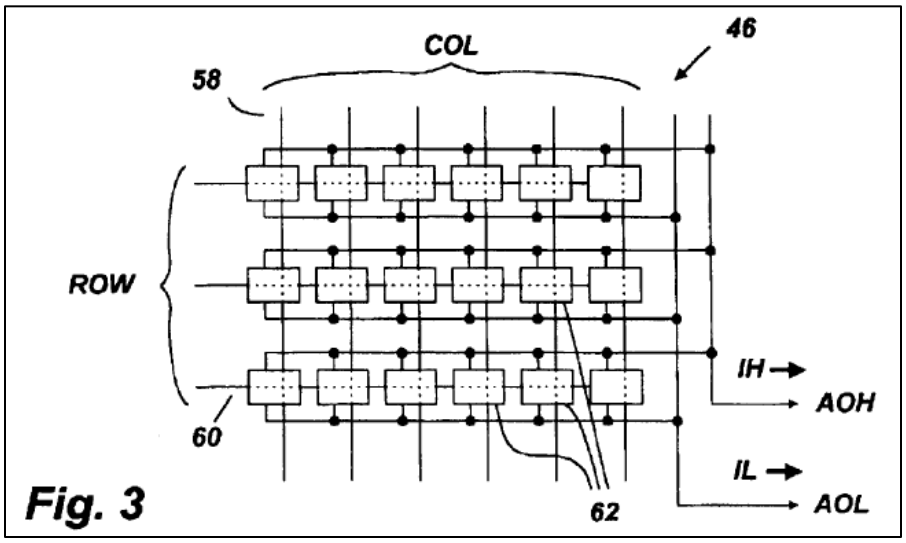
Ex. 1 ['188 Patent] at Fig. 2.

24. Referring to Figure 2, the specification explains: "ICID circuit **38** includes an array **46** of rows and columns of cells. Each cell of array **46**, when selected produces a pair of output currents IH and IL on array output lines AOH and AOL. The IH and IL currents are produced by similar transistors within the selected cell and are nearly equal. But due to differences in the transistors resulting from random parametric variations, the IH and IL currents will not exactly match. The difference between the IH and IL currents will vary from cell to cell. A stimulus circuit **48** responds to the control input **36** by supplying row select data (ROW) and a column select data (COL) to array **46** to individually select and stimulate each of its cells in turn.

As it selects a cell, stimulus circuit **48** sends timing signals (TIMING) to a measurement circuit **50** telling it when to measure a difference between the currents IH and IL of the selected cell." Ex. 1 ['188 Patent] at 5:22-37.

25. The specification further explains that: "[m]easurement circuit **50**, sequenced by TIMING strobes from stimulus circuit **48**, measures the current difference between IH and IL for each cell and … produces a serial output ID having a value that is base[d] on the particular pattern of measured current differences for all cells of array **46**." Ex. 1 ['188 Patent] at 5:51-56.

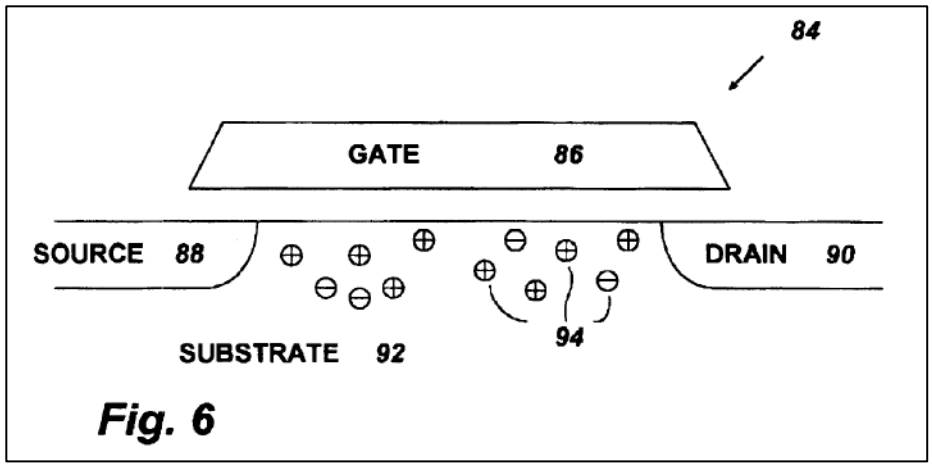
26. Figure 3 of the '188 Patent depicts more detail regarding an embodiment of an identification cell array:



Ex. 1 ['188 Patent] at Fig. 3.

27. Notably, Figure 3 is merely one example of a structure of such an array. As the specification teaches: "the number of cells 62 that should be included in array 46 is largely a function of the number of ICs to be uniquely identified." Ex. 1 ['188 Patent] at 12:13-20.

28. The cells themselves may be formed in some embodiments from transistors, such as shown in basic form with respect to Figure 6:



Ex. 1 [‘188 Patent] at Fig. 6.

29. As further described in the specification: ICID 38 (Figure 2) “may be adapted to provide an output ID that not only uniquely identifies an IC in which it is installed but also includes a ‘type code’ indicating aspects of the IC that is has in common with other ICs sharing the same photomask, such as its type, source of manufacture, etc. Thus, an output ID of ICID 38 would include one field having a value that is unique to the IC in which it is installed and another field having a value that is common to all similar ICs.” Ex. 1 [‘188 Patent] at 5:62-64.

30. Further, the specification explains that the output ID can be stored in a database and used to later identify the specific part. Ex. 1 [‘188 Patent] at 14:55-15:8. Similarly, if a part is tested and found not to be in the database, then it may be determined to be a counterfeit. Ex. 1 [‘188 Patent] at 15:12-13.

31. Additionally, an output ID “may be stored on the chip itself as a sequence of values in an on-chip Random Access Memory (RAM) which may be non-nonvolatile. The RAM may be part of a microprocessor on-board cache, and available to software executed by that microprocessor. This arrangement allows fast access to the ID during use ….” Ex. 1 [‘188 Patent] at 16:5-10.

32. The innovativeness of the solutions taught in the '188 Patent are clear from the industry's myriad references to it and its predecessor patent.[9] By way of example, the '213 Patent (predecessor to '188 Patent) has been cited in patent documents all over the world more than 260 times by the likes of Advanced Micro Devices[10], Analog Devices Inc.[11], Fujitsu[12], Hewlett Packard[13], Hitachi[14], IBM[15], Intel[16], Intrinsic ID[17], MIT[18], National Semiconductor[19], Nokia[20], Panasonic[21], Philips[22], Samsung[23], STMicroelectronics[24], Synaptics[25], Texas Instruments[26], and Verayo[27]. And despite the '188 Patent issuing more than eight years after the '213 Patent, and almost a decade after the original filing date, it continues to be cited in contemporary patents and patent applications.[28]

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[9] *See*, *e.g.*, Finding the Best Patents – Forward Citation Analysis Still Wins, available at http://www.ipwatchdog.com/2016/03/24/finding-best-patents-forward-citation-analysis-still-wins/id=67192/ (last accessed July 23, 2017) ("We've identified five primary factors for consideration in patent ranking (in order of weighting): Forward citations (45%) Age of patent from priority date (19%) Independent claim count (adjusted by number of means claims) (14%) Claim 1 word count (12%) Family size and international filings (10%) **We were surprised to discover that forward citations dominate the analysis. We evaluated millions of patents – and consistently forward citations were the biggest predictor of a higher value patent**.") (emphasis added)

[10] *See*, *e.g.*, US6968303

[11] *See*, *e.g.*, US6480136

[12] *See*, *e.g.*, US6862725 and US7062346

[13] *See*, *e.g.*, US6960753 and US6889305

[14] *See*, *e.g.*, US6941536 and US7665049

[15] *See*, *e.g.*, US8214169 and US8619979

[16] *See*, *e.g.*, US7813507 and US7102358

[17] *See*, *e.g.*, US20030204743

[18] *See*, *e.g.*, US7681103 and US7757083

[19] *See*, *e.g.*, US7602666 and US7482657

[20] *See*, *e.g.*, US7356627

[21] *See*, *e.g.*, US7655483 and US8510608

[22] *See*, *e.g.*, WO/2004/017408 and WO/2004/105125

[23] *See*, *e.g.*, US6600686

[24] *See*, *e.g.*, US8745107 and US7334131

[25] *See*, *e.g.*, US8698594 and US9697411

[26] *See*, *e.g.*, US6952623

[27] *See*, *e.g.*, US8782396 and US8683210

[28] *See*, *e.g.*, US9506983 and US9568540

33. UPF is the owner and assignee of the patent-in-suit as recorded by the USPTO at Reel/Frame: 042956/0213.

COUNT I
INFRINGEMENT OF U.S. PATENT NO. RE40,188
(AGAINST MICROSEMI)

34. UPF restates and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

35. UPF is the owner by assignment of the '188 patent. A true and correct copy of the '188 patent is attached hereto as Exhibit 1.

36. On information and belief, Microsemi makes, uses, sells, offers to sell, and/or imports the Microsemi SmartFusion 2 SoC FPGAs, the Microsemi IGLOO 2 FPGAs, and the Microsemi PolarFire FPGAs (collectively, "the Microsemi Accused Products").

37. On information and belief, to the extent the preamble of claim 21 of the '188 Patent is limiting, the Microsemi Accused Products comprise an apparatus in an integrated circuit (IC) for generating an identification number (ID) identifying the IC. For example, the Microsemi Accused Products contain design security systems to protect against tampering, cloning, overbuilding, reverse engineering, and counterfeiting, as well as providing traceability through the entire lifetime of the system. Among these design security features are physically unclonable functions ("PUFs").

> Variations of individual circuits induced during the manufacturing process can be used to create a physically unclonable function (PUF). The PUF creates a highly secure 'digital fingerprint' of the device using a dedicated SRAM block and a controller. The controller collects underlying device characteristics resulting in the generation of a unique-per-device hardware-based cryptographic key. SmartFusion2 FPGAs employ the Intrinsic-ID® SRAM-PUF along with immutable on-chip embedded non-volatile memory. This and other security features create a root-of-trust for the configuration and secure boot of the SmartFusion2 device. The SmartFusion2 FPGA can extend that trust to securely boot an external processor chip—even if the processor chip has limited or no intrinsic secure boot capability.

Overview of Secure Boot With Microsemi SmartFusion 2 FPGAs, MICROSEMI TECHNICAL DOCUMENTATION (2013), at 10.

38. On information and belief, the Microsemi Accused Products comprise an identification circuit formed within the IC, the identification circuit outputting signals that are a substantial function of random parametric variations in the IC. For example, the Microsemi Accused Products use the initial power-up values of SRAM to output a device-specific fingerprint based upon manufacturing differences such as the thickness of gate dielectrics, the number of atoms diffused into channel regions, and other random process variations.

The initial power-up values of SRAM behave randomly and independently due to manufacturing differences such as:

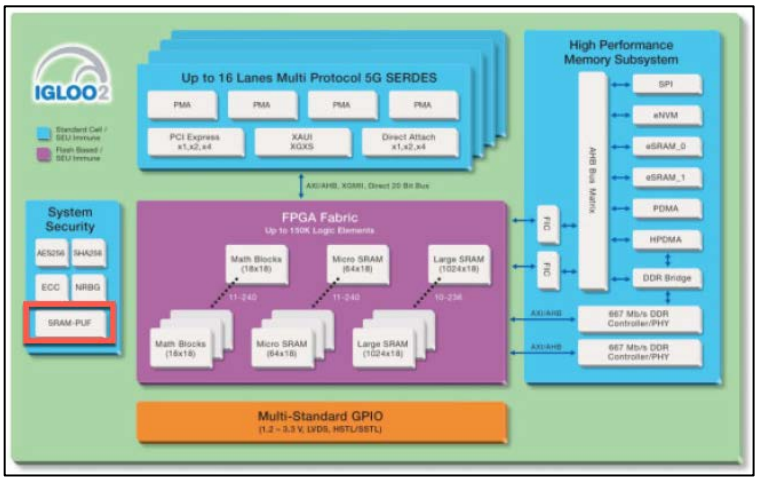
- Thickness of gate dielectric
- Number of atoms diffused into channel region
- Other random process variations

SRAM PUF can be used for the generation of keys in any data security application, because of its randomness and device individual fingerprint. The primary advantage of SRAM PUF for generating keys is that the keys are dynamically reconstructed without storing in memory. Keys are generated only when needed on-the-fly. In addition, SRAM PUF is easy to implement in hardware. The SRAM PUF generates a device-individual fingerprint using the startup behavior of SRAM. It can serve as a root of trust and provides a key that cannot be easily reverse engineered.

SRAM PUF is unique for each chip as the physical characteristics are unique for each chip, difficult to predict, easy to evaluate, and reliable.

Using SRAM PUF System Service in SmartFusion2 - Libero SoC v11.7, MICROSEMI TECHNICAL DOCUMENTATION (March 2016), at 2.

39. On information and belief, the Microsemi Accused Products comprise a measurement circuit, the measurement circuit receiving the signals that are a substantial function of random parametric variations in the IC, wherein the measurement circuit generates the ID, wherein the ID is a substantial function of the random parametric variations.



Overview of Data Security Using Microsemi FPGAs and SoC FPGAs, MICROSEMI TECHNICAL DOCUMENTATION (2013), at 7 (red box added).

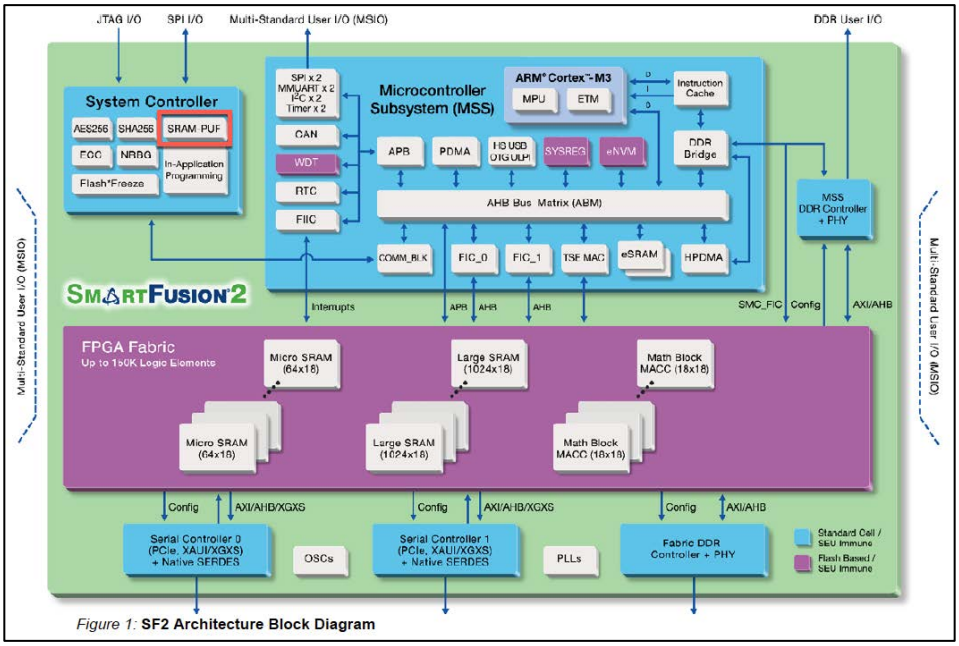


Figure 1: **SF2 Architecture Block Diagram**

Overview of Secure Boot With Microsemi SmartFusion 2 FPGAs, MICROSEMI TECHNICAL DOCUMENTATION (2013), at 4 (red box added).

40. By making, using, testing, offering for sale, selling, and/or importing integrated circuits, including but not limited to the Microsemi Accused Products, Microsemi has injured UPF Innovations and is liable to UPF Innovations for directly infringing one or more claims of the '188 Patent, including at least Claim 1, pursuant to 35 U.S.C. § 271(a).

41. In the alternative, on information and belief, Microsemi has had knowledge of the '188 Patent since at least the date of service of this Complaint or shortly thereafter, and on information and belief, Microsemi knew of the '188 Patent and knew of its infringement, including by way of this lawsuit.

42. On information and belief, Microsemi intended to induce patent infringement by third-party customers and users of the Microsemi Accused Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. Microsemi specifically intended and was aware that the normal and customary use of the accused products would infringe the '188 patent. Microsemi performed the acts that constitute induced infringement, and would induce actual infringement, with the knowledge of the '188 patent and with the knowledge that the induced acts would

constitute infringement. For example, Microsemi provides the Microsemi Accused Products, which are capable of operating in a manner that infringes one or more claims of the ’188 patent, including at least claim 21, and Microsemi further provides documentation and training materials that cause customers of the Microsemi Accused Products to utilize the products and services in a manner that directly infringes one or more claims of the ’188 patent. By providing instruction and training to customers on how to use the Microsemi Accused Products, Microsemi specifically intended to induce infringement of the ’188 patent, including at least claim 21. On information and belief, Microsemi engaged in such inducement to promote the sales of the Microsemi Accused Products and to actively induce its customers to infringe the ’188 patent. Accordingly, Microsemi has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the ’188 patent, knowing that such use constitutes infringement of the ’188 patent.

43. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ‘188 Patent.

44. As a result of Microsemi’s infringement of the ‘188 Patent, UPF has suffered monetary damages, and seeks recovery in an amount adequate to compensate for Microsemi’s infringement, but in no event less than a reasonable royalty for the use made of the invention by Microsemi together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff UPF respectfully requests that this Court enter:

1. A judgment in favor of Plaintiff UPF that Microsemi has infringed the ‘188 Patent, either literally and/or under the doctrine of equivalents;
2. An award of damages resulting from Microsemi’s acts of infringement in accordance with 35 U.S.C. § 284;

3. A judgment and order requiring Microsemi to provide accountings and to pay supplemental damages to UPF, including, without limitation, prejudgment and post-judgment interest; and
4. Any and all other relief to which UPF may show itself to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, UPF requests a trial by jury of any issues so triable by right.

Dated: August 2, 2017

Respectfully submitted,

/s/ Matt Olavi

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