Colby B. Springer (SBN No.: 214868)
cspringer@polsinelli.com
Hannah T. Yang (SBN No.: 311814)
hyang@polsinelli.com
POLSINELLI *LLP*
Three Embarcadero Center
Suite 2400
San Francisco, California 94111
T: 415.248.2100
F: 415.248.2101

Attorneys for Plaintiff
ANZA TECHNOLOGY, INC.

UNITED STATES DISTRICT COURT

EASTERN DISTRICT OF CALIFORNIA

Anza Technology, Inc., a California corporation, Plaintiff, v. Toshiba America Electronic Components, Inc., a California corporation, Defendant.	Case No. **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

Plaintiff Anza Technology, Inc. ("Anza" or "Plaintiff"), by and through its undersigned counsel complains and alleges against Defendant Toshiba America Electronic Components, Inc. ("Toshiba") as follows:

NATURE OF THE ACTION

1. This is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1, *et seq.*, including, without limitation, 35 U.S.C. §§ 271 and 281. Plaintiff Anza seeks a preliminary and permanent injunction and monetary damages for patent infringement.

JURISDICTION AND VENUE

2. This court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a) and pursuant to the patent laws of the United States of

America, 35 U.S.C. § 1, *et seq.*

3. Venue properly lies within the Eastern District of California pursuant to the provisions of 28 U.S.C. §§ 1391(b), (c), and (d) and 1400(b) because Toshiba has a regular and established place of business in this judicial district, and has committed acts of patent infringement in this district, including by making, selling, offering to sell, or importing the infringing products and/or by conducting other business in this judicial district.

4. This Court has personal jurisdiction over Toshiba because Toshiba is incorporated under the laws of the State of California, and transacts continuous and systematic business within the State of California. Toshiba's infringing activities, including, without limitation, the making, using, selling and/or offering for sale, and importing infringing products occur in the State of California and cause harm to Plaintiff in the State of California. In particular, Toshiba's infringing products are sold at local retail stores within the District at, among others, Staples, Best Buy, and Office Depot. Finally, this Court has personal jurisdiction over Toshiba because, on information and belief, Toshiba has made, used, sold, offered for sale, and/or imported its infringing products and placed such infringing products in the stream of interstate commerce with the expectation that such infringing products would be made, used, sold and/or offered for sale within the State of California.

5. Upon information and belief, certain of the products manufactured by or for Toshiba have been and/or are currently designed and/or offered for sale by Toshiba through an in-house sales and marketing team.

PARTIES

6. Plaintiff Anza is a corporation organized and existing under the laws of the State of California with an office and principal place of business at 4121 Citrus Avenue, Suite 4, Rocklin, California 95677. Anza is a designer, manufacturer and seller of products directed to the manufacture and assembly of electronics including the bonding of electrostatic-sensitive devices.

7. Toshiba is a corporation organized and existing under the laws of the State of California with an office at 35 Iron Point Circle, Folsom, California 95630. Toshiba's principal

place of business is 9740 Irvine Boulevard, Suite D700, Irvine, California, 92618. Toshiba is in the business of designing, manufacturing, and selling electronic components.

BACKGROUND

8. Toshiba designs, manufactures, assembles or imports products with Integrated Circuit ("IC") chips. The IC chips are electrostatic discharge ("ESD") sensitive devices. Assembly of Toshiba's products with these ESD-sensitive IC chips requires certain techniques and methods to guard against ESD events that have catastrophic consequences on IC chips. These certain techniques and methods infringe the Asserted Patent, described in further detail below.

9. ESD damage is a well-known phenomenon in the electronics industry and broadly-accepted standards have been developed by industry-recognized standards setting organizations (such as ANSI, JEDEC, the IEC and/or the ESDA) (cumulatively "ESD-Standards") to minimize the risk of damage to ESD sensitive devices during assembly and manufacture. Each of the aforementioned industry standards thus requires the use of manufacturing tools made of dissipative materials having approximately the same resistance values in connection with handling ICs that are particularly sensitive to ESD events. These resistance ranges are low enough to prevent an electrostatic discharge to an ESD-sensitive device such as the Accused Products (described in further detail below), but high enough to avoid current flows that may damage the device.

10. Failing to adhere to such standards could otherwise lead to ESD events during the bonding process that could damage the ICs and render them defective and/or unusable. Today, as little as five volts of an ESD event is enough to permanently change the structures in ESD-sensitive devices, which include, but are not limited to, ICs, Printed Circuit Boards ("PCBs") and other electronic components.

11. Complementary Metal-Oxide Semiconductors ("CMOS") are a type of IC commonly used in microprocessors, microcontrollers, static RAM and other digital logic circuits. CMOS ICs are known to be ESD sensitive and are highly susceptible to damage caused by ESD events.

12. CMOS chips are typically cut from a wafer of silicon into individual pieces, called "dies." The die is picked up by a tool and placed on a substrate or package for placement on a PCB as shown below in Figure 1.

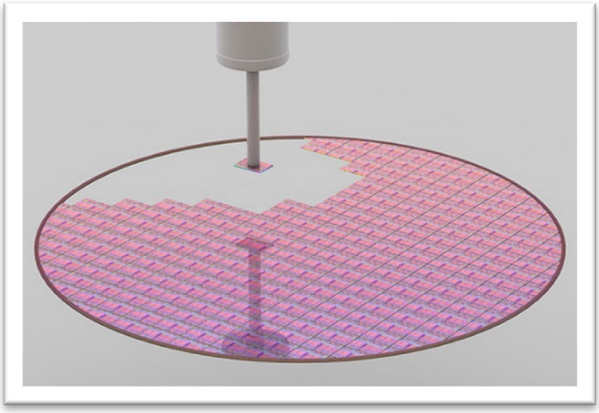

Figure 1. Die picked up by tool.

13. A common method of packaging CMOS ICs for handling and mounting on PCBs is the Ball Grid Array mounting system (or a variation thereof *e.g.*, Fine-Pitch Ball Grid Array, Tape Ball Grid Array, Plastic Ball Grid Array) (cumulatively referred to herein as "BGA"). Figure 2 below depicts an exemplary BGA mounting system. An individual CMOS IC wafer is inserted in a package that uses "solder balls" as conduits of electrical connectivity. ICs with BGA mounting packages are thereafter surface mounted to PCBs via the array of solder balls.

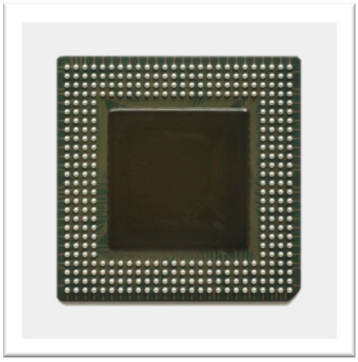

Figure 2. BGA

14. Flip chip bonding techniques are commonly used in fabricating BGA packaged ICs and in placing BGA components on PCBs. Flip chip microelectronic assembly is the direct

electronic connection of facedown electronic components onto substrates, circuit boards, or carriers by means of conductive bumps on the BGA IC package.

15. During the process of bonding a BGA IC to a PCB, the IC comes in contact with tools that place it on the PCB with the solder balls facing down. Heat is then applied causing the solder balls to melt resulting in the bonding of the IC and BGA package to the surface of the PCB. Naturally occurring electrostatic charges (of varying degrees) build up when the mounting tools come in contact with the die and when it is placed in the package. Electrostatic charges can also build up when the die in the BGA package is placed in a tray or on a tape for transport, and also when it is removed from the transport vessel and placed on a PCB for bonding.

16. Essentially, every time an ESD-sensitive device is handled, electrostatic charges to one degree or another are generated. Any type of movement can charge an ESD-sensitive device. Triboelectric charging, for example, commonly occurs in automated assembly lines with the rubbing of conveyor belts, or when ICs and product parts touch carrier trays or tapes. Electrostatic charges are therefore created at several places in an automated production line including but not limited to 1) during the application of conductive material, 2) during pickup and placement of ICs, and 3) during testing of the assembled devices.

17. Since automated production line processes generate electrostatic charges, caution has to be taken to avoid damaging ESD-sensitive components when they are moved, picked up and placed in contact with one another. For these reasons, ESD-sensitive devices that come in contact with automated handling equipment during the manufacture of the Accused Products should be made of electrostatic dissipative material and a resistance to ground where the ESD-sensitive devices are contacted.

18. As a result, Plaintiff is informed, believes and thereon alleges that Toshiba uses specific design, engineering and manufacturing practices in making the Accused Products to minimize the costs resulting from damaging ESD events. Further, Plaintiff alleges that Toshiba specifies and/or directs that the Accused Products be assembled or manufactured in ways that meet or exceed ESD-Standards for reducing the risk of damage to ESD-sensitive devices.

ACCUSED PRODUCTS

19. The Accused Products for purposes of the asserted patent include products that utilize flip chip bonding techniques during manufacturing in order to reduce ESD damage to important components. The Accused Products therefore include, but are not limited to, the following Toshiba products or product groups: ApP Lite; BiCS Flash; NAND Flash Memory; SDHC Memory Card with Wireless LAN; Removable Media; Radio-Frequency Devices; Wireless Communications Equipment ICs; Microcomputers; Logic ICs; and Automotive Devices (collectively, the "Accused Products").

20. Plaintiff is informed, believes and thereon alleges that Toshiba designs, manufactures, assembles or imports products that depend on high density ICs that are manufactured and mounted on printed circuit boards using a flip chip bonding process that require special electrostatic discharge handling in the Accused Products' assembly process. The ICs in the Accused Products are highly sensitive to ESD events as evidenced by the charge load tolerance specifications promulgated by their manufacturers.

THE ASSERTED PATENT

21. On June 24, 2008, the United States Patent and Trademark Office ("USPTO") duly and legally issued United States Patent No. 7,389,905 entitled "FLIP CHIP BONDING TOOL TIP" (the "'905 patent"). Steven F. Reiber is the patent's sole named inventor and Plaintiff is owner, by assignment, of the entire right, title and interest in and to the '905 patent and vested with the right to bring this suit for damages and other relief. A true and correct copy of the '905 patent is attached hereto as **Exhibit A**.

COUNT ONE
INFRINGEMENT OF THE '905 PATENT BY TOSHIBA

22. Plaintiff re-alleges and incorporates by reference each of the allegations set forth in paragraphs 1 through 21 above.

23. Toshiba has, since at least the filing of this complaint, had knowledge of infringement of the '905 patent.

24. The Accused Products utilize a flip chip bonding technique during manufacture

and/or assembly. Flip chip bonding utilizing dissipative materials during handling to reduce ESD damage is used for packaging and mounting integrated devices in the Accused Products.

25. Flip chip bonding in the manner described in claims 53 and 55 of the '905 patent has become the standard for mounting ESD-sensitive devices in order to reduce parasitic resistance, inductance, and capacitance. The methods of claims 53 and 55 of the '905 patent are reflected in a number of manufacturing standards, including, *e.g.,* the ANSI/ESD S20.20 standard. By way of example, the ANSI standard specifies that the current state of the art manufacturing techniques involving ESD-sensitive devices utilize tools with dissipative materials, *i.e.*, materials that ANSI defines as having a resistance value between 1×10^4 and 1×10^{11} ohms surface or volume resistance. Such specification from the standard is within the range set forth in the '905 patent. Plaintiff believes and alleges that other applicable ESD standards require substantially similar resistance values.

26. For example, Toshiba is a member of JEDEC. *See* **Exhibit B**. On information and belief, Toshiba therefore manufactures and assembles the Accused Products, or contracts with others to manufacture and assemble the Accused Products, in compliance with the JEDEC standards, which specify manufacturing techniques involving ESD-sensitive devices utilizing tools with dissipative materials with resistance values of 1×10^5 and 1×10^9 ohms surface or volume resistance. Alternatively, the JEDEC standard provides that "[Electrostatic Discharge Sensitive] Device Distributors and Users may use this standard **or ANSI/ESD S20.20**" (emphasis added). JEDEC STANDARD NO. 625B, *Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices*, p. 1, attached hereto as **Exhibit C**.

27. In addition, Plaintiff is informed, believes, and thereon alleges that Toshiba manufactures and assembles the Accused Products utilizing conductive adhesives per the method described by claim 53 and 55 of the '905 patent. Conductive adhesive, such as solder, is used as packaging interconnects in the Accused Products. The packaging interconnects are formed over the wafer in the form of bumps or balls, spherical in shape, which bumps are electrically and thermally conductive. The packaging interconnects — or solder balls — are heated and pressed against die or substrate pads to form a conductive bump or contact point between the die and the

flex.

28. In addition, Plaintiff is informed and believes and thereon alleges that the Accused Products use chipsets that utilize mounting systems, including but not limited to ball grid array(s) that are susceptible to damage resulting from ESD. Following proper manufacturing techniques, Toshiba uses assembly tools that feature the infringing dissipative and resistive technology taught by the '905 patent.

29. By engaging in the conduct described herein, Toshiba has injured Plaintiff. The Accused Products, alone or in combination with other products, directly, or, alternatively, under the doctrine of equivalents infringe each of the limitations of independent claims 53 and 55 of the '905 patent in violation of 35 U.S.C. § 271.

30. As a result of Toshiba's infringement, Plaintiff has suffered monetary damages and is entitled to a judgment in an amount adequate to compensate for Toshiba's infringement, but in no event less than a reasonable royalty for the use made of the invention by Toshiba, together with interest and costs as fixed by the Court. Plaintiff will otherwise continue to suffer damages in the future unless Toshiba's infringing activities are enjoined by the Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for relief and judgment as follows:

A. That Toshiba has infringed the Patent-in-Suit;

B. Compensation for all damages caused by Toshiba's infringement of the Patent-in-Suit to be determined at trial;

C. A finding that this case is exceptional and an award of reasonable attorneys fees pursuant to 35 U.S.C. § 285;

D. Granting Plaintiff pre-and post-judgment interest on its damages, together with all costs and expenses; and,

E. Awarding such other relief as this Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury on all claims.

Dated: August 14, 2017

POLSINELLI LLP

/S/ Hannah T. Yang

By:

Colby B. Springer (SBN 214868)
cspringer@polsinelli.com
Hannah T. Yang (SBN 311814)
hyang@polsinelli.com
Three Embarcadero Center
Suite 2400
San Francisco, CA 94111

Attorneys for Plaintiff
ANZA TECHNOLOGY, INC.