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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

POLARIS INNOVATIONS LTD., an Ireland limited company, Plaintiff, v. INTEGRATED SILICON SOLUTION, INC., a Delaware corporation, Defendant.	No. **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

Polaris Innovations Limited ("Polaris") files this Complaint against Integrated Silicon Solution, Inc. ("ISSI") for ISSI's infringement of United States Patents 6,653,882 B2 and 6,728,143 B2. Polaris alleges as follows:

PARTIES

1. Polaris is a limited company organized and existing under the laws of the Republic of Ireland, with its principal place of business at 29 Earlsfort Terrace, Dublin 2, Republic of Ireland.

2. ISSI is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 1623 Buckeye Dr., Milpitas, CA 95035.

JURISDICTION

3. Polaris brings this action under the patent laws of the United States, 35 U.S.C. § 1 *et. seq*. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331, 1332(a)(2), and 1338(a).

VENUE

4. ISSI has sold, offered to sell, and used in this District products that practice or embody one or more claims of each of the patents in suit, as discussed more fully herein. ISSI's website describes its headquarters in this District as one of the "sales offices" from which it sells computer memory products, including DDR3 synchronous dynamic random access memory ("SDRAM"), which infringes the patents in suit. ISSI's headquarters location in Milpitas, California is a regular and established place of business in this District. Venue is proper in this District under 28 U.S.C. § 1400(b).

INTRADSTRICT ASSIGNMENT

5. This is an Intellectual Property Action pursuant to Local Rule 3-2(c).

THE PATENTS IN SUIT

6. On November 25, 2003, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,653,882 B2 ("'882 Patent"), which is entitled "Output Drivers for IC," and identifies Arindam Raychaudhuri as the sole inventor. A true and correct copy of the '882 Patent is attached hereto as Exhibit A. The '882 Patent has been assigned to

Plaintiff Polaris. Polaris holds all right, title, and interest in the '882 Patent, including the right to collect and receive damages for past, present and future infringement of the '882 Patent.

7. On April 27, 2004 the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,728,143 B2 ("the '143 Patent"), which is entitled "Integrated Memory," and identifies Robert Feurle as the sole inventor. A true and correct copy of the '143 Patent is attached hereto as Exhibit B. The'143 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '143 Patent, including the right to collect and receive damages for past, present and future infringement of the '143 Patent.

8. The '882 Patent discloses inventions related to integrated circuit devices including, for example, SDRAM devices used in personal computer systems, among other products. The inventions of the '882 Patent generally are directed to a novel output driver circuit that improves data transfer speeds from an integrated circuit to other circuits in a computer system. The '143 Patent discloses inventions related to integrated memory devices such as SDRAM that can be used in personal computer systems and other products. The inventions of the '143 Patent generally are directed to improving memory access times, and thus the operating speed of a memory device, by employing a novel control circuit for performing memory accesses.

9. The usefulness and value of the patents in suit has been acknowledged by various companies engaged in the design, manufacture, and sale of SDRAM devices. Polaris has widely licensed the patents in suit to numerous SDRAM manufacturers, among others, some of which compete with ISSI for sales of SDRAM devices.

10. Polaris has offered to license the patents in suit to ISSI. Polaris has engaged in numerous discussions with ISSI, through correspondence and in person and telephonic meetings spanning several months, but ISSI has not agreed to license the patents in suit despite several good-faith offers from Polaris. Polaris has therefore been compelled to file this suit to protect its rights.

FIRST CLAIM FOR RELIEF

Infringement of U.S. Patent No. 6,653,882

11. Polaris realleges and incorporates by reference the allegations of paragraphs 1-10,

inclusive, as if set forth in full herein.

12. ISSI has infringed, and continues to infringe, at least claims 1 and 4 of the '882 Patent. ISSI uses, sells, or offers to sell in the United States, products, such as DDR3 SDRAM, including IS43/46TR16256, IS43/46TR85120 512Mx8, 256Mx16 4Gb DDR3 SDRAM ("ISSI DDR3 SDRAM"), that meet each and every limitation of claim 1.

13. Claim 1 of the '882 Patent is directed to an output driver for an integrated circuit. The output driver comprises:

a. a driver circuit for driving an external circuit, the driver circuit having:

i. a data input connected to the integrated circuit;

ii. a data output connected to a transmission line leading to the external circuit;

iii. and an impedance adjusting means for adjusting the output impedance of the driver circuit according to impedance adjusting data;

b. a dummy circuit comprising a dummy driver circuit and a dummy transmission line, the dummy driver circuit and the dummy transmission line being electrical replicas of the driver circuit and the transmission line, respectively;

c. and an impedance control circuit for controlling the output impedance of the driver circuit, the impedance control circuit being connected to the dummy circuit and the impedance adjusting means,

i. wherein the impedance control circuit is configured to control the impedance of the driver circuit by determining the impedance adjusting data necessary for matching the output impedance of the dummy driver circuit to the impedance of the dummy transmission line and outputting the determined impedance adjusting data to the impedance adjusting means of the driver circuit, wherein the dummy driver circuit is a scaled down replica of the driver circuit.

14. The ISSI DDR3 SDRAM meets each and every limitation of claim 1. For example, the ISSI DDR3 SDRAM is an integrated circuit that contains an output driver for

driving an external circuit. The output driver of the ISSI DDR3 SDRAM includes a driver circuit having a data input connected to the integrated circuit and a data output connected to a transmission line leading to the external circuit. For example, the ISSI DDR3 SDRAM contains a DQ (DQL, DQU) pinout of the bi-directional data bus. *See*, *e.g.*http://www.issi.com/WW/pdf/43-46TR16256A-85120AL.pdf ("ISSI Datasheet") at 4, 42.

15. The ISSI DDR3 SDRAM is capable of adjusting the output impedance of the driver circuit, and does so through an impedance adjusting means for adjusting the output impedance of the driver circuit according to impedance adjusting data. For example, the ISSI Datasheet describes ZQ Calibration, a way of adjusting the output impedance of the driver circuit. *See*, *e.g.*, ISSI Datasheet at 6, 13, 14, 42. The ISSI DDR3 SDRAM also contains a dummy circuit comprising a dummy driver circuit and a dummy transmission line, the dummy driver circuit and the dummy transmission line being electrical replicas of the driver circuit and the transmission line, respectively. The dummy circuit is indicated in the ISSI Datasheet as, for example, the ZQ pin and the RZQ reference resistor. *See*, *e.g.*, ISSI Datasheet at 1, 5.

16. The ISSI DDR3 SDRAM also contains an impedance control circuit for controlling the output impedance of the driver circuit, the impedance control circuit being connected to the dummy circuit and the impedance adjusting means. *See*, *e.g.*, ISSI Datasheet at 13:

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

17. The ISSI DDR3 SDRAM's use of ZQ Calibration indicates that the impedance control circuit of the ISSI DDR3 SDRAM is configured to control the impedance of the driver circuit by determining the impedance adjusting data necessary for matching the output impedance of the dummy driver circuit to the impedance of the dummy transmission line and outputting the determined impedance adjusting data to the impedance adjusting means of the driver circuit. The dummy driver circuit is a scaled down replica of the driver circuit, as shown by the RZQ/6 and RZQ/7 values in the table appearing on page 13 of the ISSI Datasheet.

18. Claim 4 of the ’882 patent depends on claim 1, and claims “The output driver according to claim 1, wherein the driver circuit is a push-pull on-chip current driver.”

19. The driver circuit of the ISSI DDR3 SDRAM is a push-pull on-chip current driver, as seen in Fig. 5.7 of the ISSI Datasheet:

5.7 34Ohm Output Driver DC Electrical Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance RON is defined by the value ofthe external reference resistor RZQ as follows:

RON34 = RZQ / 7 (nominal 34.4ohms +/-10% with nominal RZQ=240ohms)

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

RONPu = [VDDQ-Vout] / | Iout | ---------- under the condition that RONPd is turned off (1)

RONPd = Vout / | Iout | ----------under the condition that RONPu is turned off (2)

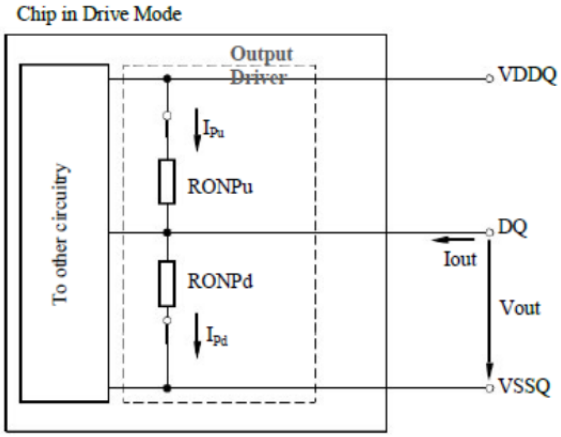

Figure 5.7 Output Driver : Definition of Voltages and Currents

20. Upon information and belief, other ISSI products similarly infringe one or more claims of the ’882 Patent. The specific part numbers of all ISSI products that practice one or more claims of the ’882 Patent are not presently known to Polaris. Polaris accuses of infringement all ISSI products that contain features and functions similar to those described above that practice one or more claims of the ’882 Patent.

21. ISSI has had notice of the ’882 Patent and of its infringement of the ’882 Patent for more than one year. Before initiating litigation, Polaris made substantial efforts to license ISSI’s use of the inventions claimed in the ’882 Patent, expecting that ISSI would engage in good faith licensing discussions. ISSI has refused to license the’882 Patent, and it continues to infringe one or more claims of the ’882 Patent despite being aware of its infringement of the ’882 Patent on the basis of claim charts provided by Polaris. ISSI’s infringement of the ’882 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and

continues to cause substantial damage to Polaris.

SECOND CLAIM FOR RELIEF

Infringement of U.S. Patent No. 6,728,143

22. Polaris realleges and incorporates by reference the allegations of paragraphs 1-10, inclusive, as if set forth in full herein.

23. ISSI has infringed, and continues to infringe, at least claims 1 and 2 of the '143 patent. ISSI uses, sells, or offers to sell in the United States, products, such as DDR3 SDRAM, including IS43/46TR16256, IS43/46TR85120 512Mx8, 256Mx16 4Gb DDR3 SDRAM, that meet each and every limitation of claim 1.

24. Claim 1 of the '143 Patent is directed to an integrated memory. The integrated memory comprises:

a. a memory cell array having memory cells;

b. a control circuit for controlling a memory access selected from the group consisting of a read memory access for reading out a data signal from one of said memory cells and a write memory access for writing a data signal into one of said memory cells;

c. for performing the memory access, said control circuit designed for receiving an access command selected from the group consisting of an activation command, a read command, and a write command;

d. for performing the memory access, said control circuit designed for receiving a configuration value in a combined manner with the access command; and

e. the configuration value being selected from the group consisting of a CAS latency value and a value for specifying a burst access.

25. ISSI DDR3 SDRAM contains a memory cell array having memory cells. For example, the datasheet for the ISSI DDR3 SDRAM describes "8 internal banks for concurrent operation." *See e.g.,* ISSI Datasheet at 1. The ISSI DDR3 SDRAM contains a control circuit for controlling read and write memory accesses. For example, the control circuit uses a command

truth table as described on page 20 of the ISSI Datasheet. The control circuit of the ISSI DDR3 SDRAM is designed to receive access commands in the form of activation commands, read commands (e.g., RDS4, RDS8), and write commands (e.g., WRS4, WRS8). *See* ISSI Datasheet, p.20. The control circuit is further designed to receive a configuration value in a combined manner with the access command, *e.g.*, A12/BC# values in the command truth table. *See* ISSI Datasheet, p.20. The configuration value received by the ISSI DDR3 SDRAM is, for example, a value for specifying a burst access. *See*, *e.g.*, ISSI Datasheet at 4:

A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

26. Claim 2 of the ’143 Patent is dependent upon Claim 1, and claims “The integrated memory according to claim 1, wherein: said control circuit is designed to receive a multi-bit signal that includes the access command and the configuration value.”

27. The control circuit of the ISSI DDR3 SDRAM is designed to receive a multi-bit signal that includes the access command and the configuration value, including bits for CS#, RAS#, CAS#, WE#, BA0-BA2, A11 A13 A14 A15, A12/BC#, A10/AP, and A0-A9. *See* ISSI Datasheet, p.20.

28. Upon information and belief, other ISSI products similarly infringe one or more claims of the ’143 Patent. The specific part numbers of all ISSI products that practice one or more claims of the ’143 Patent are not presently known to Polaris. Polaris accuses of infringement all ISSI products that contain features and functions similar to those described above that practice one or more claims of the ’143 Patent.

29. ISSI has had notice of the ’143 Patent and of its infringement of the ’143 Patent for more than one year. Before initiating litigation, Polaris made substantial efforts to license ISSI’s use of the inventions claimed in the ’143 Patent, expecting that ISSI would engage in good faith licensing discussions. ISSI has refused to license the’143 Patent, and it continues to infringe one or more claims of the ’143 Patent despite being aware of its infringement of the ’143 Patent on the basis of claim charts provided by Polaris. ISSI’s infringement of the ’143 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and

continues to cause substantial damage to Polaris.

WHEREFORE, Polaris prays that judgment be entered in its favor and against ISSI as follows:

a. For damages in an amount according to proof, but no less than a reasonable royalty for infringement of the patents in suit;

b. For enhanced damages pursuant to 35 U.S.C. § 284;

c. For prejudgment and post-judgment interest as provided by law;

d. For costs of suit and reasonable attorneys' fees incurred herein; and

e. For such other relief as the Court deems proper.

Dated: October 11, 2017

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DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Polaris demands a trial by jury on all issues so triable.

Dated: October 11, 2017

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