IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

COMPLEX MEMORY, LLC, Plaintiff -against- TEXAS INSTRUMENTS, INC. and SVTRONICS, INC., Defendants	Civil Action No.: 2:16-cv-699 **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Complex Memory, LLC ("Complex Memory"), by way of this Complaint against Defendants Texas Instruments, Inc. ("TI") and SVTronics, Inc. ("SVTronics") (TI and SVTronics are collectively referred to as the "Defendants" herein), alleges as follows:

PARTIES

1. Plaintiff Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 7116 Nicki Court, Dallas, Texas 75252.

2. On information and belief, Defendant TI is a Delaware corporation with a principal place of business at 12500 TI Boulevard, Dallas, TX 75243, and a manufacturing location at 6412 US-75, Sherman, TX 75090.

3. On information and belief, Defendant SVTronics is a Texas corporation with a principal place of business at 3465 Technology Drive, Plano, TX 75074.

JURISDICTION AND VENUE

4. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq.*, for infringement by TI and SVTronics of claims of U.S. Patent Nos. 5,890,195; 5,963,481; 6,658,576; 6,968,469; and 7,330,330 ("the Patents-in-Suit").

5. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. TI is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, (i) TI is headquartered in the State of Texas, (ii) TI maintains several office and manufacturing locations in the State of Texas; (iii) TI is registered to transact business in the State of Texas; and (iv) TI has committed and continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, and/or selling accused products and services in Texas.

7. Venue is proper as to TI in this district because, *inter alia*, on information and belief, TI maintains a regular and established place of business in this judicial district, and TI has committed and continues to commit acts of patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district.

8. SVTronics is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, (i) SVTronics is headquartered in the State of Texas, (ii) SVTronics maintains several office and manufacturing locations in the State of Texas; (iii) SVTronics is registered to transact business in the State of Texas; and (iv) SVTronics has committed and continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, and/or selling accused products and services in Texas.

9. Venue is proper as to SVTronics in this district because, *inter alia*, on information and belief, SVTronics is headquartered in, and maintains a regular and established place of business, in this judicial district, and SVTronics has committed and continues to commit acts of patent

infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district.

SINGLE ACTION

10. This suit is commenced against TI and SVTronics pursuant to 35 U.S.C. § 299 in a single action because, *inter alia*, on information and belief, (i) the Defendants incorporate TI OMAP processors into the accused products; and (ii) Defendant SVTronics integrates and sells products based on processor designs by Defendant TI. Accordingly, the claims of this Complaint arise out of the same transaction, occurrence, or series of transactions or occurrences relating to the making, using, importing into the United States, offering for sale, or selling of the same accused product or process, and questions of fact common to all Defendants will arise in the action pursuant to 35 U.S.C. § 299.

BACKGROUND

11. On March 30, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,890,195 ("the '195 Patent"), entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM".

12. G.R. Mohan Rao invented the technology claimed in the '195 Patent.

13. On October 5, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,963,481 ("the '481 Patent"), entitled "Embedded Enhanced DRAM, And Associated Method."

14. Michael Alwais and Michael Peters invented the technology claimed in the '481 Patent.

15. On December 2, 2003, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,658,576 ("the '576 Patent"), entitled "Energy-Conserving

Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-Alive Processor With Keep-Alive Operating Instruction."

16. Howard Hong-Dough Lee invented the technology claimed in the '576 Patent.

17. On November 22, 2005, the United States Patent and Trademark Office duly and lawfully issued U.S . Patent No. 6,968,469 ("the '469 Patent"), entitled "System and Method For Preserving Internal Processor Context When The Processor Is Powered Down And Restoring The Internal Processor Context When Processor Is Restored."

18. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '469 Patent.

19. On June 1, 2010, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,730,330 ("the '330 Patent"), entitled "System and Method For Saving And Restoring A Processor State Without Executing Any Instructions From A First Instruction Set."

20. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '330 Patent.

21. Complex Memory is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

COUNT I: INFRINGEMENT OF THE '195 PATENT BY TI

22. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

23. Upon information and belief, TI has infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the products identified in Attachment A

("Accused TI Products").

24. For example, on information and belief, TI has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. For example, the Accused TI Products include Texas Instruments Inc.'s (TI's) AM437x platform. On information and belief, the TI AM437x platform includes an ARM Cortex-A9 Core, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.*, Ex. 1, AM437x Datasheet. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. In performing the method of claim 6, a processing core received an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller) or an address channel of a bus. The Accused TI Products compared the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." *Id.*, Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller. When a match between the received address and a matching address stored in a one of the latches occurred, the Accused TI Products performed the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." *Id.* When a match between the received address and an address stored in one of the latches did not occur, the Accused TI Products performed the substeps of exchanging data between a location in the memory array

addressed by the received address and a selected one of the registers. "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." Ex. 4, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. When the match did not occur, the Accused TI Products further stored the received address in one of the latches corresponding to the selected register. For example, the Accused TI Products stored the received address, such as the tag, corresponding to the register being accessed, in the cache memory system registers, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way registers. *See* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. The Accused TI Products further modified the received address to generate a modified address. For example, the hardware in the Accused TI Products prefetches, for example, data stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 7.6.2 Data prefetching. *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher ("[P]refetch address = current address + (stride x programmed distance."). On information and belief, the Accused TI Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused TI Products further exchanged data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." *See* Ex. 4 ARM Cortex-A Series Programmer's Guide

Version 4.0, Chapter 8 Caches. The Accused TI Products then stored the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stored the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way registers.

25. Upon information and belief, TI has committed the foregoing infringing activities without a license.

COUNT II: INFRINGEMENT OF THE '576 PATENT BY TI

26. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

27. Upon information and belief, TI has infringed, and continues to infringe, the '576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused TI Products identified in Attachment A.

28. For example, on information and belief, TI has infringed at least claim 25 of the '576 Patent by performing steps of an energy-conserving operating system. For example, the Accused TI Products include TI's AM437x platform. On information and belief, the TI AM437x platform, includes an ARM Cortex-A9 Core, and performs the steps of claim 25 of the '576 Patent. *See, e.g.*, Ex. 1, AM437x Datasheet. "Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they

no longer perform computation. This means they consume very little power." Ex. 7, ARM Cortex-A Series Version: 4.0 Programmer's Guide, Chapter 20 Power Management. The Accused TI Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, the Accused TI Products activate a set of interrupt-handling instructions for the generic interrupt controller in connection with handling an interrupt in a standby mode, caused by, among others, the issuance of the WFI (wait for interrupt) instruction executed by a core. Ex. 8, ARM Generic Interrupt Controller Architecture version 2.0, Architecture Specification, § 3.7 Pseudocode details of interrupt handling and prioritization. If detecting a power-up signal, the Accused TI Products power up to provide a main operation that utilizes main microprocessor circuitry and a set of main operating instructions. For example, when the main microprocessor circuitry, such as a core, is in the WFI low power state, an interrupt is detected by the generic interrupt controller, followed by powering up, such as enabling various clocks, to provide the main operation that utilizes that core and a set of main operating instructions, such as the instructions of the executed code following the WFI instruction. "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: • An IRQ interrupt, even if the CPSR I-bit is set. • An FIQ interrupt, even if the CPSR F-bit is set. • An asynchronous abort. • A Debug Entry request, even if JTAG Debug is disabled. In the event of the core being woken by an interrupt when the relevant CPSR interrupt flag is disabled, the core will implement the next instruction after WFI." Ex. 9, ARM Cortex-A Series Version: 4.0 Programmer's Guide, Chapter 20.4 Power Management Assembly language power instructions. The Accused TI Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, in the

regular operating state, a WFI instruction detected by a core is a power-down signal. "Entry into WFI Standby mode is performed by executing the Wait For Interrupt instruction." Ex. 10 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 2.4.2 Cortex-A9 processor power control. If the WFI command is detected, the operating system places the system in the low-power WFI mode. "WFI and WFE Standby modes disable most of the clocks in a processor, while keeping its logic powered up. This reduces the power drawn to the static leakage current, leaving a tiny clock power overhead requirement to enable the device to wake up." *Id.* In the Accused TI Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with said main operating instructions. *Id.*

29. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

COUNT III: INFRINGEMENT OF THE '481 PATENT BY TI

30. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

31. On information and belief, TI has infringed, and continues to infringe the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating DDRxL and/or LPDDRx memories, including the Accused TI Products identified in Attachment A.

32. For example, on information and belief, TI infringes at least claim 16 of the '481 Patent by performing a method of accessing data. On information and belief, the Accused TI Products, such as the AM572x Industrial Development Kit, include DDRxL memory, such as DDR3L. *See* Ex. 11, AM572x Industrial Development Kit (IDK) Evaluation Module (EVM) Hardware

User's Guide ("The part number for the DDR3L SDRAM memory used is MT41K256M16HA-125…"). DDR3L memory included in the Accused TI Products is a memory system comprising multiple banks with multiple rows. "4Gb: x4, x8, x16 DDR3L SDRAM Description," Ex. 12 at p. 13-14 ("Row addressing is denoted as A[*n*:0] . . . DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM."). The Accused TI Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id.* at p. 12 ("The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access."). In TI's DDR3L memory, the memory locations of the first memory row are disposed upon a substrate. *See* Ex. 11 ("The package used is the 96-ball TFBGA package."). The Accused TI Products access the data stored at the memory locations identified in the first access request. Ex. 12. While the data stored at the memory locations identified by the first access request is being accessed, the Accused TI Products generate a second access request for accessing data stored at memory locations of a second memory row. For example, in a burst read operation, while data from the previous access request is being accessed, the subsequent requests access data stored in different rows of another bank. *See id.* at 12 ("As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time."). In the Accused TI Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. *See, e.g.*, Exs. 11-12. The Accused TI Products also access the data stored at the memory locations identified in the second access request. *Id.*

33. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

COUNT IV: INFRINGEMENT OF THE '469 PATENT BY TI

34. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

35. On information and belief, TI has infringed, and continues to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused TI Products identified in Attachment A.

36. For example, on information and belief, TI infringes at least claim 14 of the '469 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the Accused TI Products, which are computer systems. The Accused TI Products include, for example, AM437x devices. On information and belief, AM437x devices include a processor, such as the microprocessor unit (MPU) subsystem. *See* Ex. 13 AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 3.1 Introduction at 151. The Accused TI Products include a first memory, such as one or more L1 caches, accessible by said processor (the MPU subsystem). *Id*. On information and belief, the Accused TI Products also include a second memory, on-chip memory RAM (OCM-RAM) accessible only to said processor. *Id*. OCM-RAM is internal to said processor, the MPU subsystem. *Id*. On information and belief, in the Accused TI Products, power to said second memory is controlled separately from power to said processor and to said first memory, wherein power is maintained to said second memory (OCM-RAM) when power is removed from said processor (the MPU subsystem). For example, in the DeepSleep power mode, the MPU power domain, PD_MPU is OFF (except MPU OCM RAM

retained). *See* Ex. 14, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.4.3 Power Modes at 256. On information and belief, in the Accused TI Products, the second memory is for maintaining internal context of said processor when power is removed from said processor. In the example of the DeepSleep power mode, "In addition, power to OCMC RAM is maintained to preserve information internally during DeepSleep." *Id.*, § 6.4.3.3 DeepSleep at 257. On information and belief, the Accused TI Products also include a third memory external to said processor and accessible only to said processor. For example, the Accused TI Products include various L3 memories, some of which are external to the MPU subsystem but accessible only by the MPU subsystem. *See* Ex. 13, § 3.1 Introduction at 151; See, e.g., Ex. 15, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 2.1.1 at 140, fn. 1 ("The first 1MB of address space 0x0-0xFFFFF is inaccessible externally.") On further information and belief, certain memories containing bootcode and other sensitive and/or secure information, including High Security and/or Trustzone based memories, are also external to the MPU but accessible only by the MPU. On information and belief, in the Accused TI Products, the power to the third memory is controlled separately from power to said processor and to said first and second memories. For example, L3 memory belongs to the Peripheral power domain, PD_PER, which is separate from the MPU power domain, PD_MPU to which the MPU subsystem, the L1 cache, and the OCM-RAM belong. *See* Ex. 16, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.11 Device Modules and Power Management Attributes List at 298. In another example, the Accused TI Products include a portion of L3 memory, the access to which is limited to high-security-enabled devices such as an A9 MPCore processor. On information and belief, in the Accused TI Products, the power to the third memory, L3 memory and the high-security access portions within it, is controlled separately from power to said processor and to

said first and second memories. *Id.*

37. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

COUNT V: INFRINGEMENT OF THE '330 PATENT BY TI

38. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

39. On information and belief, TI has infringed, and continues to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused TI Products identified in Attachment A.

40. For example, on information and belief, TI infringes at least claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused TI Products include a central processing unit, such as a TI OMAP 5 processor. *See* Ex. 17, OMAP 5432 EVM, Figure 1, OMAP5432 EVM Architectural Block Diagram. On information and belief, the OMAP 5432 CPU includes an ARM Cortex-A15 MPCore. *See* Ex. 18, OMAP5432 EVM, Chapter 2.3 OMAP5432 ES2.0 Processor. On information and belief, CPUs in the Accused TI Products execute the ARM 32-bit instruction set, Thumb 16-bit instruction set, and the Thumb 32-bit instruction set. *See* Ex. 19, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 4.2 The ARM instruction sets. On information and belief, the Accused TI Products include one or more registers holding a state, such as the CPSR, R13, and R14 registers. *See* Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers. On

information and belief, in the Accused TI Products, the CPU, is adapted, upon executing a first instruction from said first instruction set (such as an instruction from an application in an A32, T16, or T32 instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save said state in a memory without executing any additional instructions from said first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs) (*see, e.g.,* Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("Before entering Dormant mode, the architectural state of the Cortex-A15 processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")), and (ii) to initiate an action that may cause the state of said registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which renders the above registers undefined). *See, e.g.,* Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers at p. 3-8 ("The reset values of R0-R14 are unpredictable"). On information and belief, in the Accused TI Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from said first instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example, by executing instructions from one of the other two instruction sets; such that, if the first instruction set is A32, instructions from T32 or A64 are executed upon exiting the dormant mode). *See, e.g.,* Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("To exit from Dormant mode to Run mode, the SoC must perform a full power-on reset sequence. The SoC must assert the reset signals until power is restored. After power is restored,

the Cortex-A15 processor exits the power-on reset sequence, and the architectural state must be restored."). In further addition, the OMAP CPU is similarly adapted when removing power from the NEON cores.

41. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

COUNT VI: INFRINGEMENT OF THE '195 PATENT BY SVTRONICS

42. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

43. Upon information and belief, SVTronics has infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the products identified in Attachment B ("Accused SVTronics Products").

44. For example, on information and belief, SVTronics has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. On information and belief, the Accused SVTronics Products include Texas Instruments Inc.'s (TI's) AM437x platform. *See, e.g.*, Ex. 22, SVTronics AM437x boards (retrieved from svtronics.com/am4). On information and belief, the AM437x platform includes an ARM Cortex-A9 Core, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.*, Ex. 1, AM437x Datasheet. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. In performing the method of claim 6, a processing core received an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller) or an address channel of a bus. The Accused

SVTronics Products compared the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." *Id.,* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller. When a match between the received address and a matching address stored in a one of the latches occurred, the Accused SVTronics Products performed the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." *Id.* When a match between the received address and an address stored in one of the latches did not occur, the Accused SVTronics Products performed the substeps of exchanging data between a location in the memory array addressed by the received address and a selected one of the registers. "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." Ex. 4, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. When the match did not occur, the Accused SVTronics Products further stored the received address in one of the latches corresponding to the selected register. For example, the Accused SVTronics Products stored the received address, such as the tag, corresponding to the register being accessed, in the cache memory system latches, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches. *See* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. The Accused SVTronics

Products further modified the received address to generate a modified address. For example, the hardware in the Accused SVTronics Products prefetches, for example, data stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 7.6.2 Data prefetching. *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher ("[P]refetch address = current address + (stride x programmed distance."). On information and belief, the Accused SVTronics Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused SVTronics Products further exchanged data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." *See* Ex. 4 ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. The Accused SVTronics Products then stored the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stored the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches.

45. Upon information and belief, SVTronics has committed the foregoing infringing activities without a license.

COUNT VII: INFRINGEMENT OF THE '576 PATENT BY SVTRONICS

46. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

47. Upon information and belief, SVTronics has infringed, and continues to infringe, the ’576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused SVTronics Products identified in Attachment B.

48. For example, on information and belief, SVTronics has infringed at least claim 25 of the ’576 Patent by performing steps of an energy-conserving operating system. On information and belief, the Accused SVTronics Products include TI’s AM437x platform. *See, e.g.,* Ex. 22, SVTronics AM437x boards (retrieved from svtronics.com/am4). On information and belief, the AM437x platform, includes an ARM Cortex-A9 Core, and performs the steps of claim 25 of the ’576 Patent. *See, e.g.,* Ex. 1, AM437x Datasheet. “Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power.” Ex. 7, ARM Cortex-A Series Version: 4.0 Programmer’s Guide, Chapter 20 Power Management. The Accused SVTronics Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, the Accused SVTronics Products activate a set of interrupt-handling instructions for the generic interrupt controller in connection with handling an interrupt in a standby mode, caused by, among others, the issuance of the WFI (wait for interrupt) instruction executed by a core. Ex. 8, ARM Generic Interrupt Controller Architecture version 2.0, Architecture Specification, § 3.7 Pseudocode details of interrupt handling and prioritization. If detecting a power-up signal, the

Accused SVTronics Products power up to provide a main operation that utilizes main microprocessor circuitry and a set of main operating instructions. For example, when the main microprocessor circuitry, such as a core, is in the WFI low power state, an interrupt is detected by the generic interrupt controller, followed by powering up, such as enabling various clocks, to provide the main operation that utilizes that core and a set of main operating instructions, such as the instructions of the executed code following the WFI instruction. "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: • An IRQ interrupt, even if the CPSR I-bit is set. • An FIQ interrupt, even if the CPSR F-bit is set. • An asynchronous abort. • A Debug Entry request, even if JTAG Debug is disabled. In the event of the core being woken by an interrupt when the relevant CPSR interrupt flag is disabled, the core will implement the next instruction after WFI." Ex. 9, ARM Cortex-A Series Version: 4.0 Programmer's Guide, Chapter 20.4 Power Management Assembly language power instructions. The Accused SVTronics Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, in the regular operating state, a WFI instruction detected by a core is a power-down signal. "Entry into WFI Standby mode is performed by executing the Wait For Interrupt instruction." Ex. 10 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 2.4.2 Cortex-A9 processor power control. If the WFI command is detected, the operating system places the system in the low-power WFI mode. "WFI and WFE Standby modes disable most of the clocks in a processor, while keeping its logic powered up. This reduces the power drawn to the static leakage current, leaving a tiny clock power overhead requirement to enable the device to wake up." *Id.* In the Accused SVTronics Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with

said main operating instructions. *Id.*

49. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

COUNT VIII: INFRINGEMENT OF THE '481 PATENT BY SVTRONICS

50. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

51. On information and belief, SVTronics has infringed, and continues to infringe the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating DDRxL and/or LPDDRx memories, including the Accused SVTronics Products.

52. For example, on information and belief, SVTronics infringes at least claim 16 of the '481 Patent by performing a method of accessing data. On information and belief, the Accused SVTronics Products, such as the OMAP5432EVM With COM8Q Connector and the SOM437X board, include DDRxL memory, such as DDR3L. *See* Ex. 23 OMAP5432 EVM With COM8Q Connector Specification (retrieved from svtronics.com/5432C). *See also* Ex. 11, AM572x Industrial Development Kit (IDK) Evaluation Module (EVM) Hardware User's Guide ("The part number for the DDR3L SDRAM memory used is MT41K256M16HA-125…"). *See* also Ex. 24, SVTronics SOM437x System-On-Module datasaheet. DDR3L memory included in the Accused SVTronics Products is a memory system comprising multiple banks with multiple rows. "4Gb: x4, x8, x16 DDR3L SDRAM Description," Ex. 12 at p. 13-14 ("Row addressing is denoted as A[*n*:0] . . . DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM."). The Accused SVTronics Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id.* at p. 12 ("The address bits registered coincident with the ACTIVATE command are used to select the

bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access."). In SVTronics' DDR3L memory, the memory locations of the first memory row are disposed upon a substrate. *See* Ex. 11 ("The package used is the 96-ball TFBGA package."). The Accused SVTronics Products access the data stored at the memory locations identified in the first access request. Ex. 12. While the data stored at the memory locations identified by the first access request is being accessed, the Accused SVTronics Products generate a second access request for accessing data stored at memory locations of a second memory row. For example, in a burst read operation, while data from the previous access request is being accessed, the subsequent requests access data stored in different rows of another bank. *See id.* at 12 ("As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time."). In the Accused SVTronics Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. *See, e.g.*, Exs. 11-12. The Accused SVTronics Products also access the data stored at the memory locations identified in the second access request. *Id.*

53. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

COUNT IX: INFRINGEMENT OF THE '469 PATENT BY SVTRONICS

54. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

55. On information and belief, SVTronics has infringed, and continues to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products

incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused SVTronics Products identified in Attachment B.

56. For example, on information and belief, SVTronics infringes at least claim 14 of the '469 by making, using, selling, or offering to sell in the United States, or importing into the United States the Accused SVTronics Products, which are computer systems. On information and belief, the Accused SVTronics Products include, for example, TI's AM437x platform. *See, e.g.*, Ex. 22, SVTronics AM437x boards (retrieved from svtronics.com/am4). On information and belief, AM437x devices include a processor, such as the microprocessor unit (MPU) subsystem. *See* Ex. 13 AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 3.1 Introduction at 151. The Accused SVTronics Products include a first memory, such as one or more L1 caches, accessible by said processor (the MPU subsystem). *Id*. On information and belief, the Accused SVTronics Products also include a second memory, on-chip memory RAM (OCM-RAM) accessible only to said processor. *Id*. OCM-RAM is internal to said processor, the MPU subsystem. *Id*. On information and belief, in the Accused SVTronics Products, power to said second memory is controlled separately from power to said processor and to said first memory, wherein power is maintained to said second memory (OCM-RAM) when power is removed from said processor (the MPU subsystem). For example, in the DeepSleep power mode, the MPU power domain, PD_MPU is OFF (except MPU OCM RAM retained). *See* Ex. 14, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.4.3 Power Modes at 256. On information and belief, in the Accused SVTronics Products, the second memory is for maintaining internal context of said processor when power is removed from said processor. In the example of the DeepSleep power mode, "In addition, power to OCMC RAM is maintained to preserve information internally during DeepSleep." *Id*., § 6.4.3.3 DeepSleep at 257. On

information and belief, the Accused SVTronics Products also include a third memory external to said processor and accessible only to said processor. For example, the Accused SVTronics Products include various L3 memories, some of which are external to the MPU subsystem but accessible only by the MPU subsystem. *See* Ex. 13, § 3.1 Introduction at 151; See, e.g., Ex. 15, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 2.1.1 at 140, fn. 1 ("The first 1MB of address space 0x0-0xFFFFF is inaccessible externally.") On further information and belief, certain memories containing bootcode and other sensitive and/or secure information, including High Security and/or Trustzone based memories, are also external to the MPU but accessible only by the MPU. On information and belief, in the Accused SVTronics Products, the power to the third memory is controlled separately from power to said processor and to said first and second memories. For example, L3 memory belongs to the Peripheral power domain, PD_PER, which is separate from the MPU power domain, PD_MPU to which the MPU subsystem, the L1 cache, and the OCM-RAM belong. *See* Ex. 16, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.11 Device Modules and Power Management Attributes List at 298. In another example, the Accused SVTronics Products include a portion of L3 memory, the access to which is limited to high-security-enabled devices such as an A9 MPCore processor. On information and belief, in the Accused SVTronics Products, the power to the third memory, L3 memory and the high-security access portions within it, is controlled separately from power to said processor and to said first and second memories. *Id.*

57. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

COUNT X: INFRINGEMENT OF THE '330 PATENT BY SVTRONICS

58. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

59. On information and belief, SVTronics has infringed, and continues to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused SVTronics Products identified in Attachment B.

60. For example, on information and belief, SVTronics infringes at least claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused SVTronics Products, such as the OMAP5432EVM With COM8Q Connector or the Jorjin OMAP4460 Application Processor Modules include a central processing unit, such as a TI OMAP 4 or OMAP 5 processor. *See, e.g.*, Ex. 23. *See also* Ex. 17, OMAP 5432 EVM, Figure 1, OMAP5432 EVM Architectural Block Diagram. On information and belief, the OMAP 5432 CPU includes an ARM Cortex-A15 MPCore. *See* Ex. 18, OMAP5432 EVM, Chapter 2.3 OMAP5432 ES2.0 Processor. On information and belief, the OMAP 4 processor includes an ARM Cortex-A9 MPCore. On information and belief, CPUs in the Accused SVTronics Products execute the ARM 32-bit instruction set, Thumb 16-bit instruction set, and the Thumb 32-bit instruction set. *See* Ex. 19, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 4.2 The ARM instruction sets. On information and belief, the Accused SVTronics Products include one or more registers holding a state, such as the CPSR, R13, and R14 registers. *See* Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers. On information and belief, in the Accused SVTronics Products, the CPU, is adapted, upon executing a first instruction from said first instruction set (such as an instruction from an application in an A32,

T16, or T32 instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save said state in a memory without executing any additional instructions from said first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs) (*see, e.g.,* Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("Before entering Dormant mode, the architectural state of the Cortex-A15 processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")), and (ii) to initiate an action that may cause the state of said registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which renders the above registers undefined). *See, e.g.,* Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers at p. 3-8 ("The reset values of R0-R14 are unpredictable"). On information and belief, in the Accused SVTronics Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from said first instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example, by executing instructions from one of the other two instruction sets; such that, if the first instruction set is A32, instructions from T32 or A64 are executed upon exiting the dormant mode). *See, e.g.,* Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("To exit from Dormant mode to Run mode, the SoC must perform a full power-on reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the Cortex-A15 processor exits the power-on reset sequence, and the architectural state must be restored."). In further addition, the OMAP CPU is similarly adapted

when removing power from the NEON cores.

61. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

PRAYER FOR RELIEF

WHEREFORE, Complex Memory prays for the judgment in its favor against each of the Defendants, jointly, and severally, and specifically, for the following relief:

A. Entry of judgment in favor of Complex Memory against the Defendants on all counts;

B. Entry of judgment that the Defendants have infringed the Patent-in-Suit;

C. An order permanently enjoining the Defendants from infringing the Patent-in-Suit;

D. Award of compensatory damages adequate to compensate Complex Memory for the Defendants' infringement of the Patent-in-Suit, in no event less than a reasonable royalty as provided by 35 U.S.C. § 284;

E. Complex Memory's costs;

F. Pre-judgment and post-judgment interest on Complex Memory's award; and

G. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. Proc., Plaintiff hereby demands trial by jury in this action of all claims so triable.

Dated: October 13, 2017

Respectfully submitted,

/s/ Dmitry Kheyfits

Dmitry Kheyfits — Lead Counsel
New York State Bar No. 4743795
dkheyfits@kheyfits.com
Andrey Belenky
New York State Bar No. 4524898
abelenky@kheyfits.com
Hanna G. Cohen
(*Pro Hac Vice* motion to be filed)
hgcohen@kheyfits.com
New York State Bar No. 4471421
KHEYFITS P.C.
1140 Avenue of the Americas
9th Floor
New York, New York 10036
Tel. (212) 203-5399
Fax. (212) 203-6445

Jeffrey G. Toler
(*Pro Hac Vice* motion to be filed)
jtoler@tlgiplaw.com
Craig S. Jepson, SBN 24061364
cjepson@tlgiplaw.com
TOLER LAW GROUP, PC
8500 Bluffstone Cove
Suite A201
Austin, TX 78759
(512) 327-5515

/s/ L. Charles van Cleef
L. Charles van Cleef TX SB #00786305
Van Cleef Law Office
PO Box 2432
Longview, TX 75606-2432
Telephone: (903) 248-8244
Facsimile: (903) 248-8249
charles@vancleef.pro

Attorneys for Plaintiff Complex Memory, LLC