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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

POLARIS INNOVATIONS LTD., an Ireland limited company, Plaintiff, v. ETRON TECHNOLOGY, INC., a Taiwan corporation, and ETRON TECHNOLOGY AMERICA, INC., a California corporation Defendants.	No. **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

Polaris Innovations Limited ("Polaris") files this Complaint against Etron Technology, Inc. ("Etron") and Etron Technology America, Inc. ("ETA"), for their infringement of United States Patents 6,653,882 B2, 6,728,143 B2, 7,532,523 B2, and 7,405,992 B2. Polaris alleges as follows:

PARTIES

1. Polaris is a limited company organized and existing under the laws of the Republic of Ireland, with its principal place of business at 29 Earlsfort Terrace, Dublin 2, Republic of Ireland.

2. Etron is a corporation organized and existing under the laws of Taiwan, with its principal place of business at No. 6, Technology Road 5, Hsinchu Science Park, Hsinchu, Taiwan 30078.

3. ETA is a corporation organized and existing under the laws of the State of California, with its principal place of business at 3375 Scott Blvd, Santa Clara, CA 95054. Upon information and belief, ETA is a wholly owned subsidiary of Etron.

JURISDICTION

4. Polaris brings this action under the patent laws of the United States, 35 U.S.C. § 1 *et. seq*. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331, 1332(a)(2), and 1338(a).

VENUE

5. Etron has sold, offered to sell, and used in this District, products that practice or embody one or more claims of each of the patents in suit, as discussed more fully herein. Etron's website describes ETA as one of the "sales offices" in this District from which it sells computer memory products, including DDR3 synchronous dynamic random access memory ("SDRAM"), which infringes the patents in suit. ETA's location in Santa Clara, California is a regular and established place of business in this District. Venue is proper in this District under 28 U.S.C. §§ 1391(c) and 1400(b).

INTRADSTRICT ASSIGNMENT

6. This is an Intellectual Property Action pursuant to Local Rule 3-2(c).

THE PATENTS IN SUIT

7. On November 25, 2003, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,653,882 B2 ("'882 Patent"), which is entitled "Output Drivers for IC," and identifies Arindam Raychaudhuri as the sole inventor. A true and correct copy of the '882 Patent is attached hereto as Exhibit A. The '882 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '882 Patent, including the right to collect and receive damages for past, present and future infringement of the '882 Patent.

8. On April 27, 2004 the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,728,143 B2 ("the '143 Patent"), which is entitled "Integrated Memory," and identifies Robert Feurle as the sole inventor. A true and correct copy of the '143 Patent is attached hereto as Exhibit B. The'143 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '143 Patent, including the right to collect and receive damages for past, present and future infringement of the '143 Patent.

9. On May 12, 2009 the United States Patent and Trademark Office duly and legally issued United States Patent No. 7,532,523 B2 ("the '523 Patent"), which is entitled "Memory Chip With Settable Termination Resistance Circuit," and identifies Georg Braun, Christian Weis, and Eckehard Plaettner as inventors. A true and correct copy of the '523 Patent is attached hereto as Exhibit C. The '523 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '523 Patent, including the right to collect and receive damages for past, present and future infringement of the '523 Patent.

10. On July 29, 2008 the United States Patent and Trademark Office duly and legally issued United States Patent No. 7,405,992 B2 ("the '992 Patent"), which is entitled "Method and Apparatus For Communicating Command And Address Signals" and identifies Jong-Hoon Oh as the sole inventor. A true and correct copy of the '992 Patent is attached hereto as Exhibit D. The'992 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '992 Patent, including the right to collect and receive damages for past, present and future infringement of the '992 Patent.

11. The ’882 Patent discloses inventions related to integrated circuit devices including, for example, SDRAM devices used in personal computer systems, among other products. The inventions of the ’882 Patent generally are directed to a novel output driver circuit that improves data transfer speeds from an integrated circuit to other circuits in a computer system. The ’143 Patent discloses inventions related to integrated memory devices such as SDRAM that can be used in personal computer systems and other products. The inventions of the ’143 Patent generally are directed to improving memory access times, and thus the operating speed of a memory device, by employing a novel control circuit for performing memory accesses. The ’523 Patent discloses inventions related to integrated memory devices such as SDRAM that can be used in personal computer systems and other products. The inventions of the ’523 Patent generally are directed to a novel memory chip that optimally sets terminations at a terminal of the memory chip by variably setting the terminations in accordance with the claims of the ’523 Patent. The ’992 Patent discloses inventions related to integrated circuits devices, including, for example, SDRAM devices used in personal computer systems, among other products. The inventions of the ’992 Patent generally are directed at a novel device that utilizes pins that are capable of carrying both command and address signals.

12. The usefulness and value of the patents in suit has been acknowledged by various companies engaged in the design, manufacture, and sale of SDRAM devices. Polaris has widely licensed the patents in suit to numerous SDRAM manufacturers, among others, some of which compete with Etron for sales of SDRAM devices.

13. Etron designs, and sells throughout the world, including in the United States, SDRAM products such as those described herein. On information and belief, Etron sells its infringing SDRAM products to customers in the United States, either directly or through ETA, its United States sales subsidiary. On information and belief, from its offices in Santa Clara and elsewhere, ETA sells to customers in the United States products that infringe the ’882, ’143, ’523, and ’992 Patents.

14. Polaris has offered to license at least 3 of the patents in suit to Etron. Polaris has engaged in numerous discussions with Etron, through correspondence and in person and

telephonic meetings spanning several months, but Etron has not agreed to license the patents in suit despite several good-faith offers from Polaris. Polaris has therefore been compelled to file this suit to protect its rights.

FIRST CLAIM FOR RELIEF

Infringement of U.S. Patent No. 6,653,882

15. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14, inclusive, as if set forth in full herein.

16. Etron and ETA have infringed, and continue to infringe, at least claims 1 and 4 of the '882 Patent. Etron and ETA use, sell, or offer to sell in the United States, products, such as DDR3L SDRAM, including EM6HE08EW8C DDR3L SDRAM ("Etron DDR3 SDRAM"), that meet each and every limitation of claim 1.

17. Claim 1 of the '882 Patent is directed to an output driver for an integrated circuit. The output driver comprises:

a. a driver circuit for driving an external circuit, the driver circuit having:

i. a data input connected to the integrated circuit;

ii. a data output connected to a transmission line leading to the external circuit;

iii. and an impedance adjusting means for adjusting the output impedance of the driver circuit according to impedance adjusting data;

b. a dummy circuit comprising a dummy driver circuit and a dummy transmission line, the dummy driver circuit and the dummy transmission line being electrical replicas of the driver circuit and the transmission line, respectively;

c. and an impedance control circuit for controlling the output impedance of the driver circuit, the impedance control circuit being connected to the dummy circuit and the impedance adjusting means,

i. wherein the impedance control circuit is configured to control the impedance of the driver circuit by determining the impedance adjusting data necessary for matching the output impedance

of the dummy driver circuit to the impedance of the dummy transmission line and outputting the determined impedance adjusting data to the impedance adjusting means of the driver circuit, wherein the dummy driver circuit is a scaled down replica of the driver circuit.

18. The Etron DDR3 SDRAM meets each and every limitation of claim 1. For example, the Etron DDR3 SDRAM is an integrated circuit that contains an output driver for driving an external circuit. The output driver of the Etron DDR3 SDRAM includes a driver circuit, for example, a DQ Buffer, having a data input connected to the integrated circuit and a data output connected to a transmission line leading to the external circuit.

19. The Etron DDR3 SDRAM is capable of adjusting the output impedance of the driver circuit, and does so through an impedance adjusting means for adjusting the output impedance of the driver circuit according to impedance adjusting data. For example, the Etron DDR3 SDRAM adjusts the output impedance of the driver circuit using pull-up and pull-down resistors. The Etron DDR3 SDRAM also contains a dummy circuit comprising a dummy driver circuit and a dummy transmission line, the dummy driver circuit and the dummy transmission line are electrical replicas of the driver circuit and the transmission line, for example including the ZQ Cal module and the RZQ reference resistor of the Etron DDR3 SDRAM, respectively.

20. The Etron DDR3 SDRAM also contains an impedance control circuit for controlling the output impedance of the driver circuit, the impedance control circuit being connected to the dummy circuit and the impedance adjusting means. For example, the Etron DDR3 SDRAM uses the ZQ Calibration command to calibrate DRAM Ron values, corresponding to the output impedance of the driver circuit. The Etron DDR3 SDRAM further transfers calibrated values from the calibration engine to DRAM IO.

21. The Etron DDR3 SDRAM's use of ZQ Calibration indicates that the impedance control circuit of the Etron DDR3 SDRAM is configured to control the impedance of the driver circuit by determining the impedance adjusting data necessary for matching the output impedance of the dummy driver circuit to the impedance of the dummy transmission line and outputting the determined impedance adjusting data to the impedance adjusting means of the driver circuit. For

example, the Etron DDR3 SDRAM uses the ZQ Calibration command to calibrate DRAM Ron values, corresponding to the output impedance of the driver circuit. The Etron DDR3 SDRAM further transfers calibrated values from the calibration engine to DRAM IO. The dummy driver circuit is a scaled down replica of the driver circuit.

22. Claim 4 of the '882 patent depends on claim 1, and claims "The output driver according to claim 1, wherein the driver circuit is a push-pull on-chip current driver." The driver circuit of the Etron DDR3 SDRAM is a push-pull on-chip current driver.

23. Upon information and belief, other Etron products similarly infringe one or more claims of the '882 Patent. The specific part numbers of all Etron products that practice one or more claims of the '882 Patent are not presently known to Polaris. Polaris accuses of infringement all Etron products that contain features and functions similar to those described above that practice one or more claims of the '882 Patent.

24. Defendants have had notice of the '882 Patent and of their infringement of the '882 Patent for more than one year. Before initiating litigation, Polaris made substantial efforts to license Defendants' use of the inventions claimed in the '882 Patent, expecting that Defendants would engage in good faith licensing discussions. Defendants have refused to license the'882 Patent, and continue to infringe one or more claims of the '882 Patent despite being aware of their infringement of the '882 Patent on the basis of claim charts provided by Polaris. Defendants' infringement of the '882 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and continues to cause substantial damage to Polaris.

SECOND CLAIM FOR RELIEF

Infringement of U.S. Patent No. 6,728,143

25. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14, inclusive, as if set forth in full herein.

26. Etron and ETA have infringed, and continue to infringe, at least claims 1 and 2 of the '143 patent. Etron and ETA use, sell, or offer to sell in the United States, products, such as Etron DDR3 SDRAM that meet each and every limitation of claim 1.

27. Claim 1 of the ’143 Patent is directed to an integrated memory. The integrated memory comprises:

a. a memory cell array having memory cells;

b. a control circuit for controlling a memory access selected from the group consisting of a read memory access for reading out a data signal from one of said memory cells and a write memory access for writing a data signal into one of said memory cells;

c. for performing the memory access, said control circuit designed for receiving an access command selected from the group consisting of an activation command, a read command, and a write command;

d. for performing the memory access, said control circuit designed for receiving a configuration value in a combined manner with the access command; and

e. the configuration value being selected from the group consisting of a CAS latency value and a value for specifying a burst access.

28. Etron DDR3 SDRAM contains a memory cell array having memory cells. The Etron DDR3 SDRAM contains a control circuit for controlling read and write memory accesses, for example the command decoder, column counter, mode register, and control signal generator modules of the Etron DDR3 SDRAM. The control circuit of the Etron DDR3 SDRAM is designed to receive access commands in the form of activation commands, read commands (e.g., BC4, BL8), and write commands (e.g., BC4, BL8). The control circuit is further designed to receive a configuration value in a combined manner with the access command, *e.g.*, BC# values. The BC# configuration value received by the Etron DDR3 SDRAM is, for example, a value for specifying a burst access.

29. Claim 2 of the ’143 Patent is dependent upon Claim 1, and claims “The integrated memory according to claim 1, wherein: said control circuit is designed to receive a multi-bit signal that includes the access command and the configuration value.”

30. The control circuit of the Etron DDR3 SDRAM is designed to receive a multi-bit signal that includes the access command and the configuration value, including bits for CS#, RAS#, CAS#, WE#, A12/BC#.

31. Upon information and belief, other Etron products similarly infringe one or more claims of the '143 Patent. The specific part numbers of all Etron products that practice one or more claims of the '143 Patent are not presently known to Polaris. Polaris accuses of infringement all Etron products that contain features and functions similar to those described above that practice one or more claims of the '143 Patent.

32. Defendants have had notice of the '143 Patent and of their infringement of the '143 Patent for more than one year. Before initiating litigation, Polaris made substantial efforts to license Defendants' use of the inventions claimed in the '143 Patent, expecting that Defendants would engage in good faith licensing discussions. Defendants have refused to license the'143 Patent, and continue to infringe one or more claims of the '143 Patent despite being aware of their infringement of the '143 Patent on the basis of claim charts provided by Polaris. Defendants' infringement of the '143 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and continues to cause substantial damage to Polaris.

THIRD CLAIM FOR RELIEF

Infringement of U.S. Patent No. 7,532,523

33. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14, inclusive, as if set forth in full herein.

34. Etron and ETA have infringed, and continue to infringe, at least claims 1 and 2 of the '523 patent. Etron and ETA use, sell, or offer to sell in the United States, products, such as Etron DDR3 SDRAM that meet each and every limitation of claim 1.

35. Claim 1 of the '523 Patent is directed to memory chip. The memory chip comprises

a. a terminal;

b. a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

c. a control command port for receiving a control command signal for affecting accessibility of the memory chip;

d. a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

e. a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,

f. wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

36. Etron DDR3 SDRAM contains a terminal, for example, the DQ0 pin. The Etron DDR3 SDRAM contains a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value. The DQ0 pin is coupled to the DQ Buffer, which is configured to terminate the terminal according to a settable resistance value, such as RZQ/4 or RZQ/2. The Etron DDR3 SDRAM contains a control command port, for example in the command decoder, for receiving a control command signal for affecting accessibility of the memory chip, for example, the Mode Register Set signals. The Etron DDR3 SDRAM contains a control circuit, such as the control signal generator, mode register, and ZQ CAL modules, that is connected to the termination circuit. The control circuit is configured to set the resistance value as a function of the received control command signal, for example, resistance values such as RZQ/4 or RZQ/2. The Etron DDR3 SDRAM further contains a termination port, such as an ODT pin, to receive a termination signal. The control circuit is configured to selectively terminate the terminal with the set resistance value, e.g., RTT_NOM, in response to the termination signal. Furthermore, the control circuit of the Etron DDR3 SDRAM, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value (e.g.,

RTT_NOM) after a first time delay (e.g., ODTLon); and (ii) does not terminate the terminal in accordance with a second time delay (ODTLoff), the first time delay being sufficiently long to set the resistance value (e.g., ODTLon = CWL + AL – 2).

37. Claim 2 of the ’523 Patent is dependent upon Claim 1, and claims “The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time.”

38. The Etron DDR3 SDRAM is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value (e.g., RTT_WR) after a first predetermined switchover time (e.g., ODTLon) and is set to a second resistance value (e.g., RTT_NOM) after a second predetermined switchover time (e.g., ODTLoff).

39. Upon information and belief, other Etron products similarly infringe one or more claims of the ’523 Patent. The specific part numbers of all Etron products that practice one or more claims of the ’523 Patent are not presently known to Polaris. Polaris accuses of infringement all Etron products that contain features and functions similar to those described above that practice one or more claims of the ’523 Patent.

40. Defendants have had notice of the ’523 Patent and of their infringement of the ’523 Patent for more than one year. Before initiating litigation, Polaris made substantial efforts to license Defendants’ use of the inventions claimed in the ’523 Patent, expecting that Defendants would engage in good faith licensing discussions. Defendants have refused to license the ’523 Patent, and they continue to infringe one or more claims of the ’523 Patent despite being aware of its infringement of the ’523 Patent on the basis of claim charts provided by Polaris. Defendants’ infringement of the ’523 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and continues to cause substantial damage to Polaris.

FOURTH CLAIM FOR RELIEF

Infringement of U.S. Patent No. 7,405,992

41. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14,

inclusive, as if set forth in full herein.

42. Etron and ETA have infringed, and continue to infringe, at least claims 1 and 2 of the '992 patent. Etron and ETA use, sell, or offer to sell in the United States, products, such as the Etron EM6KA32HVAFA LPDDR2 SDRAM product ("Etron LPDDR2 SDRAM") that meet each and every limitation of claims 1 and 2.

43. Claim 1 of the '992 Patent claims a device, comprising:

a. a command bus interface comprising one or more command pins dedicated to receiving command inputs and one or more shared pins for selectively receiving address inputs and command inputs; and

b. an address bus interface comprising one or more address pins dedicated to receiving address inputs and one or more shared pins for selectively receiving address inputs and command inputs.

44. The Etron LPDDR2 SDRAM contains a command bus interface, for example, CKE, CS_N, CA0 and CA1 pins. The command bus interface comprises one or more command pins dedicated to receiving command inputs, for example the CKE and CS_N pins. The command bus interface also comprises one or more shared pins for selectively receiving address inputs and command inputs, for example the CA0 and CA1 pins.

45. The Etron LPDDR2 SDRAM contains an address bus interface, for example, CA2 – CA9 pins. The command bus interface comprises one or more command pins dedicated to receiving command inputs, for example the CA5 – CA9 pins. The address bus interface also comprises one or more shared pins for selectively receiving address inputs and command inputs, for example the CA2 – CA5 pins.

46. Claim 2 of the '992 Patent depends upon Claim 1, and claims "The device of claim 1, wherein the one or more shared pins of the address bus interface are communicatively coupled to an address decoder and a mode register." The shared pins of the address bus of the Etron LPDDR2 SDRAM (e.g., CA2, and CA3 pins) are communicatively coupled to an address decoder (e.g., through row address activation commands) and a mode register (e.g., through MRR commands)

47. Upon information and belief, other Etron products similarly infringe one or more claims of the '992 Patent. The specific part numbers of all Etron products that practice one or more claims of the '992 Patent are not presently known to Polaris. Polaris accuses of infringement all Etron products that contain features and functions similar to those described above that practice one or more claims of the '992 Patent.

WHEREFORE, Polaris prays that judgment be entered in its favor and against Etron and ETA as follows:

a. For damages in an amount according to proof, but no less than a reasonable royalty for infringement of the patents in suit;

d. For enhanced damages pursuant to 35 U.S.C. § 284;

e. For prejudgment and post-judgment interest as provided by law;

e. For costs of suit and reasonable attorneys' fees incurred herein; and

f. For such other relief as the Court deems proper.

Dated: November 10, 2017

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/s/Jason S. Angell
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DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Polaris demands a trial by jury on all issues so triable.

Dated: November 10, 2017

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